National Semiconductor

400160

National Products for Wireless Communications

PRODUCTS FOR WIRELESS COMMUNICATIONS

DATABOOK

1996 Edition

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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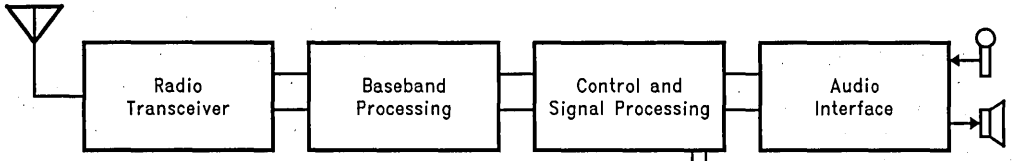
National Semiconductor

Personal Wireless Communication System

This data book collects into one complete reference National Semiconductor products that meet the needs of OEMs for the wireless industry. This data book includes existing products as well as some products that are in advanced design stages.

Future revisions of this data book will include new individual products as well as total system solutions for wireless communications.

The data book is organized around the seven blocks shown in the figure.



PHASE-LOCK-LOOPS
LMX1501A/LMX1511
LMX2314/LMX2315
LMX2301
LMX2305
LMX2320/LMX2325
LMX2330A/LMX2331A/LMX2332A
LMX2335/LMX2336/LMX2337

Single Chip Radio Transceiver
LMX3160

Low Noise Amplifiers
LMX2216B

Intermediate Frequency Receiver
LMX2240

Baseband Processor
LMX2411

Microcontrollers
COP8
COP472-3

Digital Speech Processor
NSAM265SR/NSAM265SF

Audio Amplifiers
LM4861

Non-Volatile Memory

NAND Flash
NM29N16
NM29A040

Low Voltage EEPROM
NM28C64/NM28C64L/NM28C64A
NM24C02L/NM24C04L/NM24C08L/NM24C16L
NM93C06L/NM93C46L/NM93C56L/NM93C66L

Support Circuitry

Operational Amplifiers
LMC7101
LMC7111
LMC7211
LMC6482
LMC6484
LM6142

Discrete Components
NDS351N
NDS352P
NDS355N
NDS356P

Power Management

Temperature Sensors
LM45B/LM45C
LM50B/LM50C

Voltage References
LM4040
LM4041

Low Dropout Voltage Regulators
LP2950/A-XX and LP2951/A-XX
LP2956
LP2960
LP2980
LP2952/LP2952A/LP2953/LP2953A

Switching Regulators
LM2574/LM2574HV
LM2594

Battery Charge Controller
LM3420

TL/XX/0240-1

Radio Transceiver

The PLLatinum™ phase-lock-loop product family consists of single and dual PLLs that operate up to 2.5 GHz. Each of the single and dual mode PLLatinum PLLs was designed with a dual modulus prescaler with 64/65 and 128/129 divide ratios available. PLLatinum PLLs generate a very stable low noise signal making them ideal for AMPS, DECT, GSM, IS-136, and IS-95. Because the PLLs were designed with wireless communication requirements in mind, their use can lead to significant savings in integration time.

The LMX3160 is a single chip transceiver solution for DECT applications. The LMX3160 transmitter includes a 1.1 GHz PLL, a frequency doubler, and a high frequency doubler. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency amplifier, a high gain limiting amplifier, a frequency discriminator and a received signal strength indicator (RSSI). The LMX3160's high level of integration and low current consumption make it ideal for DECT and PCS applications.

Baseband Processing

The LMX2240 Intermediate Frequency Receiver and the LMX2411 Baseband Processor are designed for use in DECT as well as other digital cellular telephone designs. The LMX2240 consists of a high gain limiting amplifier, a frequency discriminator, and a received signal strength indicator (RSSI). The LMX2240 supports single conversion receivers which reduces power requirements, size, and cost.

The LMX2411 contains both transmit and receive functions. The transmitter utilizes a low power high speed digital-to analog converter (DAC) and a mask programmable ROM to generate a Gaussian filter pulse shape. The receiver includes a high speed, low power voltage comparator with DC compensation.

Control and Signal Processing

The COP-8 family of microcontrollers offers a wide variety of RAM size, ROM size, UART and WATCHDOG™ functionality and interrupt sources. All COP-8 microcontrollers are based on the same CMOS process, use MICROWIRE™ serial communication, and have the same development tools which allow for significant reductions in design and integration time.

The NSAM265SF Digital Speech Processor with CompactSPEECH provides digital answering machine functionality by integrating a 16-bit RISC processor and a Digital Signal Processor (DSP) into one chip. CompactSPEECH implements voice compression and decompression, tone detection and generation, time and date stamp and other answering machine functions in firmware to reduce the cost and complexity associated with designing a digital answering machine.

Non-Volatile Memory

National Semiconductor has a complete line of low voltage EEPROM devices to meet the needs of the wireless communications market. All EEPROMs are designed using a 0.8 micron CMOS process that allows for access times as low as 100 ns with 3.0V operation.

The EEPROM family is a complete line of low voltage low power memory devices. With memory sizes between 2k and 16k and access times between 120 ns 200 ns.

Audio Interface

National Semiconductor's Boomer® family of audio products includes the LM4861 low voltage CMOS audio amplifier. The LM4861 is rated at 0.5W into 8Ω with less than 1% Total Harmonic Distortion (THD). With a voltage range of 2.7V to 5.5V, the LM4861 is ideal for low voltage wireless communication units.

Support Circuitry

The Tiny CMOS line of rail-to-rail operational amplifiers and the dual and quad rail-to-rail CMOS operational amplifiers in this book are ideal for mobile communications. The Tiny CMOS family provides rail-to-rail input and output, high open loop gain, and low distortion in a SOT 23-5 package. The dual and quad operational amplifiers provide multiple rail-to-rail input and output operational amplifiers and a high Common-Mode Voltage Range that make them unique and practical for wireless communication designs. This data book includes a listing of the SO-8 family of single and dual CMOS FETs as well as other N and P-channel FETs that are suited for wireless communication products.

Power Management

National Semiconductor's line of Temperature Sensors, Voltage References, and Low Drop Out Voltage Regulators are ideal for wireless applications. Precision Centigrade Temperature Sensors do not require calibration or trimming. Their accuracy, ±2°C at room temperature, low power, and their small packaging, SOT-23, make them ideal for wireless applications.

Precision Micropower Shunt Voltage References are available in a SOT-23 surface mount package. The LM4040 reduces design complexity by eliminating the need for any external stabilizing capacitor and by being available with several fixed reverse breakdown voltages between 2,500V and 10,000V.

National Semiconductor has a line Micropower Voltage Regulators. Micropower voltage regulators are available with fixed 3.0V, 3.3V and 5.0V outputs or with adjustable output voltages. The LP2950 line guarantees 100 mA output current while the LP2980 line guarantees 50 mA output current.

Complete Cordless Phone Solution

National Semiconductor has developed a CMOS chipset that includes all major functionality for 46/49 MHz cordless phones. The chipset offers OEMs a compact, low power cordless phone solution that significantly reduces time to market.

Section 1

Radio Transceiver Components

Section 1 Contents

National Semiconductor

LMX1501A/LMX1511 PLLatinum™ 1.1 GHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX1501A and the LMX1511 are high performance frequency synthesizers with integrated prescalers designed for RF operation up to 1.1 GHz. They are fabricated using National's ABiC IV BiCMOS process.

The LMX1501A and the LMX1511 contain dual modulus prescalers which can select either a 64/65 or a 128/129 divide ratio at input frequencies of up to 1.1 GHz. Using a proprietary digital phase locked loop technique, the LMX1501A/11's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Serial data is transferred into the LMX1501A and the LMX1511 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX1501A and the LMX1511 feature very low current consumption, typically 6 mA at 3V.

The LMX1501A is available in a JEDEC 16-pin surface mount plastic package. The LMX1511 is available in a TSSOP 20-pin surface mount plastic package.

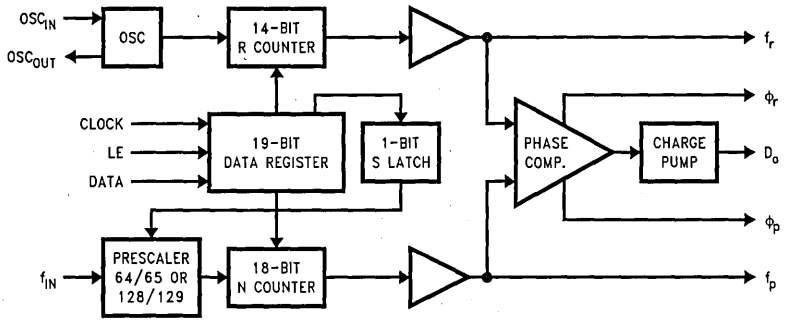
Features

- RF operation up to 1.1 GHz
- 2.7V to 5.5V operation
- Low current consumption: I_{CC} = 6 mA (typ) at V_{CC} = 3V
- Dual modulus prescaler: 64/65 or 128/129
- Internal balanced, low leakage charge pump
- Small-outline, plastic, surface mount JEDEC, 0.150" wide, (1501A) or TSSOP, 0.173" wide, (1511) package

Applications

- Cellular telephone systems (AMPS, NMT, ETACS)
- Portable wireless communications (PCS/PCN, Cordless)
- Advanced cordless telephone systems (CT-1/CT-1+, CT-2, ISM902-928)
- Other wireless communication systems

Block Diagram



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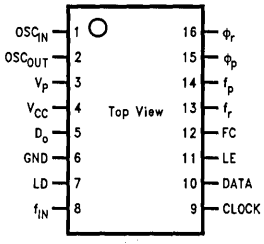
Connection Diagrams

LMX1501A



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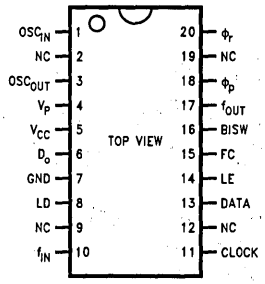
JEDEC 16-Lead (0.150" Wide) Small Outline Molded Package (M)
Order Number LMX1501AM or LMX1501AMX
See NS Package Number M16A

LMX1511



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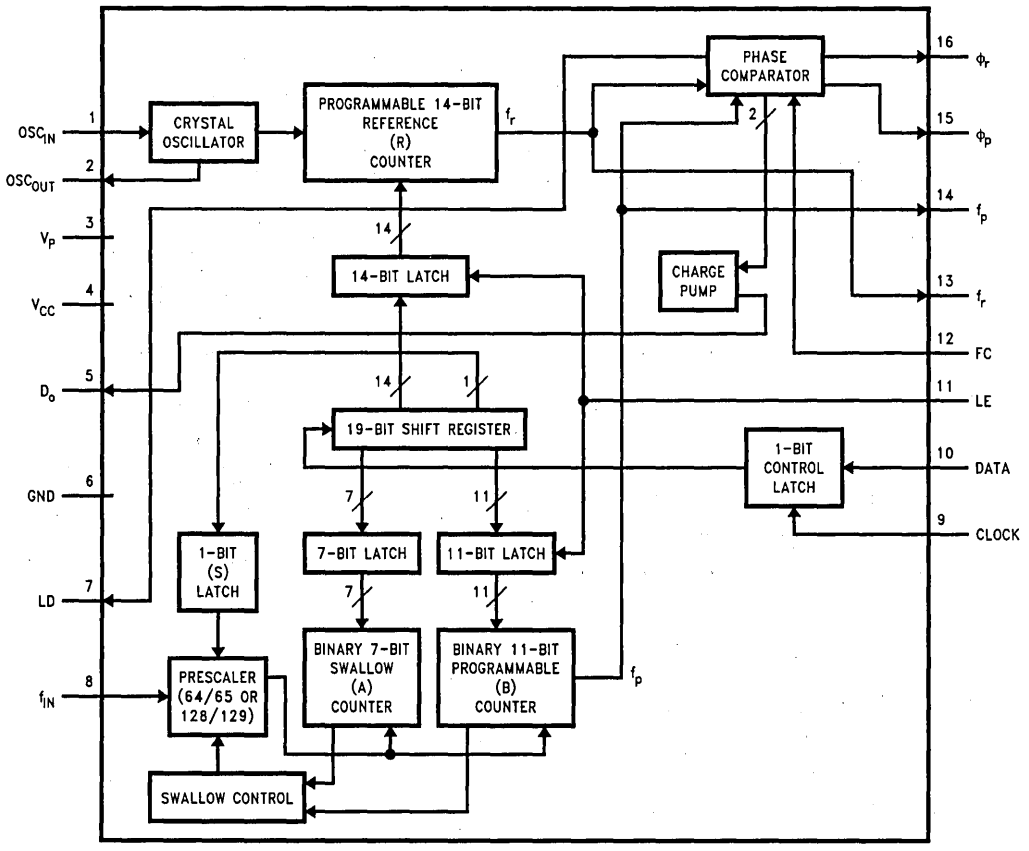
20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX1511TM or LMX1511TMX
See NS Package Number MTC20

Pin Descriptions

Pin No. 1501A	Pin No. 1511	Pin Name 1501A/1511	I/O	Description
1	1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
2	3	OSC_{OUT}	O	Oscillator output.
3	4	V_P		Power supply for charge pump must be $\geq V_{CC}$.
4	5	V_{CC}		Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
5	6	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
6	7	GND		Ground.
7	8	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in "lock". When the loop is locked, the pin's output is HIGH with narrow low pulses.
8	10	f_{IN}	I	Prescaler input. Small signal input from the VCO.
9	11	CLOCK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
10	13	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
11	14	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See Serial Data Input Timing Diagram.
12	15	FC	I	Phase control select (with internal pull-up resistor). When FC is LOW, the polarity of the phase comparator and charge pump combination is reversed.
X	16	BISW	O	Analog switch output. When LE is HIGH, the analog switch is ON, routing the internal charge pump output through BISW (as well as through D_o).
13		f_r	O	Monitor pin of phase comparator input. Programmable reference divider output.
14		f_p	O	Monitor pin of phase comparator input. Programmable divider output.
X	17	f_{OUT}	O	Monitor pin of phase comparator input. CMOS Output.
15	18	ϕ_p	O	Output for external charge pump. ϕ_p is an open drain N-channel transistor and requires a pull-up resistor.
16	20	ϕ_r	O	Output for external charge pump. ϕ_r is a CMOS logic output.
X	2,9,12,19	NC		No connect.

Functional Block Diagram

LMX1501A



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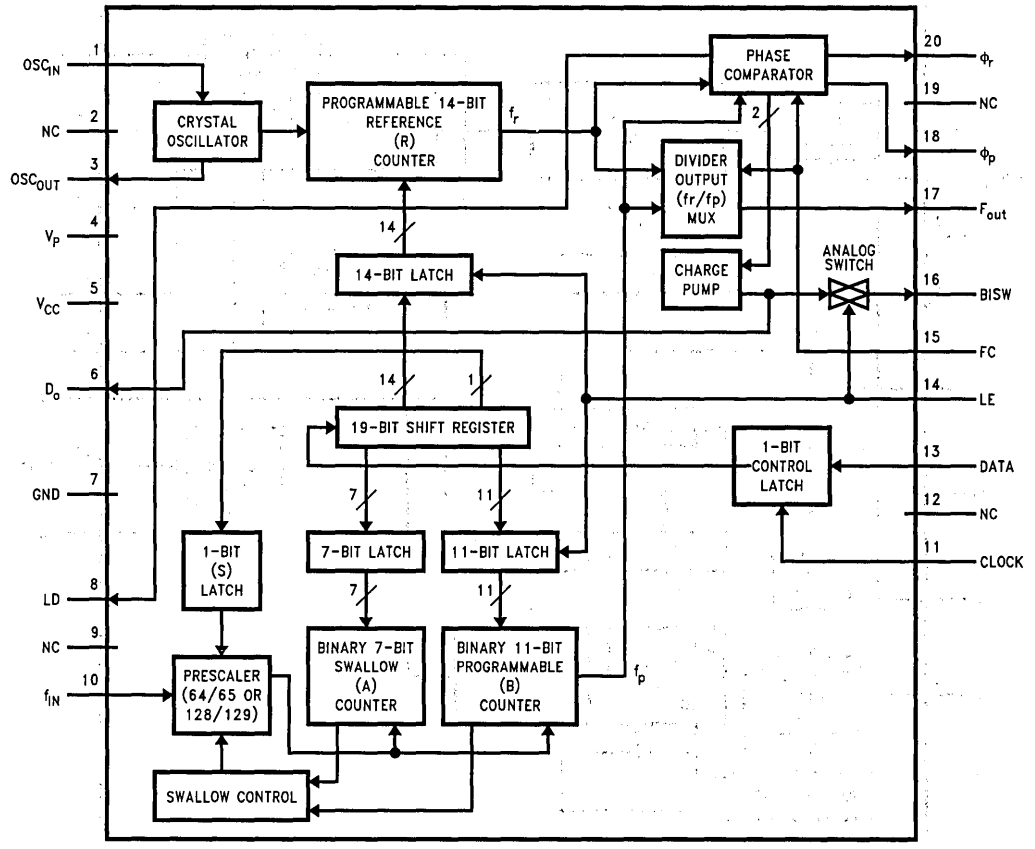
Functional Block Diagram (Continued)

LMX1511



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage
- V_{CC} −0.3V to +6.5V
- V_P −0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) −0.3V to +6.5V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (T_L) (solder, 4 sec.) +260°C

Recommended Operating Conditions

Power Supply Voltage
- V_{CC} 2.7V to 5.5V
- V_P V_{CC} to 5.5V

Operating Temperature (T_A) −40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = 3.0V		6.0	8.0	mA
		V_{CC} = 5.0V		6.5	8.5	mA
f_{IN}	Maximum Operating Frequency		1.1			GHz
f_{OSC}	Maximum Oscillator Frequency		20			MHz
f_ϕ	Maximum Phase Detector Frequency		10			MHz
Pf_{IN}	Input Sensitivity	V_{CC} = 2.7V to 5.5V	−10		+6	dBm
V_{OSC}	Oscillator Sensitivity	OSC_{IN}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage	*	0.7 V_{CC}			V
V_{IL}	Low-Level Input Voltage	*			0.3 V_{CC}	V
I_{IH}	High-Level Input Current (Clock, Data)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	μA
I_{IL}	Low-Level Input Current (Clock, Data)	V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	μA
I_{IH}	Oscillator Input Current	V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}		V_{IL} = 0V, V_{CC} = 5.5V	−100			μA
I_{IH}	High-Level Input Current (LE, FC)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	μA
I_{IL}	Low-Level Input Current (LE, FC)	V_{IL} = 0V, V_{CC} = 5.5V	−100		1.0	μA

*Except f_{IN} and OSC_{IN}

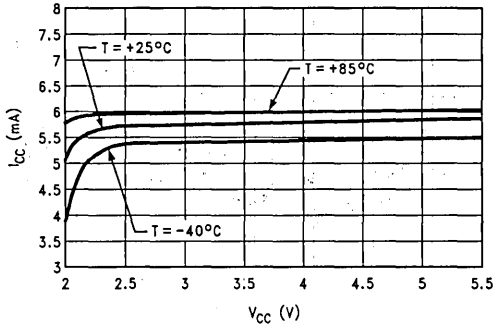
Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{D_O}-source	Charge Pump Output Current	$V_{D_O} = V_P/2$		−5.0		mA
I_{D_O}-sink		$V_{D_O} = V_P/2$		5.0		mA
I_{D_O}-Tri	Charge Pump TRI-STATE® Current	$0.5V \le V_{D_O} \le V_P - 0.5V$ T = 25°C	−5.0		5.0	nA
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA**	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA**			0.4	V
V_{OH}	High-Level Output Voltage (OSC_{OUT})	I_{OH} = −200 μA	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage (OSC_{OUT})	I_{OL} = 200 μA			0.4	V
I_{OL}	Open Drain Output Current (ϕ_P)	V_{CC} = 5.0V, V_{OL} = 0.4V	1.0			mA
I_{OH}	Open Drain Output Current (ϕ_P)	V_{OH} = 5.5V			100	μA
R_{ON}	Analog Switch ON Resistance (1511)			100		Ω
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

**Except OSC_{OUT}

Typical Performance Characteristics

I_{CC} vs V_{CC}



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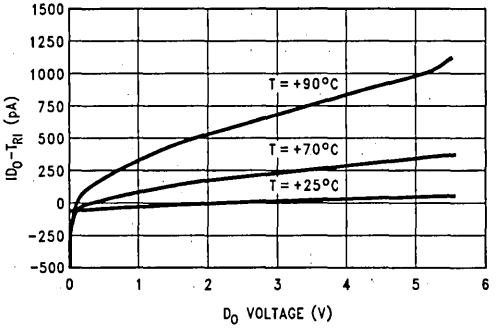
I_{D_O} TRI-STATE vs D_O Voltage



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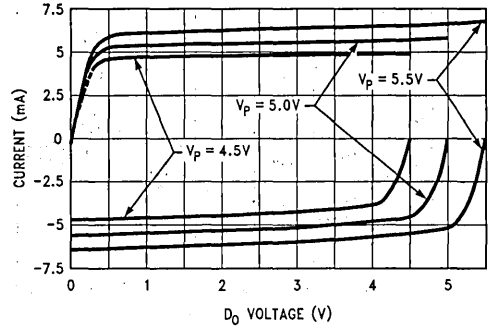
Charge Pump Current vs D_O Voltage



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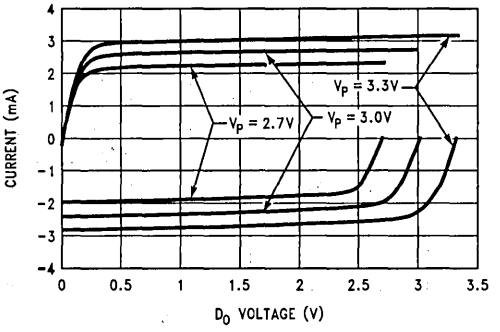
Charge Pump Current vs D_O Voltage



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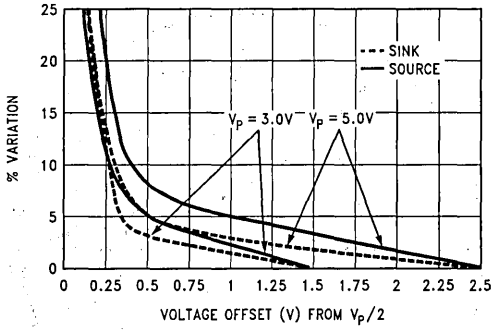
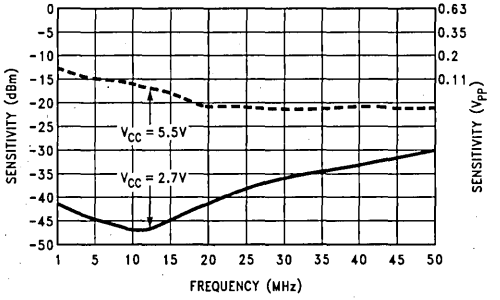
Charge Pump Current Variation



TL/W/12340-9

Oscillator Input Sensitivity



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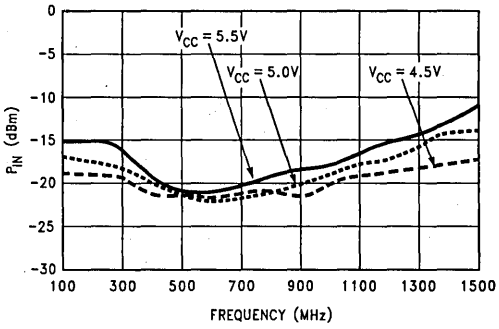
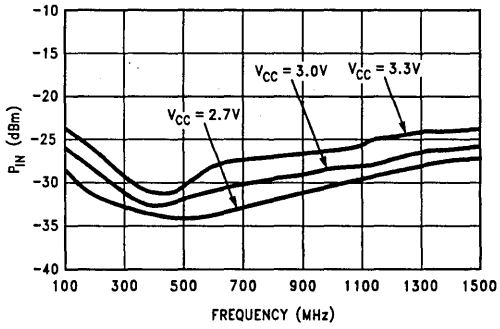
Typical Performance Characteristics (Continued)

Input Sensitivity vs Frequency



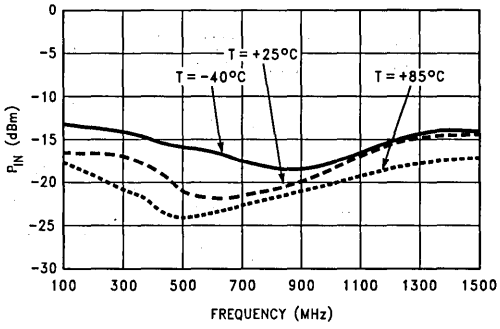
TL/W/12340–11

Input Sensitivity vs Frequency



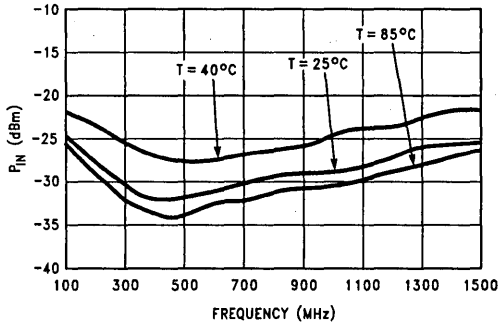
TL/W/12340–12

Input Sensitivity at Temperature Variation, V_{CC} = 5V



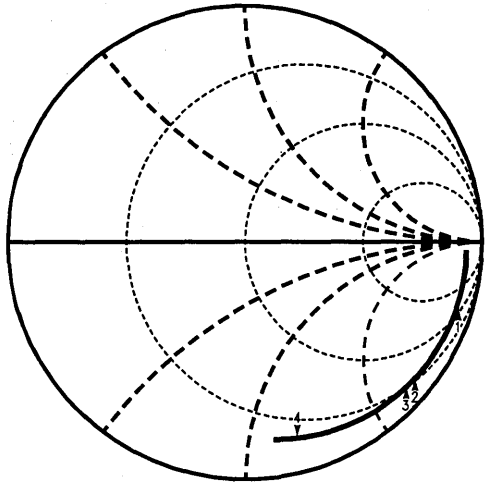
TL/W/12340–13

Input Sensitivity at Temperature Variation, V_{CC} = 3V



TL/W/12340–14

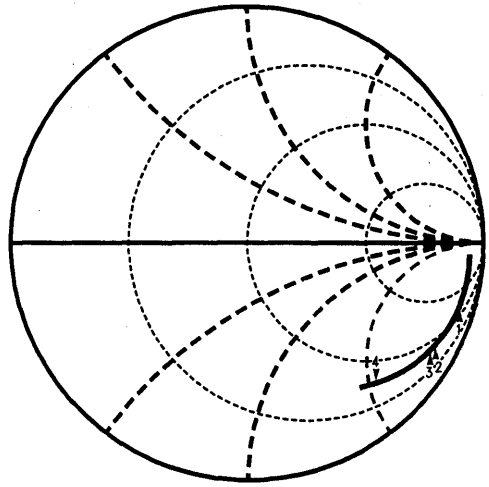
LMX1501A Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 100 MHz to 1,600 MHz



TL/W/12340–15

Marker 1 = 500 MHz, Real = 67, Imag. = −317
Marker 2 = 900 MHz, Real = 24, Imag. = −150
Marker 3 = 1 GHz, Real = 19, Imag. = −126
Marker 4 = 1,500 MHz, Real = 9, Imag. = −63

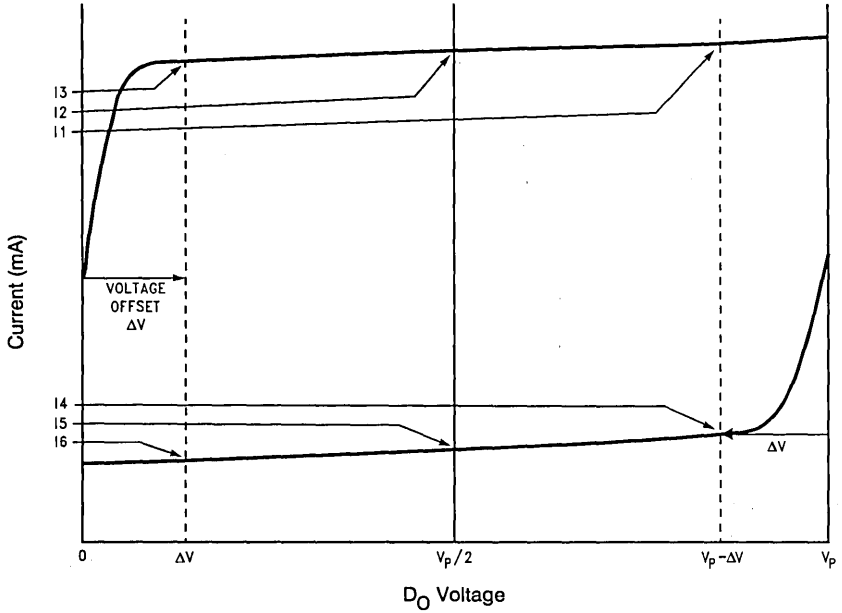
LMX1511 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 100 MHz to 1,600 MHz



TL/W/12340–16

Marker 1 = 500 MHz, Real = 69, Imag. = −330
Marker 2 = 900 MHz, Real = 36, Imag. = −193
Marker 3 = 1 GHz, Real = 35, Imag. = −172
Marker 4 = 1,500 MHz, Real = 30, Imag. = −106

Charge Pump Current Specification Definitions



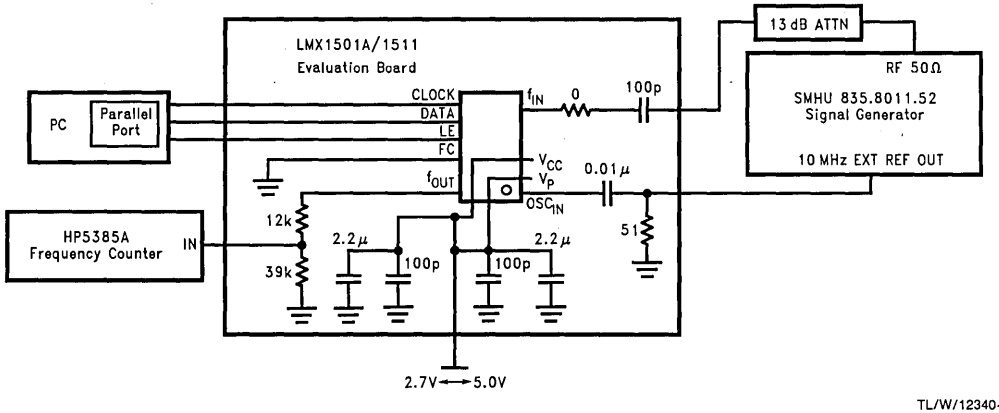
TL/W/12340–17

I1 = CP sink current at $V_{D_O} = V_P - \Delta V$
I2 = CP sink current at $V_{D_O} = V_P/2$
I3 = CP sink current at $V_{D_O} = \Delta V$
I4 = CP source current at $V_{D_O} = V_P - \Delta V$
I5 = CP source current at $V_{D_O} = V_P/2$
I6 = CP source current at $V_{D_O} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

1. I_{D_O} vs V_{D_O} = Charge Pump Output Current magnitude variation vs Voltage =
   $[\frac{1}{2} * |I1| - |I3|]/[\frac{1}{2} * \{|I1| + |I3|\}] * 100\%$ and $[\frac{1}{2} * |I4| - |I6|]/[\frac{1}{2} * \{|I4| + |I6|\}] * 100\%$
2. $I_{D_{O\text{-sink}}}$ vs $I_{D_{O\text{-source}}}$ = Charge Pump Output Current Sink vs Source Mismatch =
   $[|I2| - |I5|]/[\frac{1}{2} * \{|I2| + |I5|\}] * 100\%$
3. I_{D_O} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
   $[|I2 @ temp| - |I2 @ 25°C|]/|I2 @ 25°C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25°C|]/|I5 @ 25°C| * 100\%$
4. K_ϕ = Phase detector/charge pump gain constant = $\frac{1}{2} * \{|I2| + |I5|\}$

RF Sensitivity Test Block Diagram



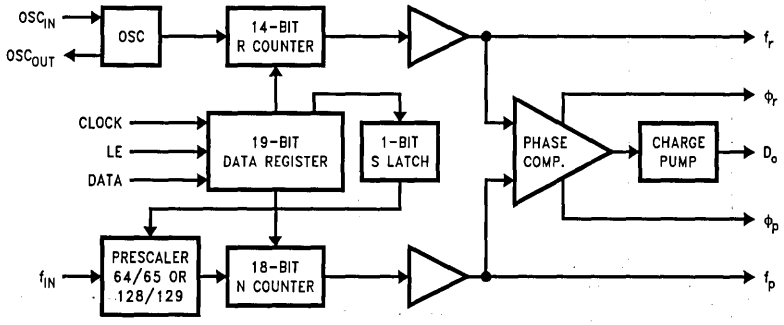
TL/W/12340–18

Note 1: N = 10,000 R = 50 P = 64

Note 2: Sensitivity limit is reached when the error of the divided RF output, f_{OUT}, is greater than or equal to 1 Hz.

Functional Description

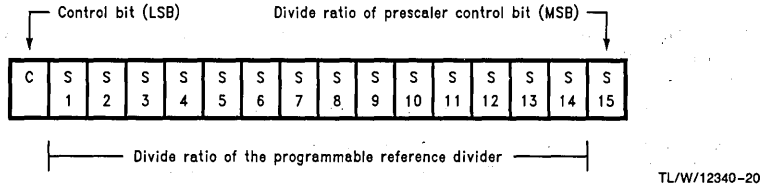
The simplified block diagram below shows the 19-bit data register, the 14-bit R Counter and the S Latch, and the 18-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (prescaler select: 64/65 or 128/129). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).



TL/W/12340-19

PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND PRESCALER SELECT (S LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit S Latch (S15, which sets the prescaler: 64/65 or 128/129). Serial data format is shown below.



TL/W/12340-20

14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 16383

S1 to S14: These bits select the divide ratio of the programmable reference divider.

C: Control bit (set to HIGH level to load R counter and S Latch)

Data is shifted in MSB first.

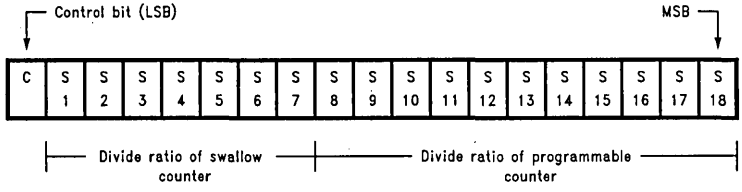
1-BIT PRESCALER SELECT (S LATCH)

Prescaler Select P	S 15
128/129	0
64/65	1

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into a 7-bit latch (which sets the 7-bit Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter). Serial data format is shown below.



TL/W/12340–21

Note: S8 to S18: Programmable counter divide ratio control bits (3 to 2047)

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio: 0 to 127
B ≥ A

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A \leq B$)

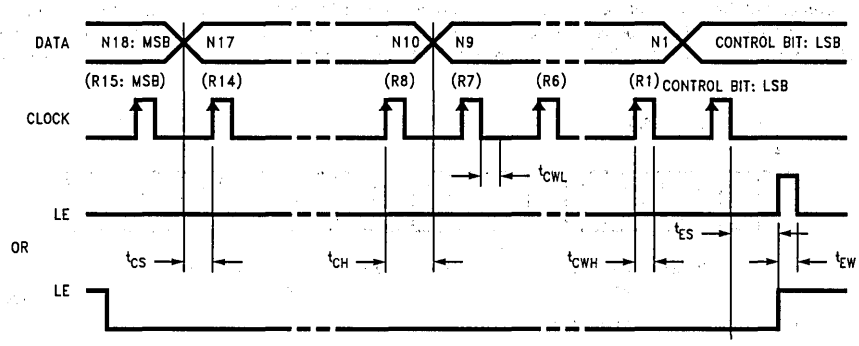
f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

P: Preset modulus of dual modulus prescaler (64 or 128)

Functional Description (Continued)

SERIAL DATA INPUT TIMING



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Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

Phase Characteristics

In normal operation, the FC pin is used to reverse the polarity of the phase detector. Both the internal and any external charge pump are affected.

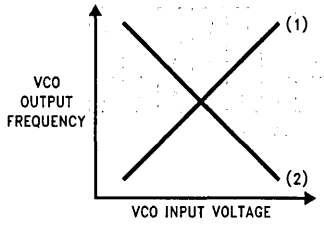
Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT;

When VCO characteristics are like (2), FC should be set LOW.

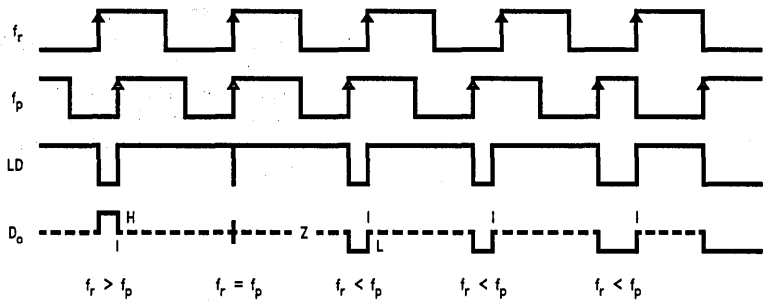
When FC is set HIGH or OPEN CIRCUIT, the monitor pin of the phase comparator input, f_{out}, is set to the reference divider output, f_r. When FC is set LOW, f_{out} is set to the programmable divider output, f_p.

VCO Characteristics



TL/W/12340–23

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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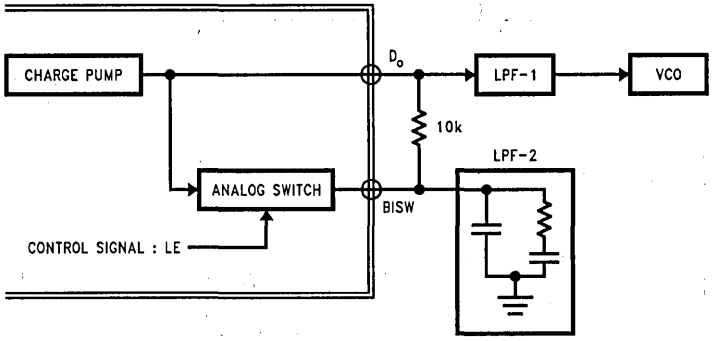
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

FC = HIGH

Analog Switch (1511 only)

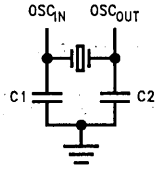
The analog switch is useful for radio systems that utilize a frequency scanning mode and a narrow band mode. The purpose of the analog switch is to decrease the loop filter time constant, allowing the VCO to adjust to its new frequency in a shorter amount of time. This is achieved by adding another filter stage in parallel. The output of the charge pump is normally through the D_O pin, but when LE is set HIGH, the charge pump output also becomes available at BISW. A typical circuit is shown below. The second filter stage (LPF-2) is effective only when the switch is closed (in the scanning mode).



TL/W/12340-25

Typical Crystal Oscillator Circuit

A typical circuit which can be used to implement a crystal oscillator is shown below.



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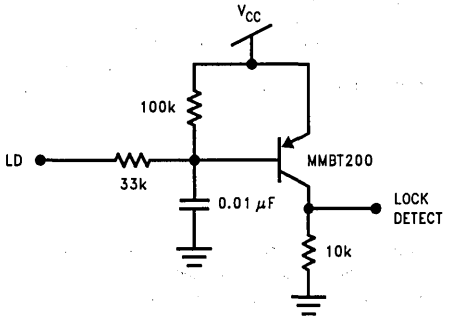
Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



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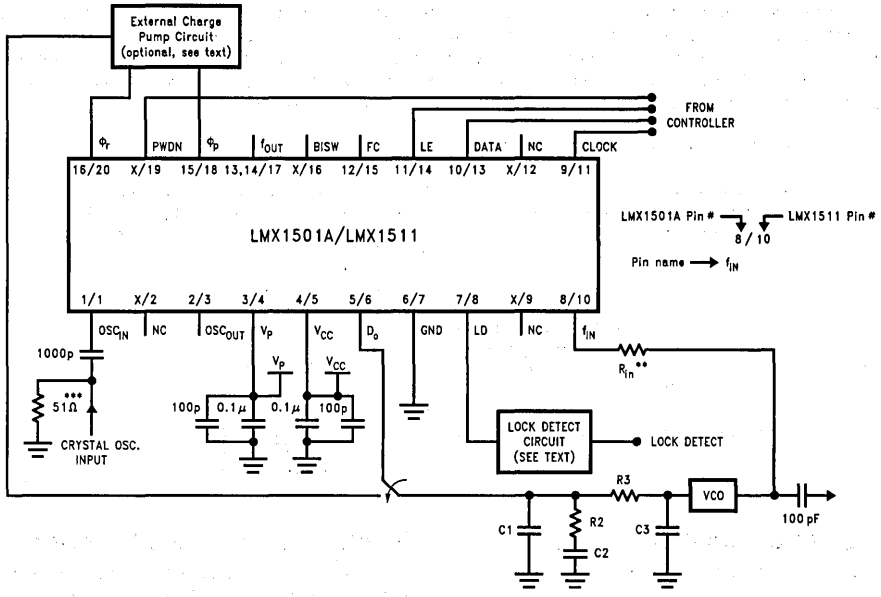
Typical Application Example



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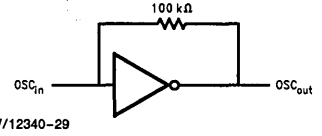
Operational Notes:

*VCO is assumed AC coupled.

**R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

***50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



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Proper use of grounds and bypass capacitors is essential to achieve a high level of performance.

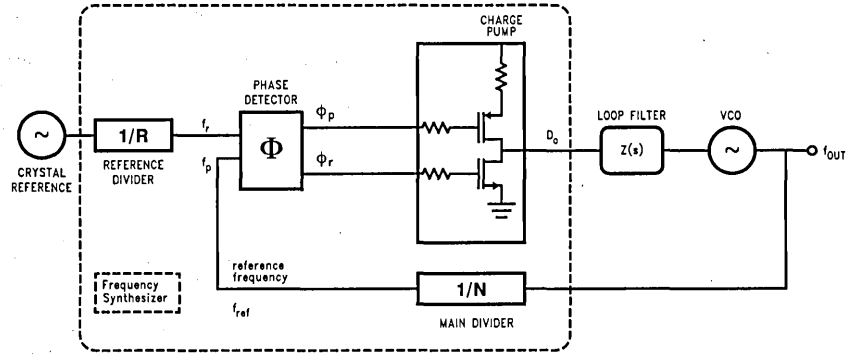
Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

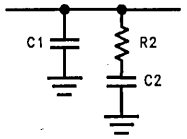
A block diagram of the basic phase locked loop is shown.



TL/W/12340-30

FIGURE 1. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in *Figure 2.*



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$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2}$$

FIGURE 2. 2nd Order Passive Filter

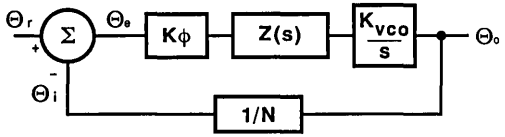
Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \qquad (1a)$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \qquad (1b)$$

The PLL linear model control circuit is shown along with the open loop transfer function in *Figure 3.* Using the phase detector and VCO gain constants [$K\phi$ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and $-180°$.



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Open Loop Gain $= \theta_i/\theta_e = H(s)\,G(s)$
$= K_\phi\,Z(s)\,K_{VCO}/Ns$

Closed Loop Gain $= \theta_o/\theta_i = G(s)/[1 + H(s)\,G(s)]$

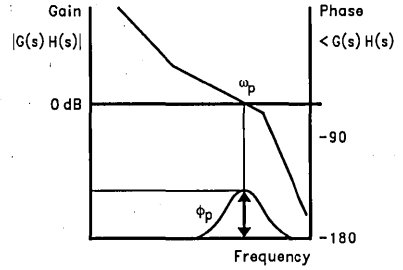

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FIGURE 3. Open Loop Transfer Function

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)\big|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \qquad (2)$$

From equation 2 we can see that the phase term will be dependent on the single pole and zero such that

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \qquad (3)$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \qquad (4)$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in equation 5.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \qquad (5)$$

For the loop to be stable the unity gain point must occur before the phase reaches -180 degrees. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \qquad (6)$$

Application Information (Continued)

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, ϕ_p, Equations 1 through 6 allow us to calculate the two time constants, T1 and T2, as shown in equations 7 and 8. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (8)$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 9 to 11.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (9)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \quad (10)$$

$$R2 = \frac{T2}{C2} \quad (11)$$

K_{VCO} (MHz/V) — Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

$K\phi$ (mA) — Phase detector/charge pump gain constant. The ratio of the current output to the input phase differential.

N — Main divider ratio. Equal to RF_{opt}/f_{ref}

RF_{opt} (MHz) — Radio Frequency output of the VCO at which the loop filter is optimized.

f_{ref} (kHz) — Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a trade off must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result.

THIRD ORDER FILTER

A low pass filter section may be needed for some applications that require additional rejection of the reference sidebands, or spurs. This configuration is given in *Figure 4.* In order to compensate for the added low pass section, the component values are recalculated using the new open loop unity gain frequency. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log[(2\pi f_{ref} \bullet R3 \bullet C3)^2 + 1] \quad (12)$$

Defining the additional time constant as

$$T3 = R3 \bullet C3 \quad (13)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}} \quad (14)$$

We then use the calculated value for loop bandwidth ω_c in equation 11, to determine the loop filter component values in equations 15–17. ω_c is slightly less than ω_p, therefore the frequency jump lock time will increase.

$$T2 = \frac{1}{\omega_c^2 \bullet (T1 + T3)} \quad (15)$$

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right] \quad (16)$$

$$C1 = \frac{T1}{T2} \bullet \frac{K_\phi \bullet K_{VCO}}{\omega_c^2 \bullet N} \bullet \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)}\right]^{1/2} \quad (17)$$

Application Information (Continued)

Example #1

K_{VCO} = 19.3 MHz/V
K_ϕ = 5 mA (Note 1)
RF_{opt} = 886 MHz
F_{ref} = 25 kHz
$N = RF_{opt}/f_{ref}$ = 35440
$\omega_p = 2\pi * 5$ kHz = 3.1415e4
ϕ_p = 43°
ATTEN = 10 dB

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} = 1.38e-5$$

$$T3 = \sqrt{\frac{10^{(10/20)} - 1}{(2\pi \bullet 25e3)^2}} = 9.361e-6$$

$$\omega_c = \frac{(\tan 43°)\bullet(1.38e-5 + 9.361e-6)}{[(1.38e-5 + 9.361e-6)^2 + 1.38e-5 \bullet 9.361e-6]} \bullet \left[\sqrt{1 + \frac{(1.38e-5 + 9.361e-6)^2 + 1.38e-5 \bullet 9.361e-6}{[(\tan 43°)\bullet(1.38e-5 + 9.361e-6)]^2}} - 1\right]$$

$$= 1.8101e4$$

$$T2 = \frac{1}{(1.8101e4)^2 \bullet (1.38e-5 + 9.361e-6)} = 1.318e-4$$

$$C1 = \frac{1.38e-5}{1.318e-4}\frac{(5e-3) \bullet 19.3e6}{(1.8101e4)^2 \bullet (35440)} \bullet \left[\frac{[1 + (1.8101e4)^2 \bullet (1.318e-4)^2]}{[1 + (1.8101e4)^2 \bullet (1.38e-5)^2]\,[1 + (1.8101e4)^2 \bullet (9.361e-6)^2]}\right]^{1/2}$$

$$= 2.153 \text{ nF}$$

$$C2 = 2.153 \text{ nF}\left(\frac{1.318e-4}{1.384e-5} - 1\right) = 18.35 \text{ nF}$$

$$R2 = \frac{1.318e-4}{18.35e-9} = 7.18 \text{ k}\Omega$$

if we choose R3 = 120k; then $C3 = \frac{9.361e-6}{120e3} = 78$ pF.

Converting to standard component values gives the following filter values, which are shown in *Figure 4*.

C1 = 2200 pF
R2 = 8.2 kΩ
C2 = 0.018 μF
R3 = 120 kΩ
C3 = 78 pF

Note 1: See related equation for K_ϕ in Charge Pump Current Specification Definitions. For this example V_P = 5.0V. The value for K_ϕ can then be approximated using the curves in the Typical Performance Characteristics for Charge Pump Current vs D_o Voltage. The units for K_ϕ are in mA. You may also use K_ϕ = (5 mA/2π rad), but in this case you must convert K_{VCO} to (rad/V) multiplying by 2π.

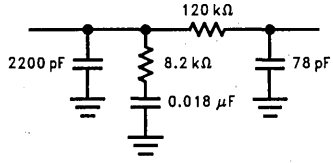

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FIGURE 4. ~5 kHz Loop Filter

Application Information (Continued)

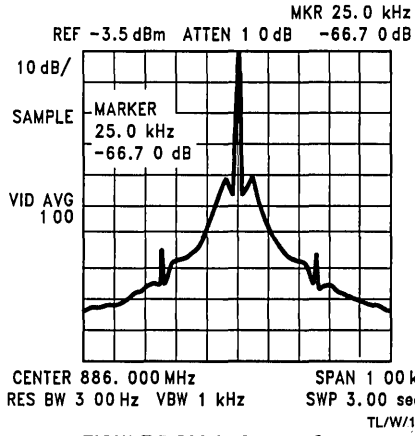

FIGURE 5. PLL Reference Spurs

The reference spurious level is < −66 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX1511.

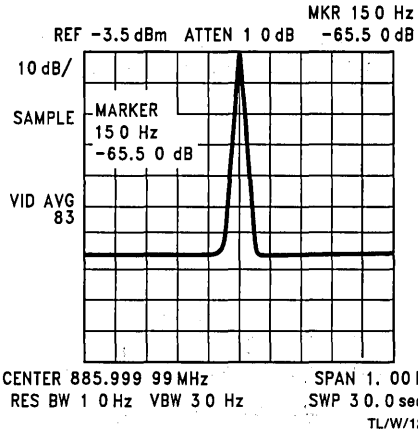

FIGURE 7. PLL Phase Noise @ 150 Hz Offset

The phase noise level at 150 Hz offset is −75.5 dBc/Hz.

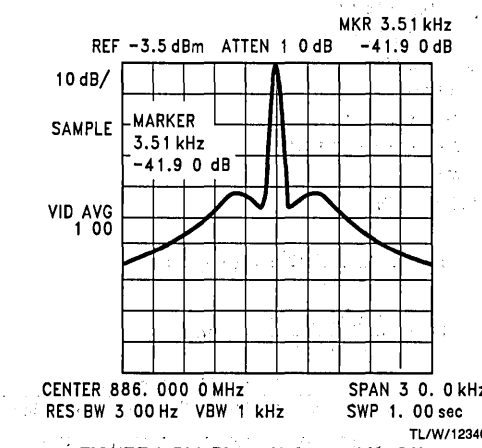

FIGURE 6. PLL Phase Noise 3.5 kHz Offset

The phase noise level at 3 kHz offset is −65 dBc/Hz.

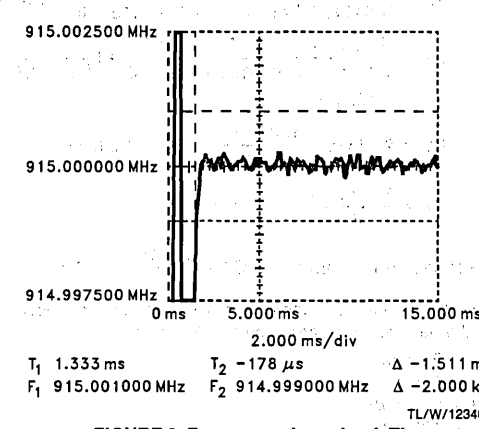

FIGURE 8. Frequency Jump Lock Time

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. *Figure 8* shows the switching waveforms for a frequency jump of 857 MHz–915 MHz. By narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±1 kHz. The lock time is seen to be < 1.6 ms for a frequency jump of 58 MHz.

Application Information (Continued)

EXTERNAL CHARGE PUMP

The LMX PLLatimum series of frequency synthesizers are equipped with an internal balanced charge pump as well as outputs for driving an external charge pump. Although the superior performance of NSC's on board charge pump eliminates the need for an external charge pump in most applications, certain system requirements are more stringent. In these cases, using an external charge pump allows the designer to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation.

One possible architecture for an external charge pump current source is shown in *Figure 9*. The signals ϕ_p and ϕ_r in the diagram, correspond to the phase detector outputs of the LMX1501/1511 frequency synthesizers. These logic signals are converted into current pulses, using the circuitry shown in *Figure 9*, to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

Referring to *Figure 9*, the design goal is to generate a 5 mA current which is relatively constant to within 5V of the power supply rail. To accomplish this, it is important to establish as large of a voltage drop across R5, R8 as possible without saturating Q2, Q4. A voltage of approximately 300 mV provides a good compromise. This allows the current source reference being generated to be relatively repeatable in the absence of good Q1, Q2/Q3, Q4 matching. (Matched transistor pairs is recommended.) The ϕp and ϕr outputs are rated for a maximum output load current of 1 mA while 5 mA current sources are desired. The voltages developed across R4, 9 will consequently be approximately 258 mV, or 42 mV < R8, 5, due to the current density differences {0.026*1n (5 mA/1 mA)} through the Q1, Q2/Q3, Q4 pairs.

In order to calculate the value of R7 it is necessary to first estimate the forward base to emitter voltage drop (Vfn,p) of the transistors used, the V_{OL} drop of ϕp, and the V_{OH} drop of ϕr's under 1 mA loads. (ϕp's V_{OL} < 0.1V and ϕr;s V_{OH} < 0.1V.)

Knowing these parameters along with the desired current allow us to design a simple external charge pump. Separating the pump up and pump down circuits facilitates the nodal analysis and give the following equations.

$$R_4 = \frac{V_{R5} - V_T \bullet 1n\left(\frac{i_{source}}{i_{p\,max}}\right)}{i_{source}}$$

$$R_9 = \frac{V_{R8} - V_T \bullet 1n\left(\frac{i_{sink}}{i_{n\,max}}\right)}{i_{sink}}$$

$$R_5 = \frac{V_{R5} \bullet (\beta_p + 1)}{i_{p\,max} \bullet (\beta_p + 1) - i_{source}}$$

$$R_8 = \frac{V_{R8} \bullet (\beta_n + 1)}{i_{r\,max} \bullet (\beta_n + 1) - i_{sink}}$$

$$R_6 = \frac{(V_p - V_{VOL\phi p}) - (V_{R5} + Vfp)}{i_{p\,max}}$$

$$R_7 = \frac{(V_P - V_{VOH\phi r}) - (V_{R8} + Vfn)}{i_{max}}$$

EXAMPLE

Typical Device Parameters	$\beta_n = 100$, $\beta_p = 50$
Typical System Parameters	$V_P = 5.0V$;
	$V_{cntl} = 0.5V - 4.5V$;
	$V_{\phi p} = 0.0V$, $V_{\phi r} = 5.0V$
Design Parameters	$I_{SINK} = I_{SOURCE} = 5.0$ mA;
	$V_{fn} = V_{fp} = 0.8V$
	$I_{rmax} = I_{pmax} = 1$ mA
	$V_{R8} = V_{R5} = 0.3V$
	$V_{OL\phi p} = V_{OH\phi r} = 100$ mV

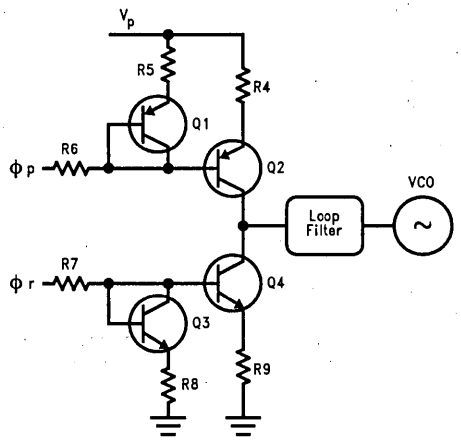

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FIGURE 9

Therefore select

$$R_4 = R_9 = \frac{0.3V - 0.026 \bullet 1n(5.0\text{ mA}/1.0\text{ mA})}{5\text{ mA}} = 51.6\Omega$$

$$R_5 = \frac{0.3V \bullet (50 + 1)}{1.0\text{ mA} \bullet (50 + 1) - 5.0\text{ mA}} = 332\Omega$$

$$R_8 = \frac{0.3V \bullet (100 - 1)}{1.0\text{ mA} \bullet (100 + 1) - 5.0\text{ mA}} = 315.6\Omega$$

$$R_6 = R_7 = \frac{(5V - 0.1V) - (0.3V + 0.8V)}{1.0\text{ mA}} = 3.8\text{ k}\Omega$$

National Semiconductor

LMX2314/LMX2315 PLLatinum™ 1.2 GHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2314 and the LMX2315 are high performance frequency synthesizers with integrated prescalers designed for RF operation up to 1.2 GHz. They are fabricated using National's ABiC IV BiCMOS process.

The LMX2314 and the LMX2315 contain dual modulus prescalers which can select either a 64/65 or a 128/129 divide ratio at input frequencies of up to 1.2 GHz. Using a proprietary digital phase locked loop technique, the LMX2314/15's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Serial data is transferred into the LMX2314 and the LMX2315 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2314 and the LMX2315 feature very low current consumption, typically 6 mA at 3V.

The LMX2314 is available in a JEDEC 16-pin surface mount plastic package. The LMX2315 is available in a TSSOP 20-pin surface mount plastic package.

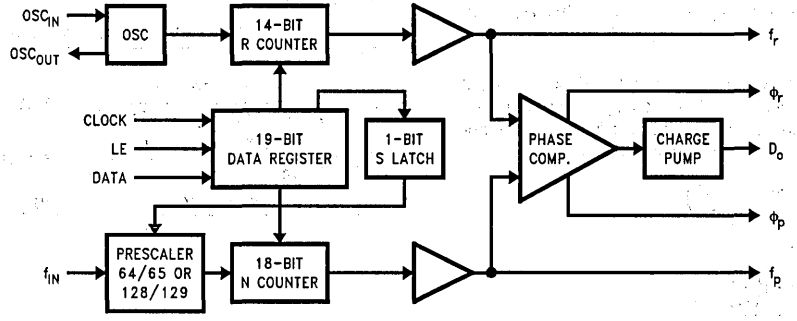
Features

- RF operation up to 1.2 GHz
- 2.7V to 5.5V operation
- Low current consumption: I_{CC} = 6 mA (typ) at V_{CC} = 3V
- Dual modulus prescaler: 64/65 or 128/129
- Internal balanced, low leakage charge pump
- Power down feature for sleep mode: I_{CC} = 30 μA (typ) at V_{CC} = 3V
- Small-outline, plastic, surface mount JEDEC, 0.150" wide, (2314) or TSSOP, 0.173" wide, (2315) package

Applications

- Cellular telephone systems (GSM, IS-54, IS-95, RCR-27)
- Portable wireless communications (DECT, ISM902-928 CT-2)
- Other wireless communication systems

Block Diagram



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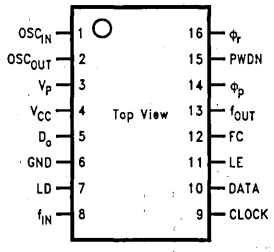
Connection Diagrams

LMX2314



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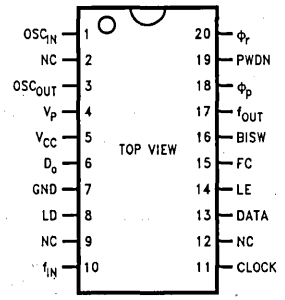
JEDEC 16-Lead (0.150" Wide) Small Outline Molded Package (M)
Order Number LMX2314M or LMX2314MX
See NS Package Number M16A

LMX2315



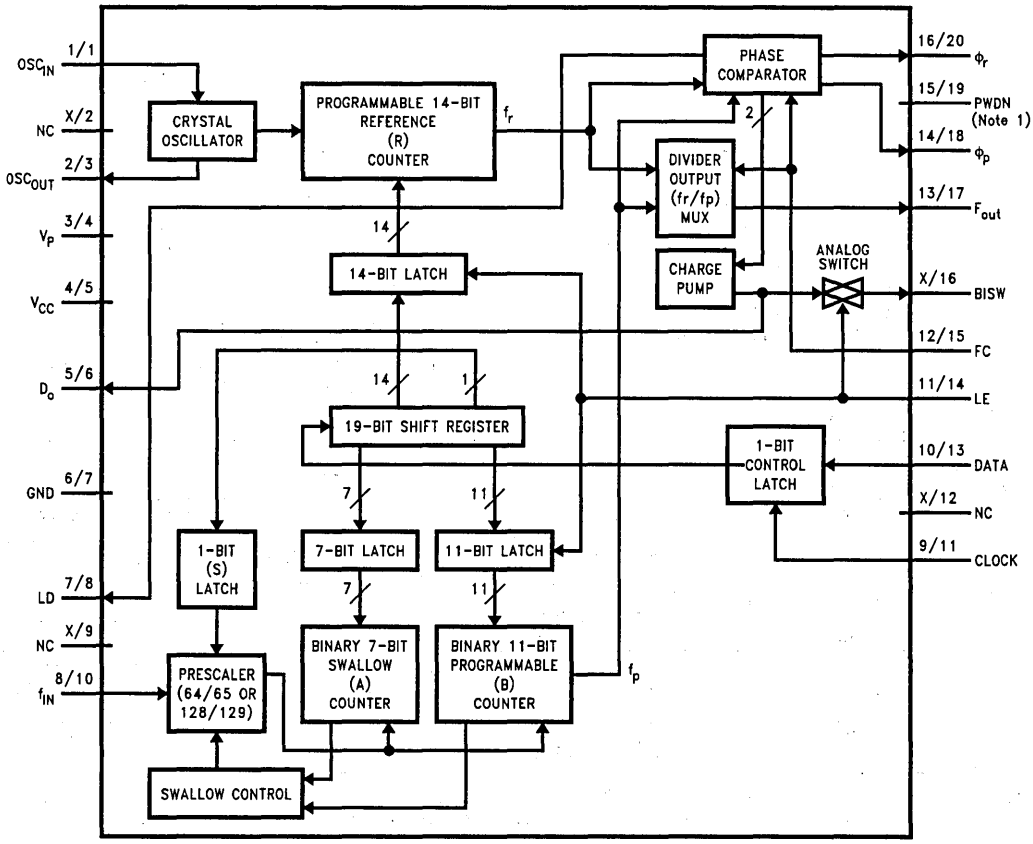
TL/W/11766-3

20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX2315TM or LMX2315TMX
See NS Package Number MTC20

Pin Descriptions

Pin No. 2314	Pin No. 2315	Pin Name 2314/2315	I/O	Description
1	1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
2	3	OSC_{OUT}	O	Oscillator output.
3	4	V_P		Power supply for charge pump. Must be $\geq V_{CC}$.
4	5	V_{CC}		Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
5	6	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
6	7	GND		Ground.
7	8	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in "lock". When the loop is locked, the pin's output is HIGH with narrow low pulses.
8	10	f_{IN}	I	Prescaler input. Small signal input from the VCO.
9	11	CLOCK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
10	13	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
11	14	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See Serial Data Input Timing Diagram.
12	15	FC	I	Phase control select (with internal pull-up resistor). When FC is LOW, the polarity of the phase comparator and charge pump combination is reversed.
X	16	BISW	O	Analog switch output. When LE is HIGH, the analog switch is ON, routing the internal charge pump output through BISW (as well as through D_o).
13	17	f_{OUT}	O	Monitor pin of phase comparator input. CMOS output.
14	18	ϕ_P	O	Output for external charge pump. ϕ_P is an open drain N-channel transistor and requires a pull-up resistor.
15	19	PWDN	I	Power Down (with internal pull-up resistor). PWDN = HIGH for normal operation. PWDN = LOW for power saving. Power down function is gated by the return of the charge pump to a TRI-STATE condition.
16	20	ϕ_r	O	Output for external charge pump. ϕ_r is a CMOS logic output.
X	2,9,12	NC		No connect.

Functional Block Diagram



LMX2314 Pin # — LMX2315 Pin #

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Pin Name → f_{IN}

X signifies a function not bonded out to a pin

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Note 1: The power down function is gated by the charge pump to prevent any unwanted frequency jumps. Once the power down pin is brought low the part will go into power down mode when the charge pump reaches a TRI-STATE condition.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage
- V_{CC} −0.3V to +6.5V
- V_P −0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) −0.3V to +6.5V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (T_L) (solder, 4 sec.) +260°C

Recommended Operating Conditions

Power Supply Voltage
- V_{CC} 2.7V to 5.5V
- V_P V_{CC} to +5.5V

Operating Temperature (T_A) −40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	V_{CC} = 3.0V		6.0	8.0	mA
		V_{CC} = 5.0V		6.5	8.5	mA
$I_{CC-PWDN}$	Power Down Current	V_{CC} = 3.0V		30	180	µA
		V_{CC} = 5.0V		60	350	µA
f_{IN}	Maximum Operating Frequency		1.2			GHz
f_{OSC}	Maximum Oscillator Frequency		20			MHz
		No Load on OSC Out	40			MHz
f_ϕ	Maximum Phase Detector Frequency		10			MHz
Pf_{IN}	Input Sensitivity	V_{CC} = 2.7V to 3.3V	−15		+6	dBm
		V_{CC} = 3.3V to 5.5V	−10		+6	
V_{OSC}	Oscillator Sensitivity	OSC_{IN}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage	*	0.7 V_{CC}			V
V_{IL}	Low-Level Input Voltage	*			0.3 V_{CC}	V
I_{IH}	High-Level Input Current (Clock, Data)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (Clock, Data)	V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	µA
I_{IH}	Oscillator Input Current	V_{IH} = V_{CC} = 5.5V			100	µA
I_{IL}		V_{IL} = 0V, V_{CC} = 5.5V	−100			µA
I_{IH}	High-Level Input Current (LE, FC)	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (LE, FC)	V_{IL} = 0V, V_{CC} = 5.5V	−100		1.0	µA

*Except f_{IN} and OSC_{IN}

Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified (Continued)

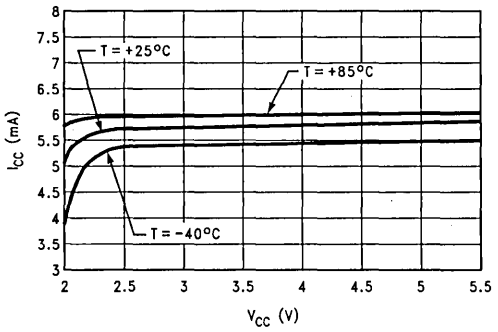
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{D_O}-source	Charge Pump Output Current	$V_{D_O} = V_P/2$		−5.0		mA
I_{D_O}-sink		$V_{D_O} = V_P/2$		5.0		mA
I_{D_O}-Tri	Charge Pump TRI-STATE® Current	0.5V ≤ V_{D_O} ≤ V_P − 0.5V T = 85°C	−2.5		2.5	nA
I_{D_O} vs V_{D_O}	Charge Pump Output Current Magnitude Variation vs Voltage (Note 1)	0.5V ≤ V_{D_O} ≤ V_P − 0.5V T = 25°C			15	%
I_{D_O}-sink vs I_{D_O}-source	Charge Pump Output Current Sink vs Source Mismatch (Note 2)	$V_{D_O} = V_P/2$ T = 25°C			10	%
I_{D_O}vs T	Charge Pump Output Current Magnitude Variation vs Temperature (Note 3)	−40°C < T < 85°C $V_{D_O} = V_P/2$		10		%
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA**	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA**			0.4	V
V_{OH}	High-Level Output Voltage (OSC_{OUT})	I_{OH} = −200 μA	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage (OSC_{OUT})	I_{OL} = 200 μA			0.4	V
I_{OL}	Open Drain Output Current (ϕ_P)	V_{CC} = 5.0V, V_{OL} = 0.4V	1.0			mA
I_{OH}	Open Drain Output Current (ϕ_P)	V_{OH} = 5.5V			100	μA
R_{ON}	Analog Switch ON Resistance (2315)			100		Ω
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

**Except OSC_{OUT}

Notes 1, 2, 3: See related equations in Charge Pump Current Specification Definitions

Typical Performance Characteristics

I_{CC} vs V_{CC}



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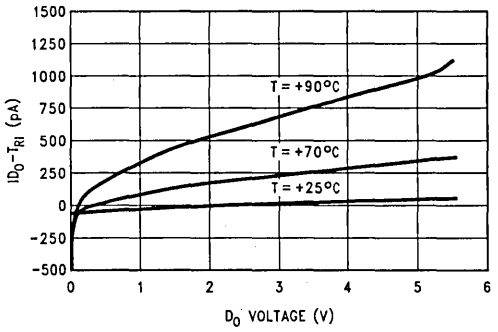
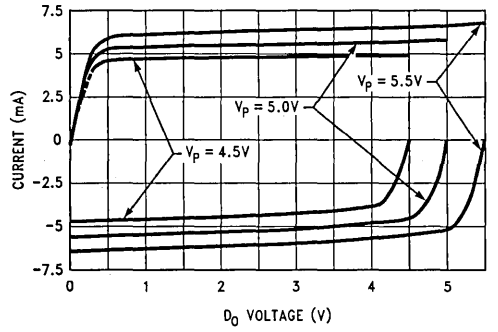
I_{D_O} TRI-STATE vs D_O Voltage



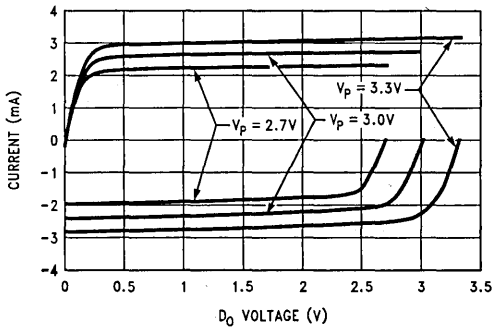
TL/W/11766-30

Charge Pump Current vs D_O Voltage



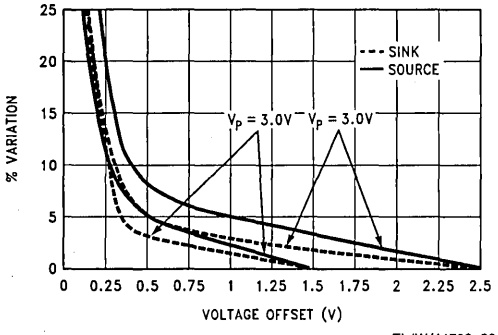
TL/W/11766-31

Charge Pump Current vs D_O Voltage



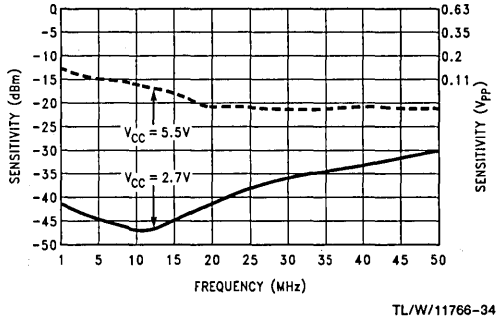
TL/W/11766-32

Charge Pump Current Variation



TL/W/11766-33

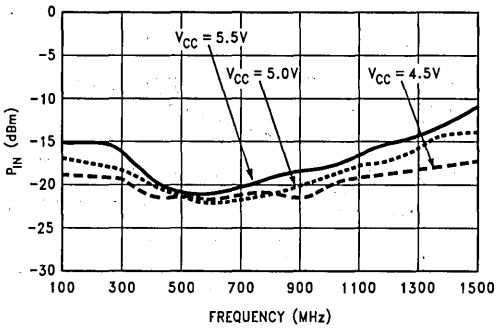
Oscillator Input Sensitivity



TL/W/11766-34

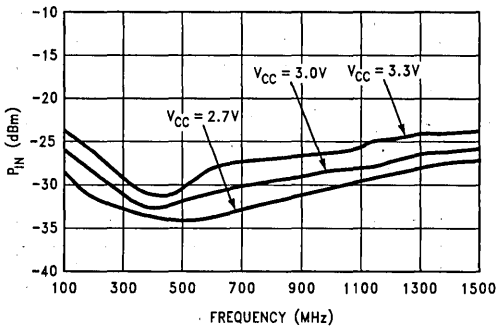
Typical Performance Characteristics (Continued)

Input Sensitivity vs Frequency



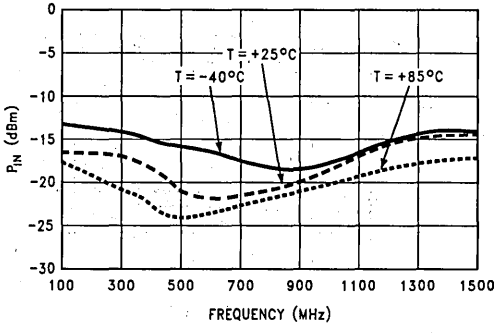
TL/W/11766–35

Input Sensitivity vs Frequency



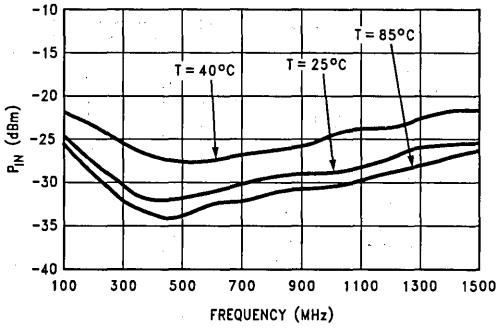
TL/W/11766–36

Input Sensitivity at Temperature Variation, V_{CC} = 5V



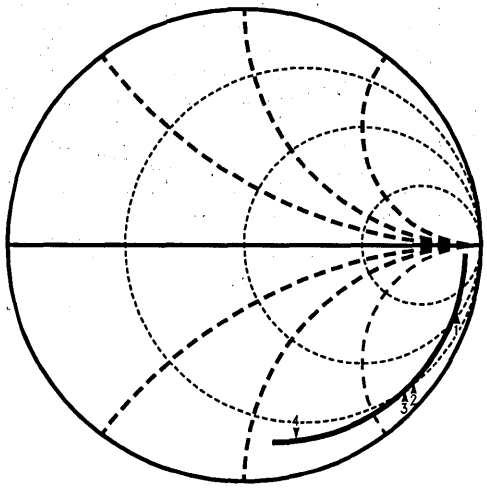
TL/W/11766–37

Input Sensitivity at Temperature Variation, V_{CC} = 3V



TL/W/11766–38

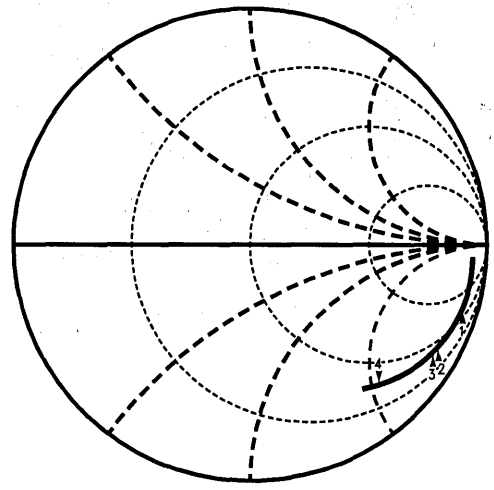
LMX2314 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 100 MHz to 1,600 MHz



TL/W/11766–40

Marker 1 = 500 MHz, Real = 67, Imag. = −317
Marker 2 = 900 MHz, Real = 24, Imag. = −150
Marker 3 = 1 GHz, Real = 19, Imag. = −126
Marker 4 = 1,500 MHz, Real = 9, Imag. = −63

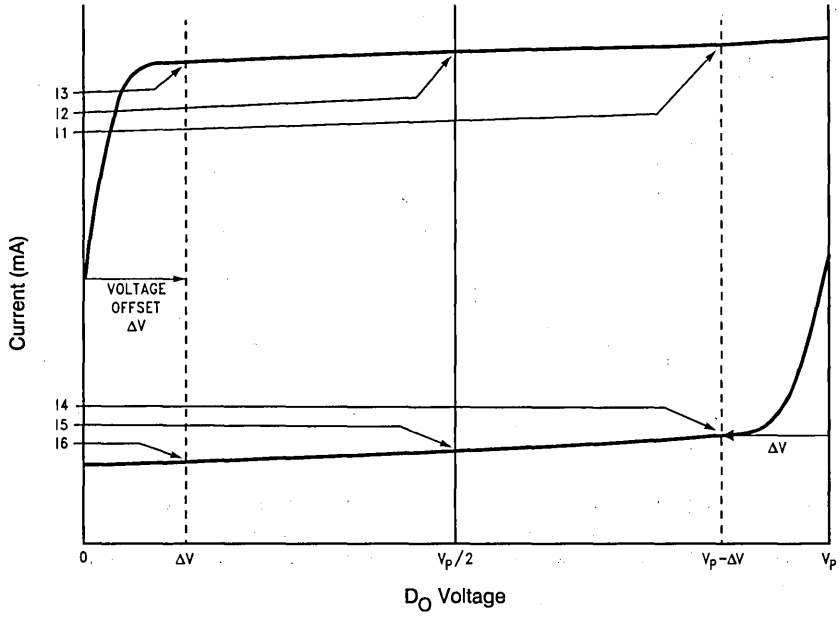
LMX2315 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 100 MHz to 1,600 MHz



TL/W/11766–39

Marker 1 = 500 MHz, Real = 69, Imag. = −330
Marker 2 = 900 MHz, Real = 36, Imag. = −193
Marker 3 = 1 GHz, Real = 35, Imag. = −172
Marker 4 = 1,500 MHz, Real = 30, Imag. = −106

Charge Pump Current Specification Definitions



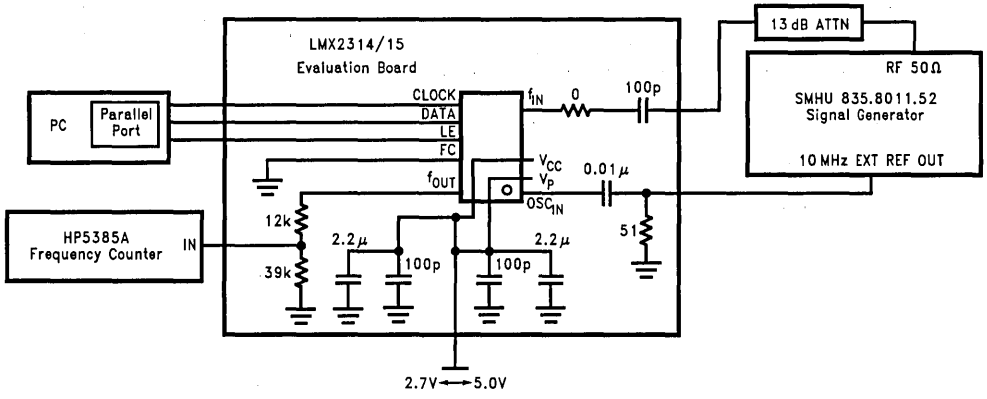
TL/W/11766–41

I1 = CP sink current at $V_{D_O} = V_P - \Delta V$
I2 = CP sink current at $V_{D_O} = V_P/2$
I3 = CP sink current at $V_{D_O} = \Delta V$
I4 = CP source current at $V_{D_O} = V_P - \Delta V$
I5 = CP source current at $V_{D_O} = V_P/2$
I6 = CP source current at $V_{D_O} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

1. I_{D_O} vs V_{D_O} = Charge Pump Output Current magnitude variation vs Voltage =
$[½ * |I1| - |I3|]/[½ * (|I1| + |I3|)] * 100\%$ and $[½ * |I4| - |I6|]/[½ * (|I4| + |I6|)] * 100\%$
2. $I_{D_{O\text{-sink}}}$ vs $I_{D_{O\text{-source}}}$ = Charge Pump Output Current Sink vs Source Mismatch =
$[|I2| - |I5|]/[½ * (|I2| + |I5|)] * 100\%$
3. I_{D_O} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
$[|I2 @ temp| - |I2 @ 25°C|]/|I2 @ 25°C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25°C|]/|I5 @ 25°C| * 100\%$
4. $K\phi$ = Phase detector/charge pump gain constant =
$½ * (|I2| + |I5|)$

RF Sensitivity Test Block Diagram



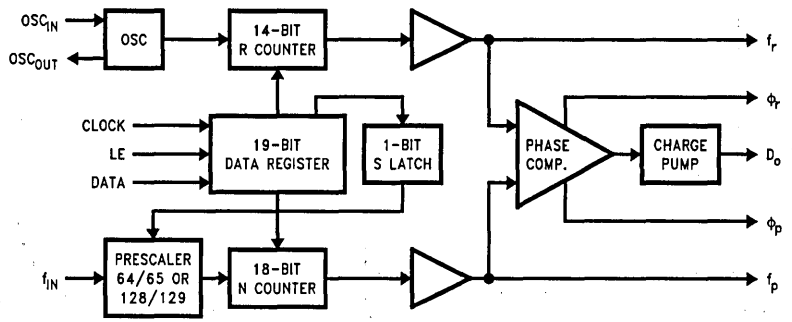
TL/W/11766–42

Note 1: N = 10,000 R = 50 P = 64

Note 2: Sensitivity limit is reached when the error of the divided RF output, f_{OUT}, is greater than or equal to 1 Hz.

Functional Description

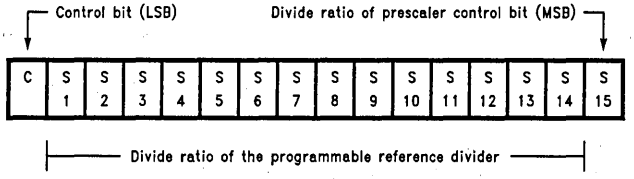
The simplified block diagram below shows the 19-bit data register, the 14-bit R Counter and the S Latch, and the 18-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (prescaler select: 64/65 or 128/129). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).



TL/W/11766–5

PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND PRESCALER SELECT (S LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit S Latch (S15, which sets the prescaler: 64/65 or 128/129). Serial data format is shown below.



TL/W/11766–6

14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1-BIT PRESCALER SELECT (S LATCH)

Prescaler Select P	S 15
128/129	0
64/65	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 16383

S1 to S14: These bits select the divide ratio of the programmable reference divider.

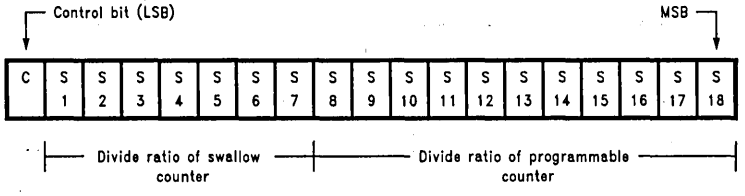
C: Control bit (set to HIGH level to load R counter and S Latch)

Data is shifted in MSB first.

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into a 7-bit latch (which sets the 7-bit Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter). Serial data format is shown below.



TL/W/11766–7

Note: S8 to S18: Programmable counter divide ratio control bits (3 to 2047)

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio: 0 to 127

$B \geq A$

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)

$B \geq A$

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A \leq B$)

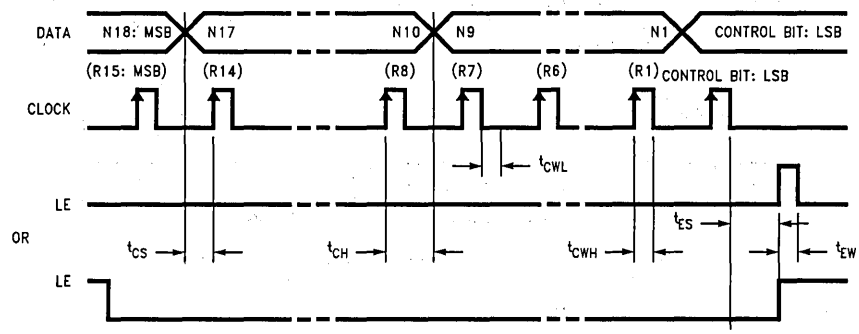
f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

P: Preset modulus of dual modulus prescaler (64 or 128)

Functional Description (Continued)

SERIAL DATA INPUT TIMING



TL/W/11766–8

Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

Phase Characteristics

In normal operation, the FC pin is used to reverse the polarity of the phase detector. Both the internal and any external charge pump are affected.

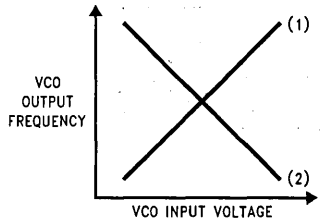
Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT;

When VCO characteristics are like (2), FC should be set LOW.

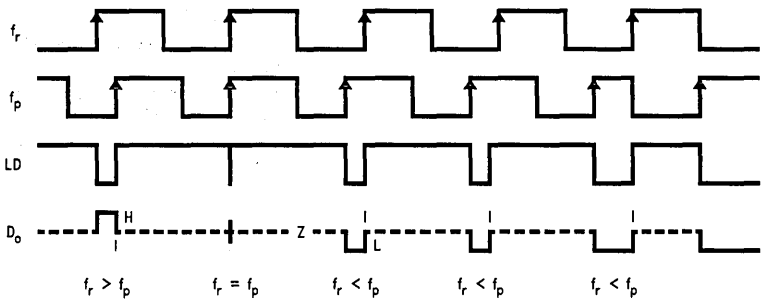
When FC is set HIGH or OPEN CIRCUIT, the monitor pin of the phase comparator input, f_{out}, is set to the reference divider output, f_r. When FC is set LOW, f_{out} is set to the programmable divider output, f_p.

VCO Characteristics



TL/W/11766–9

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



TL/W/11766–10

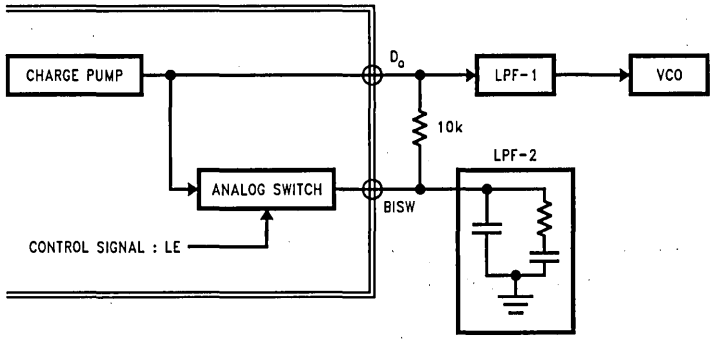
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

FC = HIGH

Analog Switch (2315 only)

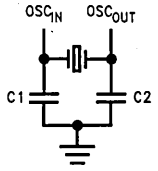
The analog switch is useful for radio systems that utilize a frequency scanning mode and a narrow band mode. The purpose of the analog switch is to decrease the loop filter time constant, allowing the VCO to adjust to its new frequency in a shorter amount of time. This is achieved by adding another filter stage in parallel. The output of the charge pump is normally through the D_O pin, but when LE is set HIGH, the charge pump output also becomes available at BISW. A typical circuit is shown below. The second filter stage (LPF-2) is effective only when the switch is closed (in the scanning mode).



TL/W/11766–11

Typical Crystal Oscillator Circuit

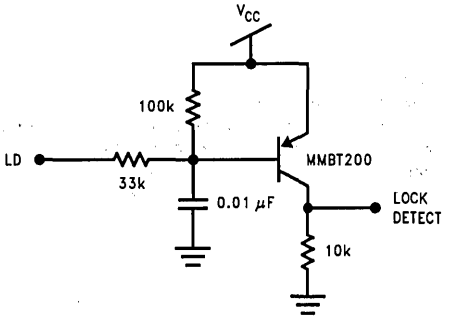
A typical circuit which can be used to implement a crystal oscillator is shown below.



TL/W/11766–12

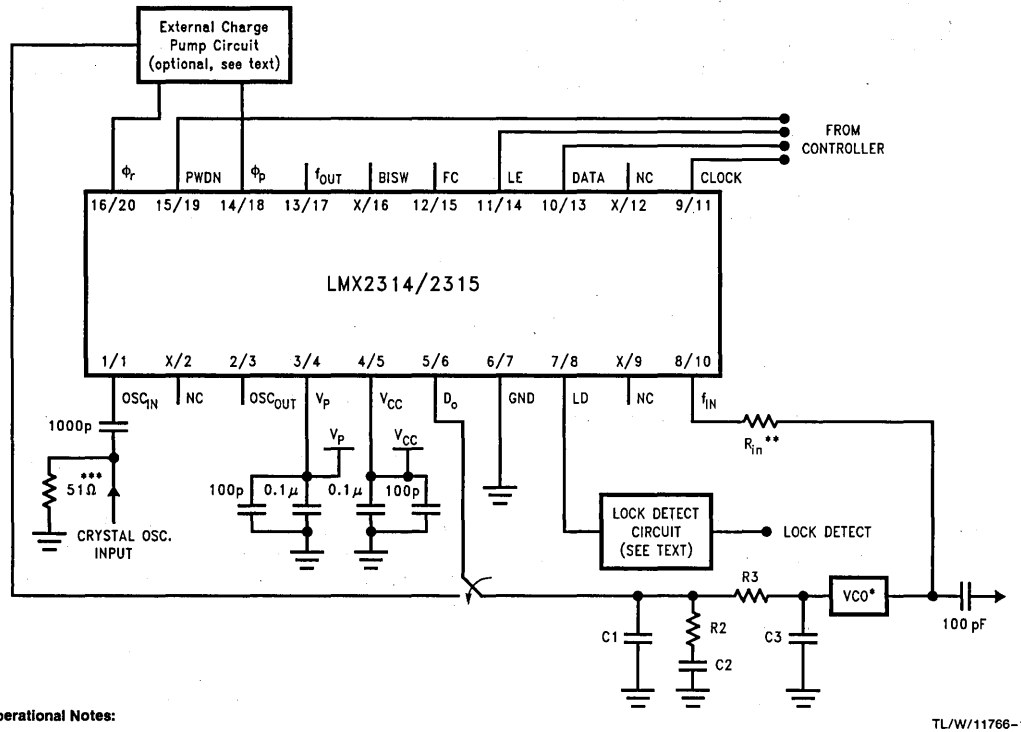
Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



TL/W/11766–13

Typical Application Example



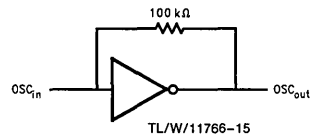
TL/W/11766–14

Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



TL/W/11766–15

Proper use of grounds and bypass capacitors is essential to achieve a high level of performance.

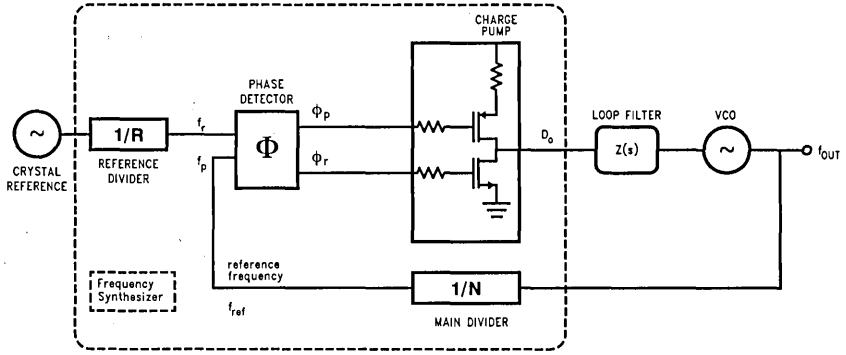
Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

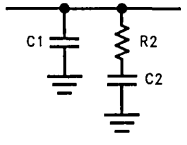
A block diagram of the basic phase locked loop is shown.



TL/W/11766–16

FIGURE 1. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in *Figure 2.*



TL/W/11766–17

$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2}$$

FIGURE 2. 2nd Order Passive Filter

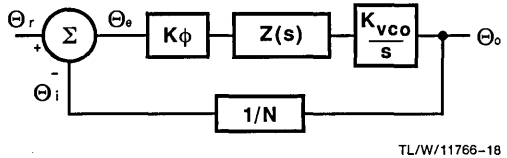
Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \qquad (1a)$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \qquad (1b)$$

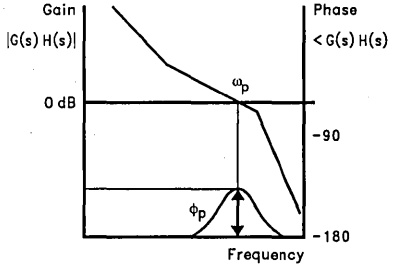
The PLL linear model control circuit is shown along with the open loop transfer function in *Figure 3.* Using the phase detector and VCO gain constants [$K\phi$ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and −180°.



TL/W/11766–18

Open Loop Gain $= \theta_i/\theta_e = H(s)\,G(s)$
$= K\phi\ Z(s)\ K_{VCO}/Ns$

Closed Loop Gain $= \theta_o/\theta_i = G(s)/[1 + H(s)\,G(s)]$



TL/W/11766–19

FIGURE 3. Open Loop Transfer Function

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \qquad (2)$$

From equation 2 we can see that the phase term will be dependent on the single pole and zero such that

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \qquad (3)$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \qquad (4)$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in equation 5.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \qquad (5)$$

For the loop to be stable the unity gain point must occur before the phase reaches −180 degrees. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \qquad (6)$$

Application Information (Continued)

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, ϕ_p, Equations 1 through 6 allow us to calculate the two time constants, T1 and T2, as shown in equations 7 and 8. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (8)$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 9 to 11.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (9)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \quad (10)$$

$$R2 = \frac{T2}{C2} \quad (11)$$

K_{VCO} (MHz/V)	Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.
$K\phi$ (mA)	Phase detector/charge pump gain constant. The ratio of the current output to the input phase differential.
N	Main divider ratio. Equal to RF_{opt}/f_{ref}
RF_{opt} (MHz)	Radio Frequency output of the VCO at which the loop filter is optimized.
f_{ref} (kHz)	Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a trade off must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result.

THIRD ORDER FILTER

A low pass filter section may be needed for some applications that require additional rejection of the reference sidebands, or spurs. This configuration is given in *Figure 4*. In order to compensate for the added low pass section, the component values are recalculated using the new open loop unity gain frequency. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log[(2\pi f_{ref} \bullet R3 \bullet C3)^2 + 1] \quad (12)$$

Defining the additional time constant as

$$T3 = R3 \bullet C3 \quad (13)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}} \quad (14)$$

We then use the calculated value for loop bandwidth ω_c in equation 11, to determine the loop filter component values in equations 15–17. ω_c is slightly less than ω_p, therefore the frequency jump lock time will increase.

$$T2 = \frac{1}{\omega_c^2 \bullet (T1 + T3)} \quad (15)$$

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right] \quad (16)$$

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_c^2 \bullet N} \bullet \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)}\right]^{1/2} \quad (17)$$

Application Information (Continued)

Consider the following application example:

Example #1

K_{VCO} = 20 MHz/V

$K\phi$ = 5 mA (Note 1)

RF_{opt} = 900 MHz

F_{ref} = 200 kHz

$N = RF_{opt}/f_{ref}$ = 4500

$\omega_p = 2\pi * 20$ kHz = 1.256e5

ϕ_p = 45°

ATTEN = 20 dB

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} = 3.29e-6$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \bullet 200e3)^2}} = 2.387e-6$$

$$\omega_c = \frac{(3.29e-6 + 2.387e-6)}{[(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6]} \bullet \left[\sqrt{1 + \frac{(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6}{[(3.29e-6 + 2.387e-6)]^2}} - 1\right]$$

$$= 7.045e4$$

$$T2 = \frac{1}{(7.045e4)^2 \bullet (3.29e-6 + 2.387e-6)} = 3.549e-5$$

$$C1 = \frac{3.29e-6}{3.549e-5} \frac{(5e-3) \bullet 20e6}{(7.045e4)^2 \bullet 4500} \bullet \left[\frac{[1 + (7.045e4)^2 \bullet (3.549e-5)^2]}{[1 + (7.045e4)^2 \bullet (3.29e-6)^2]\,[1 + (7.045e4)^2 \bullet (2.387e-6)^2]}\right]^{1/2}$$

$$= 1.085 \text{ nF}$$

$$C2 = 1.085 \text{ nF} \bullet \left(\frac{3.55e-5}{3.29e-6} - 1\right) = 10.6 \text{ nF};$$

$$R2 = \frac{3.55e-5}{10.6e-9} = 3.35 \text{ k}\Omega;$$

if we choose R3 = 22k; then $C3 = \frac{2.34e-6}{22e3} = 106$ pF.

Converting to standard component values gives the following filter values, which are shown in *Figure 4*.

C1 = 1000 pF
R2 = 3.3 kΩ
C2 = 10 nF
R3 = 22 kΩ
C3 = 100 pF

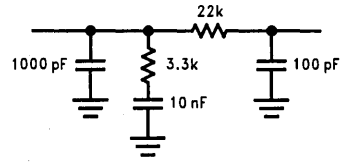


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FIGURE 4. ~20 kHz Loop Filter

Note 1: See related equation for Kϕ in Charge Pump Current Specification Definitions. For this example V_P = 5.0V. The value of Kϕ can then be approximated using the curves in the Typical Peformance Characteristics for Charge Pump Current vs. D_0 Voltage. The units for Kϕ are in mA. You may also use $K\phi = (5 \text{ mA}/2\pi \text{ rad})$, but in this case you must convert K_{VCO} to (rad/V) multiplying by 2π.

Application Information (Continued)

MEASUREMENT RESULTS

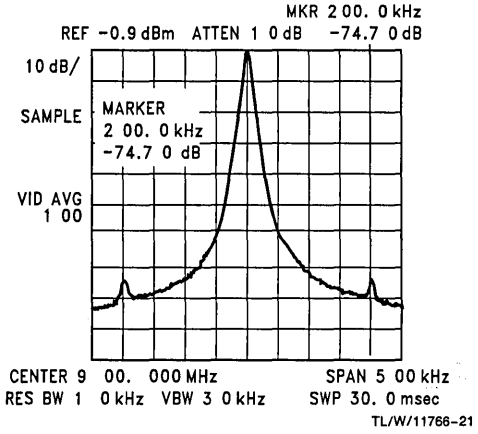

FIGURE 5. PLL Reference Spurs

The reference spurious level is < −74 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2315.

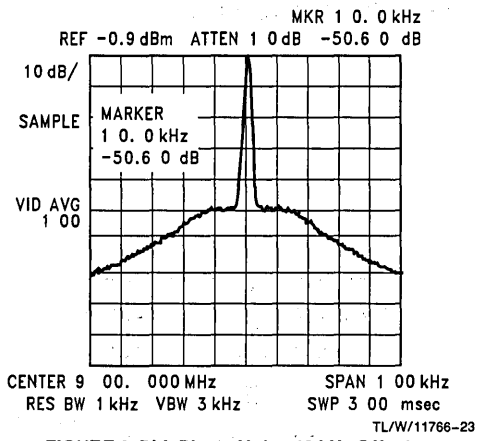

FIGURE 6. PLL Phase Noise 10 kHz Offset

The phase noise level at 10 kHz offset is −80 dBc/Hz.

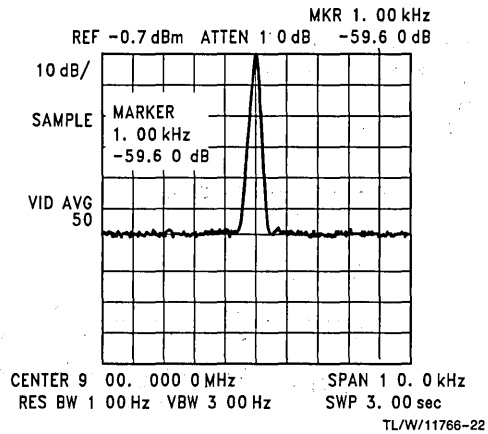

FIGURE 7. PLL Phase Noise @ 1 kHz Offset

The phase noise level at 1 kHz offset is −79.5 dBc/Hz.

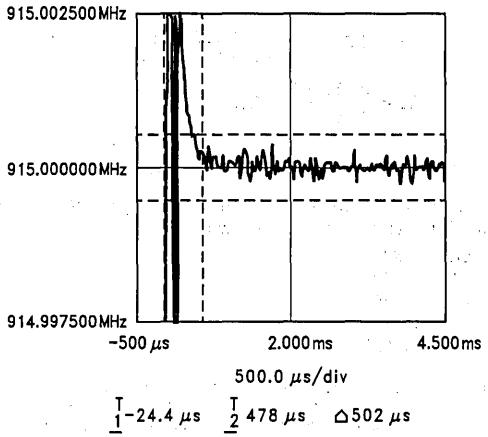

FIGURE 8. Frequency Jump Lock Time

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. *Figure 8* shows the switching waveforms for a frequency jump of 865 MHz to 915 MHz. By narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±500 Hz. The lock time is seen to be less than 500 µs for a frequency jump of 50 MHz.

Application Information (Continued)

EXTERNAL CHARGE PUMP

The LMX PLLatimum series of frequency synthesizers are equipped with an internal balanced charge pump as well as outputs for driving an external charge pump. Although the superior performance of NSC's on board charge pump eliminates the need for an external charge pump in most applications, certain system requirements are more stringent. In these cases, using an external charge pump allows the designer to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation.

One possible architecture for an external charge pump current source is shown in *Figure 9*. The signals ϕ_p and ϕ_r in the diagram, correspond to the phase detector outputs of the LMX2314/2315 frequency synthesizers. These logic signals are converted into current pulses, using the circuitry shown in *Figure 9*, to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

Referring to *Figure 9*, the design goal is to generate a 5 mA current which is relatively constant to within 5V of the power supply rail. To accomplish this, it is important to establish as large of a voltage drop across R5, R8 as possible without saturating Q2, Q4. A voltage of approximately 300 mV provides a good compromise. This allows the current source reference being generated to be relatively repeatable in the absence of good Q1, Q2/Q3, Q4 matching. (Matched transistor pairs is recommended.) The ϕp and ϕr outputs are rated for a maximum output load current of 1 mA while 5 mA current sources are desired. The voltages developed across R4, 9 will consequently be approximately 258 mV, or 42 mV < R8, 5, due to the current density differences {0.026*1n (5 mA/1 mA)} through the Q1, Q2/Q3, Q4 pairs.

In order to calculate the value of R7 it is necessary to first estimate the forward base to emitter voltage drop (Vfn,p) of the transistors used, the V_{OL} drop of ϕp, and the V_{OH} drop of ϕr's under 1 mA loads. (ϕp's V_{OL} < 0.1V and ϕr's V_{OH} < 0.1V.)

Knowing these parameters along with the desired current allow us to design a simple external charge pump. Separating the pump up and pump down circuits facilitates the nodal analysis and give the following equations.

$$R_4 = \frac{V_{R5} - V_T \bullet \ln\left(\frac{i_{source}}{i_{p\,max}}\right)}{i_{source}}$$

$$R_9 = \frac{V_{R8} - V_T \bullet \ln\left(\frac{i_{sink}}{i_{n\,max}}\right)}{i_{sink}}$$

$$R_5 = \frac{V_{R5} \bullet (\beta_p + 1)}{i_{p\,max} \bullet (\beta_p + 1) - i_{source}}$$

$$R_8 = \frac{V_{R8} \bullet (\beta_n + 1)}{i_{r\,max} \bullet (\beta_n + 1)\, i_{sink}}$$

$$R_6 = \frac{(V_p - V_{VOL\phi p}) - (V_{R5} + Vfp)}{i_{p\,max}}$$

$$R_7 = \frac{(V_P - V_{VOH\phi r}) - (V_{R8} + Vfn)}{i_{max}}$$

EXAMPLE

Typical Device Parameters	$\beta_n = 100$, $\beta_p = 50$
Typical System Parameters	$V_P = 5.0V$;
	$V_{cntl} = 0.5V - 4.5V$;
	$V_{\phi p} = 0.0V$; $V_{\phi r} = 5.0V$
Design Parameters	$I_{SINK} = I_{SOURCE} = 5.0$ mA;
	$V_{fn} = V_{fp} = 0.8V$
	$I_{rmax} = I_{pmax} = 1$ mA
	$V_{R8} = V_{R5} = 0.3V$
	$V_{OL\phi p} = V_{OH\phi r} = 100$ mV

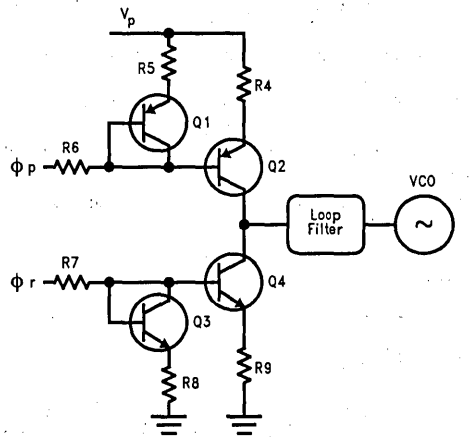

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FIGURE 9

Therefore select

$$R_4 = R_9 = \frac{0.3V - 0.026 \bullet 1n(5.0\text{ mA}/1.0\text{ mA})}{5\text{ mA}} = 51.6\Omega$$

$$R_5 = \frac{0.3V \bullet (50 + 1)}{1.0\text{ mA} \bullet (50 + 1) - 5.0\text{ mA}} = 332\Omega$$

$$R_8 = \frac{0.3V \bullet (100 - 1)}{1.0\text{ mA} \bullet (100 + 1) - 5.0\text{ mA}} = 315.6\Omega$$

$$R_6 = R_7 = \frac{(5V - 0.1V) - (0.3V + 0.8V)}{1.0\text{ mA}} = 3.8\text{ k}\Omega$$

National Semiconductor

ADVANCE INFORMATION

LMX2301
PLLatinum™ 160 MHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2301 is a high performance frequency synthesizer designed for RF operation up to 160 MHz. It is fabricated using National's ABiC IV BiCMOS process.

Using a proprietary digital phase locked loop technique, the LMX2301's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Serial data is transferred into the LMX2301 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V.

The LMX2301 features very low current consumption, typically 2 mA at 3V.

The LMX2301 is available in a TSSOP 20-pin surface mount plastic package.

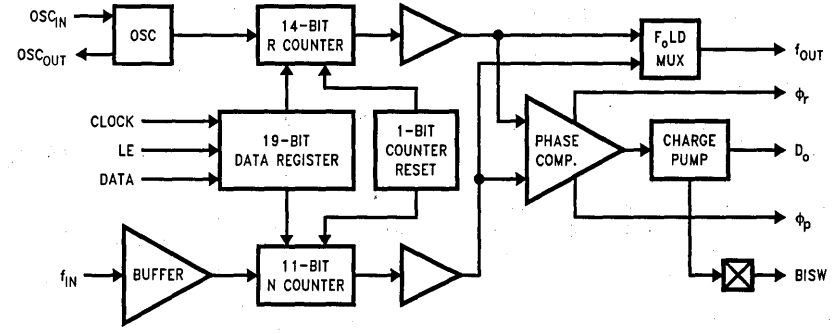
Features

- RF operation up to 160 MHz
- 2.7V to 5.5V operation
- Low current consumption: I_{CC} = 2 mA (typ) at V_{CC} = 3V
- Internal balanced, low leakage charge pump
- Thin Small-outline, plastic, surface mount TSSOP, 0.173" wide package

Applications

- Analog Cellular telephone systems (AMPS, ETACS, NMT)
- Portable wireless communications (PCS/PCN, cordless)
- Other wireless communication systems

Block Diagram



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National Semiconductor

ADVANCE INFORMATION

LMX2305
PLLatinum™ 550 MHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2305 is a high performance frequency synthesizer with an integrated prescaler designed for RF operation up to 550 MHz. It is fabricated using National's ABiC IV BiCMOS process.

The LMX2305 contains a dual modulus prescaler which can select either a 64/65 or a 128/129 divide ratio at input frequencies of up to 550 MHz. Using a proprietary digital phase locked loop technique, the LMX2305's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Serial data is transferred into the LMX2305 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.65V to 5.5V. The LMX2305 features very low current consumption, typically 3.0 mA at 2.75V.

The LMX2305 is available in a TSSOP 20-pin surface mount plastic package.

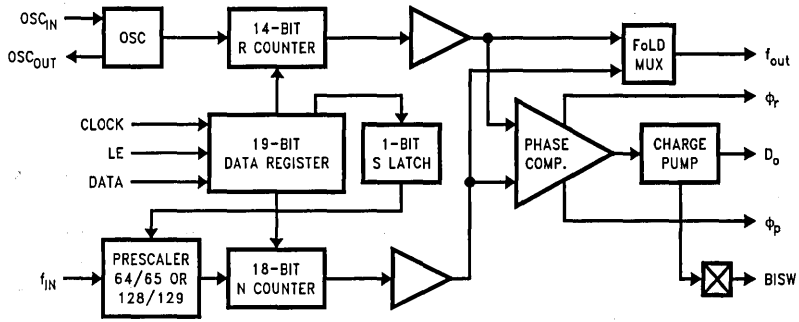
Features

- RF operation up to 550 MHz
- 2.65V to 5.5V operation
- Low current consumption: I_{CC} = 3.0 mA (typ) at V_{CC} = 2.75V
- Dual modulus prescaler: 64/65 or 128/129
- Internal balanced, low leakage charge pump
- Small-outline, plastic, surface mount TSSOP, 0.173" wide package

Applications

- Analog Cellular telephone systems (AMPS, ETACS, NMT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Other wireless communication systems

Block Diagram



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National Semiconductor

LMX2320/LMX2325 PLLatinum™ Frequency Synthesizer for RF Personal Communications LMX2325 2.5 GHz LMX2320 2.0 GHz

General Description

The LMX2320 and the LMX2325 are high performance frequency synthesizers with integrated prescalers designed for RF operation up to 2.5 GHz. They are fabricated using National's ABiC IV BiCMOS process.

A 64/65 or a 128/129 divide ratio can be selected for the LMX2320 RF synthesizer at input frequencies of up to 2.0 GHz, while 32/33 and 64/65 divide ratios are available in the 2.5 GHz LMX2325. Using a proprietary digital phase locked loop technique, the LMX2320/25's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Serial data is transferred into the LMX2320 and the LMX2325 via a three line MICROWIRE™ interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2320 and the LMX2325 feature very low current consumption, typically 10 mA and 11 mA respectively.

The LMX2320 and the LMX2325 are available in a TSSOP 20-pin surface mount plastic package.

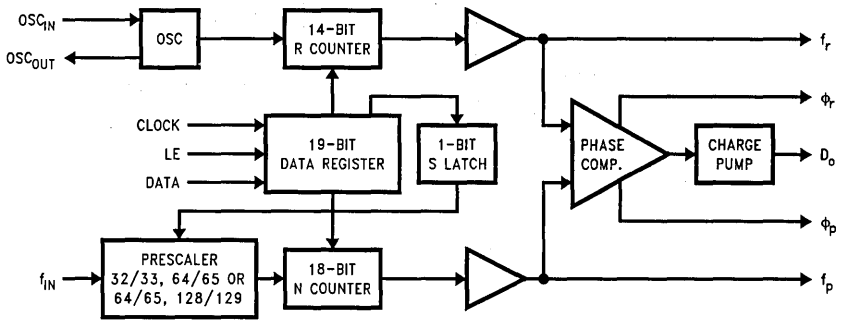
Features

- RF operation up to 2.5 GHz
- 2.7V to 5.5V operation
- Low current consumption
- Dual module prescaler:
  LM2325 32/33 or 64/65
  LM2320 64/65 or 128/129
- Internal balanced, low leakage charge pump
- Power down feature for sleep mode:
  I_{CC} = 30 μA (typ) at V_{CC} = 3V
- Small-outline, plastic, surface mount TSSOP, 0.173" wide

Applications

- Cellular telephone systems (RCR-27)
- Portable wireless communications (DECT, PHS)
- CATV
- Other wireless communication systems

Block Diagram



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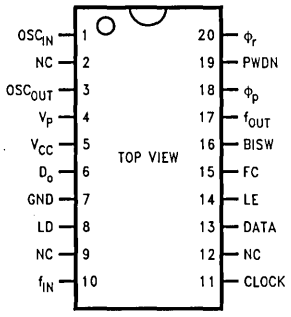
Connection Diagrams

LMX2320/LMX2325



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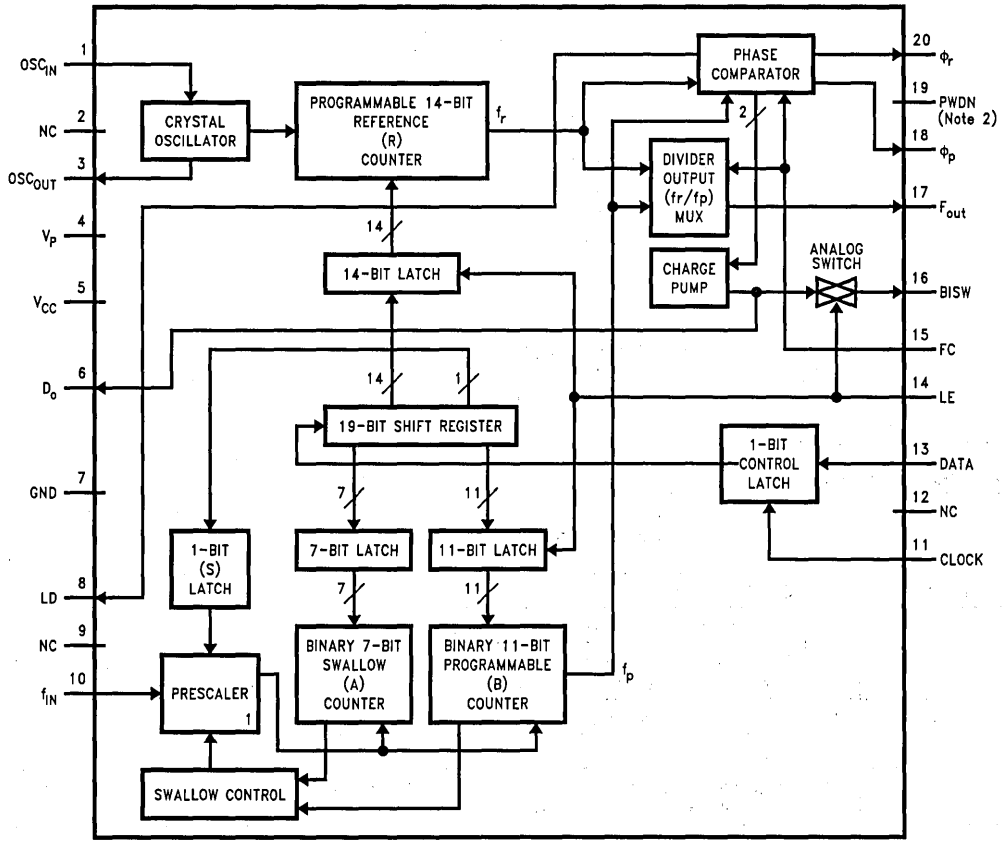
20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX2325TM, LMX2325TMX, LMX2320TM or LMX2320TMX
See NS Package Number MTC20

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
3	OSC_{OUT}	O	Oscillator output.
4	V_P		Power supply for charge pump. Must be $\geq V_{CC}$.
5	V_{CC}		Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
6	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
7	GND		Ground.
8	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in "lock". When the loop is locked, the pin's output is HIGH with narrow low pulses.
10	f_{IN}	I	Prescaler input. Small signal input from the VCO.
11	CLOCK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
13	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
14	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See Serial Data Input Timing Diagram.
15	FC	I	Phase control select (with internal pull-up resistor). When FC is LOW, the polarity of the phase comparator and charge pump combination is reversed.
16	BISW	O	Analog switch output. When LE is HIGH, the analog switch is ON, routing the internal charge pump output through BISW (as well as through D_o).
17	f_{OUT}	O	Monitor pin of phase comparator input. CMOS output.
18	ϕ_p	O	Output for external charge pump. ϕ_p is an open drain N-channel transistor and requires a pull-up resistor.
19	PWDN	I	Power Down (with internal pull-up resistor). PWDN = HIGH for normal operation. PWDN = LOW for power saving. Power down function is gated by the return of the charge pump to a TRI-STATE condition.
20	ϕ_r	O	Output for external charge pump. ϕ_r is a CMOS logic output.
2,9,12	NC		No connect.

Functional Block Diagram



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Note 1: The prescalar for the LMX2320 is either 64/65 or 128/129, while the prescalar for the LMX2325 is 32/33 or 64/65.

Note 2: The power down function is gated by the charge pump to prevent unwanted frequency jumps. Once the power down pin is brought low the part will go into power down mode when the charge pump reaches a TRI-STATE condition.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage
- V_{CC} −0.3V to +6.5V
- V_P −0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) −0.3V to +6.5V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (T_L) (solder, 4 sec.) +260°C

Recommended Operating Conditions

Power Supply Voltage
- V_{CC} 2.7V to 5.5V
- V_P V_{CC} to +5.5V

Operating Temperature (T_A) −40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	LMX2320	V_{CC} = 3.0V		10	13.5	mA
		LMX2325	V_{CC} = 3.0V		11	15	mA
$I_{CC-PWDN}$	Power Down Current		V_{CC} = 3.0V		30	180	µA
			V_{CC} = 5.0V		60	350	µA
f_{IN}	Maximum Operating Frequency	LMX2320		2.0			GHz
		LMX2325		2.5			
f_{OSC}	Maximum Oscillator Frequency			20			MHz
			No Load on OSC_{out}	40			MHz
f_ϕ	Maximum Phase Detector Frequency			10			MHz
Pf_{IN}	Input Sensitivity		V_{CC} = 2.7V to 3.3V	−15		+6	dBm
			V_{CC} = 3.3V to 5.5V	−10		+6	
V_{OSC}	Oscillator Sensitivity		OSC_{IN}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage		*	0.7 V_{CC}			V
V_{IL}	Low-Level Input Voltage		*			0.3 V_{CC}	V
I_{IH}	High-Level Input Current (Clock, Data)		V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (Clock, Data)		V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	µA
I_{IH}	Oscillator Input Current		V_{IH} = V_{CC} = 5.5V			100	µA
I_{IL}			V_{IL} = 0V, V_{CC} = 5.5V	−100			µA
I_{IH}	High-Level Input Current (LE, FC)		V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (LE, FC)		V_{IL} = 0V, V_{CC} = 5.5V	−100		1.0	µA

*Except f_{IN} and OSC_{IN}

Electrical Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified (Continued)

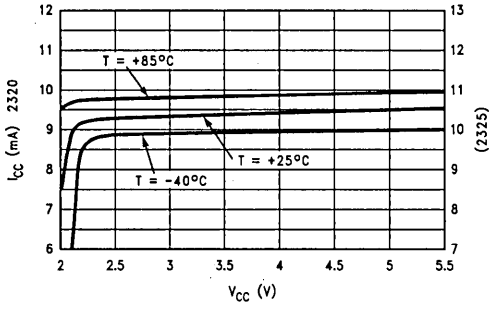
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{D_O}-source	Charge Pump Output Current	$V_{D_O} = V_P/2$		−2.5		mA
I_{D_O}-sink		$V_{D_O} = V_P/2$		2.5		mA
I_{D_O}-Tri	Charge Pump TRI-STATE® Current	0.5V ≤ V_{D_O} ≤ V_P − 0.5V T = 85°C	−2.5		2.5	nA
I_{D_O} vs V_{D_O}	Charge Pump Output Current Magnitude Variation vs Voltage (Note 1)	0.5V ≤ V_{D_O} ≤ V_P − 0.5V T = 25°C			15	%
I_{D_O}-sink vs I_{D_O}-source	Charge Pump Output Current Sink vs Source Mismatch (Note 2)	$V_{D_O} = V_P/2$ T = 25°C			10	%
I_{D_O}vs T	Charge Pump Output Current Magnitude Variation vs Temperature (Note 3)	−40°C < T < 85°C $V_{D_O} = V_P/2$		10		%
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA**	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA**			0.4	V
V_{OH}	High-Level Output Voltage (OSC_{OUT})	I_{OH} = −200 μA	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage (OSC_{OUT})	I_{OL} = 200 μA			0.4	V
I_{OL}	Open Drain Output Current (ϕ_P)	V_{CC} = 5.0V, V_{OL} = 0.4V	1.0			mA
I_{OH}	Open Drain Output Current (ϕ_P)	V_{OH} = 5.5V			100	μA
R_{ON}	Analog Switch ON Resistance (2315)			100		Ω
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

**Except OSC_{OUT}

Notes 1, 2, 3: See related equations in Charge Pump Current Specification Definitions

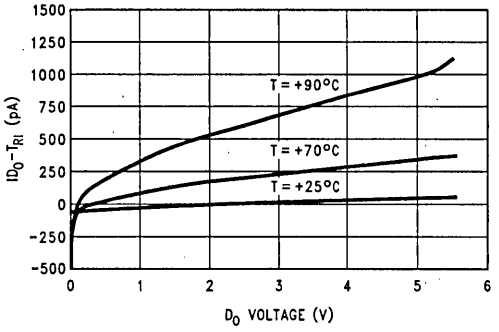
Typical Performance Characteristics

I_{CC} vs V_{CC}



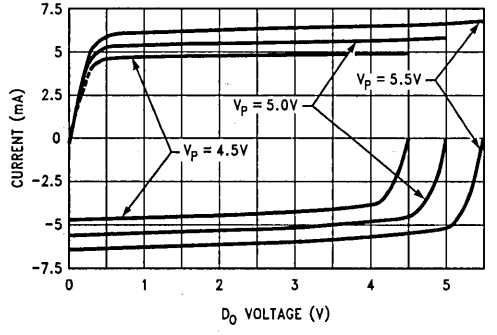
TL/W/12339-4

I_{D_O} TRI-STATE vs D_O Voltage



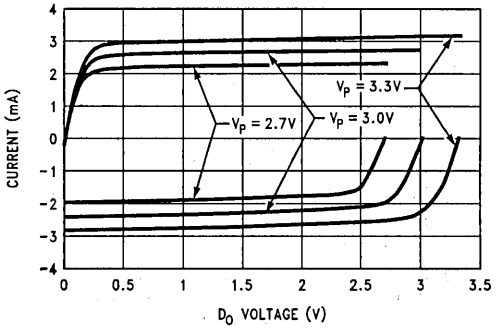
TL/W/12339-5

Charge Pump Current vs D_O Voltage



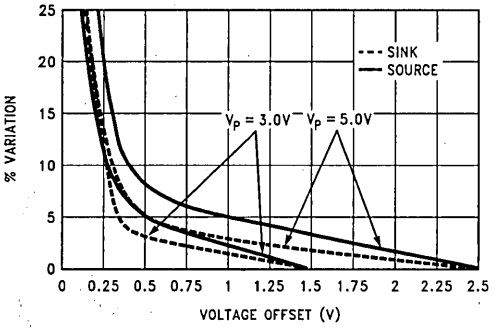
TL/W/12339-40

Charge Pump Current vs D_O Voltage



TL/W/12339-7

Charge Pump Current Variation



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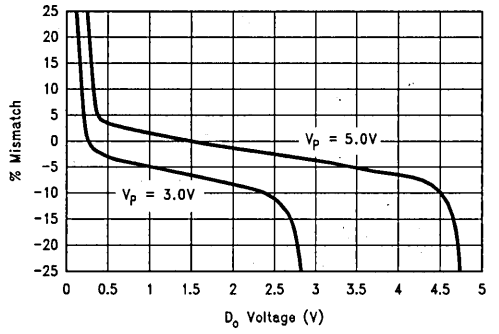
Sink vs Source Mismatch vs D_O Voltage



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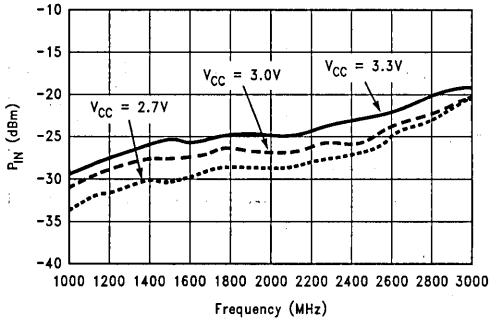
1

Typical Performance Characteristics (Continued)

Input Sensitivity vs Frequency



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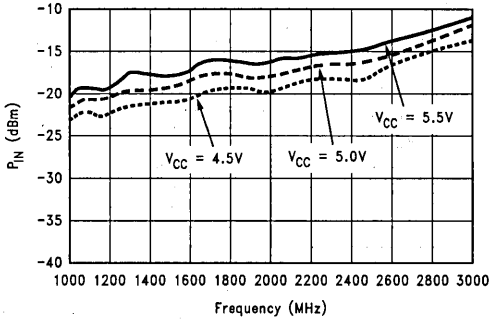
Input Sensitivity vs Frequency



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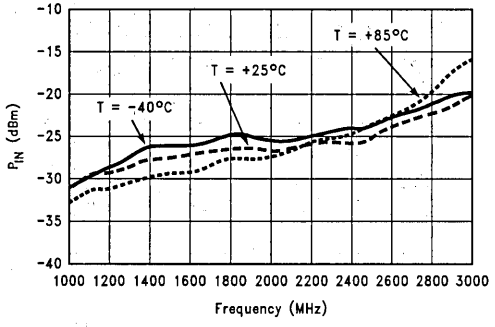
Input Sensitivity at Temperature Variation, V_{CC} = 3V



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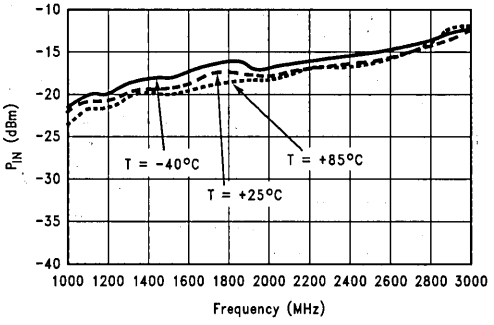
Input Sensitivity at Temperature Variation, V_{CC} = 5V



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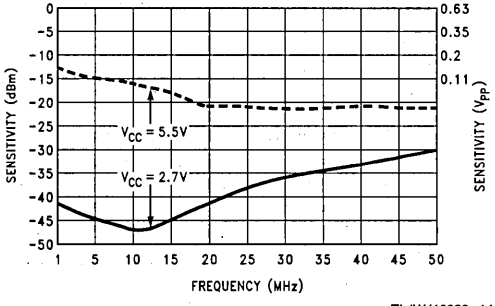
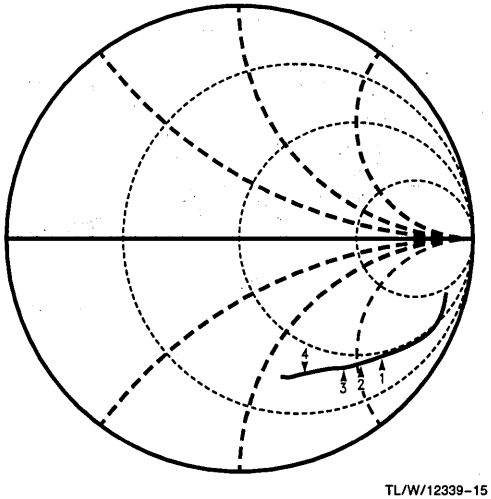
Oscillator Input Sensitivity



TL/W/12339–14

LMX2320/25 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 500 MHz to 3000 MHz



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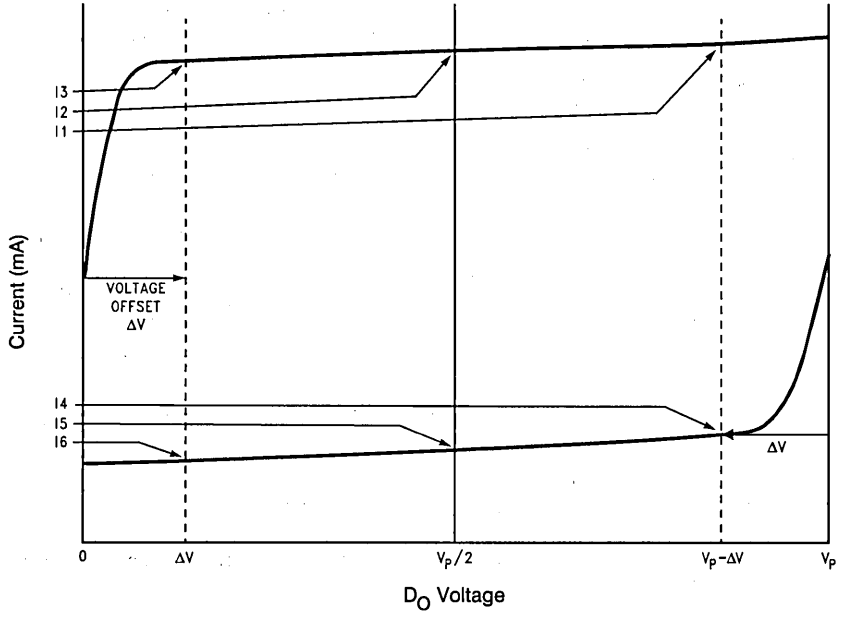
1 = 1.5 GHz, Real = 48, Im = −128
2 = 1.8 GHz, Real = 44, Im = −102
3 = 2.0 GHz, Real = 42, Im = −90
4 = 2.5 GHz, Real = 36, Im = −72

Charge Pump Current Specification Definitions



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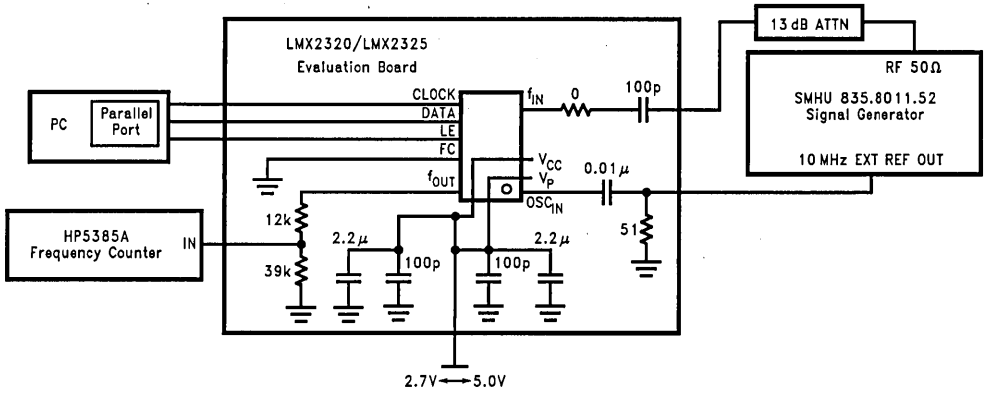
I1 = CP sink current at $V_{D_O} = V_P - \Delta V$
I2 = CP sink current at $V_{D_O} = V_P/2$
I3 = CP sink current at $V_{D_O} = \Delta V$
I4 = CP source current at $V_{D_O} = V_P - \Delta V$
I5 = CP source current at $V_{D_O} = V_P/2$
I6 = CP source current at $V_{D_O} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

1. I_{D_O} vs V_{D_O} = Charge Pump Output Current magnitude variation vs Voltage =
   $[\frac{1}{2} * |I1| - |I3|]/[\frac{1}{2} * \{|I1| + |I3|\}] * 100\%$ and $[\frac{1}{2} * |I4| - |I6|]/[\frac{1}{2} * \{|I4| + |I6|\}] * 100\%$
2. $I_{D_{O\text{-sink}}}$ vs $I_{D_{O\text{-source}}}$ = Charge Pump Output Current Sink vs Source Mismatch =
   $[|I2| - |I5|]/[\frac{1}{2} * \{|I2| + |I5|\}] * 100\%$
3. I_{D_O} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
   $[|I2 @ temp| - |I2 @ 25°C|]/|I2 @ 25°C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25°C|]/|I5 @ 25°C| * 100\%$
4. Kϕ = Phase detector/charge pump gain constant =
   $\frac{1}{2} * \{|I2| + |I5|\}$

RF Sensitivity Test Block Diagram



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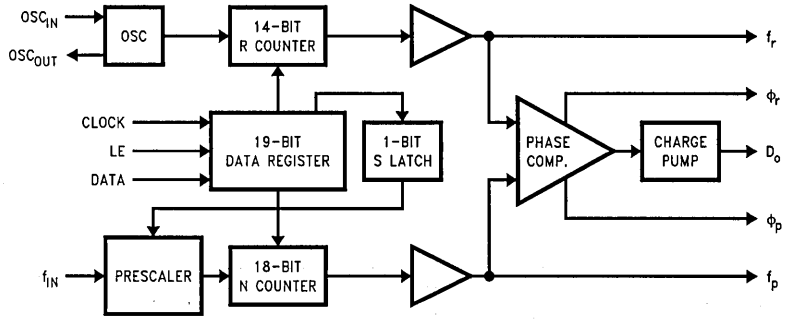
Note 1: N = 10,000 R = 50 P = 64

Note 2: Sensitivity limit is reached when the error of the divided RF output, f_{OUT}, is greater than or equal to 1 Hz.

Functional Description

The simplified block diagram below shows the 19-bit data register, the 14-bit R Counter and the S Latch, and the 18-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (prescaler select: LMX2320: 64/65 or 128/129; LMX2325 32/33 and 64/65). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).



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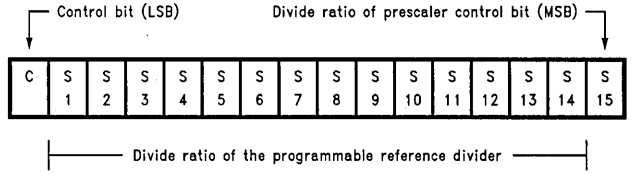
PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND PRESCALER SELECT (S LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit S Latch (S15, which sets the prescaler: 64/65 or 128/129 for the LMX2320; or 32/33 or 64/65 for the LMX2325). Serial data format is shown below.



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14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Prescaler Select		S 15
LMX2320	LMX2325	
128/129	64/65	0
64/65	32/33	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 16383

S1 to S14: These bits select the divide ratio of the programmable reference divider.

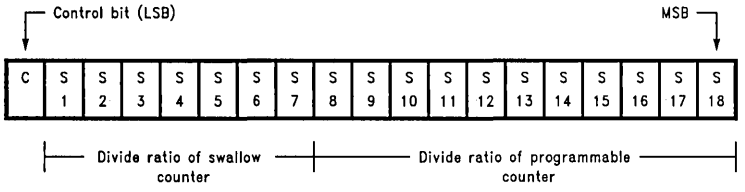
C: Control bit (set to HIGH level to load R counter and S Latch)

Data is shifted in MSB first.

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into a 7-bit latch (which sets the 7-bit Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter). Serial data format is shown below.



TL/W/12339–20

Note: S8 to S18: Programmable counter divide ratio control bits (3 to 2047)

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio: 0 to 127
B ≥ A

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A \leq B$)

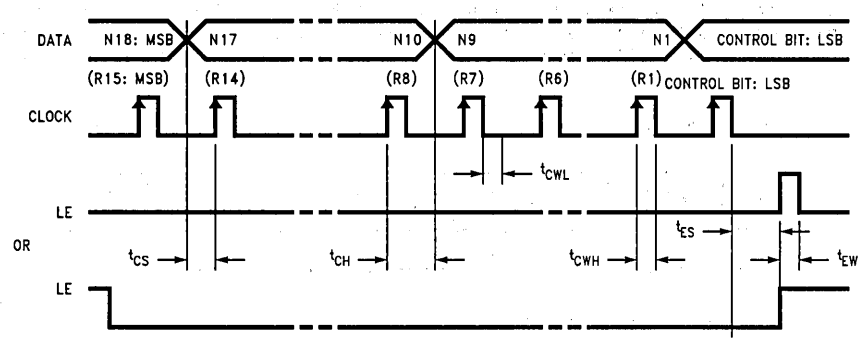
f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

P: Preset modulus of dual modulus prescaler (64 or 128 for 2320 or 32 or 64 for 2325)

Functional Description (Continued)

SERIAL DATA INPUT TIMING



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Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

Phase Characteristics

In normal operation, the FC pin is used to reverse the polarity of the phase detector. Both the internal and any external charge pump are affected.

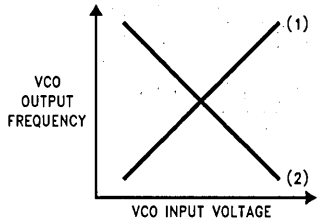
Depending upon VCO characteristics, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT;

When VCO characteristics are like (2), FC should be set LOW.

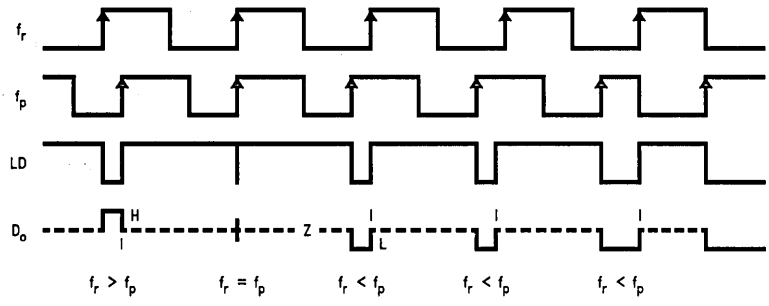
When FC is set HIGH or OPEN CIRCUIT, the monitor pin of the phase comparator input, f_{out}, is set to the reference divider output, f_r. When FC is set LOW, f_{out} is set to the programmable divider output, f_p.

VCO Characteristics



TL/W/12339-22

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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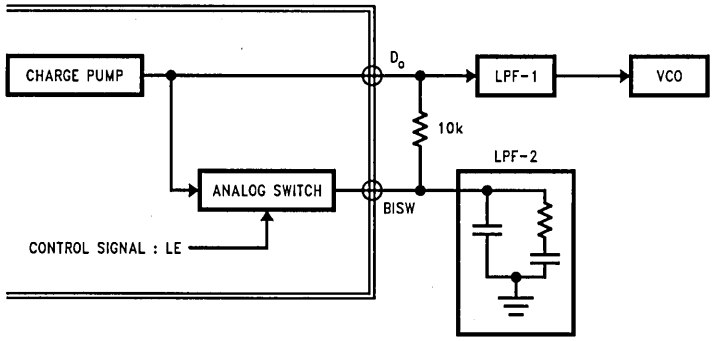
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

FC = HIGH

Analog Switch

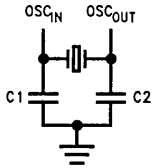
The analog switch is useful for radio systems that utilize a frequency scanning mode and a narrow band mode. The purpose of the analog switch is to decrease the loop filter time constant, allowing the VCO to adjust to its new frequency in a shorter amount of time. This is achieved by adding another filter stage in parallel. The output of the charge pump is normally through the D_O pin, but when LE is set HIGH, the charge pump output also becomes available at BISW. A typical circuit is shown below. The second filter stage (LPF-2) is effective only when the switch is closed (in the scanning mode).



TL/W/12339-24

Typical Crystal Oscillator Circuit

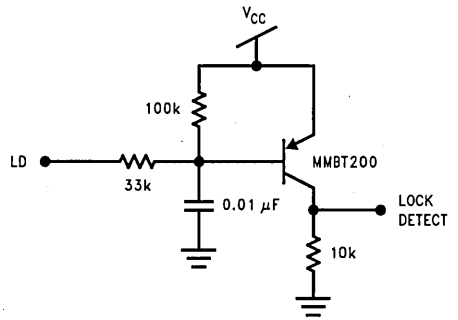
A typical circuit which can be used to implement a crystal oscillator is shown below.



TL/W/12339-25

Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



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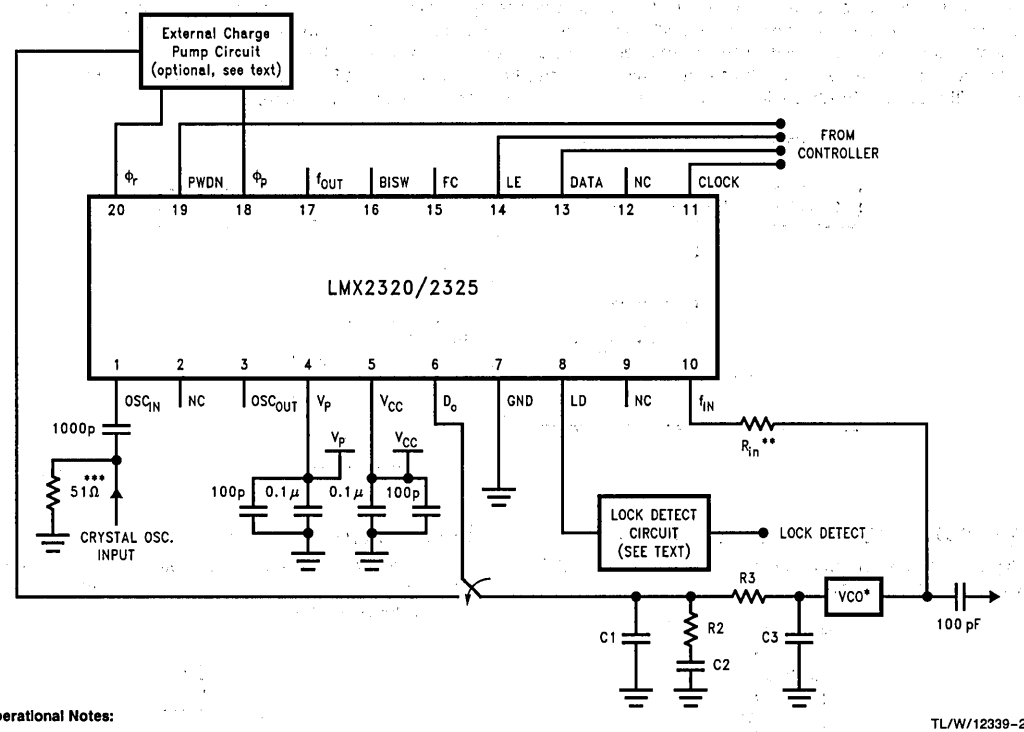
Typical Application Example



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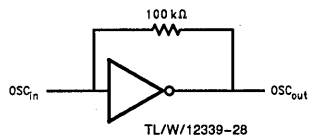
Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



TL/W/12339–28

Proper use of grounds and bypass capacitors is essential to achieve a high level of performance.

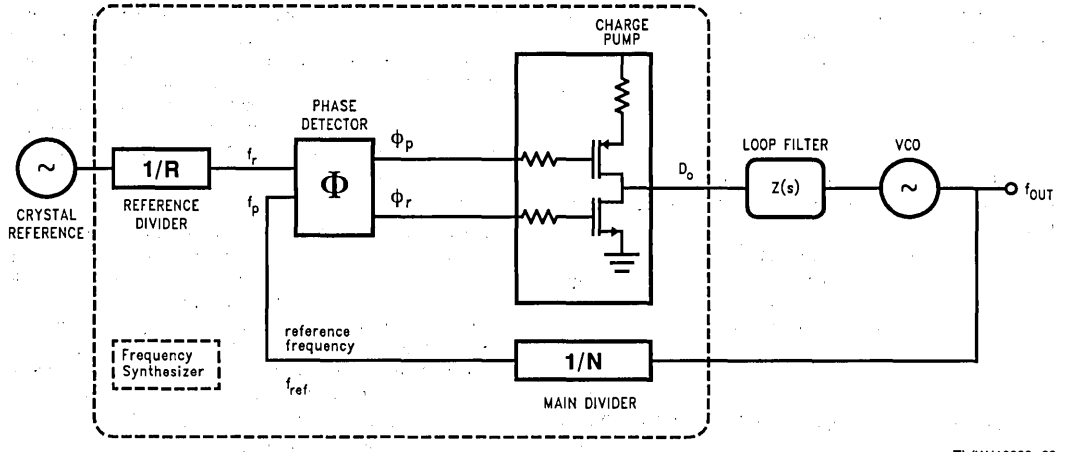
Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

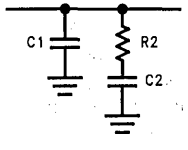
A block diagram of the basic phase locked loop is shown.



TL/W/12339-29

FIGURE 1. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in *Figure 2*.



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$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2}$$

FIGURE 2. 2nd Order Passive Filter

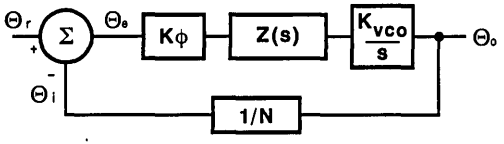
Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \tag{1a}$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \tag{1b}$$

The PLL linear model control circuit is shown along with the open loop transfer function in *Figure 3*. Using the phase detector and VCO gain constants [$K\phi$ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and $-180°$.



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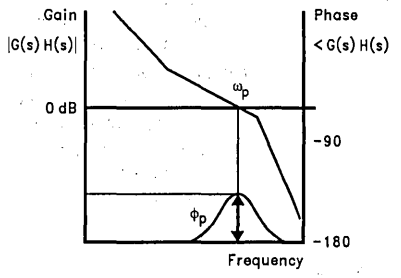
Open Loop Gain = θ_i/θ_e = H(s) G(s)
= $K\phi$ Z(s) K_{VCO}/Ns

Closed Loop Gain = θ_o/θ_i = G(s)/[1 + H(s) G(s)]



TL/W/12339-31

FIGURE 3. Open Loop Transfer Function

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \tag{2}$$

From equation 2 we can see that the phase term will be dependent on the single pole and zero such that

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \tag{3}$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \tag{4}$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in equation 5.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \tag{5}$$

For the loop to be stable the unity gain point must occur before the phase reaches -180 degrees. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \tag{6}$$

Application Information (Continued)

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, ϕ_p, Equations 1 through 6 allow us to calculate the two time constants, T1 and T2, as shown in equations 7 and 8. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (8)$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 9 to 11.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (9)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \quad (10)$$

$$R2 = \frac{T2}{C2} \quad (11)$$

K_{VCO} (MHz/V) — Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

$K\phi$ (mA) — Phase detector/charge pump gain constant. The ratio of the current output to the input phase differential.

N — Main divider ratio. Equal to RF_{opt}/f_{ref}

RF_{opt} (MHz) — Radio Frequency output of the VCO at which the loop filter is optimized.

f_{ref} (kHz) — Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a trade off must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result.

THIRD ORDER FILTER

A low pass filter section may be needed for some applications that require additional rejection of the reference sidebands, or spurs. This configuration is given in *Figure 4*. In order to compensate for the added low pass section, the component values are recalculated using the new open loop unity gain frequency. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2.

The added attenuation from the low pass filter is:

$$ATTEN = 20\log[(2\pi f_{ref} \bullet R3 \bullet C3)^2 + 1] \quad (12)$$

Defining the additional time constant as

$$T3 = R3 \bullet C3 \quad (13)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}} \quad (14)$$

We then use the calculated value for loop bandwidth ω_c in equation 11, to determine the loop filter component values in equations 15–17. ω_c is slightly less than ω_p, therefore the frequency jump lock time will increase.

$$T2 = \frac{1}{\omega_c^2 \bullet (T1 + T3)} \quad (15)$$

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right] \quad (16)$$

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_c^2 \bullet N} \bullet \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)}\right]^{1/2} \quad (17)$$

Application Information (Continued)

Consider the following application example:

Example #1

K_{VCO} = 34 MHz/V

$K\phi$ = 2.8 mA (Note 1)

RF_{opt} = 1665 MHz

F_{ref} = 300 kHz

$N = RF_{opt}/f_{ref}$ = 5550

$\omega_p = 2\pi * 20$ kHz = 1.256e5

ϕ_p = 43

ATTEN = 12 dB

$$T1 = \frac{\sec\phi - \tan\phi}{\omega_p} = 3.462e-6$$

$$T3 = \sqrt{\frac{10^{(12/20)} - 1}{(2\pi \bullet 300e3)^2}} = 9.16e-7$$

$$\omega_c = \frac{\tan 43\,(3.862e-6 + 9.16e-7)}{(3.462e-6 + 9.16e-7)^2 + 3.462e-6 \bullet 9.16e-7)} \bullet \left[\sqrt{1 + \frac{(3.462e-6 + 9.16e-7)^2 + 3.462e-6 \bullet 9.16e-7}{[\tan 43\,(3.462e-6 + 9.16e-7)]^2}} - 1\right]$$

$$T2 = \frac{1}{(9.682e4)^2\,(3.462e-6 + 9.16e-7)} = 2.437e-5$$

$$C1 = \frac{3.462e-6}{2.437e-5}\,\frac{(2.8e-3) \bullet 34e6}{(9.682e4)^2 \bullet 5550} \bullet \left[\frac{[1 + (9.682e4)^2 \bullet (2.437e-5)^2]}{[1 + (9.682e4)^2\,(3.462e-6)^2]\,[1 + (9.682e4)^2 \bullet (9.16e-7)^2]}\right]^{1/2}$$

$$= 0.63 \text{ nF}$$

$$C2 = 0.63 \text{ nF}\left(\frac{2.437e-5}{3.402e-6} - 1\right) = 3.88 \text{ nF};$$

$$R2 = \frac{2.437e-5}{3.88e-9} = 6.28 \text{ k}\Omega;$$

if we choose R3 = 27k; then $C3 = \frac{9.16e-7}{27e3} = 34$ pF.

Converting to standard component values gives the following filter values, which are shown in *Figure 4*.

C1 = 560 pF
R2 = 6.8 kΩ
C2 = 2700 pF
R3 = 27 kΩ
C3 = 56 pF

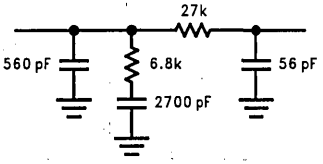


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FIGURE 4. ~20 kHz Loop Filter

Note 1: See related equation for Kϕ in Charge Pump Current Specification Definitions. For this example V_P = 3.3V. The value for Kϕ can then be approximated using the curves in the Typical Performance Characteristics for Charge Pump Current vs. D_O Voltage. The units for Kϕ are in mA. You may also use $K\phi = (2.8 \text{ mA}/2\pi \text{ rad})$, but in this case you must convert K_{VCO} to (rad/V) multiplying by 2π.

Application Information (Continued)

MEASUREMENT RESULTS

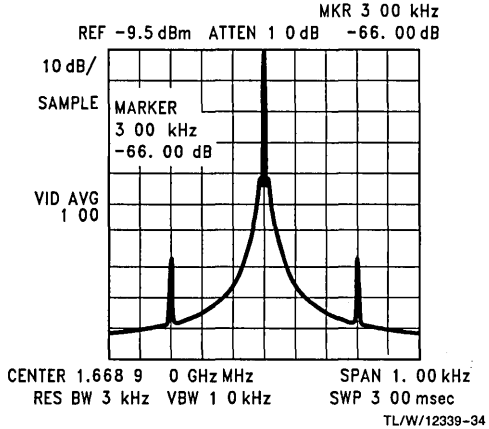

FIGURE 5. PLL Reference Spurs

The reference spurious level is < −65 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2320.

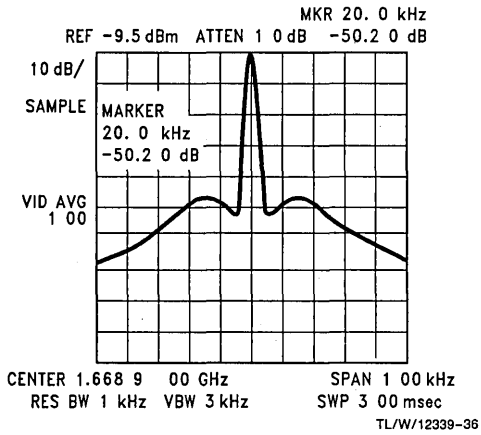

FIGURE 6. PLL Phase Noise 20 kHz Offset

The phase noise level at 20 kHz offset is −80 dBc/Hz.

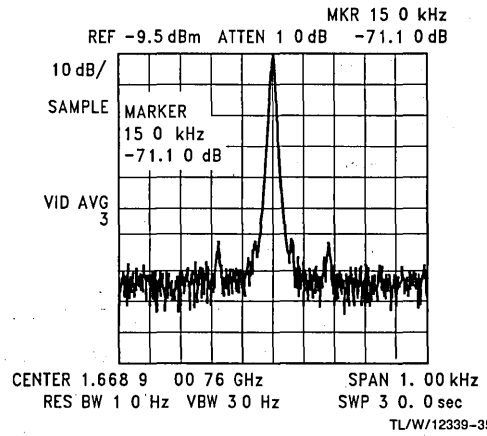

FIGURE 7. PLL Phase Noise @ 150 Hz Offset

The phase noise level at 150 Hz offset is −81.1 dBc/Hz. The spurs at 60 and 180 Hz offset are due to 60 Hz line noise from the power supply.

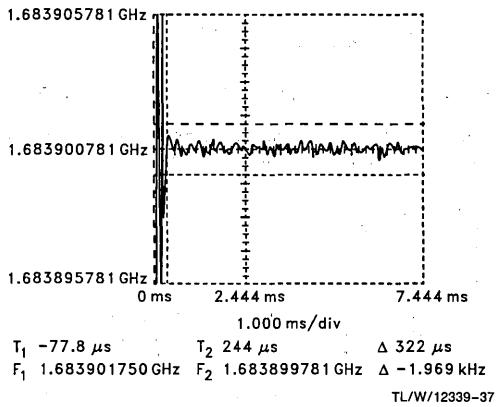

FIGURE 8. Frequency Jump Lock Time

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. *Figure 8* shows the switching waveforms for a frequency jump of 1650.9 MHz to 1683.9 MHz. By narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±1 kHz. The lock time is seen to be less than 500 µs for a frequency jump of 33 MHz.

Application Information (Continued)

EXTERNAL CHARGE PUMP

The LMX PLLatinum series of frequency synthesizers are equipped with an internal balanced charge pump as well as outputs for driving an external charge pump. Although the superior performance of NSC's on board charge pump eliminates the need for an external charge pump in most applications, certain system requirements are more stringent. In these cases, using an external charge pump allows the designer to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation.

One possible architecture for an external charge pump current source is shown in *Figure 9*. The signals ϕ_p and ϕ_r in the diagram, correspond to the phase detector outputs of the 2320/25 frequency synthesizers. These logic signals are converted into current pulses, using the circuitry shown in *Figure 9*, to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

Referring to *Figure 9*, the design goal is to generate a 5 mA current which is relatively constant to within 5V of the power supply rail. To accomplish this, it is important to establish as large of a voltage drop across R5, R8 as possible without saturating Q2, Q4. A voltage of approximately 300 mV provides a good compromise. This allows the current source reference being generated to be relatively repeatable in the absence of good Q1, Q2/Q3, Q4 matching. (Matched transistor pairs is recommended.) The ϕp and ϕr outputs are rated for a maximum output load current of 1 mA while 5 mA current sources are desired. The voltages developed across R4, 9 will consequently be approximately 258 mV, or 42 mV less than R8, 5, due to the current density differences {0.026*1n (5 mA/1 mA)} through the Q1, Q2/Q3, Q4 pairs.

In order to calculate the value of R7 it is necessary to first estimate the forward base to emitter voltage drop (Vfn,p) of the transistors used, the V_{OL} drop of ϕp, and the V_{OH} drop of ϕr's under 1 mA loads. (ϕp's V_{OL} < 0.1V and (ϕr,s V_{OH} < 0.1V).

Knowing these parameters along with the desired current allow us to design a simple external charge pump. Separating the pump up and pump down circuits facilitates the nodal analysis and give the following equations.

$$R_4 = \frac{V_{R5} - V_T \bullet 1n\left(\frac{i_{source}}{i_{p\,max}}\right)}{i_{source}}$$

$$R_9 = \frac{V_{R8} - V_T \bullet 1n\left(\frac{i_{sink}}{i_{n\,max}}\right)}{i_{sink}}$$

$$R_5 = \frac{V_{R5} \bullet (\beta_p + 1)}{i_{p\,max} \bullet (\beta_p + 1) - i_{source}}$$

$$R_8 = \frac{V_{R8} \bullet (\beta_n + 1)}{i_{r\,max} \bullet (\beta_n + 1)\, i_{sink}}$$

$$R_6 = \frac{(V_p - V_{VOL\phi p}) - (V_{R5} + Vfp)}{i_{p\,max}}$$

$$R_7 = \frac{(V_P - V_{VOH\phi p}) - (V_{R8} + Vfn)}{i_{max}}$$

EXAMPLE

Typical Device Parameters	$\beta_n = 100$, $\beta_p = 50$
Typical System Parameters	$V_P = 5.0V$;
	$V_{cntl} = 0.5V–4.5V$;
	$V_{\phi p} = 0.0V$, $V_{\phi r} = 5.0V$
Design Parameters	$I_{SINK} = I_{SOURCE} = 5.0$ mA;
	$Vfn = Vfp = 0.8V$
	$I_{r_{max}} = I_{p_{max}} = 1$ mA
	$V_{R8} = V_{R5} = 0.3V$
	$V_{OL\phi p} = V_{OH\phi p} = 100$ mV

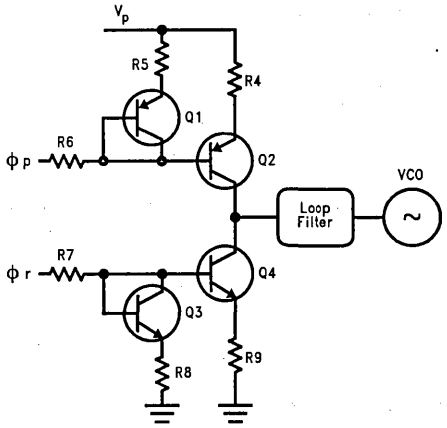

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FIGURE 9

Therefore select

$$R_4 = R_9 = \frac{0.3V - 0.026 \bullet 1n(5.0\text{ mA}/1.0\text{ mA})}{5\text{ mA}} = 51.6\Omega$$

$$R_5 = \frac{0.3V \bullet (50 + 1)}{1.0\text{ mA} \bullet (50 + 1) - 5.0\text{ mA}} = 332\Omega$$

$$R_8 = \frac{0.3V \bullet (100 + 1)}{1.0\text{ mA} \bullet (100 + 1) - 5.0\text{ mA}} = 315.6\Omega$$

$$R_6 = R_7 = \frac{(5V - 0.1V) - (0.3V + 0.8V)}{1.0\text{ mA}} = 3.8\text{ k}\Omega$$

National Semiconductor

PRELIMINARY

LMX2330A/LMX2331A/LMX2332A PLLatinum™ Dual Frequency Synthesizer for RF Personal Communications

LMX2330A 2.5 GHz/510 MHz
LMX2331A 2.0 GHz/510 MHz
LMX2332A 1.2 GHz/510 MHz

General Description

The LMX233xA family of monolithic, integrated dual frequency synthesizers, including prescalers, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver. It is fabricated using National's ABiC IV silicon BiCMOS process.

The LMX233xA contains dual modulus prescalers. A 64/65 or a 128/129 prescaler (32/33 or 64/65 in the 2.5 GHz LMX2330A) can be selected for the RF synthesizer and a 8/9 or a 16/17 prescaler can be selected for the IF synthesizer. Using a digital phase locked loop technique, the LMX233xA can generate a very stable, low noise signal for the RF and IF local oscillator. Serial data is transferred into the LMX233xA via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX233xA family features very low current consumption; LMX2330A—13 mA at 3V, LMX2331A—12 mA at 3V, LMX2332A—8 mA at 3V.

The LMX233xA are available in a TSSOP 20-pin surface mount plastic package.

Features

- 2.7V to 5.5V operation
- Low current consumption
- Selectable powerdown mode: I_{CC} = 1 μA typical at 3V
- Dual modulus prescaler:

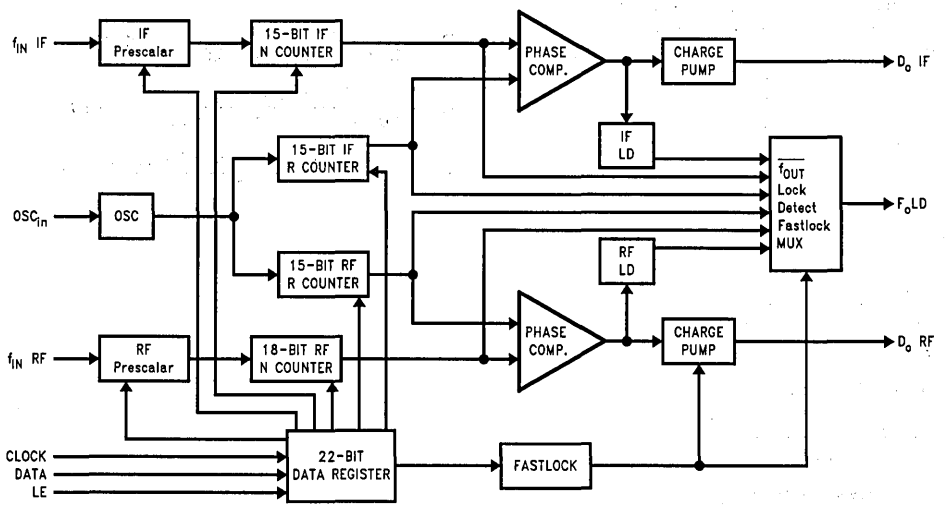
LMX2330A	(RF) 32/33 or 64/65
LMX2331A/32A	(RF) 64/65 or 128/129
LMX2330A/31A/32A	(IF) 8/9 or 16/17

- Selectable charge pump TRI-STATE® mode
- Selectable Fastlock™ mode

Applications

- Portable Wireless Communications (PCS/PCN, cordless)
- Cordless and cellular telephone systems
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Other wireless communication systems

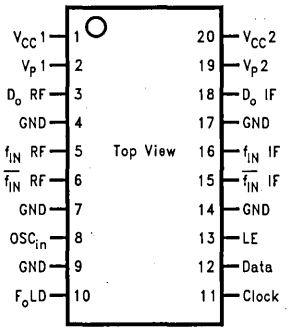
Functional Block Diagram



TL/W/12331–1

Connection Diagram

Thin Shrink Small Outline Package (TM)



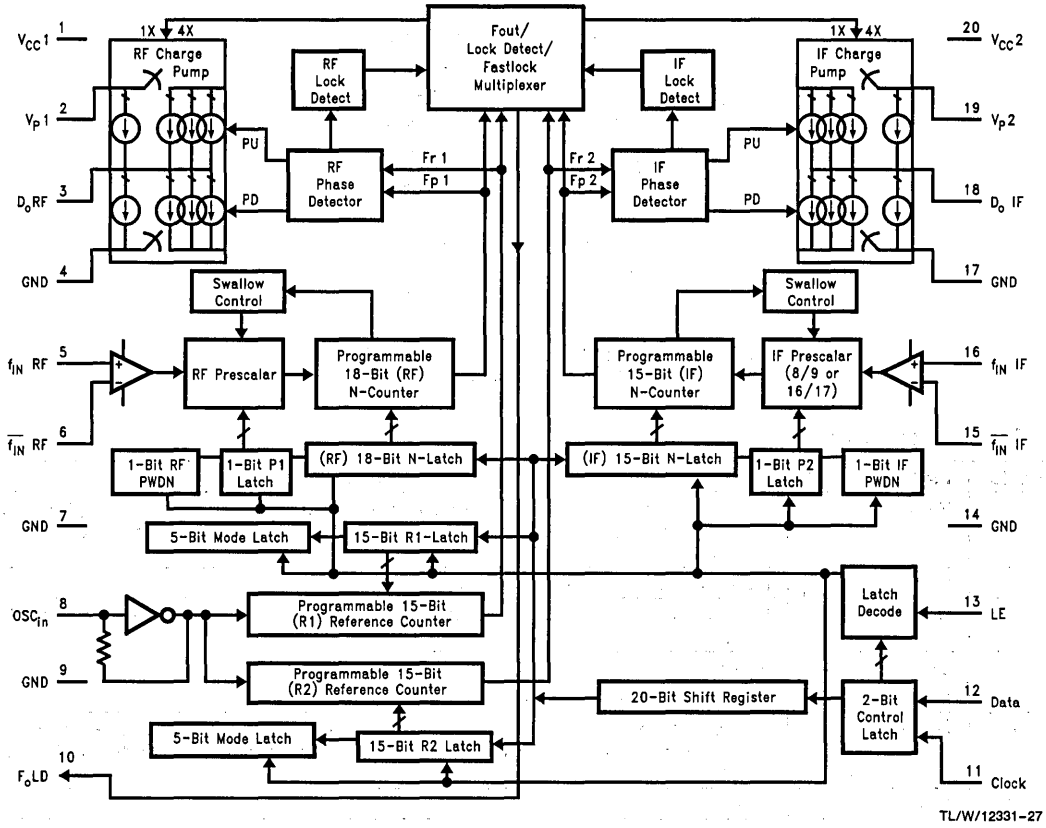
TL/W/12331–2

Order Number LMX2330ATM, LMX2331ATM or LMX2332ATM
NS Package Number MTC20

Pin Description

Pin No.	Pin Name	I/O	Description
1	$V_{CC}1$	—	Power supply voltage input. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	V_P1	—	Power Supply for RF charge pump. Must be ≥ V_{CC}.
3	D_o RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	GND	—	Ground.
5	f_{IN} RF	I	RF prescaler input. Small signal input from the VCO.
6	$\overline{f_{IN}}$ RF	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	GND	—	Ground.
8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
9	GND	—	Ground.
10	F_oLD	O	Multiplexed output of the RF/IF programmable or reference dividers, RF/IF lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes).*
11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	LE	I	Load enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
14	GND	—	Ground.
15	$\overline{f_{IN}}$ IF	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
16	f_{IN} IF	I	IF prescaler input. Small signal input from the VCO.
17	GND	—	Ground.
18	D_o IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_P2	—	Power Supply for IF charge pump. Must be ≥ V_{CC}.
20	$V_{CC}2$	—	Power supply voltage input. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

Block Diagram



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Note 1: The RF prescalar for the LMX2331A/32A is either 64/65 or 128/129, while the prescalar for the LMX2330A is 32/33 or 64/65.

Note 2: $V_{CC}1$ supplies power to the RF prescaler, N-counter and phase detector. $V_{CC}2$ supplies power to the IF prescaler, N-counter and phase detector, RF and IF R-counters along with the OSC_{IN} buffer and all digital circuitry. $V_{CC}1$ and $V_{CC}2$ are separated by a diode and must be run at the same voltage level.

Note 3: V_P1 and V_P2 can be run independently as long as $V_P \geq V_{CC}$.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage
- V_{CC} −0.3V to +6.5V
- V_P −0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) −0.3V to +6.5V

Storage Temperature Range (T_S) −65°C to +150°C

Lead Temperature (solder 4 sec.) (T_L) +260°C

Recommended Operating Conditions

Power Supply Voltage
- V_{CC} 2.7V to 5.5V
- V_P V_{CC} to +5.5V

Operating Temperature (T_A) −40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2330A RF + IF	V_{CC} = 2.7V to 5.5V		13		mA
		LMX2330A RF Only			10		
		LMX2331A RF + IF			12		
		LMX2331A RF Only			9		
		LMX2332A IF + RF			8		
		LMX2332A RF Only			5		
		LMX233XA IF Only			3		
$I_{CC-PWDN}$	Powerdown Current		V_{CC} = 3.0V		1	25	μA
f_{IN} RF	Operating Frequency	LMX2330A		500		2.5	GHz
		LMX2331A		200		2.0	
		LMX2332A		100		1.2	
f_{IN} IF	Operating Frequency	LMX233XA		45		510	MHz
f_{OSC}	Maximum Oscillator Frequency			40			MHz
f_ϕ	Maximum Phase Detector Frequency			10			MHz
Pf_{IN} RF	RF Input Sensitivity		V_{CC} = 3.0V	−15		+4	dBm
			V_{CC} = 5.0V	−10		+4	dBm
Pf_{IN} IF	IF Input Sensitivity		V_{CC} = 2.7V to 5.5V	−10		+4	dBm
V_{OSC}	Oscillator Sensitivity		OSC_{in}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage		*	0.8 V_{CC}			V
V_{IL}	Low-Level Input Voltage		*			0.2 V_{CC}	V
I_{IH}	High-Level Input Current		V_{IH} = V_{CC} = 5.5V*	−1.0		1.0	μA
I_{IL}	Low-Level Input Current		V_{IL} = 0V, V_{CC} = 5.5V*	−1.0		1.0	μA
I_{IH}	Oscillator Input Current		V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}	Oscillator Input Current		V_{IL} = 0V, V_{CC} = 5.5V	−100			μA
V_{OH}	High-Level Output Voltage		I_{OH} = −500 μA	V_{CC} − 0.4			V
V_{OL}	Low-Level Output Voltage		I_{OL} = 500 μA			0.4	V
t_{CS}	Data to Clock Set Up Time		See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time		See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High		See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low		See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time		See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width		See Data Input Timing	50			ns

*Clock, Data and LE does not include f_{IN} RF, f_{IN} IF and OSC_{IN}.

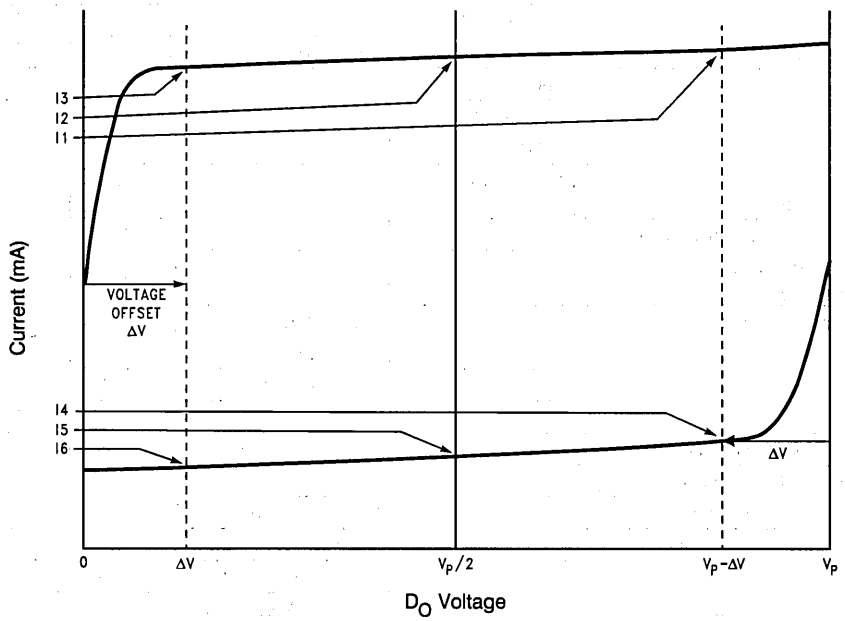
Charge Pump Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{D_O}-SOURCE	Charge Pump Output Current	$V_{D_O} = V_P/2$, I_{CP_O} = HIGH**		−5.0		mA
I_{D_O}-SINK		$V_{D_O} = V_P/2$, I_{CP_O} = HIGH**		5.0		mA
I_{D_O}-SOURCE		$V_{D_O} = V_P/2$, I_{CP_O} = LOW**		−1.25		mA
I_{D_O}-SINK		$V_{D_O} = V_P/2$, I_{CP_O} = LOW**		1.25		mA
I_{D_O}-TRI	Charge Pump TRI-STATE Current	$0.5V \le V_{D_O} \le V_P - 0.5V$ −40°C < T_A < 85°C	−2.5		2.5	nA
I_{D_O}-SINK vs I_{D_O}-SOURCE	CP Sink vs Source Mismatch (Note 2)	$V_{D_O} = V_P/2$ T_A = 25°C		3	10	%
I_{D_O} vs V_{D_O}	CP Current vs Voltage (Note 1)	$0.5 \le V_{D_O} \le V_P - 0.5V$ T_A = 25°C		10	15	%
I_{D_O}vs T_A	CP Current vs Temperature (Note 3)	$V_{D_O} = V_P/2$ −40°C < T_A < 85°C		10		%

** See PROGRAMMABLE MODES for I_{CP_O} description.

Notes 1, 2, 3: See charge pump current specification definitions below.

Charge Pump Current Specification Definitions



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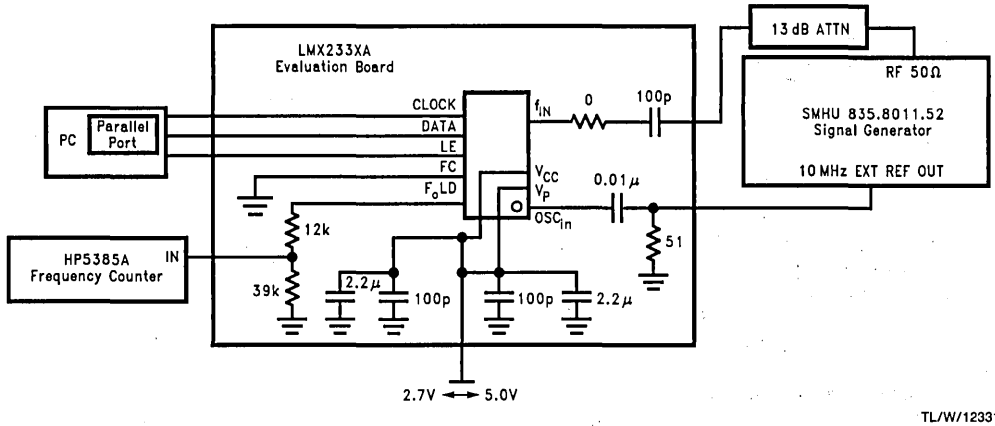
I1 = CP sink current at $V_{D_O} = V_P - \Delta V$
I2 = CP sink current at $V_{D_O} = V_P/2$
I3 = CP sink current at $V_{D_O} = \Delta V$
I4 = CP source current at $V_{D_O} = V_P - \Delta V$
I5 = CP source current at $V_{D_O} = V_P/2$
I6 = CP source current at $V_{D_O} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

1. I_{D_O} vs V_{D_O} = Charge Pump Output Current magnitude variation vs Voltage =
$[½ * (|I1| - |I3|)]/[½ * (|I1| + |I3|)] * 100\%$ and $[½ * (|I4| - |I6|)]/[½ * (|I4| + |I6|)] * 100\%$
2. $I_{D_{O\text{-sink}}}$ vs $I_{D_{O\text{-source}}}$ = Charge Pump Output Current Sink vs Source Mismatch =
$[|I2| - |I5|]/[½ * (|I2| + |I5|)] * 100\%$
3. I_{D_O} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
$[|I2 @ temp| - |I2 @ 25°C|]/|I2 @ 25°C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25°C|]/|I5 @ 25°C| * 100\%$

RF Sensitivity Test Block Diagram



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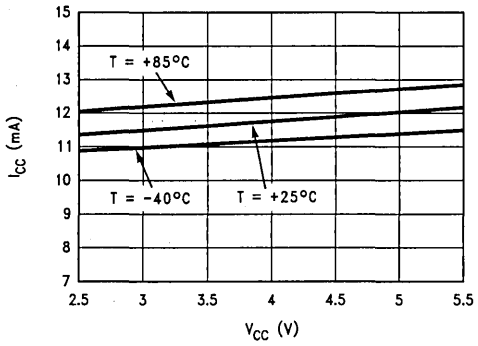
Note 1: N = 10,000 R = 50 P = 64

Note 2: Sensitivity limit is reached when the error of the divided RF output, F_oLD, is ≥ 1 Hz.

Typical Performance Characteristics

I_{CC} vs V_{CC} LMX2330A



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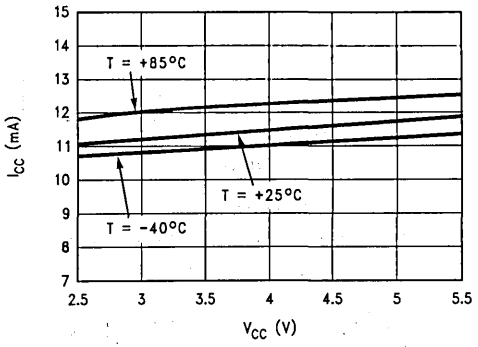
I_{CC} vs V_{CC} LMX2331A



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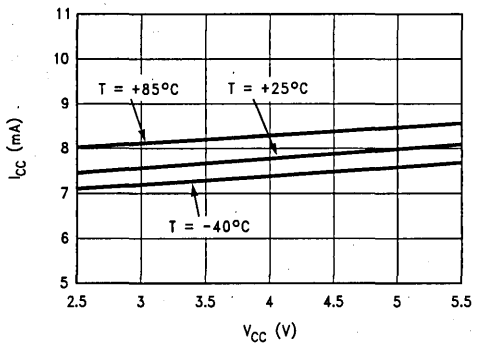
I_{CC} vs V_{CC} LMX2332A



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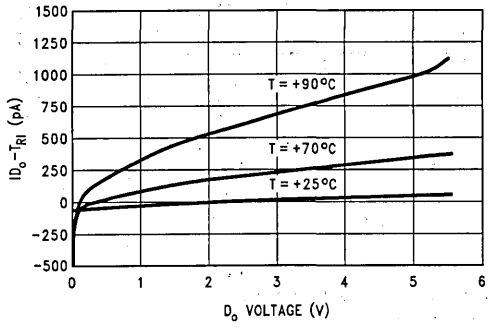
I_{DO} TRI-STATE vs D_o Voltage



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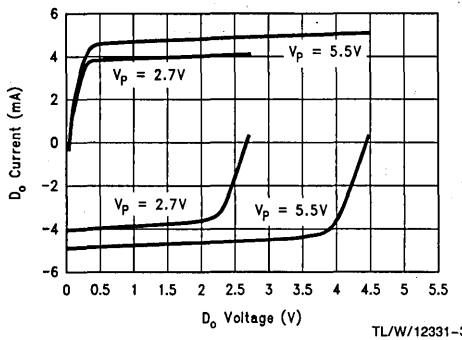
Typical Performance Characteristics (Continued)

Charge Pump Current vs D_O Voltage
I_{CP} = HIGH



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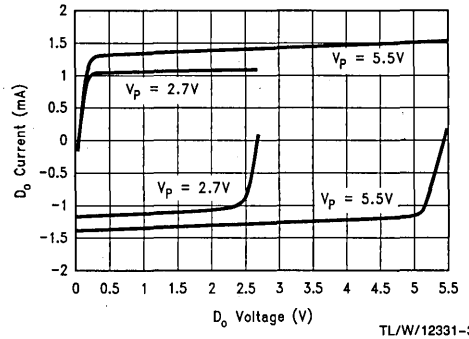
Charge Pump Current vs D_O Voltage
I_{CP} = LOW



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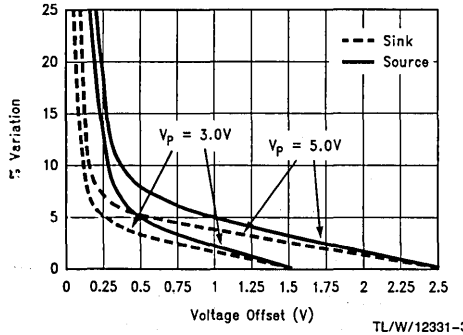
Charge Pump Current Variation
(See Note 1 under Charge Pump Current Specification Definitions)



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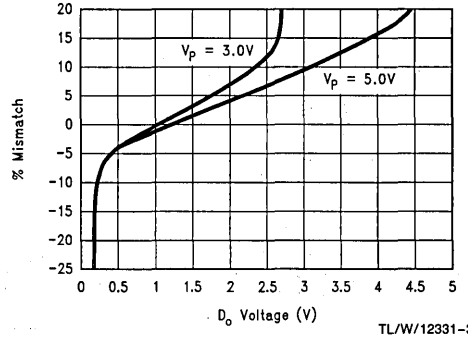
Sink vs Source Mismatch
(See Note 2 under Charge Pump Current Specification Definitions)



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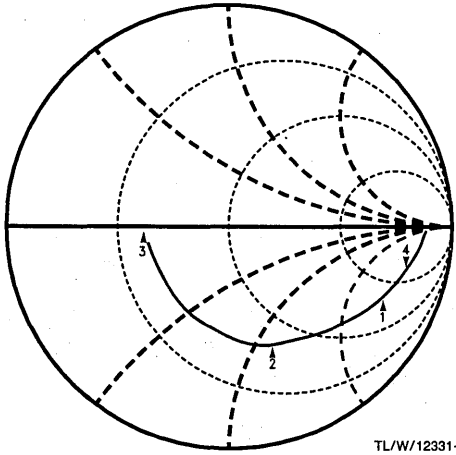
RF Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 50 MHz to 3 GHz



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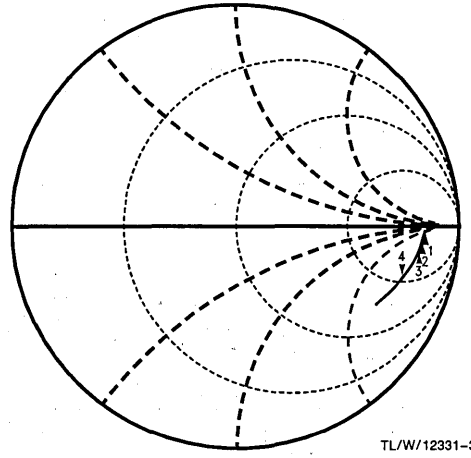
Marker 1 = 1 GHz, Real = 101, Imag. = −144
Marker 2 = 2 GHz, Real = 37, Imag. = −54
Marker 3 = 3 GHz, Real = 22, Imag. = −2
Marker 4 = 500 MHz, Real = 209, Imag. = −232

IF Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 10 MHz to 1000 MHz



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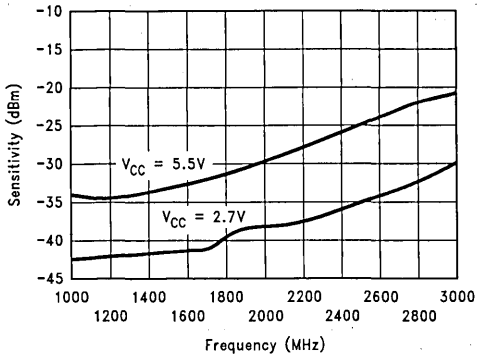
Marker 1 = 100 MHz, Real = 589, Imag. = −209
Marker 2 = 200 MHz, Real = 440, Imag. = −286
Marker 3 = 300 MHz, Real = 326, Imag. = −287
Marker 4 = 500 MHz, Real = 202, Imag. = −234

Typical Performance Characteristics (Continued)

LMX2330A RF Sensitivity vs Frequency



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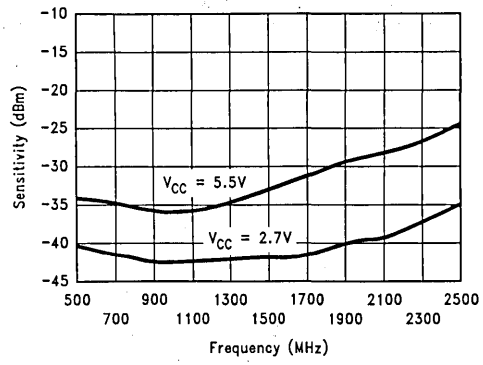
LMX2331A RF Sensitivity vs Frequency



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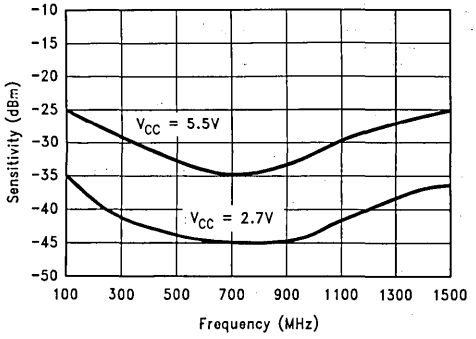
LMX2332A RF Sensitivity vs Frequency



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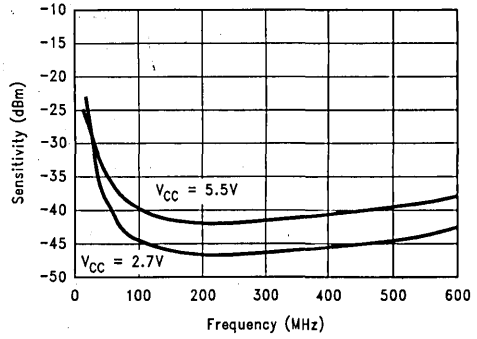
IF Input Sensitivity vs Frequency



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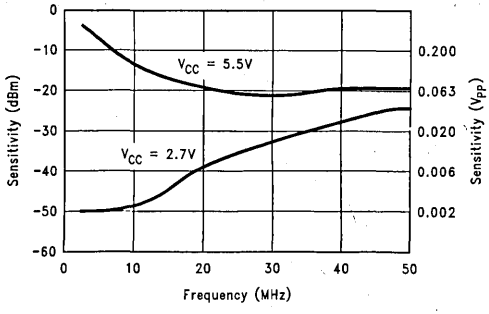
Oscillator Input Sensitivity vs Frequency



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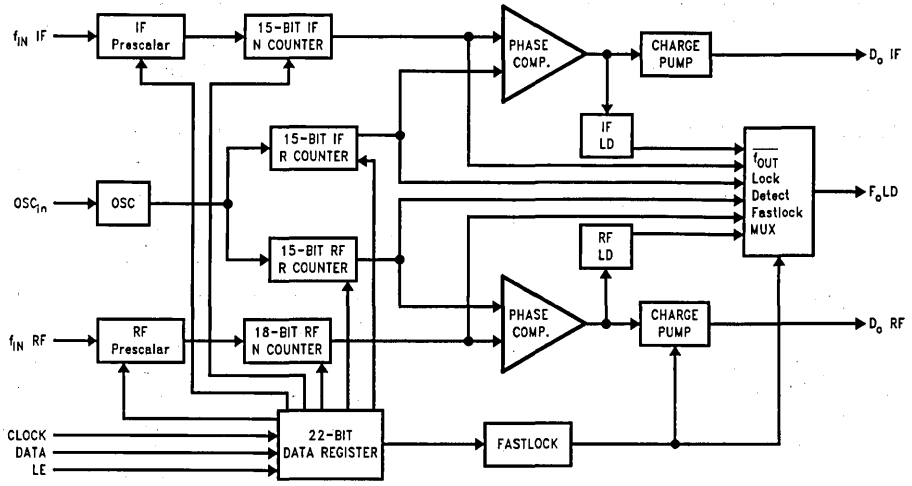
Functional Description

The simplified block diagram below shows the 22-bit data register, two 15-bit R Counters and the 15- and 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of LE) into the DATA input, MSB first. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	IF R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter



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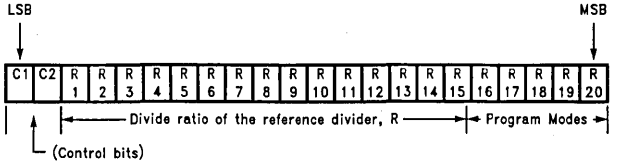
PROGRAMMABLE REFERENCE DIVIDERS (IF AND RF R COUNTERS)

If the Control Bits are 00 or 01 (00 for IF and 01 for RF) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



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15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 32767

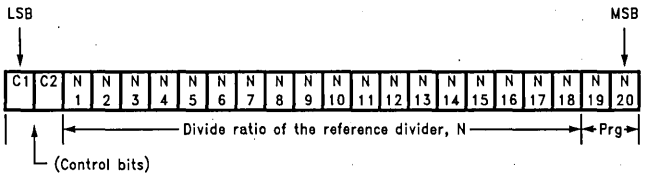
R1 to R15: These bits select the divide ratio of the programmable reference divider.

Data is shifted in MSB first.

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. **For the IF N counter bits 5, 6, and 7 are don't care bits.** The RF N counter does not have don't care bits.



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7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

RF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127
B ≥ A

IF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

X = DON'T CARE condition

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter
(0 ≤ A ≤ 127 {RF}, 0 ≤ A ≤ 15 {IF}, A ≤ B)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (for **IF**; P = 8 or 16;
for **RF**; LMX2330A: P = 32 or 64 LMX2331A/32A: P = 64 or 128)

Functional Description (Continued)

PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R16–R19 including the phase detector polarity, charge pump TRI-STATE and the output of the F_oLD pin. The prescaler and powerdown modes are selected with bits N19 and N20. The programmable modes are shown in Table I. Truth table for the programmable modes and F_oLD output are shown in Table II and Table III.

TABLE I. Programmable Modes

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CP_o}	IF D_o TRI-STATE	IF LD	IF F_o
0	1	RF Phase Detector Polarity	RF I_{CP_o}	RF D_o TRI-STATE	RF LD	RF F_o

C1	C2	N19	N20
1	0	IF Prescaler	Pwdn IF
1	1	RF Prescaler	Pwdn RF

TABLE II. Mode Select Truth Table

	Phase Detector Polarity	D_o TRI-STATE	I_{CP_o} (Note 1)	IF Prescaler	2330A RF Prescaler	2331A/32A RF Prescaler	Pwdn (Note 2)
0	Negative	Normal Operation	LOW	8/9	32/33	64/65	Pwrd Up
1	Positive	TRI-STATE	HIGH	16/17	64/65	128/129	Pwrd Dn

Note 1: The I_{CP_o} LOW current state = 1/4 × I_{CP_o} HIGH current.

Note 2: Activation of the IF PLL or RF PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_{IN} inputs (to a high impedance state). Powerdown forces the respective charge pump and phase comparator logic to a TRI-STATE condition after charge pump event. The R counter functionality does not become disabled until *both* IF and RF powerdown bits are activated. The MICROWIRE™ control register remains active amd capable of loading and latching data during all of the powerdown modes.

TABLE III. The F_oLD (Pin 10) Output Truth Table

RF R[19] (RF LD)	IF R[19] (IF LD)	RF R[20] (RF F_o)	IF R[20] (IF F_o)	F_o Output State
0	0	0	0	Disabled (Note 1)
0	1	0	0	IF Lock Detect (Note 2)
1	0	0	0	RF Lock Detect (Note 2)
1	1	0	0	RF/IF Lock Detect (Note 2)
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Fastlock (Note 3)
0	1	1	1	For Internal Use Only
1	0	1	1	For Internal Use Only
1	1	1	1	Counter Reset (Note 4)

X = don't care condition

Note 1: When the F_oLD output is disabled, it is actively pulled to a low logic state.

Note 2: Lock detect output provided to indicate when the VCO frequency is in "lock." When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF/IF lock detect mode a locked condition is indicated when RF and IF are both locked.

Note 3: The Fastlock mode utilizes the F_oLD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's Icpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).

Note 4: The Counter Reset mode bits R19 and R20 when activated reset all counters. Upon removal of the Reset bits then N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescalar cycle.) If the Reset bits are activated the R counter is also forced to Reset, allowing smooth acquisition upon powering up.

Functional Description (Continued)

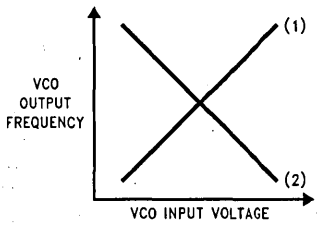
PHASE DETECTOR POLARITY

Depending upon VCO characteristics, R16 bit should be set accordingly: (see figure right)

When VCO characteristics are positive like (1), R16 should be set HIGH;

When VCO characteristics are negative like (2), R16 should be set LOW.

VCO Characteristics



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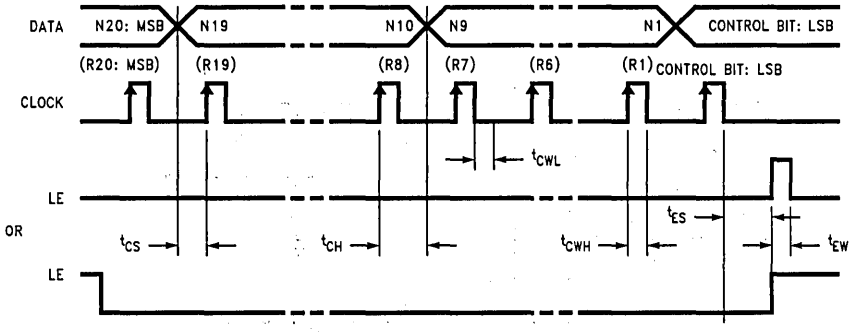
SERIAL DATA INPUT TIMING



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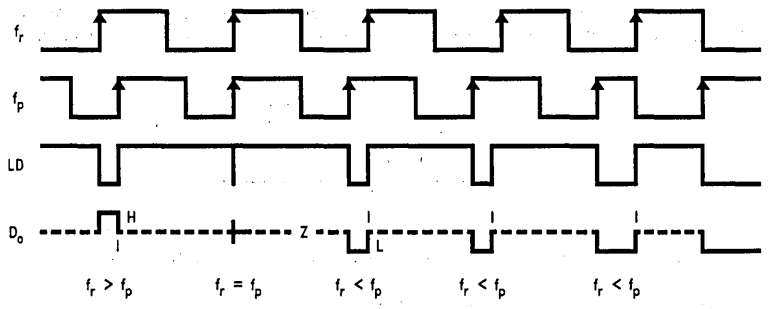
Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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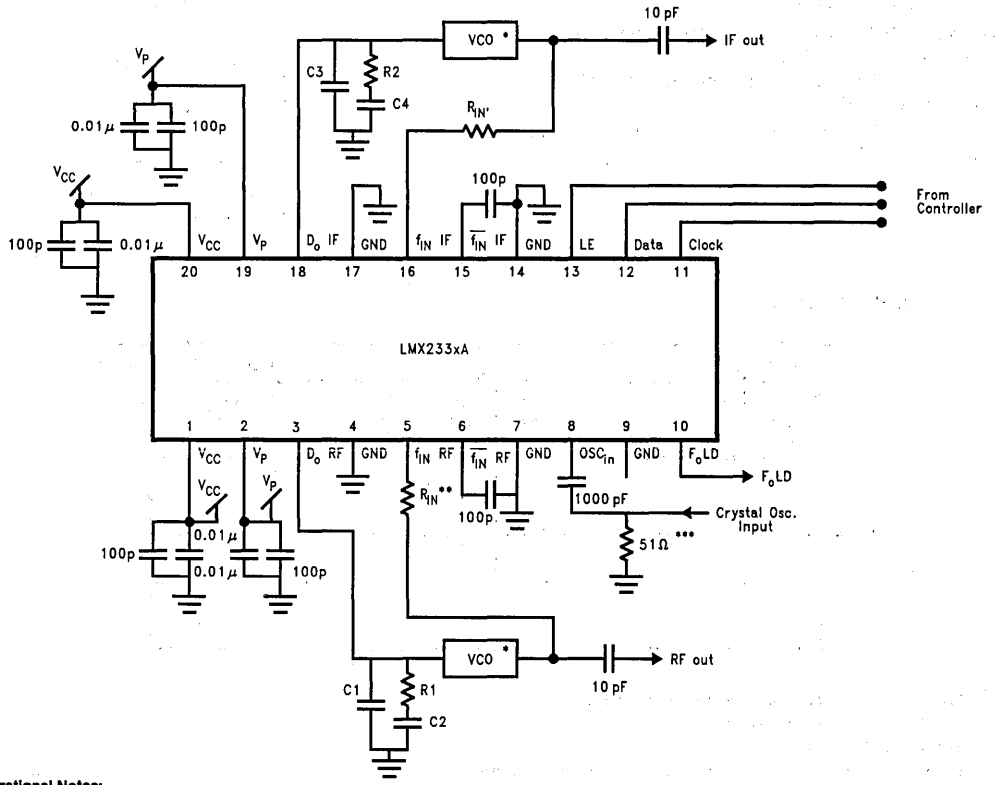
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

R16 = HIGH

Typical Application Example



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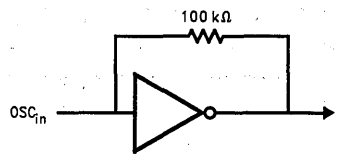
Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{in} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



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Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1.*

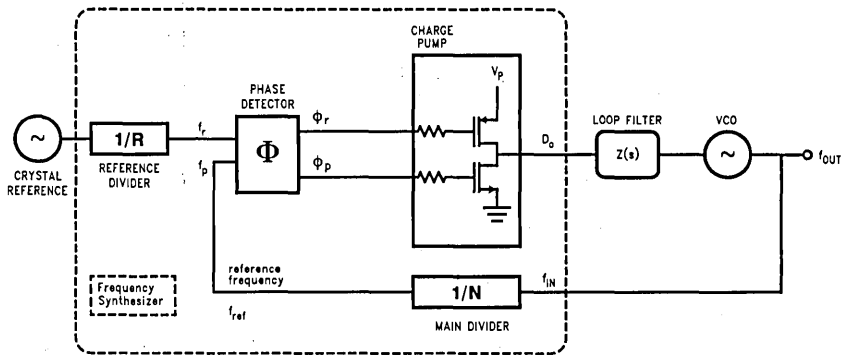

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FIGURE 1. Basic Charge Pump Phase Locked Loop

LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2.* The open loop gain is the product of the phase comparator gain (Kϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in equation 2.

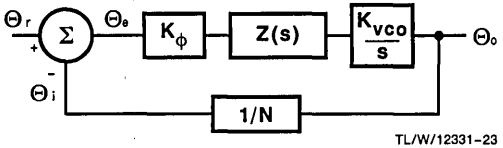

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FIGURE 2. PLL Linear Model

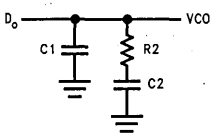

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FIGURE 3. Passive Loop Filter

$$\text{Open loop gain} = H(s)\,G(s) = \Theta i/\Theta e = K_\phi\,Z(s)\,K_{VCO}/Ns \quad (1)$$

$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$G(s) \bullet H(s)|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "1/w" or "1/w^2" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "w'" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2wp. K_{VCO}, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the w^2 term present in the denominator of equation 3. The Kϕ term was chosen to complete the transformation because it can readily be switch between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

Application Information (Continued)

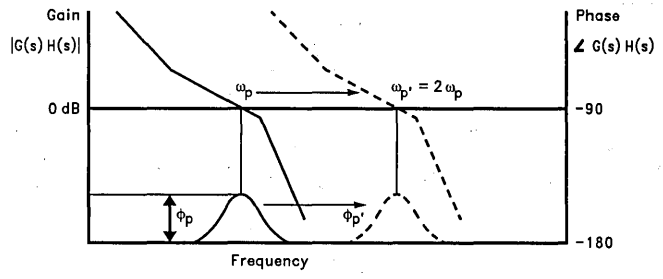

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FIGURE 4. Open Loop Response Bode Plot

FASTLOCK CIRCUIT IMPLEMENTATION

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX233xA PLL is shown in *Figure 5*. When a new frequency is loaded, and the RF Icp_o bit is set high the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF Icp_o bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

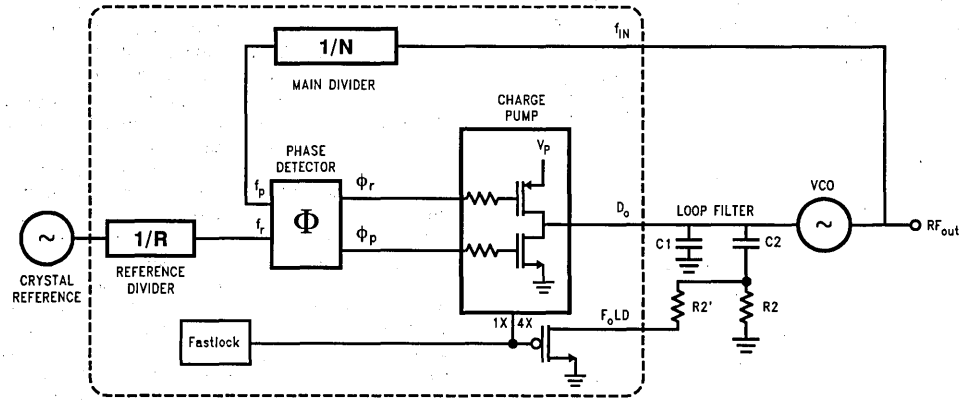

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FIGURE 5. Fastlock PLL Architecture

National Semiconductor

PRELIMINARY

LMX2335/LMX2336/LMX2337 PLLatinum™ Dual Frequency Synthesizer for RF Personal Communications

LMX2335 1.1 GHz/1.1 GHz
LMX2336 2.0 GHz/1.1 GHz
LMX2337 550 MHz/550 MHz

General Description

The LMX2335, LMX2336 and LMX2337 are monolithic, integrated dual frequency synthesizers, including two high frequency prescalers, and are designed for applications requiring two RF phase-lock loops. They are fabricated using National's ABiC IV silicon BiCMOS process.

The LMX2335/36/37 contains two dual modulus prescalers. A 64/65 or a 128/129 prescaler can be selected for each RF synthesizer. A second reference divider chain is included in the IC for improved system noise. Using a digital phase locked loop technique, the LMX2335/36/37 can generate two very stable, low noise signals for the RF local oscillators.

Serial data is transferred into the LMX2335/36/37 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2335/36/37 feature very low current consumption; LMX2335/37 −9 mA at 3V, LMX2336 −13 mA at 3V. The LMX2335/37 are available in a JEDEC 16-pin surface mount plastic package. The LMX2336 is available in a TSSOP 20-pin surface mount plastic package.

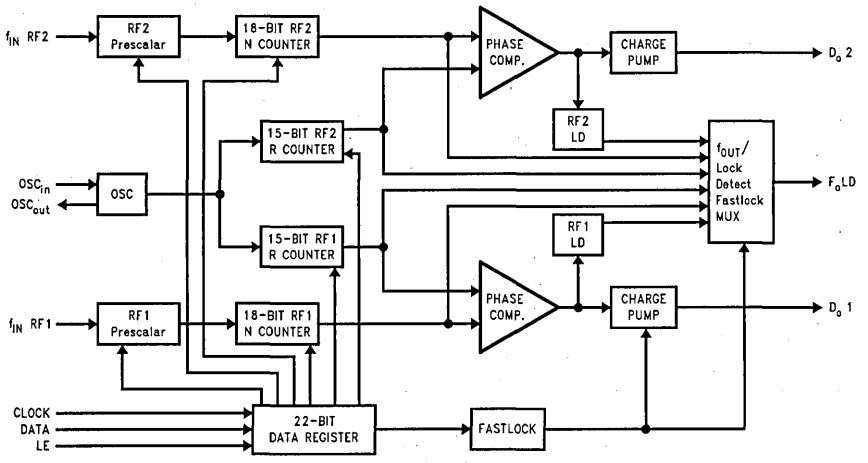
Features

- 2.7V to 5.5V operation
- Low current consumption
- Selectable powerdown mode: I_{CC} = 1 μA (typ)
- Dual modulus prescaler: 64/65 or 128/129
- Selectable charge pump TRI-STATE® mode
- Selectable charge pump current levels
- Selectable Fastlock™ mode

Applications

- Cellular telephone systems (AMPS, ETACS, RCR-27)
- Cordless telephone systems (DECT, ISM , PHS, CT-1+)
- Personal Communication Systems (DCS-1800, PCN-1900)
- Dual Mode PCS phones
- CATV
- Other wireless communication systems

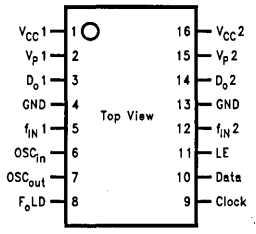
Functional Block Diagram



TL/W/12332–1

Connection Diagrams

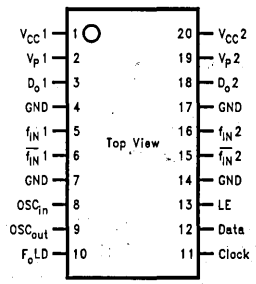
Small Outline Molded Package (M)



TL/W/12332-2

Order Number LMX2335M/LMX2337M
NS Package Number M16A

LMX2336



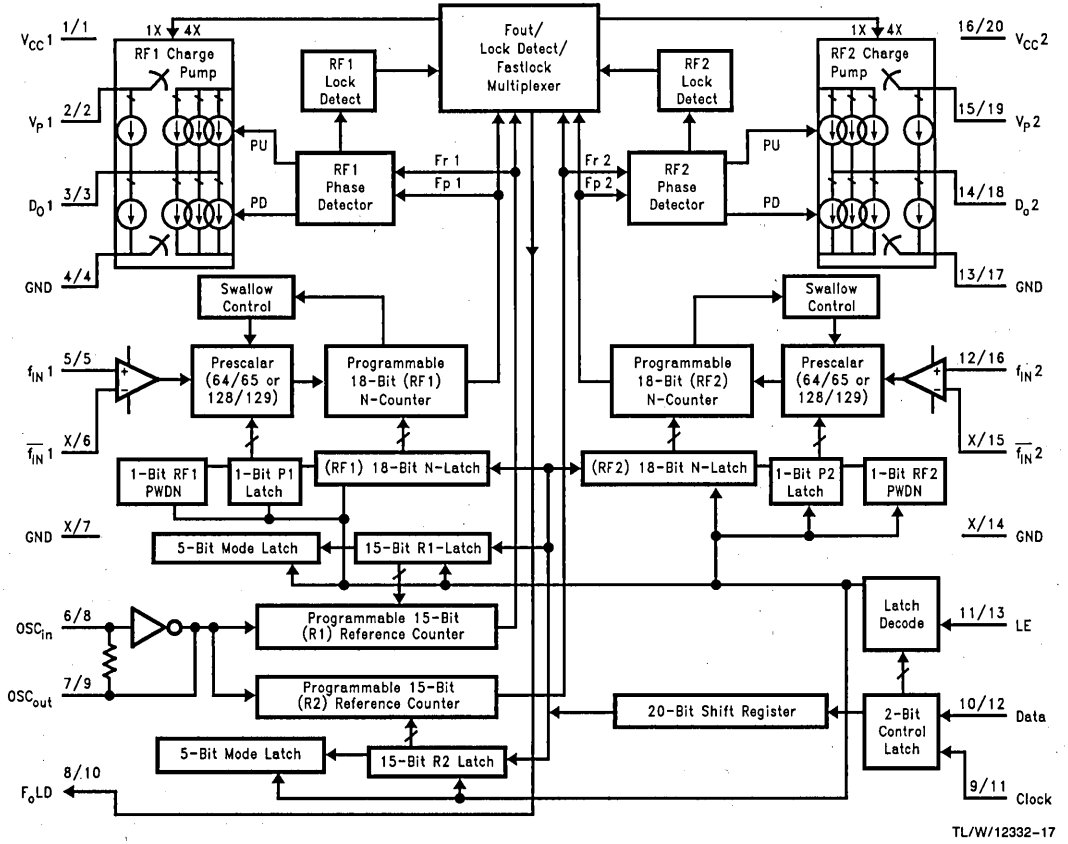
TL/W/12332-16

Order Number LMX2336TM
NS Package Number MTC20

Pin Description

Pin No. 2335/37	Pin No. 2336	Pin Name	I/O	Description
1	1	$V_{CC}1$		Power supply voltage input. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	2	V_p1		Power supply for RF1 charge pump. Must be $\geq V_{CC}$.
3	3	D_o1	O	RF1 charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	4	GND		Ground.
5	5	$f_{IN}1$	I	First RF prescaler input. Small signal input from the VCO.
X	6	$\overline{f_{IN}}1$	I	RF 1 prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity.
X	7	GND		Ground.
6	8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
7	9	OSC_{out}	O	Oscillator output.
8	10	F_oLD	O	Multiplexed output of the programmable or reference dividers, lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes).*
9	11	Clock	I	High impedance CMOS Clock input. Data for the various latches is clocked in on the rising edge, into the 20-bit shift register.
10	12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
11	13	LE	I	Load enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
X	14	GND		Ground.
X	15	$\overline{f_{IN}}2$	I	RF2 prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity.
12	16	$f_{IN}2$	I	RF2 prescaler input. Small signal input from the VCO.
13	17	GND		Ground.
14	18	D_o2	O	RF2 charge pump output. For connection to a loop filter for driving the input of an external VCO.
15	19	V_p2		Power supply for RF2 charge pump. Must be $\geq V_{CC}$.
16	20	$V_{CC}2$		Power supply voltage input. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

Block Diagram



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LMX2335/37 Pin # → 8/10 ← LMX2336 Pin #
Pin Name → F_oLD
X signifies a function not bonded out to a pin

Note 1: $V_{CC}1$ supplies power to the RF1 prescalar, N-counter and phase detector. $V_{CC}2$ supplies power to the RF2 prescaler, N-counter and phase detector, RF1 and RF2 R-dividers along with the OSC_{IN} buffer and all digital circuitry. $V_{CC}1$ and $V_{CC}2$ are separated by a diode and must be run at the same voltage level.

Note 2: V_P1 and V_P2 can be run independently as long as $V_P \geq V_{CC}$.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (solder 4 sec.) (T_L)	+260°C

Recommended Operating Conditions

Power Supply Voltage	
V_{CC}	2.7V to 5.5V
V_P	V_{CC} to +5.5V
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2335/37 RF1 and RF2	V_{CC} = 2.7V to 5.5V		9	12	mA
I_{CC}		LMX2335/37 RF1 only	V_{CC} 2.7V to 5.5V		5	7	mA
I_{CC}		LMX2336 RF1 and RF2	V_{CC} = 2.7V to 5.5V		13	18	mA
		LMX2336 RF1 only	V_{CC} = 2.7V to 5.5V		7	11	mA
$f_{IN}1$	Operating Frequency	LMX2335		0.100		1.1	GHz
$f_{IN}2$				0.050		1.1	GHz
$f_{IN}1$		LMX2336		0.200		2.0	GHz
$f_{IN}2$				0.050		1.1	GHz
$f_{IN}1$		LMX2337		100		550	MHz
$f_{IN}2$				50		550	MHz
$I_{CC\text{-}PWDN}$	Powerdown Current	LMX2335/2336	V_{CC} = 5.5V		1	25	μA
		LMX2337				100	
f_{OSC}	Maximum Oscillator Frequency			20			MHz
f_{OSC}			No load on OSC_{out}	40			MHz
f_ϕ	Maximum Phase Detector Frequency				10		MHz
Pf_{IN}	RF Input Sensitivity		V_{CC} = 3.0V, f > 100 MHz	−15		+4	dBm
Pf_{IN}			V_{CC} = 5.0V, f > 100 MHz	−10		+4	
			V_{CC} = 2.7 to 5.5V, f < 100 MHz	−10		0	
V_{OSC}	Oscillator Sensitivity		OSC_{in}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage		**	0.8 V_{CC}			V
V_{IL}	Low-Level Input Voltage		**			0.2 V_{CC}	V
I_{IH}	High-Level Input Current		V_{IH} = V_{CC} = 5.5V**	−1.0		1.0	μA
I_{IL}	Low-Level Input Current		V_{IL} = 0V, V_{CC} = 5.5V**	−1.0		1.0	μA
I_{IH}	Oscillator Input Current		V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}	Oscillator Input Current		V_{IL} = 0V, V_{CC} = 5.5V	−100			μA
$I_{D_O\text{-}SOURCE}$	Charge Pump Output Current		V_{D_O} = V_{CC}/2, I_{CP_O} = LOW*		−1.25		mA
$I_{D_O\text{-}SINK}$			V_{D_O} = V_{CC}/2, I_{CP_O} = LOW*		1.25		mA
$I_{D_O\text{-}SOURCE}$			V_{D_O} = V_{CC}/2, I_{CP_O} = HIGH*		−5.0		mA
$I_{D_O\text{-}SINK}$			V_{D_O} = V_{CC}/2, I_{CP_O} = HIGH*		5.0		mA
$I_{D_O\text{-}TRI}$	Charge Pump TRI-STATE Current	LMX2335 LMX2336	0.5V ≤ V_{D_O} ≤ V_{CC} − 0.5V T = 25°C	−5.0		5.0	nA
$I_{D_O\text{-}TRI}$	Charge Pump TRI-STATE Current	LMX2337	0.5V ≤ V_{D_O} ≤ V_{CC} − 0.5V T = 25°C		5		nA

Electrical Characteristics V_{CC} = 5.0V, V_P = 5.0V; −40°C < T_A < 85°C, except as specified (Continued)

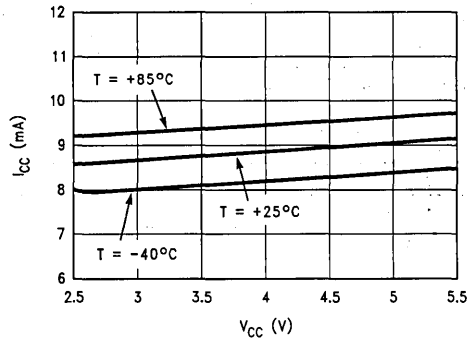
Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
V_{OH}	High-Level Output Voltage	I_{OH} = −500 μA	V_{CC} − 0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 500 μA			0.4	V
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns

*See PROGRAMMABLE MODES for I_{CP_o} description.

**Clock, Data and LE does not include $f_{IN}1$, $f_{IN}2$ and OSC_{in}.

Typical Performance Characteristics (Continued)

I_{CC} vs V_{CC}
LMX2335/37



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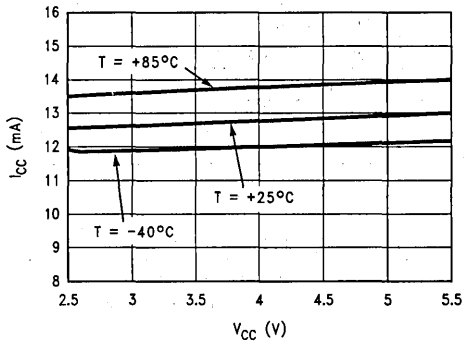
I_{CC} vs V_{CC}
LMX2336



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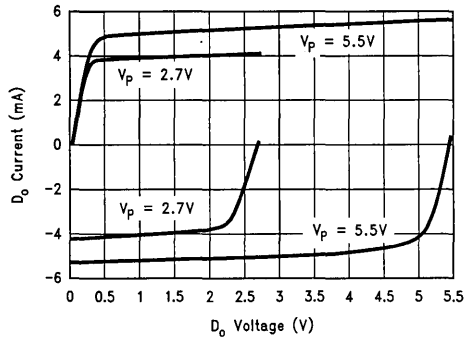
Charge Pump Current vs D_o Voltage
I_{CP} = HIGH



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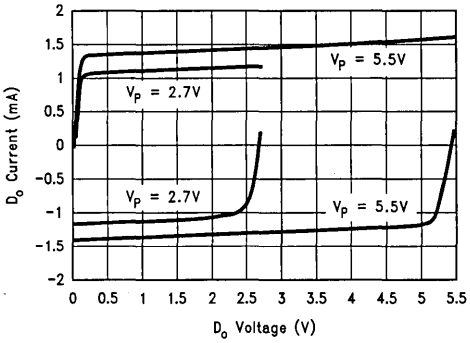
Charge Pump Current vs D_o Voltage
I_{CP} = LOW



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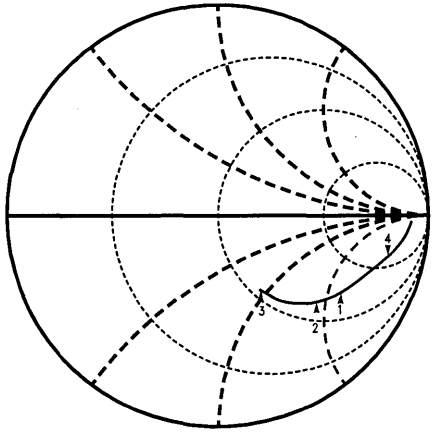
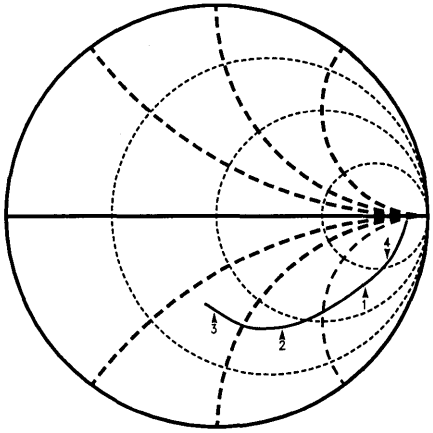
LMX2335 Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 50 MHz to 1.5 GHz



TL/W/12332-23

Marker 1 = 1 GHz, Real = 94, Image = −118
Marker 2 = 1.2 GHz, Real = 72, Image = −88
Marker 3 = 1.5 GHz, Real = 53, Image = −45
Marker 4 = 500 MHz, Real = 201, Image = −224

LMX2336 Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 50 MHz to 2.5 GHz

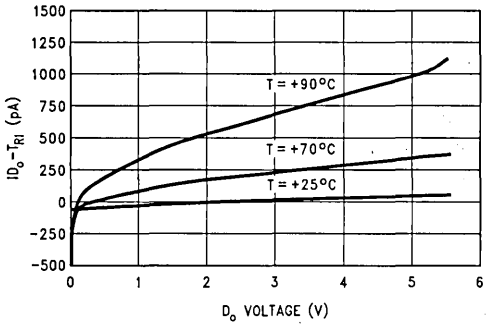


TL/W/12332-24

Marker 1 = 1 GHz, Real = 97, Image = −146
Marker 2 = 1.89 GHz, Real = 43, Image = −67
Marker 3 = 2.5 GHz, Real = 30, Image = −33
Marker 4 = 500 MHz, Real = 189, Image = −233

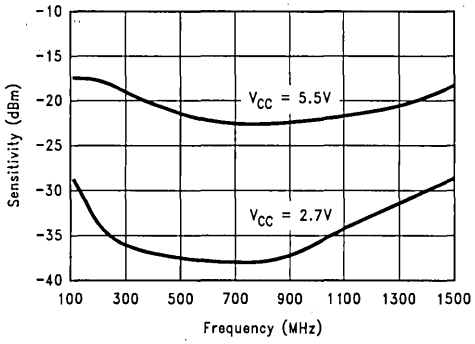
Typical Performance Characteristics (Continued)

I_{Do} TRI-STATE vs D_o Voltage



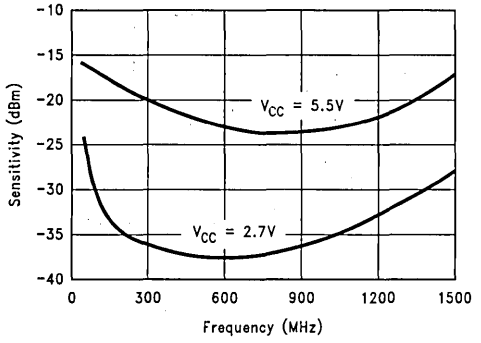
TL/W/12332-25

LMX2335/37 RF1 Sensitivity vs Frequency



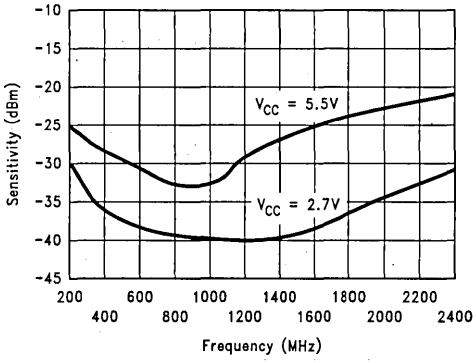
TL/W/12332-26

LMX2335/37 RF2 Sensitivity vs Frequency



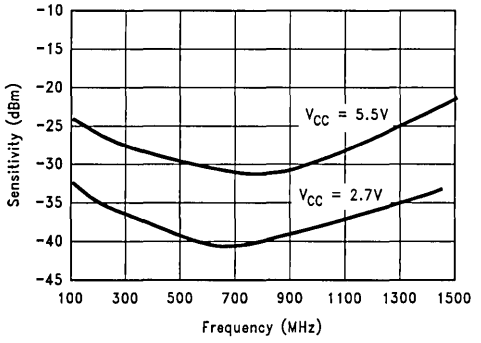
TL/W/12332-27

LMX2336 RF1 Sensitivity vs Frequency



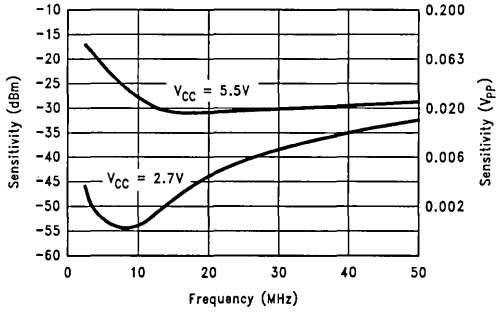
TL/W/12332-28

LMX2336 RF2 Sensitivity vs Frequency



TL/W/12332-29

Oscillator Input Sensitivity vs Frequency

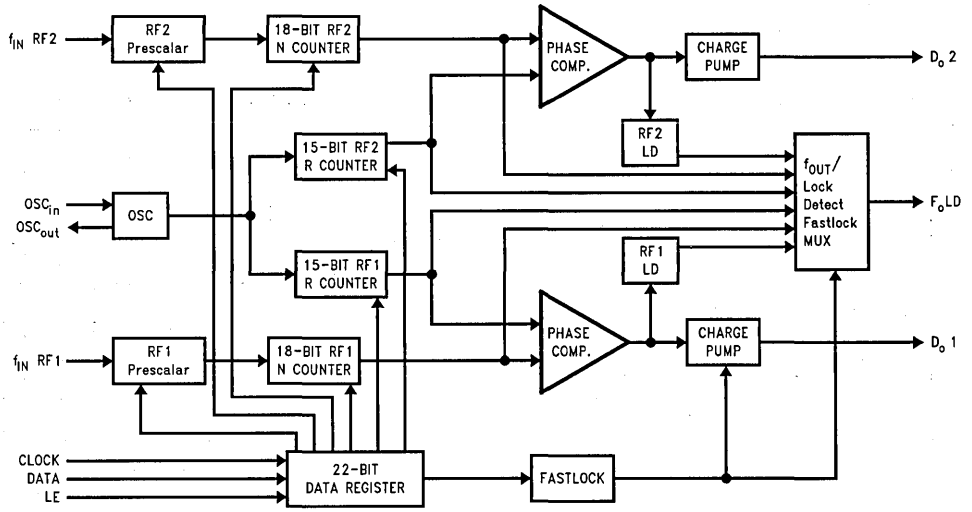


TL/W/12332-30

Functional Description

The simplified block diagram below shows the 22-bit data register, two 15-bit R Counters and two 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of LE) into the DATA input, MSB first. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	RF2 R Counter
0	1	RF1 R Counter
1	0	RF2 N Counter
1	1	RF1 N Counter

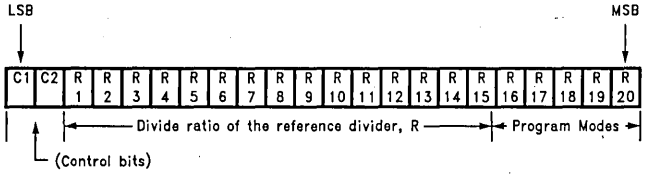


TL/W/12332-1

Functional Description (Continued)

PROGRAMMABLE REFERENCE DIVIDERS (RF1 AND RF2 R COUNTERS)

If the Control Bits are 00 or 01 (00 for RF2 and 01 for RF1) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



TL/W/12332–4

15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.

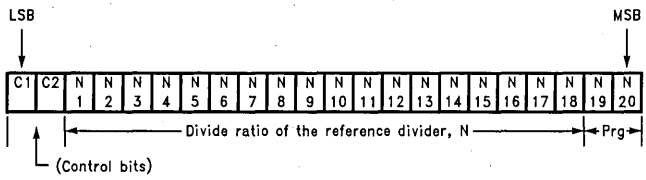
Divide ratio: 3 to 32767

R1 to R15: These bits select the divide ratio of the programmable reference divider.

Data is shifted in MSB first.

PROGRAMMABLE DIVIDER (N COUNTER)

Each N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for RF2 counter and 11 for RF1 counter) data is transferred from the 20-bit shift register into a 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below.



TL/W/12332–5

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127

$B \geq A$

$A < P$

Functional Description (Continued)

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter
(0 ≤ A ≤ P; A ≤ B)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (P = 64 or 128)

PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R16–R19 including the phase detector polarity, charge pump tristate and the output of the F_oLD pin. The prescaler and power down modes are selected with bits N19 and N20. The programmable modes are shown in Table I. Truth table for the programmable modes and F_oLD output are shown in Table II and Table III.

TABLE I. Programmable Modes

C1	C2	R16	R17	R18	R19	R20
0	0	RF2 Phase Detector Polarity	RF2 I_{CP_o}	RF2 D_o TRI-STATE	RF2 LD	RF2 F_o
0	1	RF1 Phase Detector Polarity	RF1 I_{CP_o}	RF1 D_o TRI-STATE	RF1 LD	RF1 F_o

C1	C2	N19	N20
1	0	RF2 Prescaler	Pwdn RF2
1	1	RF1 Prescaler	Pwdn RF1

Functional Description (Continued)

TABLE II. Mode Select Truth Table

	Phase Detector Polarity(3)	D_o TRI-STATE	I_{CP_o}(1)	RF1 Prescaler	RF2 Prescaler	Pwdn(2)
0	Negative	Normal Operation	LOW	64/65	64/65	pwrd up
1	Positive	TRI-STATE	HIGH	128/129	128/129	pwrd dn

Note 1: The I_{CP_o} LOW current state = 1/4 × I_{CP_o} HIGH current.

Note 2: Activation of the RF2 PLL or RF1 PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_{IN} inputs (to a high impedance state). Powerdown forces the respective charge pump and phase comparator logic to a TRI-STATE condition. The R counter and Oscillator functionality does not become disabled until *both* RF2 and RF1 powerdown bits are activated. The OSC_{in} pin reverts to a high impedance state when this condition exists. The MICROWIRE™ control register remains active and capable of loading and latching data during all of the powerdown modes.

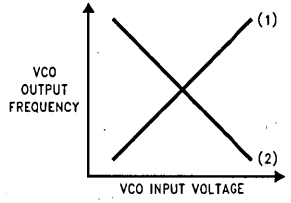
Note 3: PHASE DETECTOR POLARITY

Depending upon VCO characteristics, the R16 bits should be set accordingly:

When VCO characteristics are positive like (1), R16 should be set HIGH;

When VCO characteristics are negative like (2), R16 should be set LOW.

VCO Characteristics



TL/W/12332–7

TABLE III. The F_oLD Output Truth Table

RF1 R[19] (RF1 LD)	RF2 R[19] (RF2 LD)	RF1 R[20] (RF1 F_O)	RF2 R[20] (RF2 F_O)	F_oLD Output State
0	0	0	0	Disabled (Note 1)
0	1	0	0	RF2 Lock Detect (Note 2)
1	0	0	0	RF1 Lock Detect (Note 2)
1	1	0	0	RF1/RF2 Lock Detect (Note 2)
X	0	0	1	RF2 Reference Divider Output
X	0	1	0	RF1 Reference Divider Output
X	1	0	1	RF2 Programmable Divider Output
X	1	1	0	RF1 Programmable Divider Output
0	0	1	1	Fastlock (Note 3)
0	1	1	1	For Internal use only
1	0	1	1	For Internal use only
1	1	1	1	Counter Reset (Note 4)

X—don't care condition

Note 1: When the F_oLD output is disabled it is actively pulled to a low logic state.

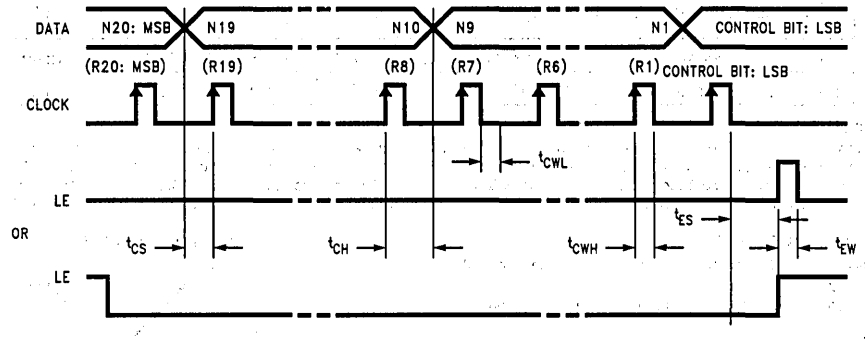
Note 2: Lock detect output provided to indicate when the VCO frequency is in "lock". When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF1/RF2 lock detect mode a locked condition is indicated when RF2 and RF1 are both locked.

Note 3: The Fastlock mode utilized the F_oLD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's Icpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).

Note 4: The Counter Reset mode bits R19 and R20 when activated reset all counters. Upon removal of the Reset bits the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescalar cycle). If the Reset bits are activated the R counter is also forced to Reset, allowing smooth acquisition upon powering up.

Functional Description (Continued)

SERIAL DATA INPUT TIMING



TL/W/12332–8

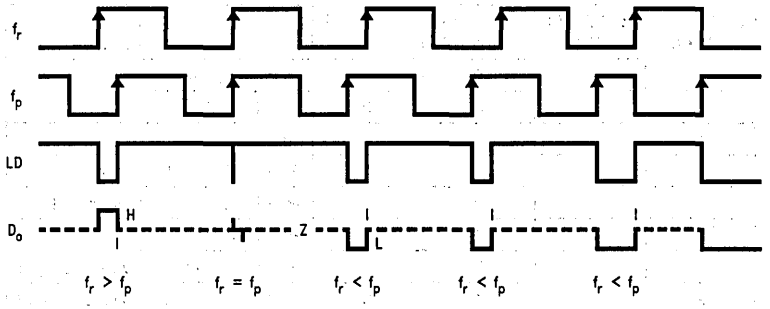
Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

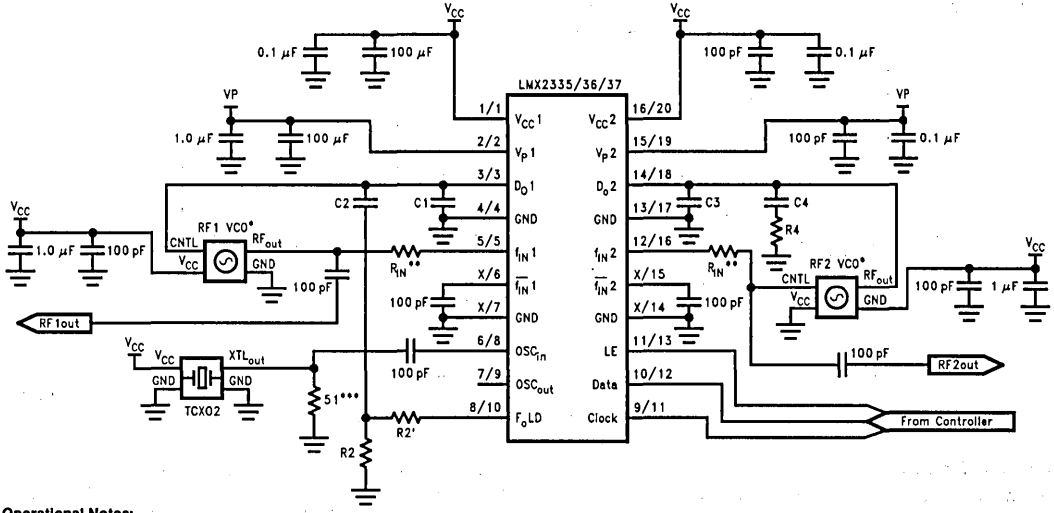


TL/W/12332–9

Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

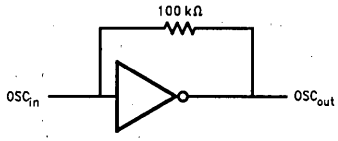
Typical Application Example



TL/W/12332–10

Operational Notes:

- VCO is assumed AC coupled.
- ** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.
- *** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{in} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below).



TL/W/12332–11

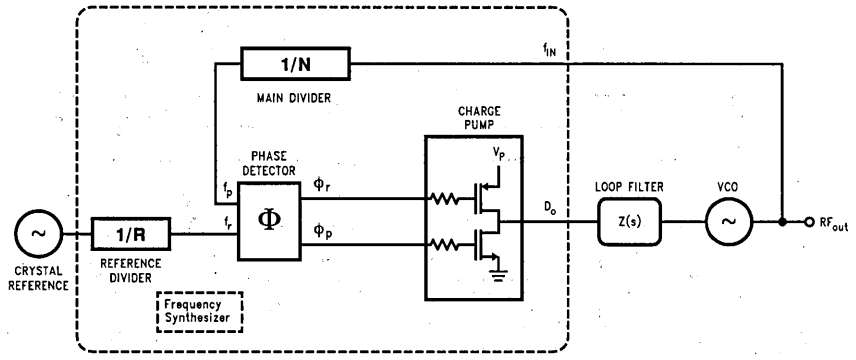
Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

1

Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1.*



TL/W/12332–12

FIGURE 1. Conventional PLL Architecture

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2.* The open loop gain is the product of the phase comparator gain (K_ϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3,* while the complex impedance of the filter is given in equation 2.

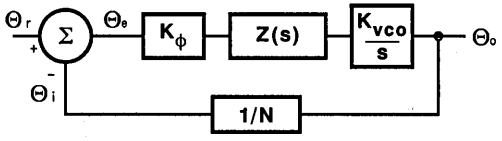


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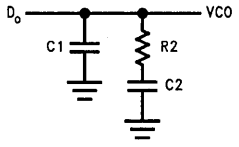
FIGURE 2. PLL Linear Model



TL/W/12332–13

FIGURE 3. Passive Loop Filter

$$\text{Open Loop gain} = H(s)\,G(s) = \frac{\Theta_i}{\Theta_e} = \frac{K_\phi\, Z(s)\, K_{VCO}}{Ns} \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{S^2 (C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time contants T1 and T2, and the design constants $K\phi$, K_{VCO}, and N.

$$G(s) \bullet H(s)\Big|_{S = j \bullet w} = \frac{-K\phi \bullet K_{VCO}\,(1 + jw \bullet T2)}{w^2\, C1 \bullet N\,(1 + jw \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180°C \quad (5)$$

A plot of the magnitude and phase of G(s) H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

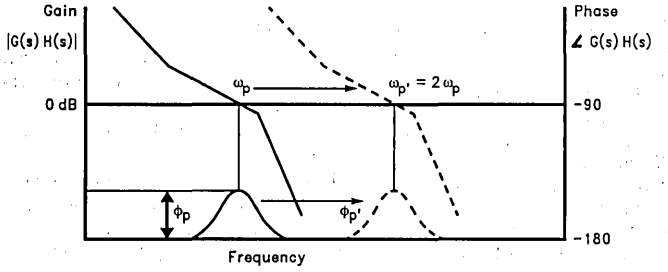
If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve *Figure 4* over to a different cutoff frequency, illustrated by dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "1/w" or "$1/w^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate with "w" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2 wp. K_{VCO}, $K\phi$, N, or the net product of these terms can be changed by a factor of 4, to counteract with w^2 term present in the denominator of

Application Information (Continued)

equation 3. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

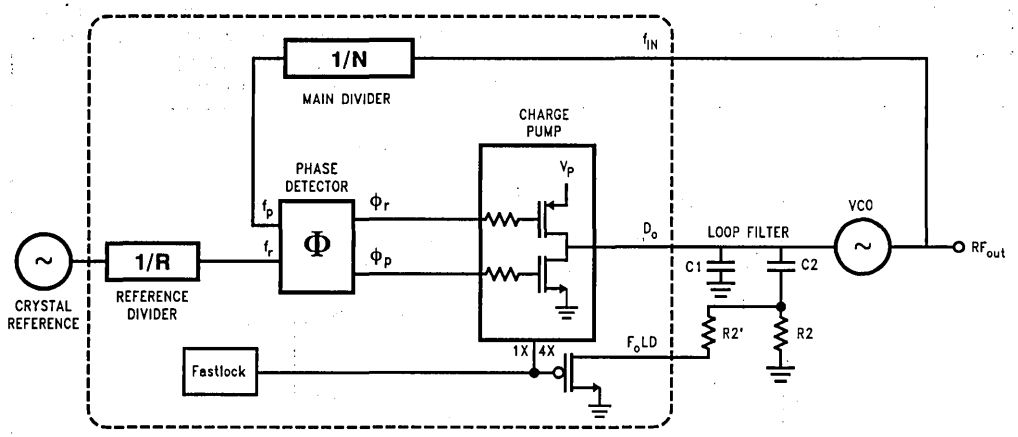
Fastlock Circuit Implementation

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX2335/36/37 PLL is shown in *Figure 5*. When a new frequency is loaded, and the RF1 I_{CPo} bit is set high, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF1 I_{CPo} bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.



TL/W/12332–15

FIGURE 4.Open Loop Response Bode Plot



TL/W/12332–18

FIGURE 5. Fastlock PLL Architecture

National Semiconductor

ADVANCE INFORMATION

LMX3160 Single Chip Radio Transceiver

General Description

The Single Chip Radio Transceiver is a monolithic, integrated radio transceiver optimized for use in the Digital European Cordless Telecommunications (DECT) system as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC V BiCMOS process (f_T = 18 GHz).

The Single Chip Radio Transceiver contains both transmit and receive functions. The transmitter includes a 1.1 GHz phase locked loop (PLL), a frequency doubler, and a high frequency buffer. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation. The circuit features an onboard voltage regulator to allow wide supply voltages. In addition, the on board voltage regulator has two outputs for regulated discrete stages in the Rx and Tx chain.

The IF amplifier, high gain limiting amplifier, and discriminator operate in the 40 to 150 MHz frequency range, and the total IF gain is 85 dB. The use of the limiter and the discriminator provides a low cost, high performance demodulator for communications systems. The RSSI output can be used for channel quality monitoring.

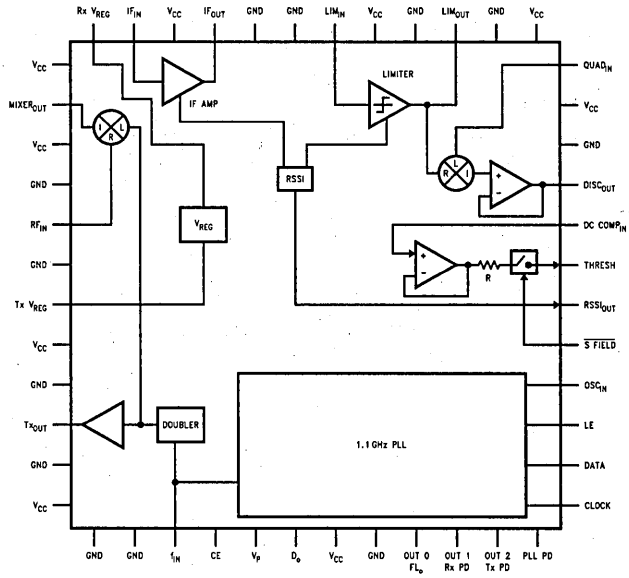
The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

Features

- Single chip solution for DECT RF transceiver
- RF sensitivity to −93 dBm; RSSI sensitivity to −100 dBm
- Two regulated voltage outputs for discrete amplifier V_{CC}
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage range
- Power down mode for increased current savings
- System noise figure 5.4 dB (typ)

Applications

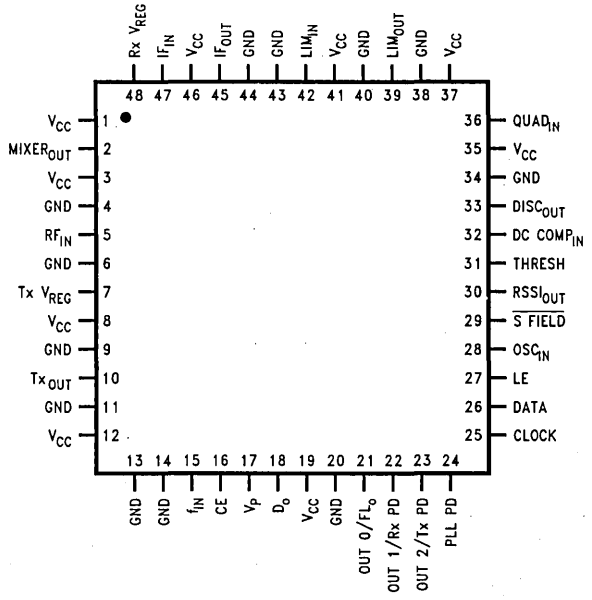
- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Other wireless communications systems



TL/W/12493–1

This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.

LMX3160 Pin Diagram



TL/W/12493–2

Pin No.	Pin Name	I/O	Description
1	V_{CC}	—	Power supply voltage input to mixer. Connect to VBAT
2	$MIXER_{OUT}$	O	IF output signal of the mixer.
3	V_{CC}	—	Power supply voltage input to mixer. Connect to VBAT
4	GND	—	Ground.
5	RF_{IN}	I	RF input to the mixer.
6	GND	—	Ground.
7	Tx V_{REG}	O	Supply voltage to external gain stage.
8	V_{CC}	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT
9	GND	—	Ground.
10	Tx_{OUT}	O	Doubler output.
11	GND	—	Ground.
12	V_{CC}	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT
13	GND	—	Ground.
14	GND	—	Ground.
15	f_{IN}	I	RF Input to doubler and PLL.
16	CE	I	Chip Enable. LOW powers down entire part. Before taking HIGH all μwire instructions should be loaded for R, N, F latches. Taking CE HIGH will power up the appropriate chip blocks depending on the state of bits F6, F7, F14, and F15. The CE state change will also load the PLL N and R counters to the correct divide ratios.

LMX3160 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
17	V_P	—	Power supply for charge pump.
18	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_{CC}	—	Power supply input for CMOS section of PLL. Connect to VBAT
20	GND		Ground.
21	Out 0/FL_o	I/O	Programmable CMOS output. Can be used for FastLock™ output (See Programmable Modes).
22	Out 1/Rx PD	I/O	Programmable CMOS output. Can be used for hardwire receiver power down (See Programmable Modes).
23	Out 2/Tx PD	I/O	Programmable CMOS output. Can be used for hardwire transmitter power down (See Programmable Modes).
24	PLL PD	I	PLL PD = LOW for PLL normal operations. PLL PD = HIGH for PLL power saving.
25	Clock	I	High impedance CMOS clock input.
26	Data	I	Binary serial data input. Data entered MSB first. High impedance CMOS input.
27	LE	I	Load enable input.
28	OSC_{IN}	I	Oscillator input.
29	$\overline{S\ Field}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled, and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator is held by the external capacitor.
30	$RSSI_{OUT}$	O	Voltage output of the received signal strength indicator (RSSI).
31	Thresh	O	Threshold level to external comparator.
32	DC $COMP_{IN}$	I	Input to DC compensation circuit.
33	$DISC_{OUT}$	O	Demodulated output of discriminator.
34	GND	—	Ground.
35	V_{CC}	—	Power supply input to discriminator circuit. Connect to VBAT
36	$QUAD_{IN}$	I	Quadrature input.
37	V_{CC}	—	Power supply input to limiter output stage. Connect to VBAT
38	GND	—	Ground.
39	LIM_{OUT}	O	Limiter output to the quadrature tank.
40	GND	—	Ground.
41	V_{CC}	—	Power supply input for limiter. Connect to VBAT
42	LIM_{IN}	I	IF input to the limiter.
43	GND	—	Ground.
44	GND	—	Ground.
45	IF_{OUT}	O	IF output to bandpass filter.
46	V_{CC}	—	Power supply input for IF amplifier. Connect to VBAT
47	IF_{IN}	I	IF input to IF amplifier.
48	Rx V_{REG}	—	Supply voltage to external LNA.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC})	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temp. (solder, 4 sec)(T_L)	+260°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 5.5V
Operating Temperature (T_A)	−10°C to +70°C

Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Rx I_{CC}	Receive Mode Current Consumption (Note 1)	Tx PLL Powered Down		38	45	mA
Tx I_{CC}	Transmit Mode Current Consumption (Note 2)	Rx PLL Powered Down		20	25	mA
I_{PD}	Power Down Current	Tx, Rx, PLL Off		1	10	μA
f_{RF}	RF Frequency Range		1.7		2.0	GHz
f_{max}	Maximum IF Input Frequency		120	150		MHz
f_{min}	Minimum IF Input Frequency			18	20	MHz
MIXER		f_{IN} = 1.9 GHz				
NF	Single Side Band Noise Figure			5.9	7	dB
GA	Gain		16	18		dB
OIP3	Output Intercept Point		−2	1		dBm
RF−RL	RF Return Loss	Z_o = 50Ω		15		dB
IF−RL	IF Return Loss	Z_o = 200Ω		15		dB
f_{IN}−RF	f_{IN} to RF Isolation			30		dB
f_{IN}−IF	f_{IN} to IF Isolation			30		dB
RF−IF	RF to IF Isolation			30		dB

Electrical Characteristics The following specifications are guaranteed over the recommended operating conditions unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AMPLIFIER		f_{IN} = 120 MHz				
NF	Noise Figure			6	8	dB
Av	Gain		20	25		dB
OIP3	Output Intercept Point		6	7		dBm
Z_{IN}	Input Impedance			200		Ω
Z_{OUT}	Output Impedance			200		Ω
IF LIMITER		f_{IN} = 120 MHz				
NF	IF Limiter Noise Figure			10	12	dB
Av	Limiter Gain		55	60		dB
Sens	Limiter/Disc. Sensitivity	BER = 10^{-3}		−65		dBm
IF_{IN}	IF Limiter Input Impedance			200		Ω
IF_{OUT}	IF Limiter Output Impedance			1000		Ω
V_{max}	Maximum Input Voltage Level		500			mV_{PP}
V_{OUT}	Output Swing			500		mV_{PP}
	Dynamic Range			60		dB
DISCRIMINATOR		f_{IN} = 120 MHz				
V_{OUT}	Discriminator Output Peak to Peak Voltage		250	400		mV
V_{OS}	Disc. Output DC Voltage		1.4		1.7	V
$DISC_{OUT}$	Disc. Output Impedance			150		Ω
RSSI		f_{IN} = 120 MHz				
RSSI	RSSI Dynamic Range		70	80		dB
$RSSI_{OUT}$	RSSI Output Voltage	Pin = −85 dBm	0.1	0.25	0.4	V
		Pin = 0 dBm	1.15	1.5	1.8	V
	RSSI Slope	Pin = −75 to −25 dBm	11	20		mV/dB
	RSSI Linearity			3		dB
FREQUENCY DOUBLER		f_{OUT} = 1.89 GHz				
f_{IN}	Input Frequency Range		885		950	MHz
V_{IN}	Input Signal Level	Z_{IN} = 200Ω	−14	−11.5	−9	dBm
Z_o	Output Impedance		45	60	80	Ω
	Fundamental Rejection (Note 3)	V_{IN} = 450 mV_{PP}		30		dB
	Harmonic Suppression (Note 3)	V_{IN} = 450 mV_{PP}		20		dB
P_{OUT}	Output Power		−10	−8		dBm

Electrical Characteristics The following specifications are guaranteed over the recommended operating conditions unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY SYNTHESIZER						
V_{OSC}	Oscillator Sensitivity		0.5	1.0		V_{PP}
$I_{Do\text{-}source}$	Charge Pump Output Current	$V_{do} = V_P/2$, I_{cpo} = LOW (Note 4)		−1.5		mA
$I_{Do\text{-}sink}$		$V_{do} = V_P/2$, I_{cpo} = LOW (Note 4)		1.5		mA
$I_{Do\text{-}source}$		$V_{do} = V_P/2$, I_{cpo} = HIGH (Note 4)		−6.0		mA
$I_{Do\text{-}sink}$		$V_{do} = V_P/2$, I_{cpo} = HIGH (Note 4)		6.0		mA
$I_{Do\text{-}Tri}$		$0.5 \le V_{do} \le V_P - 0.5$ T_A = 25°C	−1.0	0.1	1.0	nA
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA	V_{CC} −0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA			0.4	V
V_{IH}	High-Level Input Voltage		V_{CC} −0.8			V
V_{IL}	Low-Level Input Voltage				0.8	V
I_{IN}	Input Current	$GND < V_{IN} < V_{CC}$	−1.0		1.0	mA
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width	See Data Input Timing	50			ns
DC COMPENSATION SAMPLE AND HOLD CIRCUIT						
V_{OS}	Input Offset Voltage				3	mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V		1.0		V_{PP}
R_{SH}	Sample and Hold Resistor		224		336	Ω
D_V	Threshold Input Voltage Droop	C_{hold} = 2700 pF		1	10	mV/ms

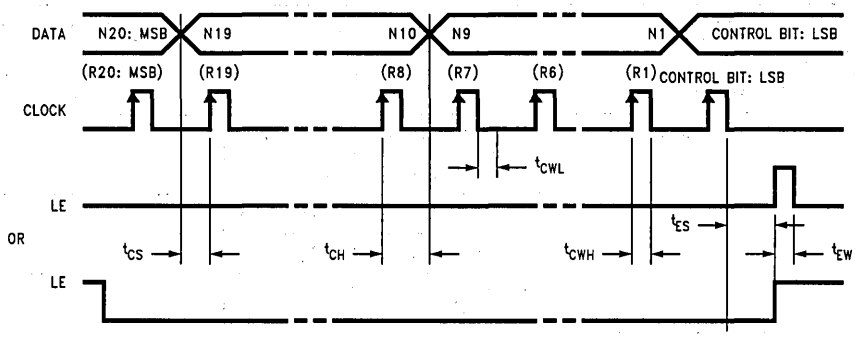
Note 1: This includes 5 mA current sourced from the Rx V_{REG} pin for the external receive LNA as shown in the application diagram.

Note 2: This includes 5 mA current sourced from the Tx V_{REG} pin for the external transmit buffer used before the power amplifier as shown in the application diagram.

Note 3: Measured at the output of external gain stage.

Note 4: See programmable modes for I_{cpo} description.

Serial Data Input Timing



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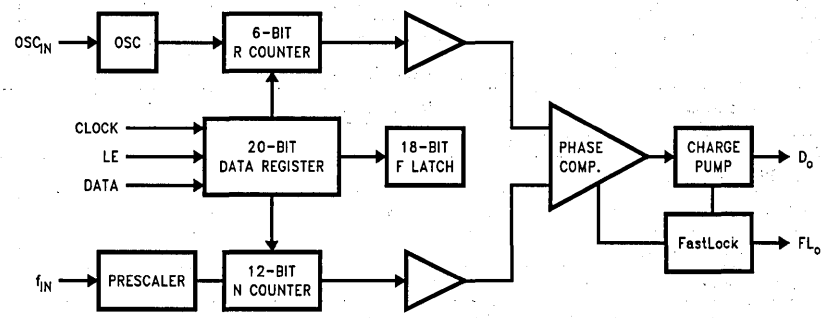
Notes: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC} = 3.0V and 2.6V @ V_{CC} = 5.5V.

PLL Functional Description

The simplified block diagram below shows the 20-bit data register, 18-bit F latch, 12 bit N counter, and 6 bit R counter.



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PLL Functional Description (Continued)

The data stream is clocked on the rising edge of LE into the DATA input, MSB first. The last two bits are the control bits. DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	N Counter
0	1	R Counter
1	X	F Latch

X = Dont Care

Programmable Divider (N Counters)

The N counter consists of the 6-bit swallow counter (A counter) and the 6-bit programmable counter (B counter). When the control bits are "00" data is transferred from the 20-bit shift register into two 6-bit latches. One latch sets the A counter while the other sets the B counter, MSB first. Serial data format is shown below.

LSB **MSB**

C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	X	X	X	X	X	X
Control Bits		Divide Ratio of Programmable Divider, N												Don't Care					

6-Bit Swallow Counter Divide Ratio (A Counter)

Divide Ratio A	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Notes: Divide ratio: 0 to 63

$B \geq A$

6-Bit Programmable Counter Divide Ratio (B Counter)

Divide Ratio B	N12	N11	N10	N9	N8	N7
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Notes: Divide ratio: 3 to 63

$B \geq A$

Programmable Reference Dividers (R Counters)

If the control bits are "01" data is transferred from the 20-bit shift register into a latch which sets the 6-bit R counter. Serial data format is shown below.

LSB **MSB**

C1	C2	R1	R2	R3	R4	R5	R6	X	X	X	X	X	X	X	X	X	X	X	X

Control Bits — Divide Ratio of Reference Divider — Don't Care

Divide Ratio R	R6	R5	R4	R3	R2	R1
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio: 3 to 63

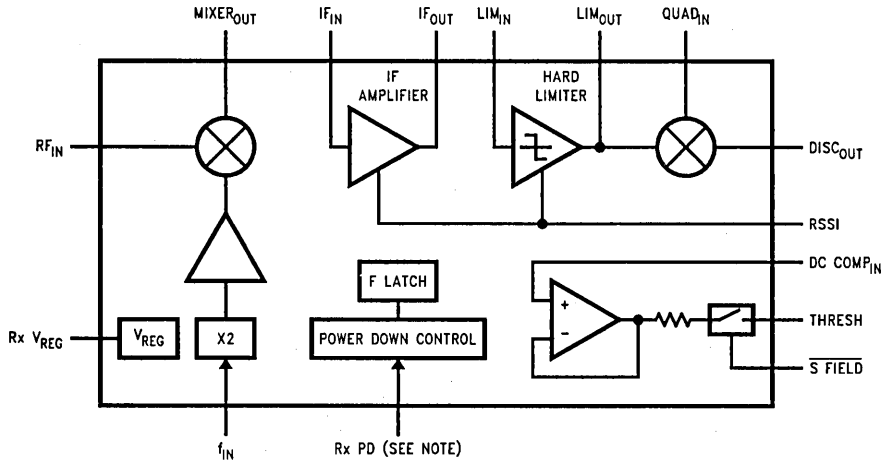
Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

- f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
- B: Preset divide ratio of binary 6-bit programmable counter (3 to 63)
- A: Preset divide ratio of binary 6-bit swallow counter ($0 \leq A \leq P$, $A \leq B$)
- f_{OSC}: Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 6-bit programmable reference counter (3 to 63)
- P: Preset modulus of dual modulus prescaler (32 or 64)

Receiver Functional Description

The simplified block diagram below shows the mixer, IF amplifier, limiter, and discriminator. In addition, the DC compensation circuit, doubler, and voltage regulator (for external LNA) are shown.



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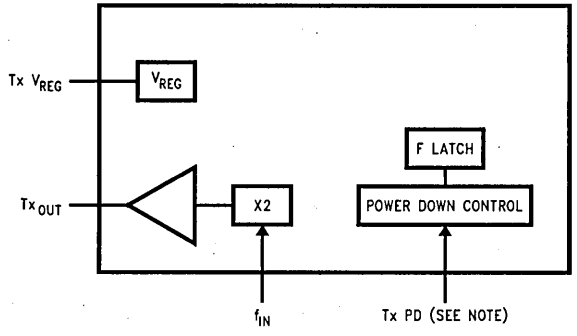
Note: Receiver power down can be controlled by software through the F Latch or hardwire through the Rx PD pin. This is determined by the state of F14 and F15 (See Programmable Modes).

Transmitter Functional Description

The simplified block diagram below shows the doubler and voltage regulator (for external transmit gain stage).



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Note: Transmitter power down can be controlled by software through the F Latch or hardwire through the Rx PD pin. This is determined by the state of F14 and F15 (See Programmable Modes).

Programmable Function Latch (F Latch)

If the control bits are "1X" data is transferred into the 20-bit shift register into the 18-bit F latch. Serial data format is shown below.

LSB **MSB**

C1	C2	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18
Control Bits																			

Programmable Modes

Several modes of operation can be programmed with the function register bits F1–F18, including the phase detector polarity, charge pump TRI-STATE® and CMOS outputs. In addition, software or hardwire power down modes may be selected with bits F14 and F15. The programmable modes are latched in when the control bits are: C1 = 1, C2 = X. Truth tables for the programmable modes are shown in Tables I–III.

TABLE I. Programmable Modes

F1	Prescaler Mod Select (32/64)
F2	Phase Detector Polarity
F3	Charge Pump Current
F4	Charge Pump TRI-STATE
F5	Don't Care
F6	Receive Section Power Down
F7	Transmit Section Power Down
F8	Out 0 CMOS Output/FastLock Output
F9	Out 1 CMOS Output/Receive Section Power Down Input
F10	Out 2 CMOS Output/Transmit Section Power Down Input
F11	Don't Care
F12	FastLock Auto/man select
F13	Out 0 Normal CMOS/FastLock Switch
F14	Mode Select. See Mode Select Table
F15	Mode Select. See Mode Select Table
F16	Auto FastLock Counter Bit #16
F17	Auto FastLock Counter Bit #32
F18	Auto FastLock Counter Bit #64

Functional Description

F1	Pre-scaler modules select. LOW selects 32/33 and HIGH selects 64/65.
F2	Phase Detector Polarity. F2 is used to reverse the polarity of the phase detector. Depending upon V_{CO} characteristics, F2 should be set accordingly: When VCO characteristics are positive, F2 should be set HIGH; When VCO characteristics are negative, F2 should be set LOW.
F3	Charge pump current. LOW selects low charge pump current (1X I_{cpo}). High selects HIGH charge pump current (4X I_{cpo}).
F4	Charge Pump TRI-STATE.
F5	Don't Care.
F6–F7	Power down. When F14 = 0 and F15 = 0, F6 controls the state of the receive section and F7 controls the state of the transmit section. A LOW powers up the section while a HIGH powers down the section.
F8–F10	CMOS Outputs. When F13 is LOW, F8 controls sets state of Out 0 (pin 21). When in normal power down mode (F14 = 0, F15 = 0), F9 and F10 sets the state of Out 1 (pin 22) and Out 2 (pin 23) respectively.
F11	Don't Care.
F12	FastLock Auto/Manual Mode Select. When F13 HIGH, selects auto or manual FastLock mode.
F13	Out 0 (pin 21) Normal/FastLock select. When LOW the state of Out 0 (pin 21) is controlled by F8. When HIGH Out 0 is used for FastLock.
F14–F15	Power Down Mode Control. See Table III.
F16–F18	FastLock Timeout Counter. See Table IV for counter values.

Table II. Mode Select Truth Table

	F1 Pre-scaler Mod.	F2 Phase Det. polarity	F3 I_{cpo}	F4 D_o TRI-STATE	F6–F7 Power Down Modes	F8–F10 CMOS Outputs
0	32/33	Negative	LOW	Normal Operation	Powered UP	LOW
1	64/65	Positive	HIGH	TRI-STATE	Powered Down	HIGH

TABLE IIIa. Power Down Modes

Function	F15	F14
Software Control	0	0
Test Mode (See Note)	0	1
Test Mode (See Note)	1	0
Hardwire Power Down	1	1

Note: Not used in application.

TABLE IIIb. Power Control Modes

		High	Low
Software Control	F6	Receiver Off	Receiver On
	F7	Transmitter Off	Transmitter On
Hardwire Control	Rx PD	Receiver Off	Reciever On
	Tx PD	Transmitter Off	Transmitter On
	PLDD PD	PLL Off	PLL On

TABLE IV. Charge Pump Output, Out 0, and FastLock Decoding

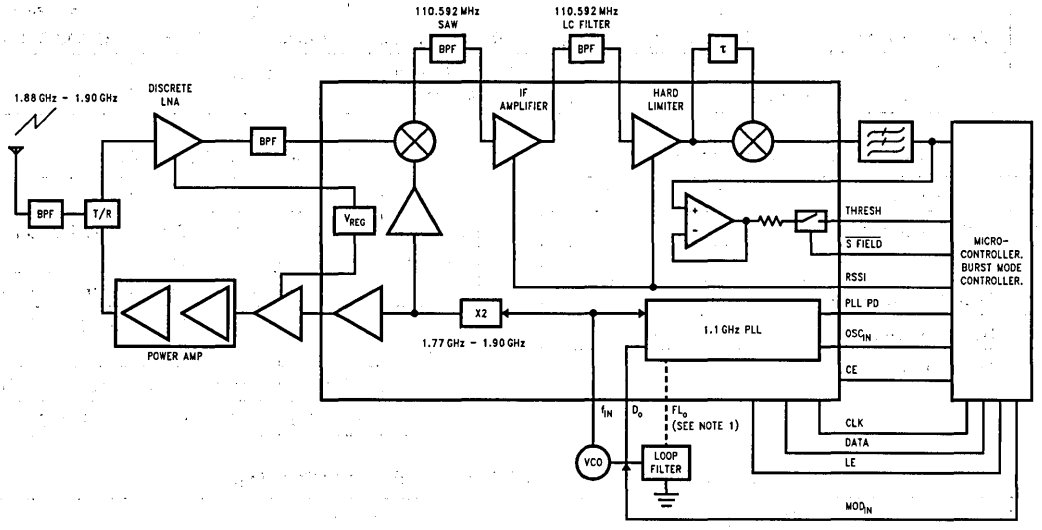
F3	F12	F13	Function
0	X	0	I_{cpo} = 1X, No FastLock, Out 0 = F8
1	X	0	I_{cpo} = 4X, No FastLock, Out 0 = F8
0	0	1	I_{cpo} = 1X, Manual FastLock, Out 0 = FL_o
1	0	1	I_{cpo} = 4X, Manual FastLock, Out 0 = FL_o
X	1	1	I_{cpo} = Set by # reference cycles present in F counter, Auto FastLock, Out 0 = FL_o

TABLE V. FastLock Timeout Counter Value Programming

Time Out (# Reference Cycles)	8	24	40	56	72	88	104	120
F16	0	1	0	1	0	1	0	1
F17	0	0	1	1	0	0	1	1
F18	0	0	0	0	1	1	1	1

Example: To set FastLock timeout for 24 reference cycles, set F16 = HIGH, F17 = LOW, and F18 = LOW.

Typical Application Block Diagram



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Note 1: Connected when using FastLock.

System: DECT—System +3V Only

		Data Per Stage			Cumulative Data				
#	Component	Gain	N Fig	OIP3	#	Gain	N Fig	IIP3	OIP3
1	Filter/Switch	−2.0	2.0	100.0	1	−2.0	2.0	97.9	95.9
2	Discrete LNA	10.0	2.0	7.0	2	8.0	4.0	−1.0	7.0
3	Filter	−2.0	2.0	100.0	3	6.0	4.2	−1.0	5.0
4	Mixer	18.0	5.9	1.0	4	24.0	5.2	−23.0	1.0
5	SAW	−11.0	11.0	100.0	5	13.0	5.3	−23.0	−10.0
6	IF Amplifier	25.0	4.0	57.0	6	38.0	5.4	−23.0	15.0
7	BPF (LC)	−2.0	2.0	100.0	7	36.0	5.4	−23.0	13.0
8	IF Limiter	60.0	18.0	68.0	8	96.0	5.4	−29.2	66.8

SYSTEM CUMULATIVE VALUES

			Gain	96.0 dB		
			N Fig	5.4 dB		
Sensitivity (@ 25°C)	−93.1 dBm		IIP3	−23.0 dBm		
Required Eb/No	14.0 dB		OIP3	66.8 dbm		

Note: Assumes 50 dB attenuation of interferer by the SAW filter and 8 dB attenuation by the LC filter.

Application Information

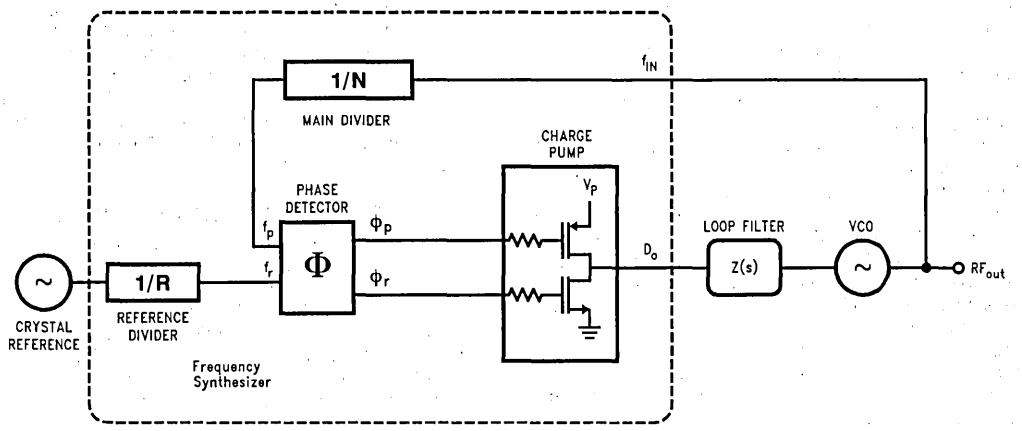

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FIGURE 1. Conventional PLL Architecture

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (K_ϕ), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation 2*.

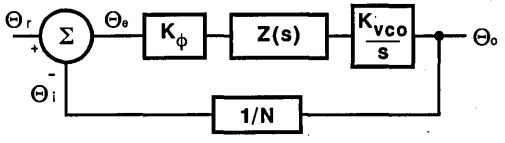

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FIGURE 2. PLL Linear Model

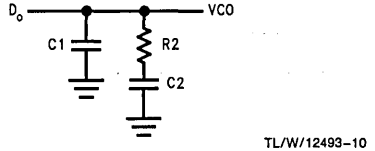

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FIGURE 3.

PASSIVE LOOP FILTER

Open loop gain = H(s) G(s) = $\Theta i/\Theta e = K_\phi Z(s) K_{VCO}/Ns$ (1)

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$G(S) \bullet H(S)\Big|_{S = j\bullet\omega} \frac{-K_\phi \bullet K_{VCO}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From *Equation 3* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation 5*.

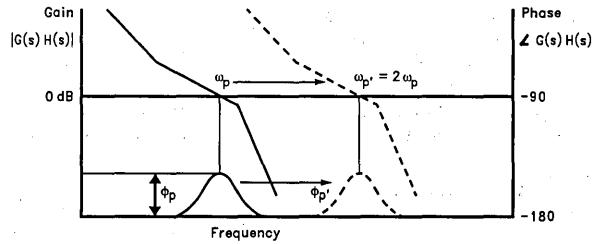
$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45°.

If we were now to redefine the cut off frequency, ω_p', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed FastLock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "$1/\omega$" or "$1/\omega^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "ω" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at $\omega_p' = 2\ \omega_p$. K_{VCO}, K_ϕ, N, or the net product of these terms can be changed by a factor of 4 to counteract the ω^2 term present in the denominator of *Equation 3*. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1.5 mA in the standard mode to 6 mA in FastLock.

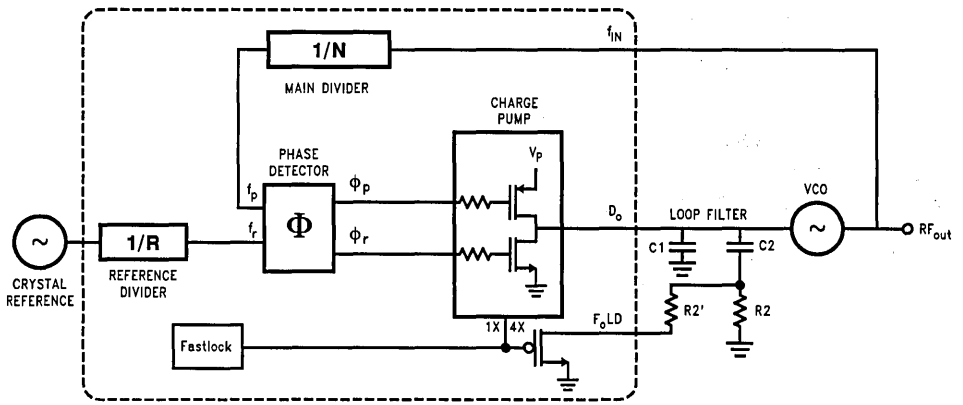
FastLock Circuit Implementation

A diagram of the FastLock scheme as implemented in National Semiconductors LMX3160 is shown in *Figure 5*. When a new frequency is loaded, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the PLL will then return to standard, low noise operation. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between FastLock and standard mode.



TL/W/12493–11

Figure 4. Open Loop Response Bode Plot



TL/W/12493–12

FIGURE 5. FastLock PLL Architecture

National Semiconductor

LMX2216
0.1 GHz to 2.0 GHz Low Noise Amplifier/Mixer for RF Personal Communications

General Description

The LMX2216 is a monolithic, integrated low noise amplifier (LNA) and mixer suitable as a first stage amplifier and down-converter for RF receiver applications. The wideband operating capabilities of the LMX2216 allow it to function over frequencies from 0.1 GHz to 2.0 GHz. It is fabricated using National Semiconductor's ABiC IV BiCMOS process.

All input and output ports of the LMX2216 are single-ended. The LNA input and output ports are designed to interface to a 50Ω system. The Mixer input ports are matched to 50Ω. The output port is matched to 200Ω. The only external components required are DC blocking capacitors. The balanced architecture of the LMX2216 maintains consistent operating parameters from unit to unit, since it is implemented in a monolithic device. This consistency provides manufacturers a significant advantage since tuning procedures—often needed with discrete designs—can be reduced or eliminated.

The low noise amplifier produces very flat gain over the entire operating range. The doubly-balanced, Gilbert-cell mixer provides good LO-RF isolation and cancellation of second-order distortion products. A power down feature is implemented on the LMX2216 that is especially useful for standby operation common in Time Division Multiple Access (TDMA) and Time Division Duplex (TDD) systems.

The LMX2216 is available in a narrow-body 16-pin surface mount plastic package.

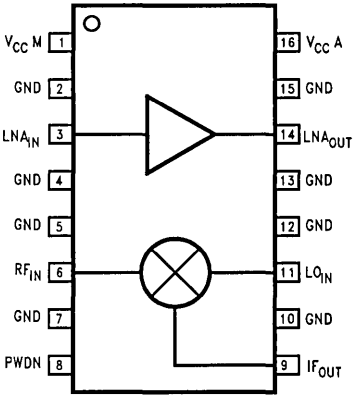
Features

- Wideband RF operation from 0.1 GHz to 2.0 GHz
- No external biasing components necessary
- 3V operation
- LNA input and output ports matched to 50Ω
- Mixer input ports matched to 50Ω, output port matched to 200Ω.
- Doubly balanced Gilbert cell mixer (single ended input and output)
- Low power consumption
- Power down feature
- Small outline, plastic surface mount package

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Digital cellular telephone systems
- Other wireless communications systems

Functional Block/Pin Diagram



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Order Number LMX2216M
See NS Package Number M16A

Pin Description

Pin No.	Pin Name	I/O	Description
1	V_{CC} M	I	Voltage supply for the mixer. The input voltage level to this pin should be a DC Voltage ranging from 2.85V to 3.15V.
2	GND		Ground
3	LNA_{IN}	I	RF input signal to the LNA. External DC blocking capacitor is required.
4	GND		Ground
5	GND		Ground
6	RF_{IN}	I	RF input to the mixer. The RF signal to be down converted is connected to this pin. External DC blocking capacitor is required.
7	GND		Ground
8	PWDN	I	Power down signal pin. Both the LNA and mixer are powered down when a HIGH level is applied to this pin (V_{IH}).
9	IF_{OUT}	O	IF output signal of the mixer. External DC blocking capacitor is required.
10	GND		Ground
11	LO_{IN}	I	Local oscillator input signal to the mixer. External DC blocking capacitor is required.
12	GND		Ground
13	GND		Ground
14	LNA_{OUT}	O	Output of the LNA. This pin outputs the amplified RF signal. External DC blocking capacitor is required.
15	GND		Ground
16	V_{CC} A	I	LNA supply Voltage. DC Voltage ranging from 2.85V to 3.15V.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Storage Temperature (T_S)	−65°C to +150°C
Operating Temperature (T_O)	−40°C to +85°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.85V–3.15V
Operating Temperature (T_A)	−10°C to +70°C
RF_{IN}	0.1 GHz to 2.0 GHz
LO_{IN}	0.1 GHz to 2.0 GHz

Electrical Characteristics: LNA

(V_{CC} = +3.0V ±5%, T_A = 25°C, Z_o = 50Ω and f_{IN} = 2.0 GHz @ −30 dBm unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	In Operation		6.5	8.0	mA
$I_{CC-PWDN}$	Supply Current	In Power Down Mode			10	μA
G	Gain		9	10		dB
P_{1dB}	Output 1 dB Compression Point		−5.0	−3.0		dBm
OIP3	Output 3rd Order Intercept Point		5.0	7.0		dBm
NF	Single Side Band Noise Figure			4.8	6.0	dB
RL_{IN}	Input Return Loss		10	15		dB
RL_{OUT}	Output Return Loss		10	11		dB

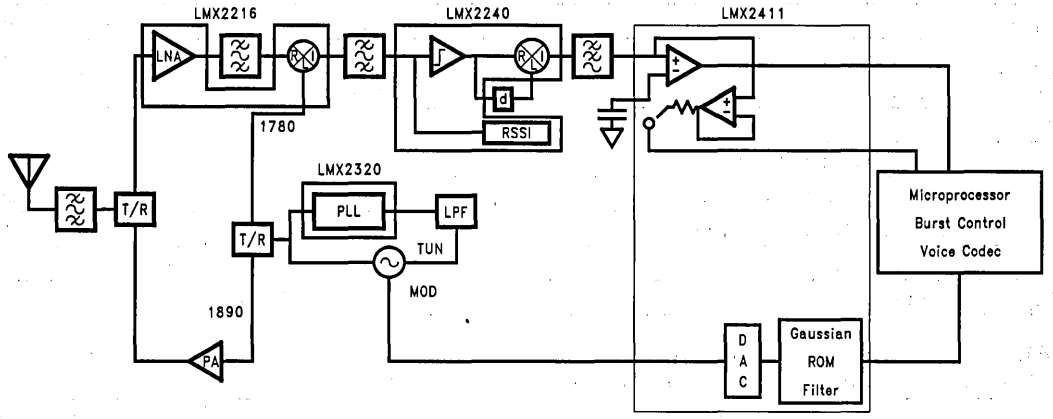
Electrical Characteristics: Mixer (V_{CC} = +3.0V ±5%, T_A = 25°C, Z_o = 50Ω, f_{RF} = 2.0 GHz @ −30 dBm, f_{LO} = 1.89 GHz @ 0 dBm; f_{IF} = 110 MHz unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	In Operation		9.0	12.0	mA
$I_{CC-PWDN}$	Supply Current	In Power Down Mode			10	μA
G_C	Conversion Gain (Single Side Band)		4.0	6.0		dB
P_{1dB}	Output 1 dB Compression Point		−13.0	−9.0		dBm
OIP3	Output Third Order Intercept Point		−3.0	0.0		dBm
SSB NF	Single Side Band Noise Figure			17	18	dB
DSB NF	Double Side Band Noise Figure			14	15	dB
LO-RF	LO to RF Isolation		20	30		dB
LO-IF	LO to IF Isolation		20	30		dB
RF RL	RF Return Loss		10	15		dB
LO RL	LO Return Loss		10	15		dB
IF RL	IF Return Loss			15		dB
Z_{IF}	IF Port Impedance			200		Ω

Electrical Characteristics: Power Down

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		V_{CC} − 0.8			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	−10.0		10.0	μA
I_{IL}	Low Level Input Current	V_{IL} = GND	−10.0		10.0	μA

Typical Application Block Diagram



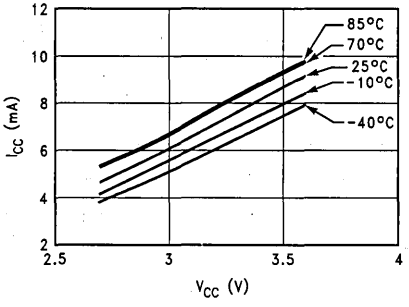
TL/W/11814-2

FIGURE 2

Typical Characteristics

LNA

LNA Current Composition vs Supply Voltage with Temperature as a Parameter



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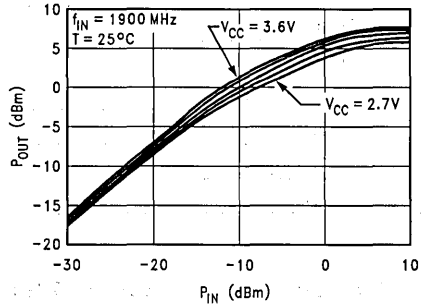
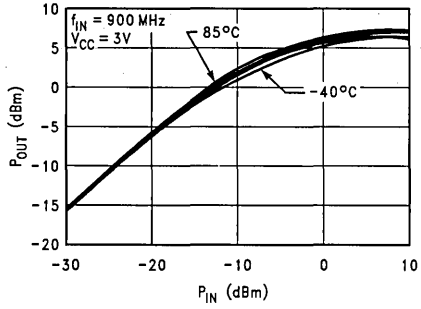
LNA P_{OUT} vs P_{IN} with Supply Voltage as a Parameter



TL/W/11814-4

LNA P_{OUT} vs P_{IN} with Temperature as a Parameter



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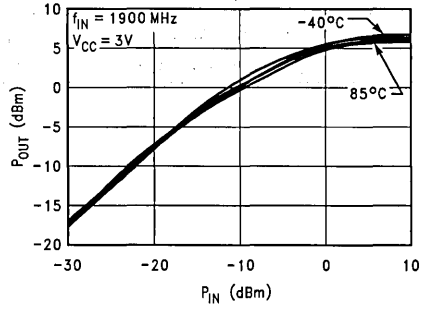
LNA P_{OUT} vs P_{IN} with Temperature as a Parameter



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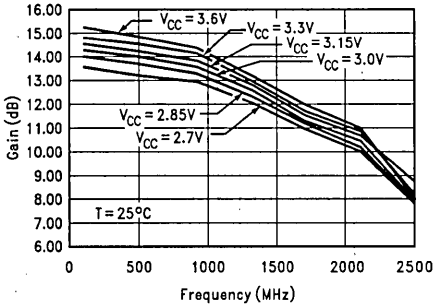
Typical Characteristics (Continued)

LNA (Continued)

LNA Gain vs Frequency with Supply Voltage as a Parameter



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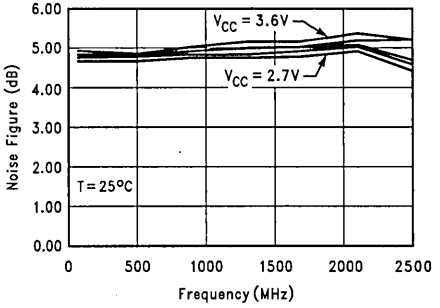
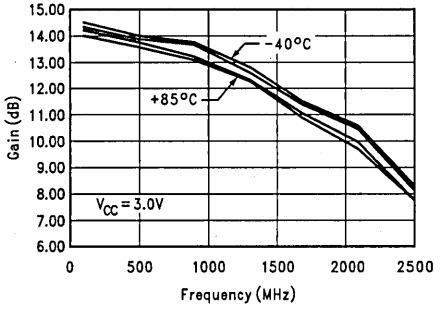
LNA Noise Figure vs Frequency with Supply Voltage as a Parameter



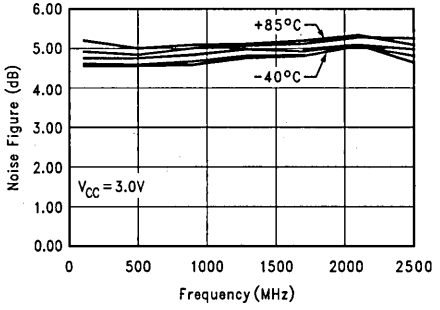
TL/W/11814–9

LNA Gain vs Frequency with Temperature as a Parameter



TL/W/11814–10

LNA Noise Figure vs Frequency with Temperature as a Parameter



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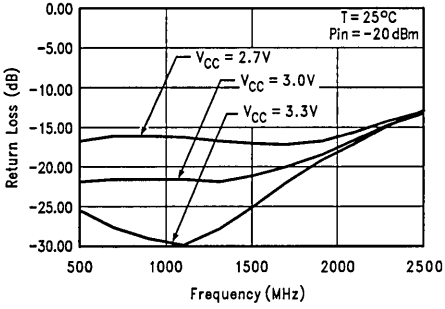
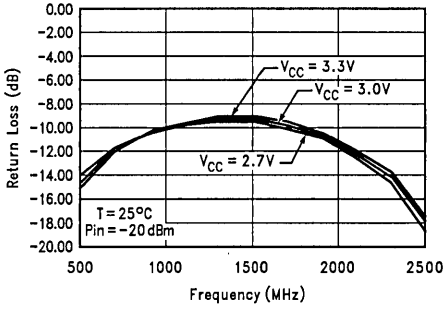
LNA Input Return Loss vs Frequency with Voltage as a Parameter



TL/W/11814–12

LNA Output Return Loss vs Frequency with Voltage as a Parameter

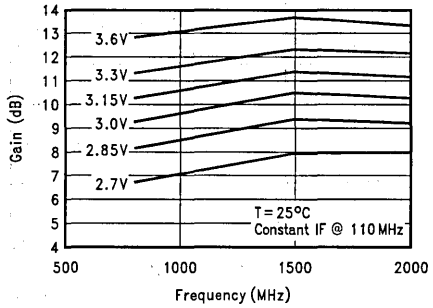


TL/W/11814–19

Typical Characteristics (Continued)

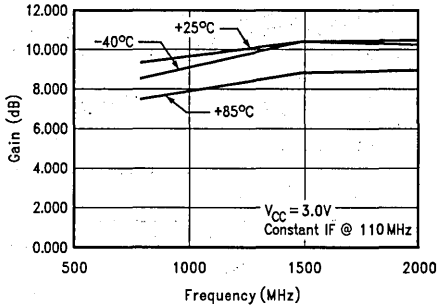
MIXER

Mixer Gain (Double Sideband) vs Frequency with Supply Voltage as a Parameter



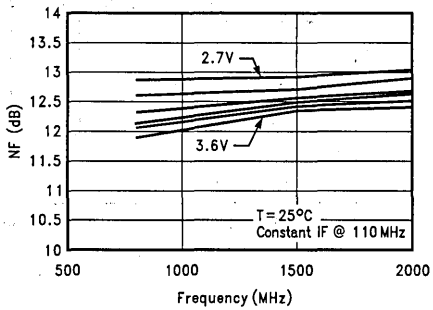
TL/W/11814–20

Mixer Gain (Double Sideband) vs Frequency with Temperature as a Parameter



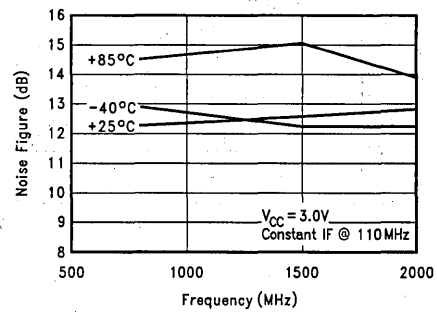
TL/W/11814–21

Mixer Noise Figure (Double Sideband) vs Frequency with Supply Voltage as a Parameter



TL/W/11814–22

Mixer Noise Figure (Double Sideband) vs Frequency with Temperature as a Parameter

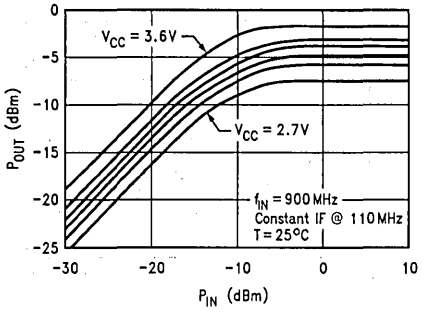


TL/W/11814–23

Typical Characteristics (Continued)

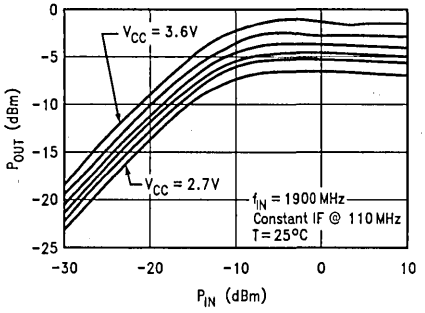
MIXER (Continued)

Mixer P_{OUT} vs P_{IN} with Supply Voltage as a Parameter



TL/W/11814-24

Mixer P_{OUT} vs P_{IN} with Supply Voltage as a Parameter



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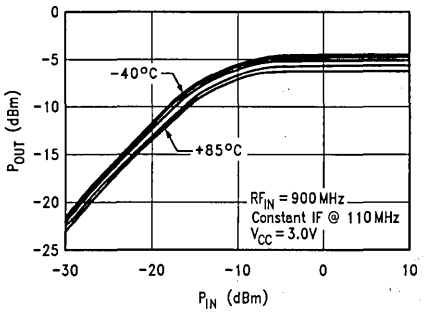
Mixer P_{OUT} vs P_{IN} with Temperature as a Parameter



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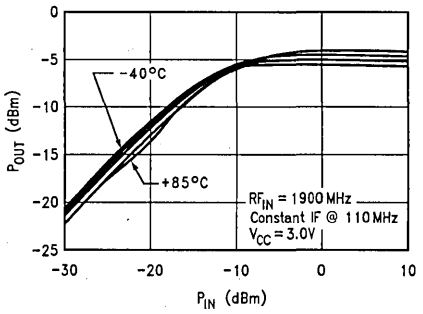
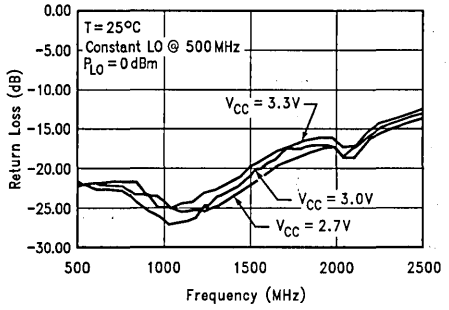
Mixer P_{OUT} vs P_{IN} with Temperature as a Parameter



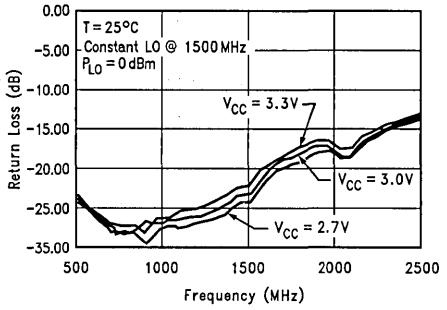
TL/W/11814-27

Mixer RF_{IN} Return Loss vs Frequency with Supply Voltage as a Parameter



TL/W/11814-28

Mixer RF_{IN} Return Loss vs Frequency with Supply Voltage as a Parameter



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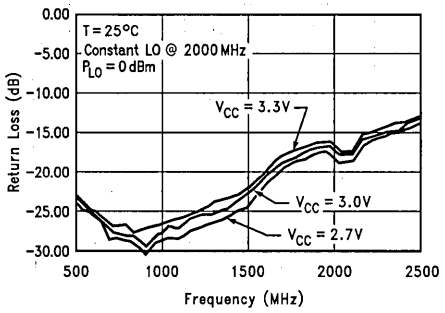
Typical Characteristics (Continued)

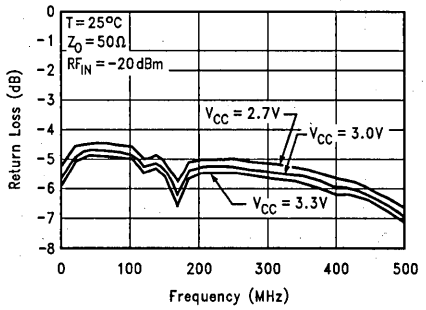
MIXER (Continued)

Mixer RF_{IN} Return Loss vs Frequency with Supply Voltage as a Parameter



TL/W/11814–30

Mixer IF_{OUT} Return Loss vs Frequency with Supply Voltage as a Parameter



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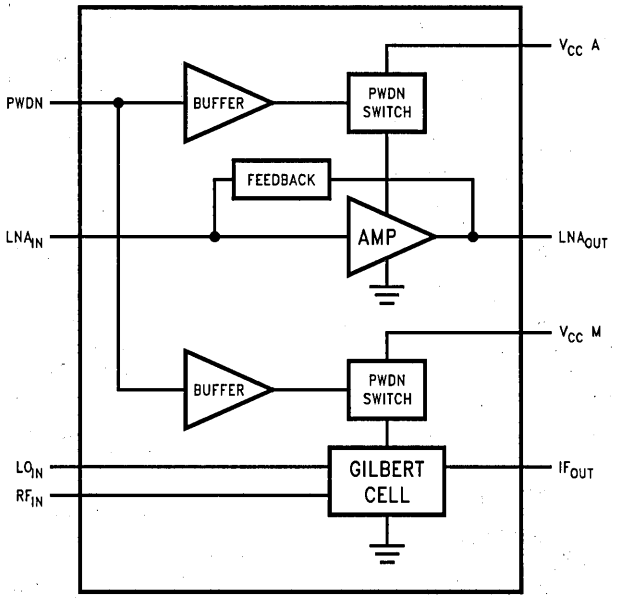
Functional Description



TL/W/11814–13

FIGURE 3. Block Diagram of the LMX2216

Functional Description (Continued)

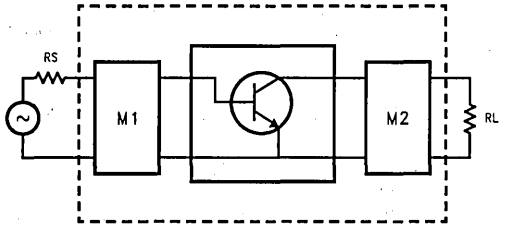
THE LNA

The LNA is a common emitter stage with active feedback. This feedback network allows for wide bandwidth operation while providing the necessary optimal input impedance for low noise performance. The power down feature is implemented using a CMOS buffer and a power-down switch. The power down switch is implemented with CMOS devices. During power down, the switch is open and only leakage currents are drawn from the supply.

THE MIXER

The mixer is a Gilbert cell architecture, with the RF input signal modulating the LO signal and single ended output taken from the collector of one of the upper four transistors. The power down circuitry of the mixer is similar to that of the LNA. The power down switch is used to provide or cut off bias to the Gilbert cell.

Typical Low Noise Amplifier



TL/W/11814–14

FIGURE 4. Typical LNA Structure

A typical low noise amplifier consists of an active amplifying element and input and output matching networks. The input matching network is usually optimized for noise performance, and the output matching network for gain. The active element is chosen such that it has the lowest optimal noise figure, F_{MIN}, an intrinsic property of the device. The noise figure of a linear two-port is a function of the source admittance and can be expressed by

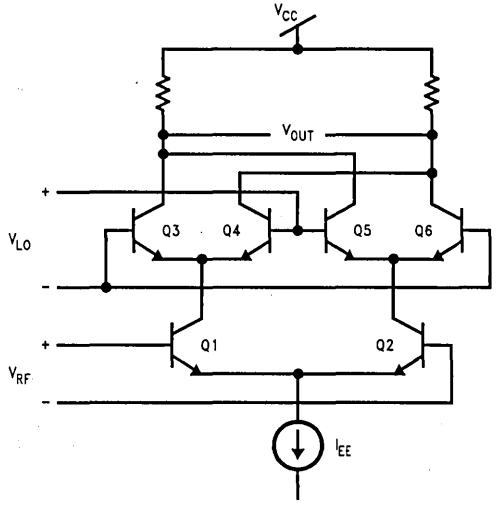
$$F = F_{MIN} + \frac{R_n}{G_G}[(G_{ON} - G_G)^2 + (B_{ON} - B_G)^2]$$

where $G_G + jB_G$ = generator admittance presented to the input of the two port,

$G_{ON} + jB_{ON}$ = generator admittance at which optimum noise figure occurs,

R_n = empirical constant relating the sensitivity of the noise figure to generator admittance.

Typical Gilbert Cell



TL/W/11814–15

FIGURE 5. Typical Gilbert Cell Circuit Diagram

The Gilbert cell shown above is a circuit which multiplies two input signals, RF and LO. The input RF voltage differentially modulates the currents on the collectors of the transistors Q1 and Q2, which in turn modulate the LO voltage by varying the bias currents of the transistors Q3, Q4, Q5, and Q6. Assuming that the two signals are small, the result is a product of the two signals, producing at the output a sum and difference of the frequencies of the two input signals. If either of these two signals are much larger than the threshold voltage V_T, the output will contain other mixing products and higher order terms which are undesirable and may need to be attenuated or filtered out.

Analysis of the Gilbert cell shows that the output, which is the difference of the collector currents of Q3 and Q6, is related to the two inputs by the equation:

$$\Delta I = I_{C3} - I_{C6} = I_{EE}\left[\tanh\left(\frac{V_{RF}}{2V_T}\right)\right]\left[\tanh\left(\frac{V_{LO}}{2V_T}\right)\right]$$

and the hyperbolic tangent function can be expressed as a Taylor series

$$\tanh(x) = x - \frac{x^3}{3} + \frac{x^5}{5} - \ldots$$

Assuming that the RF and LO signals are sinusoids.

$$V_{RF} = A\cos(\omega_{RF}t + \phi_{RF})$$
$$V_{LO} = B\cos(\omega_{LO}t + \phi_{LO})$$

then

$$\Delta I = I_{EE}\left[A\cos(\omega_{RF}t + \phi_{RF}) - \frac{A^3}{3}\cos^3(\omega_{RF}t + \phi_{RF}) + \ldots\right]$$
$$\bullet\left[B\cos(\omega_{LO}t + \phi_{LO}) - \frac{B^3}{3}\cos^3(\omega_{LO}t + \phi_{LO}) + \ldots\right]$$

The lowest order term is a product of two sinusoids, yielding a sum of two sinusoids,

$$I_{EE}\frac{AB}{2}\left[\cos((\omega_{RF} + \omega_{LO})t + \phi_{RF} + \phi_{LO}) + \cos((\omega_{RF} - \omega_{LO})t + \phi_{RF} - \phi_{LO})\right]$$

one of which is the desired intermediate frequency signal.

Figures of Merit

GAIN (G)

Many different types of gain are specified in RF engineering. The type referred to here is called transducer gain and is defined as the ratio of the power delivered to the load to the available power from the source,

$$G = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}^2/R_L}{V_{IN}^2/R_S} = 4\,\frac{R_S\,V_{OUT}^2}{R_L\,V_{IN}^2}$$

where V_{OUT} is the voltage across the load R_L and V_{IN} is the generator voltage with internal resistance R_S. In terms of scattering parameters, transducer gain is defined as

$$G = 20 \log (|S_{21}|)$$

where S_{21} is the forward transmission parameter, which can be measured using a network analyzer.

1 dB COMPRESSION POINT (P_{1dB})

A measure of amplitude linearity, 1 dB compression point is the point at which the actual gain is 1dB below the ideal linear gain. For a memoryless two-port with weak nonlinearity, the output can be represented by a power series of the input as

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \ldots$$

For a sinusoidal input,

$$v_i = A \cos \omega_1 t$$

the output is

$$v_o = \frac{1}{2} k_2 A^2 + \left(k_1 A + \frac{3}{4} k_3 A^3\right) \cos \omega_1 t + \frac{1}{2} k_2 A^2 \cos 2\omega_1 t + \frac{1}{4} k_3 A^3 \cos 3\omega_1 t$$

assuming that all of the fourth and higher order terms are negligible. For an amplifier, the fundamental component is the desired output, and it can be rewritten as

$$k_1 A \left[1 + \frac{3}{4} (k_3/k_1) A^2\right].$$

This fundamental component is larger than $k_1 A$ (the ideally linear gain) if $k_3 > 0$ and smaller if $k_3 < 0$. For most practical devices, $k_3 < 0$, and the gain compresses as the amplitude A of the input signal gets larger. The 1 dB compression point can be expressed in terms of either the input power or the output power. Measurement of P_{1dB} can be made by increasing the input power while observing the output power until the gain is compressed by 1 dB.

THIRD ORDER INTERCEPT (OIP_3)

Third order intercept is another figure of merit used to characterize the linearity of a two-port. It is defined as the point at which the third order intermodulation product equals the ideal linear, uncompressed, output. Unlike the P_{1dB}, OIP_3 involves two input signals. However, it can be shown mathematically (similar derivation as above) that the two are closely related and $OIP_3 \approx P_{1dB} + 10$ dB. Theses two figures of merit are illustrated in *Figure 6*.

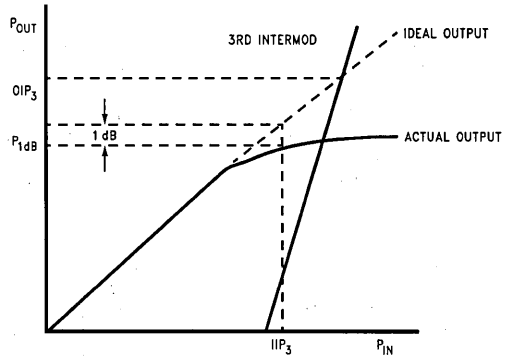


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FIGURE 6. Typical P_{OUT}–P_{IN} Characteristics

NOISE FIGURE (NF)

Noise figure is defined as the input signal to noise ratio divided by the output signal to noise ratio. For an amplifier, it can also be interpreted as the amount of noise introduced by the amplifier itself seen at the output. Mathematically,

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{G_a\,S_i/(N_a + G_a\,N_i)} = \frac{N_a + G_a\,N_i}{G_a\,N_i}$$

$$NF = 10 \log (F)$$

where S_i and N_i represent the signal and noise power levels available at the input to the amplifier, S_o and N_o the signal and noise power levels available at the output, G_a the available gain, and Na the noise added by the amplifier. Noise figure is an important figure of merit used to characterize the performance of not only a single component but also the entire system. It is one of the factors which determine the system sensitivity.

IMAGE FREQUENCY, DSB/SSB NF

Image frequency refers to that frequency which is also down-converted by the mixer, along with the desired RF component, to the intermediate frequency. This image frequency is located at the same distance away from the LO, but on the opposite side of the RF. For most mixers, it must be filtered out before the signal is down-converted; otherwise, an image-reject mixer must be used. *Figure 7* illustrates the concept.

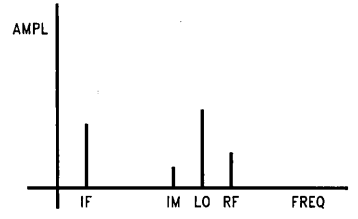

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FIGURE 7. Input and Output Spectrum of Mixers

Figures of Merit (Continued)

Due to the presence of image frequencies and the method in which noise figure is defined, noise figures can be measured and specified in two ways: double side band (DSB) or single side band (SSB). In DSB measurements, the image frequency component of the input noise source is not filtered and contributes to the total output noise at the intermediate frequency. In SSB measurements. the image frequency is filtered and the output noise is not caused by this frequency component. In most mixer applications where only one side band is wanted, SSB noise figure is 3 dB *higher* than DSB noise figure.

In this application, the LMX2216 is used in a radio receiver front end, where it amplifies the signal from the antenna and then down converts it to an intermediate frequency. The image filter placed between the LNA and the mixer attenuates the image frequency. The mixer is shown to use an LO signal generated by a PLL synthesizer, but, depending on the type of application, the LO signal could be generated by a device as simple as a free-running oscillator. The IF output is then typically filtered by a channel-select filter following the mixer, and this signal can then be demodulated or go through another down conversion, depending upon the intermediate frequency and system requirements. This external filter rejects adjacent channels and also attenuates any LO feed through. Figure 9 shows a cascade analysis of a typical RF front-end subsystem in which the LMX2216 is used. It includes the bandpass filter and the switch through which the input RF signal goes in a radio system before reaching the LNA. Typical values are used for the insertion loss of the various filters in this example.

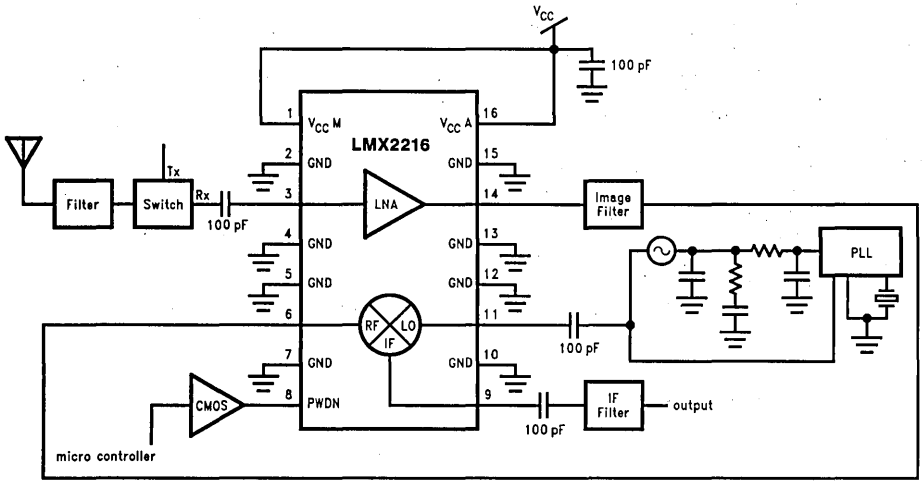

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FIGURE 8. Typical Applications Circuit of the LMX2216

		Data per Stage				Cumulative Data			
#	Comp	Gain	N Fig	OIP3	#	Gain	N Fig	IIP3	OIP3
1	Filter	−2.0	2.0	100.0	1	−2.0	2.0	97.9	95.9
2	Switch	−0.6	0.6	100.0	2	−2.6	2.6	96.6	94.0
3	LNA	12.3	3.7	6.0	3	9.7	6.3	−3.7	6.0
4	Filter	−3.0	3.0	100.0	4	6.7	6.4	−3.7	3.0
5	Mixer	5.8	13.7	3.0	5	12.5	9.6	−10.5	2.0
6	Filter	−3.0	3.0	100.0	6	9.5	9.7	−10.5	−1.0

System Cumulative Values		
	Gain	9.5 dB
	N Fig	9.7 dB
	IIP_3	−10.5 dBm
	OIP_3	−1.0 dBm

FIGURE 9. Cascade Analysis Example

National Semiconductor

LMX2240
Intermediate Frequency Receiver

General Description

The LMX2240 is a monolithic, integrated intermediate frequency receiver suitable for use in Digital European Cordless Telecommunications (DECT) systems as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC™ IV BiCMOS process (f_T = 15 GHz).

The LMX2240 consists of a high gain limiting amplifier, a frequency discriminator, and a received signal strength indicator (RSSI). The high gain limiting amplifier and discriminator operate in the 40 MHz to 150 MHz frequency range, and the limiter has approximately 70 dB of gain. The use of the limiter and the discriminator provides a low cost, high performance demodulator for communications systems. The RSSI output can be used for channel quality monitoring.

The LMX2240 is intended to support single conversion receivers. This device saves power, size, and cost by eliminating the second local oscillator (LO), second converter (mixer), and additional filters. The LMX2240 is recommended for systems with channel bandwidths of 300 kHz to 2.5 MHz.

The LMX2240 is available in a 16-pin JEDEC surface mount plastic package.

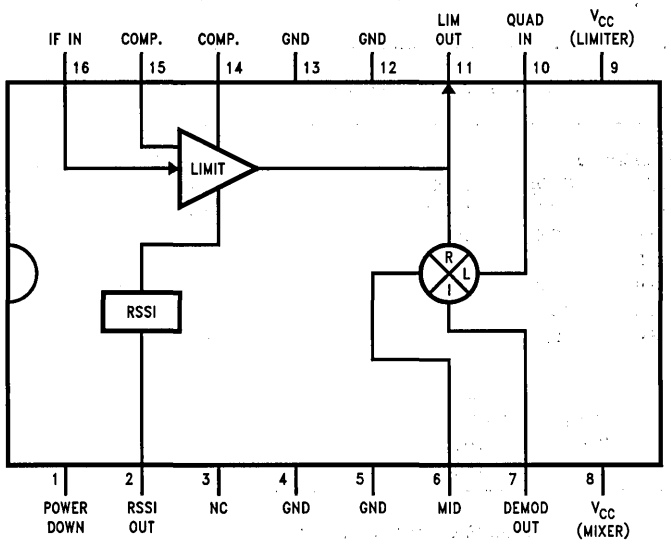
Features

- Typical operation at 110 MHz
- RF sensitivity to −75 dBm; RSSI sensitivity to −82 dBm
- High gain (70 dB) limiting amplifier
- Average current consumption: 480 μA for DECT handset (burst mode)
- +3V operation
- Power down mode for increased current savings
- Part of a complete receiver solution with the LMX2216 LNA/Mixer, the LMX2315/20 Phase-locked Loop, and the LMX2411 Baseband Processor
- Compliant to ARi1™ specification

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Digital cellular telephone systems
- Other wireless communications systems

Functional Block Diagram



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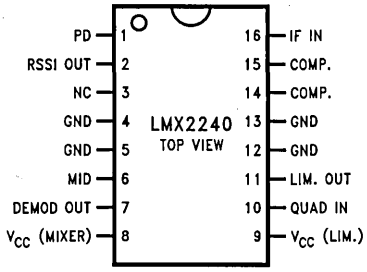
Connection Diagram

Small Outline Package



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Top View
Order Number LMX2240M
See NS Package Number M16A

Pin Description

Pin No.	Pin Name	I/O	Description
1	PD	I	Power Down; a HIGH signal switches the part to power down mode.
2	RSSI Out	O	Voltage output of the received signal strength indicator (RSSI).
3	NC		No connection
4	GND		Ground
5	GND		Ground
6	MID	O	Mid-range output of the discriminator; can be used for comparator threshold.
7	Demod Out	O	Demodulated output of the discriminator.
8	V_{CC} (Mixer)		Source voltage for the mixer (discriminator).
9	V_{CC} (Lim.)		Source voltage for the limiter.
10	Quad In	I	Quadrature input. A DC path from source through an inductor must be present at this pin, but, there must be no series resistance (a parallel resistor to the inductor is acceptable).
11	Lim. Out	O	Limiter output to the quadrature tank.
12	GND		Ground
13	GND		Ground
14	Comp.		Compensation pin for the limiter. See Applications Information for capacitor value.
15	Comp.		Compensation pin for the limiter. See Applications Information for capacitor value.
16	IF In	I	IF input to the limiter.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC})	6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) 3V	2.85	3.15	V
Operating Temperature (T_A)	−10	+70	°C

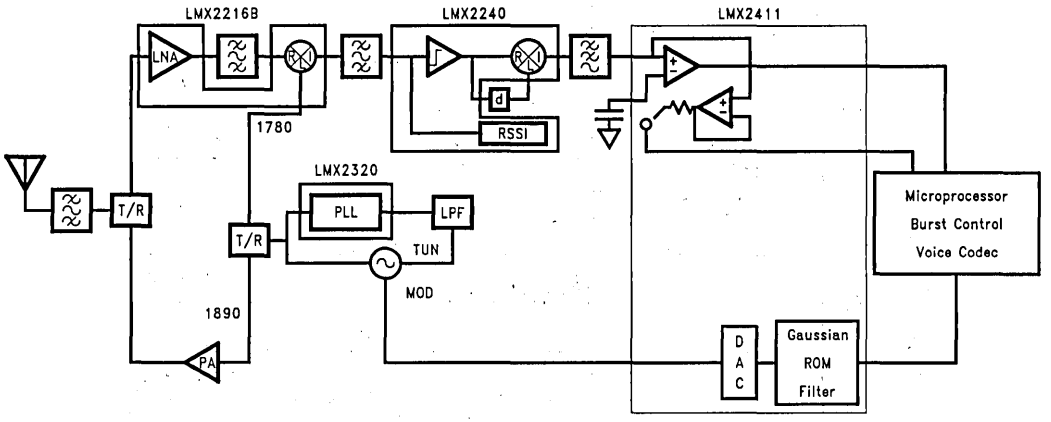
Electrical Characteristics

The following specifications apply for supply voltage V_{CC} = +3V ±5%, f_{IN} = 120 MHz, and T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Value Typ	Max	Units
I_{DD}	Supply Current			8	10	mA
I_{PD}	Power Down Current			115	200	µA
f_{max}	Maximum IF Input Frequency		120	150		MHz
f_{min}	Minimum IF Input Frequency			10		MHz
IF LIMITER						
NF	IF Limiter Noise Figure			11.5	12.5	dB
A_V	Limiter Gain	Z_L = 1000Ω		70		dB
sens	Limiter/Disc. Sensitivity	BER = 0.001		−75		dBm
IF_{in}	IF Limiter Input Impedance		150		225	Ω
IF_{out}	IF Limiter Output Impedance			250		Ω
V_{max}	Maximum Input Voltage Level			500		mV_{PP}
V_{out}	Output Swing		350	500		V_{PP}
Lim	Input Limiting Point			−70		dBm
DISCRIMINATOR						
V_{out}	Discriminator Output Peak-to-Peak Voltage (Note 1)	See Test Circuit	1.0	1.2		V_{PP}
V_{OS}	Disc. Output DC Voltage (Pin 7)		1.4		1.7	V
MID	Mid-Range Output (Pin 6)		1.4		1.7	V
$DISC_{in}$	Disc. Input Impedance			1000		Ω
$DISC_{out}$	Disc. Output Impedance			150		Ω
RSSI						
RSSI	RSSI Dynamic Range			70		dB
$RSSI_{out}$	RSSI Output Voltage	Pin = −80 dBm	0.35	0.5	0.8	V
		Pin = 0 dBm	1.15	1.5	1.8	V
	RSSI Slope	Pin = −70 dBm to −20 dBm	11	16		mV/dB
	RSSI Linearity			3		dB

Note 1: The discriminator output peak-to-peak voltage is measured by operating the discriminator mixer with two separate inputs (i.e., as a mixer). A beat frequency of 1 kHz is generated, and this tone's output swing is guaranteed to be at least 1.0 V_{PP}. When the mixer is configured as a discriminator with the limiter and a tank circuit, the guaranteed 1.0 V_{PP} output translates to (1.0V *(36/180) =) 200 mV_{PP} demodulated output, assuming at least 36° phase shift across the band of interest from the tank circuit.

Typical Application Block Diagram



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Functional Description

OVERVIEW

The LMX2240 IF demodulator is a low power IF processor that includes a frequency discriminator, an IF hard limiting amplifier, and a received signal strength indicator (RSSI). The LMX2240 is capable of differentially demodulating an FM or AM signal with as high an IF as 150 MHz, avoiding a costly second down-conversion. The RSSI output can be used for time gated channel measurements required in TDMA and other systems. Other features include high receiver sensitivity and a power down mode to allow for standby operation.

THE LIMITING AMPLIFIER

The limiting amplifier has a typical gain of 70 dB and a sensitivity of about −75 dBm. This allows it to be used in the DECT system with 20 dB net RF gain in front of it to achieve a sensitivity of −95 dBm. The limiter is a five stage amplifier with internal compensation at each stage to ensure stability. Two external compensation capacitors are also required to further enhance stability. The input to the limiter is a relatively low impedance to allow easy matching to typical IF surface acoustic wave (SAW) filters. The output of the limiter is connected off chip to an external quadrature tank circuit as well as connected internally to the discriminator (mixer). The output impedance of the limiter is 250Ω (typical).

THE RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

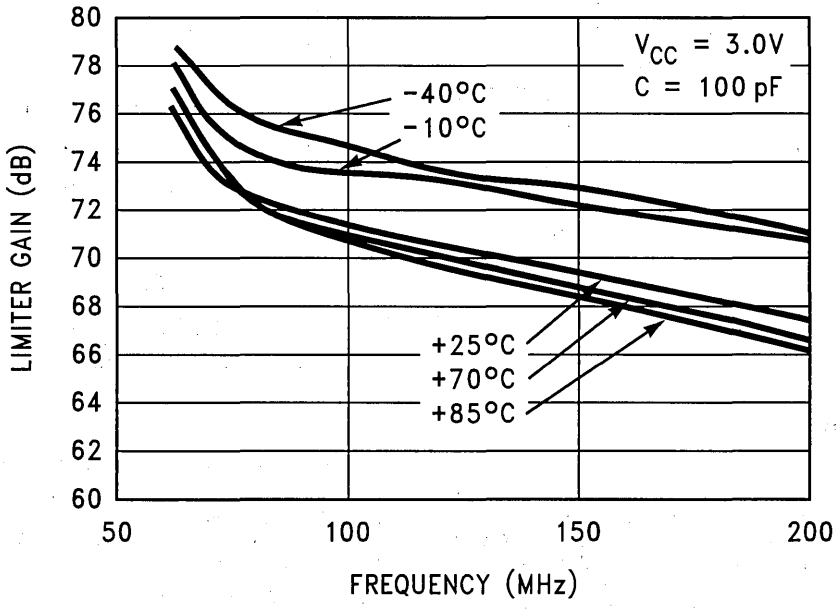
The RSSI circuit has a range of 70 dB. Its output voltage is proportional to the logarithm of the input signal level. The RSSI circuit has a sensitivity of −82 dBm. The output voltage of the circuit ranges from 0.5V to 1.5V typically.

THE FREQUENCY DISCRIMINATOR

The frequency discriminator is a Gilbert cell mixer that requires an external tank circuit to create a 90° phase shift at the desired frequency. The output of this circuit is centered at 1.5V by an internal level shifting circuit, and a mid-range voltage (at 1.5V) is also provided. The sensitivity of the discriminator to phase inaccuracies is 5.5 mV/degree (see Applications Information). This means that for a phase imbalance of 10°, the received eye diagram will be shifted by about 55 mV off of the 1.5V mid-range voltage. For the typical case, this amounts to about 10% of the output eye diagram (for 400 mV_{PP} output).

Typical Performance Characteristics

Limiter Gain vs Frequency with Temperature as a Parameter



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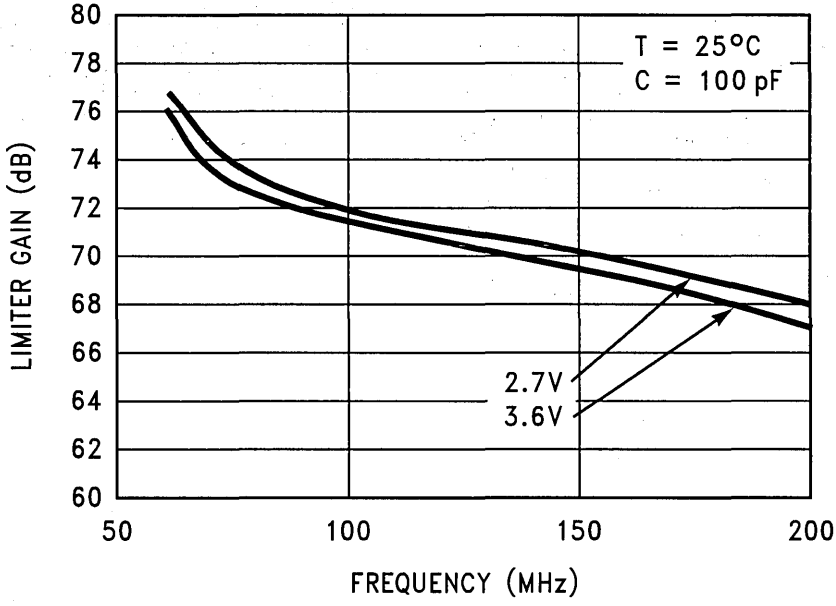
Limiter Gain vs Frequency with Supply Voltage as a Parameter



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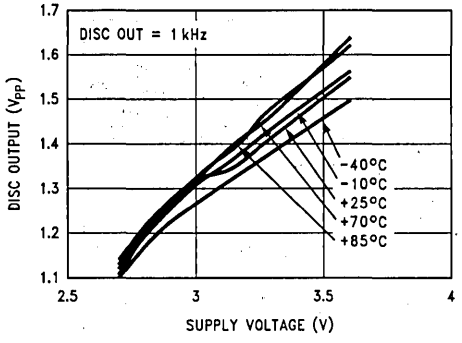
Typical Performance Characteristics (Continued)

Discriminator Output Peak-to-Peak Voltage vs Supply with Temperature as a Parameter



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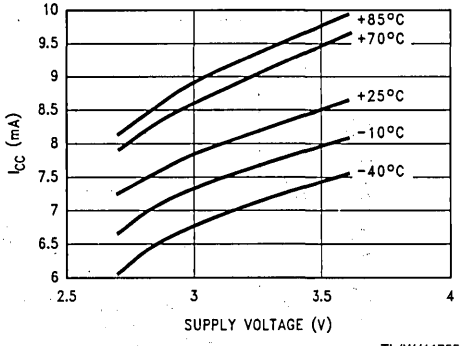
Current Consumption vs Supply Voltage with Temperature as a Parameter



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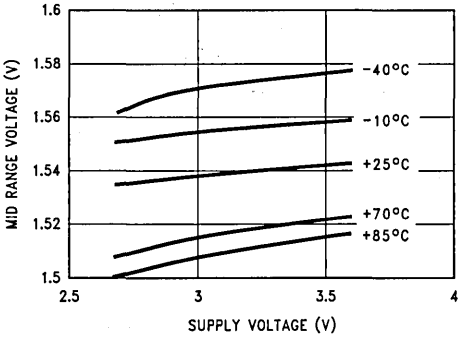
Mid-Range (Reference) Voltage vs Supply with Temperature as a Parameter



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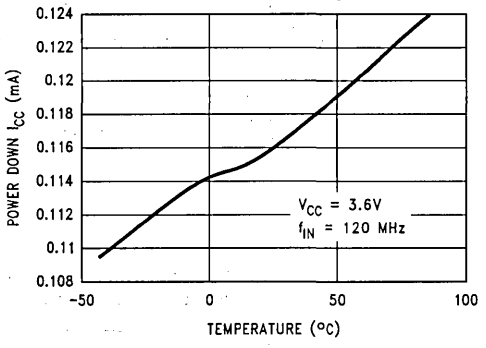
Power Down Current vs Temperature



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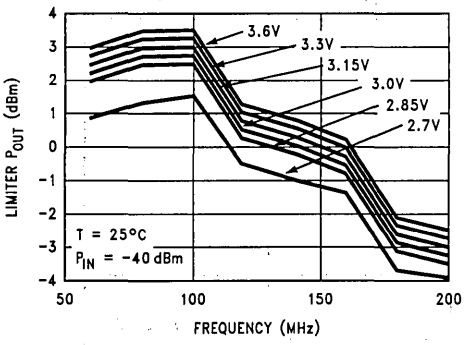
Limiter Output Power vs Frequency with Voltage as a Paramerer



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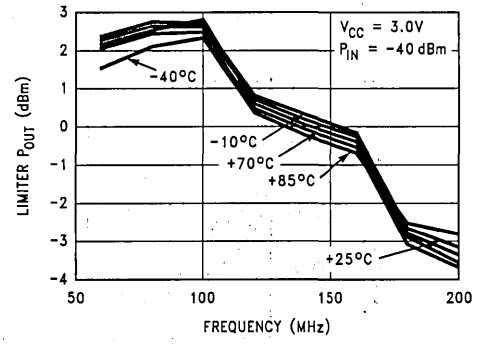
Limiter Output Power vs Frequency with Temperature as a Paramerer



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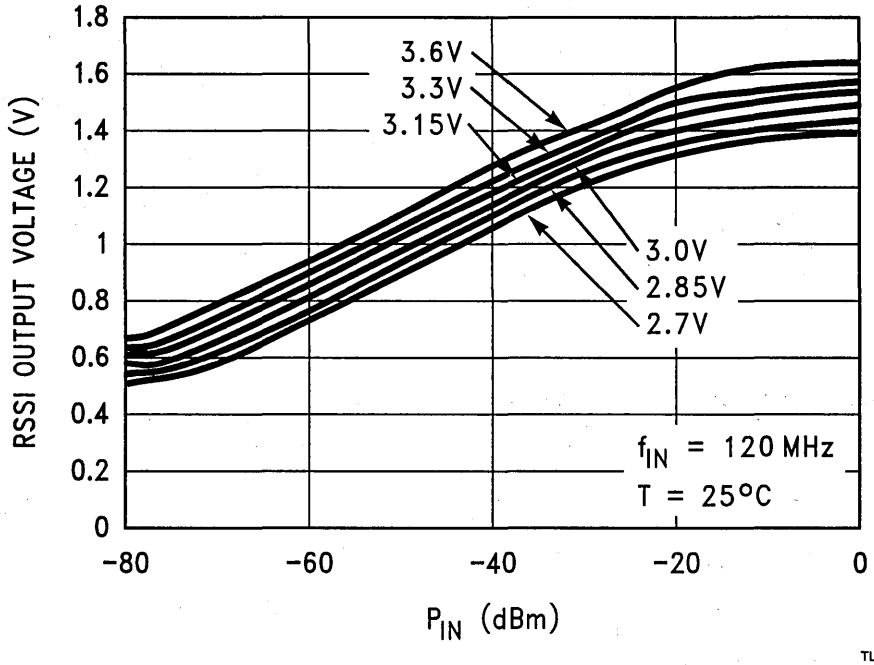
Typical Performance Characteristics (Continued)

RSSI Output vs Input Power with V_{CC} as a Parameter



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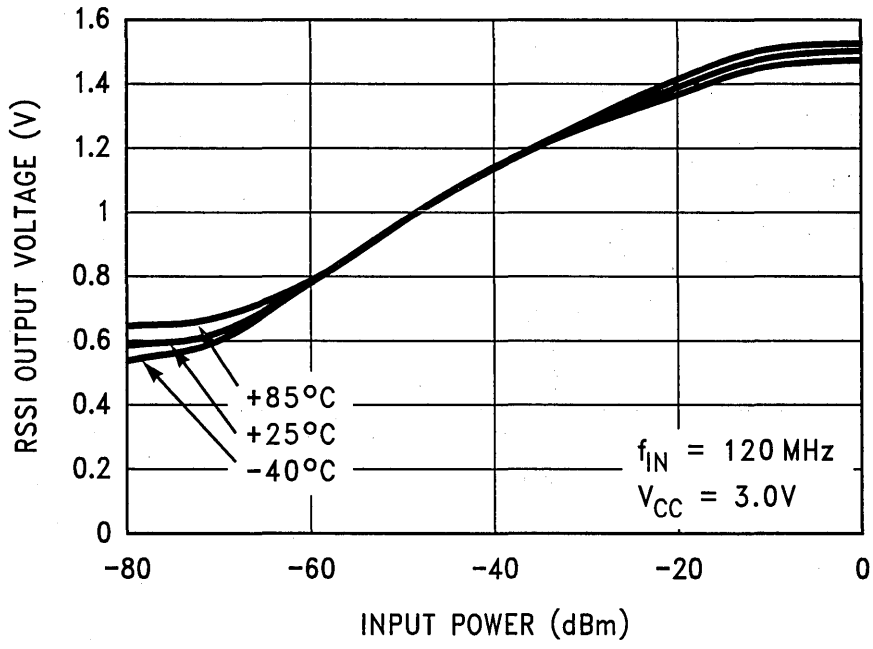
RSSI Output vs Input Power with Temperature as a Parameter



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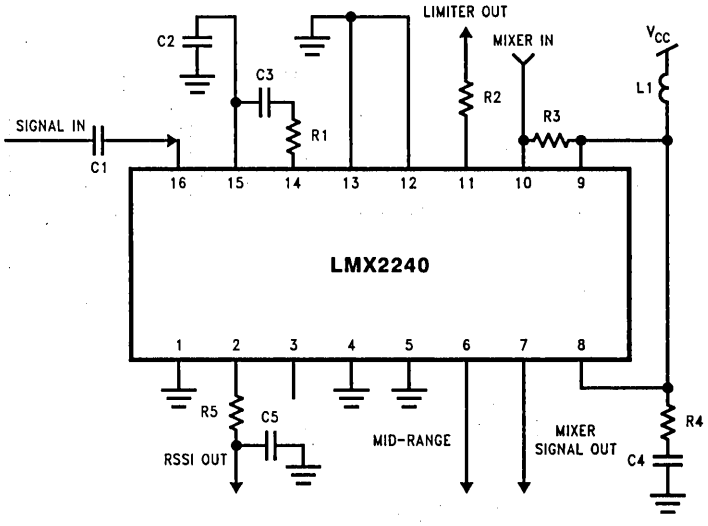
Automatic Test Circuit



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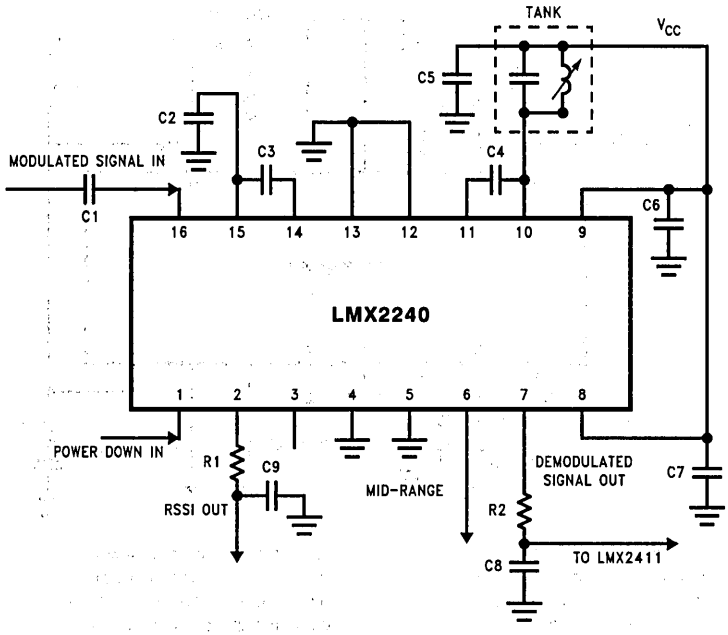
C1 = 1000 pF ±10% NPO Ceramic
C2 = 1000 pF ±10% NPO Ceramic
C3 = 1000 pF ±10% NPO Ceramic
R1 = 25Ω ±5% ¼W Thin Film Carbon
R2 = 1 kΩ ±5% ¼W Thin Film Carbon
R3 = 1 kΩ ±5% ¼W Thin Film Carbon
L1 = 10 μH ±5% Air Coil
C4 = 1000 pF ±10% NPO Ceramic
R4 = 20Ω ±5% ¼W Thin Film Carbon
C5 = 1000 pF ±10% NPO Ceramic
R5 = 3.9 kΩ ±5% ¼W Thin Film Carbon

Typical Application Example



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C1 = C2 = C3 = C5 = C6 = 100 pF ±10% NPO Ceramic
C4 = 1 pF ±10% NPO Ceramic
C7 = C9 = 0.01 µF ±10% NPO Ceramic
C8 = 82 pF ±10% X7R Ceramic
R1 = 4 kΩ ±5% ¼W Thin Film Carbon
R2 = 880Ω ±5% ¼W Thin Film Carbon
Tank = Toko #638AH-0294
All supporting components 0603 surface mount except tank.

Applications Information

THE INTERMEDIATE FREQUENCY LIMITER

The IF limiter has a large amount of gain at high enough frequency to cause concern about oscillation. To ensure that the limiter does not oscillate, a few precautions should be taken. The compensation capacitors that are used should be chosen to roll off any unwanted frequencies below the band of interest. The capacitor should be a high Q, RF type ceramic chip capacitor. For DECT, the capacitor value should be 100 pF, and the capacitors should be soldered as close to the LMX2240 as possible. This will create a pass band from 40 MHz to 150 MHz. The AC coupling capacitor at the input to the limiter (from the SAW filter) should be the same value as the compensation capacitors.

THE DISCRIMINATOR

There are two types of discriminator that can be used to demodulate FM signals. The first is a delay line discriminator, which uses a delay in one path of the received signal to introduce a phase difference between it and the received signal. The operation of the delay line discriminator is derived in the inset box. The other type of discriminator relies on a quadrature tank to directly introduce a phase shift in the received signal. This is the type of implementation that is commonly used in mobile communications because of its relative ease of construction and low cost.

The discriminator operates best when the inputs to it are hard-limited (i.e., square edges). If the input signal is small enough such that the IF amplifier cannot limit it, the output voltage swing of the limiter will suffer. Typically, the minimum voltage swing the discriminator can see and still fully switch is about 100 mV_{PP}. The two inputs to the discriminator can be of different peak-to-peak voltage swings as long as both are over the lower limit. This allows the quadrature tank circuit to have some insertion loss. In fact, up to 8 dB insertion loss can be tolerated while still ensuring that the discriminator output won't suffer.

The quadrature circuit can also affect the discriminator output voltage swing. The discriminator output voltage swing specified assumes perfect quadrature at the frequency of interest (mixer operation). With available analog components, perfect quadrature is not possible. This is due in part to the high frequency of the IF and the proportionally very narrow bandwidth of the desired signal. For example, a DECT signal is about 1 MHz wide, which is < 1% of the IF at which the demodulation occurs. This makes the quadrature circuit difficult to achieve. With moderately high Q components, however, a reasonable phase shift can be achieved with a single pole tank. This is illustrated by the following equation: the output of the discriminator is given by

$$DISC_{out} = \cos(\omega_c t) \bullet \cos(\omega_c t + \phi), \quad (1)$$

which results in

$$DISC_{out} = \cos(\omega_c t + \omega_c t + \phi) + \cos(\omega_c t - \omega_c t - \phi). \quad (2)$$

When the double frequency component is filtered out with a low pass filter, the cosine of the phase remains

$$DISC_{out} = \cos(-\phi) = \cos(\phi). \quad (3)$$

It can be seen that at 90° phase shift, the output will be zero. At 0°, the output will be 0.5, and at 180°, it will be −0.5. The output swing is then set by the multiplication of the cosine term with the discriminator output amplifier's gain.

With a circuit that gives an output peak-to-peak voltage of 1.0 V_{PP} (min) with ideal quadrature, the slope is seen to be 5.5 mV/degree. With a practical quadrature tank circuit at 110.6 MHz, the phase shift over a 1 MHz bandwidth is about 45°–50°, which translates to an output peak-to-peak voltage of about 250 mV_{PP}.

Assume the FM modulated signal is denoted as

$$s(t) = \cos(\omega ct + m(t)), \quad (4)$$

where $m(t) = m \int_{-\infty}^{t} b(t)\,dt$,

and b(t) is the modulating baseband signal. The constant m is defined as $m = 2\Delta fTb$. The signal s(t) must be delayed by some τ so that

$$I(t) = s(t+\tau) = \cos(\omega c(t+\tau) + m(t+\tau)). \quad (5)$$

If the delay τ is such that

$$\omega ct = 2n\pi + \frac{\pi}{2}, \quad n = 0, 1, 2, 3, \ldots, \quad (6)$$

then $s(t+\tau) = \sin(\omega ct + m(t+\tau))$, (7)

and multiplying (4) and (7) yields

$$s(t)\,I(t) = \cos(\omega ct + m(t)) \sin(\omega ct + m(t+\tau))$$

$$= \frac{1}{2}\sin(2\omega ct + m(t) + m(t+\tau)) \quad (8)$$

$$+ \frac{1}{2}\sin(m(t+\tau) - m(t)).$$

The double frequency component can be filtered off with a lowpass filter. If τ is kept small,

$$\frac{1}{2}\sin(m(t+\tau) - m(t)) \approx \frac{1}{2}[m(t+\tau) - m(t)]$$

$$= \frac{m}{2}\int_{-\infty}^{t+\tau} b(t)\,dt - \frac{m}{2}\int_{-\infty}^{t} b(t)\,dt \quad (9)$$

$$= \frac{m}{2}\int_{t}^{t+\tau} b(t)\,dt$$

$$\approx \tau\frac{m}{2}b(t).$$

The object for a delay line, then, is to maximize the delay while retaining the approximations necessary to satisfy (9), $\tau < 0.1$ Tb.

A Fast Locking Scheme for PLL Frequency Synthesizers

National Semiconductor
Application Note 1000
David Byrd
Craig Davis
William O. Keese

ABSTRACT

Frequency synthesizers are used in a large number of time division multiplexed (TDMA) and frequency hopping wireless applications where quickly attaining frequency lock is critical. A new frequency synthesizer is described which employs a scheme for reducing lock time by a factor of two using a conventional phase locked loop architecture. Faster lock is attained by shifting the loop filter's zero and pole corner frequencies while maintaining the PLL's gain/phase margin characteristics.

INTRODUCTION

RF system designers of TDMA based cellular systems, such as PHS, GSM and IS-54, need local oscillator (L.O.) or frequency synthesizer blocks capable of tuning to a new channel within a small fraction of each time slot. The suppression of reference spurs and phase noise is also critical for these modern digital standards. Base station and data transmission applications are now striving to utilize all the time slots available in each frame using a single synthesizer. This push towards a "zero blind slot" solution has put stringent demands upon the radio frontend's L.O. section.

The communication systems channel spacing determines the upper bound for the synthesizer's frequency resolution and loop filter bandwidth. More closely spaced channels dictate that the synthesizer's frequency resolution be finer, which in turn means the loop makes frequency corrections less often. A wider loop filter bandwidth would make it easier to attain lock within a given time constraint, but the price paid is less attenuation of the reference frequency sidebands and a higher integrated phase noise for the locked condition. An examination of the equations which govern the responsiveness of a closed loop system will provide some solutions to this dilemma.

CLOSED LOOP OPERATION

The basic phase-lock-loop configuration we will be considering is shown in *Figure 1*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2335TM, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. A passive loop filter configuration is desirable for its simplicity, low cost, and low phase noise.

The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the tuning resolution of the L.O. This reference signal, fr, is then presented to the input of a phase detector and compared with another signal, fp, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter. The phase detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The phase/frequency comparators function is to adjust the voltage presented to the VCO until the feedback signals frequency (and phase) match that of the reference signal. When this "phase-locked" condition exists, the VCO's frequency will be N times that of the comparison frequency.

Increasing the value of the N counter by 1 will cause the phase comparator to initially sense a frequency error between the reference and feedback signals. The feedback loop responds and eventually shifts the VCO frequency to be N+1 times the reference signal. The VCO's frequency has in effect increased by the minimum tuning resolution of the PLL. The rate at which the transition to the new operating frequency occurs is determined by the closed loop gain and stability criteria.

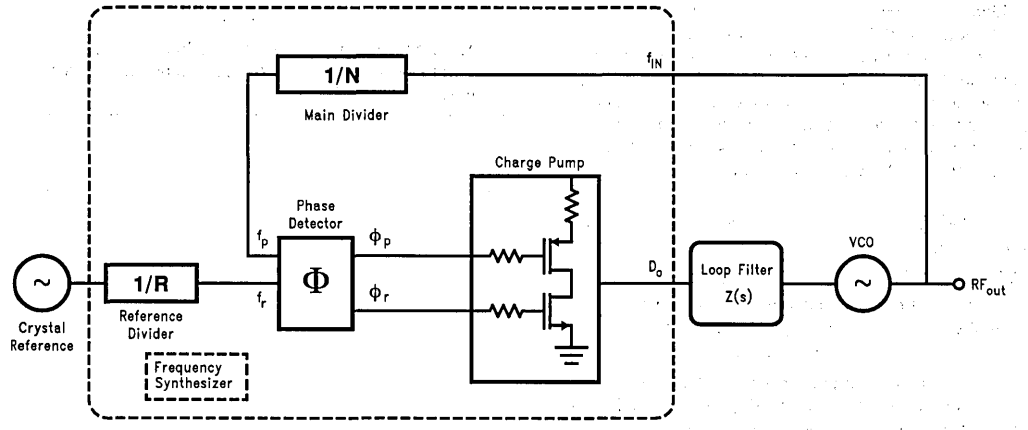

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FIGURE 1. Conventional PLL Architecture

LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (Kϕ), the VCO gain (Kvco/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in equation 2. [Ref 5]

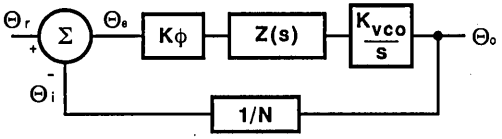

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FIGURE 2. PLL Linear Model

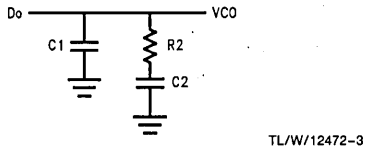

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FIGURE 3. Passive Loop Filter

$$\text{Open loop gain} = H(s)\,G(s) = \Theta i/\Theta e = K\phi\, Z(s)\, Kvco/Ns \quad (1)$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2 (C1 \bullet C2 \bullet R2) + s\,C1 + s\,C2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \bullet C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants Kϕ, Kvco, and N.

$$G(s) \bullet H(s)\Big|_{s = j\bullet\omega} = \frac{-K\phi \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\, C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (4)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45°. Given the pressure to minimize lock time, the cutoff frequency of the loop would be selected just wide enough to suppress the PLL's reference frequency spurs to a tolerable level.

If we were now to redefine the cut off frequency, ω_p', as double the frequency which gave us our desired level of spurs, ω_p, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed FastLock™ scheme, the higher spur levels and wider loop filter conditions would ex ist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase equations 4 and 5 will have to compensate by the corresponding "$1/\omega$" or "$1/\omega^2$" factor. Examination of equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "ω" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at $\omega_p' = 2\,\omega_p$. Kvco, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the ω^2 term present in the denominator of equation 3. Altering Kvco could be difficult at best, however, both N and Kϕ gain terms are readily available in an integrated PLL IC. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in FastLock. Changing the N gain term could also have been chosen to accomplish our objective. In fact, doing so causes the PLL's reference frequency to be pushed over in the frequency domain along with the loop cutoff frequency. Unfortunately changing N also means changing the R counter value by the same factor. And while this is feasible, it probably means employing fractional counter techniques along with all the associated problems of this approach, as an N/4 term may no longer be an integer.

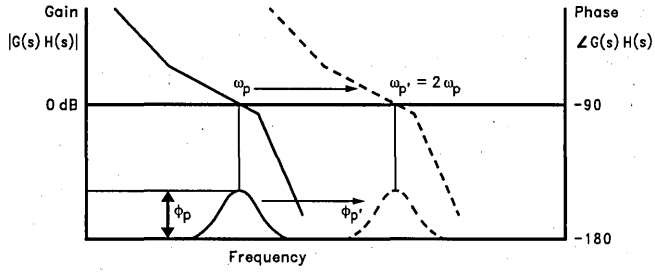

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FIGURE 4. Open Loop Response Bode Plot

CIRCUIT IMPLEMENTATION

A diagram of the FastLock scheme as implemented in National Semiconductors LMX2335 PLL is shown in *Figure 5*. When a new frequency is loaded, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second resistor element, R2, to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the PLL will then return to standard, low noise operation. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between FastLock and standard mode.

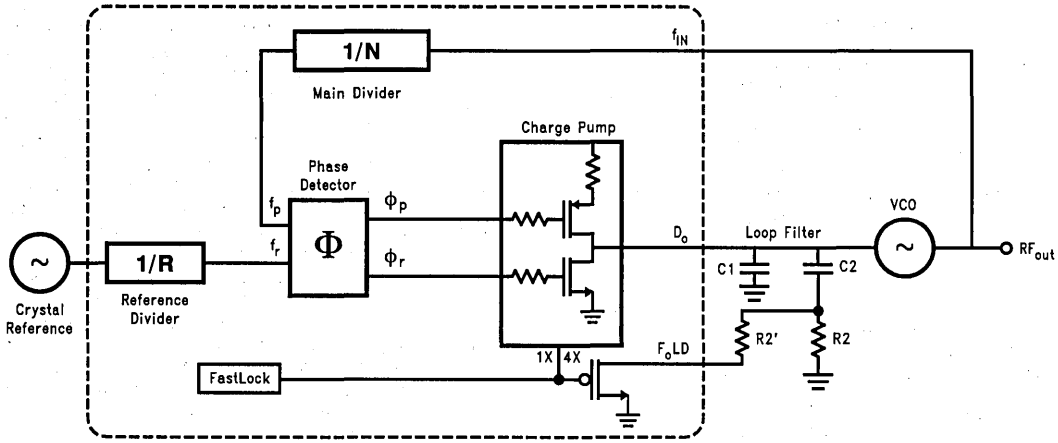

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FIGURE 5. FastLock PLL Architecture

RESULTS

An LMX2335 PLL was utilized to address the following IS-54 application constraints:

Fvco = 900 MHz, Kv = 20 MHz/V,

Channel spacing = 30 kHz.

The PLL's device attributes were as follows:

$K\phi = 1\ mA/2\pi$, N = 30,000,

Fref = 30 kHz, Fo = 3 kHz.

The loop filter values used were:

C1 = 1800 pF, R2 = 12 kΩ, C2 = 0.012 μF

The modulation domain analyzer graphs in *Figures 6–9* show the transient lock responses for the normal 1 mA mode condition side by side with the response for the FastLock mode. The FastLock operation in *Figure 9* shows lock being attained within 1 ms (to within ±1 kHz) for a frequency jump of 50 MHz, compared with 1.8 ms for the standard condition *(Figure 8)*. As much as a 2 kHz frequency disturbance can result when switching back to normal operation after steady state is fully attained. By switching out of the FastLock mode when the PLL has settled to near the desired frequency tolerance, almost the entire 2X increase in lock time can be achieved.

SUMMARY

The FastLock circuitry of the LMX2335 frequency synthesizer provides a means of improving TDMA channel switching speed, without compromising reference spur quality or phase noise. Zero blind slot RF synthesizer designs can more easily be attained through this technique.

REFERENCES

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[3] S. Swisher, et. al., *Synchronized Frequency Synthesizer with High Speed Lock*, U.S. Patent #4,330,758, 1982.

[4] K. Arnold, *Low Noise Frequency Synthesizer Using Half Integer Dividers and Analog Gain Compensation*, U.S. Patent #5,307,071, 1994.

[5] Keese, W.O., *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge-Pump Phase-Locked Loops*, RF Expo West, January 1995.

[6] Barker, Cynthia, *Introduction to Single Chip Microwave PLLs*, National Semiconductor Application Note, AN885, March 1993.

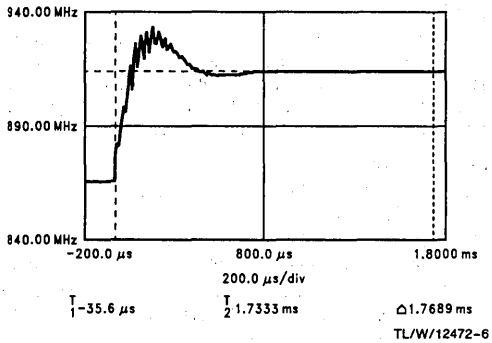

FIGURE 6. Normal Switching Waveform

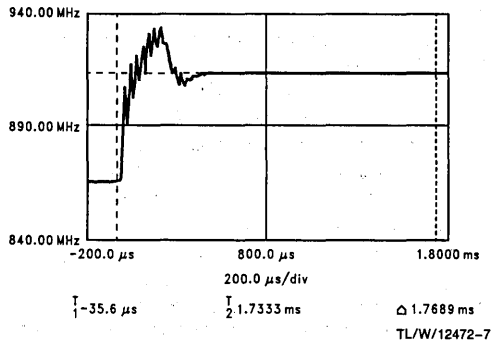

FIGURE 7. FastLock Switching Waveform

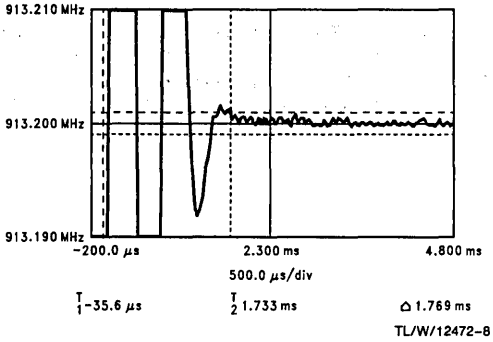

FIGURE 8. Normal Mode Lock Time

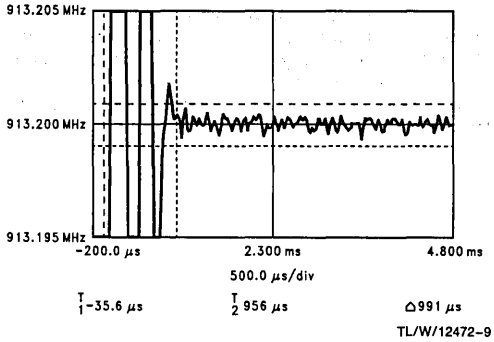

FIGURE 9. FastLock Mode Lock Time

An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops

National Semiconductor
Application Note 1001
William O. Keese

The high performance of today's digital phase-lock loop makes it the preferred choice for generation of stable, low noise, tunable local oscillators in wireless communications applications. This paper investigates the design of passive loop filters for Frequency Synthesizers utilizing a Phase-Frequency Detector and a current switch charge pump such as National Semiconductor's PLLatinum™ Series. Passive filter design for a TYPE II third order phase-lock loop is discussed in depth, with some discussion of higher order filters included. Specific test results are presented for a GSM synthesizer design. Optimization of phase-lock loop performance with respect to different parameters is discussed.

The basic phase-lock-loop configuration we will be considering is shown in *Figure 1*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2315TM, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, and programmable frequency dividers. A passive filter is desirable for its simplicity, low cost, and low phase noise.

In most standard PLL's there are several design parameters which can be treated as constant values. This linear approximation provides a good estimation of loop performance. The values of the PLL filter design constants depend on the specific application. For example, $K\phi$ is determined by the synthesizer charge pump output current magnitude. The notation and definitions for these values along with standard units used throughout this paper are given in Table I below.

TABLE I. PLL Filter Design Constants

Kvco - (MHz/Volt)

Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

Kϕ - (mA/2πrad)

Phase detector/charge pump constant. The ratio of the current output to the input phase differential.

RFopt - (MHz)

Radio Frequency output of the VCO at which the loop filter is optimized.

Fref - (kHz)

Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

N

Main divider ratio. Equal to RFopt/Fref.

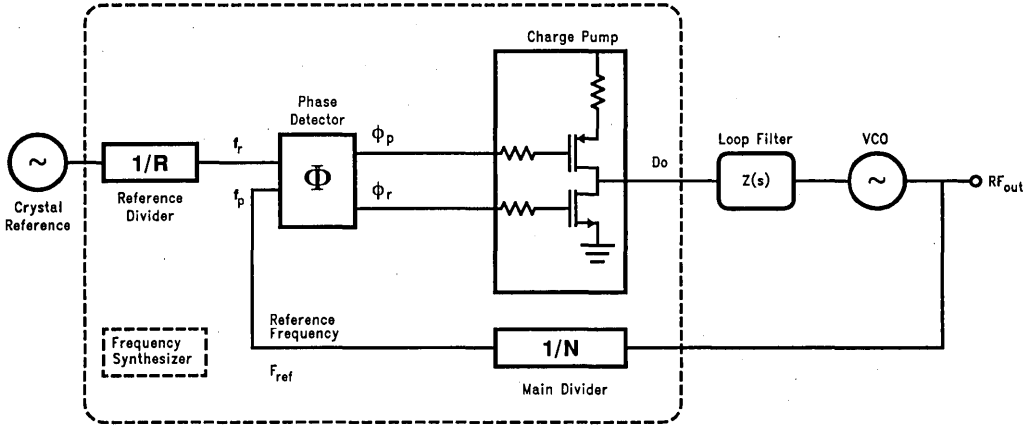

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FIGURE 1. Basic Charge Pump Phase Locked Loop

Some basic knowledge of control loop theory is necessary in order to understand PLL filter dynamics. For a more thorough treatment consult references [1] through [6]. A linear mathematical model representing the phase of the PLL in the locked state is presented in *Figure 2*. An additional integrator is needed in the transfer function for the forward gain and is usually lumped together with the VCO in the literature, references [1-4]. Using the simplified diagram in *Figure 2*, and feedback theory, one may obtain the equations for the phase transfer functions presented in Table II.

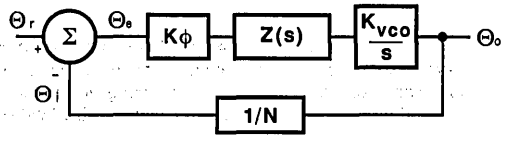

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FIGURE 2. PLL Linear Model

TABLE II. PLL Phase Transfer Functions

Forward loop gain	$G(s) = \Theta o/\Theta e$
	$= K\phi\ Z(s)\ Kvco/s$
Reverse loop gain	$H(s) = \Theta i/\Theta o = 1/N$
Open loop gain	$H(s)\ G(s) = \Theta i/\Theta e$
	$= K\phi\ Z(s) Kvco/Ns$
Closed loop gain	$\Theta o/\Theta i = G(s)/[1 + H(s)\ G(s)]$

The standard passive loop filter configuration for a type II current mode charge pump PLL is shown in *Figure 3*. The loop filter is a complex impedance in parallel with the input capacitance of the VCO, or in other words, a driving point immitance.

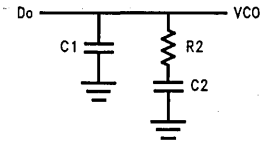

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FIGURE 3. 2nd Order Passive Filter

The phase detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The shunt capacitor C1 is recommended to avoid discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. A low pass filter section may be needed for some high performance synthesizer applications that require additional rejection of the reference sidebands, known as spurs.

One method of filter design uses the open loop gain bandwidth and phase margin to determine the component values. Locating the point of minimum phase shift at the unity gain frequency of the open loop response as shown in *Figure 4* ensures loop stability. The phase relationship between the pole and zero also allows easy determination of the loop filter component values. The phase margin, ϕ_p, is defined as the difference between 180° and the phase of the open loop transfer function at the frequency, ω_p, corresponding to 0-dB gain. The phase margin is chosen between 30° and 70°. When designing for a higher phase margin you trade off higher stability for a slower loop response time and less attenuation of Fref. A common rule of thumb is to begin your design with a 45° phase margin.

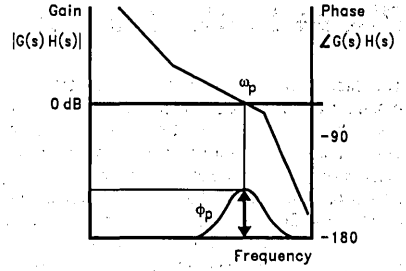

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FIGURE 4. Open Loop Response Bode Plot

The impedance of the second order filter in *Figure 3* is

$$Z(s) = \frac{s\,(CS \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (1)$$

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (2a) \qquad T2 = R2 \bullet C2 \quad (2b)$$

Thus the 3rd order PLL Open Loop Gain in Table II can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants $K\phi$, Kvco, and N.

$$G(s) \bullet H(s)\Big|_{s=j\bullet\omega} = \frac{-Kpd \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\,C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (3)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 4. The available phase margin therefore is proportional to the ratio of C1 and C2.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (4)$$

By setting the derivative of the phase margin equal to zero as shown in equation 5,

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \quad (5)$$

the frequency point corresponding to the phase inflection point is found in terms of the filter time constants T1 and T2. This relationship is given in equation 6.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \quad (6)$$

To insure loop stability, we want the phase margin to be maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{Kpd \bullet Kvco \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \quad (7)$$

Therefore, if the loop bandwidth, ω_p, and the phase margin, ϕ_p, are specified, equations 1 through 7 allow us to calculate the two time constants, T1 and T2.

The formulas for T1 and T2 are shown in equations 8 and 9.

$$T1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p} \quad (8)$$

$$T2 = \frac{1}{\omega_p^2} \bullet T1 \quad (9)$$

From the time constants, T1, T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 10 to 12.

$$C1 = \frac{T1}{T2} \bullet \frac{Kpd \bullet Kvco}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (10)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

Current switching noise in the dividers and the charge pump at the reference rate, Fref, may cause unwanted FM sidebands at the RF output. In wireless communications, the phase detector comparison frequency is generally a multiple of the RF channel spacing. These spurious sidebands can cause noise in adjacent channels. Additional filtering of the reference spurs is often times necessary, depending on how narrow your loop filter is. This is usually the case in today's TDMA digital cellular standards, such as GSM, PDC, PHS, or IS-54. The sub-millisecond lock times necessary for switching between channel frequencies makes a relatively wide loop filter mandatory. For these performance critical synthesizer applications placing a series resistor and a shunt capacitor prior to the VCO provides a low pass pole for more attenuation of unwanted spurs. The use of a passive loop filter eliminates the noise contributions from an op amp in an active filter. This is critical due to the strict RMS. phase error, and integrated phase noise requirements. The recommended filter configuration is shown in *Figure 5*.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log [(2\pi Fref \bullet R3 \bullet C3)^2 + 1] \quad (13)$$

Defining the additional filter time constant as

$$T3 = R3 \bullet C3 \quad (14)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{(ATTN/20)} - 1}{(2\pi \bullet Fref)^2}} \quad (15)$$

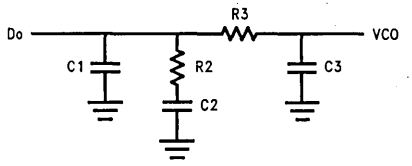

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FIGURE 5. 3rd Order Lowpass Filter

The additional pole must be lower than the reference frequency, in order to significantly attenuate the spurs, but must be at least 5 times higher than the loop bandwidth, or the loop will almost assuredly become unstable. In order to compensate for the added low pass section, the filter component values are recalculated using the new open loop unity gain frequency, ω_c, as in equation 17. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2. Note that ω_c is slightly $< \omega_p$, therefore the frequency jump lock time will increase. Although not exact, the linear assumptions used in this design technique provide suprisingly good results for loop filter bandwidths of up to 1/5 of the reference rate. The derivation of ω_c is included in the appendix.

$$T2 = 1/\omega_c^2 \bullet (T1 + T3) \quad (16)$$

$$\omega_c = \frac{\tan \phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \times \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan \phi \bullet (T1 + T3)]^2}} - 1 \right] \quad (17)$$

$$C1 = \frac{T1}{T2} \frac{Kpd \bullet Kvco}{\omega_c^2 \bullet N} \times \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)} \right]^{1/2} \quad (18)$$

Similar to the 2nd Order filter we have

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right); \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

The only component values that need to be determined comprise the added low pass pole. Since these values are solely determined from equations 13 and 14, their values are somewhat arbitrary. It is not prudent, however to have a capacitor value for C3 which is equal to or greater than the other capacitors. As rule of thumb choose C3 $\leq$ C1/10, otherwise T3 will interact with the primary poles of the filter. Likewise, choose R3 at least twice the value of R2. When selecting C3 you must also take into account the input capacitance of the VCO tuning varactor diode which will add in parallel.

The following example is a typical synthesizer developed for the Global System Mobile (GSM) digital cellular standard using the described filter design technique. The RF channel spacing is 200 kHz, and a typical synthesizer frequency range is from 865 MHz–915 MHz. Since the addition of a low pass filter will reduce the closed loop bandwidth slightly, select an initial design value which is slightly larger than desired.

Example

$$\mathbf{Kvco} = 20\ \text{MHz/V}.$$

$$\mathbf{Kphi} = 5\ \text{mA}$$

$$\mathbf{RFopt} = 900\ \text{MHz}$$

$$\mathbf{Fref} = 200\ \text{kHz}$$

$$\mathbf{N} = \mathbf{RFopt/Fref} = 4500$$

$$\omega_p = 2\pi * 20\ \text{kHz} = 1.256e5$$

$$\phi_p = 45°$$

$$\mathbf{ATTEN} = 20\ \text{dB}$$

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} = 3.29e-6$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \bullet 200e3)^2}} = 2.387e-6$$

$$\omega_c = \frac{(3.29e{-}6 + 2.387e{-}6)}{[(3.29e{-}6 + 2.387e{-}6)^2 + 3.29e{-}6 \bullet 2.387e{-}6]} \times \left[\sqrt{1 + \frac{(3.29e{-}6 + 2.387e{-}6)^2 + 3.29e{-}6 \bullet 2.387e{-}6}{[(3.29e{-}6 + 2.387e{-}6)]^2}} - 1\right]$$

$$\omega_c = 7.045e4$$

$$T2 = \frac{1}{(7.045e4)^2} \bullet (3.29e{-}6 + 2.387e{-}6) = 3.549e{-}5$$

$$C1 = \frac{3.29e{-}6}{3.549e{-}5} \frac{(5.0e{-}3) \bullet 20e{+}6}{(7.045e4)^2 \bullet 4500} \times \left[\frac{[1 + (7.045e4)^2 \bullet (3.549e{-}5)^2]}{[1 + (7.045e4)^2 \bullet (3.29e{-}6)^2 \parallel 1 + (7.045e)^2 \bullet (2.39e{-}6)^2]}\right]^{1/2}$$

$$C1 = 1.085\ \text{nF}$$

$$C2 = 1.085\ \text{nF} \bullet \left(\frac{3.55e{-}5}{3.29e{-}6} - 1\right) = 10.6\ \text{nF};$$

$$R2 = \frac{3.55e{-}5}{10.6e{-}9} = 3.35\ \text{k}\Omega;$$

if we choose $R3 = 22\ \text{k}\Omega$;

then $$C3 = \frac{2.34e{-}6}{22e3} = 106\ \text{pF}$$

Converting the calculated numbers to standard component values gives the filter shown in the test board schematic for the synthesizer implementation, *Figure 6*.

Test results for the PLL loop filter design using a National Semiconductor LMX2315 Frequency Synthesizer are shown in the following pages. A 10 MHz crystal oscillator was used as the reference oscillator input signal. The supply voltage was 5V, and the entire current consumption, including the VCO, was <15 mA.

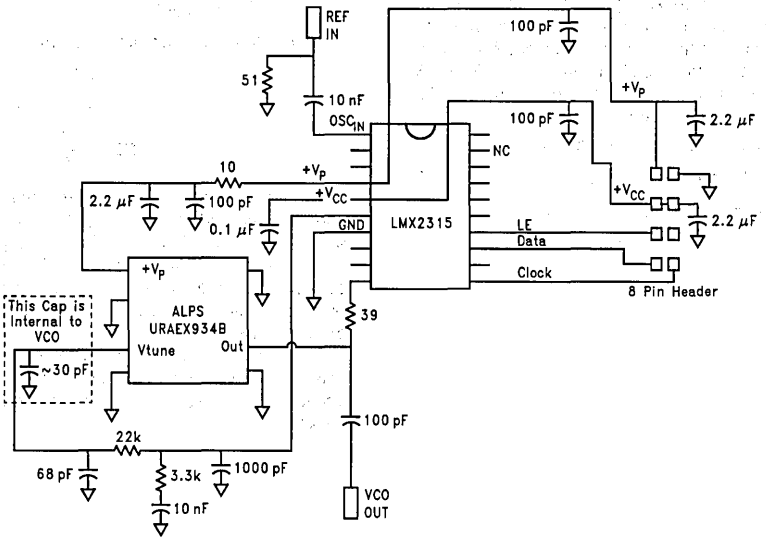

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FIGURE 6. Test Fixture Schematic

Figures 7 to *9* show HP8566 Spectrum Analyzer measurements of the RF output. The measured closed loop filter bandwidth is between 15 kHz and 17.5 kHz. The reference spurious level is ≤70 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2315. The phase noise level at 1 kHz offset in *Figure 9* is −79.5 dBc/Hz. This correlates to a phase noise floor of ≤150 dBc/Hz. The relatively flat PLL closed loop characteristics gives a measured RMS. phase error of <2°, and is also an indicator of good loop stability.

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. The HP53310A Modulation Domain Analyzer plots in *Figures 10* and *11* show the positive and negative switching waveforms for a frequency jump of 865 MHz–915 MHz. The well balanced charge pump of the LMX2315 frequency synthesizer causes the waveforms to be nearly inverted replicas of each other. Narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±500 Hz. The lock time is seen in *Figure 12* to be <500 μs for a frequency jump of 50 MHz.

CONCLUSION

An analysis of a frequency domain design technique for passive filters in charge pump phase-locked loops was presented. Measurements of a PLL designed using this method show good results in a practical synthesizer realization. The results demonstrate a high performance synthesizer in conjunction with a passive loop filter provide a fast switching, low noise frequency source for today's challenging digital wireless telecommunications standards.

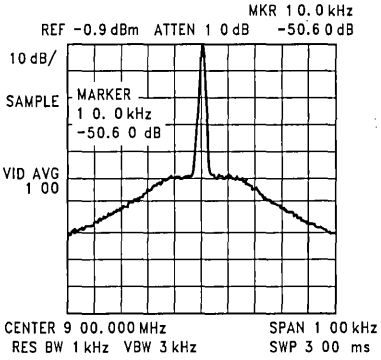

FIGURE 7. PLL Output Spectrum 100 kHz span

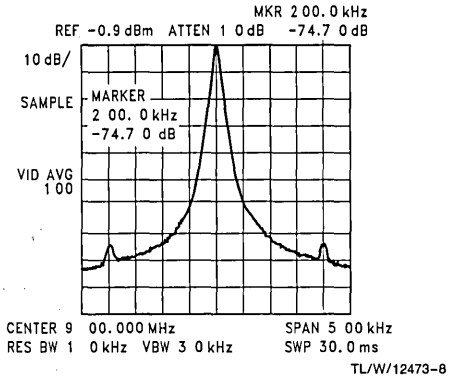

FIGURE 8. PLL 200 kHz Reference spurs

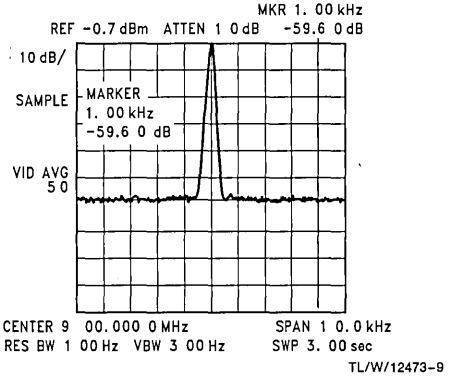

FIGURE 9. PLL Close in Phase Noise

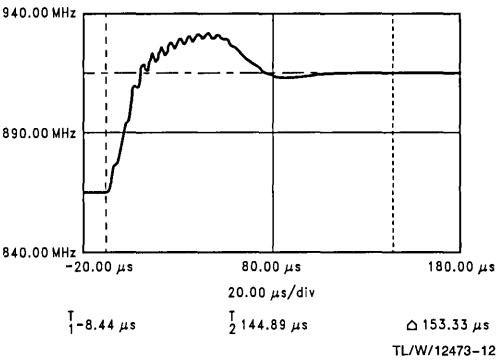

FIGURE 10. PLL Positive Frequency Jump Waveform

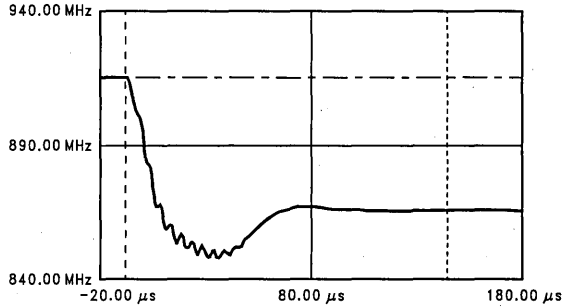

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FIGURE 11. PLL Negative Frequency Jump Waveform

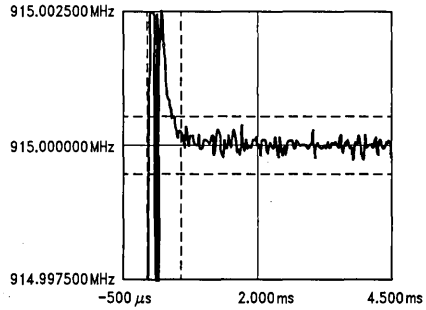

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FIGURE 12. PLL Frequency Jump Lock Time

APPENDIX

Derivation of ωc

The impedance of the loop filter shown in *Figure 5* is

$$Z_T(s) = \frac{Z(s) \bullet \left(\frac{1}{s\,C3}\right)}{Z(s) + R3 + \left(\frac{1}{s\,C3}\right)} \tag{19}$$

where Z(s) is given by equation 1.

Knowing that $C1 \geq 10\,C3;$

and by substituting $T3 = R3 \bullet C3$

along with equations 2a, 2b.

simplifies the third order equation for the open loop gain to

$$G(s) \bullet H(s)\Big|_{s = j\bullet\omega} = \frac{-Kpd \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\,C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \bullet \frac{1}{(1 + j\omega \bullet T3)} \tag{20}$$

$$\phi(\omega) \infty (1 + \omega \bullet T2) \bullet (1 - \omega \bullet T1) \bullet (1 - \omega \bullet T3) \tag{21}$$

Similar to equation 9

$$T2 = \frac{1}{\omega^2\,(T1 + T3)} \tag{22}$$

Substituting (22) into (21) gives

$$\phi(\omega) \infty 2 - \omega^2 \bullet T1 \bullet T3 - j\omega \bullet (T1 + T3) + \frac{j}{\omega \bullet (T1 + T3)} - \frac{j\omega \bullet T1 \bullet T3}{(T1 + T3)} \tag{23}$$

Thus

$$\tan\phi = \frac{-\omega \bullet (T1 + T3) - \frac{\omega \bullet T1 \bullet T3}{(T1 + T3)} + \frac{1}{\omega \bullet (T1 + T3)}}{2 - \omega^2 \bullet T1 \bullet T3} \tag{24}$$

Assuming $\omega^2 \bullet T1 \bullet T2 \ll 2$ (25)

After some manipulation we arrive at the characteristic equation

$$\omega^2 + \omega \frac{2 \tan\phi \bullet (T1 + T2)}{[(T1 + T3)^2 + T1 \bullet T3]} - \frac{1}{(T1 + T3)^2 + T1 \bullet T3} = 0 \tag{26}$$

Taking the negative root, and multiplying through gives the expression for the closed loop bandwidth, ω_c, equation (20).

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right]$$

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[4] Gardner, F.M., *Phase-Locked Loop Techniques,* 2nd ed., John Wiley & Sons, 1980

[5] Gardner, F.M., *Charge-Pump Phase-Lock Loops,* IEEE Trans. Commun., vol. COM-28, pp 1849–1858, Nov 1980

[6] Barker, Cynthia, *Introduction to Single Chip Microwave PLLs,* National Semiconductor Application Note, AN885, March 1993

Upgrading from the MB150X to National LMX1501A: Replacement Issues

National Semiconductor
Application Note 935

ABSTRACT

Compatibility of the LMX1501AM with the MB1501(std, and options H, and L) and MB1502 (in the FPT-16P-M06 package option) is inspected with emphasis on issues related to dual sourcing, or replacement of the MB150X parts with the LMX1501A. The devices are fundamentally similar, with identical (1501) or compatible (1502) pin outs, and identical programming specifications. Some key differences are found, however, which require attention. These include, package size and footprint, charge pump characteristics, loop filter configuration, and programming timing. In many cases the LMX1501A will easily replace MB150X components with few or no changes at all. This will not be true in all cases, however, particularly when data sheet programming specifications of the MB150X or LMX1501A have not been followed, or when high charge pump tuning voltages are required.

SIMILARITIES

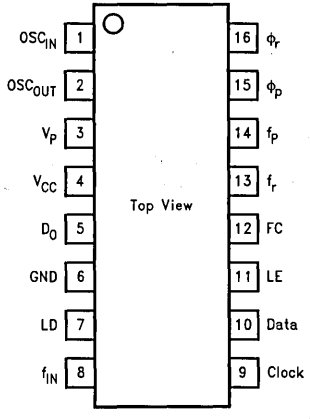
- Architecture
- Pinout
- Operating voltage (V_{CC})
- Programming content, format, and levels
- Temperature range
- RF fin sensitivity and impedance

DIFFERENCES

- Package Size/Footprint
- Charge pump magnitude, balance, deadband
- Charge pump maximum supply voltage
- Loop filter configuration
- Programming timing. (Faster, t_{ES})
- I_{CC} vs V_{CC} dependency

COMMON ELEMENTS

The LMX1501A and MB1501(H/L)—2 have a great deal in common. Both devices consist of 1.1 GHz programmable prescalers with an option of 64/65 or 128/129 dual modulus division. Both have a reference divider channel. Both have an internal phase detector and charge pump circuit, and outputs which allow use of an external charge pump circuit. The MB1501 and the LMX1501A share pinout and definitions, and the LMX1501A and MB1502 have compatible pinouts, shown in *Figure 1.* The components operate over the same temperature and voltage ranges (except the MB1502 operates only at 5V) and are programmed with the same information in the same format. For all these similarities, there are a number of key distinctions. This application note is focused on those issues which are relevant to replacing the MB150X with the LMX1501A. This means that certain performance improvements in the LMX1501A are not listed at length, and no effort is made to compare and contrast the parts generally. Full specifications are available in the LMX1501A data sheet—Lit. # 108500.



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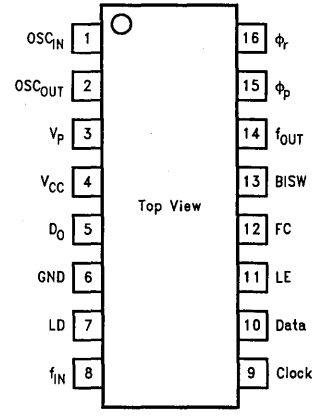
a) LMX1501A/MB1501



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b) MB1502

FIGURE 1. Pinouts

PHYSICAL DIFFERENCES

Footprint. The MB1501 and MB1502 are packaged in a EIAJ standard SO 16. This package has a pin to pin pitch of 0.050 in. with a **body width of 0.209"**. The NSC LMX1501A is packaged in a standard JEDEC SO 16, which has the same pin to pin pitch, but a **body width of 0.153"**. *Figure 2* shows an overlay of the JEDEC package on a PCB showing (typical) EIAJ solder pads. *Figures 3* and *4* show the dimensions of the two packages. Re-layout of the PCB is advisable, but probably not mandatory. Although not optimal, lengthening the solder pads by 0.35" will accommodate both package types. ***Corrective action:*** *re-design the PCB using a smaller footprint.*

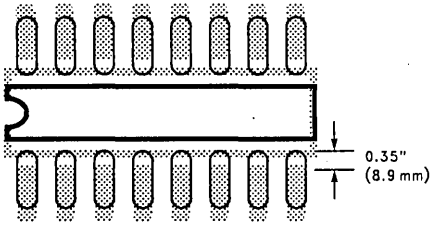

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FIGURE 2. Footprint Overlay

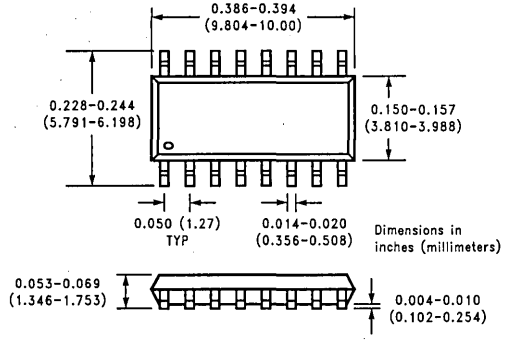

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FIGURE 3. LMX1501A Outline Drawing

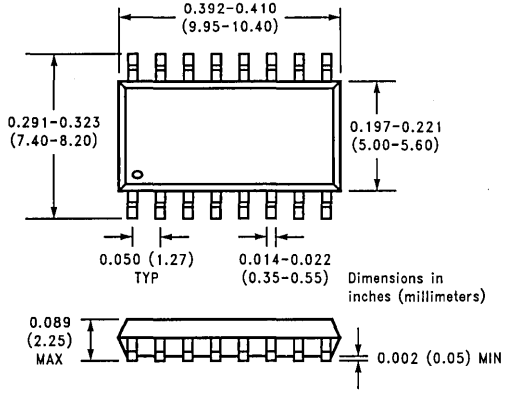

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FIGURE 4. MB150X Outline Drawing

Loop Filter Configuration. *Figure 5* shows a loop filter topology which is often found with MB150X components. It is unusual in its placement of a series resistor before the integrating capacitor. This resistor effectively causes the voltage at the charge pump (CP) output to increase instantaneously as the CP delivers large current pulses. For the MB150X, since the sink current is much higher than the source current, the delivered pump up current is limited by this resistor, which makes the negative frequency lock time increase. Because of the low output of the MB150X charge pump source current, the series R does not noticeably degrade performance, and it allows an additional lowpass filter function to cope with the large spurious response caused by time and current imbalance. The LMX1501A, however, with a balanced CP design, is sensitive to this resistance. It causes current limiting in the CP output, D_O, which decreases the phase detector gain. This effect is most noticeable in large frequency steps or steps towards the high end of the tuning range. Fortunately, this resistance can be removed with no ill effect. The dramatically lower spurious content of the LMX1501A eases the filter requirement substantially. ***Corrective Action:*** *remove and short the series resistor at* D_O.

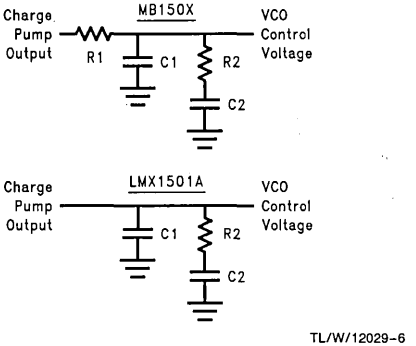

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FIGURE 5. Loop Filters

ELECTRICAL DIFFERENCES

Charge pump output magnitude and balance of the source and sink currents can be seen in *Figure 6.* Laboratory measurements of the LMX1501A/MB1501 sink and source currents using an HP4145A Semiconductor Parameter Analyzer are shown for $V_{CC} = V_{PP} = 5V$.

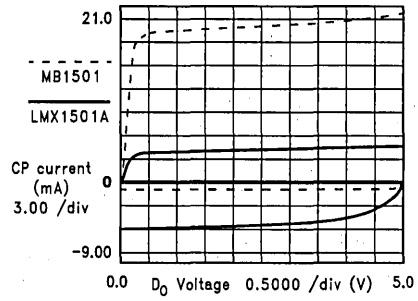

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FIGURE 6. Charge Pump Magnitude and Balance

Clearly, from the sample tested, the LMX1501A has better balance between the sink and source currents. The positive and negative lock times are therefore nearly equivalent, and the spurious energy is greatly reduced. Since the overall magnitude of the charge pump currents are markedly different, the PLL dynamics will change due to the change in the closed loop gain. In order to take full advantage of the superior performance of the LMX1501A charge pump, loop filter component values should be optimized corresponding to the LMX1501A phase detector gain. If an external charge pump implementation is used, no modification is necessary. ***Corrective Action:*** *Optimize component values for appropriate loop gain.*

Max voltage on the internal (D_O), and external (ϕ_r, ϕ_p) charge pump of the MB150X is 10V, and 6V for the LMX1501A. Although the bulk of applications, do not require VCO tuning voltages above 5V, certain systems use higher V_{CC}'s. The LMX1501A cannot attain voltages higher than 6V because of the N-channel breakdown voltage. For the charge pump of the LMX1501A to drive voltages greater than 6V one may use an active loop filter to provide the DC gain needed. Unfortunately, this is a redesign, and reduces the tuning sensitivity of the PLL. ***Corrective Action:*** *If Vp < 6V, No Action needed.*

SOFTWARE COMPATIBILITY

If the specifications for the MB150X for the data timing are met, the LMX1501A will also program correctly, since the programming protocol is identical. If t_{ES}, the clock to enable set-up time, equals 0 ns, then the LMX1501A will not program correctly, while the MB15XX will continue to function out of spec. The data input timing of the LMX1501A is more than fast enough to accept MB150X programming, since the specification for setup and hold times are ≥50 ns, and the MB150X specification calls for setup and hold times of ≥1 μs. ***Corrective Action:*** *Make sure Clock returns to a low state before the rising edge of Load Enable.*

ADDITIONAL NOTES

The major differences between the LMX1501AM and the MB150X that merit attention when replacing or dual sourcing have been discussed. Although the user may realize additional performance advantages from the LMX1501A, such as power dissipation, phase noise, lock time, and spurious performance, these are not discussed in depth, with the emphasis put on fundamental similarities and differences in the functional operation of the parts. With attention to the package size, loop filter, and programming, the LMX1501A will easily replace the MB150X series for many applications.

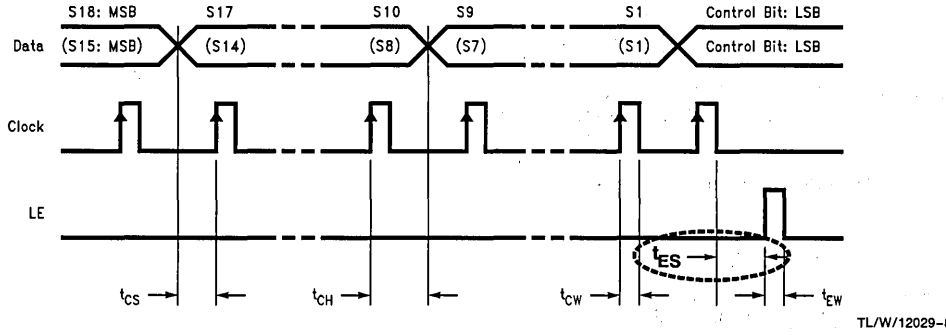

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FIGURE 7. Data Input Timing

Specification for the DECT ARi[1]™ Interface to the Radio Frequency Front End

National Semiconductor
Application Note 908

INTRODUCTION

This document will describe the I/O necessary to drive the National Semiconductor DECT radio frequency (RF) front end chip set. This is intended to help the system designer define the control signals for the RF front end, implemented as a direct modulation, single conversion receiver architecture. A single conversion transmitter and dual conversion receiver can be added with a second PLL and some other minor changes.

1.0 DECT SYSTEM OVERVIEW

1.1 I/O Requirements

The National Semiconductor solution for the DECT RF front end includes microwave circuits, frequency synthesizers, and pre-baseband functions (modems, DACs, RSSI, etc.). From the block diagram in *Figure 1,* it can be seen that the analog microwave circuits require only a power down signal, but that the digital circuits will require more control signals. The requirements for each part will be described in detail below.

1.2 The Front End Function

The Radio Frequency (RF) Front End serves as the air interface for the communication link. When transmitting, the user transmit data is shaped by the lowpass filter in the baseband processor (LMX2411). This shaped data is then transformed into a modulated waveform by modulating a Voltage Controlled Oscillator (VCO). This modulated signal is amplified to the proper output level by the power amplifier and output through a switch (or circulator), the roofing filter, and the antenna.

When receiving, the signal is input through the antenna, the switch (or circulator), and the roofing filter. The signal is amplified with the low noise amplifier and downconverted with the mixer (LMX2216B) to a fixed intermediate frequency. Channel changes are done by changing the local oscillator frequency driving the mixer with the frequency synthesizer (LMX2320). The intermediate frequency is then stripped of its information by a limiter/discriminator (LMX2240). Data values are then recovered from the signal (LMX2411) and sent to the burst mode controller. The received signal strength is also recovered (LMX2240) and filtered. The RSSI signal is digitized by an ADC on the burst mode controller or on the microprocessor.

To accomplish modulation of the VCO, the phase-locked loop that is used to set the channel frequency must be opened. This is done by powering down the LMX2320 PLL using the Power Down (PD) pin. When this is done, the charge pump output shifts to a TRI-STATE® mode, effectively preserving the loop voltage. The modulating signal is then added to the loop voltage by a resistive adder. The DECT TDMA/TDD bursts are short enough that with appropriate components and careful design, the discharge of the loop filter voltage (frequency accuracy) is within DECT specifications. Note that this method only requires a VCO to have a single tuning port.

A critical feature of open loop modulation is control over the VCO load. The receive power down signal turns the receive mixer on and off, changing its impedance. The LO switch transitions from this mixer to the power amplifier input. The power amplifier input impedance is a function of the power amplifier power down signal and of input power to it. The timing and sequence of these control signals will affect the VCO frequency error (jump) and should be carefully managed once the PA, switch, mixer, and VCO are chosen. See Section 2.5 for more details on open loop modulation.

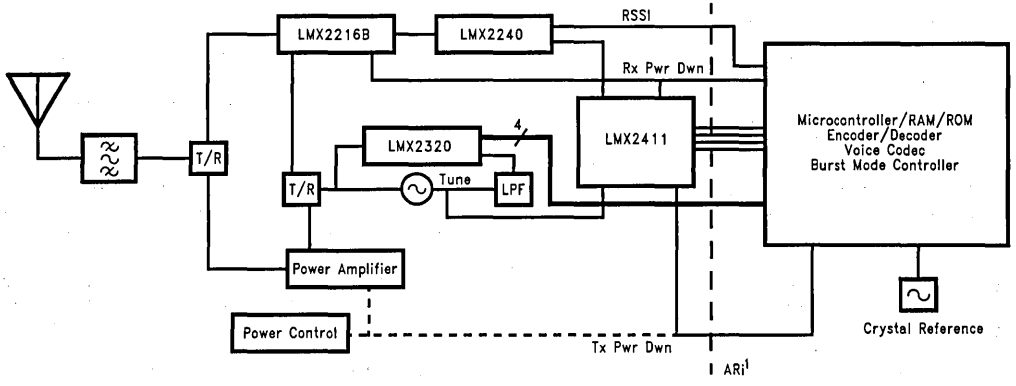

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FIGURE 1. Typical DECT RF Front-End Subsystem with ARi[1] Dividing Line Indicated

2.0 SYSTEM CONTROL SIGNAL REQUIREMENTS

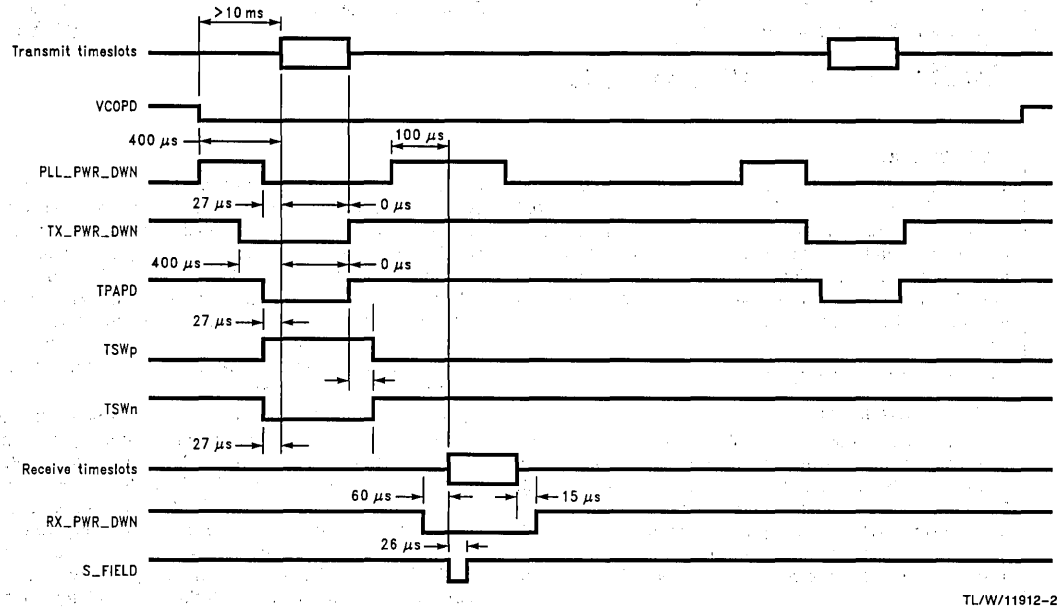

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FIGURE 2. A Typical Timing Diagram for the RF Front End Power Down Signals (during Active Locked Mode).

Symbol	Parameter	Time before Burst			Time after Burst			Unit
		Min	Typ	Max	Min	Typ	Max	
VCOPD	VCO Power Down	10						ms
PLL_PWR_DWN	PLL Power Down HIGH	30	150	400				µs
TPAPD	Power Amplifier Power Down	15	27	40	0			µs
TX_PWR_DWN	Transmit Section Power Down	30	50	240	0			µs
TSWp	T/R Switch Positive Signal	15	27	40		27		µs
TSWn	T/R Switch Negative Signal	15	27	40		27		µs
RX_PWR_DWN	Receiver Section Power Down		60			15		µs
S_FIELD	DC Compensation Circuit Enable		0					µs

In *Figure 2* above, the timing diagram for the overall front end power down signals is shown. Note that this is a typical case, and that in fact there are some signals that will vary in length. The table below shows the ranges of values for the various power down signals. In the table, the times are referenced to either the time required before a burst (timeslot) starts or the time required after a burst ends.

In the above table and in *Figure 2*, it can be noticed that the VCO is turned on and left on for the entire active locked period, while the PLL is powered down between bursts. The transmit and receive power down signals, as well as the switch signals (see Section 2.3), are toggled for each burst to conserve current. The numbers given in the table and *Figure 2* represent a typical DECT application. The power amplifier should be ramped both on and off in 27 µs each (DECT specification, Part 2: Physical Layer, Sections 5.2–5.3, *Figure 13*). The S_FIELD signal should be enabled at the start of the burst and last for 30 bits of the 32-bit preamble. This allows for some timing offsets in the burst mode logic. The transmit/receive switches need to be thrown at the same time or before the power amplifier begins its final power up, so their times are chosen to be the same before the burst, but they are delayed while the power amplifier turns off to avoid any more amplitude modulation of the signal than necessary and to correctly terminate the power amplifier. The phase locked loop and the transmit section must be turned on 400 µs before PLL_PWR_DWN goes LOW so that the loop compensates for the mid band voltage of the modulating signal. This is why they have two different power down signals offset in *Figure 2*. In transmit mode, the PLL must first settle to the transmit frequency and then be opened to allow modulation to take place. The transmit DAC's output should be at mid-range voltage prior to opening the loop to ensure that the loop centers on the correct frequency and then deviates equally to each side based on the modulation (see *Figure 3*). This is achieved by toggling Tx PD LOW (i.e., powering up the transmit portion) on the LMX2411 and holding Tx Data constant (either HIGH or LOW). The first edge on Tx Data will synchronize the LMX2411 to the transmit data and will also start transmission of the data through the digital filter.

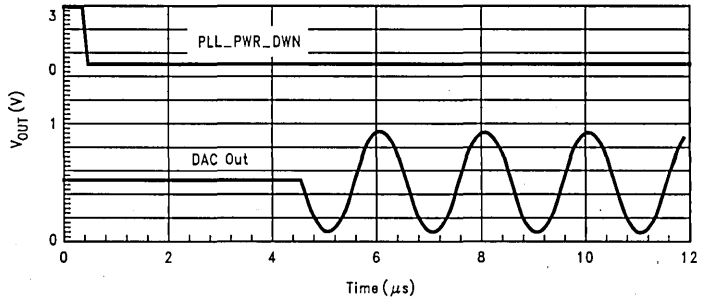

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FIGURE 3. Plot of PLL_PWR_DWN Signal and Modulator Output after TX_PWR_DWN is LOW

The receiver must be powered up 60 μs before a receive burst to allow the receive chain to fully power up and settle. Note that some standard products, such as the Sierra Semiconductor SC14400, have burst mode control signals that comply with the ARi[1]. The SC14400, for example, provides 9 pins for power down and load enable functions that are fully flexible with respect to timing. These signals can switch at any bit time, as long as only one is switched at a time. Also, two of these pins are higher in current to support the current required for PIN diode switches. A typical order of power down signals for one burst is the following:

Action:

1) Program PLL to the transmit frequency
2) Turn on PLL
3) Turn on Baseband Processor transmit section
4) Throw LO switch to "Transmit" position
5) After loop settles, open PLL
6) Throw RF output switch (if any) to "Transmit" position
7) Ramp on power amplifier
8) Transmit data
9) Ramp off power amplifier
10) Throw Transmit/Receive switches to "Receive" position
11) Turn off Baseband Processor transmit section
12) PAUSE
13) Program PLL to the receive frequency
14) Turn on PLL
15) Turn on receiver section
16) Receive data; generate S_FIELD signal for DC compensation
17) Turn off receiver section
18) Turn off PLL
19) Repeat steps 13) through 18) to monitor a second channel.

It is interesting to note that the unlocked output from the synthesizer is very low in noise. The user should consider using the unlocked LO during receive mode. This would result in a lower noise LO, but it could also result in more frequency drift. The drift specification in DECT is 13 kHz/ms. Presently, National Semiconductor has observed typical drift measurements of 55 kHz/second, or 55 Hz/ms.

2.1 The Receive Chain

The LMX2216B is the Low Noise Amplifier and Mixer, and the LMX2240 is the Intermediate Frequency Receiver. For DECT, these functions should be active only during receive mode. To accomplish this, the power down pin of either part should be driven low to activate the device and high to power it down. This polarity is chosen so that the user can simply ground the power down pin to permanently activate the part. The power down signal for each part should be the global receive power down (RX_PWR_DWN) signal for the entire receiver. This and all global power down signals should be CMOS power down signals unless noted otherwise. Using CMOS signals and CMOS power down switches on board each IC reduces power consumption and avoids the longer power up times that would be governed by decoupling capacitors on regulated supplies.

In addition to the power down signal, the analog output of the LMX2240's RSSI circuit should be sent to either the burst mode controller (e.g., Sierra SC14400) or to the microcontroller (e.g., Mitsubishi M37702) for digitization and peak hold by the ADC. Note that the microcontroller's ADC may not be fast enough to do the peak hold function digitally. In that case, an analog peak hold circuit must be added before the input to the microcontroller's ADC.

2.2 The Phase Locked Loop (PLL) Frequency Synthesizer

The LMX2320 is the 2.0 GHz frequency synthesizer. This part is provided with a power down pin as well as three pins to be used for serial programming of the desired center frequency and step size. The power down pin requires a separate control signal (PLL_PWR_DWN) because the synthesizer may be operating during both transmit and receive modes. The programming interface is a three wire MICROWIRE™-compatible interface with write-only capability. The Load Enable (LE) pin is active low. When the LE pin goes high, the loaded data is sent to the appropriate register in the synthesizer.

The timing for the LMX2320 is as follows. When the LE pin is low, the LMX2320 is ready for data from the channel controller (microprocessor or burst mode controller). On each rising edge of the clock, a serial bit is loaded from the data input. When LE goes high, the data is loaded into the prescaler and reference registers, and the channel is changed. The data cannot be shifted into the shift register until LE goes low.

The LMX2320 has two registers that need to be programmed. The Reference divider (R Counter) is a counter that divides the (crystal) reference frequency. It is programmed with a 14-bit word when the control bit is high, or "1". A fifteenth bit is used to set the programmable (128/129 or 64/65) prescaler. The frequency divider (N Counter) divides the input frequency and is programmed with a 18-bit word when the control bit is a low, or "0". The structure of the words is given on the following page.

To program the R Counter, the data should be the following (P = "1" for 64/65, P = "0" for 128/129):

P	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	C
d*	d	d	d	d	d	d	d	d	d	d	d	d	d	d	1

*d signifies a desired data bit, i.e., a "1" or a "0"

To program the N Counter, the data should be the following:

D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	C
d*	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	0

*d signifies a desired data bit, i.e., a "1" or a "0"

For DECT operation using a 10.368 MHz crystal and a reference, or step size, of 1.728 MHz,

R = 6

N = 1089 . . . 1098

P = 64

For further information, please consult the LMX2320 Data Sheet.

2.3 The Voltage Controlled Oscillator (VCO) and Transmit/Receive (T/R) Switches

The VCO power down signal will probably originate from the LP2951 regulator directly. When the regulator is powered up, the VCO will be powered up. This is due largely to the long turn on times for VCO's. The VCO's individual data sheets must be consulted for turn on time, as these may vary among manufacturers.

Up to two switch functions are required. The first is the signal control between the antenna and the Low Noise Amplifier (LNA) or power amplifier. A quarter wave length pin diode switch directs the RF signal to the LNA with low power dissipation. In transmit mode, current is passed through two PIN diodes to provide a low loss connection from the power amplifier to the antenna, and to isolate the LNA. Note that this switch can be replaced by a circulator.

The second switch controls the output of the VCO. This switch directs the VCO output to the receiver mixer or directly to the power amplifier input. *Figure 4* shows these functions below. Presently, two VCO manufacturers, ALPS and muRata, produce wideband VCOs which span the entire 130 MHz needed to achieve a single conversion receiver.

2.4 The Power Amplifier

The power amplifier requires a separate TPAPD signal for turning the PA on because of the power amplifier ramping required by DECT. (TX_PWR_DWN must turn on earlier to allow the PLL to lock to the correct frequency and not be offset by the mid band voltage of the LMX2411.) The power amplifier can be ramped with a single RC circuit or with a more complex raised cosine shaping. The technique used will depend on the power amplifier manufacturer's circuit. One circuit which has been used at National for GaAs power amplifiers is shown in *Figure 5*.

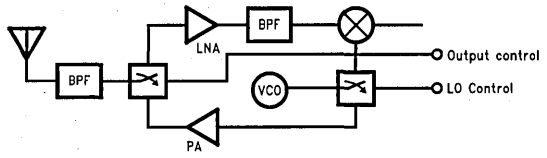

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FIGURE 4. Block Diagram of the Possible Switches Necessary in the RF Front End

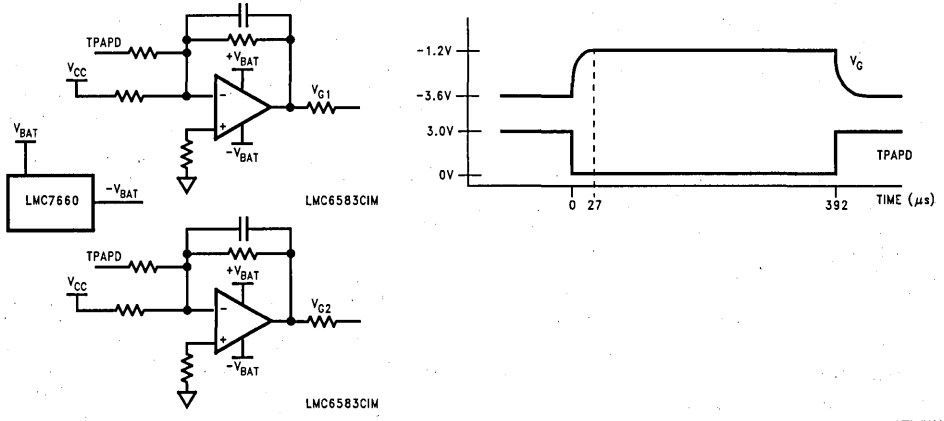

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FIGURE 5. The Circuit for the Power Amplifier Ramping Used by National Semiconductor and its Typical Performance

2.5 The Baseband Processor

2.5.1 General Functions

The LMX2411 is the baseband processor, or the interface between the RF front end and the digital back end. It functions in both the transmit mode and the receive mode, although only part of the chip is powered up at any given time. The LMX2411 has two power down pins, Tx PD and Rx PD, that should be driven with the appropriate global power down signal. This power down configuration reduces current consumption. In addition to the power down pins, the LMX2411 requires a Sys Clock and Tx Data input, a control signal input for its DC compensation circuit ($\overline{\text{S-Field}}$), and a Comp Out output line.

The Sys Clk input can be one of three system clocks commonly used in DECT: 10.368 MHz (9x), 13.824 MHz (12x), and 18.432 MHz (16x). This clock is used to clock the ROM filter and shift the Tx Data bits through the ROM addresses. Tx Data is the actual information data to be transmitted and is input from the burst mode controller. The control line that is needed for the DC compensation circuit, S_FIELD, also comes from the burst mode controller. This should only enable the DC compensation circuit during 30 bits of the DECT preamble to allow for 3 bits of timing inaccuracy. The DC compensation on the LMX2411 is an analog loop using a sample and hold circuit. The DC compensation method using the sample and hold circuit is intended to provide a fast RC averaging over a known sequence (DECT preamble). The analog method can be used without an S_FIELD signal, providing a long term average of the DC value through the use of a large capacitor on pin 2 of the LMX2411. However, this technique is not recommended due to its long start-up time and its sensitivity to long strings of 1's and 0's. Note that some burst mode controllers, in particular the Sierra SC14400, can support both this method and a digital DC compensation loop (see *DC Compensation*). The only output of the LMX2411 is the comparator output, which provides a CMOS level output ready for timing recovery to the digital back end.

2.5.2 Open Loop Modulation

Open loop modulation is a technique that allows for a relatively simple implementation as long as frequency pushing and load pulling effects can be controlled. The loop is opened by powering down the PLL, which in the LMX2320 results in a TRI-STATE at the charge pump output. For short bursts, the loop filter will not lose the charge, and the center frequency will not drift. *Figure 6* shows a sample circuit for modulating on an open loop. Note that the VCO requires only one tuning port for both locking and modulation. R_1 and R_2 will vary depending on which wideband VCO is used. The proper equation to be used in determining R_1 and R_2 is below:

$$V_{DAC} * \frac{R_2}{R_1 + R_2} * K_V = 576\,\text{kHz} \qquad (1)$$

In this case, K_V is the VCO sensitivity, expressed in MHz/V, and V_{DAC} is nominally 1V. Generally, R_1 will be on the order of 50 kΩ to 250 kΩ, and the ratio of R_1 to R_2 will vary from 30:1 to 50:1 for wideband VCOs, and will be smaller for narrowband VCOs. Also, the 576 kHz is the peak-to-peak frequency deviation for DECT, which means the peak frequency deviation is half of that, or 288 kHz.

It should be noted that the schematic in *Figure 6* contains a unity gain buffer op amp at the output of the PLL's loop filter. This op amp must have a low output impedance so as not to affect the voltage summing node for open loop modulation. This op amp will be necessary when using VCO's with high varactor leakage to prevent the varactor from discharging the loop capacitor and therefore causing frequency drift. This buffer should be powered up whenever the VCO is powered up, and so should be connected to the VCO's power down line. *Figure 7* shows a plot of typical frequency jump and drift that can be expected from open loop modulation when the load pulling and frequency pushing effects have been properly controlled.

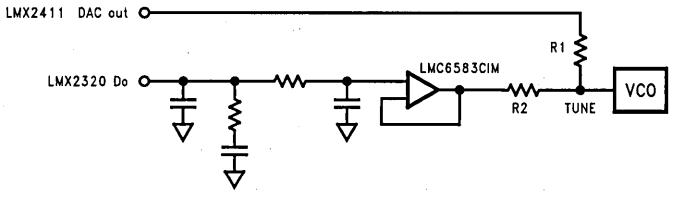

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FIGURE 6. Circuit Diagram for Direct, Open Loop Modulation

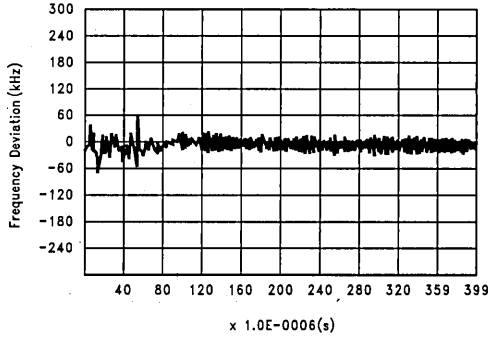

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FIGURE 7. Plot of Frequency Discriminator Output of Unmodulated Open Loop Carrier over a 400 μs Burst Showing the Loop Opening at 60 μs and the Resulting (Lack of) Drift. Units are kHz/μs.

Frequency pushing is controlled by putting a series 10Ω resistor and a shunt 1 μF to 4 μF capacitor on the VCO V_{CC} line from the LP2951 voltage regulator. Load pulling is controlled by using an attenuator and an RF buffer between the VCO and the power amplifier. The power amplifier and T/R switch both affect load pulling. RF coupling can also cause frequency drift, and this is controlled by providing good shielding between the power amplifier and the VCO.

2.5.3 DC Compensation

Compensation of the drift in DC of the demodulated eye due to frequency error, co-channel interference, or temperature effects can be implemented by using an analog "sample and hold" technique, or by using a digital duty cycle detection. In the analog method, the received, demodulated signal is input both to the comparator "+" input and to the sample-and-hold (S&H) buffer amplifier. The S&H buffer allows a single RC filter to average the DC value of the received signal without distorting it. This DC value is connected to the "−" input of the comparator. When the signal S_FIELD is used (named after the synchronization field in DECT), this circuit can acquire the DC voltage during the preamble and then hold it (with the external capacitor) for the duration of the burst. This solution avoids the problem of long strings of 1's and 0's that conventional continuous averaging circuits have while still reacting quickly to acquire the proper DC average at the beginning of a burst. This solution is provided internally to the LMX2411. *Figure 8* shows a typical response curve of the DC threshold level from initial startup. Note that the discharge of the capacitor is very low, which means that once the first burst acquisition has been done, all following bursts should be recovered with minimal CRC errors.

Another method of DC compensation is to monitor the duty cycle of the output of Comp Out, and adjust the level of an external threshold DAC that drives the LMX2411's comparator threshold directly. The digital method has the added advantage that the last value of the DAC can be pre-loaded for each timeslot, thus introducing memory into the system. The Sierra SC14400 supports both DC compensation methods.

2.6 Summary of ARi[1] Signals

The following is a summary of all thirteen (13) signals that are contained in the ARi[1] specification and their descriptions.

2.6.1 Tx Interface

2.6.1.1 TX_PWR_DWN

This signal is used to change the transmitter between power down and active modes. TX_PWR_DWN should go low 460 bits (400 μs) prior to start of transmission.

2.6.1.2 TPAPD

This signal is used for turning the power amplifier on and off. This signal should enable the power amplifier 31 bits (27 μs) prior to start of transmission.

2.6.1.3 TSWp/TSWn

These signals are used for the Tx/Rx switch at the antenna and/or VCO output. They are inverse signals of each other, and one or both may be used in a given implementation. In the case of TSWp, a "LOW" signal indicates the output of the VCO goes to the Rx mixer. A "HIGH" signal indicates the output of the VCO goes to the power amplifier. For TSWn, the polarity is reversed. This signal should switch approximately 30 bits (27 μs) before the start of either transmission or reception of the signal.

2.6.1.4 TX_DATA

Data to be transmitted. This is sent three bit times prior to start of transmission to account for three bit delay in the ROM filter. Also, three padding bits are added at the end of the burst to ensure the last desired bit is transmitted. The polarity of this signal determines reset state of LMX2411 ROM address. See the LMX2411 data sheet for more details.

2.6.1.5 SYS_CLK

This is the reference clock for both the LMX2411 and the LMX2320. It should have a frequency of either 10.368 MHz, 13.824 MHz, or 18.432 MHz and should be active anytime the transmitter or frequency synthesizer is active. This signal can be a CMOS signal or have a voltage swing with as little as 500 mV_{PP}.

2.6.2 Rx Interface

2.6.2.1 RX_PWR_DWN

This signal is used for the Rx to change between power down and active modes. RX_PWR_DWN should go LOW 70 bits (60 μs) prior to start of reception of the signal.

2.6.2.2 RSSI

This is the analog RSSI signal that originates from the LMX2240. This signal should be connected to an ADC that is either in the burst mode logic or the microcontroller.

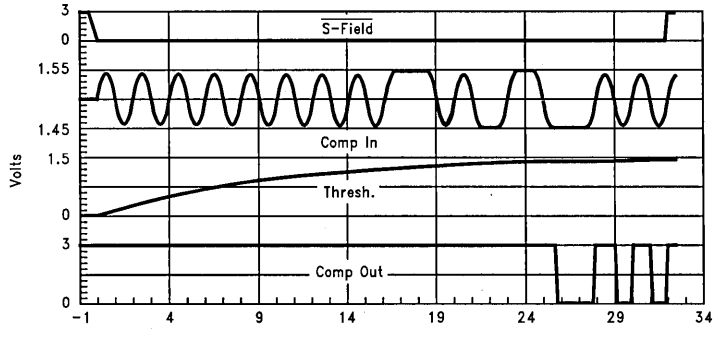

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FIGURE 8. Plot of DC Compensation Circuit Response vs Time from Full Discharge of Hold Capacitor

2.6.2.3 RX_DATA

Demodulated, received data for input to the burst mode controller. This is the output from the comparator.

2.6.2.4 S_FIELD

This signal is used to enable the analog DC compensation circuit on the LMX2411. This signal should go LOW 2 bits (2 μs) to 0 bits (0 μs) before the start of reception of the signal. This signal should go HIGH 32 bits (29 μs) to 30 bits (27 μs) later for an effective 30-bit averaging period for the sample and hold circuit.

2.6.3 Synthesizer Interface

2.6.3.1 PLL_PWR_DWN

This signal changes the phase-locked loop (PLL) frequency synthesizer between power down and active modes. PLL_PWR_DWN should go HIGH between 115 bits (100 μs) and 461 bits (400 μs) before the PLL will be locked. **Note that this results in a blind slot implementation for DECT.** PLL_PWR_DWN should go LOW 31 bits (27 us) before the start of a transmission to unlock the PLL. **NOTE: THE LMX2320 PLL CAN BE PROGRAMMED IN THE POWER DOWN STATE.**

2.6.3.2 ENABLE

Enable signal for the LMX2320 programming interface.

2.6.3.3 DATA

Data line for the LMX2320 programming interface.

2.6.3.4 CLOCK

Clock line for the LMX2320 programming interface.

2.6.4 System Signals

2.6.4.1 VCO_PD

May be used as a system PD as well by connecting to an LP2951 (or equivalent) voltage regulator output. To power down the VCO, the regulator would be turned off, which would also turn off the entire RF front end.

2.6.4.2 V_{BAT}

The battery voltage that presumably will come from 3 NiCad battery cells or their equivalents. This is the power supply that is regulated on board the RF front end. All ICs are driven by this except the power amplifier, which operates directly from the battery. This signal should be connected directly to the battery with short lead lengths to minimize losses during times when the power amplifier is on and also to avoid lead inductances which cause variations in V_{CC} and V_{BAT}.

2.6.4.3 GND

This is the return path to the battery.

3.0 ELECTRICAL SPECIFICATIONS

The RF front end runs on a single +3V supply. The table below gives the pertinent electrical specifications to interface to the RF front end's CMOS circuitry.

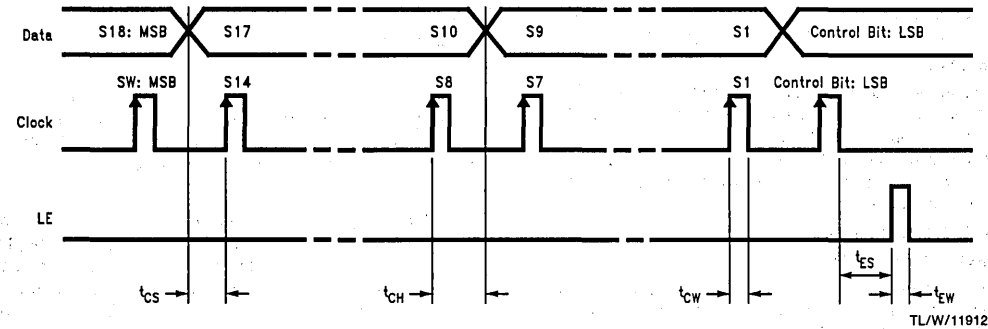
ELECTRICAL CHARACTERISTICS

(The following specifications apply for supply voltage V_{CC} = +3V ±5% V unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INTERFACE SECTION						
V_{OH}	High-Level Output Voltage	I_{OH} = −1.0 mA	V_{CC} −0.4			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1.0 mA			0.4	V
V_{IH}	High-Level Input Voltage		V_{CC} − 0.8			V
V_{IL}	Low-Level Input Voltage				0.8	V
I_{IN}	Input Current	GND < V_{IN} < V_{CC}	−1.0		1.0	μA
t_{CS}	Data to Clock Setup Time	See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	0			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
t_{ES}	Clock to Enable Setup Time	See Data Input Timing	50			ns
t_{EW}	Enable Pulse Width	See Data Input Timing	50			ns

Note 1: DC Electrical Characteristics for the digital section apply to all digital input and output pins. This includes Clock, Data, LE, PD, Tx Data, Tx PD, Rx PD, Comp Out and S-Field.

SERIAL DATA INPUT TIMING



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NOTES: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.

Introduction to Single Chip Microwave PLLs

National Semiconductor
Application Note 885
Cynthia L. Barker
Wireless Communications

ABSTRACT

Synthesizer and Phase Locked Loop (PLL) figures of merit including phase noise, spurious output and lock time, at microwave frequencies, are examined. Measurement methods for these parameters and supporting software are discussed in detail. The requirements for the loop filter, the charge pump, the dual modulus prescaler and their effects on PLL performance are analyzed.

INTRODUCTION

Phase Locked Loops are used for many radio applications including frequency synthesizers, carrier recovery and clock recovery circuits, tunable filters, frequency multipliers, receiver demodulators and modulators. This application note will concentrate on the use of a PLL as a frequency synthesizer, as shown in *Figure 1.*

There are two main reasons for using a PLL as a frequency synthesizer. One is to translate the frequency accuracy of a high quality signal source to a tunable signal source. The second is to translate the noise characteristics of a high quality signal source to a lower quality signal source. The block diagram of a basic PLL is shown in *Figure 1.* The high quality signal source, in this case, is a crystal reference.

A single chip PLL consists of the reference divider, the main divider (including a dual modulus prescaler), the phase detector and a charge pump.

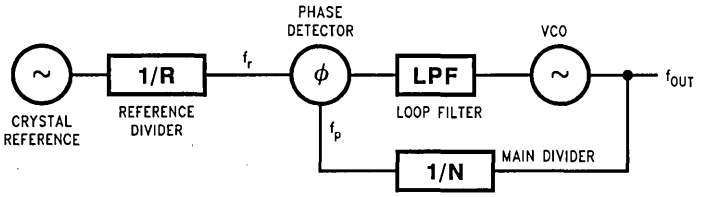

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FIGURE 1. Block Diagram of a Basic Phase Locked Loop

SYNTHESIZER AND PLL FIGURES OF MERIT

Phase noise is a measure of the spectral purity of the tone produced by the PLL. It is dependent on the noise characteristics of the crystal oscillator reference and the VCO as well as some noise contribution of the dividers. Phase noise is defined as the ratio of the single sideband power (within a 1 Hz bandwidth at some offset frequency) to the total carrier power. Phase noise is often measured in units of dBc/Hz.

Spurious output is a measure of the level of the reference spurs (sometimes referred to as reference sidebands) on the output tone. The reference spurs appear on the output tone at the center frequency ± the reference frequency and at integer multiples of the reference frequency. For example, a PLL operating at 836 MHz with a reference frequency of 25 kHz will have reference spurs at 836.025 MHz, 835.075 MHz, 836.050 MHz, 835.050 MHz, etc.

Lock time or switching speed is a measure of the settling time of the PLL once a change in frequency has been initiated. The frequency step and the frequency accuracy to define "locked" must both be defined for this measurement to be useful.

PHASE NOISE MEASUREMENT METHODS

The phase noise characteristics of the PLL can be measured on a spectrum analyzer or using a phase noise test set. The spectrum analyzer test technique is described here. Phase noise is measured in units of dBc/Hz. This is done at several offsets from the output signal such as 1 kHz, 10 kHz and 100 kHz. The spectrum analyzer is tuned to the desired center frequency and the span is adjusted so the appropriate offset frequency can be viewed. The difference between the level of the carrier and the noise level minus 10 [log (resolution bandwidth)] is equal to the phase noise in dBc/Hz. The resolution bandwidth is read directly from the spectrum analyzer. The phase noise result in dBc/Hz is a negative number. Since phase noise is measured in dBc/Hz the measurement is always normalized to a 1 Hz bandwidth. The video averaging feature of the analyzer is used to better determine the noise level. An example of such a measurement, for the LMX1501A PLL using a reference frequency of 25 kHz, is shown in *Figure 2.* Refer to the LMX1501A data sheet for application circuits.

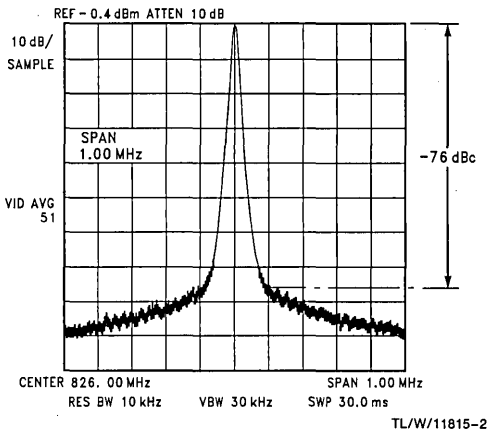

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FIGURE 2. An 826 MHz Synthesizer Phase Noise Measurement @ 100 kHz = −116 dBc/Hz. Using the LMX1501A PLL.

Example Phase Noise Calculation

phase noise

(@100 kHz) = −76 dBc −10 • log(res.BW)

= −76 dBc − 10 • log (10 kHz)

= (−76 − 10 • 4) dBc/Hz

= −116 dBc/Hz

REFERENCE SIDEBAND MEASUREMENT METHODS

The reference sidebands can be seen on a spectrum analyzer and are measured in dBc. The analyzer is set to the desired center frequency and the span is set to allow the reference sidebands to be viewed. For example, to see the reference spurs for a 1.7 MHz reference frequency the span would be set to 10 MHz. The spurious output is the difference between the level of the PLL tone (at the center frequency) and the level of the reference spur (at the center frequency ± the reference frequency). In *Figure 3,* the reference sidebands for a 1.7 MHz reference frequency are about 78 dB down from the PLL tone, or −78 dBc. Refer to the LMX2320 data sheet for application circuits.

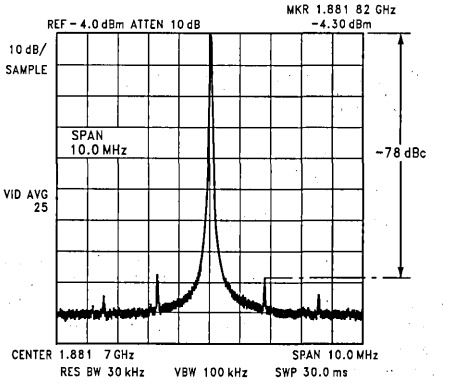

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FIGURE 3. An 1881 MHz Synthesizer with a Reference Frequency of 1.7 MHz and Sidebands @ 1.7 MHz = −78 dBc. Using the LMX2320 PLL.

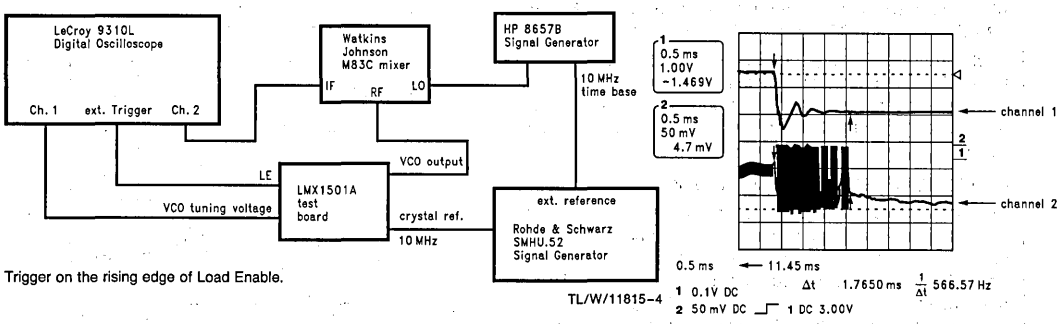
SWITCHING SPEED MEASUREMENT METHODS

Switching speed is measured on an oscilloscope by probing the VCO tuning voltage. The transient response will be seen directly. This method shows the damping characteristics of the loop but does not provide the accuracy of the frequency match.

Figure 4 illustrates an evaluation method using a mixer to determine the accuracy of the frequency match. The signal generator is phase locked to the crystal reference input to the PLL. This is accomplished by using a signal generator for the crystal reference and having the 10 MHz reference used as an external reference for the other signal generator. The output of the VCO is mixed with a signal (from a signal generator) at the desired frequency (using the mixer as a phase detector). When the frequencies are matched a DC voltage appears at the output of the mixer. When the frequencies are mismatched a beat note appears at the output of the mixer. Either of these signals is viewed on a scope. The peak to peak amplitude of the beat note represents a phase offset of ±180°. The slope of the beat note represents a change in phase divided by time, which is equivalent to frequency. This frequency represents the frequency mismatch. As the slope of the line approaches zero the frequencies converge, and the loop locks. This method gives a frequency accuracy within 100 Hz.

An example of the above two types of switching speed measurements is shown in *Figure 4.* Channel 1 shows the VCO tuning voltage and channel 2 shows the output of the mixer IF port.

A third method uses a spectrum analyzer to view the transient response by setting the frequency span to 0 Hz. The display is effectively now frequency versus time. The video band width should be set on maximum. The frequency offset will be equal to the resolution bandwidth setting at 10 dB down from the top on the vertical axis. This is due to the filter characteristics of the analyzer. To be fully accurate the external trigger of the analyzer should be triggered off the loading of the new frequency. This method is not recommended for measuring lock times under 10 milliseconds because on some spectrum analyzers the display response time of the analyzer is longer than a few milliseconds and erroneous data can result. A modulation domain analyzer can also be used to measure switching speed. It displays frequency versus time directly but it is not available in all labs.



Trigger on the rising edge of Load Enable.

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FIGURE 4. Test Setup and Lock Time for 10 MHz Step = 1.77 ms using a LMX1501A with a Reference Frequency of 25 kHz.

SUPPORTING SOFTWARE

A software program of some kind is needed in order to program the PLL chip to test it. National Semiconductors LMX series of PLL chips are programmed via a three line MICROWIRE™ serial interface (clock, data, load enable). National Semiconductor Corporation provides a DOS program to allow the user to program the chip from the parallel port of a DOS personal computer. The user enters the frequency of operation, the reference frequency and the crystal frequency then presses one key to load in the appropriate divider values. The frequency can be tuned in steps of the reference frequency and a switching mode is available to test the lock time. The user enters the number of steps and the PLL will switch between the two frequencies. The user interface for the program is function key driven. Detailed operating instructions are provided with the software. For more information on the PLL software program contact:

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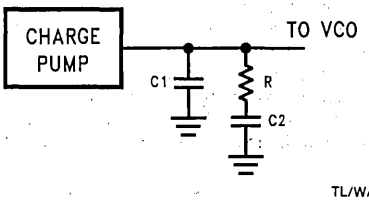
LOOP FILTER

The design of the loop filter involves a trade off between reference sidebands and switching speed. The loop filter must be designed for the correct balance between reference spurs and lock time that the system requires. Generally, the narrower the loop bandwidth the lower the reference spurs but the longer the lock time. The circuit in *Figure 5* shows a type 2 third order passive loop filter configuration and its transfer function.



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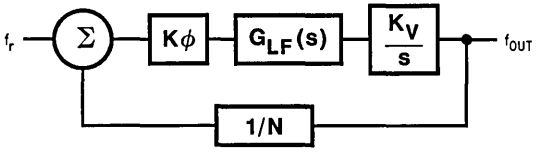
$$G_{LF}(s) = \frac{R \bullet C2 \bullet s + 1}{s\,(C2 + C1\,(R \bullet C2 \bullet s + 1))}$$

FIGURE 5. Passive Loop Filter Circuit and Loop Filter Transfer Function.

A type 2 loop has two integrators within the loop, a VCO and an integrator/filter. The order of the loop is determined by number of poles of the transfer function. Using the phase detector and VCO constants (K_ϕ and K_V) and the loop filter transfer function (G_{LF}) the open loop Bode plot can be calculated. K_ϕ and K_V are available from the PLL IC and VCO manufacturers. The control circuit, the open loop transfer function and the open loop Bode plot are shown in *Figure 6.* The loop bandwidth is shown on the Bode plot as (ω_p) the point of unity gain.

Control Circuit



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(G = Forward transfer function, H = Feed back)

Open Loop Transfer Equation

$$GH(s) = \frac{K_\phi\, G_{LF}(s)\, K_V}{Ns}$$

Open Loop Response Bode Plot

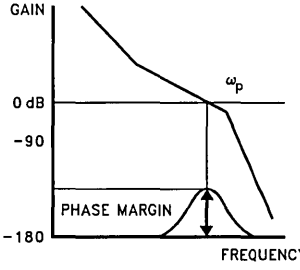

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FIGURE 6. Control Circuit, Open Loop Equation and Bode Plot

CHARGE PUMP AND PHASE DETECTOR

A current charge pump and a phase frequency detector are implemented in National Semiconductor's LMX series of PLL chips. To increase the VCO frequency the charge pump outputs a pump up (source) current. To decrease the VCO frequency the charge pump outputs a pump down (sink) current. This current pulse charges the voltage of the capacitor C1. The charge pump is capable of supplying a controlled charge to the loop filter over a wide range of voltages, as shown in *Figure 7.*

The phase detector and charge pump are difficult to characterize separately. The figures of merit for the combination include linearity, sensitivity and deadband range. The linearity of the charge produced by the charge pump with respect to the detected phase error is critical to providing low spurious and low phase noise. The sensitivity (K_ϕ) is measured in mA/radian and depends on the charge pump current capability. Current mode charge pumps commonly have a dead zone where the gain changes dramatically for a very small phase error. The divider outputs fr and fp are a series of pulses whose relative timing reflect the phase or frequency error, as shown in *Figure 8.* At some point the pulses are too close together for the phase frequency detector to distinguish them. This is the deadband or dead zone, as shown in *Figure 9.* The LMX series of PLLs use a proprietary feedback method to minimize deadband.

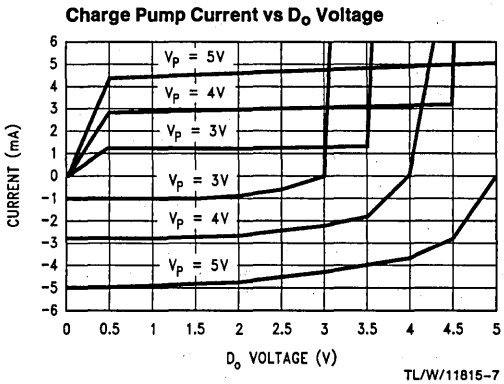

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FIGURE 7. Charge Pump Current vs Voltage for the LMX Series of PLL Chips

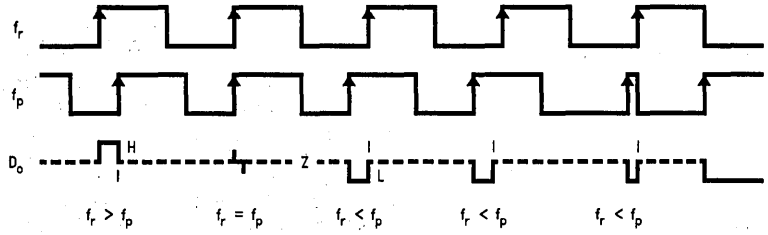

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FIGURE 8. Phase/Frequency Error Pulses

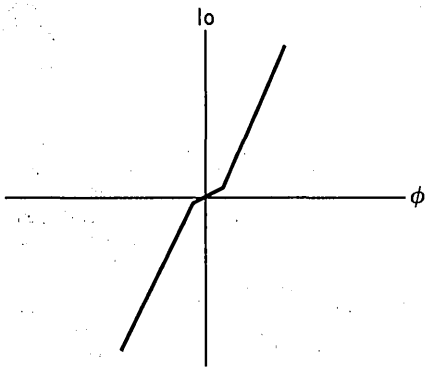

FIGURE 9. Charge Pump Current vs. Phase Error, showing Deadband.

DUAL MODULUS PRESCALER

Dual modulus prescalers allow operation of the divider chain at high frequencies while most of the divider operates at a lower frequency. However, this capability sets limits on the range of the divider. The divider is made up of an A counter and a B counter. The A counter is the swallow counter and the B counter is the programmable divider. The condition for a legal divide ratio is that B ≥ A.

The necessary divide number (N) is calculated by dividing the desired frequency by the reference frequency.

$$f_{out} = Nf_{ref} = \frac{N}{R} f_{crystal}$$

$$R = \text{reference divide ratio} = \frac{\text{crystal frequency}}{f_{ref}}$$

The output frequency must be an integer multiple of the reference frequency. Once the divide ratio is calculated a check can be made to determine whether it is above the minimum continuous divide ratio. The minimum continuous divide ratio is equal to P(P−1) where P is the prescaler divider. For example the minimum divide ratio for a 64/65 prescaler is 64(64−1) or 4032. If the divide ratio required (N) is below the minimum continuous divide ratio it may be a legal number but it must be verified that B ≥ A. The values for A and B can be calculated from the following equations:

$$B = N \text{ div } P$$

$$A = N \bmod P$$

A divide ratio that is above the minimum continuous divide ratio or satisfies the condition B ≥ A is a legal divide number. The PLL will not operate if it is programmed with an illegal divide number. For example, in choosing a prescaler for a DECT (Digital European Cordless Telephony) system the required divide ratios for the transmit side would be 1089 to 1098. The frequencies of operation for DECT are 1881.792MHz to 1897.344 MHz with a channel spacing of 1.728 MHz. The reference frequency used is 1.728 MHz.

$$\frac{1881.792}{1.728} = 1089 \quad \text{and} \quad \frac{1897.344}{1.728} = 1098$$

The minimum continuous divide ratio for a 64/65 prescaler is 64(64−1) or 4032. The minimum continuous divide ratio for a 128/129 prescaler is 128(128−1) or 16,256. For DECT the divide ratios required do not exceed the minimum continuous divide ratio for a 64/65 or 128/129 prescaler. Therefore, it must be verified that the condition of B ≥ A holds true. This is determined as follows:

TABLE I. Example Dual Modulus Prescaler Calculation

N	64/65		128/129	
	B	A	B	A
1089	17	1	8	65
1090	17	2	8	66
-	-	-	-	-
-	-	-	-	-
-	-	-	-	-
1097	17	9	8	73
1098	17	10	8	74

For the 64/65 prescaler, Table 1 shows B ≥ A therefore it can be used. The 128/129 prescaler cannot be used since A > B. The above calculation demonstrates that a 64/65 prescaler can be used in the DECT system for the transmit PLL.

CONCLUSION

The performance of a PLL as a frequency synthesizer is measured in terms of phase noise, spurious output and lock time. The techniques for measuring these parameters have been discussed. The loop filter, charge pump/phase detector and dual modulus prescaler and their impact on PLL performance have been analyzed. Example performance metrics were demonstrated for National Semiconductor's LMX series of PLL chips. These ICs provide the capability to produce a low power, low noise, low spurious and fast switching frequency synthesizer. With a properly designed loop filter excellent performance can be achieved. The LMX series of PLL chips provide the building block around which a high performance frequency synthesizer can be designed.

References

W.F. Egan: *Frequency Synthesizers By Phase Lock*, John Wiley and Sons, 1981

F.M. Gardner: *Phaselock Techniques, Wiley, 1989*

F.M. Gardner: *"Charge-Pump Phase-Lock Loops"*, IEEE Transactions on Communications, Com-28, No. 11, November 1980

U.L. Rohde: *Digital PLL Frequency Synthesizers: Theory and Design*, Prentice Hall, 1983

Integrated LNA and Mixer Basics

National Semiconductor
Application Note 884
A. Dao

ABSTRACT

Basic theory and operation of low noise amplifiers and mixers are presented. Important figures of merits of these two devices such as gain, noise figure, compression point, and third order intercept point are introduced and derived. Measurement methods of these figures of merit are also described.

LNA

Low noise amplifiers (LNAs) are widely used in wireless communications. They can be found in almost all RF and microwave receivers in commercial applications such as cordless telephones, cellular phones, wireless local area networks, and satellite uplinks and downlinks and in military applications such as doppler radars and signal interceptors. Depending upon the system in which they are used, low noise amplifiers can adopt many design topologies and structures—those used in military applications tend to be discrete, large in size, and consume high power, whereas those in commercial applications aim toward high integration and low voltage and bias currents. The LMX2215 and LMX2216B, for example, can be classified into the latter catergory. LNAs are usually placed at the front-end of a receiver system, immediately following the antenna. A band pass filter may be required in front of it if there are many adjacent interfering bands leaking through the antenna, but this filter generally degrades the noise performance of the system. The purpose of an LNA is to boost the desired signal power while adding as little noise and distortion as possible so that retrieval of this signal is possible in the later stages in the system. With this in mind, low noise amplifier designers have developed many design concepts and theories applied to low noise amplifiers and important figures of merit used to characterize and compare their performance. These concepts and figures of merit are discussed in the following sections.

MIXER

Mixers are found in virtually all wireless communication systems. They are frequency translating devices that convert input signals from one frequency to another by mixing these signals with another signal of known frequency. One reason frequency translation is a necessary process in wireless transmission is that information signals such as human speech or digital data are usually low frequency signals and are not suitable for a wireless channel. Another is that wireless channels are common channels that are shared by many signals and these signals must be separated into different frequency bins so that electronic circuits (which contain frequency selective components) can keep them from destructively interfering with each other. Among many other properties, frequency is one that is most easily exploited in signal identification.

Mixers can be classified into two broad categories: passive or active. The most commonly available and used are passive diode mixers since they are easier to design and more thoroughly understood. Active mixers, on the other hand, involve transistors and the most popular ones are built from the basic Gilbert cell structure. Some higher frequency active mixers exploit the nonlinear characteristics of high gain transistors and can perform the mixing action using only one transistor. Among these types, the Gilbert cell structure has the most desirable characteristics in terms of isolation and harmonic suppression due to its balanced structure. The LMX2215, LMX2216B, and LMX2213B use the Gilbert cell (the LMX2216B is the 3V equivalent of the LMX2215, and the LMX2213B is the LMX2216B without the LNA).

Most down converting mixers are three-port devices, as shown in *Figure 1.* They take two input signals: the RF and the LO (local oscillator) signals. The output is a mixing product of these two inputs and is an intermediate frequency (IF) signal. There are self-oscillating mixers which provide their own LO signal by having an internal resonating element coupled with the RF input. The LMX2215 and LMX2216B require external LO drives.

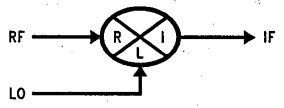

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FIGURE 1. Three-Port Mixer

Mixers perform the mixing operation by multiplying the two input signals. The output, IF, is the product of the two signals RF and LO, and it contains the sum and difference of the two input frequencies. In receivers, the lower frequency component is usually the desired one and can be obtained by lowpass filtering the mixer output signal. Derivations of the mixer effect are shown below in the section on nonlinearities (OIP_3).

CONCEPTS

Noise

Noise in electrical systems is defined as random fluctuations in voltage and current. It can be generated internally by components employed in the system or externally by electrical radiation from other systems or induced mechanical vibrations. RF and microwave oscillators, for example, are very susceptible to external radiation if they are not properly shielded. They are also susceptible to mechanical vibrations, a phenomenon called microphonics, if they are not sufficiently isolated from physical contact with nearby objects. Integrated low noise amplifiers are, on the other hand, most vulnerable to noise that is generated by their own transistors and resistors. Transistors exhibit flicker noise, which is caused by a change in conductance caused by a relatively slow process (e.g. the exchange of charge with surface traps or metallic impurities through tunneling), and shot noise, which is due to random one-way crossings of some barrier by discrete quantities of charge. For amplifiers at radio and microwave frequencies, flicker noise is negligible since it's power spectrum has a 1/f property. The

power spectral density of flicker noise is described by equation (1) below:

$$G_i(f) = C_1 \frac{I^a}{f^b} \quad (1)$$

where a ~ 1 to 2, b ~ 1, and C_1 is a device dependent constant. Shot noise power, however, depends on the net total current crossing the pn junctions, and its power spectral density is given by

$$G_i(f) = qI \quad (2)$$

where q is the electronic charge and I is the total current. Resistors exhibit thermal noise, which is generated by the random movement of electrons inside the resistive material at a non zero absolute temperature. The thermal noise power (per unit of frequency) of resistors, thus, depends on temperature and the resistance value of the resistors. However, the available thermal noise power depends solely on temperature. Equation (3) gives the power spectral density of thermal noise

$$G_v(f) = KTR \quad (3)$$

where K is the Boltzmann's constant, T is the absolute temperature in Kelvins, and R is the resistance.

The combined effect from the noise sources mentioned above and all other possible noise sources is often treated as though it were caused by only thermal noise. Moreover, LNAs are sometimes specified, not by their noise figure, but by their noise temperature, the temperature at which a resistor would generate the equivalent noise power.

Noise Figure (NF)

Noise figure is noise factor in decibel units (dB) and is an important figure of merit used to characterize the performance of not only a single component but also the entire system. It is one of the factors which determine the system sensitivity. Noise factor is defined as the input signal to noise ratio divided by the output signal to noise ratio. For an amplifier, it can also be interpreted as the amount of noise introduced by the amplifier seen at the output besides that which is caused by the noise of the input signal. Mathematically,

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{G_a S_i/(N_a + G_a N_i)} = \frac{N_a + G_a N_i}{G_a N_i} \quad (4)$$

$$NF = 10 \log (F) \quad (5)$$

where S_i, and N_i, represent the signal and noise power levels available at the input to the amplifier, S_o and N_0 the signal and noise power levels available at the output, G_a the available gain, and N_a the noise added by the amplifier. For a mixer which is used in applications where the desired signal power is contained in only one sideband, N_i is interpreted as the input noise contained in only one sideband. Therefore, in specifying noise figure for mixers, the term single-sideband or double-sideband must be noted to indicate how N_i was measured. In most communication receivers, single-sideband noise figure is the "true" noise figure and is 3 dB higher than double-sideband noise figure.

Design for Optimum Noise Performance

Based on the above equations, noise models for transistors can be developed. Furthermore, analysis of these models shows that for an amplifier using bipolar transistors, the only noise determining factor is the input match (which can also be translated into a bias current dependence). If resistors are also employed in the matching networks, then these will affect the noise performance as well. For each transistor operating at a particular frequency and bias current, there exists an optimum input match $\Gamma_{opt} = R_{opt} + jX_{opt}$ (6), which will yield an optimum noise figure F_{opt} This input match can be obtained by measurements using a noise figure meter and a vector network analyzer. A matching network designed to present this optimum impedance at the input of the transistor yields the optimum noise performance. The noise figure of the resulting amplifier can be calculated using the following formula,

$$F = F_{opt} + \frac{4R_n}{Z_0} \frac{|\Gamma_s - \Gamma_{opt}|^2}{|1 + \Gamma_{opt}|^2 (1 - |\Gamma_s|^2)} \quad (7)$$

where R_n = noise resistance

Z_0 = system impedance

Γ_s = input reflection coefficient seen by the device (see *Figure 1*).

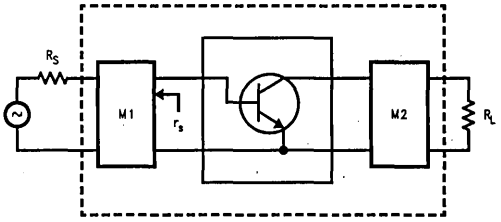

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FIGURE 2. Typical LNA Topology

Note that if the input match is perfect, the noise figure is F_{opt}. This value is usually not achievable in practice and tradeoffs between noise performance, match to available filters, gain, and stability is often required.

Noise Figure Measurements

Noise figure can be measured using a noise figure meter, which consists of a noise source and an RF receiver. The noise source is placed at the input of the device under test (DUT), and the output of the DUT is connected to the receiver (see *Figure 3*). There are several methods which noise figure receivers use to calculate noise figure, one of which involves computing the Y factor. With this method, the noise source (an avalanche diode) is cycled between two effective noise temperatures: T_h and T_c, shown in *Figure 4.* T_h corresponds to the hot temperature, when the diode is bias with a DC current, and T_c corresponds to the cold temperature, when the diode is off. The receiver detects the noise power at the output of the DUT under these two temperatures and computes the straight-line noise characteristics, from which the noise added, N_a, can be determined. Along with N_a, the noise figure meter also measures the available gain of the DUT to compute the noise figure using equations (4) and (5). *Figures 3* and *4* below illustrate the measurement setup and the straight-line noise characteristic.

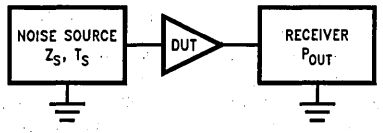

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FIGURE 3. Noise Figure Measurement Setup

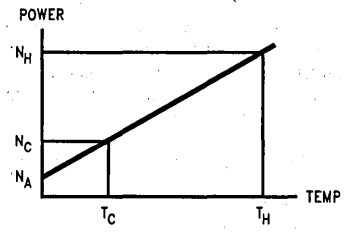

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FIGURE 4. Noise Power vs Noise Source Temperature

GAIN (G)

At radio and microwave frequencies, efficiency in transmission of signal power is of great importance. For this reason, RF and microwave circuits are optimized for power gain instead of voltage or current gain as commonly found in most low frequency circuits. The unit of power used to specify absolute power level is the dBm, or decibels referenced to 1 mW. Power levels in dBm can be computed from the equation

$$P(dBm) = 10 \log \left(\frac{P(mW)}{1\ mW} \right) \quad (8)$$

In cases where the load impedance is known or assumed, equivalent voltage levels can be used to specify power levels indirectly. In these cases, the unit dBμV is often used. A similar equation converts μV units to dBμV units.

$$V(dB\mu V) = 20 \log \left(\frac{V(\mu V)}{1\ \mu V} \right) \quad (9)$$

The importance of power transfer is one of the reasons for which power gain, and not voltage or current gain, is often used to specify RF and microwave devices. Many different types of power gain are used in RF engineering. The type used here is called transducer gain, which is defined as the ratio of the power delivered to the load to the available power from the source,

$$G = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2/R_L}{V_{in}^2/4R_s} = 4\frac{R_s}{R_L}\frac{V_{out}^2}{V_{in}^2} \quad (10)$$

where V_{out} is the voltage across the load R_L, and V_{in} is the generator voltage with internal resistance R_s. In terms of scattering parameters, transducer gain is defined as

$$G = 20 \log (|S_{21}|) \quad (11)$$

where S_{21} is the forward transmission parameter, which can be measured using a network analyzer.

1 dB COMPRESSION POINT (P_{1dB})

A measure of amplitude linearity, 1 dB compression point is the point at which the actual gain is 1 dB below the ideal linear gain. For a memoryless two-port network with weak nonlinearity, the output can be represented by a power series of the input as

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \ldots \quad (12)$$

For a sinusoidal input,

$$v_i = A \cos \omega_1 t \quad (13)$$

the output is

$$v_0 = \frac{1}{2} k_2 A^2 + \left(k_1 A + \frac{3}{4} k_3 A^3 \right) \cos \omega_1 t + \frac{1}{2} k_2 A^2 \cos 2\omega_1 t + \frac{1}{4} k_3 A^3 \cos 3\omega_1 t \quad (14)$$

assuming that all of the fourth and higher order terms are negligible. For an amplifier, the fundamental component is the desired output, and it can be rewritten as

$$k_1 A \left[1 + \frac{3}{4} (k_3/k_1) A^2 \right] \quad (15)$$

This fundamental component is larger than k_1 A (the ideally linear gain) if $k_3 > 0$ and smaller if $k_3 < 0$. For most practical devices, $k_3 < 0$, and the gain compresses as the amplitude A of the input signal gets larger. The 1 dB compression point can be expressed in terms of either the input power or the output power. Measurement of P_{1dB} can be made by increasing the input power while observing the output power until the gain is compressed by 1 dB.

P_{1dB} is an important characteristic of a device since it indicates the upper limit of the power level of the input signal without saturating the device and generating nonlinear effects.

THIRD ORDER INTERCEPT (OIP_3)

Third order intercept is another figure of merit used to characterize the linearity of a two-port. It is defined as the point at which the third order intermodulation product equals the ideal linear, uncompressed, output. Unlike the P_{1dB}, OIP_3 involves two input signals. However, it can be shown mathematically (similar derivation as above) that the two are closely related and $OIP_3 \approx P_{1dB} + 10$ dB. Theses two figures of merit are illustrated in *Figure 5* below.

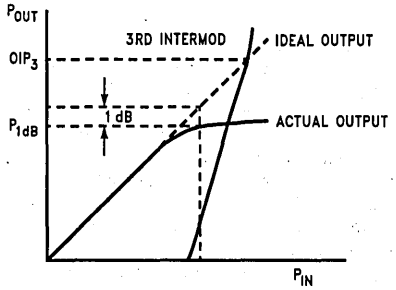

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FIGURE 5. Typical P_{out}–P_{in} Characteristics

Third order intermodulation products are important since their frequencies are located close to the wanted signal frequency, making them more difficult to be rejected by practical filters. If the two-port network is an LNA used in a receiver, intermodulation products at the output of the LNA can mask out signals from adjacent channels. For example, the third order intermodulation products resulted from 2 channels at 1 MHz apart, f1 = 408 MHz and f2 = 409 MHz, will be at 407 MHz and 410 MHz, a 1 MHz offset from f1 and f2. Similarly, two channels f4 = 411 MHz and f5 = 412 MHz will produce intermodulation products at 410 MHz and 413 MHz. If f3 = 410 MHz is the desired signal, it will be interfered with by the intermodulation products created by its adjacent channels f1, f2, f4, and f5.

To see how third order intermodulation products come about, assume that the input to a two-port with the same output-input relationship as stated in the above section consists of a sum of two sinusoids:

$$v_i = A(\cos \omega_1 f + \cos \omega_2 t) \tag{16}$$

Then, the output voltage is

$$\begin{aligned} v_o = {} & k_1 A(\cos \omega_1 t + \cos \omega_2 t) \\ & + k_2 A^2 (\cos \omega_1 t + \cos \omega_2 t)^2 \\ & + k_3 A^3 (\cos \omega_1 t + \cos \omega_2 t)^3 + \ldots \end{aligned} \tag{17}$$

Expanding these square and cube terms and ignoring the higher order terms, the output voltage is seen to contain not only harmonics of each of the two individual input frequencies but also the intermodulation terms:

$$\frac{3}{4} k_3 A^3 \cos(2\omega_2 \pm \omega_1)t$$

and

$$\frac{3}{4} k_3 A^3 \cos(2\omega_1 \pm \omega_2)t$$

The amplitude of these terms are proportional to the cube of the amplitude of the input signals; therefore, these terms increase three times faster than the fundamental term as the input signals increase, as can be seen in *Figure 5*.

MATCHING

Matching and microwave circuit design are to some designers synonymous. It is the act of making the source and load impedances matched to achieve the desired amount of power reflected and power transferred. Matching is required if the circuit is to yield optimum gain and return loss. Poorly matched devices can cause large amount of reflected power, poor noise performance, and low gain. For an LNA, power reflected caused by improper input match can travel back to the antenna and be re-radiated. Poor input match can also reduce the gain of the LNA and causes the system to have non-optimum noise performance.

Amplifiers can achieve maximum gain and return loss when they are presented with conjugate impedances at the input and output ports. There are two types of matching networks: resistive and reactive. Resistive matching networks rely on resistive elements for matching, usually have wider bandwidths, and consume more power than their reactive counterparts, which use lossless elements (capacitors and inductors). Simple matching networks can be designed with the help of the Smith chart, but more complicated ones often require the use of a computer and some type of network synthesis software.

Standard input and output impedances of most microwave instruments are 50Ω. Therefore, microwave and RF devices are designed to have 50Ω input and output impedances so that they can be easily characterized. In a communication system, however, not every component can be designed or optimized for 50Ω impedances due to other constraints. While most RF ceramic or helical filters have 50Ω impedances, most available SAW filters used to filter intermediate frequencies, for example, exhibit 200Ω impedances, IF ceramic filters usually have impedances of 330Ω, and crystal filters have 1 kΩ impedances. So, devices that are designed to be used with these components may have input or output impedances that are different from 50Ω and need matching networks to perform the necessary impedance transformation for proper characterization. In this case, simple narrow band LC matching networks can be designed to operate at the frequency of interest. Narrow band matches are also useful to reduce NF in some devices and to trade current for voltage in low headroom power amplifiers (such as 3V devices). Shown below is an example of a 50Ω to 200Ω matching network

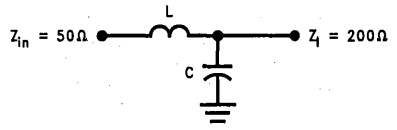

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FIGURE 6. 50Ω–200Ω Matching Network

The actual values of inductance and capacitance for the above network depend on the frequency of operation, f, and can be obtained using the following equations

$$\frac{L}{C} = 10000, \qquad LC = \frac{0.75}{(2\pi f)^2} \tag{18}$$

In general, for a step-up transformer where $Z_{in} < Z_l$ and both are real impedances, the following equations apply:

$$\frac{L}{C} = Z_{in} Z_l, \qquad LC = \frac{1 - Z_{in}/Z_l}{(2\pi f)^2} \tag{19}$$

MIXER CONVERSION GAIN

Conversion gain of mixers is defined as the delivered IF power divided by the available input RF power. The term conversion is used to refer to the frequency converting action of the mixer. Conversion gain can be measured using similar method and equipment setup as those used to measure amplifier gain. More details on conversion gain measurement are deferred to a later application note.

MIXER ISOLATION

Isolation is a measure of how much power is coupled from one port to the next. The two most useful isolation measurements are LO-to-IF isolation and LO-to-RF isolation. The former indicates how much LO power leaks through the output IF port, and the latter indicates how much LO power leaks through the input RF port. LO appearing at the output IF port can be attenuated easily by a lowpass filter since the two frequencies are far apart, but it is more difficult to suppress at the RF port. LO leakage through the RF port usually results in a re-radiation through the antenna if the mixer is used as the first downconverter in a wireless receiver.

MIXER NOISE FIGURE (DSB vs SSB)

Mixer noise figures can be measured and specified in two ways: double side band or single side band. Double side band noise figure measurements involve measuring the noise power contained in both the IF and image components, whereas single side band measurements demand that the image component be filtered out, and only the noise power in the IF component is measured. The DSB method assumes that the gain of the DUT is the same at both image and intermediate frequencies, so it is not recommended for a narrowband DUT or a high intermediate frequency. The SSB method does not require this assumption but does require an external image frequency filter at the input of the DUT. SSB noise figure is used in most applications where the desired information is contained only in the intermediate frequency and the image frequency is rejected. If the DSB measurement method is employed, 3 dB must be added to the measured noise figure to arrive at the SSB noise figure number.

MEASUREMENT TECHNIQUES

Gain, Return Loss, and P_{1dB}

Gain, return loss, and P_{1dB} of the LNA can be measured using a standard scalar S parameter test set which includes a signal generator (e.g., HP8350), a scalar network analyzer (e.g., HP8757) with detector and directional bridge, a two-way splitter, and a variable attenuator. *Figure 7* shows the setup.

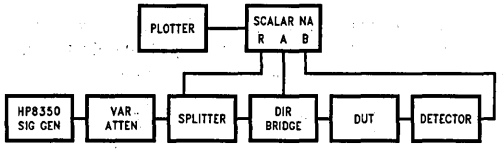

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FIGURE 7. Gain, RL, P_{1dB} Measurement Setup

After the signal generator is set to sweep over the desired frequency range and the variable attenuator at the desired value, the system can be calibrated using standard short and open terminations. Once calibrated, gain measurement can be obtained by setting the scalar analyzer to display the corrected (memory subtracted) channel B power divided by channel R power. This method allows the calculation to remain valid as the signal generator output power is changed. The variable attenuator value must be set such that the input power into the DUT is far (at least 10 dB) below the expected 1 dB compression point so that the DUT is operating in its linear region. To measure input return loss, the analyzer should display the corrected channel A divided by channel R power. Most analyzers allow dual channel displays, in which case, gain and return loss can be obtained in one plot. P_{1dB} can be obtained by gradually decreasing the attenuator value until the observed gain is 1 dB below the linear gain.

Intercept Point (OIP_3)

Output third order intercept point measurement requires two signal generators, a combiner, and a spectrum analyzer. The input of the DUT is a sum of two continuous wave RF signals at Δf apart, combined by the combiner, and the output is displayed on the spectrum analyzer. The power level of the two input signals are such that the DUT is operating in the linear range, and Δf is about a few hundred kHz or a few MHz. The intercept point is obtained by dividing the measured power level difference between the fundamental and the third order mixing product components (denoted by D in *Figure 8*) by 2 and adding the result to the power level of the fundamental component (P_0). The frequency spectrum observed on the spectrum analyzer may look similar to that illustrated by the *Figure* below.

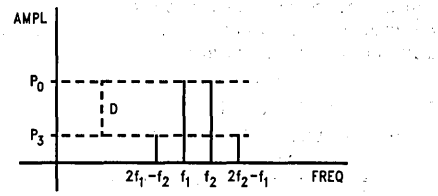

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FIGURE 8. Third Order Intermodulation

As shown above, the output third order intercept point is given by the following equation:

$$OIP_3 = P_0 + \frac{D}{2} \qquad (20)$$

This equation is a direct result of the fact the third order products grow three times faster than the fundamental term, as mentioned earlier.

CONCLUSION

Basic theory and operation of low noise amplifiers and mixers have been presented, together with the most important figures of merit and measurement methods. Also discussed were fundamental concepts on noise in electrical systems, particularly how it is generated and measured as applied to low noise amplifiers.

REFERENCES

1. *"Fundamentals of RF and Microwave Noise Figure Measurements,"* Hewlett Packard, Application Note 57-1.
2. Vendelin, G.D., Pavio, A.M. and Rohde, U.L. *"Microwave Circuit Design"*, John Wiley & Sons, New York, 1990.
3. Maas, S.A. *"Microwave Mixers"*, Artech House, 1986.
4. Spencer, R.R. *"Noise in Electronic Devices, Circuits, and Systems"*, University of California, Davis, 1991.

Section 2

Baseband Processing Components

Section 2 Contents

National Semiconductor

PRELIMINARY

LMX2411
Baseband Processor for Radio Communications

General Description

The LMX2411 is a monolithic, integrated baseband processor suitable for use in Digital European Cordless Telecommunications (DECT) systems as well as other mobile telephony and wireless communications applications. It is fabricated using National's ABiC IV BiCMOS process (f_T = 15 GHz).

The LMX2411 contains both transmit and receive functions. The transmitter utilizes a low power, high speed digital-to-analog converter (DAC) and a mask programmable Read Only Memory (ROM) to generate a Gaussian filter pulse shape. The receiver includes a high speed, low power voltage comparator for making hard decisions on incoming data and a CMOS switch coupled with a sample and hold circuit for DC compensation. Supply voltage can range from 2.85V to 3.6V. The LMX2411 features very low current consumption of 2.5 mA transmit and 5 mA receive (steady state). It also has separate power down pins for transmit and receive functions to further reduce power consumption.

The LMX2411 can be used with the LMX2216B LNA/Mixer, the LMX2240 IF Receiver, and the LMX2320 Phase-Locked Loop to form a complete RF front end solution. These chips form the major blocks of an RF front end solution for DECT.

The LMX2411 is available in a 16-pin JEDEC surface mount plastic package.

Features

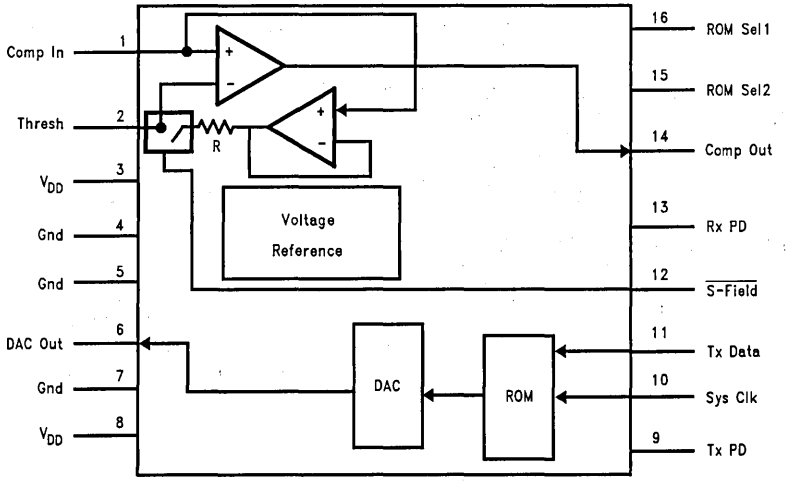
- High speed voltage comparator (40 ns settling time)
- Generates Gaussian filtered modulating signal for a direct VCO modulator
- Bit rates to 1.152 Mb/s (DECT)
- Supports 10.368, 13.824, and 18.432 MHz system clocks through pin selection
- On-chip DC compensation circuit
- Average current consumption 0.6 mA for DECT handset (burst mode operation)
- Power down mode for extended battery life
- Compatible with Sierra SC14400 and Philips PCD5040 DECT Burst Mode Controllers

Applications

- Digital European Cordless Telecommunications (DECT)
- Portable wireless communications (PCS/PCN, cordless)
- Wireless local area networks (WLANs)
- Other wireless communications systems

This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.

Functional Block Diagram



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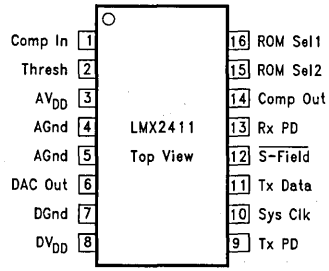
LMX2411 Connection Diagram

Small Outline Package—(SOP)



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Top View

Order Number LMX2411M
See NS Package Number M16A

Pin Description

Pin No.	Pin Name	I/O	Description
1	Comp In	I	Positive input to the threshold comparator
2	Thresh	I/O	Negative input to the threshold comparator. This pin should be connected to a DC voltage only if the internal DC compensation circuit is not used. When the DC compensation loop is used, this pin should have a capacitor to ground on it.
3	V_{DD}		Supply voltage
4	GND		Ground
5	GND		Ground
6	DAC Out	O	Output of the Gaussian filter for modulating a VCO
7	GND		Ground
8	V_{DD}		Supply voltage
9	Tx PD	I	Transmitter power down. DAC is set to 128 (HEX 80) (Mid-range) when this is HIGH.
10	Sys Clk	I	Oversampling input clock from the system (9x, 12x, or 16x the bit rate). If 12x or 16x is used, the effective sampling rate for the ROM filter is 6x or 8x, respectively.
11	Tx Data	I	Transmit data input
12	$\overline{\text{S-Field}}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled, and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold is held by the external capacitor.
13	Rx PD	I	Receiver power down pin; should be grounded if power down is not used.
14	Comp Out	O	Comparator output
15	ROM Sel2	I	ROM selection pin 2. Selects the oversampling clock to be used for the ROM filter.
16	ROM Sel1	I	ROM selection pin 1. Selects the oversampling clock to be used for the ROM filter.

Gaussian ROM Selection Table

ROM Sel2	ROM Sel1	Function
0	0	10.368 MHz System Clk ROM is selected
0	1	13.824 MHz System Clk ROM is selected
1	0	18.432 MHz System Clk ROM is selected
1	1	Reserved

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage (V_{CC})	6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_l) (Soldering, 10 Seconds)	+260°C

Recommended Operating Conditions

Supply Range (V_{CC})	2.85V to 3.6V
Operating Temperature (T_A)	−10°C to +70°C

DC Electrical Characteristics

The following specifications are guaranteed over the recommended operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INTERFACE SECTION (Note 1)						
V_{OH}	High Level Output Voltage	$I_{OH} = -1.0$ mA	$V_{CC} - 0.4$			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 1.0$ mA			0.4	V
V_{IH}	High Level Input Voltage		$V_{CC} - 0.8$			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IN}	Input Current	$GND < V_{IN} < V_{CC}$	−1.0		1.0	μA

Note 1: DC Electrical Characteristics for the digital section apply to all digital input and output pins. This includes Tx Data, Tx PD, Rx PD, Comp Out, ROM Sel1, ROM Sel2, and S-Field.

Electrical Characteristics

The following specifications are guaranteed over recommended operating conditions, and oscillator (Sys Clk) frequency of 10.368 MHz unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{Rx}	Rx Mode Current Consumption (Note 1)	Tx Mode Off		6	7	mA
I_{Tx}	Tx Mode Current Consumption (Note 2)	Rx Mode Off		3.5	5	mA
I_{PD}	Standby Current (Power Down)	Tx and Rx Mode Off		50	100	μA
SYSTEM CLK INPUT						
V_{OSC}	Oscillator Sensitivity	Sys Clk Input	0.5			V_{PP}
f_{OSC}	Maximum Oscillator Frequency	40% < Duty Cycle < 60%	19			MHz
V_{OFF}	Oscillator DC Offset			1.5		V
I_{OSC}	Oscillator Input Current	$GND < V_{IN} < V_{CC}$		±30	±50	μA
TRANSMIT ROM FILTER						
t_S	DAC Voltage Settling Time to within ½ LSB	$C_{LOAD} = 3$ pF All 0's to all 1's		100		ns
R_{OUT}	Output Impedance (Pin 6)		2.9		4.1	kΩ
V_{OUT}	Output Voltage Swing (Pin 6) (Note 3)	Measured from 0V	0.95		1.05	V
	DAC Midband Voltage	DAC Code = 10000000	479		529	mV
	Gaussian Filter Pulse Response Accuracy (Note 4)				±0.5	%
	ISI from Gaussian Filter (Note 5)	$B_b T = 0.5$ Filter		11		%
DC COMPENSATION SAMPLE AND HOLD CIRCUIT						
V_{OS}	Input Offset Voltage				3	mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V		1		V_{PP}
R_{SH}	Sample and Hold Resistor		2240		3360	Ω
D_V	Threshold Input Voltage Droop	$C_{HOLD} = 2700$ pF (Pin 2)		1	10	mV/ms

Electrical Characteristics The following specifications are guaranteed over recommended operating conditions, and oscillator (Sys Clk) frequency of 10.368 MHz unless otherwise specified. (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
COMPARATOR						
t_{SET}	Settling Time	100 mV step with 5 mV Overdrive; 20 pF load		40		ns
V_{IN}	Input Voltage Range	Centered at 1.5V	1.1		2	V
I_{BIAS}	Comp In Bias Current (Pin 1)				4	µA
I_t	Threshold Input Bias Current			2.7	27	nA
V_{IOS}	Input Offset Voltage				3	mV

Note 1: Average current consumption for an 8% power up duty cycle is 8% × 6 mA = 0.48 mA; average current consumption for a 40% power up duty cycle is 40% × 6 mA = 2.4 mA.

Note 2: Average current consumption for a 5% power up duty cycle is 5% × 3.5 mA = 0.175 mA.

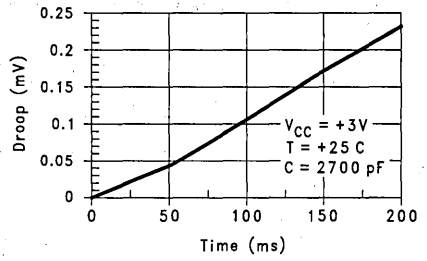
Note 3: Output range = 0 to (V_{REF} * 0.8). V_{REF} is an internal bandgap reference which produces a voltage of nominally 1.25V ±50 mV.

Note 4: Pulse response accuracy is measured as a percentage of the measured output pulse response vs. the calculated ideal Gaussian pulse response.

Note 5: ISI is Inter-symbol Interference, and is defined as the smallest peak-to-peak voltage obtained by an alternating bit pattern divided by the largest peak-to-peak voltage obtained by alternating four 1's and four 0's.

Typical Performance Characteristics

Sample and Hold Droop vs Time



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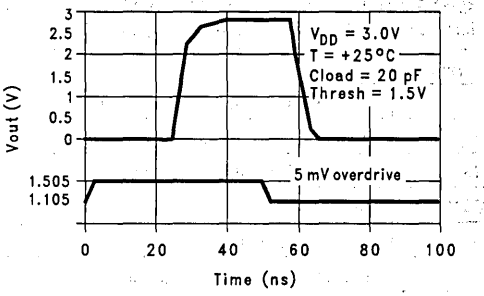
Comparator Output vs Time



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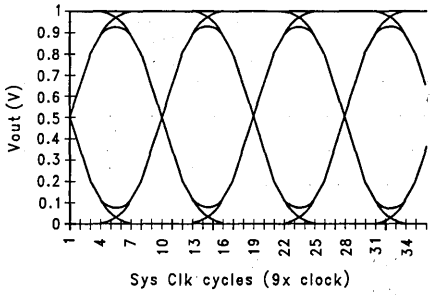
Gaussian B_b T = 0.5 Output Eye Diagram



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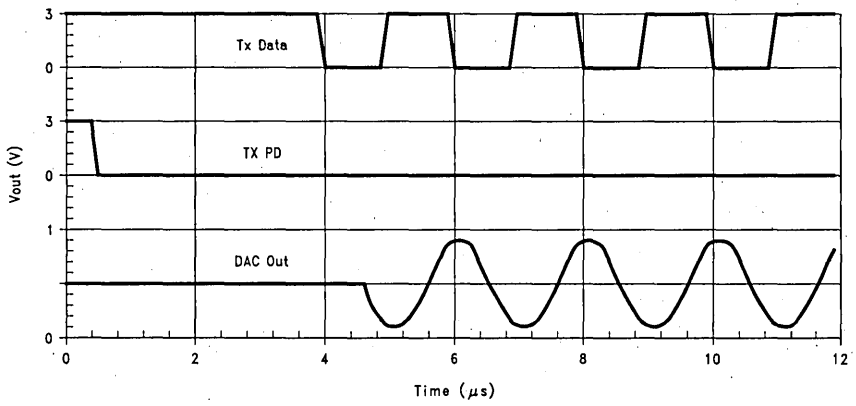
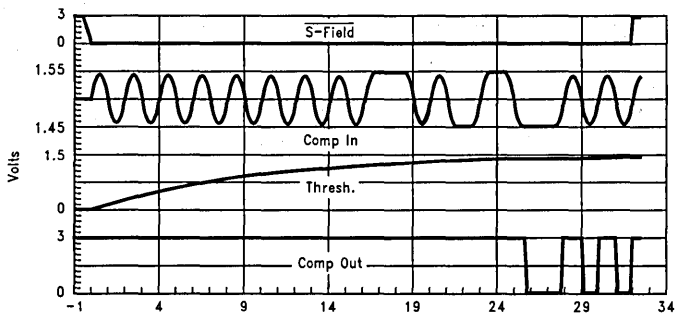
Typical Performance Characteristics (Continued)

DAC Output at Start of Transmit Burst vs Time



TL/W/11911–6

DC Comp. Circuit Response vs Time
(from Full Discharge of Hold Capacitor)
(See Application Circuit)



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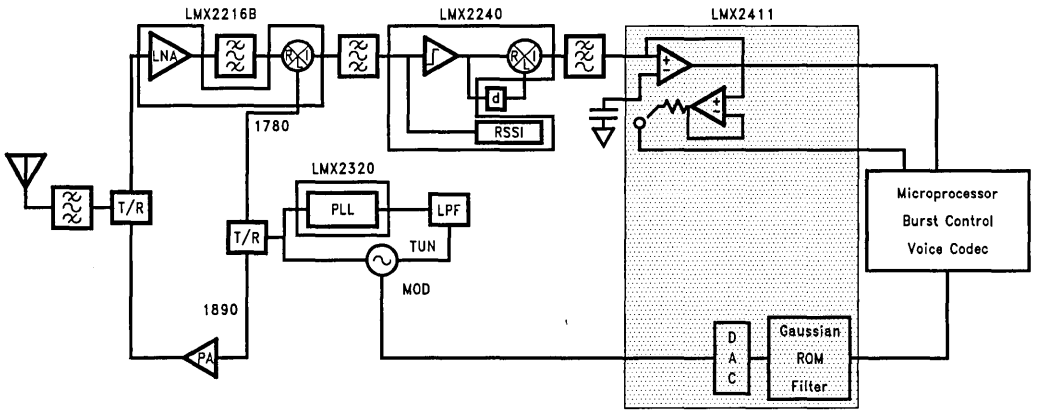
Typical Application Block Diagram



TL/W/11911–8

Functional Description

OVERVIEW

The LMX2411 is a 3V integrated circuit designed to be capable of regenerating received GMSK data and generating GMSK transmitter drive signals to meet the specifications of the Digital European Cordless Telecommunications (DECT) standard.

The transmit portion of the LMX2411 functions as a pulse shaper for incoming serial data, delivering a filtered data stream capable of modulating a VCO. The ROM and supporting logic is designed to create Gaussian filter pulse responses. The output of the LPF ROM and DAC is the modulating baseband drive signal that is fed to a VCO.

The receiver section of the LMX2411 processes the filtered data stream produced by a demodulator (e.g., the LMX2240). The data stream is compared against a threshold voltage determined by the DC compensation circuit. This DC compensation circuit allows control over DC drift due to temperature, frequency drift, component tolerance, and aging.

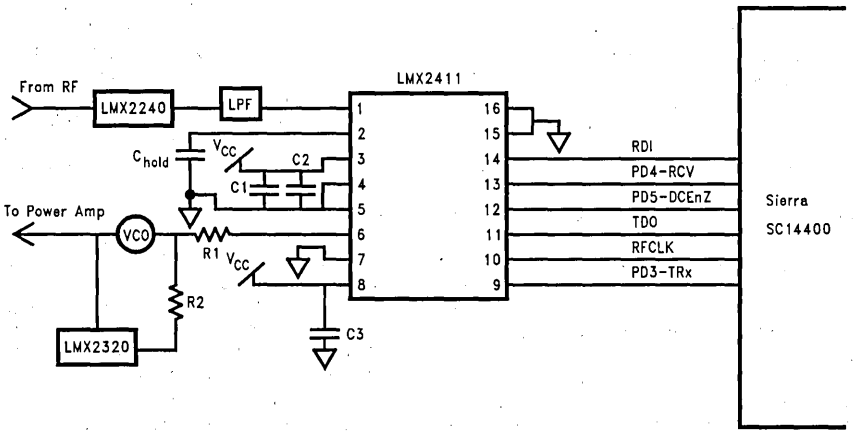
THE TRANSMIT ROM FILTER

The LMX2411 uses a mask-programmable Read-Only Memory (ROM) look-up table to construct pulse responses of a Gaussian filter shape. For DECT, this filter is half the bandwidth of the bit rate (B_b T = 0.5). The output of the ROM addresses a (voltage mode output) digital-to-analog converter (DAC). The LMX2411 ROM Filter supports three different system clocks selected by two external pins. These pins (ROM Sel1 and ROM Sel2) choose the proper oversampling clock. When the 12x or 16x clock is chosen, a divide by 2 flip flop is enabled to give the ROM a 6x or 8x clock from which to operate. However, when the 9x oversampling clock (10.368 MHz) is chosen, the divide by 2 circuit is not enabled. The Tx Data is synchronized with the Sys Clk in the following manner: When Tx PD is taken LOW, the first edge (rising or falling) of Tx Data initializes an internal counter, so that the data bits are sampled near their center. The power up state of the three bit memory in the ROM filter depends on the state of Tx Data during power down. If Tx Data is LOW when the Tx PD pin is HIGH, the ROM filter register will be set to 010. If Tx Data is HIGH when the Tx PD pin is HIGH, the ROM filter register will be set to 101. This allows the filter to be set for either base station or handset operation.

THE COMPARATOR AND ANALOG DC COMPENSATION CIRCUIT

The high speed comparator's threshold can be set either by an external voltage or by using the internal DC compensation circuit. When using the internal DC compensation loop, the received, demodulated signal is input both to the comparator "+" input and to the sample-and-hold (S&H) buffer amplifier. The S&H buffer allows a single RC filter to average the DC value of the received signal without distorting it. This DC value is connected to the "−" input of the comparator. When the signal $\overline{\text{S-Field}}$ is used (named after the synchronization field in DECT), this circuit can acquire the DC voltage during the preamble and then hold it (with the external capacitor) for the duration of the burst. This solution avoids the problem of long strings of 1's and 0's that conventional continuous averaging circuits have while still reacting quickly to acquire the proper DC average at the beginning of a burst.

Typical Application Examples



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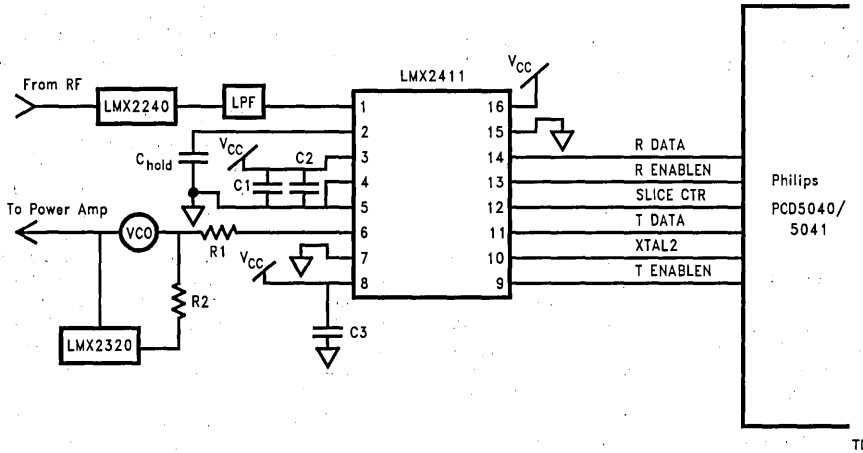
(a)



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(b)

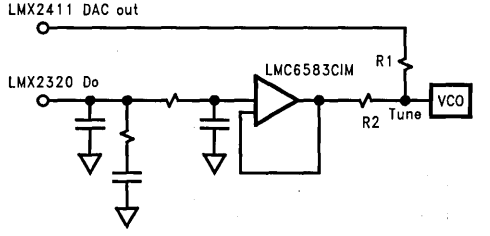
C1 = 1 μF ±10% Tantalum (polarized) C2 = 0.01 μF ±10% NPO Ceramic
C3 = 0.01 μF ±10% NPO Ceramic C_{HOLD} = 2700 pF ±10% NPO Ceramic
R1 and R2 are 5% ¼W Thin Film Carbon (values calculated from equation (1))
LPF = 1 MHz low pass filter (Toko H354LAI-2484DDD)

Application Information

THE TRANSMIT DAC

The transmit DAC uses a voltage mode output. By nature, the output impedance of voltage mode DACs is relatively high. To conserve current, the output impedance of the LMX2411 was designed at 3 kΩ. This results in very low current consumption in the resistor strings, but also results in low drive capability. The user should be aware that in order to achieve the minimum settling time, the maximum capacitive load for the DACs should be no more than 3 pF. To achieve a settling time suitable for DECT bit rates, the maximum capacitive load the transmit DAC should see is about 15 pF.

VCO modulation of a TDD and/or TDMA radio requires some compromise to the VCO phase-locked loop circuitry. A common practice is to use a very narrow PLL loop bandwidth to avoid distorting the modulating signal. However, this is not an effective technique when fast switching is required. Rapid switching times demand a wide loop bandwidth. A typical loop bandwidth of 20 kHz will distort the lower frequency components of the DECT modulating signal.



TL/W/11911–11

FIGURE 1. Illustration of a Circuit That Could Be Used to Modulate an Open Loop VCO.

An alternate modulation technique is to open the loop by powering down the PLL, which in the LMX2320 results in a TRI-STATE® at the charge pump output. For short bursts, the loop filter will not lose the charge, and the center frequency will not drift. *Figure 1* shows a sample circuit for modulating on an open loop. Note that the VCO requires only one tuning port for both locking and modulation. R1 and R2 will vary depending on which wideband VCO is used. The proper equation to be used in determining R1 and R2 is below:

$$V_{DAC} * \frac{R2}{R1 + R2} * K_V = 576\ kHz \qquad (1)$$

In this case, K_V is the VCO sensitivity, expressed in MHz/V, and V_{DAC} is nominally 1V. Generally, R1 will be on the order of 50 kΩ to 250 kΩ, and the ratio of R1 to R2 will vary from 30:1 to 50:1 for wideband VCOs, and will be smaller for narrowband VCOs. Also, the 576 kHz is the peak to peak frequency deviation for DECT, which means the peak is half of that, or 288 kHz.

The Gaussian filter ROM DAC uses a three bit memory to represent the filter's pulse response. The result is an effective 3 bit time delay from input of the first bit to when that bit is actually output from the filter. When using the LMX2411 transmit section, the bits must be sent two bit times before they must be seen at the antenna to account for this small delay in the ROM DAC. There is also a half bit sample delay to allow the 2411 to sample the data near the center of the bit. Also, the end of the information data stream must be padded by 3 bits to push the last data bit through the filter. Finally, it should be noted that after the Tx PD pin goes low, the ROM filter output will be at the mid-band voltage until the first edge of Tx Data, which is used for synchronizing the internal clock with the transmitted data.

The three bit address of the ROM filter is preset to an alternating pattern when Tx PD is HIGH. The value of the alternating pattern depends on the polarity of Tx Data when Tx PD is HIGH. If Tx Data is HIGH (handset), the three bit memory is set to 101, and if Tx Data is LOW (base station), the three bit memory is set to 010. This allows for either the base station or handset preamble.

When beginning the burst for open loop modulation, the Tx Data line should be held constant at the polarity opposite to the first bit to be transmitted. For handsets, this means Tx Data should be HIGH; for base stations, this means Tx Data should be LOW. When Tx PD goes LOW, the output of the ROM filter will stay at mid-band (DAC code "10000000") until the first edge on Tx Data. This allows the DAC average output voltage to be added to the PLL loop voltage while the center frequency is being acquired, thus avoiding a frequency offset problem.

THE DC COMPENSATION LOOP

The analog DC compensation loop is designed to provide a simple yet accurate way to track and correct the effects of DC drift due to center frequency drift. This loop will provide accurate representations of the center voltage of the received signal. However, on initial startup (i.e., full Hold capacitor discharge), the average DC value will not be recovered until the end of the DECT synchronization word for the first burst. The second and subsequent bursts should have the DC value recovered within the first few bits of the synchronization field. This means that in normal situations, the receiver will miss the first burst due to lack of synchronization (i.e., too many errors in the CRC).

It should be noted, however, that because the droop in the sample and hold circuit is small, a normal DECT conversation can take place without degradation. The Typical Performance Characteristics plots should be consulted for expected droop values and DC compensation loop performance.

Some burst mode controllers support a digital DC compensation method (i.e., Sierra SC14400). In this method, the duty cycle of the incoming signal is monitored by a counter, and an update value is sent to a DAC that sets the threshold value for the comparator. In this case, the LMX2411 should have the pin for $\overline{\text{S-Field}}$ pulled HIGH, and the output of the BMC's DAC should be input directly to the comparator's threshold input (pin 2).

Section 3

Control and Signal Processing Components

Section 3 Contents

National Semiconductor

The 8-Bit COP8™ Family: Optimized for Value

Key Features

- High-performance 8-bit microcontroller
- Full 8-bit architecture and implementation
- 1 μs instruction-cycle time
- High code efficiency with single-byte, multiple-function instructions
- UART
- A/D converter
- WATCHDOG™/clock monitor
- Brown Out Detect
- On-chip ROM from 768 bytes to 16k bytes
- On-chip RAM to 256 bytes
- EEPROM
- M²CMOS™ fabrication
- MICROWIRE/PLUS™ serial interface
- Wide operating voltage range: +2.3V to +6V
- Military temp range available: −55°C to +125°C
- MIL-STD-883C versions available
- 16- to 44-pin packages

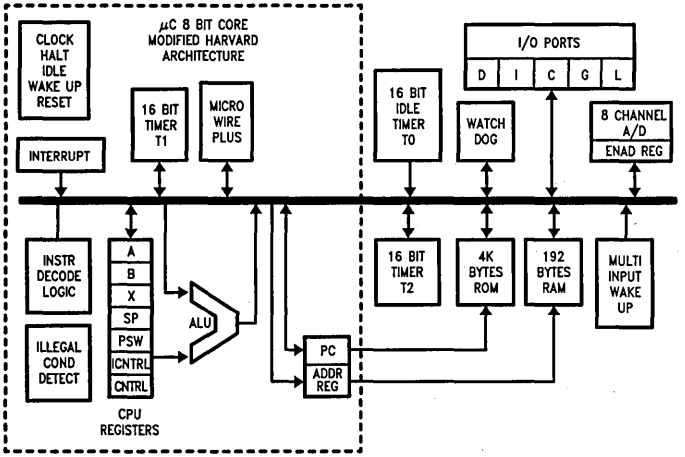
The COP8 combines a powerful single-byte, multiple-function instruction set with a memory-mapped core architecture.

Key Applications

- Automotive systems
- Process control
- Robotics
- Telecommunications
- AC-motor control
- DC-motor control
- Keyboard controllers
- Modems
- RS232C controllers
- Toys and games
- Industrial control
- Small appliances

The COP8 family offers high performance in a low-cost, easy-to-design-in package.

An Example of COP888 Block Diagram (COP888CF)



TL/XX/0073–3

Embedded Control: Practical Solutions to Real Problems

Microcontrollers have played an important role in the semiconductor industry for quite some time. Unlike microprocessors, which typically address a range of more compute intensive, general purpose applications, microcontrollers are based on a central processing unit, data memory and input/output circuitry that are designed primarily for specific, single function applications.

During the 1970s, microcontrollers were initially used in simple applications such as calculators and digital watches. But the combination of decreasing costs and increasing integration and performance has created many new application opportunities over the years. Even as the bulk of application growth occurs in the 8-bit arena, the same issues that system designers were concerned with in the 4-bit world continue in force today. These include cost/performance tradeoffs, low power and low voltage capabilities, time to market, space/pin efficiency and ease of design.

- **Cost/Performance.** A price difference of just a few pennies can be the gating factor in today's 8-bit design decisions. Manufacturers must offer a wide range of cost/performance options in order to meet customer demands.
- **Low Power and Low Voltage.** The increasing range of mobile and/or battery-powered applications is placing a premium on low-power, low-voltage, CMOS and BiCMOS embedded control solutions.
- **Time to Market.** All 8-bit microcontroller's architecture, functionality and feature set have a major influence on product design cycles in today's competitive market, with its shrinking windows of opportunity.
- **Space/Pin Efficiency.** Real estate and board configuration considerations demand maximum space and I/O pin efficiency, particularly given today's high integration and small product form factors.
- **Ease of Design.** A familiar and easy to use application design environment—including complete development tool support—is one of the driving factors affecting today's 8-bit microcontroller design decisions.

All of these issues must be considered when searching for the appropriate 8-bit microcontroller to meet specific application needs. And that's why National Semiconductor's COP8 family of 8-bit microcontrollers is enjoying widespread success in today's global embedded control marketplace.

One of the leaders in the design, manufacture and sale of 8-bit microcontrollers is National Semiconductor. Long a prominent player in the worldwide microcontroller market, National and its COP8 family of products spans today's range of applications, providing customers with a wealth of options at every price/performance point in the 8-bit microcontroller market.

National's 8-bit COP8 microcontrollers enable the company to meet a wide range of embedded control application requirements. COP8 microcontrollers offer users cost-effective solutions at virtually every price/performance point in today's market for 8 bit applications.

Designers can select from a variety of building blocks centered around a common memory-mapped core and modified Harvard architecture. These building blocks include ROM, RAM, user programmable memory, UART, comparator, A/D and I/O functions.

The COP8 family incorporates 1 μs instruction cycle times, watchdog and clock monitors, multi-input wake up circuitry and National's MICROWIRE/PLUS™ interface. In addition, National's COP8 microcontrollers are available in a wide variety of temperature range configurations from −55°C on up through +125°C—optimizing them for rugged industrial and military applications.

COP8 Benefits

The COP8 family provides designers with a number of features that result in substantial benefits. These include a code-efficient instruction set, low power/voltage features, efficient I/O, a flexible and configurable design methodology, robust design tools and electromagnetic interference (EMI) control.

The COP8 family's compact, efficient and easy-to-program instruction set enables designers to reduce time to market for their products. Thanks to the instruction set, efficient ROM utilization lowers costs while providing the opportunity to integrate additional functionality on-chip. Low voltage operation, low current drain, multi-input wakeup and several power saving modes reduce power consumption for today's increasing range of handheld, battery-driven applications. And an array of user-friendly development tools—including hardware from MetaLink, and state of the industry assemblers, C compilers, and a "fuzzy logic" design environment help design engineers save valuable development time.

National's Configurable Controller Methodology (CCM) for the COP8 family creates "whole products" that are bug-free, fully tested and characterized, and supported by a range of documentation and hardware/software tools. National developed CCM because the majority of customer requests for new products have typically called for reconfigurations of existing proven blocks—such as RAM, ROM, timers, comparators, UARTs, and I/O.

In addition, COP8 products incorporate circuitry that guards against electromagnetic interference—an increasing problem in todays microcontroller board designs. Nationals patented EMI reduction technology offers low EMI clock circuitry, EMI-optimized pinouts gradual turn-on outputs (GTO) an on-chip choke device and to help customers circumvent many of the EMI issues influencing embedded control designs.

A Growing Family

National's wide-ranging COP8 family is well-positioned to meet the expanding variety of consumer 8- bit microcontroller applications. Available in a wealth of different ROM (768 bytes to 16k bytes) and RAM (64 x 8, 128 x 8, and 512 x 8) configurations, COP8 microcontrollers provide designers with cost-effective solutions at every price/performance point in todays market. And the recent introduction of the new COP912C—National's first 8 bit microcontroller priced below 50¢ per unit when purchased in volume quantities—continues to drive prices down in the highly competitive 8-bit market.

A code-efficient instruction set. Low power operation. I/O pin efficiency. A "whole product" philosophy that includes superior development tools, documentation and support. These are the reasons that National's COP8 family is a key player in the worldwide 8-bit microcontroller market. As that market continues to expand. National continues its microcontroller technology research and development efforts—an ongoing commitment that began during the infancy of embedded control and continues in full force today.

COP8 Features/Benefits Analysis

	Key Features	Benefits
Instruction Set	• Efficient Instruction Set (77% Single Byte/Single Cycle) • Easy To Program • Compact Instruction Set • Multi Function Instructions • Ten Addressing Modes	• Efficient ROM Utilization (compact code) • Low Cost Microcontroller (small ROM size) • Fast Time To Market
Low Power	• Low Voltage Operation • Lower Current Drain • Multi-Input Wakeup • Power Savings Modes (HALT/IDLE)	• Lower Power Consumption for Hand Held Battery Driven Applications
Efficient I/O	• Software Programmable I/O • Efficient Pin Utilization • Breadth of Available Packages • Package Types Including Variety of Low Pin Count Devices • High Current Outputs • Schmitt Trigger Inputs	• Multiple Use of I/O Pins • Economical Use of External Components (lower system cost) • Cleaner Hardware Design • Choice of Optimum Package Type (price/outline/pinout)
Flexible/Powerful On-Board Features	• Smart 16-Bit Timers (processor independent PWM) • Comparators • UART • Multi-Input Wakeup • Multi-Source Hardware Interrupts • MICROWIRE/PLUS Serial Interface • Application Specific Features (CAN, Motor Control Timers, etc.)	• Timers Allow Less Software/Process Overhead for Frequency • Measurement (capture) and PWM • Cleaner Hardware (eliminating the need for external components) • Overall Cost Reduction
Safety/Software-Runaway Protection	• WATCHDOG • Software Interrupt • Clock Monitor • Brown Out Detection	• No Need for External Protection Circuitry • Brown Out Detection Allows the Use of Low Cost Power Supply
Development Tools	Hardware: • New, User Friendly, Development Tool Hardware from MetaLink • Low Cost Version of the Development Tool (Debug Module) • Various Third Party Programmers for Programming OTPs Software: • New, User Friendly Assembler, a C Compiler and a "Fuzzy" Logic Design Environment	• Saves Engineering Development Time—Fast Time to Market

COP8 Features/Applications Matrix

Market Segment		Applications	Applications Features/Functions	Microcontroller Features Required	Appropriate COP8 Devices
Consumer	Children Toys and Games	Basketball/Baseball Games Children Electronic Toys Darts Throws Juke Box Pinball Laser Gun	Battery Driven Replacing Discrete with Low Cost Driving Piezo/Speaker/LEDs Directly Very Cost Sensitive	Very Low Price Low Power Consumption Wide Voltage Range High Current Outputs Small Packages	COP912C COP920C/COP922C
	Electronic Audio Items	Audio Greeting Cards Electronic Musical Equipment	Battery Driven Tone Generation Low Power	Wide Voltage Range Low Power Consumption Efficient Table Lookup Flexible Timer	COP912C COP820C/840C/880C
	Electronic Appliances/ Tools	Small Appliances: Irons Coffee Makers Digital Scales Microwave Ovens Cookers Food Processors Blenders	Low Cost Power Supply Temp Measurement Safety Features Noise Immunity Driving LEDs/Relays/Heating Elements	Brown Out Detection On-Board Comparator High Current Outputs Watchdog/Software Interrupt Schmtt Trigger Inputs 16-Bit PWM Timer	COP820/840 COP820CJ Family
		Household Appliances: Oven Control Dishwasher Washing Machine/Dryer Vacuum Cleaner Electronic Heater Electronic Home Control (Doorbell, Light Dimmer, Climate) Sewing Machine	Rely on Hard-Wire Relay Circuits, Timers, Counters, Mechanical Sequence Controllers Temp Control Noise Immunity Safety Features Timing Control Main Driven	Brown Out Detection On-Board Comparator On-Board A/D Watchdog/Soft Interrupt Schmitt Trigger Inputs Flexible Timers PWM Outputs High Current Outputs Safety Features	COP820CJ (on-board comparator) COP888CF (on-board A/D)
	Portable/ Handheld/ Battery Powered	Scales Multimeters (portable) Electronic Key Laptop/Notebook Keyboard Mouse Garage Door Opener TV/Electronic Remote Control Portable PRP or Retail Pos Device Jogging Monitor Smart Cards	Battery Driven Minimal Power Consumption Low Voltage Sensing Measurement Standby Mode Flexible Package Offerings Small Physical Size	Low Voltage Operation Low Power Consumption Wide Voltage Range Power Saving Modes Multi-Input Wakeup On-Board Comparator Small Packages	COP820CJ COP840/COP880 COP888CL (Keyboards) COP8646 (Smart Cards)
Personal Communications		Cordless Phone (base/handset) Phone Dialer Answering Machine Feature Phone PBX Card CB Radios/Digital Tuners Cable Converter	Low Power Timing Serial Interfaces Low Voltage Tone Dialing Battery Saving Functions Small Physical Size	Low Current Drain Low Voltage Operation Standby Mode UART Serial Synchronous Interface 16-Bit Timers Schmitt Trigger Inputs LED Direct Drive Sufficient I/O in Small Packages	Cordless Phone: COP840/COP880 Feature Phone PBX Card: COP888CG/COP888EG Others: Generic COP8 Devices

COP8 Features/Applications Matrix (Continued)

Market Segment		Applications	Applications Features/Functions	Microcontroller Features Required	Appropriate COP8 Devices
Medical	Monitors	Thermometer Pressure Monitors Various Portable Monitors	Battery Driven Sensing/Measurement Data Transmission Low Power Low Voltage	On-Board Comparator (low cost A/D) 16-Bit Timer Low Power Consumption Low Voltage Operation	COP820CJ (on-board) comparator) COP840/COP880 COP888CL
	Medical Equipment	Bed-Side Pump/Timers Ultrasonic Imaging System Analyzers (chemical, data) Electronic Microscopes	Monitoring Data Data Transmission Timing	Serial Interface A/D 16-Bit Timers	COP888CS COP888CF COP888CG/COP888EG
Industrial	Motion Control	Motor Control Power Tools	Motor Speed Control Noisy Environment Timing Control	Flexible PWM Timers Schmitt Trigger Inputs High Current Outputs	COP820/COP840 COP888CL
	Security/ Monitoring System	Security Systems Burglar Alarms Remote Data Monitoring Systems Emergency Control Systems Security Switches	Data Transmission Monitoring (scan inputs from sensors) Keypad Scan Timing Diagnostic Data Monitoring Drive Alarm Sounders Interface to Phone System Standby Mode	UART Flexible 16-Bit PWM Timers Flexible I/O Single Slop A/D Capability Power Saving Modes (HALT, Multi-Input wakeup) Serial Synchronous Interface	Basic Systems: COP840/COP880, COP888CL (Multi-Input wakeup) More Involved Systems: COP888CS/COP888CG COP888EK (muxed analog inputs, constant current source)
	Misc.	Switch Controls (elevator, traffic, power switches) Sensing Control Systems/Displays Pressure Control (scales) Metering (utility, monetary, industrial) Lawn Sprinkler/Lawn Mowers Taxi Meter Coin Controls Industrial Timers Temperature Meters Gas Pump Gas/Smoke Detectors	Timing/Counting Sensing Measurement	Generic Microcontroller	Generic COP8 Microcontroller: COP820/COP840/COP880
Automotive		Radio/Tape Deck Controls Window/Seat/Mirror/Door/ Controls Heat/Climate/Controls Headlight/Antenna Power Steering Anti Theft Slave Controllers	Timing Motion Control Display Control Soft Runaway/Trap Recovery (safety considerations) EMI/Noise Immunity Serial Interfaces Standby Modes Wide Temp Range	Flexible PWM Timers Power Saving Modes Multi-Input Wakeup WATCHDOG Software Trap UART CAN Interface Special Features for Dashboard Control (counters, capture modules, MUL/DIV) Reduced EMI Wide Temp Range	Radio/Climate Control: COP888CG/888EG/888EK Seat/Motional Control, Slave Controller: COP884BC Dashboard Control: COP888GW Mirror Control, etc.: COP8 Basic Family Climate Control: COP888CF

COP8 Family Selection Guide

Common Features:

- Multi-Source Interrupt
- Pinout
- Instruction Set
- MICROWIRE Serial Communication
- 1 μs Instruction Cycle Time
- Wide Power Supply—2.3V to 6.0V
- CMOS Process Technology
- Halt Mode
- Software Selectable I/O
- Wide Temperature Range
- Development Tools
- OTP Emulators (Note 2)

Comm Temp 0°C to +70°C	Ind Temp −40°C to +85°C	Mil Temp −55°C to +125°C	Memory		I/O	Packages				Features							
			ROM (Bytes)	RAM (Bytes)	Pins	# of Pins	N	WM	V	Interrupt Sources	Timers PWM/ Capture	Comparators	UART	WATCHDOG	Multi-Input Wakeup	Idle Timer	Additional Features
	COP823CJ		1.0k	64	11	16		x		3	1	1		x	x		Brown Out Detection
	COP822CJ		1.0k	64	15	20	x	x		3	1	1		x	x		Modulator, Special PWM,
	COP820CJ		1.0k	64	23	28	x	x		3	1	1		x	x		Timer, High Current Outputs
COP942CJ	COP842CJ	COP642CJ	2.0k	128	15	20	x	x		3	1	1		x	x		Brown Out Detection
COP940CJ	COP840CJ	COP640CJ	2.0k	128	23	28	x	x		3	1	1		x	x		Modulator, Special PWM
																	Timer, High Current Outputs
COP912C			768	64	15	20	x	x		3	1						
COP922C	COP822C	COP622C	1.0k	64	15	20	x	x		3	1						
COP920C	COP820C	COP620C	1.0k	64	23	28	x	x		3	1						
COP942C	COP842C	COP642C	2.0k	128	15	20	x	x		3	1						
COP940C	COP840C	COP640C	2.0k	128	23	28	x	x		3	1						
COP981C	COP881C	COP681C (Note 1)	4.0k	128	23	28	x	x		3	1						
COP980C	COP880C	COP680C (Note 1)	4.0k	128	35	40/44	x		x	3	1						
	COP8622C	COP6622C	1.0k	64	15	20	x	x		3	1						
	COP86L22C	COP6622C	1.0k	64	15	20	x	x		3	1						
	COP8620C	COP6620C	1.0k	64	23	28	x	x		3	1						64 x 8
	COP86L20C	COP6620C	1.0k	64	23	28	x	x		3	1						EEPROM
	COP8642C	COP6642C	2.0k	64	15	20	x	x		3	1						IN
	COP86L42C	COP6642C	2.0k	64	15	20	x	x		3	1						RAM
	COP8640C	COP6640C	2.0k	64	23	28	x	x		3	1						
	COP86L40C	COP6640C	2.0k	64	23	28	x	x		3	1						
COP984CL	COP884CL	COP684CL	4.0k	128	23	28	x	x		10	2			x	x	x	Clock
COP988CL	COP888CL	COP688CL	4.0k	128	33/39	40/44	x		x	10	2			x	x	x	Monitor
COP984CF	COP884CF		4.0k	128	23	28	x	x		10	2			x	x	x	8 Channel
COP988CF	COP888CF		4.0k	128	33/37	40/44	x		x	10	2			x	x	x	(8-bit) A/D

Note 1: MIL-STD-883 in J Pkg

Note 2: Contact sales office for availability.

N = Plastic DIP

V = Plastic Leaded Chip Carrier (PLCC)

WM = Small Outline Package—Wide Body

COP8 Family Selection Guide (Continued)

Common Features:

- Multi-Source Interrupt
- Pinout
- Instruction Set
- MICROWIRE Serial Communication
- 1 μs Instruction Cycle Time
- Wide Power Supply—2.3V to 6.0V
- CMOS Process Technology
- Halt Mode
- Software Selectable I/O
- Wide Temperature Range
- Development Tools
- OTP Emulators (Note 2)

Comm Temp 0°C to +70°C	Ind Temp −40°C to +85°C	Mil Temp −55°C to +125°C	Memory		I/O	Packages				Features							
			ROM (Bytes)	RAM (Bytes)	Pins	# of Pins	N	WM	V	Interrupt Sources	Timers PWM/ Capture	Comparators	UART	WATCHDOG	Multi-Input Wakeup	Idle Timer	Additional Features
COP984CS	COP884CS	COP684CS	4.0k	192	23	28	x	x		12	1	1	x	x	x	x	
COP988CS	COP888CS	COP688CS	4.0k	192	35/39	40/44	x		x	12	1	1	x	x	x	x	
	COP884CG		4.0k	192	23	28	x	x		14	3	2	x	x	x	x	Reduced EMI
	COP888CG		4.0k	192	35/39	40/44	x		x	14	3	2	x	x	x	x	Reduced EMI
COP984EK	COP884EK	COP684EK	8.0k	256	23	28	x	x		12	3	1		x	x	x	6 Analog Inputs, Constant Current Source, Reduced EMI
COP988EK	COP888EK	COP688EK	8.0k	256	35/39	40/44	x		x	12	3	1		x	x	x	
COP984EG	COP884EG	COP684EG	8.0k	256	23	28	x	x		14	3	2	x	x	x	x	
COP988EG	COP888EG	COP688EG	8.0k	256	35/39	40/44	x		x	14	3	2	x	x	x	x	
	COP888GG		16.0k	512	35/39	40/44	x		x	14	3	2	x	x	x	x	Reduced EMI
	COP884BC		2.0k	64	18	28		x		12	1	2			x	x	CAN Interface, Motor Control Timer
	COP888GW		16.0k	512	56	68			x	14	2		x		x	x	Hardware Multiply/ Divide Function, 4x Counter Block, Reduced EMI

Note 1: MIL-STD-883 in J Pkg

Note 2: Contact sales office for availability.

N = Plastic DIP

V = Plastic Leaded Chip Carrier (PLCC)

WM = Small Outline Package—Wide Body

National Semiconductor

COP472-3 Liquid Crystal Display Controller

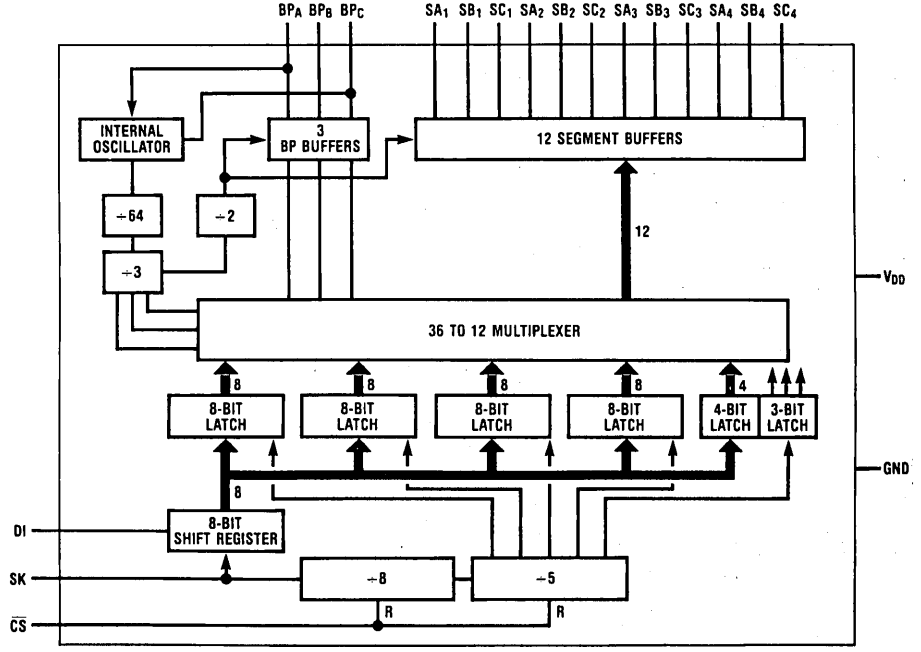
General Description

The COP472-3 Liquid Crystal Display (LCD) Controller is a peripheral member of the COPS™ family, fabricated using CMOS technology. The COP472-3 drives a multiplexed liquid crystal display directly. Data is loaded serially and is held in internal latches. The COP472-3 contains an on-chip oscillator and generates all the multi-level waveforms for backplanes and segment outputs on a triplex display. One COP472-3 can drive 36 segments multiplexed as 3 x 12 (4½ digit display). Two COP472-3 devices can be used together to drive 72 segments (3 x 24) which could be an 8½ digit display.

Features

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 μW typ.)
- Low cost
- Compatible with all COPS processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Operates from display voltage
- MICROWIRE™ compatible serial I/O
- 20-pin Dual-In-Line package and 20-pin SO

Block Diagram



TL/DD/6932-1

Absolute Maximum Ratings

Voltage at CS, DI, SK pins	−0.3V to +9.5V	Storage Temperature	−65°C to +150°C
Voltage at all other Pins	−0.3V to V_{DD}+0.3V	Lead Temp. (Soldering, 10 Seconds)	300°C
Operating Temperature Range	0°C to 70°C		

DC Electrical Characteristics

GND = 0V, V_{DD} = 3.0V to 5.5V, T_A = 0°C to 70°C (depends on display characteristics)

Parameter	Conditions	Min	Max	Units
Power Supply Voltage, V_{DD}		3.0	5.5	Volts
Power Supply Current, I_{DD} (Note 1)	V_{DD}=5.5V		250	μA
	V_{DD}=3V		100	μA
Input Levels				
DI, SK, CS				
V_{IL}			0.8	Volts
V_{IH}		0.7 V_{DD}	9.5	Volts
BPA (as Osc. in)				
V_{IL}			0.6	Volts
V_{IH}		V_{DD}−0.6	V_{DD}	Volts
Output Levels, BPC (as Osc. Out)				
V_{OL}			0.4	Volts
V_{OH}		V_{DD}−0.4	V_{DD}	Volts
Backplane Outputs (BPA, BPB, BPC)				
$V_{BPA, BPB, BPC}$ ON	During	$V_{DD}-\Delta V$	V_{DD}	Volts
$V_{BPA, BPB, BPC}$ OFF	BP+ Time	⅓ $V_{DD}-\Delta V$	⅓ $V_{DD}+\Delta V$	Volts
$V_{BPA, BPB, BPC}$ ON	During	0	ΔV	Volts
$V_{BPA, BPB, BPC}$ OFF	BP− Time	⅔ $V_{DD}-\Delta V$	⅔ $V_{DD}+\Delta V$	Volts
Segment Outputs (SA_1 ~ SA_4)				
V_{SEG} ON	During	0	ΔV	Volts
V_{SEG} OFF	BP+ Time	⅔ $V_{DD}-\Delta V$	⅔ $V_{DD}+\Delta V$	Volts
V_{SEG} ON	During	$V_{DD}-\Delta V$	V_{DD}	Volts
V_{SEG} OFF	BP− Time	⅓ $V_{DD}-\Delta V$	⅓ $V_{DD}+\Delta V$	Volts
Internal Oscillator Frequency		15	80	kHz
Frame Time (Int. Osc. ÷ 192)		2.4	12.8	ms
Scan Frequency ($1/T_{SCAN}$)		39	208	Hz
SK Clock Frequency		4	250	kHz
SK Width		1.7		μs
DI				
Data Setup, t_{SETUP}		1.0		μs
Data Hold, t_{HOLD}		100		ns
$\overline{CS}$				
t_{SETUP}		1.0		μs
t_{HOLD}		1.0		μs
Output Loading Capacitance			100	pF

Note 1: Power supply current is measured in stand-alone mode with all outputs open and all inputs at V_{DD}.

Note 2: $\Delta V = 0.05V_{DD}$.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at CS, DI, SK Pins	−0.3V to +9.5V
Voltage at All Other Pins	−0.3V to V_{DD}+0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

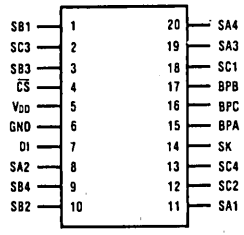
GND = 0V, V_{DD} = 3.0V to 5.5V, T_A = −40°C to +85°C (depends on display characteristics)

Parameter	Conditions	Min	Max	Units
Power Supply Voltage, V_{DD}		3.0	5.5	Volts
Power Supply Current, I_{DD} (Note 1)	V_{DD}=5.5V		300	μA
	V_{DD}=3V		120	μA
Input Levels				
DI, SK, CS				
V_{IL}			0.8	Volts
V_{IH}		0.7 V_{DD}	9.5	Volts
BPA (as Osc. In)				
V_{IL}			0.6	Volts
V_{IH}		V_{DD}−0.6	V_{DD}	Volts
Output Levels, BPC (as Osc. Out)				
V_{OL}			0.4	Volts
V_{OH}		V_{DD}−0.4	V_{DD}	Volts
Backplane Outputs (BPA, BPB, BPC)				
$V_{BPA, BPB, BPC}$ ON	During BP+ Time	V_{DD}−ΔV	V_{DD}	Volts
$V_{BPA, BPB, BPC}$ OFF		⅓ V_{DD}−ΔV	⅓ V_{DD}+ΔV	Volts
$V_{BPA, BPB, BPC}$ ON	During BP− Time	0	ΔV	Volts
$V_{BPA, BPB, BPC}$ OFF		⅔ V_{DD}−ΔV	⅔ V_{DD}+ΔV	Volts
Segment Outputs (SA_1 ~ SA_4)				
V_{SEG} ON	During BP+ Time	0	ΔV	Volts
V_{SEG} OFF		⅔ V_{DD}−ΔV	⅔ V_{DD}+ΔV	Volts
V_{SEG} ON	During BP− Time	V_{DD}−ΔV	V_{DD}	Volts
V_{SEG} OFF		⅓ V_{DD}−ΔV	⅓ V_{DD}+ΔV	Volts
Internal Oscillator Frequency		15	80	kHz
Frame Time (Int. Osc.÷192)		2.4	12.8	ms
Scan Frequency ($1/T_{SCAN}$)		39	208	Hz
SK Clock Frequency		4	250	kHz
SK Width		1.7		μs
DI				
Data Setup, t_{SETUP}		1.0		μs
Data Hold, t_{HOLD}		100		ns
$\overline{CS}$				
t_{SETUP}		1.0		μs
t_{HOLD}		1.0		μs
Output Loading Capacitance			100	pF

Note 1: Power supply current is measured in stand-alone mode with all outputs open and all inputs at V_{DD}.

Note 2: ΔV = 0.05 V_{DD}.

Dual-In-Line Package



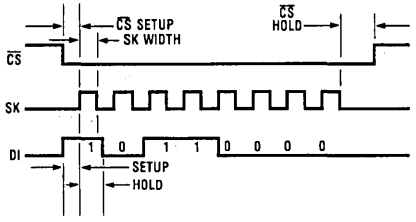
Top View

TL/DD/6932-2

Pin	Description
$\overline{CS}$	Chip select
V_{DD}	Power supply (display voltage)
GND	Ground
DI	Serial data input
SK	Serial clock input
BP_A	Display backplane A (or oscillator in)
BP_B	Display backplane B
BP_C	Display backplane C (or oscillator out)
SA1 ~ SC4	12 multiplexed outputs

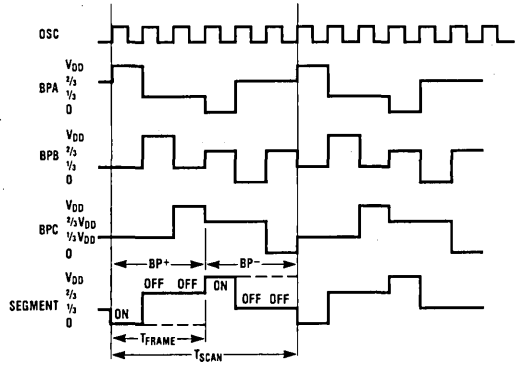
Order Number COP472MW-3 or COP472N-3
See NS Package Number M20A or N20A

FIGURE 2. Connection Diagram



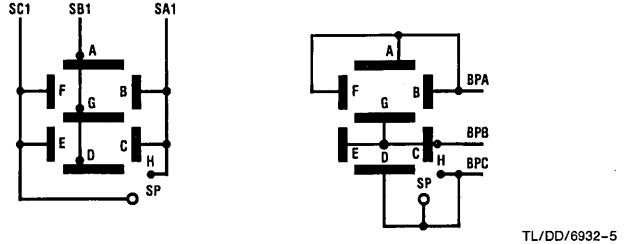
TL/DD/6932-3

FIGURE 3. Serial Load Timing Diagram



TL/DD/6932-4

FIGURE 4. Backplane and Segment Waveforms



TL/DD/6932-5

FIGURE 5. Typical Display Internal Connections
Epson LD-370

Functional Description

The COP472-3 drives 36 bits of display information organized as twelve segments and three backplanes. The COP472-3 requires 40 information bits: 36 data and 4 control. The function of each control bit is described below. Display information format is a function of the LCD interconnections. A typical segment/backplane configuration is illustrated in *Figure 5*, with this configuration the COP472-3 will drive 4 digits of 9 segments.

To adapt the COP472-3 to any LCD display configuration, the segment/backplane multiplex scheme is illustrated in Table I.

Two or more COP472-3 chips can be cascaded to drive additional segments. There is no limit to the number of COP472-3's that can be used as long as the output loading capacitance does not exceed specification.

TABLE I. COP472-3 Segment/Backplane Multiplex Scheme

Bit Number	Segment, Backplane	Data to Numeric Display	
1	SA1, BPC	SH	
2	SB1, BPB	SG	
3	SC1, BPA	SF	
4	SC1, BPB	SE	Digit 1
5	SB1, BPC	SD	
6	SA1, BPB	SC	
7	SA1, BPA	SB	
8	SB1, BPA	SA	
9	SA2, BPC	SH	
10	SB2, BPB	SG	
11	SC2, BPA	SF	
12	SC2, BPB	SE	Digit 2
13	SB2, BPC	SD	
14	SA2, BPB	SC	
15	SA2, BPA	SB	
16	SB2, BPA	SA	
17	SA3, BPC	SH	
18	SB3, BPB	SG	
19	SC3, BPA	SF	
20	SC3, BPB	SE	Digit 3
21	SB3, BPC	SD	
22	SA3, BPB	SC	
23	SA3, BPA	SB	
24	SB3, BPA	SA	
25	SA4, BPC	SH	
26	SB4, BPB	SG	
27	SC4, BPA	SF	
28	SC4, BPB	SE	Digit 4
29	SB4, BPC	SD	
30	SA4, BPB	SC	
31	SA4, BPA	SB	
32	SB4, BPA	SA	
33	SC1, BPC	SPA	Digit 1
34	SC2, BPC	SP2	Digit 2
35	SC3, BPC	SP3	Digit 3
36	SC4, BPC	SP4	Digit 4
37	not used		
38	Q6		
39	Q7		
40	SYNC		

SEGMENT DATA BITS

Data is loaded in serially, in sets of eight bits. Each set of segment data is in the following format:

SA	SB	SC	SD	SE	SF	SG	SH

Data is shifted into an eight bit shift register. The first bit of the data is for segment H, digit 1. The eighth bit is segment A, digit 1. A set of eight bits is shifted in and then loaded into the digit one latches. The second set of 8 bits is loaded into digit two latches. The third set into digit three latches, and the fourth set is loaded into digit four latches.

CONTROL BITS

The fifth set of 8 data bits contains special segment data and control data in the following format:

SYNC	Q7	Q6	X	SP4	SP3	SP2	SP1

The first four bits shifted in contain the special character segment data. The fifth bit is not used. The sixth and seventh bits program the COP472-3 as a stand alone LCD driver or as a master or slave for cascading COP472-3's. BPC of the master is connected to BPA of each slave. The following table summarizes the function of bits six and seven:

Q7	Q6	Function	BPC Output	BPA Output
1	1	Slave	Backplane Output	Oscillator Input
0	1	Stand Alone	Backplane Output	Backplane Output
1	0	Not Used	Internal Osc. Output	Oscillator Input
0	0	Master	Internal Osc. Output	Backplane Output

The eighth bit is used to synchronize two COP472-3's to drive an 8½-digit display.

LOADING SEQUENCE TO DRIVE A 4½-DIGIT DISPLAY

Steps:

1. Turn $\overline{CE}$ low.
2. Clock in 8 bits of data for digit 1.
3. Clock in 8 bits of data for digit 2.
4. Clock in 8 bits of data for digit 3.
5. Clock in 8 bits of data for digit 4.
6. Clock in 8 bits of data for special segment and control function of BPC and BPA.

0	0	1	1	SP4	SP3	SP2	SP1

7. Turn $\overline{CS}$ high.

Note: $\overline{CS}$ may be turned high after any step. For example to load only 2 digits of data, do steps 1, 2, 3, and 7.

$\overline{CS}$ must make a high to low transition before loading data in order to reset internal counters.

LOADING SEQUENCE TO DRIVE AN 8½-DIGIT DISPLAY

Two or more COP472-3's may be connected together to drive additional segments. An eight digit multiplexed display is shown in *Figure 7*. The following is the loading sequence to drive an eight digit display using two COP472-3's. The right chip is the master and the left the slave.

Steps:

1. Turn $\overline{CS}$ low on both COP472-3's.
2. Shift in 32 bits of data for the slave's four digits.
3. Shift in 4 bits of special segment data: a zero and three ones.

1	1	1	0	SP4	SP3	SP2	SP1

This synchronizes both the chips and BPA is oscillator input. Both chips are now stopped.

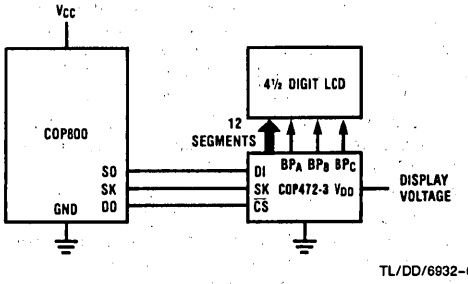
4. Turn CS high to both chips.
5. Turn CS low to master COP472-3.
6. Shift in 32 bits of data for the master's 4 digits.
7. Shift in four bits of special segment data, a one and three zeros.

0	0	0	1	SP4	SP3	SP2	SP1

This sets the master COP472-3 to BPA as a normal backplane output and BPC as oscillator output. Now both the chips start and run off the same oscillator.

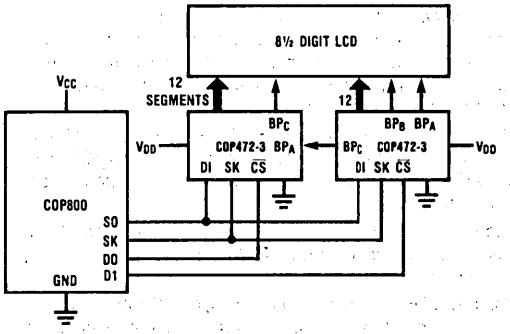
8. Turn $\overline{CS}$ high.

The chips are now synchronized and driving 8 digits of display. To load new data simply load each chip separately in the normal manner, keeping the correct status bits to each COP472-3 (0110 or 0001).



TL/DD/6932-6

FIGURE 6. System Diagram – 4½ Digit Display



TL/DD/6932-7

FIGURE 7. System Diagram – 8½ Digit Display

National Semiconductor

PRELIMINARY

NSAM265SR/NSAM265SF CompactSPEECH™ Digital Speech Processors

General Description

The NSAM265SR and the NSAM265SF are members of National Semiconductor's CompactSPEECH, Digital Speech processors family. These processors provide Digital Answering Machine (DAM) functionality to embedded systems. Both processors are based on the NSAM265.

Unless specified otherwise, all references to the CompactSPEECH processor in this document apply to both the NSAM265SR and the NSAM265SF.

The CompactSPEECH processor integrates the functions of a traditional Digital Signal Processing (DSP) chip and a general purpose 16-bit RISC processor. The device contains system support functions such as DRAM Controller, Interrupt Control Unit, Codec Interface, MICROWIRE™ interface, WATCHDOG™ timer and a Clock Generator.

The CompactSPEECH processor operates as a slave peripheral that is controlled by an external microcontroller via a serial MICROWIRE interface. In a typical DAM environment the microcontroller controls the analog circuits, buttons and display, and activates the CompactSPEECH by sending it commands. The CompactSPEECH processor executes the commands and returns status information to the microcontroller.

The CompactSPEECH firmware implements voice compression and decompression, tone detection and generation, message storage management, on-chip speech synthesis for time and day stamp, and support for user-defined voice prompts in various languages.

The NSAM265SR CompactSPEECH supports DRAM/ARAM for message storage while the NSAM265SF supports FLASH/AFLASH. In all other respects, the processors are identical.

The CompactSPEECH implements echo cancellation techniques to support improved DTMF tone detection during message playback.

CompactSPEECH supports speech synthesis: the technology used to create voice prompts from predefined words and phrases stored in a vocabulary.

The CompactSPEECH can synthesize messages in various languages, in addition to the on-chip English vocabulary, via the International Vocabulary Support (IVS) mechanism. Synthesized messages can be stored on an external ROM. One ROM can contain several vocabularies in various languages. The NSAM265SF can also store vocabularies on FLASH memory. DAM manufacturers can thus create machines that "speak" in different languages, simply by using other vocabularies. For more details about IVS, refer to the *IVS User's Manual.*

Features

- Designed around a 16-bit RISC processor
- 16-bit architecture and implementation
- 20.48 MHz operation
- On-chip DSP Module (DSPM) for high speed DSP operations
- On-chip Codec clock generation and interface
- Power-down mode
- MICROWIRE interface to an external microcontroller
- Storage and management of messages
- Programmable message tag for message categorization, e.g., Mailboxes, InComing Messages (ICM), OutGoing Messages (OGM)
- Skip forward or backward during message playback
- Variable speed playback
- Built-in vocabulary for speech synthesis, and support for external vocabularies. using expansion ROM
- Multi-lingual speech synthesis using International Vocabulary Support (IVS)
- DTMF and single tone generation and detection
- DTMF tone detection during OutGoing Message playback
- Telephone line functions, including busy and dial tone detection
- Real-time clock
- Direct access to message memory
- Supports long-frame and short-frame codecs
- Available in PLCC 68-pin, and PQFP 100-pin packages

NSAM265SR only

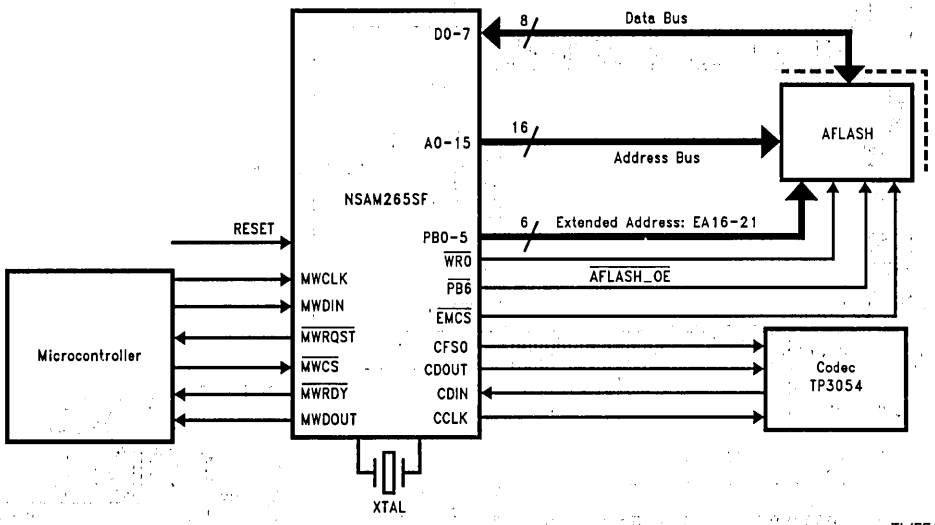
- On-chip ARAM/DRAM Controller for 4-Mbit (1M x 4) and 16-Mbit (4M x 4) devices
- 15 minutes recording on a 4-Mbit ARAM
- Supports various ARAM configurations. No glue logic required
- Storage of up to 1600 messages
- Production diagnostics support

NSAM265SF only

- Supports 4-Mbit and 8-Mbit, byte wide, FLASH/AFLASH devices
- Up to 15 minutes recording on a 4-Mbit FLASH
- Supports various AFLASH configurations. No glue logic required for a single AFLASH configuration
- The number of messages that can be stored is limited only by memory size
- Supports prerecorded IVS and OGM on FLASH

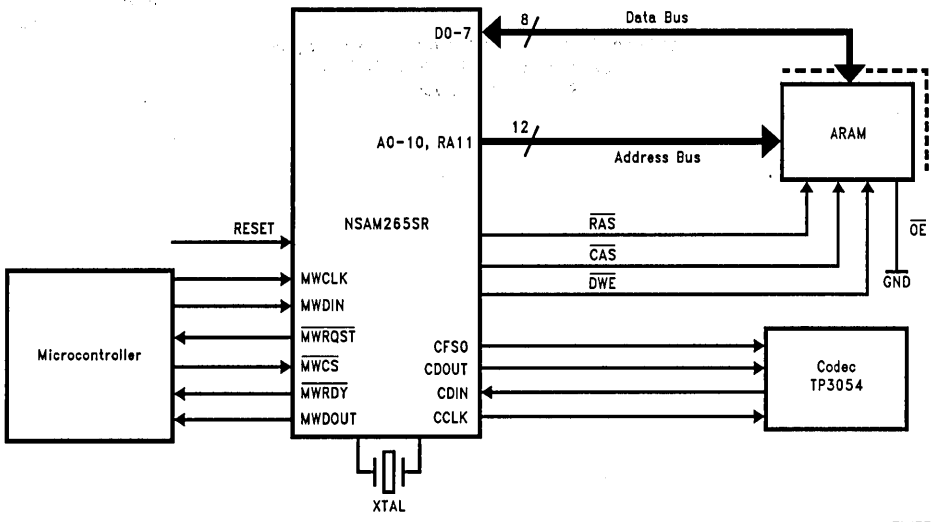
Block Diagrams

NSAM265SF Basic Configuration



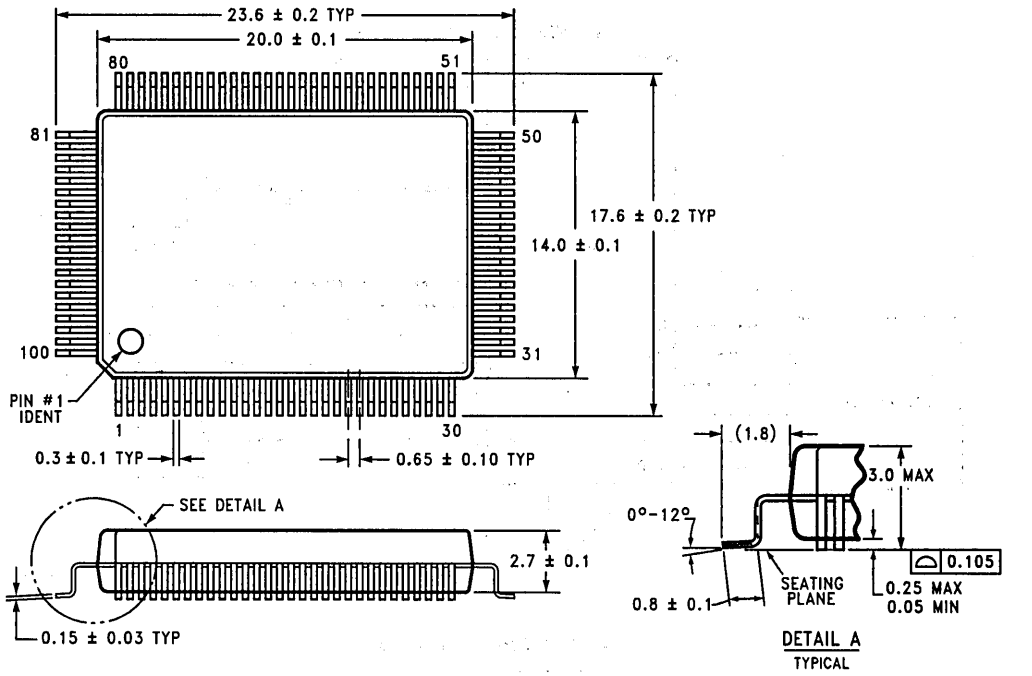
TL/EE/12500-1

NSAM265SR Basic Configuration



TL/EE/12500-2

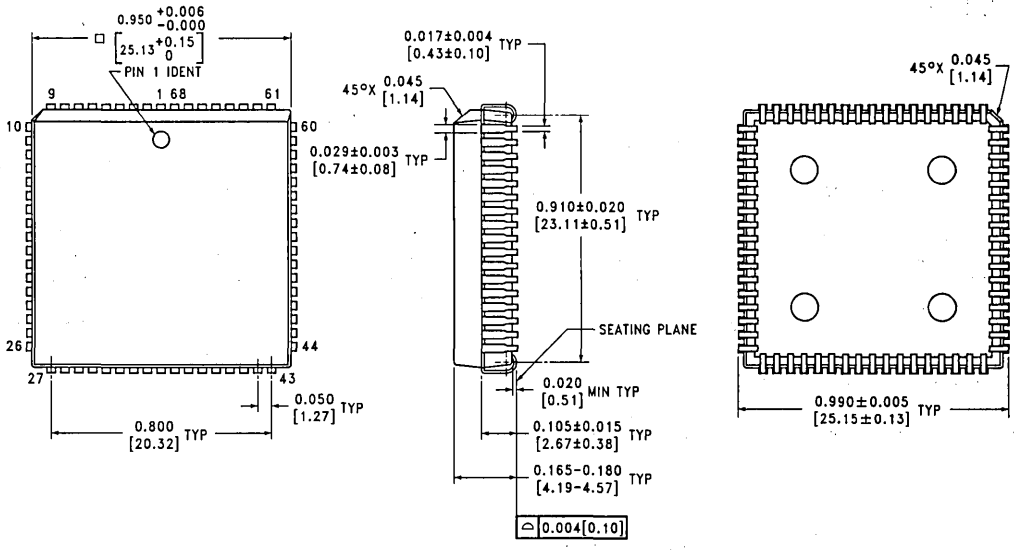
Physical Dimensions inches (millimeters)



TL/EE/12500-3

100-Pin Molded Plastic Quad Flat Package (EIAJ)
Order Number NSAM265SRA/SFA
NS Package Number VLJ100A

Physical Dimensions inches (millimeters) (Continued)



TL/EE/12500–4

68-Pin Plastic Leaded Chip Carrier (V)
Order Number NSAM265SRA/SFA
NS Package Number V68A

LCD Triplex Drive with COP820CJ

National Semiconductor
Application Note 953
Klaus Jaensch and
Siegfried Rueth

INTRODUCTION

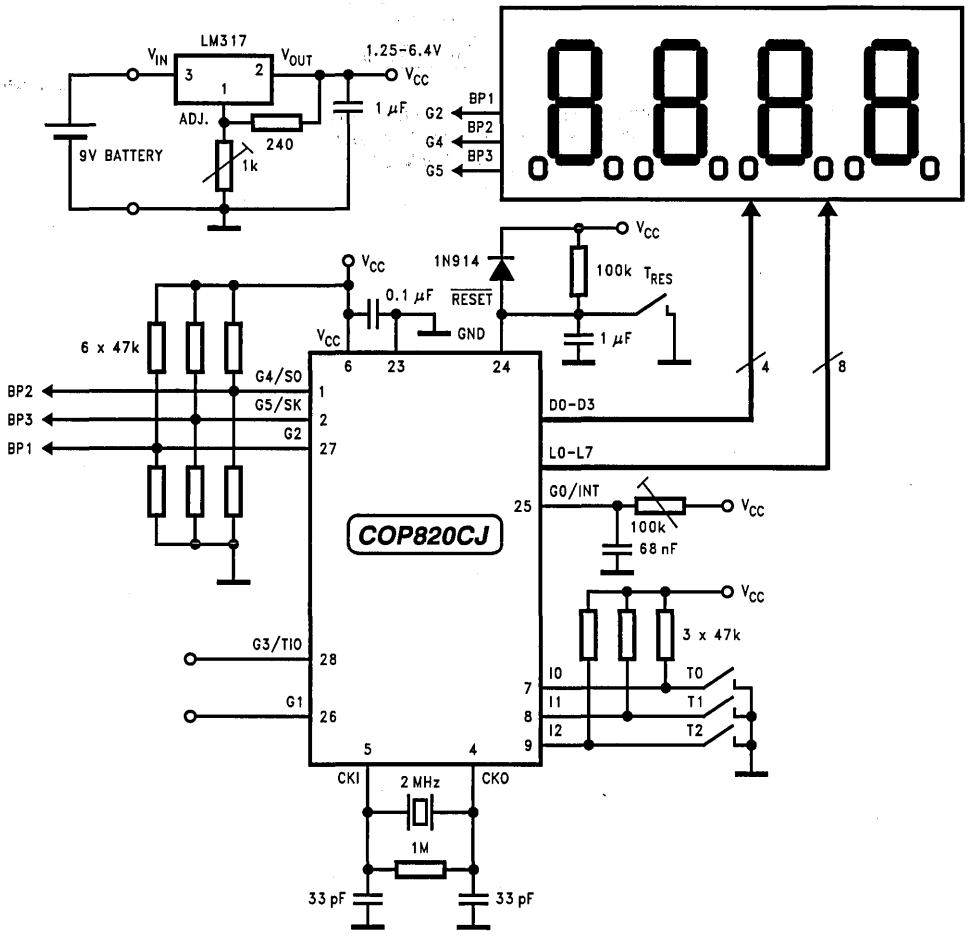
There are many applications which use a microcontroller in combination with a Liquid Crystal Display. The normal method to control a LCD panel is to connect it to a special LCD driver device, which receives the display data from a microcontroller. A cheaper solution is to drive the LCD directly from the microcontroller. With the flexibility of a COP8 microcontroller the multiplexed LCD direct drive is possible. This application note shows a way how to drive a three way multiplexed LCD with up to 36 segments using a 28-pin COP800 device.

ABOUT MULTIPLEXED LCD'S

There is a wide variety of LCD's, ranging from static devices to multiplexed versions with multiplex rates of up to 1:256.

The multiplex rate of a LCD is determined by the number of its backplanes (segment-common planes). The number of segments controlled by one line (with one segment pin) is equal to the number of backplanes on the LCD. So, a three way multiplexed LCD has three backplanes and three segments are controlled with one segment pin. For example in a three way multiplexed LCD with three segment inputs (SA, SB, SC) one can drive a 7-segment digit plus two special segments.

These are $3 \times 3 = 7 + 2 = 9$ segments. The special segments can have an application specific image. ("+", "−", ".", "mA", ... etc).



TL/DD/12076-1

FIGURE 1. Schematic for LCD Triplex Driver

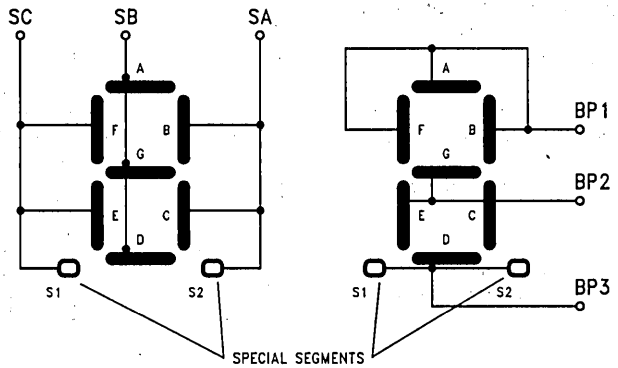


FIGURE 2. Example: Backplane-Segment Arrangement

A typical configuration of a triplex LCD is a four digit display with 8 special segments (thus having a total of 36 segments). Fifteen outputs of the COP8 are needed; **4 × 3 segment** pins and **3 backplane** pins.

Common to all LCD's is that the voltage across backplane(s) and segment(s) has to be an AC-voltage. This is to avoid electrochemical degradation of the liquid crystal layer. A segment being "off" or "on" depends on the **r.m.s.** voltage across a segment.

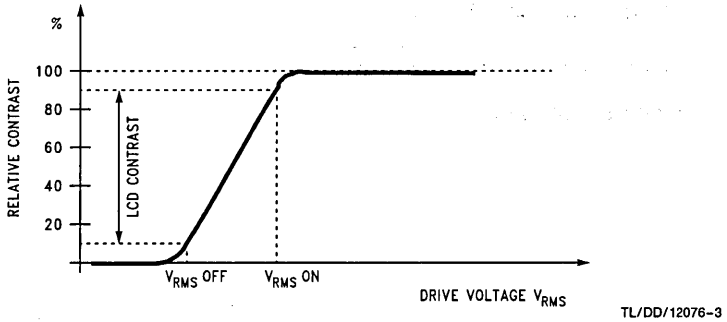
The maximum attainable ratio of "on" to "off" r.m.s. voltage (discrimination) is determined by the multiplex ratio. It is given by:

$(V_{ON}/V_{OFF})max = SQR((SQR(N) + 1)/(SQR(N) - 1))$

N is the multiplex ratio.

The maximum discrimination of a 3 way multiplexed LCD is 1.93, however, it is also possible to order a customized display with a smaller ratio. With the approach used in this application note, it may not be possible to acheive the optimum contrast acheived with a standard 3 way muxed driver. As a result of decreased discrimination (1.93 to 1.73) the user may have to live with a tighter viewing angle and a tighter temperature range.

In this application you get a **VrmsOFF** voltage of 0.408*Vop and a **VrmsON** voltage of 0.707*Vop. Vop is the operating voltage of the LCD. Typical Vop values range from 3V–5V. With the optoelectrical curve of the LCD you can evaluate the maximum contrast of the LCD by calculating the difference between the relative "OFF" contrast and the relative "ON" contrast.



In this example:

VrmsON = 0.707*Vop

VrmsOFF = 0.408*Vop

FIGURE 3. Example Curve: Contrast vs r.m.s. Drive Voltage

The backplane signals are generated with the voltage steps **0V, Vop/2** and **Vop** at the backplanes; also see *Figure 4.*

Two resistors are necessary for each backplane to establish all these levels.

The backplane connection scheme is shown in *Figure 1.*

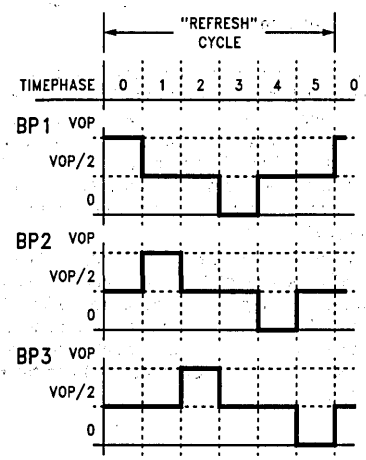
The Vop/2 level is generated by switching the appropriate COP's port pin to Hi-Z.

The following timing considerations show a simple way how to establish a discrimination ratio of 1,732.

TIMING CONSIDERATIONS

A Refresh cycle is subdivided in 6 timephases. *Figure 4* shows the timing for the backplanes during the equal distant timephases 0 . . . 5.

Backplane Control



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Note: After timephase 5 is over the backplane control timing starts with timephase 0 again.

FIGURE 4. Backplane Timing

While the backplane control timing continuously repeats after 6 timephases, the segment control depends on the combination of segments just being activated.

TABLE I. Possible Segment ON/OFF Variations

Tiphtab Address	Segment A	Segment B	Segment C
0	off	off	off
1	on	off	off
2	off	on	off
3	on	on	off
4	off	off	on
5	on	off	on
6	off	on	on
7	on	on	on

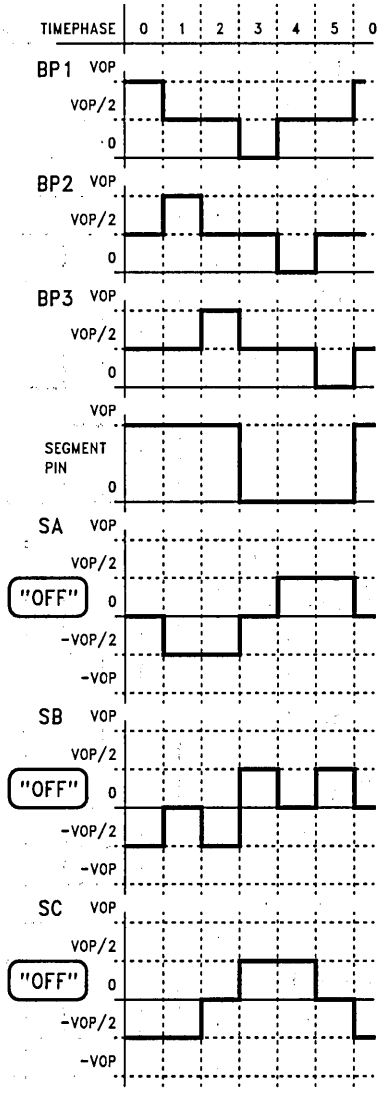
Figure 5 through *Figure 12* below show all possible combinations of controlling a **"Segment Triple"** with help of the 3 backplane connections and one segment pin. The segment switching has to be done according to the ON/OFF combination required (see also Table I).

Each figure shows in the first 3 graphs the constant backplane timing.

The 4th graph from the top shows the segment control timing necessary to switch the 3 segments (SA/SB/SC), activated from one pin, in the eight possible ways.

The 3 lower graphs show the resulting r.m.s. voltages across the 3 segments (SA, SB, SC).

Segment/Backplane Control-Timing



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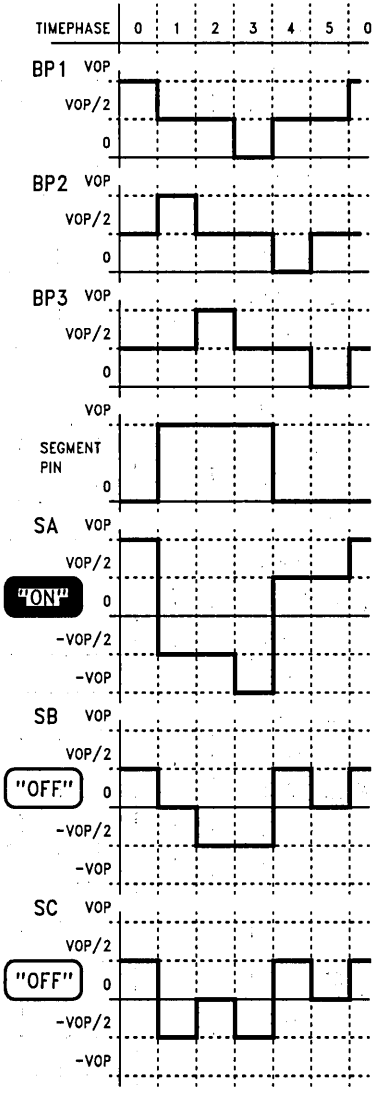
tiphtab address = 0

FIGURE 5



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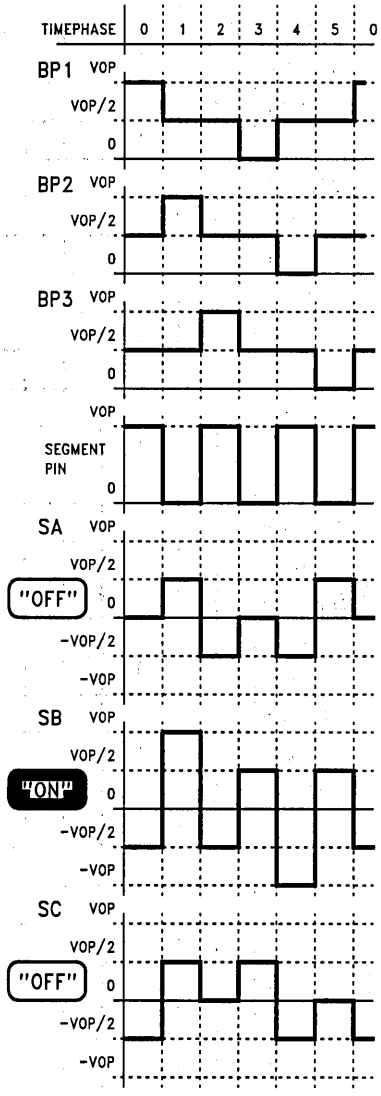
tiphtab address = 1

FIGURE 6

Segment/Backplane Control-Timing



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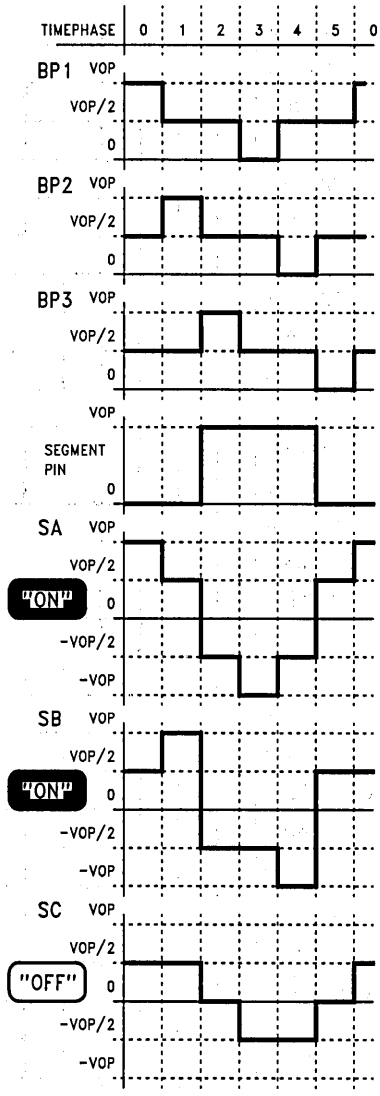
tiphtab address = 2

FIGURE 7



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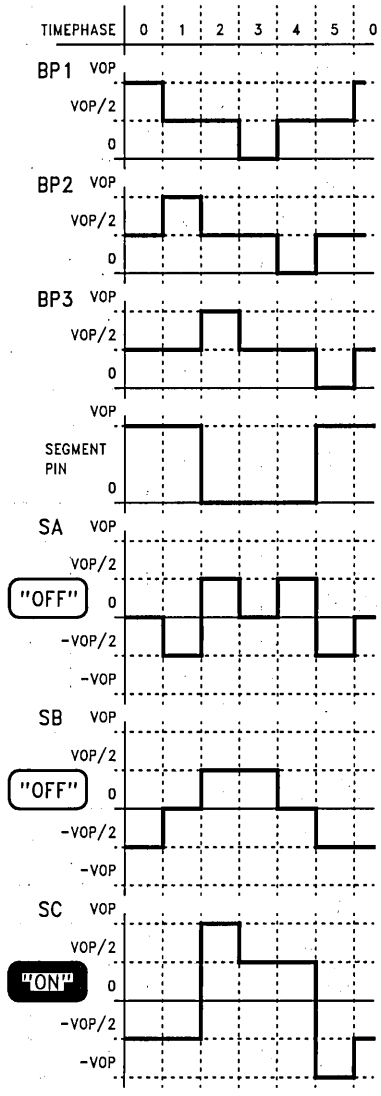
tiphtab address = 3

FIGURE 8

Segment/Backplane Control-Timing



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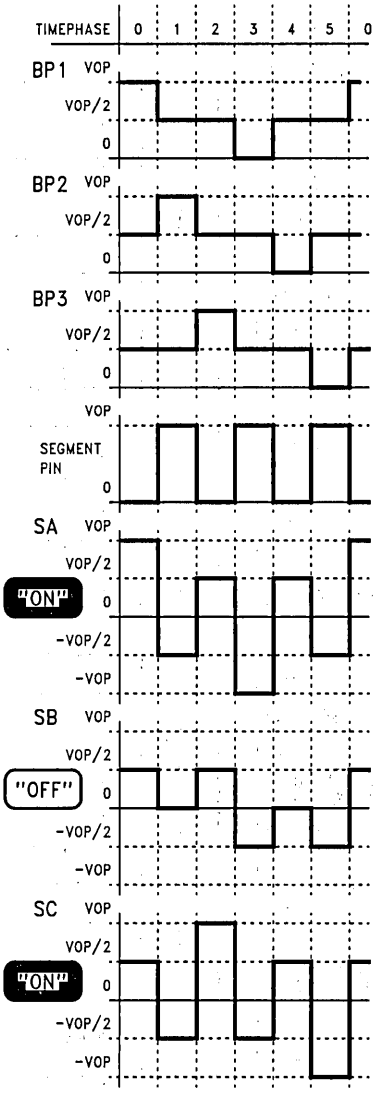
tiphtab address = 4

FIGURE 9



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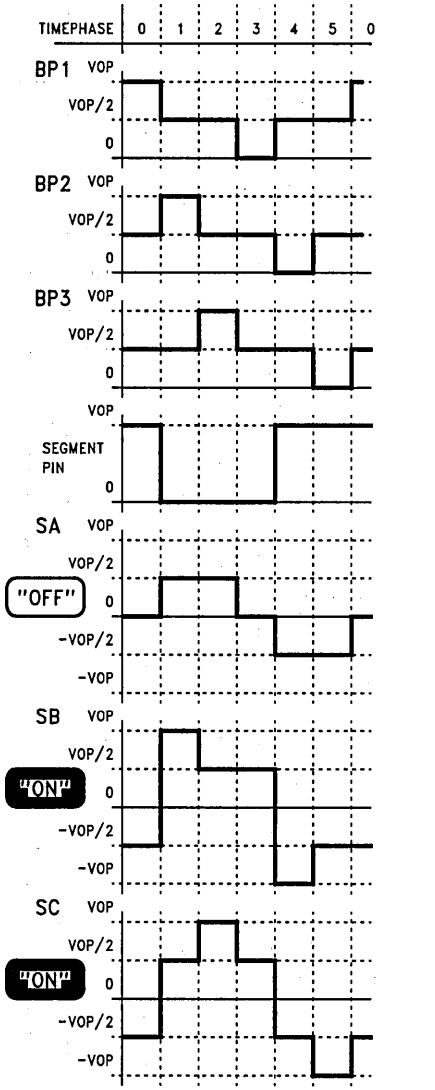
tiphtab address = 5

FIGURE 10

Segment/Backplane Control-Timing



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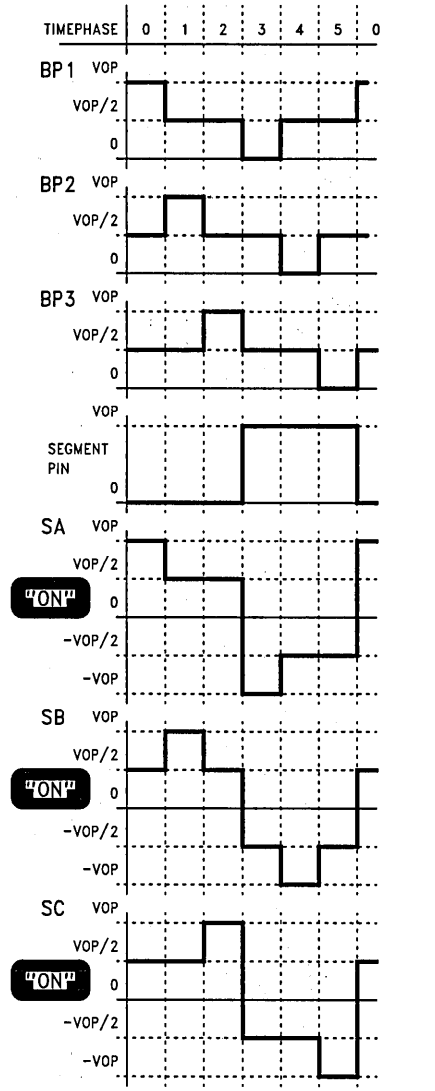
tiphtab address = 6

FIGURE 11



TL/DD/12076-12

tiphtab address = 7

FIGURE 12

REFRESH FREQUENCY

One period with six timephases is called a **refresh cycle** (also see *Figure 4*).

The refresh cycle should be in a frequency range of 30 ... 60 Hz. A frequency below 30 Hz will cause a flickering display. On the other hand, current consumption increases with the LCD's frequency. So it is also recommended to choose a frequency below 60 Hz.

In order to periodically update the µC's port pins (involved in backplane or segment control) at the beginning of a new timephase, the COP8 needs a timebase of typ. 4 ms which is realized with an external RC-circuit at the G0/INT pin.

The G0 pin is programmable as input (Schmitt Trigger). The conditions for the external interrupt could be set for a low to high transition on the G0 pin setting the IPND-flag (external interrupt pending flag) upon an occurrence of such a transition. The external capacitor can be discharged, with the G0 pin configured as Push/Pull output and programmed to "0". When, switching G0 as input the Cap. will be charged through the resistor, until the threshold voltage of the Schmitt-Trigger input is reached. This triggers the external interrupt. The first thing the interrupt service routine has to do is to discharge the capacitor and switch G0 as input to restart the procedure.

This timing method has the advantage, that the timer of the device is free for other tasks (for example to do an A/D conversion).

The time interval between two interrupts depends on the RC circuit and the threshold of the G0 Schmitt Trigger V_{TH}.

The refresh frequency is independent of the clock frequency provided to the COPs device.

The variations of "threshold" levels relative to V_{CC} (over process) are as follows:

$$(V_{TH}/V_{CC})\ \text{min} = 0.376$$

$$(V_{TH}/V_{CC})\ \text{max} = 0.572$$

at V_{CC} = 5V

Charge Time:

$$T = -(\ln(1-V_{TH}/V_{CC})*RC)$$

To prevent a flickering display one should aim at a minimum refresh frequency of f_{refr} = 30 Hz. This means an interrupt frequency of f_{int} = 6 × 30 Hz = 180 Hz. So, the maximum charge up time T_{max} must not exceed 5.5 ms (T_{min} = 2.78 ms).

With the formula:

$$RC_{max} = T_{max}/(-\ln(1-(V_{TH}/V_{CC})max)) = 5.5\ ms \times 0.849$$

$$RC_{max} = 6.48\ ms$$

$$(RC_{min} = 5.98\ ms)$$

The maximum RC time-constant is calculated. The minimum RC time constant can be calculated similarly.

A capacitor in the nF-range should be used (e.g. 68 nF), because a bigger one needs too much time to discharge. To discharge a 68 nF Cap., the G0 pin of the device has to be low for about 40 µs.

On the other hand the capacitor should be large enough to reduce noise susceptibility.

When the RC combination is chosen, one can calculate the maximum refresh frequency by using the minimum values of the RC constant and the minimum threshold voltage:

$$T_{min} = RC_{min}*(-\ln(1-(V_{TH}/V_{CC})min = RC_{min}*0.472$$

and

$$f_{refr,max} = f_{int,max}/6 = 1/(T_{min}*6)$$

In the above example one timephase would be minimum 2.82 ms long. This means that about 250 instructions could be executed during this time.

SOFTWARE

The software for the triplex LCD drive-demo is composed of three parts:

1. The initialization routine is executed only once after resetting the device, as part of the general initialization routine of the main program. The function of this routine is to **configure the ports, set the timephase counter (tiphase) to zero, discharge the external capacitor and enable the external interrupt.**

The initialization routine needs 37 bytes ROM.

Figure 13 shows the flowchart of this routine.

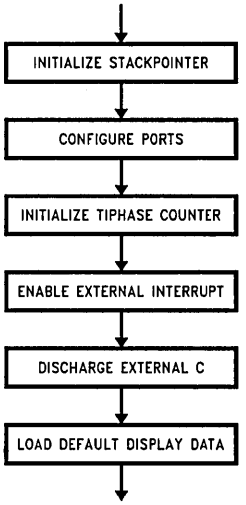


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FIGURE 13. Flowchart for Initialization Routine

2. The update routine calculates the port-data for each timephase according to the BCD codes in the RAM locations **'digit1' ... 'digit4'** and the **special segments**. This routine is only called if the display image changes.

The routine converts the BCD code to a list **1st**, which is used by the refresh routine. *Figure 14* gives an overview and illustrates the data flow in this routine.

In *Figure 15* the data flow chart is filled with example data according to the display image in *Figure 16*.

First the routine creates the **seg1st** (4 bytes long), which contains the "on/off" configuration of each segment of the display. The display has 36 segments but the 4 bytes have only 32 bits, so the four special segments **S1** are stored in the **specbuf** location. The **bcdsegtab** table (in ROM) contains the LOOK-UP data for all possible Hex numbers from **0 to F**.

The routine takes three bits at the beginning of each time-phase from the **seg1st**.

These 3 bits address the 8 bytes of the **tiphtab** table in ROM. Each byte of this table contains the **time curve** for a segment pin (only 6 bits out of 8 are used).Using this information, the program creates the lists **for port D and port L (pod1st, pol1st)**. Every byte of this list contains the **timing representatives** for the pins D0–D3 and L0–L7, to allow an easy handling of the refresh routine.

The external interrupt has to be disabled while the **copy** routine is working, because the mixed data of two different display images would result in improper data on the display. *Figure 17* shows the flowchart of the **update** routine. The Flowchart of the **convert** subroutine is shown in *Figure 18*.

MEMORY REQUIREMENTS

ROM: 152 bytes incl. look up tables

RAM: 43 bytes (*Figure 15* illustrates the RAM locations)

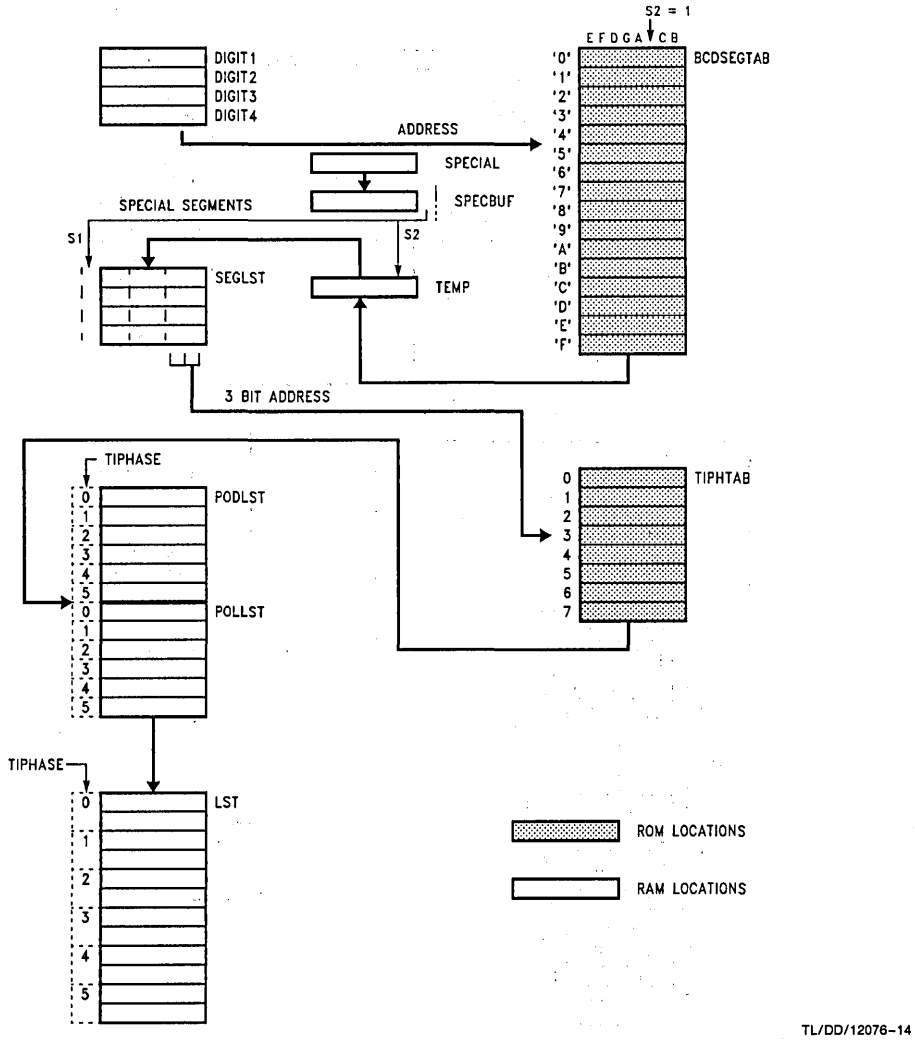

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FIGURE 14. Data Flow Chart for Update Routine

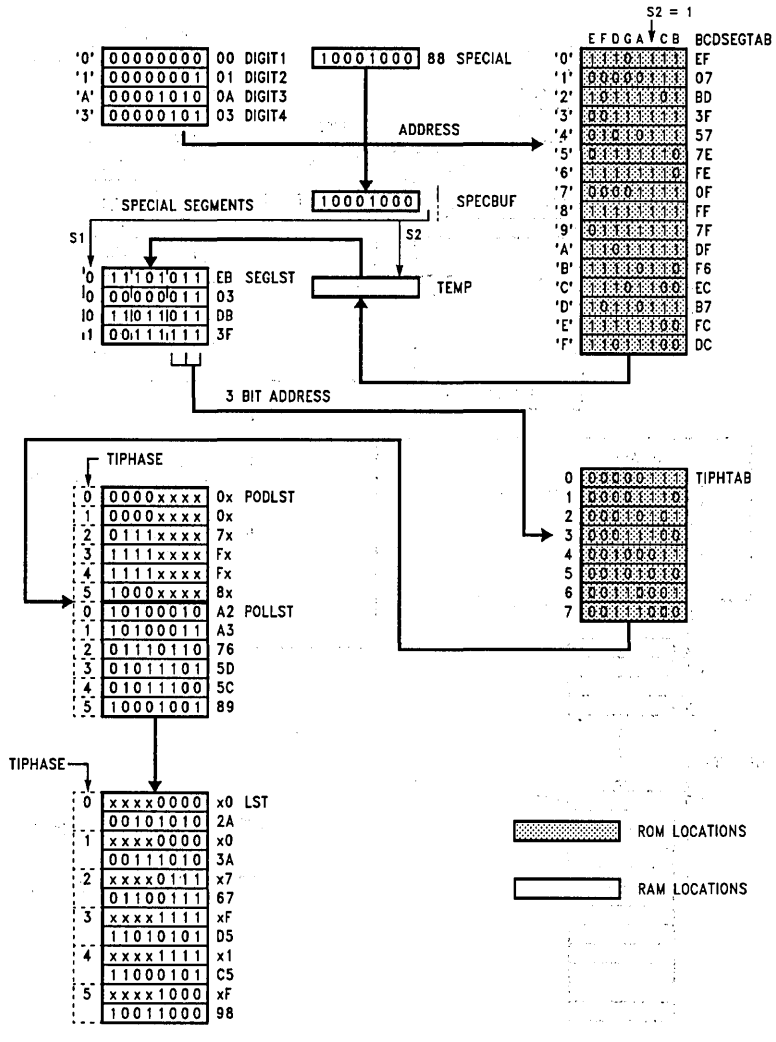

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FIGURE 15. Data Flow Chart for Update Routine

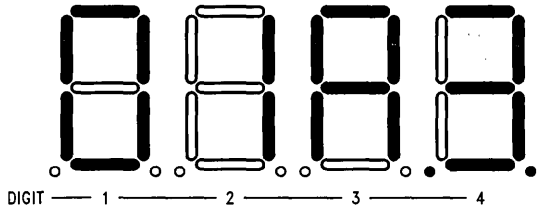

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FIGURE 16. Display Example

3. The refresh routine is the interrupt service routine of the external interrupt and is invoked at the beginning of a new timephase. First the routine discharges the external capacitor and switches the G0/INT pin back to the input mode, to initialize the next timephase. The backplane ports G2, G4 and G5 and the segment pin ports D and L are updated by this routine according to the actual timephase. For the backplanes the data are loaded from the **bptab** table in ROM.

Table II shows how the **bptab** values are gathered. *Figure 20* shows the flowchart for the refresh routine.

TIME REQUIREMENTS

The routine runs max. 150 cycles.

For a non flickering display, the refresh frequency must be 30 Hz minimum. One refresh cycle has six timephases and is max. 33 ms long. So each timephase is 5.5 ms long. With an oscillator (CKI) frequency of 2 MHz, one instruction cycle takes 1/(2 MHz/10) = 5 μs to execute. During one timephase the controller can execute:

5.5 ms/5 μs = 1100 cycles. So the refresh routine needs 134/1100 = 0.122 = 12.2% of the whole processing time (in this case).

With a refresh frequency of 50 Hz the routine needs about 20.1% of the whole processing time.

The refresh routine needs about **103** ROM bytes.

TABLE II. Phase Values

Tiphase	G5	G4	G2	Portg Data	Hex	Portg Config.	Hex
0	0/0	0/0	1/1	XX00X1XX	04	XX00X1XX	04
1	0/0	1/1	0/0	XX01X0XX	10	XX01X0XX	10
2	1/1	0/0	0/0	XX10X0XX	20	XX10X0XX	20
3	0/0	0/0	0/1	XX00X0XX	00	XX00X1XX	04
4	0/0	0/1	0/0	XX00X0XX	00	XX01X0XX	10
5	0/1	0/0	0/0	XX00X0XX	00	XX10X0XX	20

data/configuration register of portg

0/0 : Hi-Z input
0/1 : output low
1/1 : output high

SUMMARY OF IMPORTANT DATA

LCD type:	3 way multiplexed
Amount of segments:	36
V_{OP} = (V_{CC}) (range):	2.5V to 6V
Oscillator frequency:	2 MHz (typ.)
Instruction cycle time:	5 μs
ROM requirements:	
init routine:	37 bytes
update routine:	152 bytes
refresh routine:	103 bytes
total:	292 bytes
RAM requirements:	
permanent use:	25 bytes
temporary use:	18 bytes
stack:	6 bytes
total:	49 bytes
	(also see *Figure 19*)
Timer:	not used
External interrupt:	with RC circuit used as time-base generator
Ports D, L:	used for LCD control
Port G:	3 G-pins are still free for other purposes +
Port I:	can be used as key-inp.

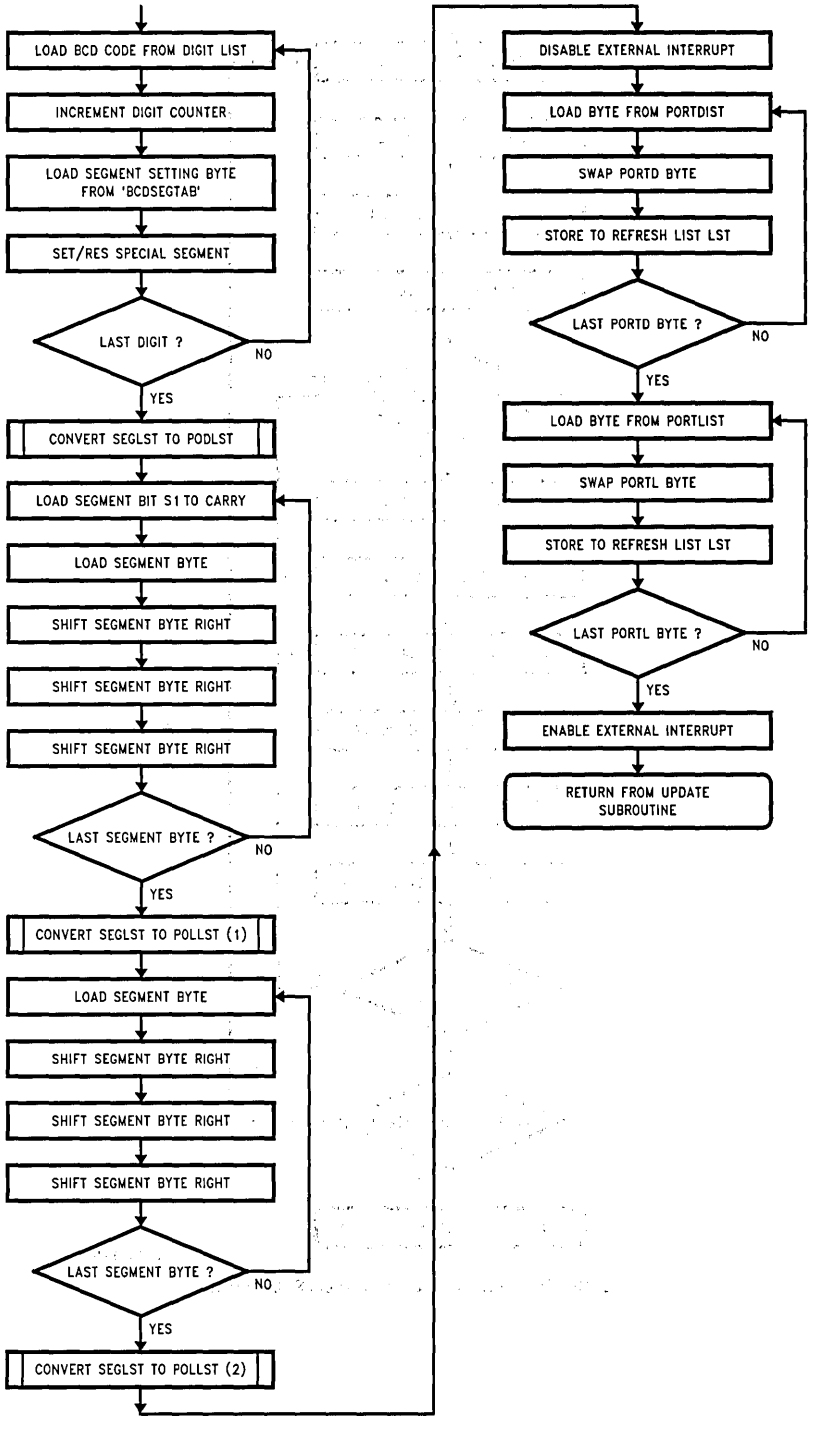

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FIGURE 17. Flowchart for Update Routine

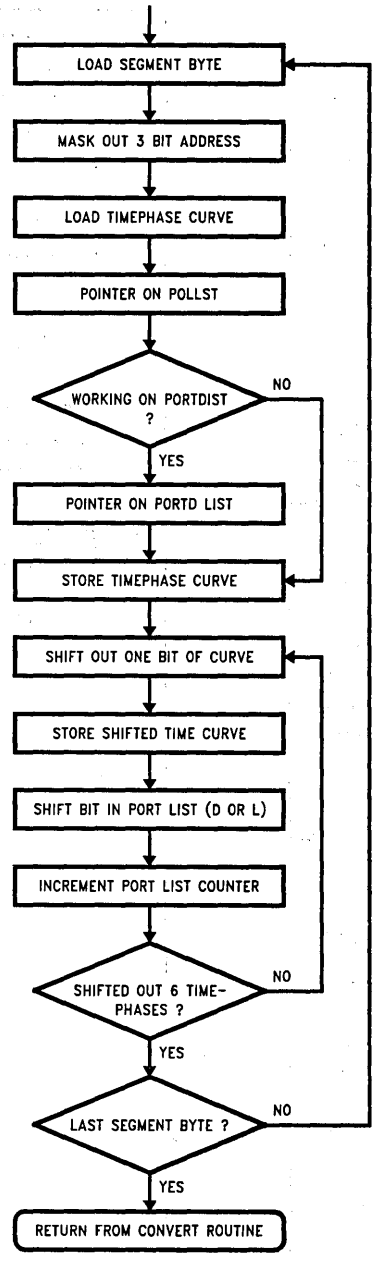

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FIGURE 18. Flowchart for Convert Subroutine

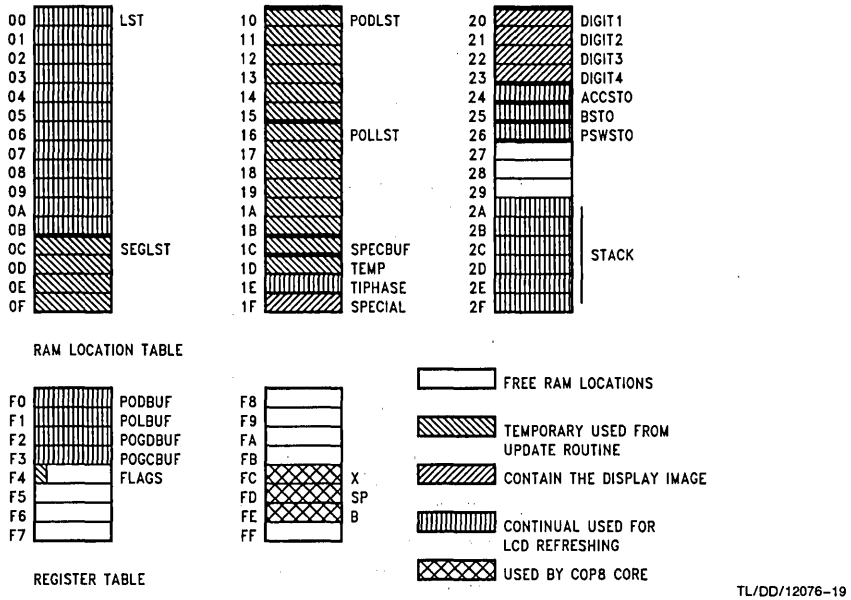

FIGURE 19. RAM Assignment

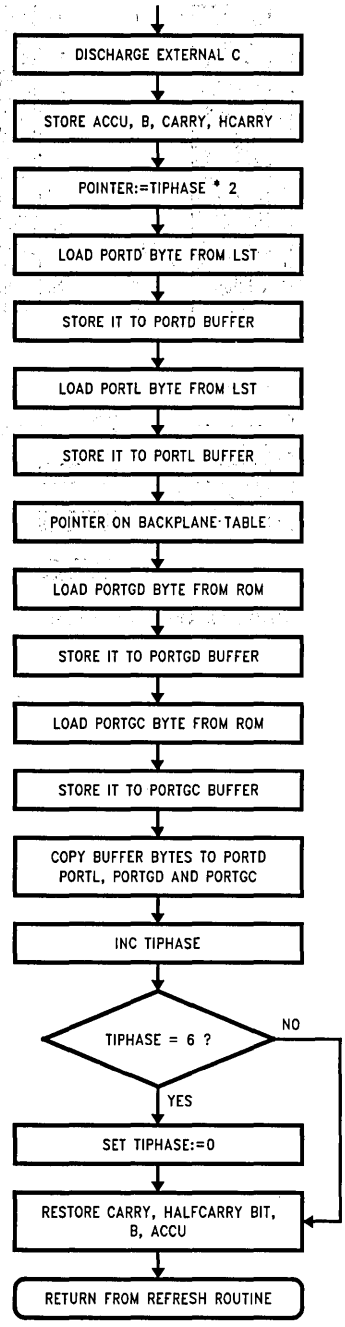

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FIGURE 20. Flowchart for Refresh-Routine

Listing

```
;   DEMO FOR COP820CJ:
;   3 WAY MULTIPLEXED LCD DRIVER DEMO
;   CONSTANT DISPLAY "01A3" and two special segments on

                .incld cop820cj.inc

;RAM assignments

                tiphase=01E
                special=01F             ;this byte must contain the
                                        ;on/off configuration of
                                        ;the extra segments
                                        ;('-','low bat',etc.)

                digit1=020              ;in these RAM locations the
                digit2=021              ;BCD code of the display
                digit3=022              ;digits are stored.
                digit4=023              ;

                accsto=024              ;accu buffer used during
                                        ;interrupt service routine
                bsto=025                ;b buffer
                pswsto=026              ;psw buffer

;register definition:

                podbuf=0f0              ;portd buffer
                polbuf=0f1              ;portl buffer
                pogdbuf=0f2             ;portgd buffer
                pogcbuf=0f3             ;portgc buffer
                flags=0f4               ;flag byte for podfla

;flag definition in flags byte

                podfla=07

;************** initialization routine ******************************

init:

                ld sp,#02f              ;initialize stackpointer

                ld portlc,#0ff          ;port l output
                ld portgc,#037          ;port g:G1,G2,G4,G5  are
                                        ;outputs
                ld portgd,#00           ;all outputs low, all
                                        ;inputs Hi-Z
                                        ;C at G0 is discharged
                ld tiphase,#00          ;begin with timephase 0
                ld psw,#002             ;ext. interrupt enable
```

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```
begin:          sbit #gie,psw           ;interrupts are welcome now
                rbit #00,portgc         ;now the external C can be
                                        ;charged
                ld b,#special
                ld [b+],#088            ;two special segments
                                        ;are 'ON'

                                        ;display:"01A3"
                ld [b+],#00             ;digit1
                ld [b+],#001            ;digit2
                ld [b+],#00A            ;digit3
                ld [b],#003             ;digit4

;************** main program ************************************
loop:
                jsr update
                jp loop

;************** update subroutine *******************************

;RAM definitions:

                specbuf=01C             ;buffer for 'special'
                temp=01D                ;temporary used

;pointer on tables:

                podlst=010              ;adress of list for port d
                pollst=016              ;adress of list for port l
                lst   =000              ;main list for display
                                        ;routine to refresh
                                        ;port d,l each timephase

                seglst=00C              ;this list contains the
                                        ;on/off configuration of
                                        ;the segments

                .=0200
                .local
update:
                ld a,special            ;load 'special' register
                x a,specbuf             ;to the buffer 'specbuf'
                ld x,#seglst            ;x points the segmentlist
                ld b,#digit1            ;b points digitlist

nxtdig:         ld a,[b+]               ;load BCD code of
                                        ;current digit
                add a,#L(bcdsegtab)     ;set pointer on look up
                                        ;table for segment setting
                laid                    ;load segment data of
                                        ;current digit
                x a,temp                ;store it to RAM
                ld a,specbuf            ;load special bit
                rrc a                   ;to carry
```

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```
                x a,specbuf             ;prepare for next
                                        ;special segment
                ifnc                    ;special bit not set ?
                rbit #2,temp            ;then reset it in the
                                        ;temp byte
                ld a,temp               ;store temp
                x a,[x+]                ;to the seglst list
                ifbne #04               ;if not last digit
                jp nxtdig               ;load data for next digit

                sbit #podfla,flags      ;set flag for working at
                                        ;port d list
                jsr convert             ;convert 3 bits from the
                                        ;segment bytes to the
                                        ;timephaselist for portd


;shift with carry

shwc:
                ld b,#seglst            ;b points seglst
nxtshwc:        ld a,specbuf            ;load special segment bit
                rrc a                   ;to carry
                x a,specbuf             ;prepare for next
                                        ;special segment
                ld a,[b]                ;shift the segmentbyte
                rrc a                   ;three positions right
                rrc  a                  ;and append the special
                                        ;segment bit
                rrc  a                  ;
                x a,[b+]                ;store shifted byte
                ifbne #00               ;end of segment list
                                        ;not reached ?
                jp nxtshwc              ;then shift the next
                                        ;segment byte

                rbit #podfla,flags      ;reset flag for working
                                        ;at port 1 list
                jsr convert             ;convert 3 bits of the
                                        ;segment bytes to the
                                        ;timephaselist for port 1
;shift (without carry)

shift:          ld b,#seglst            ;b points segmnet list
nxtshift:       ld a,[b]                ;load segment byte
                rrc a                   ;shift the segmentbyte
                rrc a                   ;three positions right
                rrc a                   ;
                x a,[b+]                ;store shifted byte
                ifbne #00               ;end of segment list
                                        ;not reached ?
                jp nxtshift             ;then shift the next
                                        ;segment byte
```

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```
                jsr convert             ;convert 3 bits of the
                                        ;segment bytes to the
                                        ;timephaselist for port 1

;copy portdata to the list on which the refresh routine will access

copy:
                rbit #eni,psw           ;disable interrupt to
                                        ;prevent fail display
                ld b,#podlst            ;b points podlst
                ld x,#lst               ;x points refresh list
nxtd:           ld a,[b+]               ;load portbyte
                swap a                  ;swap it
                x a,[x+]                ;store it to refresh list
                ld a,[x+]               ;increment x
                ifbne #06               ;if the end of the podlst
                                        ;is not reached
                jp nxtd                 ;then next timephase
                ld b,#pollst            ;b points pollst
                ld x,#lst               ;x points refresh list
nxtl:           ld a,[x+]               ;increment x
                ld a,[b+]               ;load portbyte
                swap a                  ;swap it
                x a,[x+]                ;store it to refresh list
                ifbne #0C               ;if the end of the pollst
                                        ;is not reached
                jp nxtl                 ;then next timephase
                sbit #eni,psw           ;refresh routine allowed
                                        ;again

                ret                     ;end of update routine

;subroutines for update routine:

convert:
                ld x,#seglst            ;x points segment list
nxtsgl:         ld a,[x+]               ;load segment byte
                and a,#007              ;mask out first three bits
                add a,#L(tiphtab)       ;pointer on timephase table
                laid                    ;load timephase curve for
                                        ;one segment pin
                ld b,#pollst            ;b points list for portd
                ifbit #podfla,flags     ;working at podlst ?
                ld b,#podlst            ;then b points on podlst

;shift timephase data according to 3 bits ( 8 combinations are
;possible with 3 segments)

tipsh:
                x a,temp                ;store timephase curve to
                                        ;temp buffer
nxtphsh:
                ld a,temp               ;load timephase curve again
                rrc a                   ;shift out one bit into
```

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```
                                        ;carry bit
                x a,temp                ;store shifted curve
                ld a,[b]                ;load portbyte
                rrc a                   ;shift in one bit from
                                        ;carry bit
                x a,[b+]                ;store shifted portbyte
                                        ;again
                ld a,#pollst            ;end of podlst ?
                ifeq a,b                ;
                jp eplst                ;then return
                ifbne #0C               ;else end of pollst
                jp nxtphsh              ;
eplst:
                ld a,#L(seglst+4)       ;if the end of the segment
                ifgt a,x                ;list is not reached
                jp nxtsg1               ;work at next segment byte
                ret


bcdsegtab:

;in this bytes are the on/off configuration of the segments
;for a digit are stored. there are only 7 bits of each byte
;the configuration of the 2 special segments is stored
;in the 'special' byte.

                .BYTE 0EF,007,0BD,03F   ;'0'...'3'
                .BYTE 057,07E,0FE,00F   ;'4'...'7'
                .BYTE 0FF,07F,0DF,0F6   ;'8'...'B'
                .BYTE 0EC,0B7,0FC,0DC   ;'C'...'F'
tiphtab:

;one pin controls 3 segments. there are 8 possible
;combinations. for each combination there is one byte.
;6 bits of one byte control the pin for each timephase.

                .BYTE 007,00E,015,01C,023,02A,031,038



;************** interrupt service routine *************************

                .=0ff
refresh:
                x a,accsto              ;store accu
                ld a,b                  ;store b
                x a,bsto                ;

                ld b,#portgd
                                        ;discharge C
                rbit #00,[b]
                ld a,[b+]               ;increment b (b=#portgc)
                sbit #00,[b]            ;by switching G0 to a
                                        ;low output
```

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```
rbit #00,[b]            ;C can be charged again
ld b,#psw
rbit #ipnd,[b]          ;reset ext. interrupt
                        ;pending flag

ld a,[b]                ;load psw
x a,pswsto              ;store psw

ld a,tiphase            ;accu:=tiphase*2
add a,tiphase           ;

x a,b                   ;store accu in b
ld a,[b+]               ;load portbyte from
                        ;refresh list('lst')
x a,podbuf              ;store it to port d buffer
ld a,[b+]               ;load portbyte
x a,polbuf              ;store it to port l buffer
ld a,b                  ;accu:=timephase*2+2
add a,#L(bptab)-2       ;accu points on
                        ;backplane table
x a,b                   ;store pointer
ld a,b                  ;
laid                    ;load port g data byte
x a,pogdbuf             ;store it to port g data
                        ;buffer
ld a,[b+]               ;increment b
ld a,b                  ;load pointer
laid                    ;load portg conf. byte
x a,pogcbuf             ;store it to buffer


ld b,#podbuf            ;b points buffer list
ld a,[b+]               ;
x a,portd               ;refresh port d
ld a,[b+]               ;
x a,portld              ;refresh port l

ld portgc,#00           ;all backplane wires on
                        ;Vop/2 level to prevent
                        ;spikes

ld a,[b+]               ;
x a,portgd              ;refresh port g data
ld a,[b+]               ;
x a,portgc              ;refresh port g config.

ld a,tiphase            ;update timephase counter
inc a                   ;
ifeq a,#06              ;tiphase = 0..5
ld a,#00                ;
x a,tiphase             ;
ld b,#pswsto
rc                      ;restore carry bit
ifbit #07,[b]           ;
```

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```
                sbit #07,psw
                ifbit #06,[b]           ;restore halfcarry bit
                sbit #06,psw            ;

                ld a,bsto               ;restore b
                x a,b                   ;
                ld a,accsto             ;restore accu


                reti                    ;return from lcd
                                        ;refresh routine

bptab:          .BYTE 004,004,010,010,020,020
                .BYTE 000,004,000,010,000,020

                .END
```

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DTMF Generation with a 3.58 MHz Crystal

National Semiconductor
Application Note 666
Verne H. Wilson

DTMF (Dual Tone Multiple Frequency) is associated with digital telephony, and provides two selected output frequencies (one high band, one low band) for a duration of 100 ms. DTMF generation consists of selecting and combining two audio tone frequencies associated with the rows (low band frequency) and columns (high band frequency) of a push-button touch tone telephone keypad.

This application note outlines two different methods of DTMF generation using a COP820C/840C microcontroller clocked with a 3.58 MHz crystal in the divide by 10 mode. This yields an instruction cycle time of 2.79 μs. The application note also provides a low true row/column decoder for the DTMF keyboard.

The first method of DTMF generation provides two PWM (Pulse Width Modulation) outputs on pins G3 and G2 of the G port for 100 ms. These two PWM outputs represent the selected high band and low band frequencies respectively, and must be combined externally with an LM324 op amp or equivalent feed back circuit to produce the DTMF signal.

The second method of DTMF generation uses ROM lookup tables to simulate the two selected DTMF frequencies. These table lookup values for the selected high band and low band frequencies are then combined arithmetically. The high band frequencies contain a higher bias value to compensate for the DTMF requirement that the high band frequency component be 2 dB above the low band frequency component to compensate for losses in transmission. The resultant value from the arithmetic combination of sine wave values is output on L port pins L0 to L5, and must be combined externally with a six input resistor ladder network to produce the DTMF signal. This resultant value is updated every 118 μs. The COP820C/840C timer is used to time out the 100 ms duration of the DTMF. A timer interrupt at the end of the 100 ms is used to terminate the DTMF output. The external ladder network need not contain any active components, unlike the first method of DTMF generation with the two PWM outputs into the LM324 op amp.

The associated COP820C/840C program for the DTMF generation is organized as three subroutines. The first subroutine (KBRDEC) converts the low true column/row input from the DTMF keyboard into the associated DTMF hexadecimal digit. In turn, this hex digit provides the input for the other two subroutines (DTMFGP and DTMFLP), which represent the two different methods of DTMF generation. These three subroutines contain 35, 94, and 301 bytes of COP820C/840C code respectively, including all associated ROM tables. The Program Code/ROM table breakdowns are 19/16, 78/16, and 88/213 bytes respectively.

DTMF KEYBOARD MATRIX

The matrix for selecting the high and low band frequencies associated with each key is shown in *Figure 1*. Each key is uniquely referenced by selecting one of the four low band frequencies associated with the matrix rows, coupled with selecting one of the four high band frequencies associated with the matrix columns. The low band frequencies are 697 Hz, 770 Hz, 852 Hz, and 941 Hz, while the high band frequencies are 1209 Hz, 1336 Hz, 1477 Hz, and 1633 Hz. The DTMF keyboard input decode subroutine assumes that the keyboard is encoded in a low true row/column format, where the keyboard is strobed sequentially with four low true column selects with each returning a low true row select. The low true column and row selects are encoded in the upper and lower nibbles respectively of the accumulator, which serves as the input to the DTMF keyboard input decode subroutine. The subroutine will then generate the DTMF hexadecimal digit associated with the DTMF keyboard input digit.

The DTMF keyboard decode subroutine (KBRDEC) utilizes a common ROM table lookup for each of the two nibbles representing the low true column and row encodings for the keyboard. The only legal low true nibbles for a single key input are E, D, B, and 7. All other low true nibble values represent multiple keys, no key, or no column strobe. Results from two legal nibble table lookups (from the same 16 byte ROM table) are combined to form a hex digit with the binary format of 0000RRCC, where RR represents the four row values and CC represents the four column values. The illegal nibbles are trapped, and the subroutine is exited with a RET (return) command to indicate multiple keys or no key. A pair of legal nibble table lookups result in the subroutine being exited with a RETSK (return and skip) command to indicate a single key input. This KBRDEC subroutine uses 35 bytes of code, consisting of 19 bytes of program code and 16 bytes of ROM table.

DTMF GENERATION USING PWM AND AN OP AMP

The first DTMF generation method (using the DTMFGP subroutine) generates the selected high band and low band frequencies as PWM (Pulse Width Modulation) outputs on pins G3 and G2 respectively of the G port. The COP820C/840C microcontrollers each contain only one timer, and three times must be generated to satisfy the DTMF application. These three times are the half periods of the two selected frequencies and the 100 ms duration period. Obviously the single timer can only generate one of the required times, while the program must generate the two remaining times. The solution lies in dividing the 100 ms duration time by the half periods for each of the eight DTMF frequencies, and then examining the respective high band and low band quotients and remainders. Naturally these divisions must be normalized to the instruction cycle time (t_C). 100 ms represents 35796 t_C's. The results of these divisions are detailed in Table I.

The four high band frequencies are produced by running the COP820C/840C timer in PWM (Pulse Width Modulation) mode, while the program produces the four low band frequencies and the 100 ms duration timeout. The programmed times are achieved by using three programmed register counters R0, R2 and R3, with a backup register R1 to reload the counter R0. These three counters represent the half period, the 100 ms quotient, and the 100 ms remainder associated with each of the four low band frequencies.

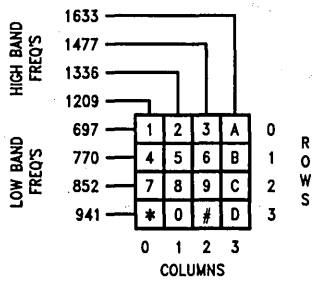

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FIGURE 1. DTMF Keyboard Matrix

TABLE I. Frequency Half Periods, Quotients and Remainders

	Freq. Hz	Half Period In μs	Half Period In t_C's	100 ms/0.5P In t_C's	
				Quotient	Remainder
Low Band Frequencies	697	717.36	257	139	73
	770	649.35	232	154	68
	852	586.85	210	170	96
	941	531.35	190	188	76
High Band Frequencies	1209	413.56	148	241	128
	1336	374.25	134	267	18
	1477	338.53	121	295	101
	1633	306.18	110	325	46

Note: 100 ms represents 35796 t_C's.

The DTMFGP subroutine starts by transforming the DTMF hex digit in the accumulator (with binary format 0000RRCC) into low and high frequency vectors with binary formats 0011RR11 and 0011CC00 respectively. The transformation of the hex digit 0000RRCC (where RR is the row select and CC is the column select) into the frequency vectors is shown in Table II. The conversion produces a timer vector 0011CC00 (T), and three programmed counter vectors for R1, R2, and R3. The formats for the three counter vectors are 0011RR11 (F), 0011RR10 (Q), and 0011RR01 (R). These four vectors created from the core vector are used as inputs for a 16 byte ROM table using the LAID (Load Accumulator InDirect) instruction. One of these four vectors (the T vector) is a function of the column bits (CC), while the other three vectors (F, Q, R) are a function of the row bits (RR). This correlates to only one parameter being needed for the timer (representing the selected high band frequency), while three parameters are needed for the three counters (half period, 100 ms quotient, 100 ms remainder) associated with the low band frequency and 100 ms duration. The frequency parameter ROM translation table, accessed by the T, F, Q, and R vectors, is shown in Table III.

TABLE II. DTMF Hex Digit Translation

DTMF Hex Digit— 0000RRCC

Timer Vector	Timer	T	0011CC00
Half Period Vector	R1	F	0011RR11
100 ms Quotient Vector	R2	Q	0011RR10
100 ms Remainder Vector	R3	R	0011RR01

TABLE III. Frequency Parameter ROM Translation Table

T— Timer F— Frequency Q— Quotient R— Remainder

Address	Data (Decimal)	Vector
0x30	147	T
0x31	10	R
0x32	140	Q
0x33	38	F
0x34	133	T
0x35	9	R
0x36	155	Q
0x37	33	F
0x38	120	T
0x39	14	R
0x3A	171	Q
0x3B	31	F
0x3C	109	T
0x3D	10	R
0x3E	189	Q
0x3F	26	F

The theory of operation in producing the selected low band frequency starts with loading the three counters with values obtained from a ROM table. The half period for the selected frequency is counted out, after which the G2 output bit is toggled. During this half period countout, the quotient counter is decremented. This procedure is repeated until the quotient counter counts out, after which the program branches to the remainder loop. During the remainder loop, the remainder counter counts out to terminate the 100 ms. Following the remainder countout, the G2 and G3 bits are both reset, after which the DTMF subroutine is exited. Great care must be taken in time balancing the half period loop for the selected low band frequency. Furthermore, the toggling of the G2 output bit (achieved with either a set or reset bit instruction) must also be exactly time balanced to maintain the half period time integrity. Local stall loops (consisting of a DRSZ instruction followed by a JP jump back to the DRSZ for a two byte, six instruction cycle loop) are embedded in both the half period and remainder loops. Consequently, the ROM table parameters for the half period and remainder counters are approximately only one-sixth of what otherwise might be expected. The program for the half period loop, along with the detailed time balancing of the loop for each of the low band frequencies, is shown in *Figure 2*.

	Program		Bytes/ Cycles	Conditional Cycles		Cycles	Total Cycles
	LD	B,#PORTGD	2/3				
	LD	X,#R1	2/3				
LUP1:	LD	A,[X−]	1/3			3	
	IFBIT	2,[B]	1/1			1	
	JP	BYP1	1/3	3	1		
	X	A,[X+]	1/3		3		
	SBIT	2,[B]	1/1		1		
	JP	BYP2	1/3		3		
BYP1:	NOP		1/1	1			
	RBIT	2,[B]	1/1	1			
	X	A,[X+]	1/3	3			
BYP2:	DRSZ	R2	1/3			3	
	JP	LUP2	1/3			3	
	JP	FINI	1/3				
LUP2:	DRSZ	R0	1/3		3	3	
	JP	LUP2	1/3		3	1	
	LD	A,[X]	1/3			3	
	IFEQ	A,#31	2/2			2	
	JP	LUP1	1/3		1	3	30
	NOP		1/1		1		
	NOP		1/1		1		
	IFEQ	A,#38	2/2		2		
	JP	LUP1	1/3	1	3		35
	LAID		1/3	3			
	NOP		1/1	1			
	JP	LUP1	1/3	3			40

Table III Frequency	Stall Loop	Total Cycles	Half Period
[(38 − 1)	× 6]	+ 35	= 257
[(33 − 1)	× 6]	+ 40	= 232
[(31 − 1)	× 6]	+ 30	= 210
[(26 − 1)	× 6]	+ 40	= 190

FIGURE 2. Time Balancing for Half Period Loop

TABLE IV. Time Balancing for Remainder Loop

Table III Remainder	Stall Loop	R Loop Overhead	Total Cycles	Table I Remainder
[(10 − 1)	× 6]	+ 20	= 74	73
[(9 − 1)	× 6]	+ 20	= 68	68
[(14 − 1)	× 6]	+ 20	= 98	96
[(10 − 1)	× 6]	+ 20	= 74	76

Note that the Q value in Table III is one greater than the quotient in Table I to compensate for the fact that the quotient count down to zero test is performed early in the half period loop. The overhead in the remainder loop is 20 instruction cycles. The detailed time balancing for the remainder loop is shown in Table IV.

The selected high band frequency is achieved by loading the half period count in t_C's minus one (from Table III) into the timer autoreload register and running the timer in PWM output mode. The minus one is necessary since the timer toggles the G3 output bit when it underflows (counts down through zero), at which time the contents of the autoreload register are transferred into the timer.

In summary, the input digit from the keyboard (encoded in low true column/row format) is translated into a digit matrix vector XXXXRRCC which is checked for 1001RRCC to indicate a single key entry. No key or multiple key entries will set a flag and terminate the DTMF subroutine. The digit matrix vector for a single key is transformed into the core vector 0000RRCC. The core vector is then translated into four other vectors (T, F, Q, R) which in turn are used to select four parameters from a 16 byte ROM table. These four parameters are used to load the timer, and the respective half period, quotient, and remainder counters. The 16 byte ROM table must be located starting at ROM location 0030 (or 0X30) in order to minimize program size, and has reference setups with the "OR A,#033" instruction for the F vector and the "OR A,#030" instruction for the T vector.

The three parameters associated with the two R bits of the core vector require a multi-level table lookup capability with the LAID instruction. This is achieved with the following section of code in the DTMF subroutine:

```
        LD      B,#R1
LUP:    X       A,[B]
        LD      A,[B,]
        LAID
        X       A,[B+]
        DEC     A
        IFBNE   #4
        JP      LUP
```

This program loads the F frequency vector into R1, and then decrements the vector each time around the loop. The vector is successively moved with the exchange commands from R1 to R2 to R3 as one of the same exchange commands loads the data from the ROM table into R1, R2, and R3. This successive decrementation of the F vector changes the F vector into the Q vector, and then changes the Q vector into the R vector. These vectors are used to access the ROM table with the LAID instruction. The B pointer is incremented each time around the loop after it has been used to store away the three selected ROM table parameters (one per loop). These three parameters are stored in sequential RAM locations R1, R2, and R3. The IFBNE test instruction is used to skip out of the loop once the three selected ROM table parameters have been accessed and stored away.

The timer is initialized to a count of 15 so that the first timer underflow and toggling of the G3 output bit (with timer PWM mode and G3 toggle output selected) will occur at the same time as the first toggling of the G2 output bit. The half period counts for the high band frequencies minus one are stored in the timer section of the ROM table. The selected value from this frequency ROM table is stored in the timer autoreload register. The timer is selected for PWM output mode and started with the instruction LD [B],#0B0 where the B pointer is selecting the CNTRL register at memory location 0EE.

This first DTMF generation subroutine for the COP820C/840C uses 94 bytes of code, consisting of 78 bytes of program code and 16 bytes of ROM table. A program test routine to sequentially call the DTMFGP subroutine for each of the 16 keyboard input digits is supplied with the listing for the DTMF35 program. This test routine uses a 16 byte ROM table to supply the low true encoded column/row keyboard input to the accumulator. An input from the I0 input pin of the I port is used to select which DTMF generation subroutine is to be used. The DTMFGP subroutine is selected with I0 = 0.

A TYPICAL OP AMP CONFIGURATION FOR MIXING THE TWO DTMF PWM OUTPUTS IS SHOWN IN *FIGURE 3*.

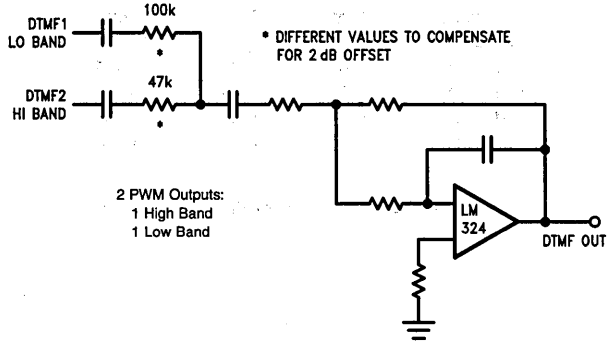

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FIGURE 3. Typical Op Amp Configuration for Mixing DTMF PWM Outputs

DTMF GENERATION USING A RESISTOR LADDER NETWORK

The second DTMF generation method (using the DTMFLP subroutine) generates and combines values from two table lookups simulating the two selected sine waves. The high band frequency table values have a higher base line value (16 versus 13) than the low band frequency table values. This higher bias for the high frequency values is necessary to satisfy the DTMF requirement that the high band DTMF frequencies need a value 2 dB greater than the low band DTMF frequencies to compensate for losses in transmission.

The resultant value from arithmetically combining the table lookup low band and high band frequency values is output on pins L0 to L5 of the L port in order to feed into a six input external resistor ladder network. The resultant value is updated every 117⅓ μs (one cycle of the LUP42 program loop). The LUP42 program loop contains 42 instruction cycles (t_C's) of 2.7936511 μs each for a total loop time of 117⅓ μs. The COP820C/840C timer is used to count out the 100 ms DTMF duration time.

An interrupt from the timer terminates the 100 ms DTMF output. Note that the Stack Pointer (SP) must be adjusted following the timer interrupt before returning from the DTMFLP subroutine.

The DTMFLP subroutine starts by quadrupling the value of the DTMF hex digit value in the accumulator, and then adding an offset value to reach the first value in the telephone key table. The telephone key ROM table contains four values associated with each of the 16 DTMF hex keys. These four values represent the low and high frequency table sizes and table starting addresses associated with the pair of frequencies (one low band, one high band) associated with each DTMF key. The FRLUP section of the program loads the four associated telephone key table values from the ROM table into the registers LFTBSZ (Low Freq Table Size), LFTADR (Low Freq Table Address), HFTBSZ (High Freq Table Size), and HFTADR (High Freq Table Address). The program then initializes the timer and autoreload register, starts the timer, and then jumps to LUP42. Note that the timer value in t_C's is 100 ms plus one LUP42 time, since the initial DTMF output is not until the end of the LUP42 program.

Multiples of the magic number 118 μs (approximately) are close approximations to all eight of the DTMF frequencies. The LUP42 program uses 42 instruction cycles (of 2.7936511 μs each) to yield a LUP42 time of 117⅓ μs. The purpose of the LUP42 program is to update the six L port outputs by accessing and then combining the next set of values from the selected low band and high band sine wave frequency tables in the ROM. The ROM table offset frequency pointers (LFPTR and HFPTR) must increment each time and then wrap around from top to bottom of the two selected ROM tables. The ROM table size parameters (LFTBSZ and HFTBSZ) for the selected frequencies are tested during each LUP42 to determine if the wrap around from ROM table top to bottom is necessary. The wrap around is implemented by clearing the frequency pointer in question. Note that the ROM tables are mapped from a reference of 0 to table size minus one, so that the table size is used in a direct comparison with the frequency offset pointer to test for the need for a wrap around. Also note that the offset pointer incremented value is used during the following LUP42 cycle, while the pre-incremented value of the pointer is used during the current cycle. However, it is the incremented value that is tested versus the table size for the need to wrap around.

After the low band and high band ROM table sine wave frequency values are accessed in each cycle of the LUP42 program, they are added together and then output to pins L0–L5 of the L port. As stated previously, the low band frequency values have a lower bias than the high band frequency values to compensate for the required 2 dB offset. Specifically, the base line and maximum values for the low frequency values are 13 and 26 respectively, while the base line and maximum values for the high frequency values are 16 and 32 respectively. Thus the combined base line value is 29, while the combined maximum value is 58. This gives a range of values on the L port output (L0–L5) from 0 to 58.

The minimum time necessary for the LUP42 update program loop is 36 instruction cycles including the jump back to the start of the loop. Consequently, two LAID instructions are inserted just prior to the jump back instruction at the end of LUP42 to supply the six extra NOP instruction cycles needed to increase the LUP42 instruction cycles from 36 to 42. A three cycle LAID instruction can always be used to simulate three single cycle NOP instructions if the accumulator data is not needed.

Table V shows the multiple LUP42 approximation to the eight DTMF frequencies, including the number of sine wave cycles and data points in the approximation. As an example, three cycles of a sine wave with a total of 19 data points across the three cycles is used to approximate the 1336 Hz DTMF frequency. The 19 cycles of LUP42 times the LUP42 time of 117⅓ μs is divided into the three cycles to yield a value of 1345.69 Hz. This gives an error of +0.73% when compared with the DTMF value of 1336 Hz. This is well within the 1.5% North American DTMF error range.

TABLE V. DTMF Frequency Approximation Table

DTMF Freq.	# of Sine Wave Cycles	# of Data Points	Calculation	Approx. Freq.	% Error
697	4	49	4/(49 x 117⅓)	= 695.73	−0.18
770	1	11	1/(11 x 117⅓)	= 774.79	+0.62
852	1	10	1/(10 x 117⅓)	= 852.27	+0.03
941	1	9	1/(9 x 117⅓)	= 946.97	+0.63
1209	1	7	1/(7 x 117⅓)	= 1217.53	+0.71
1336	3	19	3/(19 x 117⅓)	= 1345.69	+0.73
1477	4	23	4/(23 x 117⅓)	= 1482.21	+0.35
1633	4	21	4/(21 x 117⅓)	= 1623.38	−0.59

The frequency approximation is equal to the number of cycles of sine wave divided by the time in the total number of LUP42 cycles before the ROM table repeats.

The values in the DTMF sine wave ROM tables are calculated by computing the sine value at the appropriate points, scaling the sine value up to the base line value, and then adding the result to the base line value. The following example will help to clarify this calculation.

Consider the three cycles of sine wave across 19 data points for the 1336 Hz high band frequency. The first value in the table is the base line value of 16. With 2π radians per sine wave cycle, the succeeding values in the table represent the sine values of $1 \times (6\pi/19)$, $2 \times (6\pi/19)$, $3 \times (6\pi/19)$, . . . , up to $18 \times (6\pi/19)$. Consider the seventh and eighth values in the table, representing the sine values of $6 \times (6\pi/19)$ and $7 \times (6\pi/19)$ respectively. The respective calculatons of $16 \times \sin[6 \times (6\pi/19)]$ and $16 \times \sin[7 \times (6\pi/19)]$ yield values of -5.20 and 9.83. Rounding to the nearest integer gives values of -5 and 10. When added to the base line value of 16, these values yield the results 11 and 26 for the seventh and eighth values in the 1336 Hz DTMF ROM table. Symmetry in the loop of 19 values in the DTMF table dictates that the fourteenth and thirteenth values in the table are 21 and 6, representing values of 5 and -10 from the calculations.

The area under a half cycle of sine wave relative to the area of the surrounding rectangle is $2/\pi$, where π radians represent the sine wave half cycle. This surrounding rectangle has a length of π and a height of 1, with the height representing the maximum sine value. Consequently, the area of the surrounding rectangle is π. The integral of the area under the half sine wave from 0 to π is equal to 2. The ratio of $2/\pi$ is equal to 63.66%, so that the total of the values for each half sine wave should approximate 63.66% of the sum of the max values. The maximum values (relative to the base line) are 13 and 16 respectively for the low and high band DTMF frequencies.

For the previous 1336 Hz example, the total of the absolute values for the 19 sine values from the 1336 Hz ROM table is equal to 196. The surrounding rectangle for the three cycles of sine wave is 19 by 16 for a total area of 304. The ratio of 196/304 is 64.47% compared with the $2/\pi$ ratio of 63.66%. Thus the sine wave approximation gives an area abundance of 0.81% (equal to 64.47 − 63.66).

An application of the sine wave area criteria is shown in the generation of the DTMF 852 Hz frequency. The ten sine values calculated are 0, 7.64, 12.36, 12.36, 7.64, 0, −7.64, −12.36, −12.36, and −7.64. Rounding off to the nearest integer yields values of 0, 8, 12, 12, 8, 0, −8, −12, −12 and −8. The total of these values (absolute numbers) is 80, while the area of the surrounding rectangle is 130 (10 x 13). The ratio of 80/130 is 61.54% compared with the $2/\pi$ ratio of 63.66%. Thus the sine wave approximation gives an area deficiency of 2.12% (equal to 63.66 − 61.54), which is overly deficient. Consequently, two of the ten sine values are augmented to yield sine values of 0, 8, 12, 13*, 8, 0, −8, −12, −13*, and −8. This gives an absolute total of 82 and a ratio of 82/130, which equals 63.08% and serves as a much better approximation to the $2/\pi$ ratio of 63.66%.

The sine wave area criteria is also used to modify two values in the DTMF 941 Hz frequency. The nine sine values calculated are 0, 8.36, 12.80, 11.26, 4.45, −4.45, −11.26, −12.80, and −8.36. Rounding off to the nearest integer yields values of 0, 8, 13, 11, 4, −4, −11, −13, and −8. The total of these values (absolute numbers) is 72, while the area of the surrounding rectangle is 117 (9 x 13). The ratio of 72/117 is 61.54% compared to the $2/\pi$ ratio of 63.66%. Thus the sine wave approximation gives an area deficiency of 2.12% (equal to 63.66 − 61.54), which is overly deficient. Rounding up the two values of 4.45 and −4.45 to 5 and −5, rather than down to 4 and −4, yields values of 0, 8, 13, 11, 5, −5, −11, −13 and −8. This gives an absolute total of 74 and a ratio of 74/117, which equals 63.25% and serves as a much better approximation to the $2/\pi$ ratio of 63.66%.

With these modified values for the 852 and 941 DTMF frequencies, the area criteria ratio of $2/\pi$ = 63.66% for the sine wave compared to the surrounding rectangle has the following values:

DTMF Freq.	Sum of Values	Rectangle Area	Percentage	Diff.
697 Hz	406	49 x 13 = 637	63.74%	+0.08%
770 Hz	92	11 x 13 = 143	64.34%	+0.68%
852 Hz	82	10 x 13 = 130	63.08%	−0.58%
941 Hz	74	9 x 13 = 117	63.25%	−0.41%
1209 Hz	72	7 x 16 = 112	64.29%	+0.63%
1336 Hz	196	19 x 16 = 304	64.47%	+0.81%
1477 Hz	232	23 x 16 = 368	63.04%	−0.62%
1633 Hz	216	21 x 16 = 336	64.29%	+0.63%

The LUP42 program loop is interrupted by the COP820C/840C timer after 100 ms of DTMF output. As stated previously, the Stack Pointer (SP) must be adjusted (incremented by 2) following the timer interrupt before returning from the DTMFLP subroutine.

This second DTMF generation subroutine for the COP820C/840C uses 301 bytes of code, consisting of 88 bytes of program code and 213 bytes of ROM table. The following is a summary of the DTMFLP subroutine code allocation.

DTMFLP Code Allocation	# of Bytes
1. Subroutine Header Code	42
2. Interrupt Code	16
3. LUP42 Code	30
4. Telephone Key Table	64
5. Sine Value Tables	149
Total	301

A program test routine to sequentially call the DTMFLP subroutine for each of the 16 DTMF keyboard input digits is supplied with the listing for the DTMF35 program. This test routine uses a 16 byte ROM table to supply the low true encoded column/row keyboard input to the accumulator. An input from the I0 pin of the I port is used to select which DTMF generation subroutine is to be used. The DTMFLP subroutine is selected with I0 = 1.

A TYPICAL RESISTOR LADDER NETWORK IS SHOWN IN *FIGURE 4.*

SUMMARY

In summary, the DTMF35 program assumes a COP820C/840C clocked with a 3.58 MHz crystal in divide by 10 mode. The DTMF35 program contains three subroutines, KBRDEC, DTMFGP, and DTMFLP. The KBRDEC subroutine is a low true DTMF keyboard decoder, while the DTMFGP and DTMFLP subroutines represent the alternative methods of DTMF generation.

The KBRDEC subroutine provides a low true decoding of the DTMF keyboard input and assumes that the keyboard input has been encoded in a low true column/row format, with the columns of the keyboard being sequentially strobed.

The DTMFGP subroutine produces two PWM (Pulse Width Modulation) outputs (representing the selected high and low band DTMF frequencies) for combination with an external op amp network (LM324 or equivalent).

The DTMFLP subroutine produces six bits of combined high band and low band DTMF frequency output for combination in an external resistor ladder network. This output represents a combined sine wave simulation of the two selected DTMF frequencies by combining values from two selected ROM tables, and updating these values every 118 μs.

The three DTMF35 subroutines contain the following number of bytes of program and ROM table memory:

Subroutine	# of Bytes of Program	# of Bytes of ROM Table	Total # of Bytes
KBRDEC	19	16	35
DTMFGP	78	16	94
DTMFLP	88	213	301

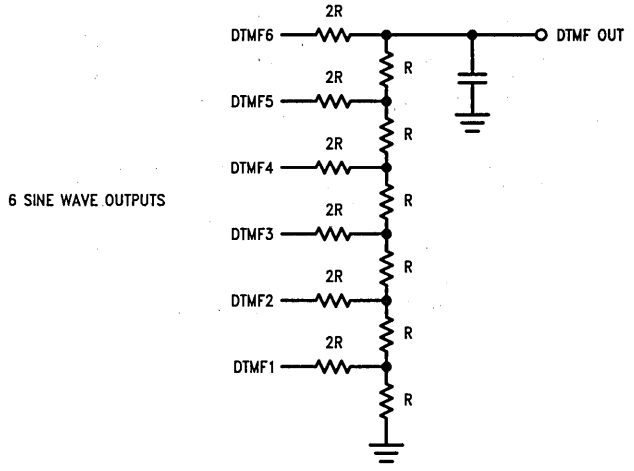

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FIGURE 4. Typical Resistor Ladder Network

```
1                       ;
2                       ; DTMF GENERATION WITH A 3.58 MHZ       VERNE H. WILSON
3                       ;       CRYSTAL FOR COP820C/840C          10/28/89
4                       ;
5                       ; DTMF - DUAL TONE MULTIPLE FREQUENCY
6                       ;
7                       ; PROGRAM NAME: DTMF35.MAC
8                       ;
9                               .TITLE DTMF35
10                              .CHIP 840
11                      ;
12                      ;
13                      ; THIS DTMF PROGRAM IS BASED ON A COP820C/840C RUNNING
14                      ; WITH A CKI CLOCK OF 3.579545 MHZ (TV COLOR CRYSTAL
15                      ; FREQUENCY) IN DIVIDE BY 10 MODE, FOR AN INSTRUCTION
16                      ; CYCLE TIME OF 2.7936511 MICROSECONDS.
17                      ;
18                      ; THIS PROGRAM CONTAINS THREE SUBROUTINES, ONE FOR A
19                      ; LOW TRUE ROW/COLUMN DTMF KEYBOARD DECODING (KBRDEC),
20                      ; AND THE OTHER TWO (DTMFGP, DTMFLP) FOR ALTERNATE
21                      ; METHODS OF DTMF GENERATION.
22                      ;
23                      ; KEYBOARD INPUT DATA IS IN ACCUMULATOR WITH A
24                      ;    LOW TRUE FORMAT AS FOLLOWS:
25                      ;        BITS 7 TO 4 : LOW TRUE COLUMN VALUE (E,D,B,7)
26                      ;        BITS 3 TO 0 : LOW TRUE ROW VALUE (E,D,B,7)
27                      ;
28                      ; ASSUMPTION MADE THAT COLUMN STROBES (LOW TRUE) ARE
29                      ;    OUTPUT, WHILE ROW VALUES (LOW TRUE) ARE INPUT.
30                      ;
31                      ; THE FIRST METHOD OF DTMF GENERATION CONSISTS OF
32                      ; GENERATING TWO PWM OUTPUTS ON THE G PORT G2 AND G3
33                      ; OUTPUT PINS. THESE TWO OUTPUTS NEED TO BE MIXED
34                      ; EXTERNALLY WITH AN APPROPIATE LM324 OP AMP FEEDBACK
35                      ; CIRCUIT TO GENERATE THE DTMF.
36                      ;
37                      ; THE SECOND METHOD OF DTMF GENERATION USES ROM LOOKUP
38                      ; TABLES TO SIMULATE THE TWO DTMF SINE WAVES AND
39                      ; COMBINES THEM ARITHMETICALLY. THE RESULT IS OUTPUT ON
40                      ; THE LOWER SIX BITS OF THE L PORT (L0 - L5). THESE SIX
41                      ; OUTPUTS ARE COMBINED EXTERNALLY WITH A LADDER NETWORK
42                      ; TO GENERATE THE DTMF.
43                      ;
44                      ; THE SECOND DTMF GENERATION METHOD USES APPROXIMATELY
45                      ; THREE TIMES AS MUCH ROM CODE (INCLUDING PROGRAM CODE
46                      ; AND ROM TABLES) AS THE FIRST METHOD, BUT HAS THE
47                      ; ADVANTAGE OF ELIMINATING THE COST OF THE EXTERNAL
48                      ; ACTIVE COMPONENT (LM324 OR EQUIVALENT).
49                      ;
50                      ; BOTH OF THE DTMF SUBROUTINES GENERATE THEIR OUTPUTS
51                      ; FOR A PERIOD OF 100 MILLISECONDS.
```

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```
52                          ;
53                          ; DECLARATIONS:
54                          ;
55      0000                        KDATA  = 0          ; *** KEYBOARD DATA ***
56      00D0                        PORTLD = 0D0        ; PORTL DATA REG
57      00D1                        PORTLC = 0D1        ; PORTL CONFIG REG
58      00D4                        PORTGD = 0D4        ; PORTG DATA REG
59      00D5                        PORTGC = 0D5        ; PORTG CONFIG REG
60      00D7                         PORTI = 0D7        ; PORTI INPUT PINS
61      00DC                         PORTD = 0DC        ; PORTD REG
62      00EA                         TMRLO = 0EA        ; TIMER LOW COUNTER
63      00EB                         TMRHI = 0EB        ; TIMER HIGH COUNTER
64      00EC                         TAULO = 0EC        ; TMR AUTORELOAD REG LO
65      00ED                         TAUHI = 0ED        ; TMR AUTORELOAD REG HI
66      00EE                         CNTRL = 0EE        ; CONTROL REG
67      00EF                           PSW = 0EF        ; PROC STATUS WORD
68      00F0                            R0 = 0F0        ; LB FREQ LOOP COUNTER
69      00F1                            R1 = 0F1        ; LB FREQ LOOP COUNT
70      00F2                            R2 = 0F2        ; LB FREQ Q COUNT
71      00F3                            R3 = 0F3        ; LB FREQ R COUNT
72                          ;
73 0000 DD2F                START:  LD      SP,#02F     ; INITIALIZE STACK PTR
74                          ;
75                          ;                                   KEYBOARD HEX DIGIT MATRIX
76                          ;                                         1  2  3  A
77 0002 DEDC                        LD      B,#PORTD    ;             4  5  6  B
78 0004 9E00                        LD      [B],#0      ;             7  8  9  C
79 0006 A0                  LOOP:   RC                  ;             *  0  #  D
80 0007 AE                          LD      A,[B]       ; DTMF TEST LOOP
81 0008 9405                        ADD     A,#5        ; SEQUENCE IS 1,5,9,D,4,
82 000A A6                          X       A,[B]       ; 8,#,A,7,0,3,B,*,2,6,C
83 000B 6C                          RBIT    4,[B]       ; HEX MATRIX TO LOOKUP
84 000C 9420                        ADD     A,#020      ;    TABLE FOR LOW TRUE
85 000E A4                          LAID                ;    COLUMN/ROW INPUT TO
86 000F 3210                        JSR     KBRDEC      ;    KBRDEC SUBROUTINE
87 0011 A1                          SC                  ; SET C IF NOT SINGLE KEY
88 0012 DED7                        LD      B,#PORTI    ; TEST BIT 0 OF PORTI TO
89 0014 70                          IFBIT   0,[B]       ;    DETERMINE WHICH
90 0015 03                          JP      BYPA        ;    DTMF SUBROUTIINE
91 0016 3040                        JSR     DTMFGP      ; TWO PWM OUTPUTS ON
92 0018 02                          JP      BYPB        ;    G PORT PINS G2,G3
93 0019 308E                BYPA:   JSR     DTMFLP      ; SIX LADDER OUTPUTS ON
94                                                      ;    L PORT PINS L0 - L5
95 001B DEDC                BYPB:   LD      B,#PORTD    ; DO WILL TOGGLE FOR EACH
96 001D E8                          JP      LOOP        ;    CALL OF SUBROUTINE
97                          ;
98                          ;
99                          ;
```

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3

```
                                        .FORM
                        ;
                        ; KEYBOARD DIGIT MATRIX TABLE
                        ;
                                        . = 020
                        ;
                        ;                 1   5   9   D   4   8   #   A
0020 EE                 .BYTE    0EE,0DD,0BB,077,0ED,0DB,0B7,07E
0021 DD
0022 BB
0023 77
0024 ED
0025 DB
0026 B7
0027 7E
                        ;                 7   0   3   B   *   2   6   C
0028 EB                 .BYTE    0EB,0D7,0BE,07D,0E7,0DE,0BD,07B
0029 D7
002A BE
002B 7D
002C E7
002D DE
002E BD
002F 7B
                        ;
                        ;
                        ;
                        ;
                        ;
                        ; FIRST DTMF SUBROUTINE (DTMFGP) PRODUCES TWO PWM
                        ;     (PULSE WIDTH MODULATION) OUTPUTS ON PINS G3, G2
                        ;
                        ;
                        ; G PORT IS USED FOR THE TWO OUTPUTS
                        ;     -     HIGH BAND (HB) FREQUENCY OUTPUT ON G3
                        ;     -     LOW BAND (LB) FREQUENCY OUTPUT ON G2
                        ;
                        ; TIMER COUNTS OUT
                        ;     -     HB FREQUENCIES
                        ;
                        ; PROGRAM COUNTS OUT
                        ;     -     LB FREQUENCIES
                        ;     -     100 MSEC DIVIDED BY LB HALF PERIOD QUOTIENT
                        ;     -     100 MSEC DIVIDED BY LB HALF PERIOD REMAINDER
                        ;
                        ; NOTE THAT ALL COUNTS MUST BE NORMALIZED TO THE
                        ;     2.7936511 MICROSECOND INSTRUCTION CYCLE Tc
                        ;
                        ; 100 MSEC REPRESENTS 35796 Tc's
                        ;
                        ;
```

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```
137                     ;
138                     ;
139                     ; HALF PERIODS FOR THE 8 DTMF FREQUENCIES (697,770,852,
140                     ;     941,1209,1336,1477, AND 1633 KHZ) ARE 257,232,
141                     ;     210,190,148,134,121, AND 110 Tc's RESPECTIVELY
142                     ;
143                     ; THE 100 MSEC DIVIDED BY HALF PERIOD QUOTIENTS ARE
144                     ;     139,154,170,188,241,267,295, AND 325 RESPECTIVELY
145                     ;
146                     ; THE 100 MSEC DIVIDED BY HALF PERIOD REMAINDERS ARE
147                     ;     72,67,95,75,127,17,100, AND 45 RESPECTIVELY
148                     ;
149                     ;
150                     ;
151                     ;
152                     ; BINARY FORMAT FOR THE HEX DIGIT KEY VALUE FROM THE
153                     ;    KBRDEC SUBROUTINE IS 0000RRCC,
154                     ;       WHERE  -  RR IS ROW SELECT (LB FREQUENCIES)
155                     ;              -  CC IS COLUMN SELECT (HB FREQUENCIES)
156                     ;
157                     ; FREQUENCY VECTORS (HB & LB) FOR FREQ PARAMETER TABLE
158                     ;    MADE FROM KEY VALUE
159                     ;
160                     ; HB FREQ VECTORS (4) END WITH 00 FOR TIMER COUNTS,
161                     ;    WHERE VECTOR FORMAT IS 0011CC00
162                     ;
163                     ; LB FREQUENCY VECTORS (12) END WITH:
164                     ;    11 FOR HALF PERIOD LOOP COUNTS,
165                     ;         WHERE VECTOR FORMAT IS 0011RR11
166                     ;    10 FOR 100 MSEC DIVIDED BY HALF PERIOD QUOTIENTS,
167                     ;         WHERE VECTOR FORMAT IS 0011RR10
168                     ;    01 FOR 100 MSEC DIVIDED BY HALF PERIOD REMAINDERS,
169                     ;         WHERE VECTOR FORMAT IS 0011RR01
170                     ;
171                     ; FREQ PARAMETER TABLE AT HEX 003*  (REQUIRED LOCATION)
172                     ;
173                     ;
174                     ;
175                     ;              KEY VALUE
176                     ;               0000RRCC
177                     ;
178                     ;    TIMER      T     CC00
179                     ;    R1         F     RR11
180                     ;    R2         Q     RR10
181                     ;    R3         R     RR01
182                     ;
183                     ;
184                     ;
```

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3

```
                                        .FORM
                        ;
                        ;
                        ;FREQUENCY AND 100 MSEC PARAMETER TABLE
                        ;
0030 93                         .BYTE     147           ; T
0031 0A                         .BYTE      10           ; R
0032 8C                         .BYTE     140           ; Q
0033 26                         .BYTE      38           ; F
0034 85                         .BYTE     133           ; T
0035 09                         .BYTE       9           ; R
0036 9B                         .BYTE     155           ; Q
0037 21                         .BYTE      33           ; F
0038 78                         .BYTE     120           ; T
0039 0E                         .BYTE      14           ; R
003A AB                         .BYTE     171           ; Q
003B 1F                         .BYTE      31           ; F
003C 6D                         .BYTE     109           ; T
003D 0A                         .BYTE      10           ; R
003E BD                         .BYTE     189           ; Q
003F 1A                         .BYTE      26           ; F
                        ;
                        ;
                        ;
0040 DED5               DTMFGP:   LD        B,#PORTGC   ; CONFIGURE G PORT
0042 9B3F                         LD        [B-],#03F   ;    FOR OUTPUTS
0044 6B                           RBIT      3,[B]       ; OPTIONAL HB RESET
0045 6A                           RBIT      2,[B]       ; OPTIONAL LB RESET
0046 5F                           LD        B,#KDATA
0047 A6                           X         A,[B]       ; STORE KEY VALUE
0048 AE                           LD        A,[B]       ; KEY VALUE TO ACC
0049 9733                         OR        A,#033      ; CREATE LB FREQ VECTOR
004B DEF1                         LD        B,#R1       ;    FROM KEY VALUE
004D A6                 LUP:      X         A,[B]
004E AE                           LD        A,[B]       ; THREE PARAMETERS
004F A4                           LAID                  ;    FROM LOW BAND
0050 A2                           X         A,[B+]      ;    FREQ ROM TABLE
0051 8B                           DEC       A           ;    TO R1,R2,R3
0052 44                           IFBNE     #4
0053 F9                           JP        LUP
0054 5F                           LD        B,#KDATA
0055 AE                           LD        A,[B]       ; KEY VALUE TO ACC
0056 65                           SWAP      A           ; CREATE HB FREQ VECTOR
0057 A0                           RC                    ;    FROM KEY VALUE
0058 B0                           RRC       A
0059 B0                           RRC       A
005A 9730                         OR        A,#030
005C A4                           LAID                  ; HB FREQ TABLE
005D DEEA                         LD        B,#TMRLO    ;   (1 PARAMETER)
005F 9A0F                         LD        [B+],#15    ; INSTRUCTION CYCLE
0061 9A00                         LD        [B+],#0     ;   TIME UNTIL TOGGLE
```

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```
236 0063 A2                    X       A,[B+]      ; HB FREQ PARAMETER TO
237 0064 9A00                  LD      [B+],#0     ;   AUTORELOAD REGISTER
238 0066 9EB0                  LD      [B],#0B0    ; START TIMER PWM
239 0068 DED4                  LD      B,#PORTGD
240 006A DCF1                  LD      X,#R1
241 006C BB             LUP1:  LD      A,[X-]
242 006D 72                    IFBIT   2,[B]       ; TEST LB OUTPUT
243 006E 03                    JP      BYP1
244 006F B2                    X       A,[X+]
245 0070 7A                    SBIT    2,[B]       ; SET LB OUTPUT
246 0071 03                    JP      BYP2
247 0072 B8             BYP1:  NOP
248 0073 6A                    RBIT    2,[B]       ; RESET LB OUTPUT
249 0074 B2                    X       A,[X+]
250 0075 C2             BYP2:  DRSZ    R2          ; DECR. QUOT. COUNT
251 0076 01                    JP      LUP2
252 0077 0E                    JP      FINI        ; Q COUNT FINISHED
253 0078 C0             LUP2:  DRSZ    R0          ; DECR. F COUNT
254 0079 FE                    JP      LUP2        ; LB (HALF PERIOD)
255                    ;
256 007A BE                    LD      A,[X]       ; ******************
257 007B 921F                  IFEQ    A,#31       ; BALANCE         ***
258 007D EE                    JP      LUP1        ; LOW BAND        ***
259 007E B8                    NOP                 ; FREQUENCY       ***
260 007F B8                    NOP                 ; RESIDUE         ***
261 0080 9226                  IFEQ    A,#38       ; DELAY FOR       ***
262 0082 E9                    JP      LUP1        ; EACH OF THE     ***
263 0083 A4                    LAID                ; FOUR LOW BAND   ***
264 0084 B8                    NOP                 ; FREQUENCIES     ***
265 0085 E6                    JP      LUP1        ; ******************
266 0086 C3             FINI:  DRSZ    R3        ; DECR. REMAINDER COUNT
267 0087 FE                    JP      FINI      ; REM. COUNT NOT FINISHED
268 0088 BDEE6C                RBIT    4,CNTRL   ; STOP TIMER
269 008B 6B                    RBIT    3,[B]     ; OPTIONAL CLR HB OUTPUT
270 008C 6A                    RBIT    2,[B]     ; OPTIONAL CLR LB OUTPUT
271 008D 8E                    RET               ; RETURN FROM SUBROUTINE
272                    ;
273                    ;
274                    ;
```

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```
                        .FORM
                ;
                ; SECOND DTMF SUBROUTINE (DTMFLP) PRODUCES SIX
                ;     COMBINED LOW BAND AND HIGH BAND FREQUENCY
                ;     SINE WAVE OUTPUTS ON PINS L0 - L5
                ;
                ; SIX L PORT OUTPUTS (L0 - L5) FEED INTO AN EXTERNAL
                ; RESISTOR LADDER NETWORK TO CREATE THE DTMF OUTPUT.
                ;
                ; FOUR VALUES FROM A KEYBOARD ROM TABLE ARE LOADED
                ; INTO LFTBSZ (LOW FREQ TABLE SIZE), LFTADR (LOW
                ; FREQ TABLE ADDRESS), HFTBSZ (HIGH FREQ TABLE SIZE),
                ; AND HFTADR (HIGH FREQ TABLE ADDRESS).
                ;
                ; LUP42 USES THE LFPTR (LOW FREQ POINTER) AND HFPTR
                ; (HIGH FREQ POINTER) TO ACCESS THE SINE DATA TABLES
                ; FOR THE SELECTED FREQUENCIES ONCE PER LOOP. THESE
                ; POINTERS ARE BOTH INCREMENTED ONCE PER LUP42.
                ;
                ; LUP42 PROGRAM LOOP UPDATES THE OUTPUT VALUE EVERY
                ; 117 1/3 uSEC BY SELECTING AND THEN COMBINING NEW
                ; VALUES FROM THE SELECTED LOW BAND AND HIGH BAND
                ; FREQUENCY ROM TABLES WHICH SIMULATE THE SINE WAVES
                ; FOR THE TWO FREQUENCIES.
                ;
                ; MULTIPLES OF THE MAGIC NUMBER OF APPROXIMATELY
                ; 118 uSEC ARE CLOSE APPROXIMATIONS TO ALL EIGHT OF
                ; THE DTMF FREQUENCIES.
                ;
                ; COP820C/840C TIMER USED TO INTERRUPT THE DTMF LUP42
                ; PROGRAM LOOP AFTER 100 MSEC TO FINISH THE DTMF
                ; OUTPUT AND RETURN FROM THE DTMFLP SUBROUTINE. NOTE
                ; THAT THE STACK POINTER (SP) MUST BE ADJUSTED AFTER
                ; THE INTERRUPT BEFORE RETURNING FROM THE SUBROUTINE.
                ;
                ;
                ;
                ;
                ;
                ; DECLARATIONS:
                ;
0005                    LFPTR   =  05           ; LOW FREQ POINTER
0006                    TEMP    =  06           ; TEMPORARY
0007                    HFPTR   =  07           ; HIGH FREQ POINTER
0008                    LFTBSZ  =  08           ; LO FREQ TABLE SIZE
0009                    LFTADR  =  09           ; LO FREQ TABLE ADDR
000A                    HFTBSZ  =  0A           ; HI FREQ TABLE SIZE
000B                    HFTADR  =  0B           ; HI FREQ TABLE ADDR
                ;
0004                    TRUN    =  04
                ;
```

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```
326                             ;
327 008E BCD1FF         DTMFLP:  LD       PORTLC,#0FF     ; INITIALIZE PORT L
328 0091 BCD01D                  LD       PORTLD,#29      ;    FOR NO TONE OUT
329 0094 BC0500                  LD       LFPTR,#0        ; INITIALIZE OFFSET
330 0097 58                      LD       B,#HFPTR        ;    POINTERS FOR
331 0098 9A00                    LD       [B+],#0         ;    DTMF SINE WAVE
332 009A A0                      RC                       ;    TABLE LOOKUP
333 009B 65                      SWAP     A               ; QUADRUPLE KEY
334 009C B0                      RRC      A               ;    VALUE AND ADD
335 009D B0                      RRC      A               ;    OFFSET FOR KEY
336 009E 94B8                    ADD      A,#0B8          ;    TABLE LOOKUP
337 00A0 A6              FRLUP:  X        A,[B]           ; LOAD FOUR VALUES
338 00A1 AE                      LD       A,[B]           ;    FROM ROM KEY
339 00A2 A4                      LAID                     ;    TABLE INTO LOW
340 00A3 A2                      X        A,[B+]          ;    FREQ LFTBSZ,
341 00A4 8A                      INC      A               ;    LFTADR, AND HI
342 00A5 4C                      IFBNE    #0C             ;    FREQ HFTBSZ,
343 00A6 F9                      JP       FRLUP           ;    HFTADR
344 00A7 DEEA                    LD       B,#TMRLO        ; INITIALIZE TIMER
345 00A9 9A00                    LD       [B+],#0         ;    WITH A tC COUNT
346 00AB 9A8C                    LD       [B+],#140       ;    EQUIVALENT TO
347 00AD 9A00                    LD       [B+],#0         ;    100 MSEC PLUS
348 00AF 9A8C                    LD       [B+],#140       ;    A LUP42 TIME
349 00B1 9A80                    LD       [B+],#080       ; TIMER PWM, NO OUT
350 00B3 9B11                    LD       [B-],#011       ; ENABLE TMR INTRPT
351 00B5 7C                      SBIT     TRUN,[B]        ; START TIMER
352 00B6 210F                    JMP      LUP42
353                             ;
354                             ;
355                             ;
356                             ;
357                             ; TELEPHONE KEY TABLE:
358                             ;
359                             ;    TABLE FORMAT:
360                             ;         PARAMETER 1:  # OF LOW FREQ TABLE VALUES
361                             ;         PARAMETER 2:  BASE ADDR. OF LOW FREQ VALUES
362                             ;         PARAMETER 3:  # OF HIGH FREQ TABLE VALUES
363                             ;         PARAMETER 4:  BASE ADDR. OF HIGH FREQ VALUES
364                             ;
365                             ; KEY 1
366 00B8 31                              .BYTE    49,02D,7,07C
    00B9 2D
    00BA 07
    00BB 7C
367                             ;
368                             ; KEY 2
369 00BC 31                              .BYTE    49,02D,19,083
    00BD 2D
    00BE 13
    00BF 83
370                             ;
```

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```
371                             ; KEY 3
372 00C0 31                                 .BYTE     49,02D,23,096
    00C1 2D
    00C2 17
    00C3 96
373                             ;
374                             ; KEY A
375 00C4 31                                 .BYTE     49,02D,21,0AD
    00C5 2D
    00C6 15
    00C7 AD
376                             ;
377                             ; KEY 4
378 00C8 0B                                 .BYTE     11,05E,7,07C
    00C9 5E
    00CA 07
    00CB 7C
379                             ;
380                             ; KEY 5
381 00CC 0B                                 .BYTE     11,05E,19,083
    00CD 5E
    00CE 13
    00CF 83
382                             ;
383                             ; KEY 6
384 00D0 0B                                 .BYTE     11,05E,23,096
    00D1 5E
    00D2 17
    00D3 96
385                             ;
386                             ; KEY B
387 00D4 0B                                 .BYTE     11,05E,21,0AD
    00D5 5E
    00D6 15
    00D7 AD
388                             ;
389                             ; KEY 7
390 00D8 0A                                 .BYTE     10,069,7,07C
    00D9 69
    00DA 07
    00DB 7C
391                             ;
392                             ; KEY 8
393 00DC 0A                                 .BYTE     10,069,19,083
    00DD 69
    00DE 13
    00DF 83
394                             ;
395                             ; KEY 9
396 00E0 0A                                 .BYTE     10,069,23,096
    00E1 69
```

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```
     00E2 17
     00E3 96
397                          ;
398                          ; KEY C
399  00E4 0A                 .BYTE     10,069,21,0AD
     00E5 69
     00E6 15
     00E7 AD
400                          ;
401                          ; KEY *
402  00E8 09                 .BYTE     9,073,7,083
     00E9 73
     00EA 07
     00EB 83
403                          ;
404                          ; KEY 0
405  00EC 09                 .BYTE     9,073,19,07C
     00ED 73
     00EE 13
     00EF 7C
406                          ;
407                          ; KEY #
408  00F0 09                 .BYTE     9,073,23,096
     00F1 73
     00F2 17
     00F3 96
409                          ;
410                          ; KEY D
411  00F4 09                 .BYTE     9,073,21,0AD
     00F5 73
     00F6 15
     00F7 AD
412                          ;
413                          ;
414                          ;
415                          ;
416       00FF               .=00FF
417                          ;
418  00FF BCD01D             INTRPT:   LD        PORTLD,#29      ; BASE LINE VALUE
419  0102 DEEF                         LD        B,#PSW          ; 100 MSEC INTERRUPT
420  0104 9B00                         LD        [B-],#0         ;    FROM TIMER
421  0106 9E00                         LD        [B],#0          ; CLR PSW AND CNTRL
422  0108 DEFD                         LD        B,#SP           ; RESTORE STACK
423  010A AE                           LD        A,[B]           ;    POINTER (SP)
424  010B 8A                           INC       A               ;    TO ITS VALUE
425  010C 8A                           INC       A               ;    BEFORE THE
426  010D A6                           X         A,[B]           ;    INTERRUPT
427  010E 8E                           RET                       ; RETURN FROM
428                                                              ;    SUBROUTINE
429                          ;
430                          ;
```

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```
                                .FORM
                    ;
                    ; LUP42 CONSISTS OF 42 COP840C INSTRUCTION CYCLE TIMES
                    ; LUP42 TIMING LOOP IS 42 / 0.3579545 = 117 1/3 uSEC
                    ;
                    ;
010F 5A             LUP42:    LD        B,#LFPTR
0110 AE                       LD        A,[B]           ; INCREMENT LOW FREQ
0111 8A                       INC       A               ;    OFFSET POINTER
0112 57                       LD        B,#LFTBSZ       ; TEST IF LFPTR
0113 82                       IFEQ      A,[B]           ;    BEYOND LIMIT
0114 64                       CLR       A               ; REINITIALIZE LFPTR
0115 5A                       LD        B,#LFPTR        ;    FOR NEXT TIME
0116 A6                       X         A,[B]
0117 56                       LD        B,#LFTADR       ; ADD PTR TO LO FREQ
0118 84                       ADD       A,[B]           ;    TABLE ADDRESS
0119 A4                       LAID                      ; LOW FREQ COMPONENT
011A 59                       LD        B,#TEMP         ; RESULT TO TEMP
011B A2                       X         A,[B+]
011C AE                       LD        A,[B]           ; INCREMENT HI FREQ
011D 8A                       INC       A               ;    OFFSET POINTER
011E 55                       LD        B,#HFTBSZ       ; TEST IF HFPTR
011F 82                       IFEQ      A,[B]           ;    BEYOND LIMIT
0120 64                       CLR       A               ; REINITIALIZE HFPTR
0121 58                       LD        B,#HFPTR        ;    FOR NEXT TIME
0122 A6                       X         A,[B]
0123 54                       LD        B,#HFTADR       ; ADD PTR TO HI FREQ
0124 84                       ADD       A,[B]           ;    TABLE ADDRESS
0125 A4                       LAID                      ; HI FREQ COMPONENT
0126 59                       LD        B,#TEMP         ; ADD LOW FREQ VALUE
0127 84                       ADD       A,[B]           ;   TO HI FREQ VALUE
0128 9CD0                     X         A,PORTLD        ; RESULT TO PORT L
012A A4                       LAID                      ; EQUIVALENT OF
012B A4                       LAID                      ;    SIX NOP'S
012C E2                       JP        LUP42           ; TIMING LOOP OF
                                                        ;    117 1/3 uSEC
                    ;
                    ;
                    ;
                    ;
```

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```
                .FORM
;
; THE FREQUENCY APPROXIMATION IS EQUAL TO THE NUMBER OF
; CYCLES OF SINE WAVE DIVIDED BY THE TIME IN THE TOTAL
; NUMBER OF LUP42 CYCLES BEFORE THE REPETITION OF THE
; ROM TABLE. AS AN EXAMPLE, CONSIDER THE THREE CYCLES
; OF SINE WAVE AND 19 VALUES IN THE ASSOCIATED 1336 HZ
; ROM TABLE. THE 19 CYCLES OF LUP42 TIMES THE LUP42
; TIME OF 117 1/3 uSEC IS DIVIDED INTO THE THREE CYCLES
; OF SINE WAVE TO YIELD A VALUE OF 1345.69 HZ AS THE
; 1336 HZ APPROXIMATION.
;
; THE VALUES IN THE ROM TABLES FOR THE DTMF SINE WAVES
; SHOULD WRAP AROUND END TO END IN EITHER DIRECTION TO
; FORM A SYMETRICAL LOOP. THE FIRST VALUE IN THE ROM
; TABLE REPRESENTS THE BASE LINE FOR THAT FREQUENCY.
;
; THE HIGH BAND DTMF FREQUENCIES HAVE A BASE LINE VALUE
; OF 16 AND A MAXIMUM VALUE OF 32. THE LOW BAND DTMF
; FREQUENCIES HAVE A BASE LINE VALUE OF 13 AND A
; MAXIMUM VALUE OF 26. THIS DIFFERENCE IN BASE LINE
; VALUES IS NECESSARY TO SATISFY THE REQUIREMENT OF THE
; HIGH BAND FREQUENCIES NEEDING A LEVEL 2 dB ABOVE THE
; LEVEL OF THE LOW BAND FREQUENCIES TO COMPENSATE FOR
; LOSSES IN TRANSMISSION. THE SUM OF THE TWO BASE LINE
; VALUES YIELDS A BASE LINE VALUE OF 29, WHILE THE SUM
; OF THE TWO MAXIMUM VALUES YIELDS A MAXIMUM VALUE OF
; 58. THUS THE SIX BIT DTMF OUTPUT FROM THE L PORT TO
; THE LADDER NETWORK RANGES FROM 0 TO 58, WITH A BASE
; LINE VALUE OF 29.
;
; THE VALUES IN THE DTMF SINE WAVE TABLES ARE
; CALCULATED BY COMPUTING THE SINE VALUE AT THE
; APPROPIATE POINTS, SCALING THE SINE VALUE UP TO THE
; BASE LINE VALUE, AND THEN ADDING THE RESULT TO THE
; BASE LINE VALUE. THE FOLLOWING EXAMPLE WILL HELP TO
; CLARIFY THIS CALCULATION.
;
; CONSIDER THE THREE CYCLES OF SINE WAVE ACROSS 19
; DATA POINTS FOR THE 1336 HZ DTMF HIGH BAND FREQUENCY.
; THE FIRST VALUE IN THE TABLE IS THE BASE LINE VALUE
; OF 16. WITH 2 PI RADIANS PER SINE WAVE CYCLE,
; THE SUCCEEDING VALUES IN THE TABLE REPRESENT THE
; SINE VALUES OF 1 X (6 PI / 19), 2 X (6 PI / 19),
; 3 X (6 PI / 19), . . . . , UP TO 18 X (6 PI / 19).
; LET US NOW CONSIDER THE SEVENTH AND EIGHTH VALUES
; IN THE TABLE, REPRESENTING THE SINE VALUES OF
; 6 X (6 PI / 19) AND 7 X (6 PI / 19) RESPECTIVELY.
; THE CALCULATIONS OF 16 X SIN [6 X (6 PI / 19)] AND
; 16 X SIN [7 X (6 PI / 19)] YIELD VALUES OF - 5.20 AND
; 9.83 RESPECTIVELY. ROUNDED TO THE NEAREST INTEGER
```

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```
                        ; GIVES VALUES OF - 5 AND 10. WHEN ADDED TO THE BASE
                        ; LINE VALUE OF 16, THESE VALUES YIELD THE RESULTS
                        ; 11 AND 26 FOR THE SEVENTH AND EIGHTH VALUES IN THE
                        ; 1336 HZ DTMF TABLE. SYMMETRY IN THE LOOP OF 19 VALUES
                        ; IN THE DTMF TABLE DICTATES THAT THE FOURTEENTH AND
                        ; THIRTEENTH VALUES IN THE TABLE ARE 21 AND 6,
                        ; REPRESENTING VALUES OF 5 AND - 10 FROM THE
                        ; CALCULATIONS.
                        ;
                        ; THE AREA UNDER A HALF CYCLE OF SINE WAVE RELATIVE TO
                        ; THE AREA OF THE SURROUNDING RECTANGLE IS 2/PI, WHERE
                        ; PI RADIANS REPRESENT THE SINE WAVE HALF CYCLE. THIS
                        ; SURROUNDING RECTANGLE HAS A LENGTH OF PI AND A HEIGHT
                        ; OF 1, WITH THE HEIGHT REPRESENTING THE MAXIMUM SINE
                        ; VALUE. CONSEQUENTLY, THE AREA OF THIS SURROUNDING
                        ; RECTANGLE IS PI. THE INTEGRAL OF THE AREA UNDER THE
                        ; HALF SINE WAVE FROM 0 TO PI IS EQUAL TO 2. THE RATIO
                        ; OF 2/PI IS EQUAL TO 63.66 % , SO THAT THE TOTAL OF
                        ; THE VALUES FOR EACH HALF SINE WAVE SHOULD APPROXIMATE
                        ; 63.66 % OF THE SUM OF THE MAX VALUES. THE MAXIMUM
                        ; VALUES (RELATIVE TO THE BASE LINE) ARE 13 AND 16
                        ; RESPECTIVELY, FOR THE LOW AND HIGH BAND FREQUENCIES.
                        ;
                        ;
                        ;
                        ;
                        ;
                        ; LF697:   4 CYCLES OF SINE WAVE SPREAD
                        ;                ACROSS 49 TIMING LOOP (LUP42) CYCLES
                        ;
                        ;         FREQ. = 4 / (49 X 117 1/3) = 695.73 HZ
                        ;         ERROR = (697 - 695.73) / 697  = - 0.18 %
                        ;
555 012D 0D                     .BYTE     13,19,24,26,25,20,14,7,2,0
    012E 13
    012F 18
    0130 1A
    0131 19
    0132 14
    0133 0E
    0134 07
    0135 02
    0136 00
556 0137 01                     .BYTE     1,5,11,18,23,26,25,21,15,9
    0138 05
    0139 0B
    013A 12
    013B 17
    013C 1A
    013D 19
    013E 15
```

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```
    013F 0F
    0140 09
557 0141 03                         .BYTE     3,0,1,4,10,16,22,25,26,23
    0142 00
    0143 01
    0144 04
    0145 0A
    0146 10
    0147 16
    0148 19
    0149 1A
    014A 17
558 014B 11                         .BYTE     17,11,5,1,0,3,8,15,21,25
    014C 0B
    014D 05
    014E 01
    014F 00
    0150 03
    0151 08
    0152 0F
    0153 15
    0154 19
559 0155 1A                         .BYTE     26,24,19,12,6,1,0,2,7
    0156 18
    0157 13
    0158 0C
    0159 06
    015A 01
    015B 00
    015C 02
    015D 07
560                         ;
561                         ;
562                         ; LF770:    1 CYCLE OF SINE WAVE SPREAD
563                         ;                 ACROSS 11 TIMING LOOP (LUP42) CYCLES
564                         ;
565                         ;           FREQ. = 1 / (11 X 117 1/3) = 774.79 HZ
566                         ;           ERROR = (774.79 - 770) / 770  = + 0.62 %
567                         ;
568 015E 0D                         .BYTE     13,20,25,26,23,17,9,3,0,1
    015F 14
    0160 19
    0161 1A
    0162 17
    0163 11
    0164 09
    0165 03
    0166 00
    0167 01
569 0168 06                         .BYTE     6
570                         ;
```

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```
                        ;
                        ; LF852:    1 CYCLE OF SINE WAVE SPREAD
                        ;                   ACROSS 10 TIMING LOOP (LUP42) CYCLES
                        ;
                        ;           FREQ. = 1 / (10 X 117 1/3) = 852.27 HZ
                        ;           ERROR = (852.27 - 852) / 852  = + 0.03 %
                        ;
0169 0D                             .BYTE     13,21,25,26,21,13,5,1,0,5
016A 15
016B 19
016C 1A
016D 15
016E 0D
016F 05
0170 01
0171 00
0172 05
                        ;
                        ;
                        ; LF941:    1 CYCLE OF SINE WAVE SPREAD
                        ;                   ACROSS 9 TIMING LOOP (LUP42) CYCLES
                        ;
                        ;           FREQ. = 1 / (9 X 117 1/3) = 946.97 HZ
                        ;           ERROR = (946.97 - 941) / 941  = + 0.63 %
                        ;
0173 0D                             .BYTE     13,21,26,24,18,8,2,0,5
0174 15
0175 1A
0176 18
0177 12
0178 08
0179 02
017A 00
017B 05
                        ;
                        ;
                        ;
                        ; HF1209:   1 CYCLE OF SINE WAVE SPREAD
                        ;                   ACROSS 7 TIMING LOOP (LUP42) CYCLES
                        ;
                        ;           FREQ. = 1 / (7 X 117 1/3) = 1217.53 HZ
                        ;           ERROR = (1217.53 - 1209) / 1209  = + 0.71 %
                        ;
017C 10                             .BYTE     16,29,32,23,9,0,3
017D 1D
017E 20
017F 17
0180 09
0181 00
0182 03
                        ;
```

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```
599                             ;
600                             ; HF1336:  3 CYCLES OF SINE WAVE SPREAD
601                             ;                  ACROSS 19 TIMING LOOP (LUP42) CYCLES
602                             ;
603                             ;          FREQ. = 3 / (19 X 117 1/3) = 1345.69 HZ
604                             ;          ERROR = (1345.69 - 1336) / 1336  = + 0.73 %
605                             ;
606 0183 10                             .BYTE     16,29,31,19,4,0,11,26,32,24
    0184 1D
    0185 1F
    0186 13
    0187 04
    0188 00
    0189 0B
    018A 1A
    018B 20
    018C 18
607 018D 08                             .BYTE     8,0,6,21,32,28,13,1,3
    018E 00
    018F 06
    0190 15
    0191 20
    0192 1C
    0193 0D
    0194 01
    0195 03
608                             ;
609                             ;
610                             ; HF1477:  4 CYCLES OF SINE WAVE SPREAD
611                             ;                  ACROSS 23 TIMING LOOP (LUP42) CYCLES
612                             ;
613                             ;          FREQ. = 4 / (23 X 117 1/3) = 1482.21 HZ
614                             ;          ERROR = (1482.21 - 1477) / 1477  = + 0.35 %
615                             ;
616 0196 10                             .BYTE     16,30,29,14,1,4,20,32,26,10
    0197 1E
    0198 1D
    0199 0E
    019A 01
    019B 04
    019C 14
    019D 20
    019E 1A
    019F 0A
617 01A0 00                             .BYTE     0,8,24,32,22,6,0,12,28,31
    01A1 08
    01A2 18
    01A3 20
    01A4 16
    01A5 06
    01A6 00
```

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```
    01A7 0C
    01A8 1C
    01A9 1F
618 01AA 12                         .BYTE     18,3,2
    01AB 03
    01AC 02
619                         ;
620                         ;
621                         ; HF1633:  4 CYCLES OF SINE WAVE SPREAD
622                         ;                  ACROSS 21 TIMING LOOP (LUP42) CYCLES.
623                         ;
624                         ;          FREQ. = 4 / (21 X 117 1/3) = 1623.38 HZ.
625                         ;          ERROR = (1633 - 1623.38) / 1633  = - 0.59 %
626                         ;
627 01AD 10                         .BYTE     16,31,27,9,0,11,29,30,14,0
    01AE 1F
    01AF 1B
    01B0 09
    01B1 00
    01B2 0B
    01B3 1D
    01B4 1E
    01B5 0E
    01B6 00
628 01B7 07                         .BYTE     7,25,32,18,2,3,21,32,23,5
    01B8 19
    01B9 20
    01BA 12
    01BB 02
    01BC 03
    01BD 15
    01BE 20
    01BF 17
    01C0 05
629 01C1 01                         .BYTE     1
630                         ;
631                         ;
632                         ;
```

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```
633                                     .FORM
634                             ;
635                             ; DTMF KEYBOARD DECODE SUBROUTINE (KBRDEC)
636                             ;
637                             ; KEYBOARD INPUT DATA IS IN ACCUMULATOR WITH A
638                             ;    LOW TRUE FORMAT AS FOLLOWS:
639                             ;        BITS 7 TO 4 : LOW TRUE COLUMN VALUE (E,D,B,7)
640                             ;        BITS 3 TO 0 : LOW TRUE ROW VALUE (E,D,B,7)
641                             ;
642                             ; ASSUMPTION MADE THAT COLUMN STROBES (LOW TRUE) ARE
643                             ;    OUTPUT, WHILE ROW VALUES (LOW TRUE) ARE INPUT.
644                             ;
645                             ; LOW TRUE COLUMN/ROW INPUT DIGIT IN ACCUMULATOR IS
646                             ;     TRANSFORMED INTO A DTMF HEX DIGIT KEY VALUE
647                             ;
648                             ; TABLE LOOKUP TRANSFORMATION CHECKS FOR MULTIPLE KEYS,
649                             ;     NO KEY, OR NO COLUMN SELECT, AND THEN PRODUCES
650                             ;     A DTMF HEX DIGIT KEY VALUE WITH A BINARY FORMAT
651                             ;     OF 0000RRCC FOR A SINGLE KEY INPUT,
652                             ;     WHERE   -  RR IS LOW BAND (LB) FREQUENCY SELECT
653                             ;             -  CC IS HIGH BAND (HB) FREQUENCY SELECT
654                             ;
655                             ; KBRDEC SUBROUTINE IS EXITED WITH A RETURN (RET)
656                             ;     COMMAND TO INDICATE MULTIPLE KEYS, NO KEY,
657                             ;     OR NO COLUMN SELECT
658                             ;
659                             ; KBRDEC SUBROUTINE IS EXITED WITH A RETURN AND SKIP
660                             ;     (RETSK) COMMAND TO INDICATE A SINGLE KEY ENTRY
661                             ;
662                             ;
663     0200                            .=0200
664                             ;
665                             ; LOW TRUE TRANSLATION TABLE  - ONLY E,D,B,7 ACCEPTABLE
666                             ;
667 0200 C0                             .BYTE  0C0,0C0,0C0,0C0,0C0,0C0,0C0,0C
    0201 C0
    0202 C0
    0203 C0
    0204 C0
    0205 C0
    0206 C0
    0207 0C
668 0208 C0                             .BYTE  0C0,0C0,0C0,8,0C0,4,0,0C0
    0209 C0
    020A C0
    020B 08
    020C C0
    020D 04
    020E 00
    020F C0
669                             ;
```

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```
670                         ;
671 0210 5F             KBRDEC:   LD        B,#KDATA
672 0211 A6                       X         A,[B]     ; STORE LOW TRUE
673 0212 AE                       LD        A,[B]     ;   COLUMN/ROW VALUE
674 0213 95F0                     AND       A,#0F0    ; EXTRACT LOW TRUE COLUMN
675 0215 65                       SWAP      A         ;   & PUT IN LOWER NIBBLE
676 0216 A4                       LAID                ; 0000CC00 FROM TABLE
677 0217 A0                       RC                  ; SHIFT TABLE VALUE DOWN
678 0218 B0                       RRC       A         ;   TWO BITS TO PRODUCE
679 0219 B0                       RRC       A         ;   000000CC
680 021A A6                       X         A,[B]     ; STORE RESULT
681 021B 950F                     AND       A,#0F     ; EXTRACT LOW TRUE ROW
682 021D A4                       LAID                ; 0000RR00 FROM TABLE
683 021E 84                       ADD       A,[B]     ; ADD TO PRODUCE 0000RRCC
684 021F 930F                     IFGT      A,#0F     ; RETURN IF MULTIPLE KEYS,
685 0221 8E                       RET                 ;   NO KEYS, OR NO COLUMN
686 0222 8D                       RETSK               ; RETURN AND SKIP
687                                                   ;   IF SINGLE KEY
688                         ;
689                         ;
690                         ;
691                               .END
```

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```
B       00FE          BYP1    0072          BYP2    0075          BYPA    0019
BYPB    001B          CNTRL   00EE          DTMFGP  0040          DTMFLP  008E
FINI    0086          FRLUP   00A0          HFPTR   0007          HFTADR  000B
HFTBSZ  000A          INTRPT  00FF  *       KBRDEC  0210          KDATA   0000
LFPTR   0005          LFTADR  0009          LFTBSZ  0008          LOOP    0006
LUP     004D          LUP1    006C          LUP2    0078          LUP42   010F
PORTD   00DC          PORTGC  00D5          PORTGD  00D4          PORTI   00D7
PORTLC  00D1          PORTLD  00D0          PSW     00EF          R0      00F0
R1      00F1          R2      00F2          R3      00F3          SP      00FD
START   0000  *       TAUHI   00ED  *       TAULO   00EC  *       TEMP    0006
TMRHI   00EB  *       TMRLO   00EA          TRUN    0004          X       00FC
```

TL/DD/10740-20

Low Cost A/D Conversion Using COP800

National Semiconductor
Application Note 952
Robert Weiss

INTRODUCTION

Many microcontroller applications require a low cost analog to digital conversion. In most cases the controller applications do not need high accuracy and short conversion time.

This appnote describes a simple method for performing analog to digital conversion by reducing external elements and costs.

PRINCIPLE OF A/D CONVERSION

The principle of the single slope conversion technique is to measure the time it takes for the RC network to charge up to the threshold level on the port pin, by using Timer T1 in the input capture mode. The cycle count obtained in Timer T1 can be converted into voltage, either by direct calculation or by using a suitable approximation.

Figure 1 shows the block diagram for the simple A/D conversion which measures the temperature.

BASIC CIRCUIT IMPLEMENTATION

Usually most applications use a comparator to measure the time it takes for a RC network to charge up to the voltage level on the comparator input. To reduce cost, it is possible to switch both inputs as shown in *Figure 2*.

Port G3 is the Timer T1 input. Ports G2/G1 are general purpose I/O pins that can be configurated using the I/O configurations (push-pull output/tristate). All Port G pins are Schmitt Trigger inputs. R_{LIM} is required to reduce the discharge current.

GENERAL IMPLEMENTATION

The temperature is measured with a NTC which is linearized with a parallel resistor. Using a parallel resistor, a linearization in the range of 100 Kelvin can be reached. The value of the resistor can be calculated as follow:

$$R_P = R_{tm} * (B - 2T_m)/(B + 2T_m)$$

R_{tm} Value of the NTC at a medium temperature

T_m Medium Temperature

B NTC–material constant

The linearization reduces the code, improves the accuracy and the tolerance of the NTC-R network (e.g. NTC = 100 kΩ ±10%, R = 12 kΩ ±1%, NTC//R ±2%). Using that method the useful range does not cover the whole operating temperature range of the NTC.

GENERAL ACCURACY CONSIDERATIONS

Using a single slope A/D conversion the accuracy is dependent on the following parameters:

— Stability of the Clock frequency
— Time constant of the RC network
— Accuracy of the Schmitt Trigger level
— Non-linearity of the RC-network

Figure 3. The maximum failure that appears when a sawtooth is generated without using a current source. In the current application the maximum failure would be more than 15% without using methods for reducing the non-linearities of RC-network/NTC-network.

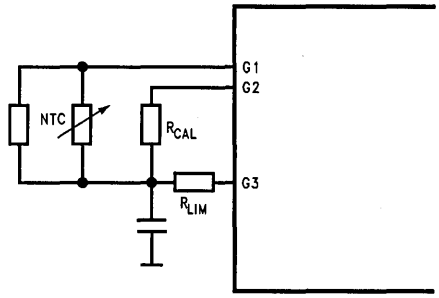

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FIGURE 2. Basic Circuit Implementation

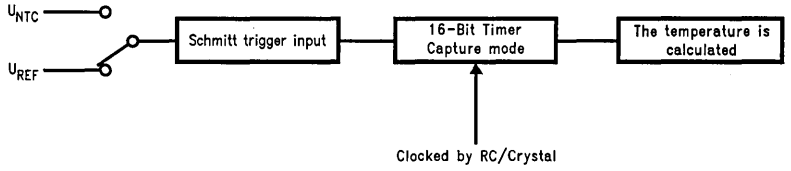

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FIGURE 1. Simple A/D Conversion

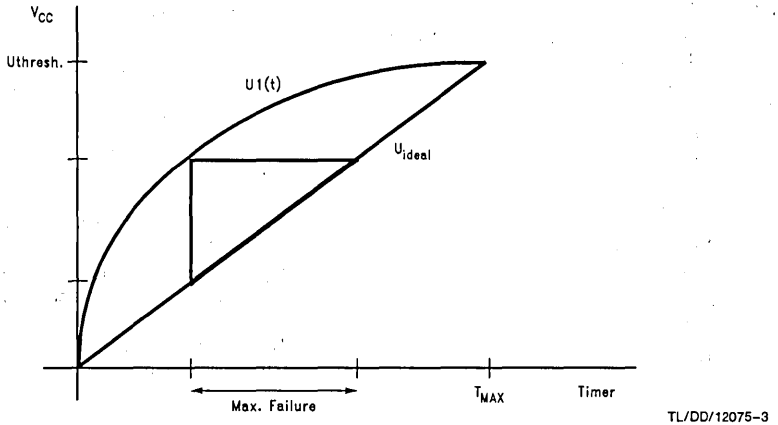

FIGURE 3. Single Slope A/D Conversion

The maximum error occurs when the gradient of the exponential function (RC) equals the gradient of the straight line (counter).

To reduce the error that is caused by the non-linearity of the RC-network a offset should be added to the calculated value. The offset reduce the failure to the middle.

Further, the accuracy can be improved by using a relative measurement method. The following diagram shows the method.

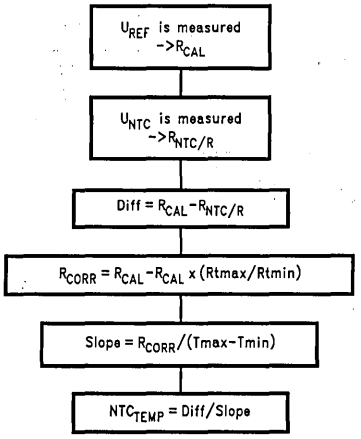

FIGURE 4. Accuracy Improvement

Measurement:

— Timer Capture mode: R_{CAL} * C is measured

— Timer Capture mode: $R_{NTC//R}$ * C is measured

Calculation:

— Build the vertical-component (R_{TMIN} − R_{TMAX}) of the triangle

— Calculate the slope

— Calculate the actual temperature

Using this method the accuracy is primarily dependent on the accuracy of R_{TMIN} and R_{TMAX} and independent of the stability of the system clock, the capacitor and the threshold of the Schmitt Trigger level. The variation of the capacitor only leads to variation of the resolution.

The following diagram shows the ideal resistance/temperature characteristic of a NTC which is linearized with a parallel resistor.

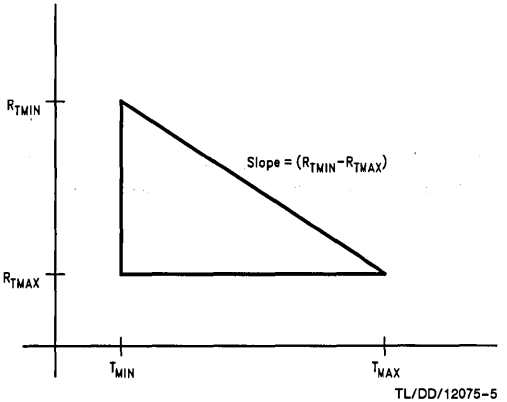

FIGURE 5. Resistance vs Temperature Characteristics

APPLICATION EXAMPLE

The following application example for temperature measurement demonstrates the procedure. The temperature is measured from 20° to 100° and is displayed on a Triplex LCD display.

NTC_{20} = 100 kΩ ±10%
R_P = 12 kΩ ±1%
T_m = 333 Kelvin → 60 Degrees
B = 4800 Kelvin
$NTC_{20}//R_P$ = 10.7 kΩ ±2%
R_{CAL} = 10.7 kΩ ±1%
T_{MIN} = 20 Degree
R_{TMIN} = 10.7 kΩ
T_{MAX} = 100 Degree
R_{TMAX} = 2.8 kΩ
C = 1 µF
RC-Clock = 2 MHz → 200 kHz instruction cycle, 5 µs
Timeconst. = R_{CAL} * C → 0.0107s
Resolution = 2140 → 11 byte, depends which Cap. value is used
Accuracy = ±2 Degree

This temperature measurment example shows a low cost technique ideally suited for cost sensitive applications which do not need high accuracy.

Figure 6 shows the complete circuit of the demoboard using the Triplex LCD method and the low cost A/D conversion technique.

The Triplex LCD drive technique is documented in a separate application note.

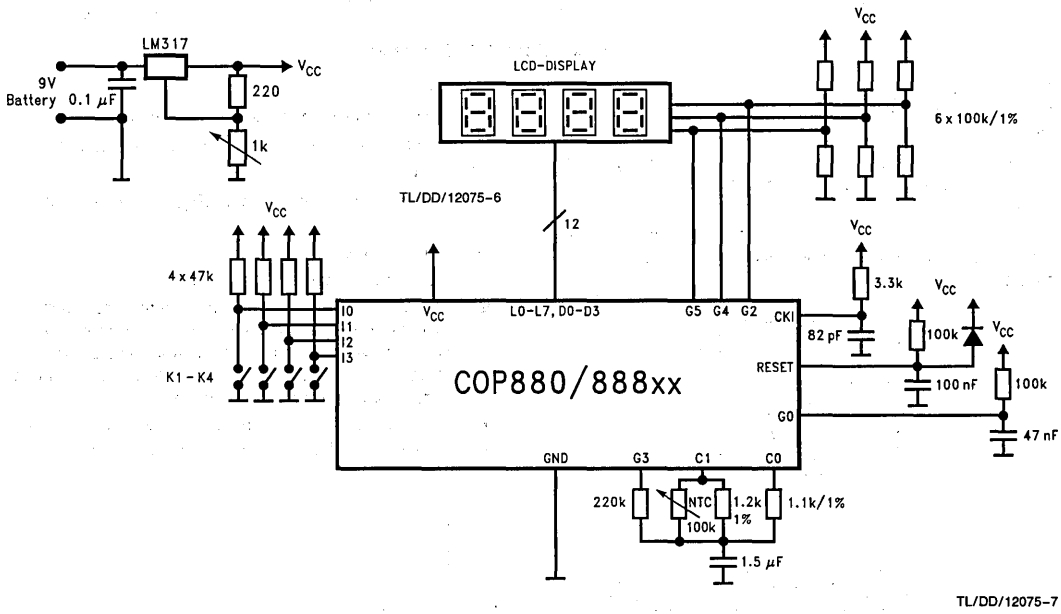

FIGURE 6. Circuit Diagram

Pressing key 1, key 2 the temperature is displayed in Degree/Fahrenheit.
Pressing key 3, key 4 Up/Down counter is displayed.

SOURCE CODE

Figure 7 shows the flow chart of the program.

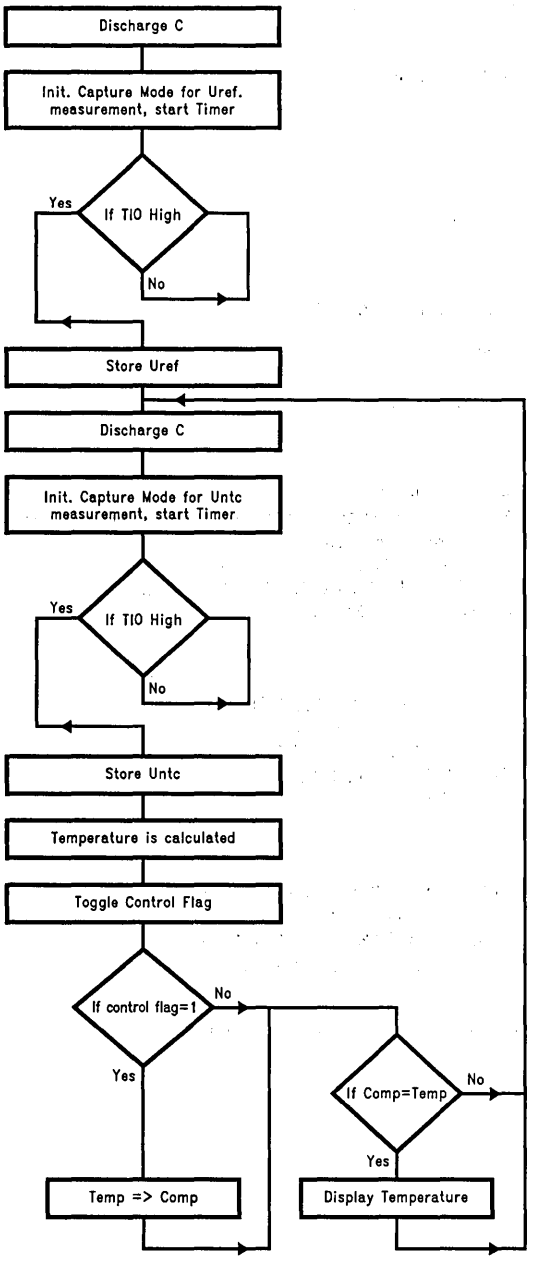

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FIGURE 7. Flow Chart

The following code is required to implement the function. It does not include the code for the Triplex LCD drive.

```
RAM = 17 Byte;
ROM = 450 Byte; Optimization is possible about 50 byte if the B - pointer consistent is used!
;*****************************A/D-CONVERSION************************************
;
;
;*****************************VAR. DECLARIATION*********************************
.SECT REGPAGE,REG
COUNT1:     .DSB 1
COUNT2:     .DSB 1
;
.SECT BASEPAGE,BASE
ZL:         .DSB 1      ;TEMPORARY
YL:         .DSB 1      ;TEMPORARY
;
.SECT RAMPAGE,RAM
CALIBLO:    .DSB 1      ;CALIBRATION-VALUE
CALIBHI:    .DSB 1
NTCLO:      .DSB 1      ;NTC-VALUE
NTCHI:      .DSB 1
TEMP:       .DSB 2      ;TEMP.-VALUE
KORRL:      .DSB 2
COMPL:      .DSB 1
COMPH:      .DSB 1
CONTROL:    .DSB 1      ;STATUS REGISTER
;*****************************START MAIN PROGRAM*********************************
MAIN: LD    SP,#06F     ;INIT SPACKPOINTER
      JSR   DISCH       ;DISCHARGE C (A/D-CONVERSION)
      JSR   CALB        ;INIT CAPTURE MODE FOR UREF. MEASURMENT
POLL: IFBIT 3,PORTGP    ;POLL - MODE (TIO - PORT)
      JP    CAL
      JP    POLL
CAL:  LD    B,#CALIBLO
      JSR   CAPTH       ;STOP TIMER, STORE CAPTURE VALUE
      JSR   CALCR       ;SLOPE IS CALCULATED
NEW:  JSR   DISCH       ;DISCHARGE C (A/D-CONVERSION)
      JSR   NTC         ;INIT CAPTURE MODEFOR UNTC MEASURMENT
POLL1: IFBIT 3,PORTGP   ;POLL-MODE
      JP    CAL1
      JP    POLL1
CAL1: LD    B,#NTCLO
      JSR   CAPTH       ;STOP TIMER, STORE CAPTURE VALUE
      JSR   CALCN       ;TEMPERATURE IS CALCULATED
      JSR   DISCH       ;DISCHARGE C (A/D-CONVERSION)
      JSR   DCHECK      ;REDUCE THE DISPLAY FLICKERING
      JMP   NEW
.ENDSECT
;*******************************************************************************
```

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```
;*************************************************************************
.SECT CODE1,ROM
;THIS ROUTINE IS REQUIRED TO REDUCE THE NOICE ON THE LINE AND THE
; DISPLAY FLICKERING.
.SECT CODE1,ROM
DCHECK:                 ;COMPARE TWO VALUES, IF EQUAL THEN
        LD   A,CONTROL  ;DISPLAY IT, OTHERWISE THE OLD VALUE
        XOR  A,#080     ;IS DISPLAYED
        X    A,CONTROL
        IFBIT 7,CONTROL
        JSR  SAVE       ;TEMP. SAVE
        JSR  COMP       ;COMPARE
        RET
;*************************************************************************
; HANDLER FOR CAPTURE MODE
CAPTH: RBIT TPND,PSW    ;RESET TIMER PENDING
        RBIT TRUN,PSW   ;STOP TIMER
        LD   A,#0FF
        SC
        SUBC A,TAULO
        X    A,[B+]     ;STORE THE CAPTURED VALUE
        LD   A,#0FF
        SUBC A,TAUHI
        X    A,[B+]     ;STORE THE CAPTURED VALUE
        RET
;*************************************************************************
; CALIBRATION SUBROUTINE, UREF IS MEASURED
CALB:
        RBIT 3,PORTGD
        RBIT 3,PORTGC   ;TRISTATE TIO
        LD PORTCD,#00
        LD PORTCC,#00   ;TRISTATE PORT C
        T1CAP HIGH      ;INIT CAPTURE MODE, HIGH SENSITIVE (MACRO)
        LD B,#CALIBLO
        SBIT 0,PORTCD   ;CONFIGURE C0 TO OUTPUT HIGH
        SBIT 0,PORTCC   ;CHARGE CAP.
        SBIT TRUN,CNTRL ;START TIMER CAPTURE MODE
        RET
;*************************************************************************
; NTC SUBROUTINE, UNTC IS MEASURED
NTC:
        RBIT 3,PORTGD
        RBIT 3,PORTGC   ;TRISTAT TIO
        LD PORTCD,#00
        LD PORTCC,#00   ;TRISTATE PORT C
        T1CAP HIGH      ;INIT CAPTURE MODE, HIGH SENSITIVE (MACRO)
        LD B,#NTCLO
        SBIT 1,PORTCD   ;CONFIGURE C1 TO OUTPUT HIGH
        SBIT 1,PORTCC   ;CHARGE CAP.
        SBIT TRUN,CNTRL ;START TIMER CAPTURE MODE
        RET
;*************************************************************************
```

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```
;*****************************************************************************
;DISCHARGE - ROUTINE
DISCH:
        LD PORTCD,#000
        LD PORTCC,#000
        RBIT TIO,PORTGD     ;DISCHARGE CAP.
        SBIT TIO,PORTGC
        LD COUNT1,#H(500)  ;DISCHARGE TIME
        LD COUNT2,#L(500)
        JSR C1              ;DELAY ROUTINE FOR DISCHARGE TIME
        RET
;*****************************************************************************
;THIS SUBROUTINE CALCULATES THE SLOPE
;THE FOLLOWING CALCULATIONS ARE DONE
;KORR=CALIB/11KOHM (RCALIB.=11KOHM)
;KORR=KORR*2,8KOHM (T=100 DEGREE, RNTC=2,8KOHM)
;CALIB=CALIB-KORR
;DIV=CALIB\80     (TEMPRANGE=80 DEGREE,100-20), SLOPE IS CALCULATED
CALCR:
;KORR=CALIB/11KOHM
        LD ZL,#L(110)
        LD ZL+1,#H(110)
        LD A,CALIBLO
        X  A,YL
        LD A,CALIBHI
        X  A,YL+1
        JSR DIVBIN16        ;SUBROUTINE BINARY DIVIDE 16 BIT BY 16 BIT
        LD A,YL
        X  A,KORRL
;*****************************************************************************
;KORR=KORR*28
        LD A,KORRL
        X  A,ZL
        LD A,#28
        X  A,YL
        JSR MULBIN8         ;SUBROUTINE MULTIPLY TWO 8 BIT VALUES
        LD A,YL
        X  A,KORRL
        LD A,YL+1
        X  A,KORRL+1
;*****************************************************************************
;KORR=CALIB-KORR
        LD B,#CALIBLO
        LD A,[B+]
        SC
        SUBC A,KORRL
        X A,KORRL
        LD A,[B]
```

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```
        SUBC A,KORRL+1
        X A,KORRL+1
;*****************************************************************************
;DIV=KORR/80
        LD ZL,#L(80)
        LD ZL+1,#H(80)
        LD A,KORRL
        X A,YL
        LD A,KORRL+1
        X A,YL+1
        JSR DIVBIN16        ;SUBROUTINE BINARY DIVIDE 16 BIT BY 16 BIT
        LD A,YL
        X A,DIV
        RET
;*****************************************************************************
;THIS SUBROUTINE CALCULATES THE TEMPERATURE
;THE FOLLOWING CALCULATIONS ARE DONE
;TEMP=CALIB-NTC
;TEMP=TEMP/DIV
;ADD OFFSET 20 DEGREE
;CONVERSION FROM HEX TO BCD
;*****************************************************************************
;TEMP=CALIB-NTC
CALCN: LD B,#CALIBLO
        LD A,[B+]
        SC
        SUBC A,NTCLO
        X A,TEMP
        LD A,[B]
        SUBC A,NTCHI
        IFNC
        JMP ERR
        X A,TEMP+1
;*****************************************************************************
;TEMP=TEMP/DIV
        LD A,TEMP
        X A,YL
        LD A,TEMP+1
        X A,YL+1
        LD A,DIV
        X A,ZL
        CLRA
        X A,ZL+1
        JSR DIVBIN16        ;SUBROUTINE BINARY DIVIDE 16 BIT BY 16 BIT
        LD A,YL
        ADD A,#20           ;ADD TEMPERATURE OFFSET
        IFGT A,#56          ;IF TEMPERATURE IS HIGER THAN 56 DEGREE THEN
        JSR CORR            ;ADD CORRECTION. OFFSET
;*****************************************************************************
```

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```
;*************************************************************************
;HEX TO BCD CONVERSION
        X  A,ZL
        LD A,ZL
        IFGT A,#100             ;IF TEMPERATURE IS MORE THAN 100 DEGREE THEN
        JP  ERR                 ;ERROR
        JSR BINBCD              ;SUBROUTINE BINARY TO BCD CONVERSION;
        LD A,BCDLO
        X  A,TEMP
        LD A,BCDLO+1
        X  A,TEMP+1
        RET
ERR:    LD  A,#00E              ;ERROR MESSAGE IS DISPLAYED
        X  A,TEMP
        CLR A
        X  A,TEMP+1
        RET
;*************************************************************************
COMP:LD     A,COMPL             ;IF THE LAST BOTH MEASURMENTS ARE EQUAL
        SC                      ;THEN DISPLAY
        SUBC  A,TEMP
        IFEQ  A,#0
        JP    DISPLAY
        RET                     ;OTHERWISE DISPLAY THE OLD VALUE
DISPLAY:LD  A,TEMP
        X     A,PB+2
        LD    A,TEMP+1
M1:     X     A,PB+3
        JSR   LCDDR             ;UPDATE THE DISPLAY
        JSR   DEL               ;DELAY TIME
        RET
;*************************************************************************
SAVE: LD    A,TEMP              ;TEMPORARY SAVE
        X     A,COMPL
        LD    A,TEMP+1
        X     A,COMPH
        RET
;*************************************************************************
```

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Section 4

Non-Volatile Memory

Section 4 Contents

National Semiconductor

NM29N16
16 MBit (2M x 8 Bit) CMOS NAND FLASH E²PROM

General Description

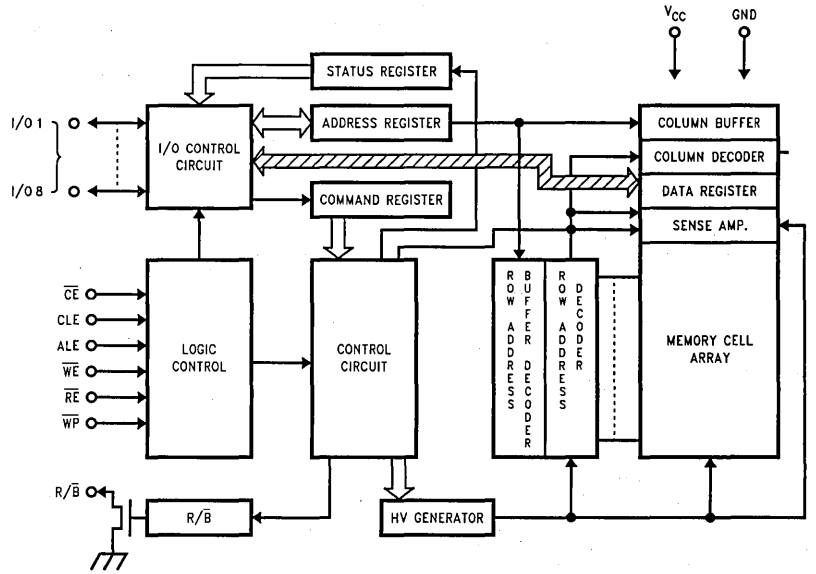
The NM29N16 is a 16 Mbit (2 Mbyte) NAND FLASH. The device is organized as an array of 512 blocks, each consisting of 16 pages. Each page contains 264 bytes. All commands and data are sent through eight I/O pins. To read data, a page is first transferred out of the array to an on-chip buffer. Sending successive read pulses ($\overline{RE}$ low) reads out successive bytes of data. The erase operation is implemented in either a single block (4 kbytes) or on multiple blocks at the same time. Programming the device requires sending address and data information to the on-board buffer and then issuing the program command. Typical program time for 264 bytes is 400 μs. All erase and program operations are internally timed.

The NM29N16 incorporates a number of features that make it ideal for portable applications requiring high density storage. These features include single 5V operation, high read/write endurance (250k cycle), and low current operation (15 mA during reads). The device comes in a TSOP Type II package which meets the requirements of PCMCIA cards. The NM29N16 is suited for numerrious applications such as Solid State Drives (SSD), Audio Recording, and Image Storage for digital cameras.

Features

- Single 5V ±5% power supply
- Write/Erase endurance of 250,000 cycles, target of 1,000,000 cycles
- Fast Erase/Program Times
  - — Average Program Time of 400 μs/264 bytes
  - — Typical Block Erase Time of 6 ms
- Organized as 512 blocks, each consisting of 16 pages of 264 bytes
  - — Read/Program in pages of 264 bytes
  - — Erase in Blocks of 4 kbytes
- High Performance Read Access times
  - — Initial 25 μs page transfer
  - — Sequential 80 ns access
- Low Operating Current
  - — Typical Read current of 15 mA
  - — Typical Program current of 40 mA
  - — Typical Erase current of 20 mA
  - — Standby current less than 100 μA (CMOS)
- Command Register for Mode Control:
  - — Read
  - — Auto Page Program
  - — Auto Block Erase
  - — Auto Multi-Block Erase
  - —Reset
  - —Suspend/Resume
  - —Status Read
- 400 mil TSOP Type II Package
- JEDEC standard pinout

Block Diagram



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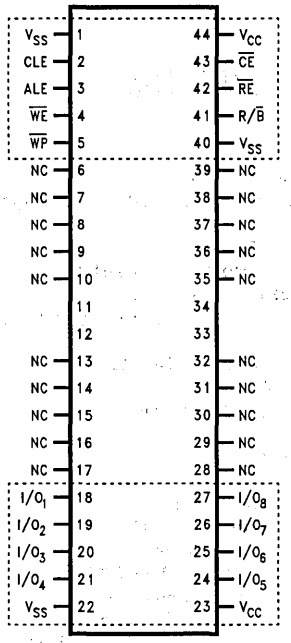
Pin Connection (Top View)

NM29N16S



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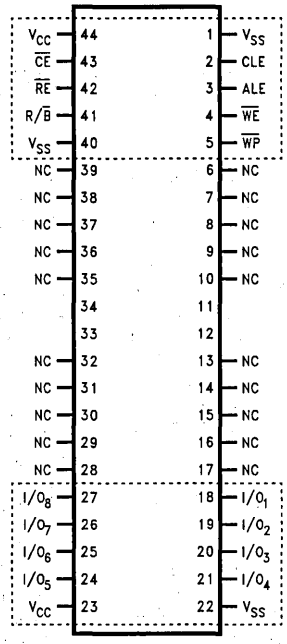
NM29N16R



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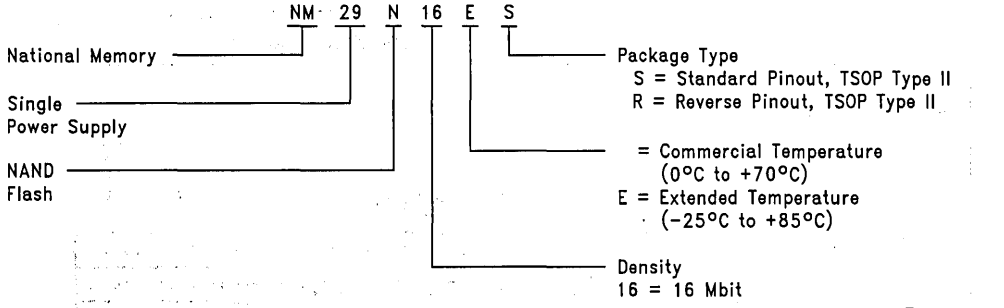
Pin Assignment

I/O_{I-8}	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
$R/\overline{B}$	Ready/Busy
V_{CC}/V_{SS}	Power Supply/Ground



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Number of Valid Blocks (1)

Symbol	Parameter	NM29N16			Units
		Min	Typ	Max	
N_{VB}	Valid Block Number	502	508	512	Blocks

Note 1: The NM29N16S/R may include unusable blocks. Refer to notification (17) toward the end of this document.

Capacitance* (T_A = +25°C, f = 1 MHz)

Symbol	Parameter	Condition	Min	Type	Max	Units
C_{IN}	Input	V_{IN} = 0V		5	10	pF
C_{OUT}	Output	V_{OUT} = 0V		5	10	pF

*This parameter is periodically sampled and is not 100% tested

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply (V_{CC})	−0.6V to 7.0V
Input Voltage (V_{IN})	−0.6V to 7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to V_{CC} ±0.5V (≤7V)
Power Dissipation (P_D)	0.5W
Soldering Temperature (T_{solder}) (10 seconds)	260°C
Storage Temperature (T_{stg})	−55°C to 150°C
Operating Temperature (T_{opr})	−25°C to 85°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Power Supply (V_{CC})	4.75	5.0	5.25	V
High Level Input Voltage (V_{IH})	2.4		V_{CC} + 0.5	V
Low Level Input Voltage (V_{IL})	−0.3*		0.6	V

* −2V (Pulse Width < 20 ns)

DC Operating Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V to V_{CC}				±10	μA
I_{CC01}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	t_{CYCLE} = 80 ns		15	30	mA
I_{CC02}	Operating Current (Serial Read)		t_{CYCLE} = 1 μs			5	mA
I_{CC03}	Operating Current (Command Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC04}	Operating Current (Data Input)	t_{CYCLE} = 80 ns			50	80	mA
I_{CC05}	Operating Current (Address Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC06}	Operating Current (Register Read)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC07}	Programming Current				40	70	mA
I_{CC08}	Erasing Current				20	45	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}				1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2V				100	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA		2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA				0.4	V
$I_{OL}(R/\overline{B})$	Output Current of (R/$\overline{B}$) Pin	V_{OL} = 0.4V			10		mA

Pin Functions

The NM29N16 is a sequential access memory which utilizes time sharing input of address and data information.

Command Latch Enable: CLE The CLE input signal is used to control the input of commands into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE The ALE signal is used to control the input of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable : $\overline{CE}$ The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in a busy state (R/$\overline{B}$ = L) such as during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input.

Write Enable : $\overline{WE}$ The $\overline{WE}$ signal is used to strobe data into the I/O port.

Read Enable: $\overline{RE}$ The $\overline{RE}$ signal strobes data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O 1–8 The I/O 1–8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect : $\overline{WP}$ The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: R/$\overline{B}$ The R/$\overline{B}$ output signal is used to indicate the operating condition of the device. The R/$\overline{B}$ signal is in a busy state (R/$\overline{B}$ = L) during the program, erase or read operations and will return to a ready state (R/$\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

AC Test Conditions

Input Level	2.4V/0.4V
Input Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1TTL & C_L (100 pF)

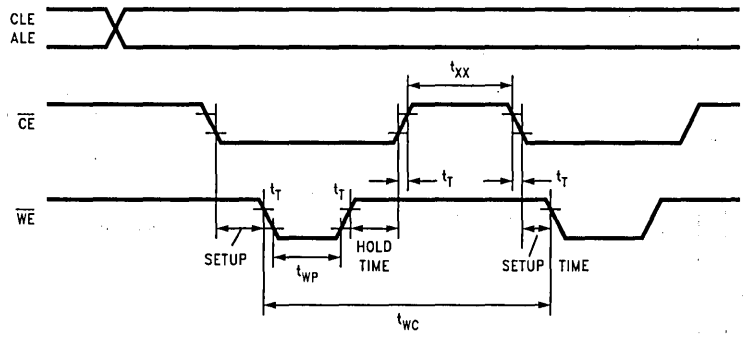
AC Electrical Characteristics (T_A = −25°C to 85°C, V_{CC} = 5V +5%)

Symbol	Parameter	Min	Max	Unit	Notes
t_{CLS}	CLE Setup Time	20		ns	
t_{CLH}	CLE Hold Time	40		ns	
t_{CS}	$\overline{CE}$ Setup Time	20		ns	
t_{CH}	$\overline{CE}$ Hold Time	40		ns	
t_{WP}	Write Pulse Width	40		ns	
t_{ALS}	ALE Setup Time	20		ns	
t_{ALH}	ALE Hold Time	40		ns	
t_{DS}	Data Setup Time	30		ns	
t_{DH}	Data Hold Time	20		ns	
t_{WC}	Write Cycle Time	80		ns	(1)
t_{WH}	$\overline{WE}$ High Hold Time	20		ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20		ns	
t_{RC}	Read Cycle Time	80		ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)		48	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in Serial Read Cycle	300		ns	(3)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)		90	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	5	20	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance		30	ns	
t_{REH}	$\overline{RE}$ High Hold Time	20		ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0		ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)		48	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)		60	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0		ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	50		ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	50		ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (Address Register Read, ID Read)	250		ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (Address Register Read, ID Read)	250		ns	
t_R	Memory Cell Array to Starting Address		25	μs	
t_{WB}	$\overline{WE}$ High to Busy		200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (Read Cycle)	150		ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (At Sequential Read)		200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at Read Mode)		100+ tr($R/\overline{B}$)	ns	(2)

AC Electrical Characteristics (T_A = −25°C to +85°C, V_{CC} = 5V ±5%) (Continued)

Note 1: In case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 80 ns. Transition time $t_T \leq 5$ ns

$$\frac{\text{set-up time}}{20\text{ ns}} + \frac{\text{hold time}}{40\text{ ns}} + \frac{t_{WP}}{40\text{ ns}} + \frac{t_{XX}}{} + \frac{4t_T}{20\text{ ns}}$$



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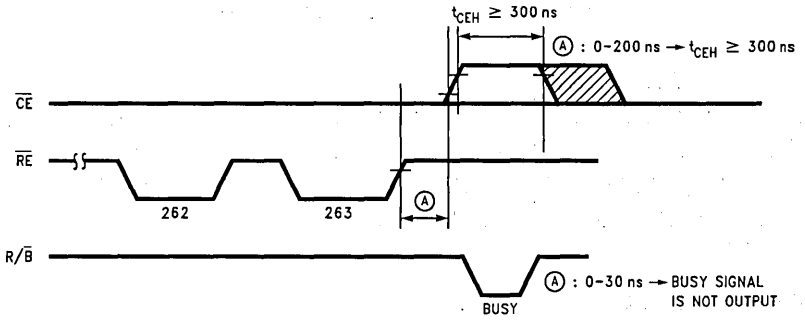
Note 2: $\overline{CE}$ high to Ready time depends on Pull up resister tied to R/$\overline{B}$ pin. (Refer to notification (11) toward the end of this document.)

Note 3: In the case that $\overline{CE}$ turns to a high level after accessing the last address (263) in read mode (1) or (2), $\overline{CE}$ high time must keep equal to or greater than 300 ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200 ns as shown below.

In the second case, the device will not turn to a "Busy" state when the $\overline{CE}$ delay time is less than 30 ns.



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Programming and Erasing Characteristic (T_A = −25°C to + 85°C, V_{CC} = 5V ±5%)

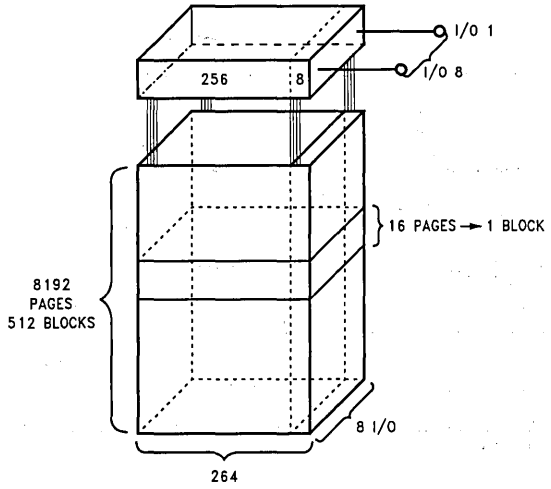
Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{PROG}	Average Programming Time		300–1000	5000	μs	
N	Divided Number on Same Page			10	Cycles	(1)
t_{BERASE}	Block Erasing Time	6	6	110	ms	
$t_{MBERASE}$	Multi-Block Erasing Time	6–12	6–12	150	ms	(2)
t_{SR}	Suspend Input to Ready			2	ms	
$N_{W/E}$	Number Write/Erase Cycles		2.5×10^5		Cycles	

Note 1: Refer to the notification (16) toward the end of this document

Note 2: $t_{MBERASE}$ depends on the number of blocks to be erased (min 6 ms + 15 μs x Erase block number)

Schematic Cell Layout and Address Assignment

Programming is done in page units of 264 Bytes while the erase operation is carried out in blocks of 4 kBytes.



A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 page = 264 bytes

1 Block = 264 bytes x 16 pages = (4k + 128) bytes

Total device density = (264 bytes) x (16 pages) x (512 block)
= 17.3 MBits (2.162 MBits)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Table I.

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FIGURE 1. NM29N16 Schematic Cell Layout

TABLE I. Addressing

	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	I/O_8
First Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
Second Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
Third Cycle	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	*L	*L	*L

* I/O 6–8 at the third cycle must be set low

A_0–A_7 : Byte (Column) Address
A_8–A_{11} : Page Address in Block
A_{12}–A_{20} : Block Address

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend, and Reset are controlled by the twelve different command operations shown in Table III. The Address, Command Input and Data Input/Output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals as shown in Table II.

TABLE II. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	*
Address Input	L	H	L	↑	H	*
Address Output	L	H	L	H	↓	*
Serial Data Output	L	L	L	H	↓	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

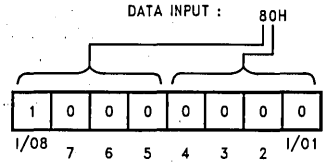
H: V_{IH}, L: V_{IL} *: V_{IH} or V_{IL}

Operation Mode: Logic and Command Tables (Continued)

TABLE III. Command Table (HEX Data)

	First Cycle	Second Cycle	Acceptable Command During Busy
Sequential Data Input	80		
Read Mode (1)	00		
Read Mode (2)	50		
Reset	FF		Yes
Auto Program	10		
Auto Block Erase	60	D0	
Auto Multi Block Erase	60...60	D0	
Suspend in Erasing	B0		Yes
Resume	D0		
Status Read	70		Yes
Register Read	E0		
ID Read	90		

Bit Assignment of HEX Data (Example)



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Once the device is set into Read mode by "00H" or "50H" command, additional Read commands are not needed for sequential page read operations. Table III shows the operation mode for Reads.

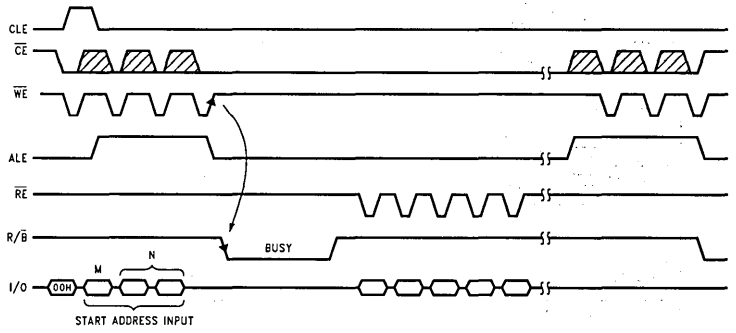
TABLE IV. Operation Mode for Reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O_1–I/O_8	Power
Read Mode	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active
Standby	L	L	H	H	*	High Impedance	Standby

Device Operation

READ MODE (1)

The Read mode (1) is set by issuing a "00H" command to the command register. Refer to *Figure 2* below for timing details and block diagram.



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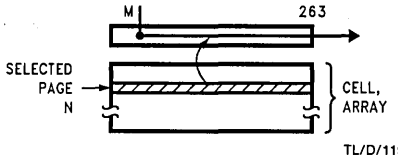

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A data transfer operation from the cell array to the register starts at the rising edge of $\overline{WE}$ in the third cycle (after latching the address information). The device will be in a busy state during this transfer period.

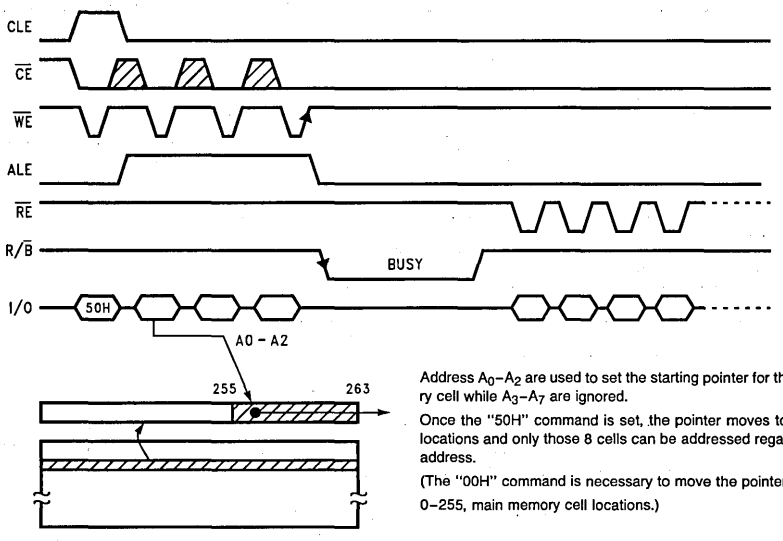
After the transfer period the device returns to a ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the designated starting pointer indicated during the address input cycle.

FIGURE 2. Read Mode (1) Operation

Device Operation (Continued)

READ MODE (2)

The Read mode (2) is the same timing as Read mode (1) but it is used to access information in the extra 8 byte redundancy area of the page. The starting pointer is therefore assigned between byte 256 and 263.



Address A_0–A_2 are used to set the starting pointer for the redundant memory cell while A_3–A_7 are ignored.

Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed regardless of the A_3–A_7 address.

(The "00H" command is necessary to move the pointer back to the 0–255, main memory cell locations.)

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FIGURE 3. Read Mode (2) Operation

SEQUENTIAL READ (1) (2)

This mode allows sequential read without the additional address input

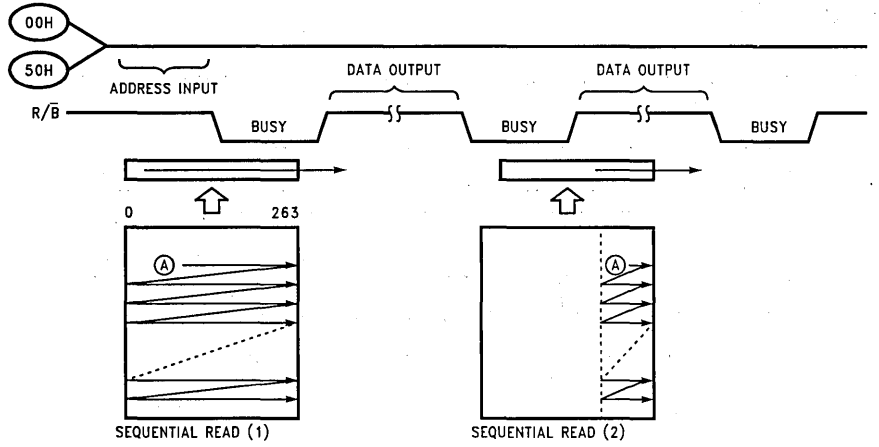

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FIGURE 4. Sequential Read

Sequential Read mode (1) outputs the address 0 to 263 while Sequential Read mode (2) outputs the redundant address location only. When the pointer reaches the last address, the device continues to output last data with each $\overline{RE}$ clock signal.

Device Operation (Continued)

STATUS READ

The NM29N16S/R automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the Ready/Busy status of the device, determines the pass/fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table V.

TABLE V. Status Output Table

	Status	Output	
I/O 1	Pass/Fail	Pass: "0"	Fail : "1"
I/O 2	Not Used	"0"	
I/O 3	Not Used	"0"	
I/O 4	Not Used	"0"	
I/O 5	Not Used	"0"	
I/O 6	Suspend	Suspended: "1"	Not suspended: "0"
I/O 7	Ready/Busy	Ready: "1"	Busy: "0"
I/O 8	Write Protect	Protect: "0"	Not Protect: "I"

The Pass/Fail status in I/O 1 is only valid when the device is in the Ready state. The device will always indicate a Pass status while in the Busy state at Read mode.

Application example with multiple devices is shown in *Figure 5* below.

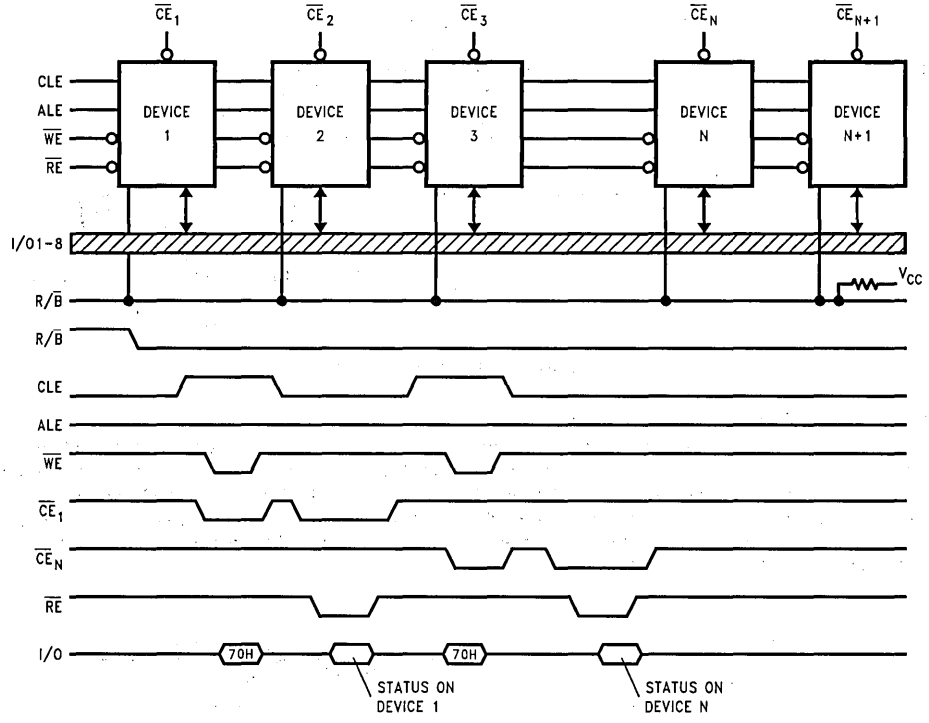

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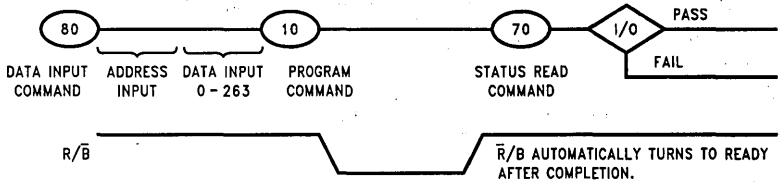
FIGURE 5. Status Read Timing Application Example

Note: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status Read function can be used to determine the status of each individually selected device.

Device Operation (Continued)

AUTO PAGE PROGRAM

The NM29N16S/R implements the automatic page program operation by receiving a "10H" program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detail timing chart).



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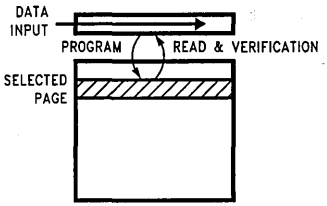

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The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the "10H" command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

If the device failed, the bit by bit pass/fail result can be verified by the following sequence:

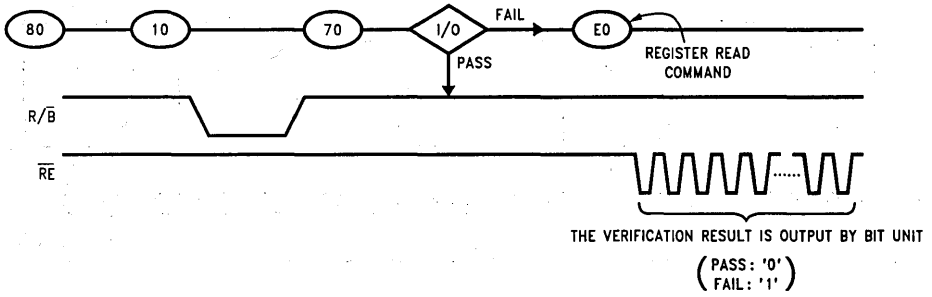

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FIGURE 6. Auto Page Program

AUTO BLOCK ERASE/AUTO MULTI-BLOCK ERASE

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command "D0H" which follows the erase setup command "60H". This two cycle process for erase operations acts as an extra layer protection from accidental erasure of data due to possible external noise issues. The device automatically executes the erase and verify operations.

Multiple blocks can be simultaneously erased by inputting the "60H" setup command and the block address for all desired blocks before issuing the "D0H" command to start the erase operation. The length of the erase busy period will depend upon the number of blocks. The command sequence is shown as follows:

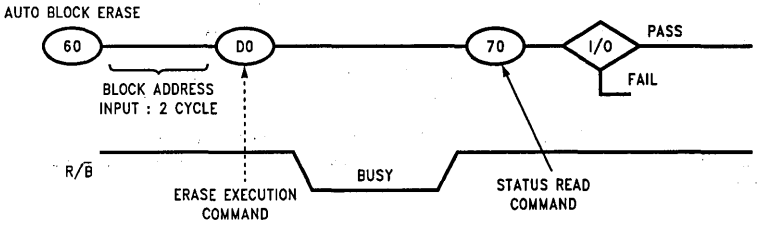

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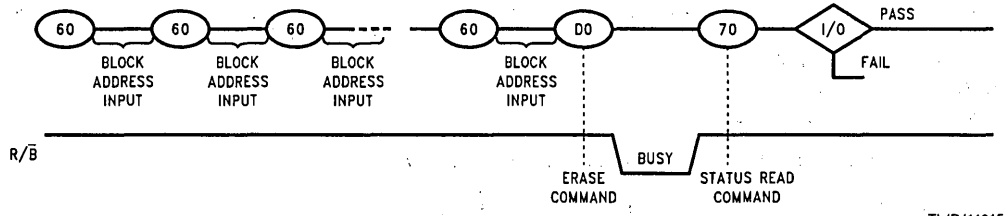
FIGURE 7. Auto Block Erase Operation

Device Operation (Continued)

AUTO MULTI BLOCK ERASE



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Busy duration will be approximately (erase time + verify time) calculated as, $t_{MBERASE}$ = 6 ms + 15 μs × Erase block number

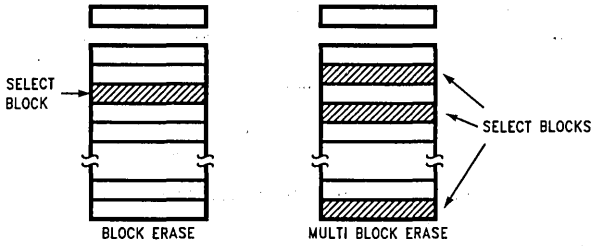

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FIGURE 8. Auto Block/Auto Multi Block Erase Operation

SUSPEND/RESUME ERASE OPERATION

Because a multi-block erase operation can keep the device in a busy state for an extended period of time, the NM29N16S/R has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence on this operation are shown as below. (Refer to the detail timing chart).

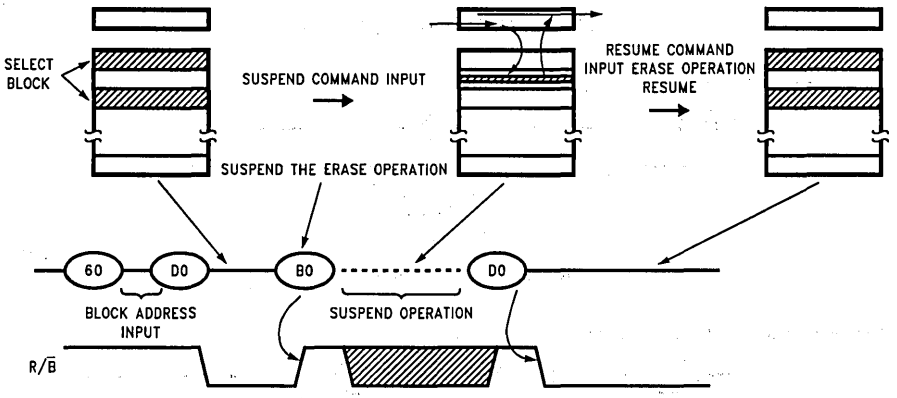

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FIGURE 9. Suspend/Resume Erase Operation

The B0...D0 suspend/resume cycle can be repeated up to 20 times during a multi-block erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

Device Operation (Continued)

RESET

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go to a wait state. The address and data register are set as follows after a reset:

- Address Register: All "0"
- Data Register: All "1"
- Operation Mode: Wait State

The response after "FFH" reset command input during each operation is as follows:

- In the case that reset (FFH) command is input during programming:

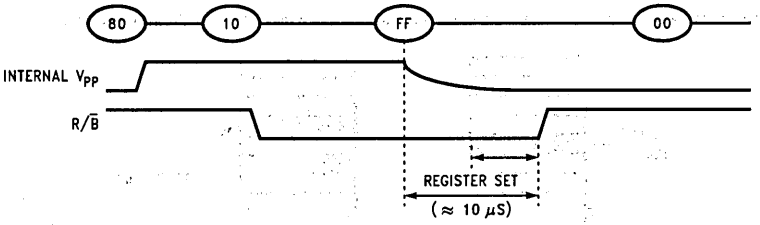

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FIGURE 10. Reset During Programming

- In the case that reset (FFH) command is input during erasing:

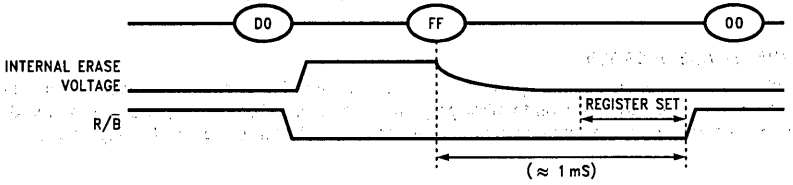

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FIGURE 11. Reset During Erasing

- In the case that reset (FFH) command is input during read operation:

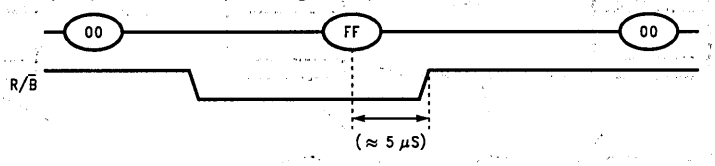

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FIGURE 12. Reset During Read

- In the case that reset (FFH) command is input during suspend:

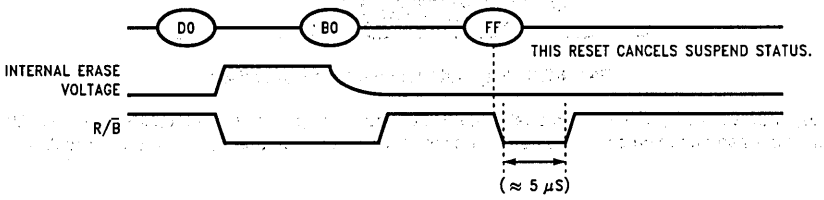

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FIGURE 13. Reset During Suspend

Device Operation (Continued)

- In the case that the status read command (70H) is input after reset:

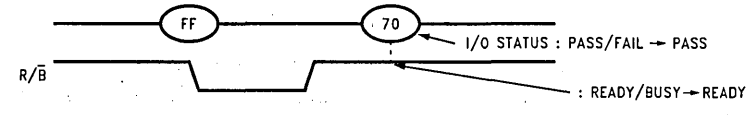


FIGURE 14. Read After Reset

- However the following operation is prohibited. If the following operation is executed, set up for address and data register can not be guaranteed.

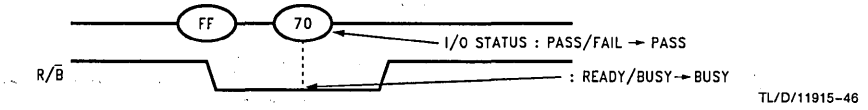


FIGURE 15. Prohibited Reset

- In the case that the reset command is input in succession:

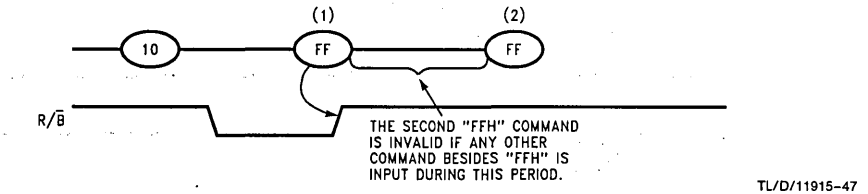


FIGURE 16. Consecutive Resets

ID READ

The NM29N16S/R contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

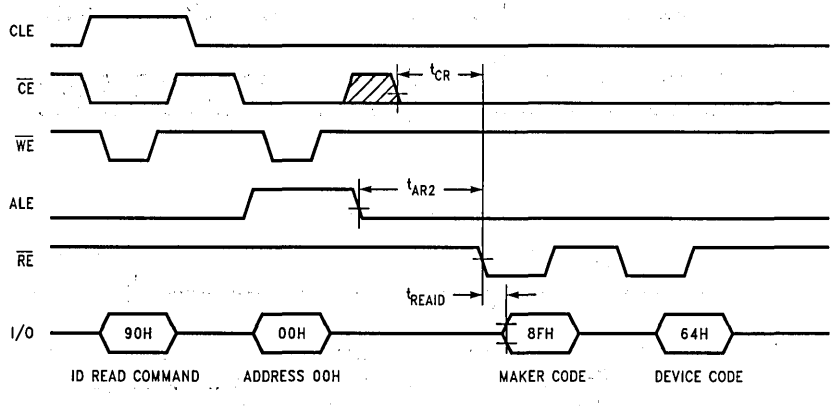


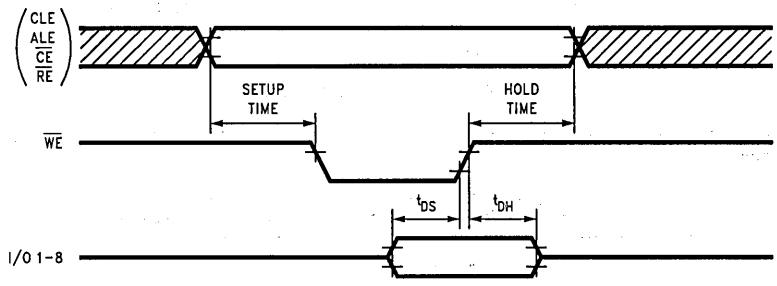
TABLE VI. Code Table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker Code	1	0	0	0	1	1	1	1	8FH
Device Code	0	1	1	0	0	1	0	0	64H

Refer to the timing specifications for the access time of t_{READ}, t_{CR}, t_{AR2}.

Timing Diagrams

Latch Timing Chart for Command/Address/Data



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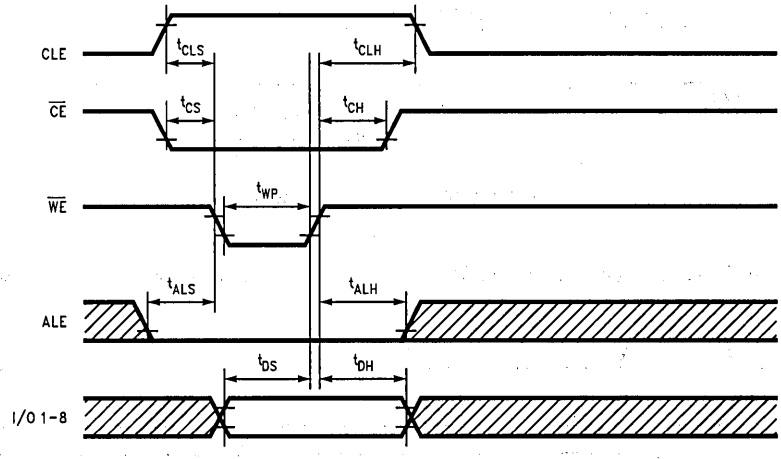
Command Input Cycle



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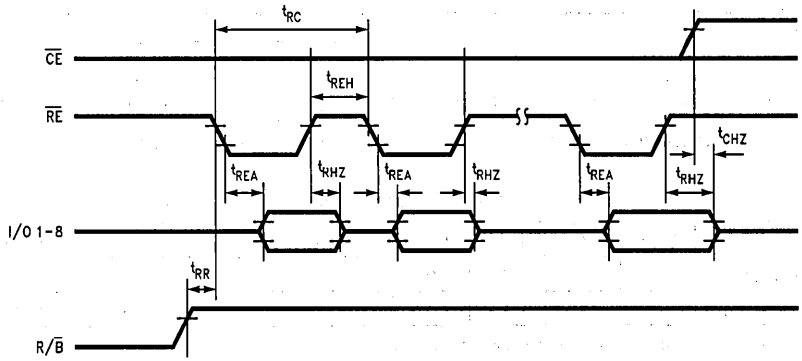
Serial Read Cycle



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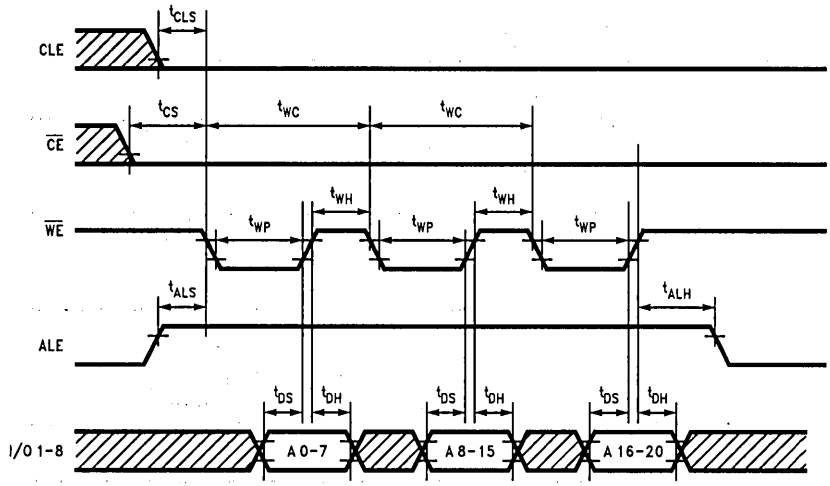
Timing Diagrams (Continued)

Address Input Cycle



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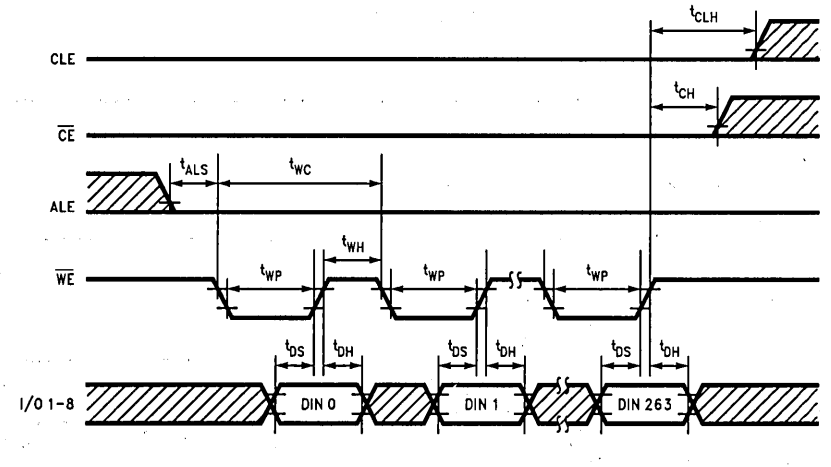
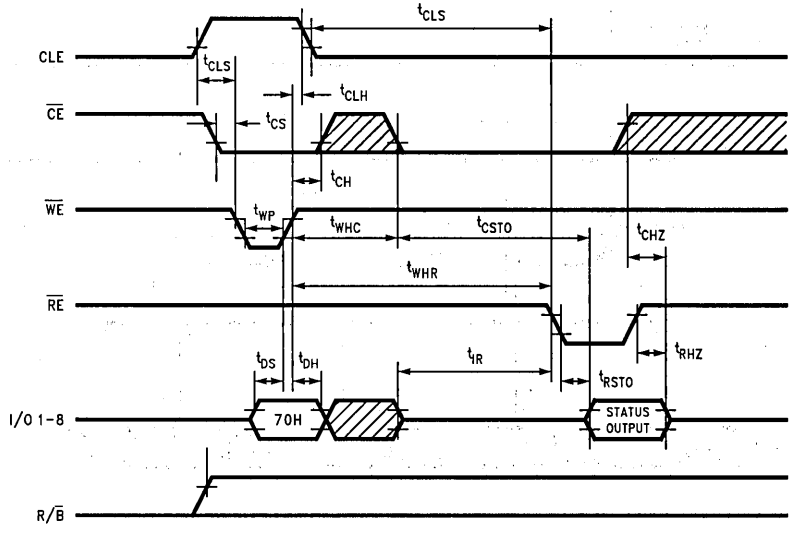
Data Input Cycle



TL/D/11915–10

Timing Diagrams (Continued)

Status Read Cycle



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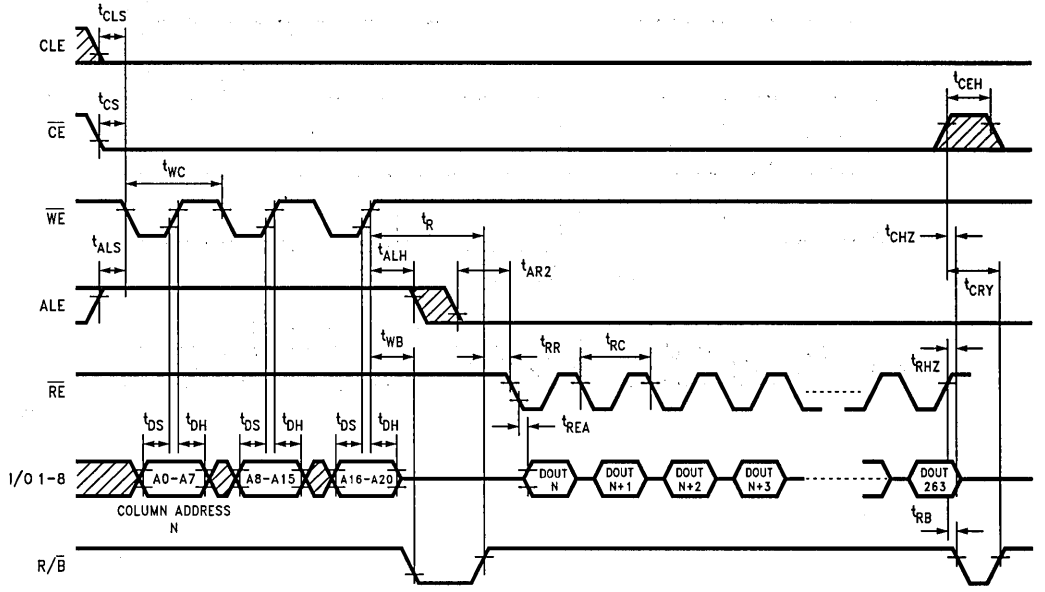
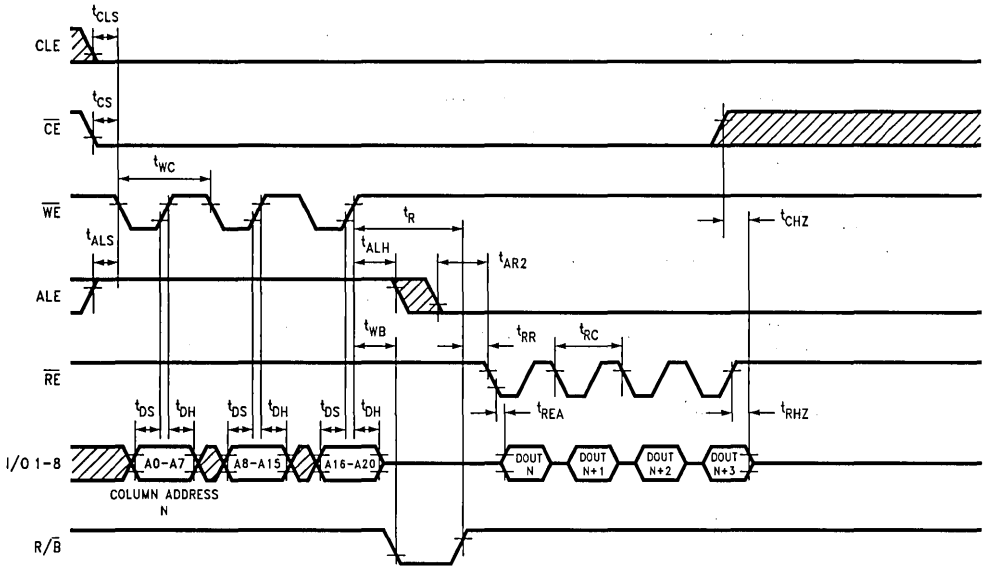
Read Cycle (1)



TL/D/11915–12

Timing Diagrams (Continued)

Read Cycle (1): Terminated by $\overline{CE}$



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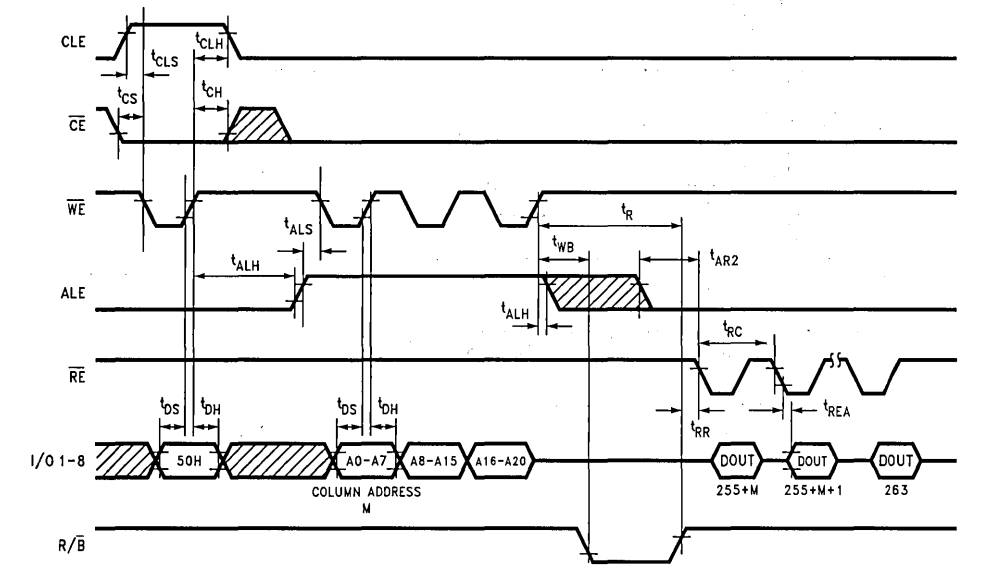
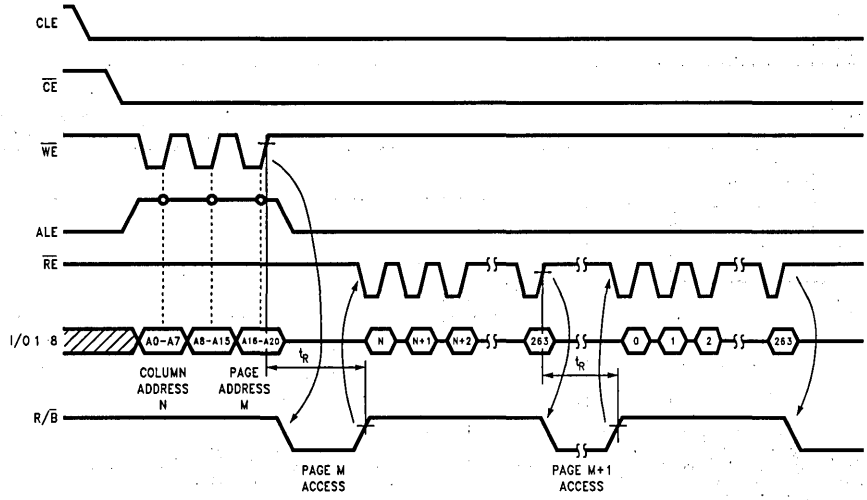
Read Cycle (2)



TL/D/11915–14

Timing Diagrams (Continued)

Sequential Read Timing



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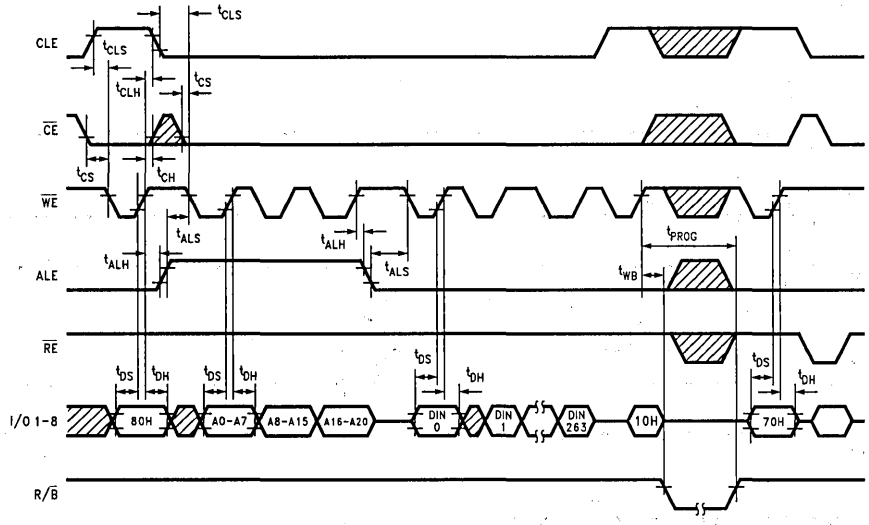
Auto Program Timing Chart



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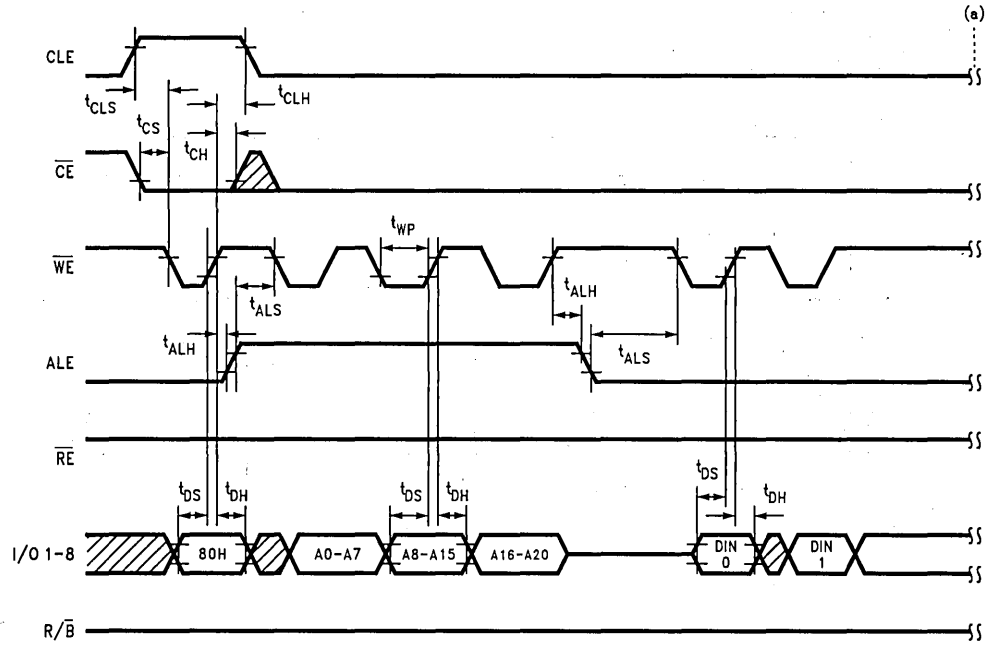
Timing Diagrams (Continued)

Auto Program and Register Read



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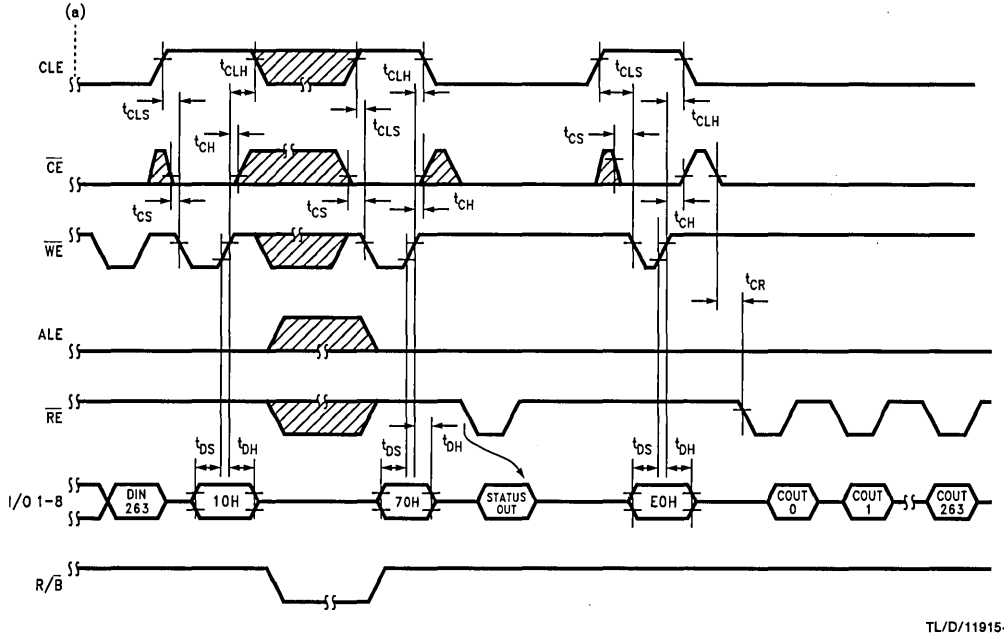
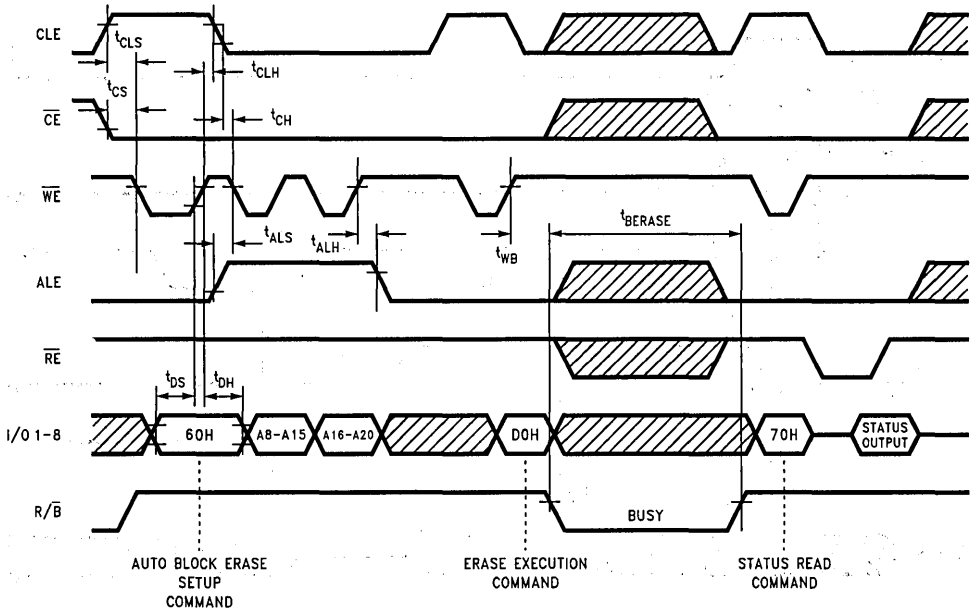


TL/D/11915-18

(a): Continued

Timing Diagrams (Continued)

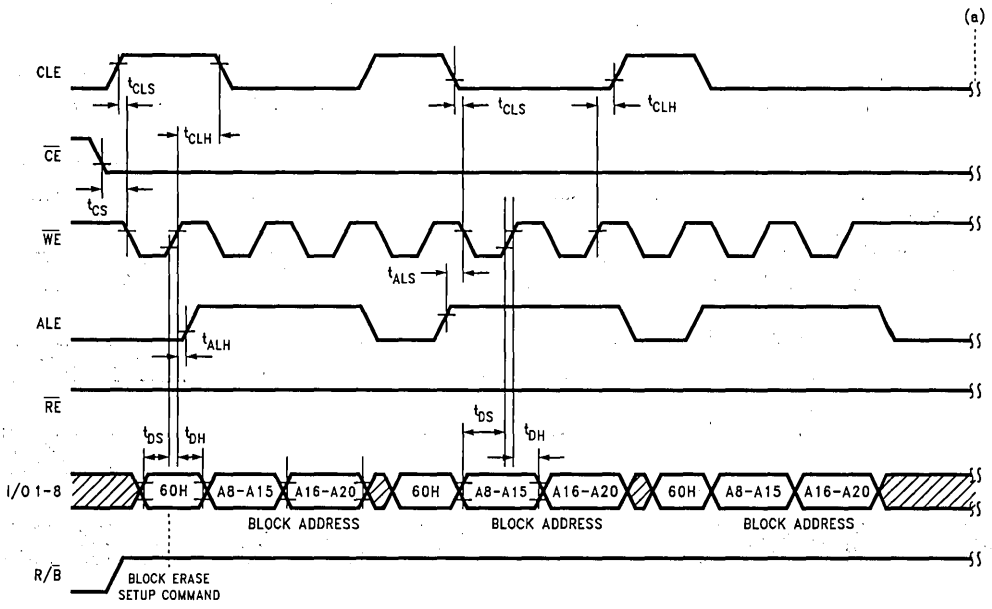
Auto Block Erase Timing



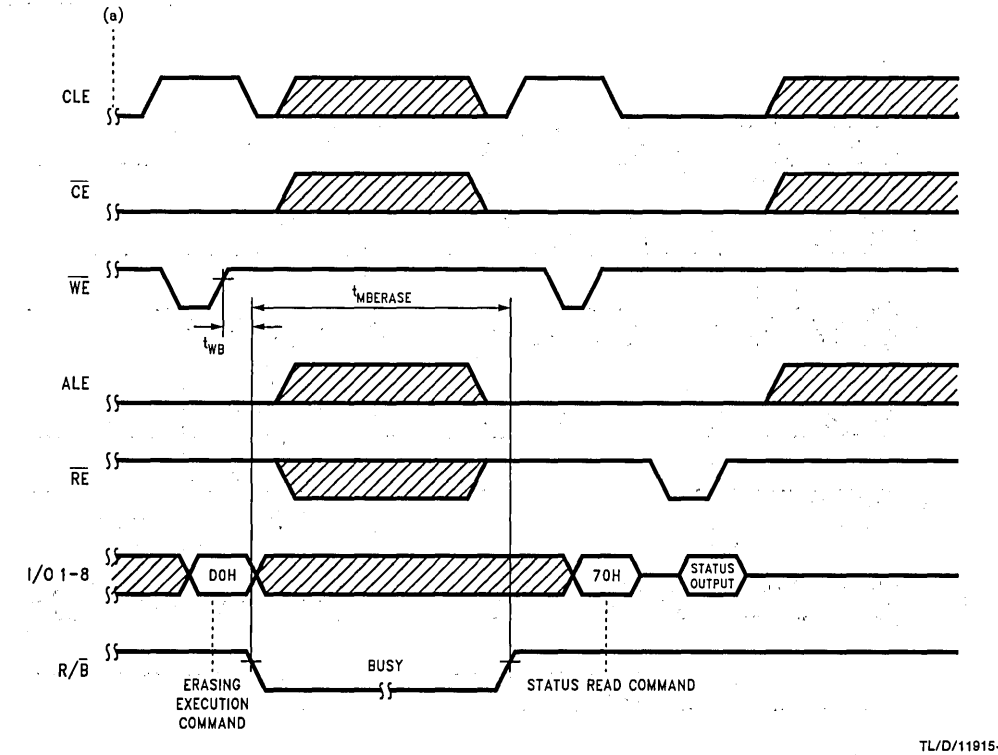
TL/D/11915-19

Timing Diagrams (Continued)

Auto Multi Block Erase Timing



TL/D/11915–20

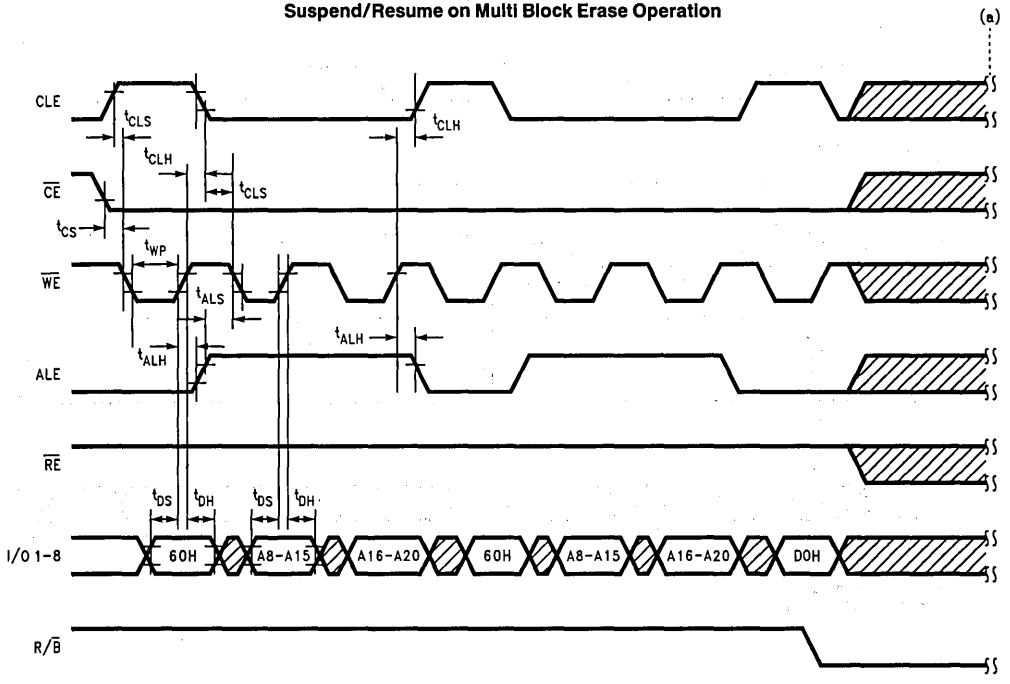


TL/D/11915–21

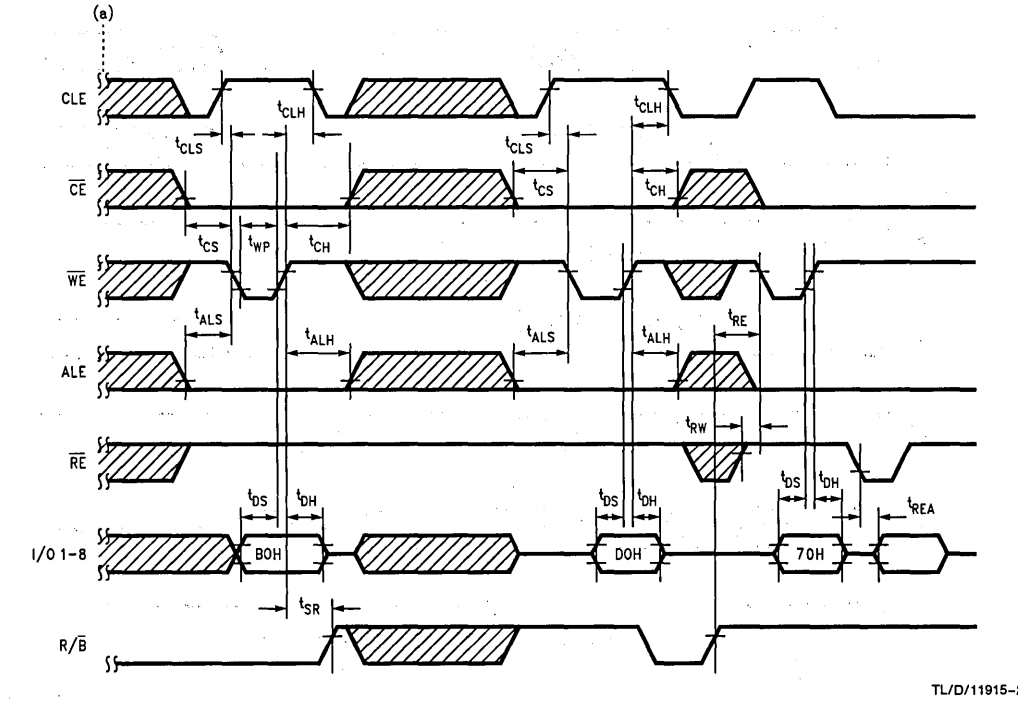
(a): Continued

Timing Diagrams (Continued)

Suspend/Resume on Multi Block Erase Operation



TL/D/11915-22

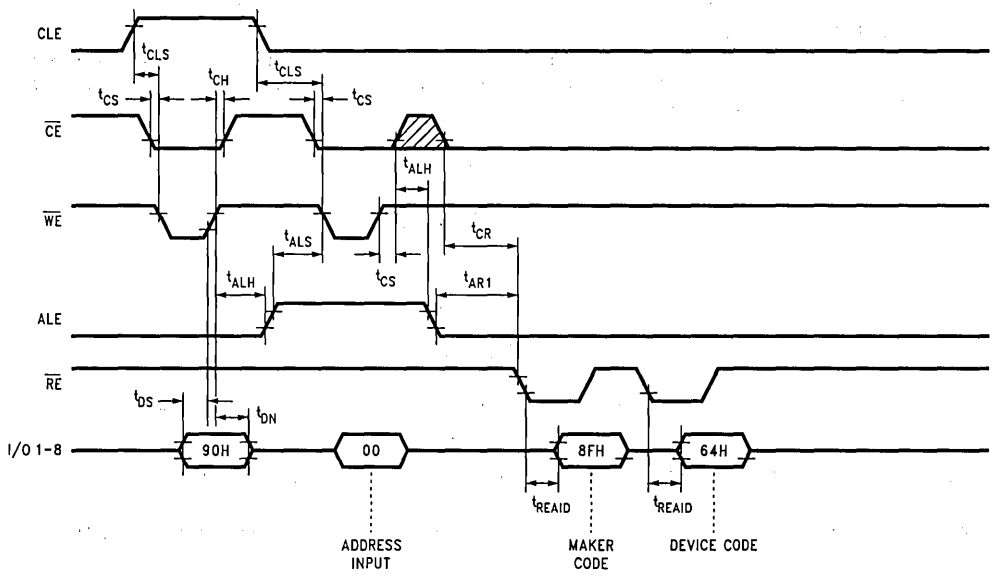


TL/D/11915-23

(a): Continued

Timing Diagrams (Continued)

ID Read Operation



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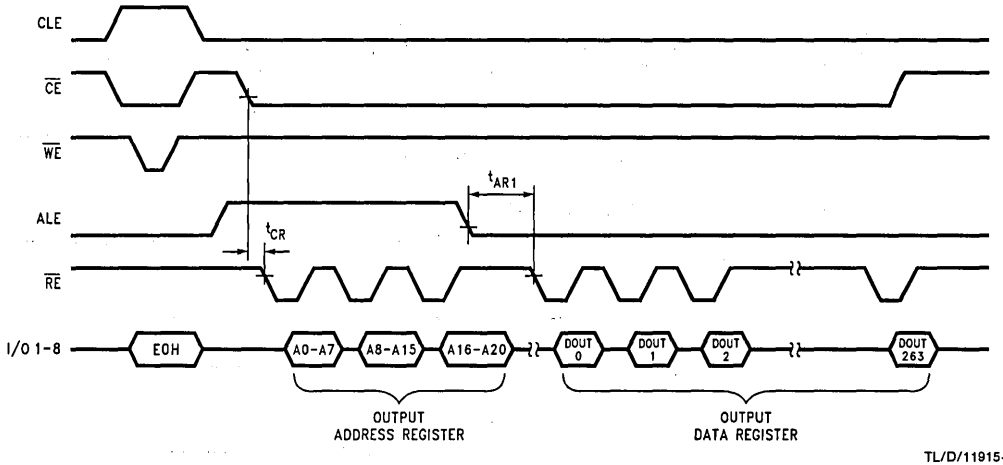
Register Read Cycle



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Supplementary Device Operation

(1) PROHIBITION OF UNSPECIFIED COMMANDS

The operation commands are listed in Table III. Data input as a command other than the specified commands in Table III is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) POINTER CONTROL FOR "00H", "50H"

The NM29N16S/R has two read modes to set the destination of the pointer in either the main memory area of a page or the redundancy area. The pointer can be designated at any location between 0 and 255 in read mode (1) and between 256 and 263 in read mode (2). *Figure 17* shows the block diagram of their operations.

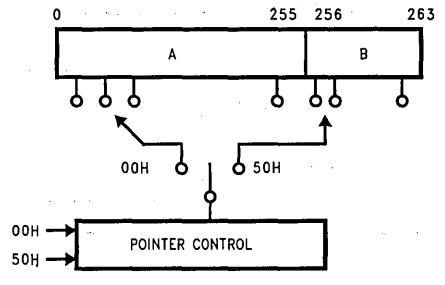

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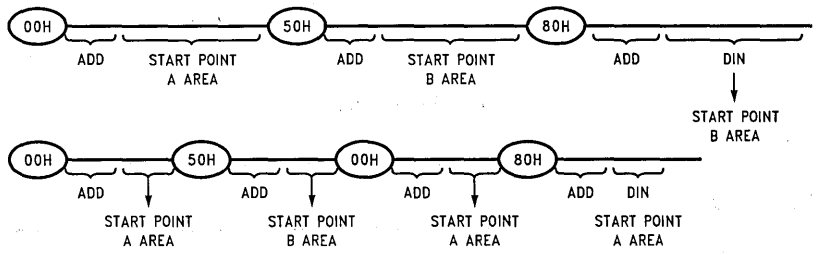
FIGURE 17. Pointer Control

The pointer is set to region "A" by the "00H" command and to region "B" by the "50H" command.

(Example)

The "00H" command needs to be input to set the pointer back to region "A" when the pointer exists in region "B".



TL/D/11915–50

FIGURE 18. Example for Pointer Set

(3) ACCEPTABLE COMMANDS AFTER SERIAL INPUT COMMAND OF "80H"

Once the serial input command ("80H") is input, do not input any command other than the program execution command ("10H") or the reset command ("FFH") during programming.

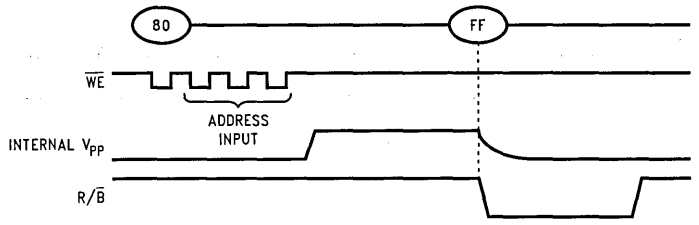


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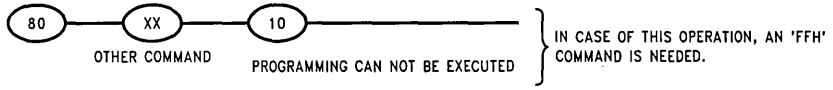
FIGURE 19. Reset After Serial Input

If a command other than "10H" or "FFH" is input, the program operation is not performed.



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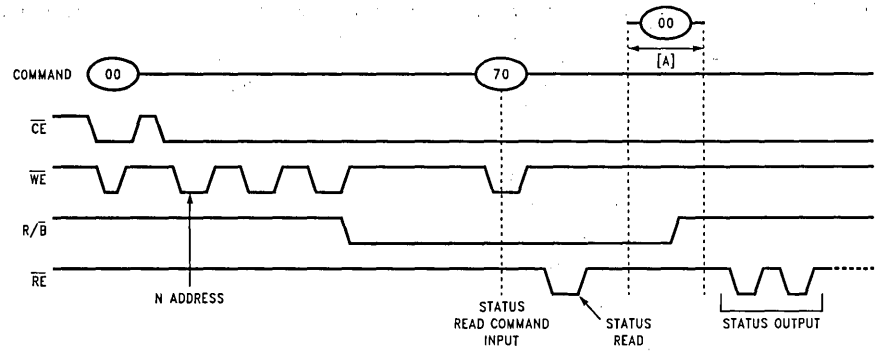
Supplementary Device Operation (Continued)

(4) STATUS READ DURING READ OPERATION



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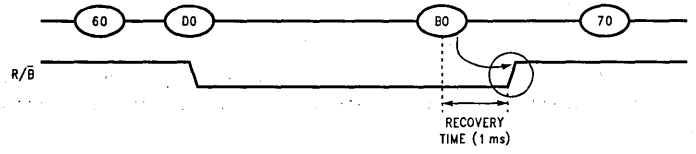
The device status can be read out by inputting the status read command "70H" during the read mode. Once the device is set to the status read mode after the "70H" command input, the device does not return to the read mode. Therefore, the status read during the read operation is prohibited. However, when the read command "00H" is input during [A], the status mode is reset, then the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) SUSPEND COMMAND "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.



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Although the device status changes from busy to ready after "B0H" is input, the following two cases cannot be recognized.

— After a "B0H" command input, Busy → Ready

— After an erase operation is finished with "D0H", Busy → Ready

Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to ready.

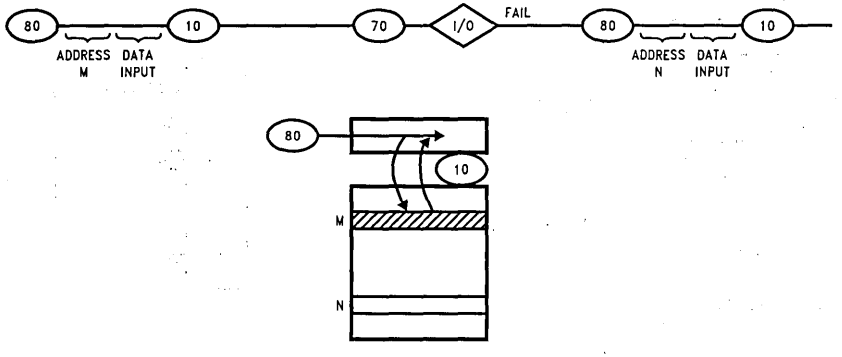
The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

— "B0H" has been accepted : Erase operation is executed. (The device is busy.)

— "B0H" has not been accepted. (Erase operation has been completed) : "D0H" command cannot be accepted. (The device is in ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) PROGRAM FAIL



TL/D/11915–55

FIGURE 20. Program Fail

When the programming result for the page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

Supplementary Device Operation (Continued)

(7) DATA TRANSFER

The data in page Address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e., "1" data will become "0" and "0" will become "1").

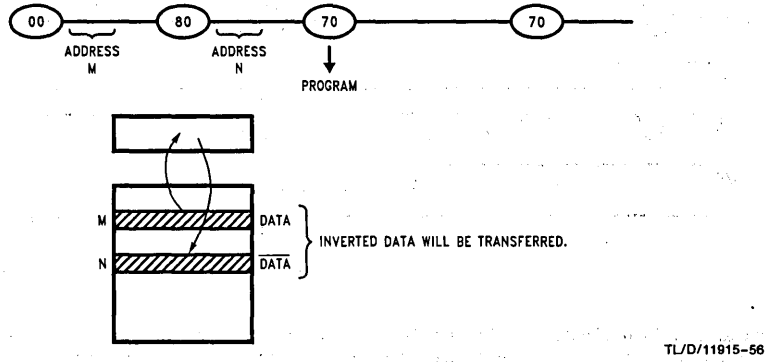
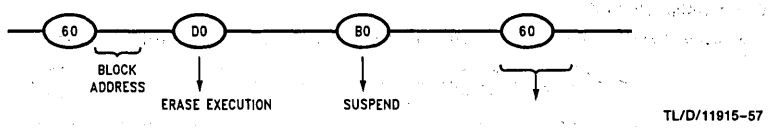


FIGURE 21. Page to Page Transfer

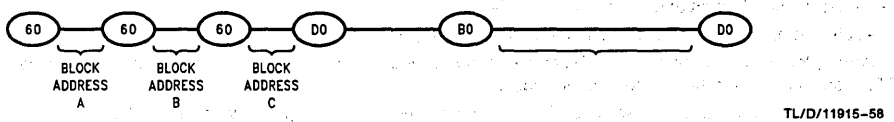
(8) BLOCK ERASE AFTER SUSPEND COMMAND "B0H"



A block erase command is prohibited when the device has been suspended by inputting "B0H" during a block erase or multi-block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

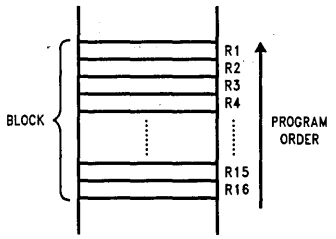
(9) INTERRUPTION OF AN ERASING BLOCK

After a "B0H" command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



(10) ADDRESSING FOR PROGRAM OPERATION

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block (i.e., Row 16 must be programmed before row 15, etc.). Random page address input is prohibited. Programming must be executed in order from the NAND cell transistor closest to ground to the one closest to the bit line. Refer to the diagram below.



Correspondence of internal and external address

NAND address → A_8–A_{11} { 000: R16 ↓ 111: R1

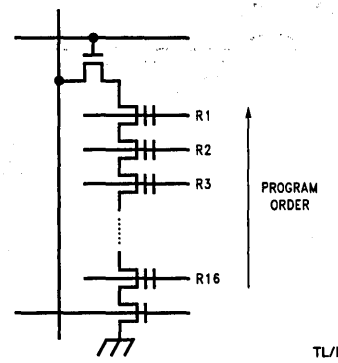


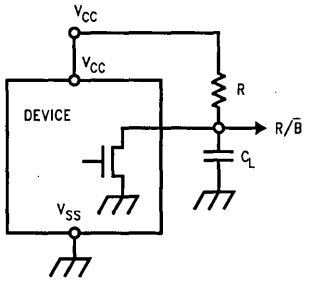
FIGURE 22. Page Program In Order within a Block

The order of the external address from A_8 to A_{11} corresponds to the device internal page address from R16 to R1.

Supplementary Device Operation (Continued)

(11) R/$\overline{B}$: TERMINATION FOR THE READY/BUSY PIN (R/$\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.



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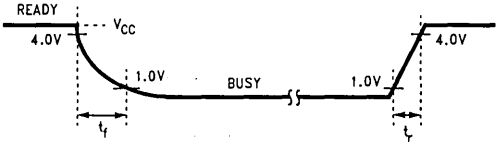
This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.



TL/D/11915-62

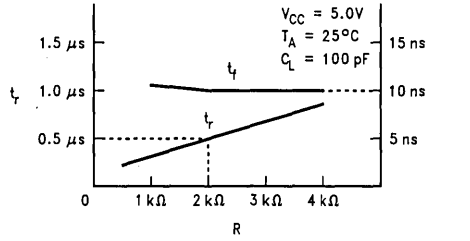


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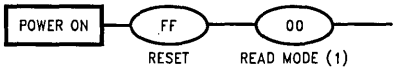
FIGURE 23. Ready/Busy Pin Termination

(12) STATUS AFTER POWER ON

Although the device is set to read mode after power-up, the following sequence is recommended because each input signal may not be stable at power on.

- Operation mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminacy
- High voltage generation circuit : Off state

Recommended sequence



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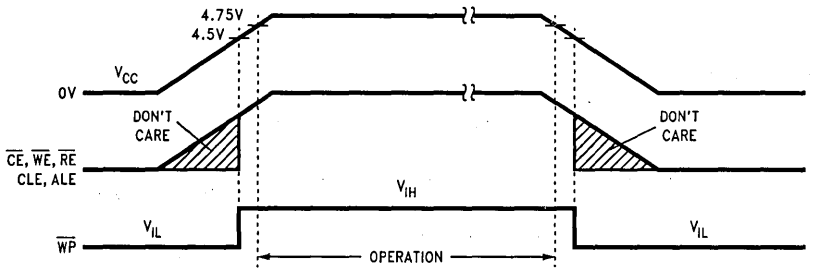
(13) POWER ON/OFF SEQUENCE

The $\overline{WP}$ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:



TL/D/11915-65

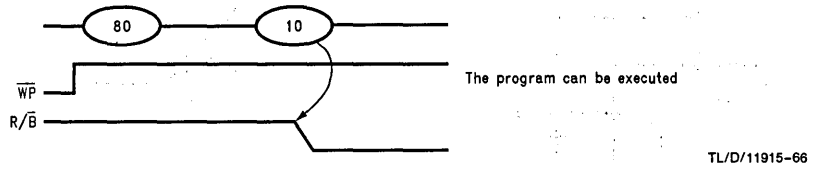
FIGURE 24. NM29N16 Power On/Off Sequence

Supplementary Device Operation (Continued)

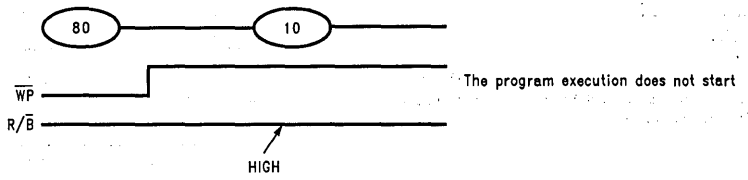
(14) NOTIFICATION FOR $\overline{WP}$ SIGNAL

The erase and program operations are reset when $\overline{WP}$ goes low. The following conditions must be recognized:

Program

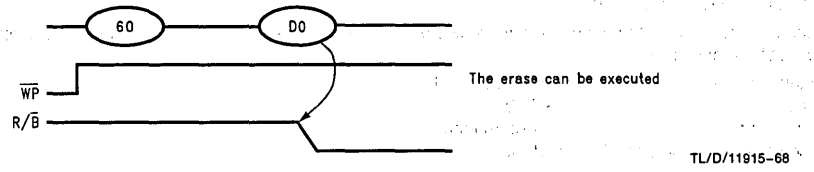


TL/D/11915-66

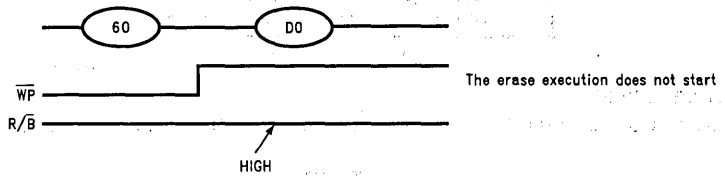


TL/D/11915-67

Erase

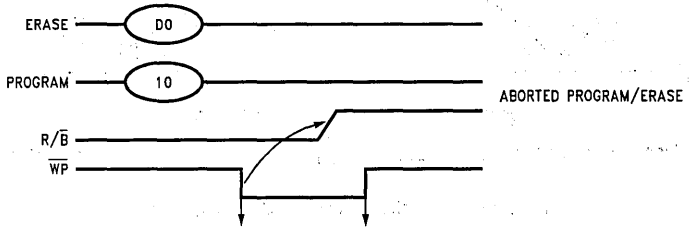


TL/D/11915-68



TL/D/11915-69

In the case that $\overline{WP}$ goes high during erase/program operation



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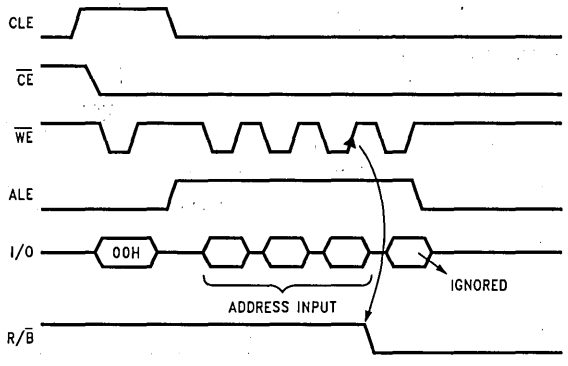
The previous operation is reset even when $\overline{WP}$ returns to high level and the device waits for the next command. The same loading sequence as after the reset command is needed to restart the operation.

Supplementary Device Operation (Continued)

(15) IN THE CASE THAT 4 ADDRESS CYCLES ARE INPUT

Although the device may acquire the fourth address, it is ignored inside the chip.

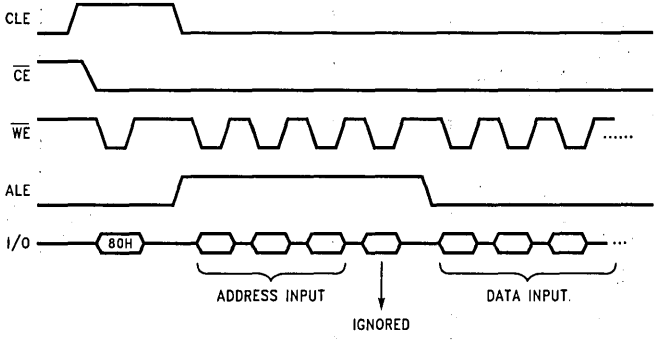
At Read operation:



TL/D/11915-71

FIGURE 25

At programming operation:

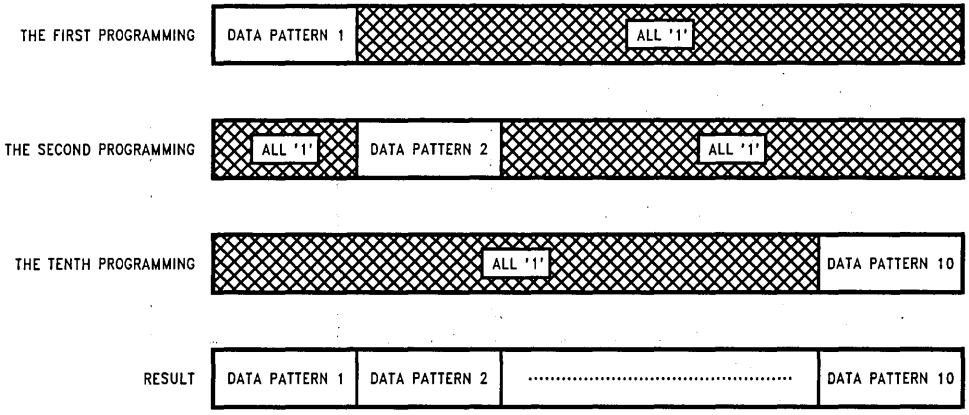


TL/D/11915-72

FIGURE 26

(16) DIVIDED PROGRAM IN THE SAME PAGE (PARTIAL PAGE PROGRAM)

The device allows a page to be divided typically into 10 segments and to program each page segment selectively as follows:



TL/D/11915-73

FIGURE 27

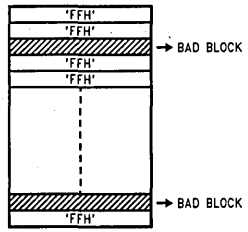
Note: The input data of unprogrammed or previously programmed page segments must be "1". (i.e., Mask all page bytes outside the segment to be programmed with "1" data.)

Supplementary Device Operation (Continued)

(17) BAD BLOCK IDENTIFICATION

The NM29N16 may contain unusable blocks. To simplify identification, usable or good blocks leave the factory in the erased state. On initial power up (after board assembly), reading all the bytes in a usable block will result in FFH being read out. Unusable or bad blocks will read out some data other than FFH. These blocks should be mapped out of the system and not used. The valid number of blocks is as follows:

	Min	Typ	Max	Unit
Number of good blocks	502	508	512	Block



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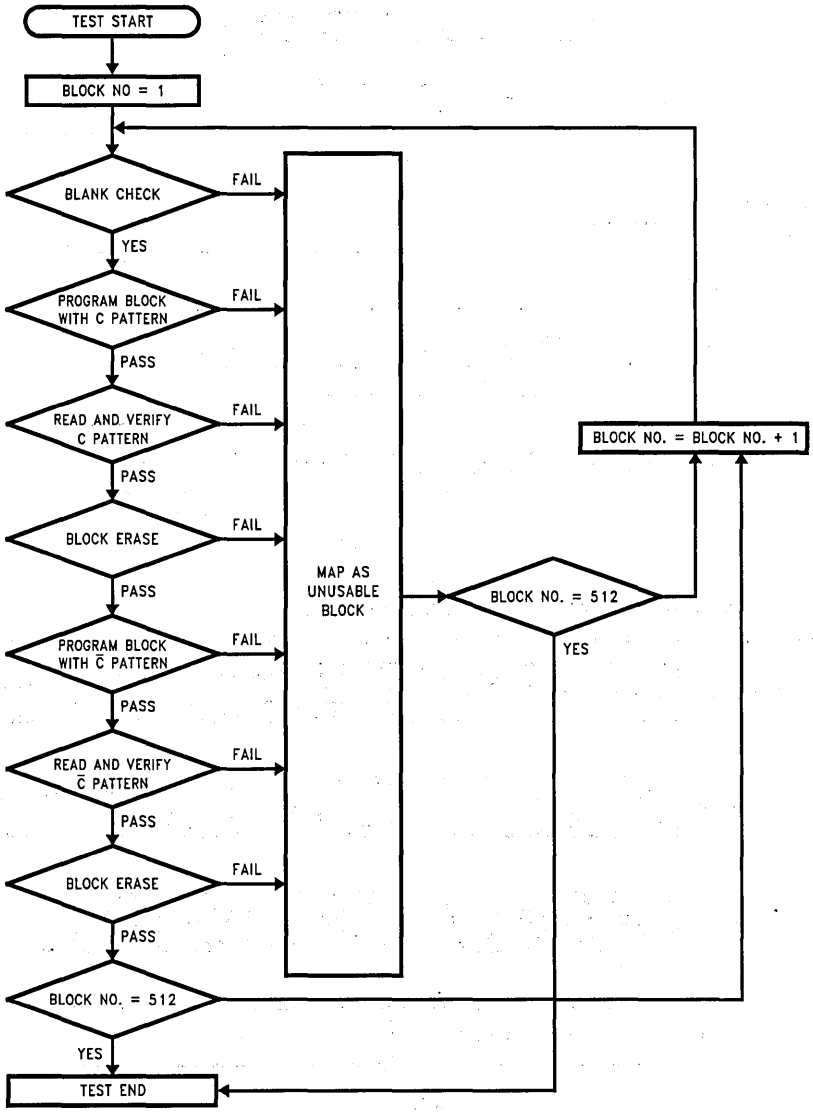
C: Checkboard Pattern, AAH
$\overline{C}$: Inverse Checkerboard Pattern, 55H
Blank Check: Usable blocks will read out 'FFH' for all bytes in block



TL/D/11915–4

FIGURE 37. Identification of Bad Blocks at Initial Power Up

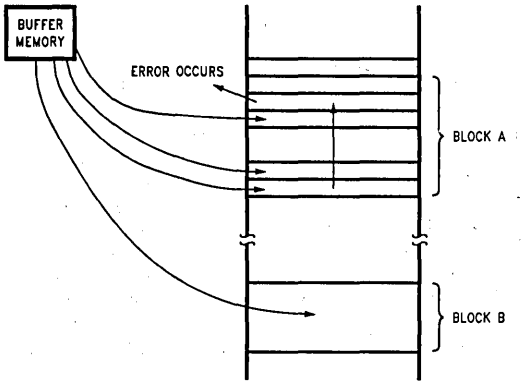
Supplementary Device Operation (Continued)

(18) ERROR IN PROGRAM OR ERASE OPERATION (FAIL AT STATUS READ)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs:

Program

When the error happens in Block A, try to reprogram the data into another Block B by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad block" table or other appropriate scheme).



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Erase

When the error oocurs after an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme).

National Semiconductor

PRELIMINARY

NM29A040
4-Mbit CMOS Serial FLASH E²PROM

General Description

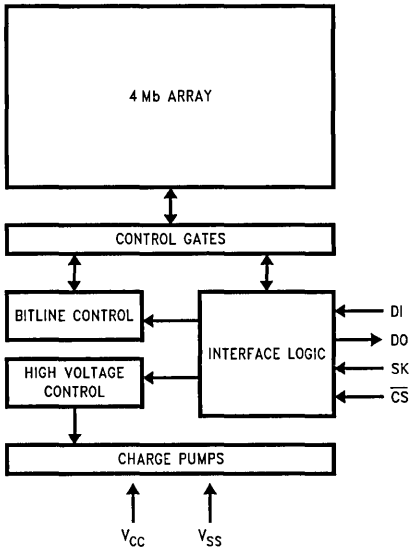
The NM29A040 is a 4-Mbit Flash memory designed with a MICROWIRE™ serial interface. All of the features of the device are designed to provide the most cost effective solution for applications requiring low bandwidth file storage. Examples of these applications include digital answering machines and personal digital recorders (digital audio) or FAX and digital scanners (digital imaging). The Serial Flash requires only a single 5V power supply, has a small erase block size (4 kbytes) and a low EMI serial interface.

The NM29A040 has been designed to work seamlessly with National's CompactRISC™ family (e.g. NSAM266). In this manner National is able to provide the complete system solution to digital audio recording (processor, CODEC, Flash memory, software) or digital imaging.

Features

- Single 5V ±10% power supply
- 4 kbyte erase block
- Organized as 128 Blocks per 4-Mbit Device
  - 128 pages per block
  - 32 bytes per page (256 bits)
- MICROWIRE™ compatible interface
- Low operating current (typical)
  - 5 mA read current
  - 15 mA write current
  - 10 mA erase current
  - 5 μA standby current
- Target 100k write/erase cycle endurance
- Offered in PLCC and SOIC packages

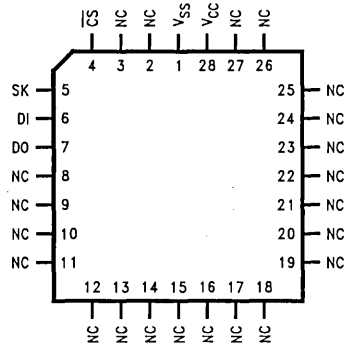
Block Diagram



TL/D/12475–1

Connection Diagrams

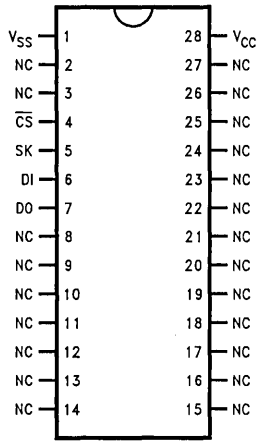
Plastic Chip Carrier (V)



TL/D/12475–2

NS Package Number V28A

Small Outline Package (M)



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NS Package Number MA28A

Pin Assignments

DO	Serial Data Output
DI	Serial Data Input
SK	Serial Data Clock
$\overline{CS}$	Chip Select
NC	No Connection

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM29A040V
NM29A040M

Extended Temp. Range (−40°C to +85°C)

Order Number
NM29A040EV
NM29A040EM

Pin Functions

SERIAL DATA INPUT: DI

The DI pin is used for transferring in commands and data. Data is latched on the rising edge of SK.

SERIAL DATA OUT: DO

The DO pin is used for transferring out status and data. Data output will change following the falling edge of SK.

CHIP SELECT: $\overline{CS}$

This signal indicates which device is selected. When this signal is inactive the device ignores SK. This signal can be tied to ground when there is only one Serial Flash device. The $\overline{CS}$ pin may be pulled high to reset the device.

SERIAL DATA CLOCK: SK

This is the standard synchronous MICROWIRE clock which determines the rate of data transfer. On each toggle, one data bit is shifted into or out of the Serial Flash.

System Concepts

The NM29A040 is a 4-Mbit NAND Flash designed to provide the most cost effective solution for file storage applications. These applications include digital audio recording, digital image storage and data logging applications.

For digital audio storage, the NM29A040 has been matched with National's NSAM266 voice processor. Applications that can benefit from this combination include digital answering machines, personal digital recorders, pagers and voicemail systems. When combined with National Semiconductor's CompactSPEECH™ embedded software and the NSAM266 processor, customers can quickly bring to market systems capable of recording up to 15 minutes of audio on a single 4 Mb device. Multiple NM29A040's can be used to extend the record time.

Digital imaging applications include FAX machines, handheld scanners and digital cameras. Combining the NM29A040 with the CompactRISC family of embedded processors can enable complete solutions for image storage.

Data logging applications can take advantage of the NM29A040's simple interface and nonvolatility to allow simple 8-bit microcontroller based systems to have access to over 4 Mb of storage. The nonvolatility ensures data integrity in remote, battery powered applications.

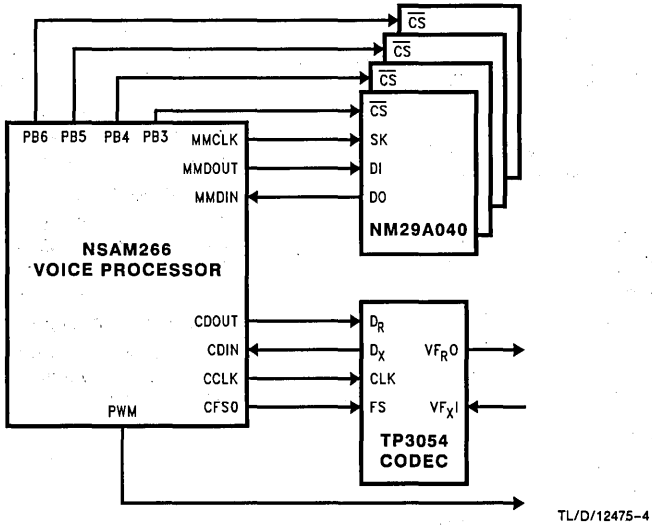

FIGURE 1. Digital Audio Recording Solution

TABLE I. Data Transfer Rates

	Transfer Rates		Total Time	
	Page	Block	Page	Block
Read	1.02 Mbits/s (127.5 kbytes/s)	2.61 Mbits/s (325.8 kbytes/s)	251 μs	12.6 ms
Write	406.3 kbits/s (50.8 kbytes/s)	536.4 kbits/s (67.1 kbytes/s)	630 μs	61.1 ms
Erase	—	—	—	6 ms

Device Operation

The basic functions required for storing messages or images on the NM29A040 are Page Read, Page Write, and Block Erase. These functions can be implemented by combining the different instructions for the NM29A040 in the following sequences.

PAGE READ

Page Read will read out the 32 bytes of a page for the specified address. To continue reading the page at the next address, an Increment command (90H) can be issued. In this way the system can avoid repeatedly using the three byte Set-Address command. The Increment command is then followed by the Read command and proceeds in the same manner as shown in *Figure 2*.

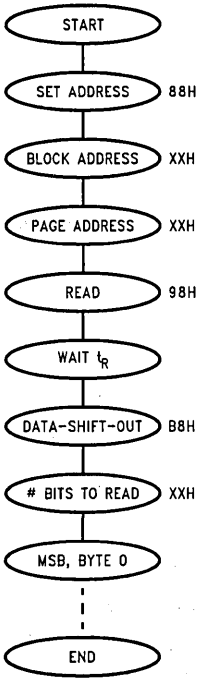

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FIGURE 2. Page Read Sequence

PAGE WRITE

Page Write sequence will write up to 32 bytes into a specified page. Like the Page Read sequence, the Increment command can be used to quickly set the address to the next page for writing data sequentially into a block.

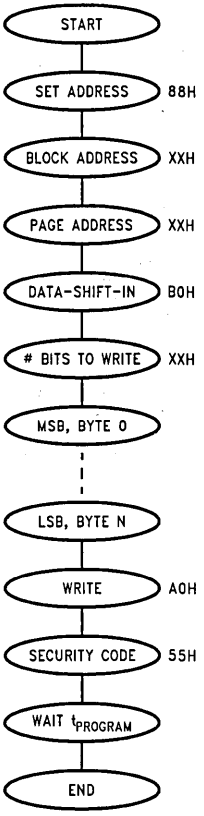

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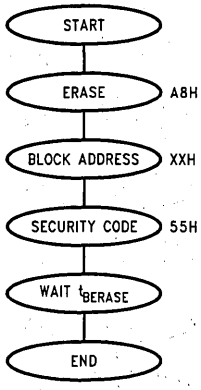
FIGURE 3. Page Write Sequence

Device Operation (Continued)

BLOCK ERASE

The Block Erase sequence erases a specified block (4 kB) of data. Flash memory devices require that a block be in an erased state prior to writing to a memory cell. In this manner, a block must be erased prior to the recording of any messages or storage of any images.



TL/D/12475–7

FIGURE 4. Block Erase Sequence

Functional Description

ORGANIZATION

The NM29A040 is a 4-Mbit device organized as 128 blocks of 128 pages. A block is the smallest unit that can be erased and is 4 kbytes in size. Within a block are 16 master pages, each 256 bytes long. A master page is further segmented into 8 pages with each page being 32 bytes long. Read and write operations always operate on a page at a time.

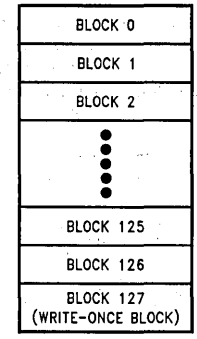


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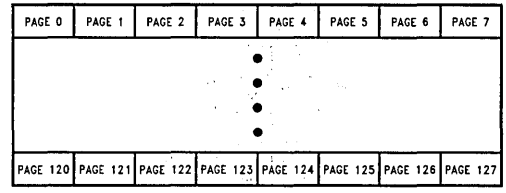
FIGURE 5. Array Organization



TL/D/12475–9

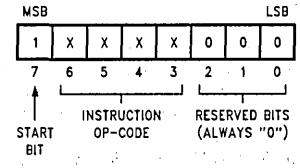
FIGURE 6. Block Organization

WRITE ONCE BLOCK

The NM29A040 contains 127 blocks (blocks 0 thru block 126) which are fully accessible to the user for reading, writing and erasing. The final block, number 127, has been set aslde as a write once block. The pages in this block may only be written to once. Once the data is written, it may not be erased. In this manner, block 127 may be used for storing system configuration information that cannot be lost.

Instruction Set

The NM29A040 has 12 instructions which are described in Table II. All instructions are one byte long and specified in the following manner:



TL/D/12475–10

FIGURE 7. Command Byte

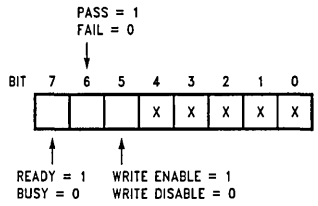
The MSB is always a "1" and is considered the start bit. The next 4 bits are the instruction opcode. These instruction opcodes are listed in Table II. The final 3 bits are reserved and must always be "0". Data input of a command other than those listed in Table II is prohibited. Data may be corrupted if unspecified commands are used.

TABLE II. Instruction Set

Instruction	Start Bit	Opcode	Reserved	Hex Command
Get-Status	1	0000	000	80H
Set-Address	1	0001	000	88H
Increment	1	0010	000	90H
Read	1	0011	000	98H
Write	1	0100	000	A0H
Erase	1	0101	000	A8H
Data-Shift-In	1	0110	000	B0H
Data-Shift-Out	1	0111	000	B8H
Write Enable	1	1100	000	E0H
Write Disable	1	1101	000	E8H
Write Last Block	1	1110	000	F0H
Read Last Block	1	1010	000	D0H

GET-STATUS

The Get-Status command allows the user to determine the status of the NM29A040. It may be issued whether the device is busy or not. The output is a status byte which indicates the internal state of the Serial Flash. The output byte is defined as:

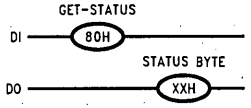


TL/D/12475–11

FIGURE 8. Get-Status Byte

Bit 7 of the status byte tells whether the device is busy performing an operation (write, erase, etc.) or is ready for a new command. Bit 6 tells if an operation just completed was performed successfully. Bit 5 tells if the device is in a write enabled or disabled mode. The remaining bits are reserved for future use and may appear as any value ("1" or "0").

Bit 7 of the status byte tells whether the device is busy performing an operation (write, erase, etc.) or is ready for a new command. Bit 6 tells if an operation just completed was performed successfully. Bit 5 tells if the device is in a write enabled or disabled mode. The remaining bits are reserved for future use and may appear as any value ("1" or "0").



TL/D/12475–12

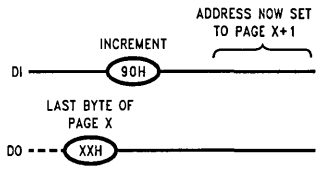
FIGURE 9. Get-Status Sequence

SET-ADDRESS

The Set-Address command defines which page and block of the memory is affected by an operation. The Set-Address command is followed by two bytes, the first indicating the block number and the second indicating the page number. The block number chooses one of the 127 blocks while the page number chooses one of the 128 pages within the given block. The Set-Address command is usually followed by a Read, Write, or Data-Shift-In command. Between the page address byte and the next command there is a delay of t_{SADD}. The address that is selected remains the active address until a new Set-Address or Increment command is given.

INCREMENT

The Increment command automatically increments the selected page address. When the Increment command is given after the last page in a block has been read, the address will roll over to the first page in the following block. When the last page in Block 126 is read out followed by an Increment command, the new address is indeterminate.



TL/D/12475–13

FIGURE 10. Increment Sequence

READ

The Read command transfers data from the selected page of the memory array into the on-chip buffer. To read the data out through DO, the Read command is followed by the two byte Data-Shift-Out command. There is a delay of t_R between the Read command and the Data-Shift-Out command as the data is transferred from the array to the on-chip buffer. During t_R the status byte will indicate that the part is busy.

WRITE

The Write command programs data from the on-chip buffer into a page in the memory array for the currently selected address. A security code 55H follows the Write command to ensure against accidental Writes. Get-Status may be used to ensure that the operation was successful. The Write command will be ignored if Write-Enable has not been set.

Instruction Set (Continued)

ERASE

The Erase command erases a single block. The Erase command is followed by a single byte telling which block to erase. In this manner, no Set-Address sequence is required to erase a block. Following the block address byte is a single byte security code, 55H, that is used to prevent inadvertent erasure. Get-Status may be used to check if the operation was completed successfully.

DATA-SHIFT-IN

The Data-Shift-In command is used to send data into the on-chip buffer. The number of bits sent into the buffer is determined by an 8-bit argument following the command. The argument is always 1 less than the actual number of bits to shift in. For example, to shift in all 32 bytes (256 bits), the argument would be FFH (255). To shift in just the first 4 bytes (32 bits), the argument would be 1FH (31). Following the argument, the data is shifted in through DI. Data-Shift-In may come before or after the Set-Address sequence when performing a page write operation.

DATA-SHIFT-OUT

The Data-Shift-Out command is used to shift data out of the on-chip buffer through DO. The number of bits sent out is determined by an 8-bit argument following the command. The argument is always 1 less than the actual number of bits to shift out. For example, to shift out all 32 bytes (256 bits), the argument would be FFH (255). To shift out the first 2 bytes (16 bits), the argument would be 0FH (15). Following the argument, the data is shifted out through DO.

WRITE ENABLE

The Write Enable command is used as a security check against inadvertant writes or erases to the device. When this command is issued, any subsequent Write or Erase commands proceed in the normal fashion. If the Write Enable command is not given or the device is in the Write Disable mode then a write to any page or erase to any block will not be allowed. Use the Get-Status command to determine whether the device currently is in the Write Enabled or Disabled mode. The NM29A040 will always power up in the Write Disable mode.

WRITE DISABLE

The Write Disable command is used to prevent inadvertant writes or erases. Once this command is executed, all subsequent Write or Erase commands will not be accepted.

READ LAST BLOCK

The Read Last Block command is used to read the contents of block 127. The Read Last Block operation procedes like a normal read operation except that the block number is ignored in the Set-Address sequence. The block address is automatically set to block 127. The Set Address command is still necessary to set the page to be read.

WRITE LAST BLOCK

The Write Last Block command writes in a page of data to the currently selected page of Block 127. A Set-Address sequence and Data-Shift-In sequence must precede the Write Last Block command. Once the information has been written into the memory array, it may not be erased.

Notifications

(1) Interruption by $\overline{CS}$ Going High

When the NM29A040 begins reading a page from-the array (t_R), writing a page to the array (t_{PROG}), or erasing a block (t_{BERASE}), the operation will complete regardless of the state of $\overline{CS}$. The $\overline{CS}$ pin may go high during these operations. If $\overline{CS}$ is held low during these operations the DO pin will reflect the state of the operation with a low state (busy) while the operation is being executed. When the operation is completed, DO will pull high to reflect the ready state.

(2) Device Reset

The NM29A040 is reset whenever $\overline{CS}$ changes from low to high. The command register will be cleared at this point. As long as the device is powered, the data register will continue to hold whatever data is in the register. To clear the data register, use the Data-Shift-In command and shift in 33 bytes of "00H". The state of $\overline{CS}$ does not affect on-going operations as described in Notification (1).

(3) Write Disable at Power-Up

On power-up, the NM29A040 is set in the write disable mode. This prevents any spurious writes to the device. To enable writes or erases, the Write Enable (E0H) command must be given.

(4) Multiple Programs to a Page

It is possible to program a page more than one time between block erases. Between block erases a bit (cell) may only be programmed once. After a block is erased, all bytes will read as "FFH". When less than 32 bytes need to be programmed into a page, the remaining bytes may be masked by writing "FFH" to those locations. In this way the cells are not changed from their erased states. Later, these bytes can be programmed with the desired data. It is suggested that the number of writes to a page between block erasses be held to as few as possible.

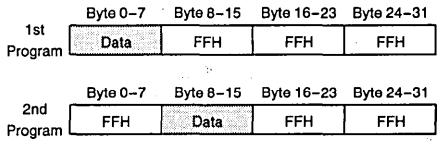


FIGURE 11. Multiple Page Program

(5) Identification of Unusable Blocks

The NM29A040 may contain unusable blocks. These unusable blocks are due to bit errors in the block. An unusable block will not affect adjacent blocks. The location of these blocks may be found pre-programmed in Block 127. Each page in Block 127 corresponds to a block in the array at a similar address. For example, Page 3 in Block 127 corresponds to Block 3. If Block 3 is a usable block, then all bytes in Page 3 of Block 127 will read out "FFH". If Block 3 is an unusable block, then some of the bytes in Page 3 of Block 127 will read out data other than "FFH". For customers using the NM29A040 with the NSAM266 speech processor, the embedded CompactSPEECH embedded software automatically locates the unusable blocks and works around these locations when performing Read, Write and Erase operations.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply (V_{CC})	−0.6V to 7.0V
Input Voltage (V_{IN})	−0.6V to 7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to V_{CC} ±0.5V (≤7V)
Power Dissipation (P_D)	300 mW
Soldering Temperature (T_{solder}, 10 sec.)	260°C
Storage Temperature (T_{stg})	−55°C to +150°C
Operating Temperature (T_{opr})	−40°C to +85°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Power Supply (V_{CC})	4.50	5.0	5.50	V

DC Operating Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0V − V_{CC}			±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V − V_{CC}			±10	μA
I_{CC01}	Operating Current Data Input/Output	t_{CYCLE} = 500 ns		5	20	mA
I_{CC02}	Programming Current			15	60	mA
I_{CC03}	Erasing Current			10	40	mA
I_{CCS1}	Standby Current	$\overline{CS}$ = V_{IH}		120	500	μA
I_{CCS2}	Standby Current	$\overline{CS}$ = V_{CC} − 0.2V		5	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.3*		0.8	V

* −2V (Pulse width ≤20 ns)

AC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		0		4	MHz
t_{SKH}	SK High Time		125			ns
t_{SKL}	SK Low Time		125			ns
t_{SKS}	SK Setup Time	Relative to $\overline{CS}$ Falling Edge	50			ns
t_{CS}	Minimum $\overline{CS}$ High Time		250			ns
t_{CSS}	$\overline{CS}$ Setup Time	Relative to SK Rising Edge	100			ns
t_{DIS}	DI Setup Time	Relative to SK Rising Edge	50			ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to SK Falling Edge	50			ns
t_{DIH}	DI Hold Time	Relative to SK Rising Edge	20			ns
t_{DF}	$\overline{CS}$ to DO in TRI-STATE®	AC Test			100	ns
t_{DH}	DO Hold Time	Relative to SK Falling Edge	0			ns
t_{PD}	Output Delay	Relative to SK Falling Edge			100	ns
t_{SADD}	Set Address Time	AC Test			150	μs
t_{PROG}	Page Program Time			400	5000	μs
t_{BERASE}	Block Erase Time			6	100	ms
t_R	Page Read Transfer Time			9	25	μs

Number of Valid Blocks

The NM29A040 may contain unusable blocks. These unusable blocks should not be used to store data. Notification (5) describes how to identify unusable blocks.

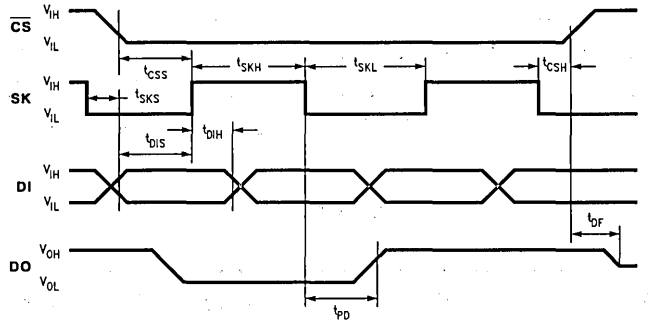
Symbol	Parameter	Min	Typ	Max	Units
N_{VB}	Number of Valid Blocks(1)	117	TBD	127(2)	Block

Note 1: A valid block is a block having all 4096 bytes usable. An unusable block is a block in which one bit is unusable.

Note 2: Not including Block 127.

Timing Diagrams

Synchronous Data Timing



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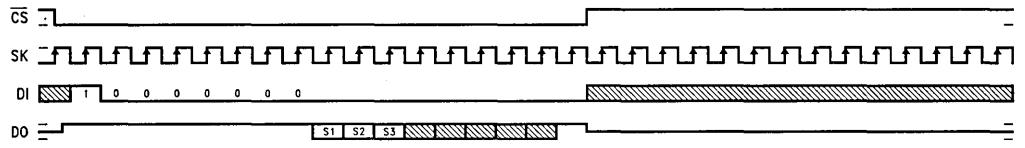
Get Status Timing



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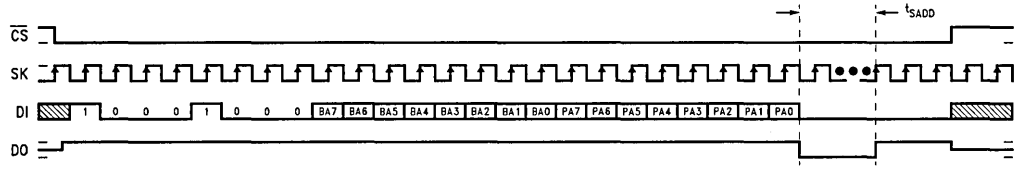
Note: To avoid putting the device in an unknown state, DI should be held low when not clocking in data/commands.

Set Address Timing



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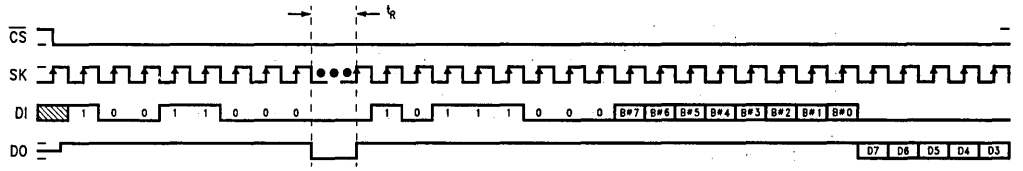
Note: $\overline{CS}$ may pull high during t_{SADD}, t_R, t_{PROG}, and t_{BERASE}. However, DO will only reflect the status (ready/busy) while $\overline{CS}$ is low.

Timing Diagrams (Continued)

Read Timing



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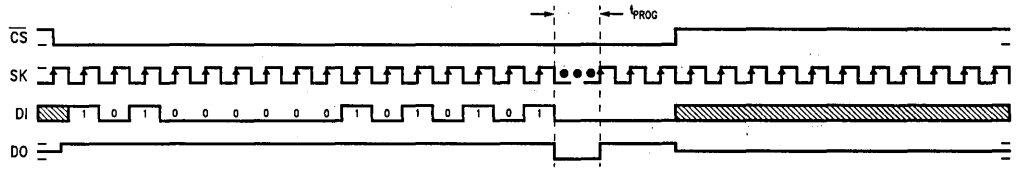
Write Timing



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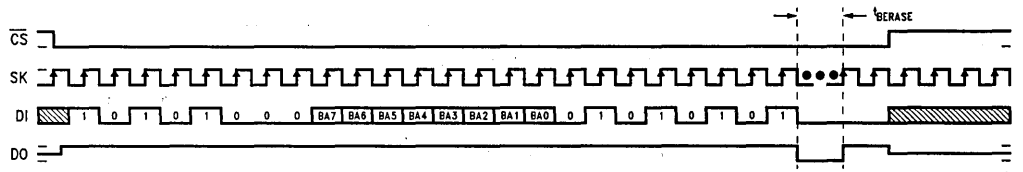
Erase Timing



TL/D/12475–21

National Semiconductor

PRELIMINARY

NM28C64/C64L/C64A
64k (8k x 8) Parallel Extended Voltage Range CMOS EEPROM

General Description

The NM28C64/C64L/C64A are fast, single-power supply CMOS EEPROM organized as 8k by 8 bits. Both READ and WRITE modes function over the full V_{CC} range of 2.7V–5.5V.

In-system programming of the part requires only a simple interface. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power-up/down protection eliminate the need for extemal timing and protection hardware.

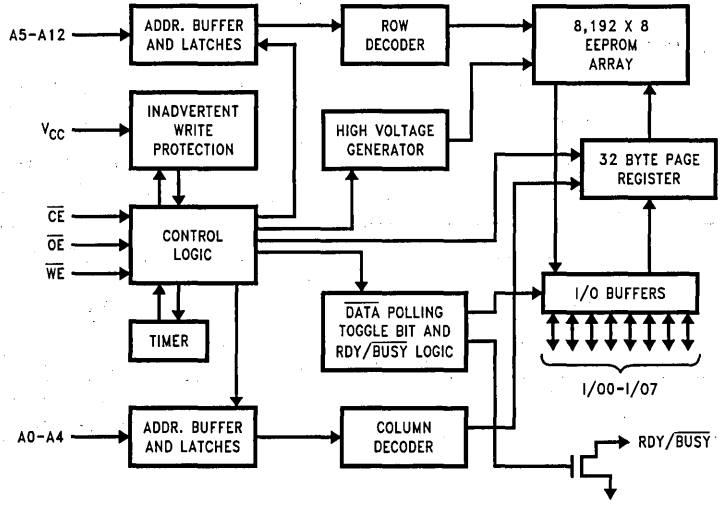
$\overline{DATA}$ and Toggle-Bit Polling and a RDY/$\overline{BUSY}$ pin provide a convenient means for determining the beginning and end of the internal self-timed WRITE cycle.

Both internal hardware and software WRITE protection are provided. Page organization permits the loading of from one to 32 bytes into a data register, the entire page is programmed at one time in 10 ms.

Features

- Voltage Supply
  - — Full Read and Write operation
  - — C64: 4.5V to 5.5V
  - — C64L: 2.7V to 3.6V
  - — C64A: 2.7V to 5.5V
- Low Power Dissipation
  - — 8 mA Active Current
  - — 50 μA CMOS Standby Current
- Read Access Time
  - — 200 ns at 2.7V
  - — 120 ns at 4.5V
- 32 Byte Page Write
- End of Write Detection
  - — $\overline{DATA}$ Polling on I/O_7
  - — Toggle Bit Polling on I/O_6
  - — READY/$\overline{BUSY}$ Open Drain Output
- Hardware Data Protection
- High Reliability CMOS Technology
  - — Endurance 100,000 Cycles
  - — Data Retention: 10 years
- Low Voltage CMOS and TTL Compatible Inputs and Outputs
- JEDEC Standard Byte-Wide Pinout
- Commercial and Industrial Temperature Ranges

Block Diagram



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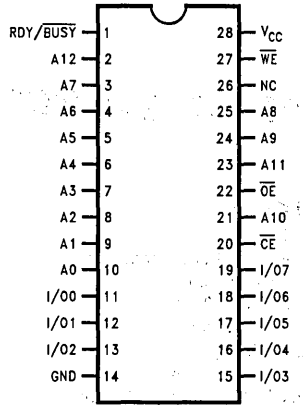
Pin Configurations

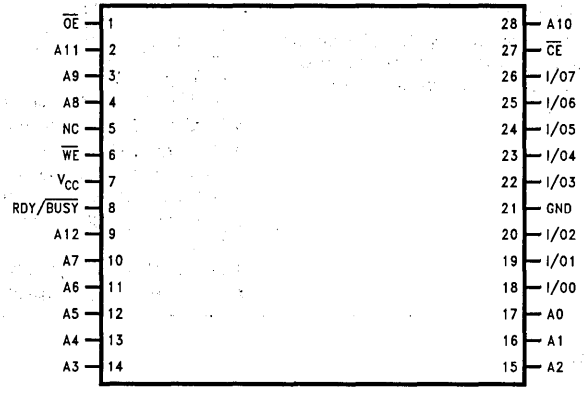
DIP (N)



TL/D/12398-2

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0–I/O_7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/Busy Output
NC	No Connect

TSOP (T) Package Type I



TL/D/12398-3

Top View

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number	4.5V–5.5V
NM28C64N28 NM28C64T28	

Order Number	2.7V–3.6V
NM28C64LN28 NM28C64LT28	

Order Number	2.7V–5.5V
NM28C64AN28 NM28C64AT28	

Extended Temperature Range (−40°C to +85°C)

Order Number	4.5V–5.5V
NM28C64EN28 NM28C64ET28	

Order Number	2.7V–3.6V
NM28C64LEN28 NM28C64LET28	

Order Number	2.7V–5.5V
NM28C64AEN28 NM28C64AET28	

Functional Description

DEVICE OPERATION

Read Mode

Data are transferred from the addressed memory location to the external data bus when $\overline{WE}$ is held HIGH, $\overline{OE}$ is held LOW, and $\overline{CE}$ is held LOW. The 2-line control architecture of the $\overline{OE}$ and $\overline{CE}$ pins eliminates bus contention in a system environment. When either the $\overline{OE}$ or $\overline{CE}$ lines are set HIGH, the NM28C64A releases the data bus.

Write Mode

A write cycle is initiated when both the $\overline{WE}$ and $\overline{CE}$ lines are LOW and $\overline{OE}$ is HIGH. The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs last. The data are latched on the rising edge of either the $\overline{WE}$ or $\overline{CE}$, whichever occurs first. It takes approximately 10 ms for the write cycle to erase the addressed memory locations and store the new data.

Page Write

From one to thirty-two bytes can be written to the selected page address (A5–A12) during any write operation. The page address is latched once the data-load cycle is started. The data latch loading may be interrupted in order to fetch data from another system location. However, data loading must continue again within the byte load cycle time (t_{BLC}), otherwise the internal programming cycle will begin. When returning to loading data into the latches, the page address is ignored because of the latched-page register.

There are no page write window limitations; the page write window can continue indefinitely as long as the $t_{BLC\ MAX}$ time is not exceeded.

The program cycle first erases data located in the addressed cells, then writes the new data into these addressed cells. A page write does not rewrite the entire page, only those locations selected during data-latch loading.

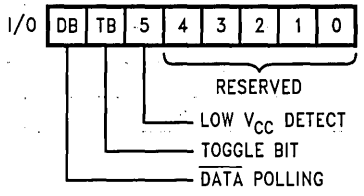
Write Abort

During a data load cycle in preparation for programming, $\overline{OE}$ must be held at V_{IH}. If $\overline{OE}$ is held LOW during the rising edge of $\overline{CE}$ ($\overline{CE}$ controlled WRITE), or $\overline{WE}$ ($\overline{WE}$-controlled WRITE), the WRITE operation is aborted and the data latches are reset.

RDY/$\overline{BUSY}$

The RDY/$\overline{BUSY}$ pin is an open drain output that monitor the status of a write cycle. The open drain connection allows for OR-tying several devices to the same RDY/$\overline{BUSY}$ pin. This output is actively pulled LOW during the write cycle and released at the end of the cycle.

Additional methods for monitoring status and internal programming cycles are provided.



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Toggle Bit (I/O_6)

The toggle bit (I/O_6) toggles between ZERO and ONE on alternate READS while the NM28C64A performs an internal write cycle. After the write cycle is completed, I/O_6 stops toggling.

$\overline{DATA}$ Polling (I/O_7)

A third method for determining the end an internal programming cycle is $\overline{DATA}$ polling. This method allows the host to perform a simple bit test to determine whether the device is in an internal write cycle without the need for system interrupts or external hardware.

After the initiation of the internal programming cycle, bit 7 of the last byte written is complemented and sent to I/O_7. The host can read I/O_7 to determine whether or not the device is in an internal write cycle. Upon completion of the write cycle, I/O_7 provides the true value.

Low V_{CC} Detect (I/O_5)

Once an internal write cycle is initiated, it continues to completion even if the supply voltage falls below 2.0V (typical) during the cycle. In the event that V_{CC} does fall below 2.0V during the programming cycle, an internal latch is set. Its status can be polled by reading the state of I/O_5.

A high level on I/O_5 indicates that a sub-2.0V level was detected and programmed-data integrity may be suspect.

Hardware Data Protection

The device is protected from inadvertent memory writes by the following three hardware methods:

1. V_{CC} Sense: The write function is inhibited if V_{CC} falls below 2.0V (typical), prior to the beginning of an internal write cycle.
2. Noise Protection: A write cycle will not be initiated if the $\overline{WE}$ or $\overline{CE}$ LOW pulse is < 20 ns wide (typical).
3. Write Inhibit: Write cycles can be inhibited during power-on and power-off by holding any one or more of the following pins to the indicated levels.
   (a) $\overline{OE}$ LOW
   (b) $\overline{CE}$ HIGH
   (c) $\overline{WE}$ HIGH

Chip Erase

The entire memory can be erased (set to logic ONE) by a single operation. To activate Chip Erase, $\overline{OE}$ must be raised to 12V ±0.5V and all I/O pins set HIGH while $\overline{CE}$ and $\overline{WE}$ are simultaneously brought LOW. The erase operation occurs within 10 ms.

Device Identification

The user has an extra 32 bytes (one page) of memory available for device identification. This extra memory can be read or written to just like the regular memory array but only by setting address pin A9 to 12V ±0.5V and selecting addresses 1FE0h–1FFFh.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input Voltage (including NC pins) with Respect to Ground	−0.6V to V_{CC} + 0.6V
Lead Temperature (Soldering, 10 seconds)	+300°C
All Output Voltages with Respect to Ground	−0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	−0.6V to +13.5V
ESD Rating	2000V

Note: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC and AC Operating Range

		NM28C64	NM28C64L	NM28C64A
Operating Temperature (Case)	**Comm.**	0°C–70°C	0°C–70°C	0°C–70°C
	Indust.	−40°C–85°C	−40°C–85°C	−40°C–85°C
V_{CC} Power Supply		4.5V–5.5V	2.7V–3.6V	2.7V–5.5V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Power	A9
Standby	V_{IH}	X	X	High Z	Standby	
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active	
Write ($\overline{WE}$ Controlled)	V_{IL}	V_{IH}	⊓	D_{IN}	Active	
Write ($\overline{CE}$ Controlled)	⊓	V_{IH}	V_{IL}	D_{IN}	Active	
Read and Write Inhibit	V_{IL}	V_{IH}	V_{IH}	High Z	Active	
Output Disable	X	V_{IH}	X	High Z		
Chip Erase*	V_{IL}	12V ±0.5V	⊓	$D_{IN} = V_{IH}$	Active	
Chip ID Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active	12V ±0.5V
Chip ID Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active	12V ±0.5V

*$\overline{OE}$ must be raised to 12V prior to establishing the condition $\overline{CE} = \overline{WE} = V_{IL}$ to initiate a chip-erase cycle.

DC Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		5	μA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	μA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}$		50	μA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; $\overline{CE} = V_{IL}$		8.0	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = −100 μA	2.0		V

Capacitance ($f = 1.0$ MHz, $T_A = 25°C$)

Symbol	Conditions	Typ	Max	Units
C_{IN}	$V_{IN} = 0V$	4	6	pF
C_{VO}	$V_{I/O} = 0V$	8	12	pF

AC Read Characteristics—NM28C64

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	4.5V–5.5V			120	ns
t_{CE}	$\overline{CE}$ to Output Delay	4.5V–5.5V			120	ns
t_{OE}	$\overline{OE}$ to Output Delay	4.5V–5.5V	0		50	ns
t_{OH}	Output Hold from Address Change	4.5V–5.5V	0			ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	4.5V–5.5V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	4.5V–5.5V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	4.5V–5.5V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	4.5V–5.5V			50	ns

AC Read Characteristics—NM28C64L

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	2.7V–3.6V			200	ns
t_{CE}	$\overline{CE}$ to Output Delay	2.7V–3.6V			200	ns
t_{OE}	$\overline{OE}$ to Output Delay	2.7V–3.6V	0		80	ns
t_{OH}	Output Hold from Address Change	2.7V–3.6V	0			ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	2.7V–3.6V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	2.7V–3.6V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	2.7V–3.6V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	2.7V–3.6V			50	ns

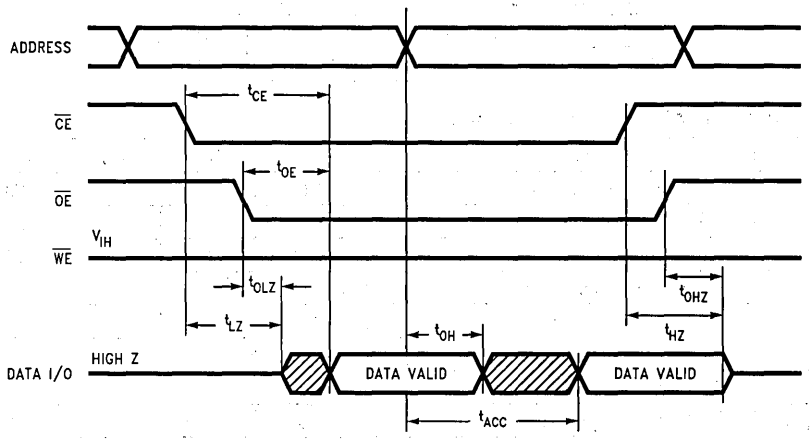
AC Read Characteristics—NM28C64A

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units
t_{ACC}	Address to Output Delay	2.7V–4.4V			200	ns
		4.5V–5.5V			120	ns
t_{CE}	$\overline{CE}$ to Output Delay	2.7V–4.4V			200	ns
		4.5V–5.5V			120	ns
t_{OE}	$\overline{OE}$ to Output Delay	2.7V–4.4V			80	ns
		4.5V–5.5V	0		50	ns
t_{OH}	Output Hold from Address Change	2.7V–4.4V				ns
		4.5V–5.5V				ns
t_{LZ} (Note 1)	$\overline{CE}$ Low to Output Active	2.7V–4.4V	0			ns
		4.5V–5.5V	0			ns
t_{OLZ} (Note 1)	$\overline{OE}$ Low to Output Active	2.7V–4.4V	0			ns
		4.5V–5.5V	0			ns
t_{HZ} (Notes 1, 2)	$\overline{CE}$ High to Output Float	2.7V–4.4V			50	ns
		4.5V–5.5V			50	ns
t_{OHZ} (Notes 1, 2)	$\overline{OE}$ High to Output Float	2.7V–4.4V			50	ns
		4.5V–5.5V			50	ns

Note 1: This parameter is characterized and is not 100% tested.

Note 2: Output floating (High Z) is defined as the state when the external data line is no longer driven by the output buffer.

AC Read Waveforms



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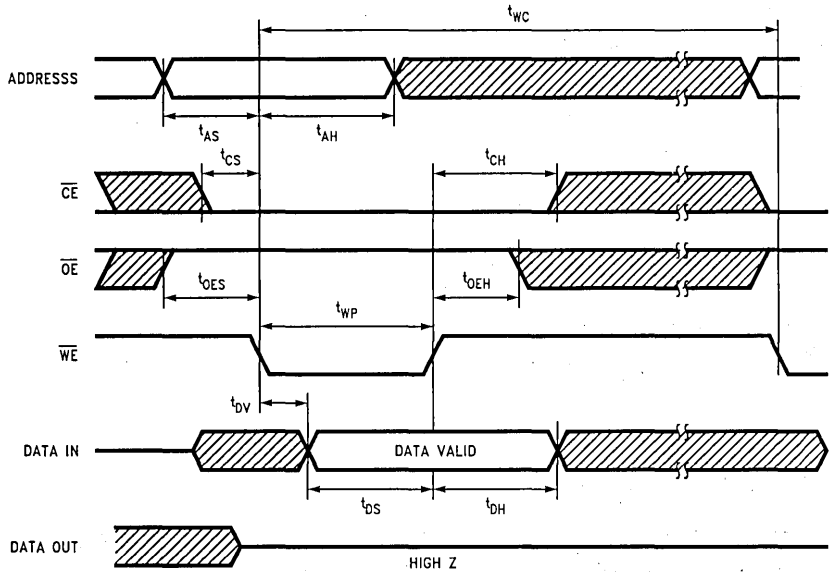
AC Write Characteristics

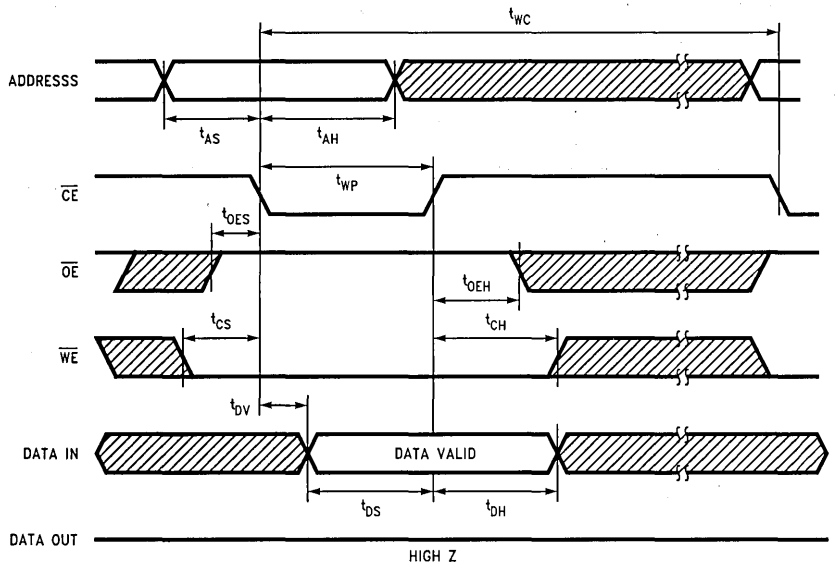
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{WC}	Write Cycle Time				10	ms
t_{AH}	Address Hold Time		100			ns
t_{AS}	Address Setup		10			ns
t_{CH}	Write Hold Time		0			ns
t_{CS}	Write Setup Time		0			ns
t_{DH}	Data Hold		10			ns
t_{DS}	Data Setup Time		100			ns
t_{OEH}	$\overline{OE}$ High Hold Time		10			ns
t_{OES}	$\overline{OE}$ High Setup Time		10			ns
t_{RB}	$\overline{WE}$ Low to RSY/$\overline{BUSY}$ Low				120	ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		150			ns
t_{BLC}	Byte Load Cycle Time		1		100	μs
t_{INIT}	Write Inhibit Period after Power Up		5		15	ms

AC Write Waveforms—$\overline{WE}$ Controlled



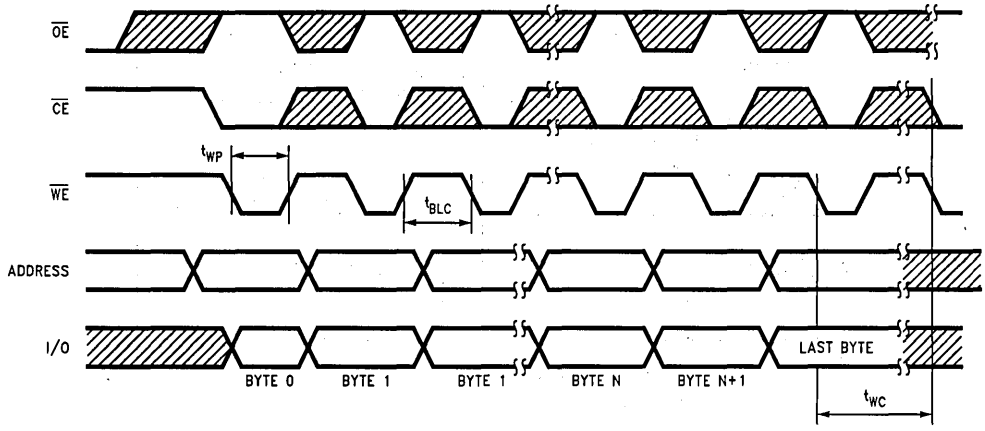
TL/D/12398–7

AC Write Waveforms—$\overline{CE}$ Controlled



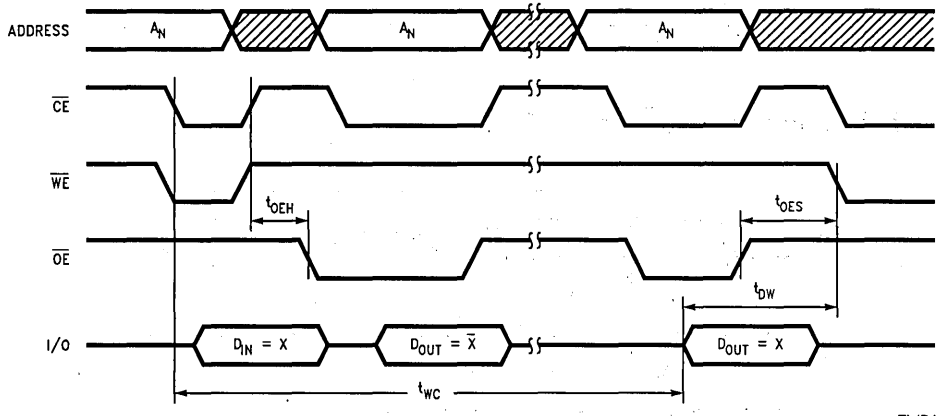
TL/D/12398–8

Page Write Cycle



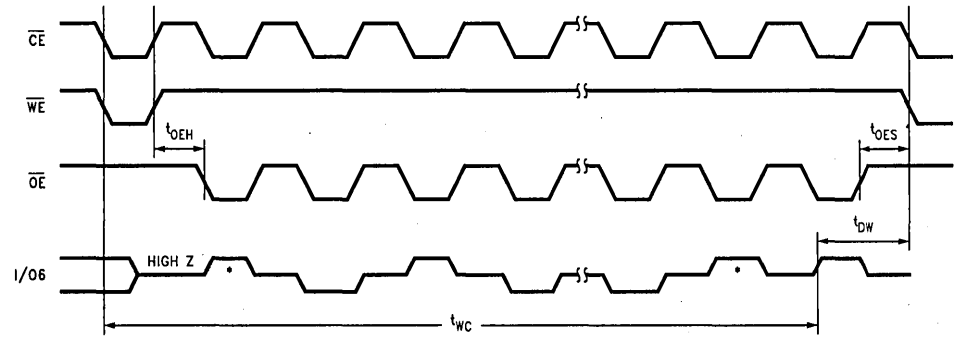
TL/D/12398–9

Data Polling Waveforms (Note 1)



TL/D/12398–10

Toggle Bit Timing Diagram (Note 1)



*STARTING AND ENDING STATE OF I06 WILL VARY, DEPENDING UPON ACTUAL t_{WC}.

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Note 1: Polling operations are by definition read cycles and are therefore subject to read cycle timings

National Semiconductor

NM24C02L/C04L/C08L/C16L
2K-/4K-/8K-/16K-Bit Serial EEPROM (I²C Synchronous 2-Wire Bus)

General Description

The NM24C02L/C04L/C08L/C16L devices are 2048/4096/8192/16,384 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements.

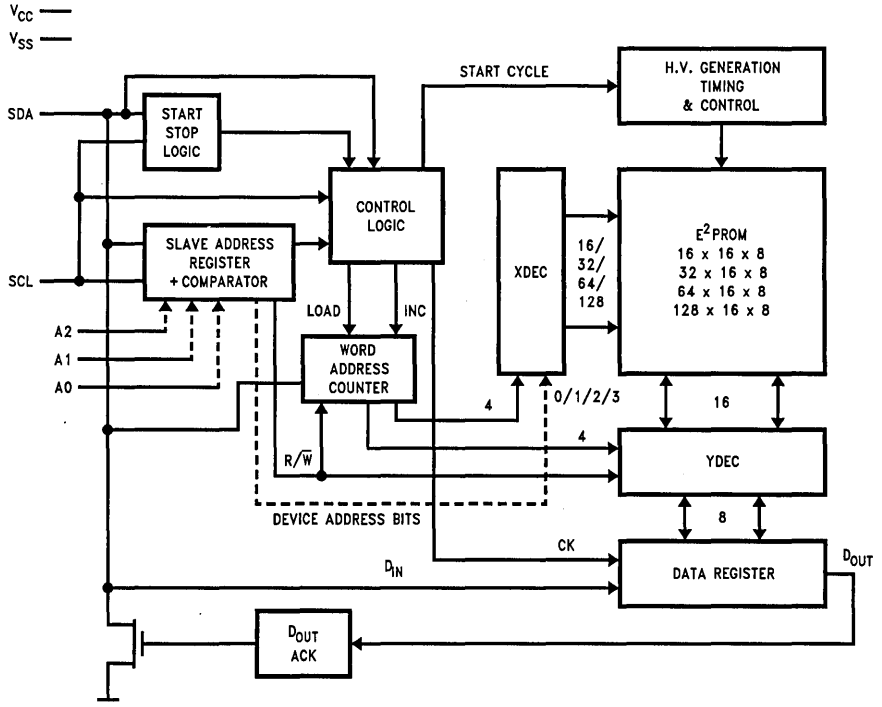
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended Operating Voltage: 2.5V → 5.5V
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I²C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP, 8 and 14 pin SO

Functional Diagram



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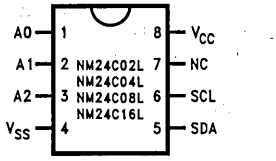
Connection Diagrams

Dual-In-Line Package (N)



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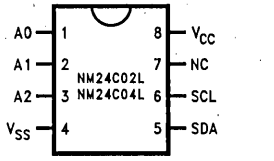
Top View

See NS Package Number N08E (N)

SO Package (M8)



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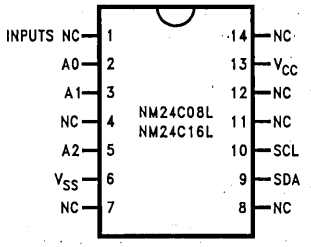
Top View

See NS Package Number M08A (M8)

SO Package (M)



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Top View

See NS Package Number M14B (M)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection (Float, GND, or V_{CC})
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02LN/NM24C04LN/NM24C08LN/NM24C16LN NM24C02LM8/NM24C04LM8/NM24C08LM/NM24C16LM

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02LEN/NM24C04LEN/NM24C08LEN/NM24C16LEN NM24C02LEM8/NM24C04LEM8/NM24C08LEM/NM24C16LEM

4

Standard Voltage ($4.5V \leq V_{CC} \leq 5.5V$) Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C02L/C04L/C08L/C16L	0°C to +70°C
NM24C02LE/C04LE/C08LE/C16LE	−40°C to +85°C
NM24C02LM/C04LM/C08LM/C16LM (Mil. Temperature)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	µA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

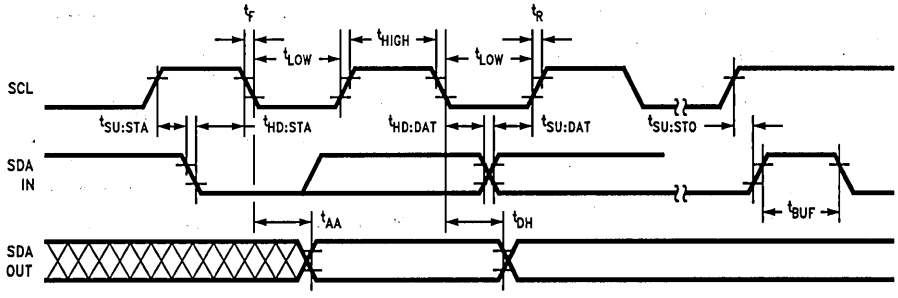
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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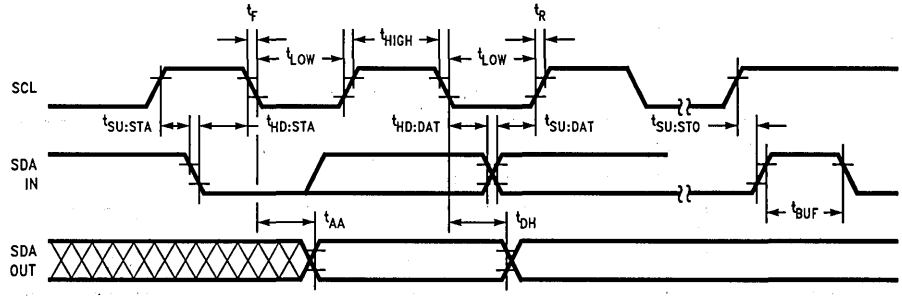
Read and Write Cycle Limits ($4.5V \leq V_{CC} \leq 5.5V$)

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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Bus Timing (Continued)

BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMS on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

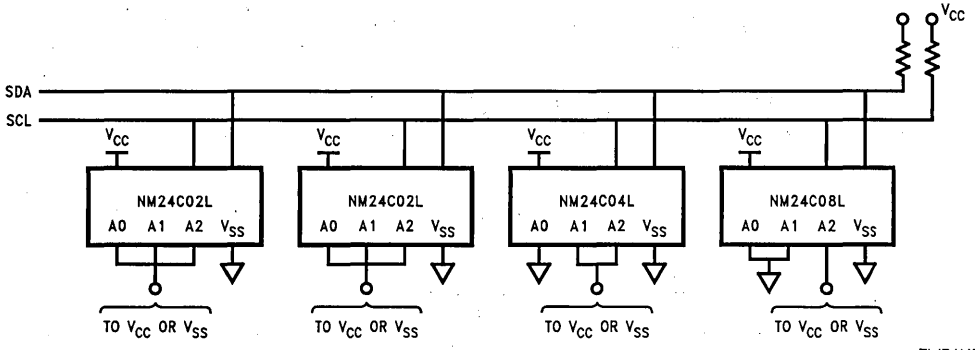
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits.
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16K (Maximum Size) of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note: It is recommended that the total line capacitance be less than 400 pF.

Note: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02L	DA	DA	DA	2048 Bits	1
NM24C04L	V_{SS}	DA	DA	4096 Bits	2
NM24C08L	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C16L	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24CxxL device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02L	ADR	ADR	ADR	$2^3 = 8$ (8) x (2K) = 16K
NM24C04L	X	ADR	ADR	$2^2 = 4$ (4) x (4K) = 16K
NM24C08L	X	X	ADR	$2^1 = 2$ (2) x (8K) = 16K
NM24C16L	X	X	X	$2^0 = 1$ (1) x (16K) = 16K

ADR: Denotes an active pin used for device addressing
X: Not used for addressing (Must be tied to Ground/V_{SS})

Device Operation

The NM24CxxL supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24CxxL will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

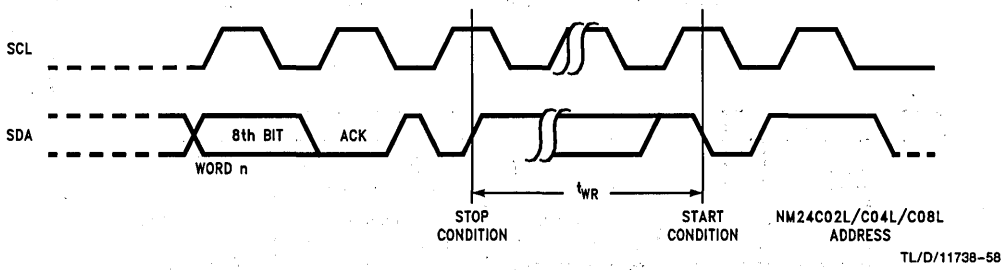
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24CxxL to place the device in the standby power mode.

Write Cycle Timing



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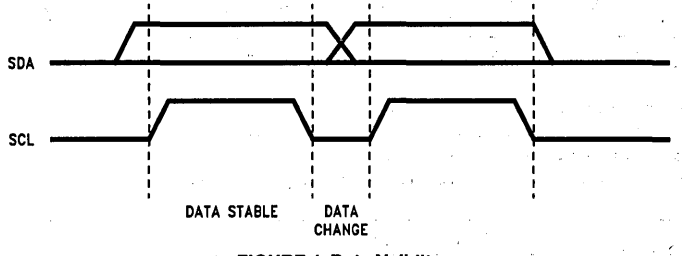

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FIGURE 1. Data Validity

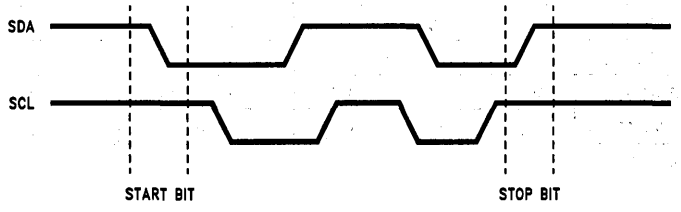

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FIGURE 2. Definition of Start and Stop

Device Operation (Continued)

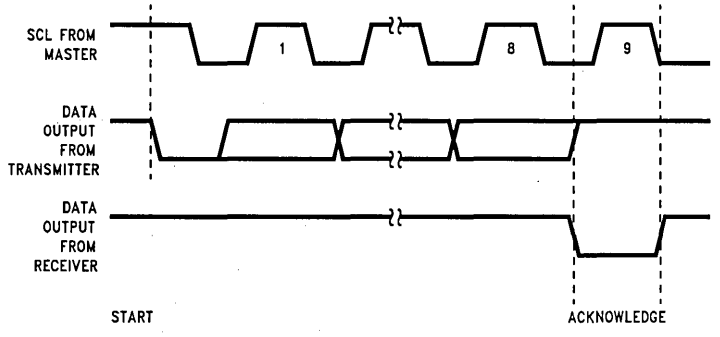

FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C02L, NM24C04L, NM24C08L and NM24C16L.

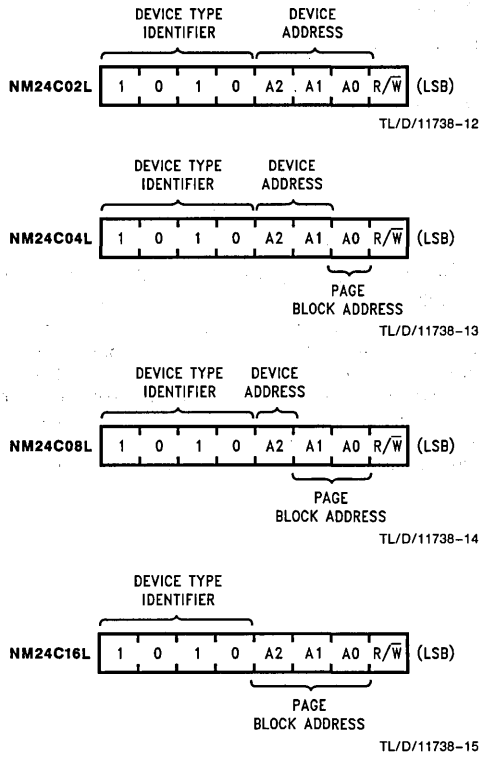

FIGURE 4. Slave Addresses

DEVICE ADDRESSING

Refer to the following table for Slave Addresss string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02L	A	A	A	1 (2K)	(NONE)
NM24C04L	P	A	A	2 (4K)	0 1
NM24C08L	P	P	A	4 (8K)	00 01 10 11
NM24C16L	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed, and a "0" initiates the write mode.

A simple review: After the NM24C02L/C04L/C08L/C16L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24CxxL responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation the NM24CxxL initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24CxxL is still busy with the write operation no ACK will be returned. If the NM24CxxL has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

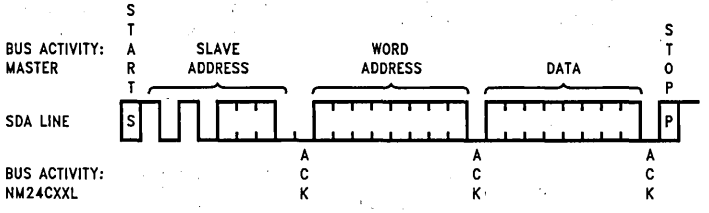

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FIGURE 5. Byte Write

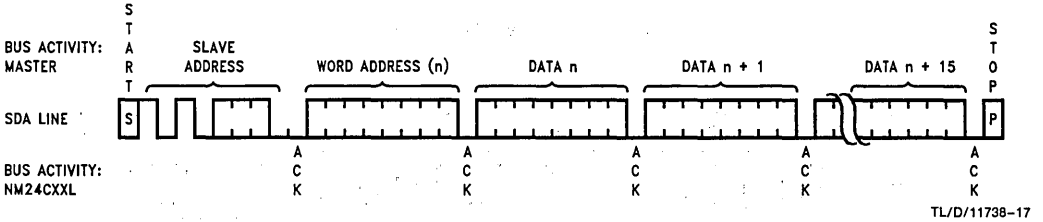

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FIGURE 6. Page Write

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24CxxL contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24CxxL issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24CxxL discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24CxxL and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24CxxL discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24CxxL continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24CxxL continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

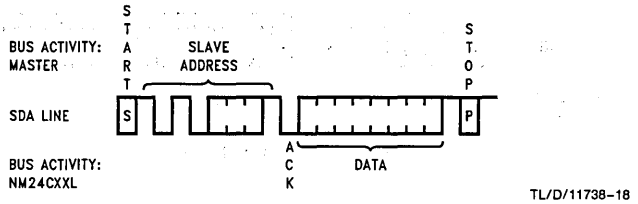

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FIGURE 7. Current Address Read

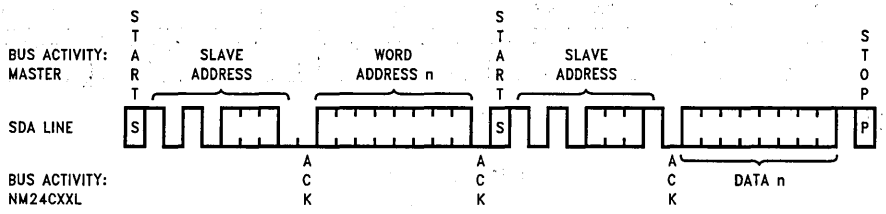

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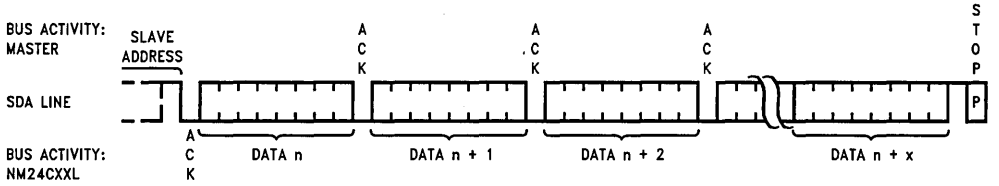
FIGURE 8. Random Read



TL/D/11738–20

FIGURE 9. Sequential Read

Read Operations (Continued)

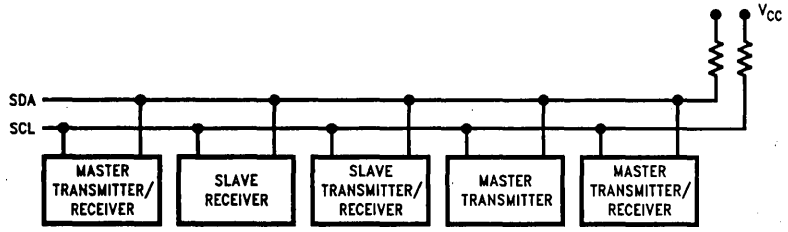


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FIGURE 10. Typical System Configuration

Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

National Semiconductor

NM93C06L/C46L/C56L/C66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V t0 5.5V) (MICROWIRE™ Bus Interface)

General Description

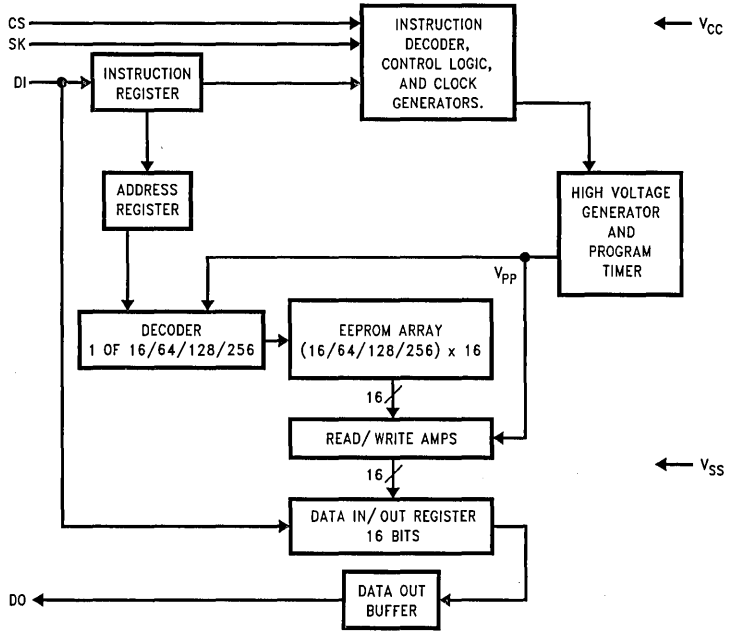
The NM93C06L/C46L/C56L/C66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CxxL Family functions in an extended voltage operating range, requires only a single power supply and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. These devices are available in an SO package for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- 2.0V to 5.5V operation in Read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; Typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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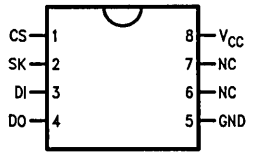
Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

NS Package Number N08E or M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C06LN/NM93C46LN
NM93C56LN/NM93C66LN
NM93C06LM8/NM93C46LM8
NM93C56LM8/NM93C66LM8

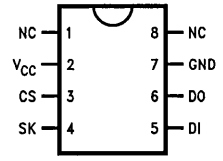
Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C06LEN/NM93C46LEN
NM93C56LEN/NM93C66LEN
NM93C06LEM8/NM93C46LEM8
NM93C56LEM8/NM93C66LEM8

Alternate (Turned) SO Pinout

Order Number
NM93C06TLM8/NM93C46TLM8/NM93C56TLM8
NM93C06TLEM8/NM93C46TLEM8/NM93C56TLEM8

Alternate SO Pinout (TM8)



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NS Package Number M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
Bulk (ERAL/WRALL) Programming	3.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250 kHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V
f_{SK}	SK Clock Frequency		(Note 5)	0	250	kHz
t_{SKH}	SK High Time			1		μs
t_{SKL}	SK Low Time			1		μs
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	0.2		μs
t_{CS}	Minimum CS Low Time		(Note 2)	1		μs
t_{CSS}	CS Setup Time			0.2		μs
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time			0.4		μs
t_{CSH}	CS Hold Time			0		μs
t_{DIH}	DI Hold Time			0.4		μs
t_{PD1}	Output Delay to "1"				2	μs
t_{PD0}	Output Delay to "0"				2	μs
t_{SV}	CS to Status Valid				1	μs
t_{DF}	CS to DO in TRI-STATE®		CS = V_{IL}		0.4	μs
t_{WP}	Write Cycle Time				15	ms

DC and AC Electrical Characteristics: 4.5V < V_{CC} < 5.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1 MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0	1	MHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup TIme		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 2)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/t_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Levels	V_{OL}/V_{OH} Timing Levels	I_{OL}/I_{OH}
2.0V ≤ V_{CC} < 4.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10 μA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C06L/C46L/C56L/C66L device have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Functional Description (Continued)

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specificed address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data distrub, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: NSC CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06L and NM93C46L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRALL	1	00	01XXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06L.

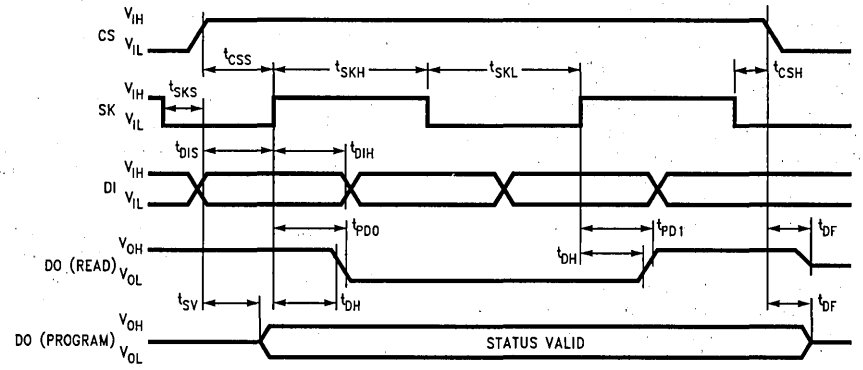
Instruction Set for the NM93C56L and NM93C66L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory at specified address.
WEN	1	00	11XXXXXX		Enable all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXXXX		Disables all programming modes.

Note: Address bit A7 is "Don't Care" for the NM93C56L.

Timing Diagrams

Synchronous Data Timing



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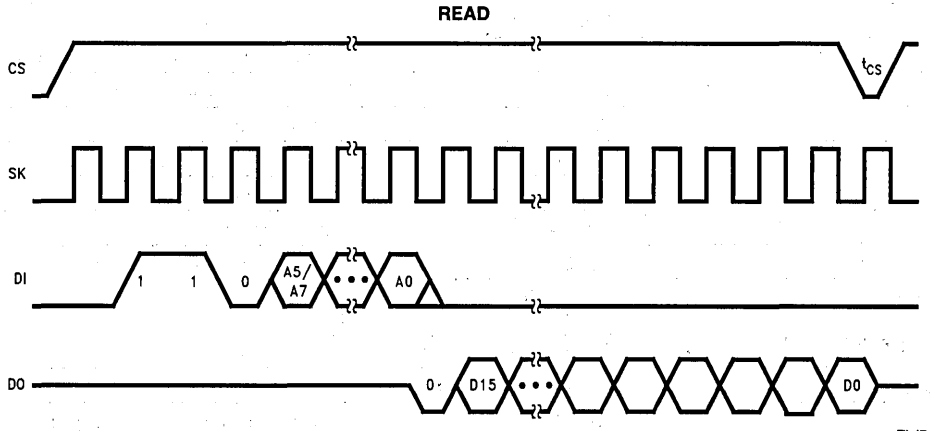
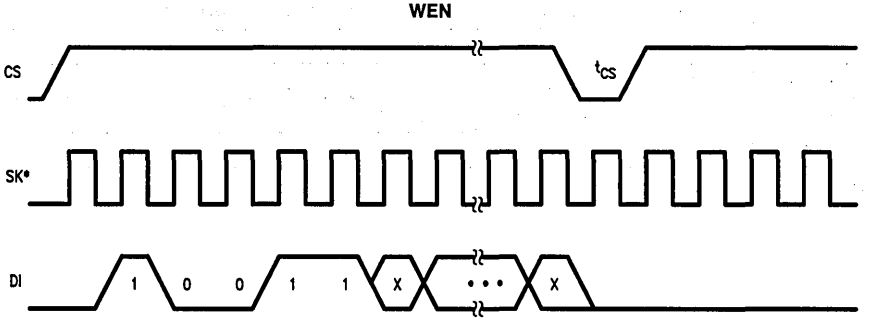
READ



TL/D/10045–5

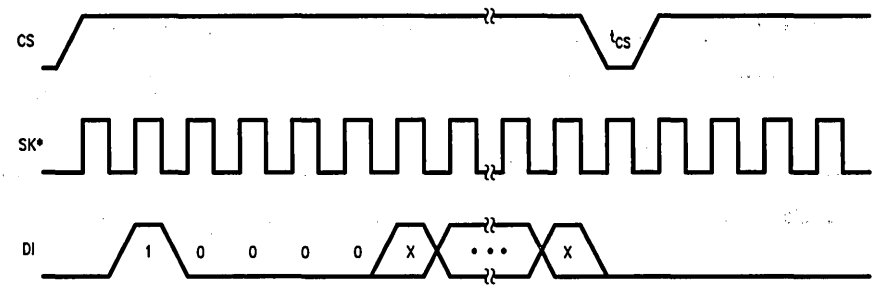
WEN



TL/D/10045–6

Timing Diagrams (Continued)

WDS



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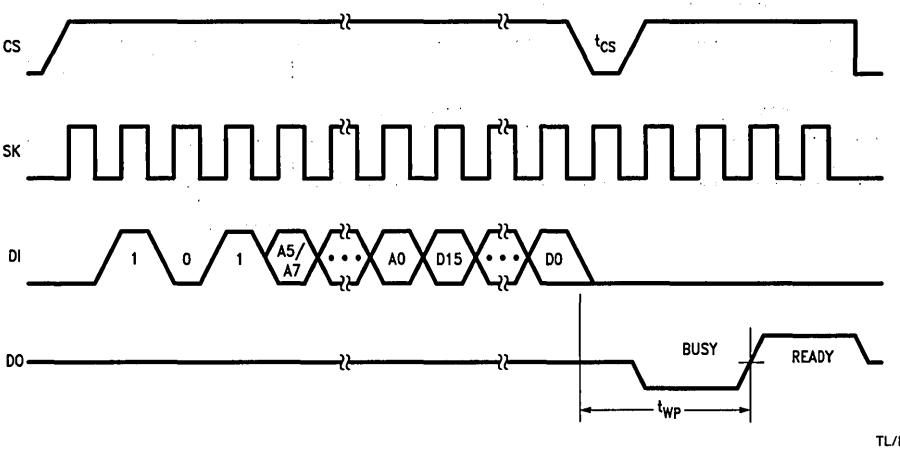
WRITE



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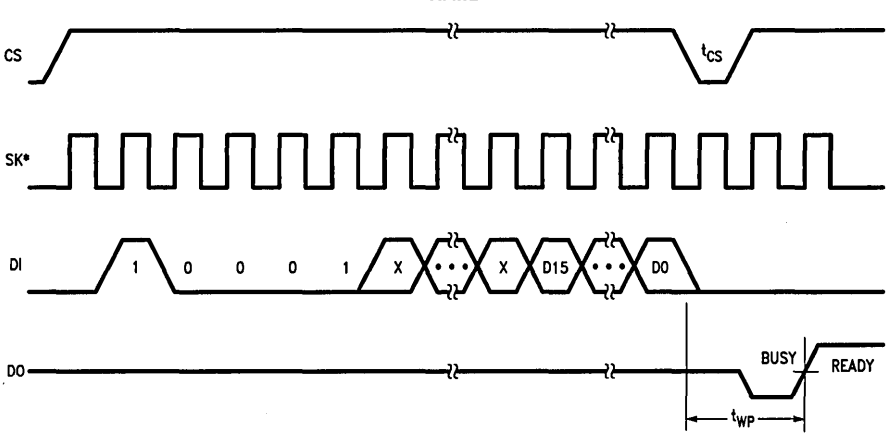
WRALL



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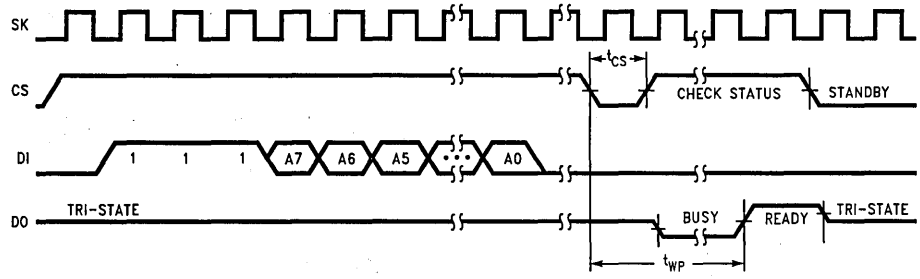
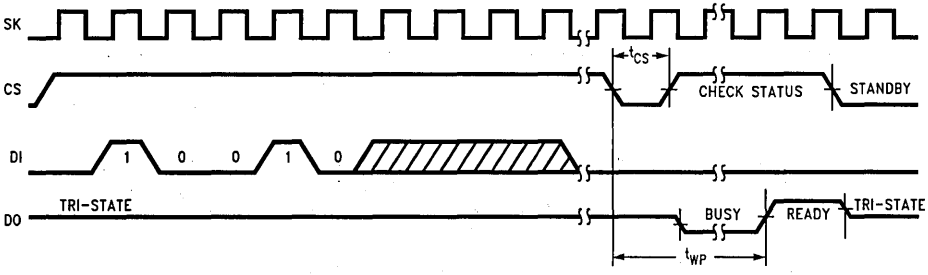
Timing Diagrams (Continued)

ERASE



TL/D/10045–10

ERAL



TL/D/10045–11

Protecting Data in Serial EEPROMs

National Semiconductor
Application Brief 15
Paul Lubeck

National offers a broad line of serial interface EEPROMs which share a common set of features:

- Low cost
- Single supply in all modes (+5V ± 10%)
- TTL compatible interface
- MICROWIRE™ compatible interface
- Read-Only mode or read-write mode

This Application Brief will address protecting data in any of National's Serial Interface EEPROMs by using read-only mode.

Whereas EEPROM is non-volatile and does not require V_{CC} to retain data, the problem exists that stored data can be destroyed during power transitions. This is due to either uncontrolled interface signals during power transitions or noise on the power supply lines. There are various hardware design considerations which can help eliminate the problem although the simplest most effective method may be the following programming method.

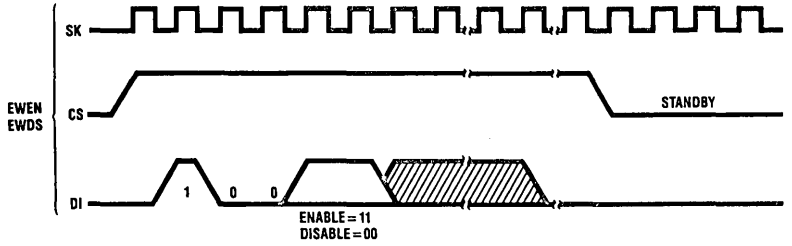
All National Serial EEPROMs, when initially powered up are in the Program Disable Mode*. In this mode, the EEPROM will abort any requested Erase or Write cycles. Prior to Erasing or Writing it is necessary to place the device in the Program Enable Mode†. Following placing the device in the Program Enable Mode, Erase and Write will remain enabled until either executing the Disable instruction or removing V_{CC}. Having V_{CC} unexpectedly removed often results in uncontrolled interface signals which could result in the EEPROM interpreting a programming instruction causing data to be destroyed.

Upon power up the EEPROM will automatically enter the Program Disable Mode. Subsequently the design should incorporate the following to achieve protection of stored data.

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.
2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return

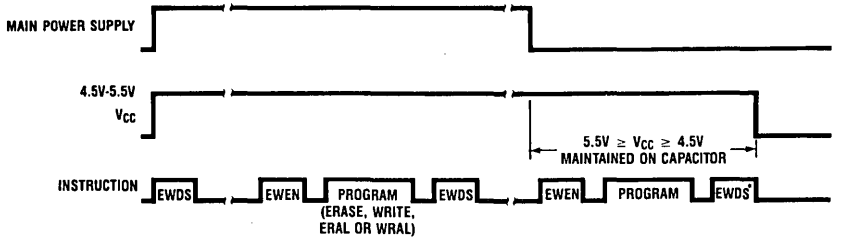
*EWDS or WDS, depending on exact device.

†EWEN or WEN, depending on exact device.



TL/D/7085–1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085–2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Designing with the NM93C06 A Versatile Simple to Use E² PROM

National Semiconductor
Application Note 338
Masood Alavi

This application note outlines various methods of interfacing an NM93C06 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NM93C06; as well as how serial data outputted from an NM93C06 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NM93C06.

The third part of the application note shows a list of various applications that can use a NM93C06.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

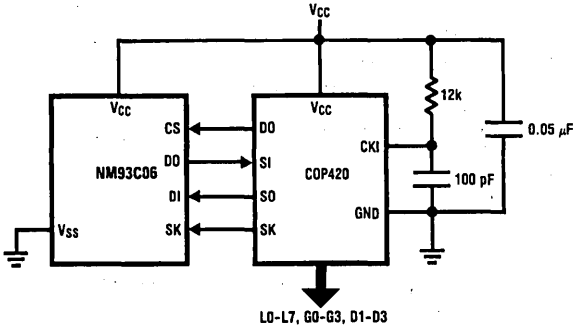
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E²P-ROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NM93C06—COP420 Interface

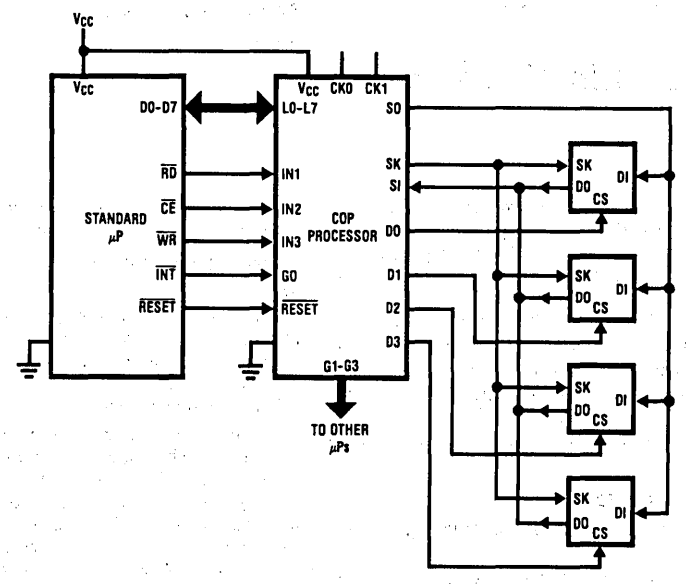
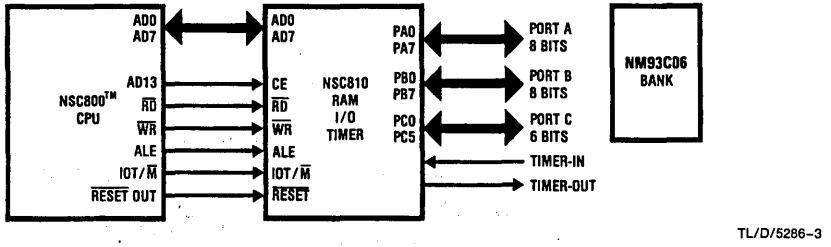


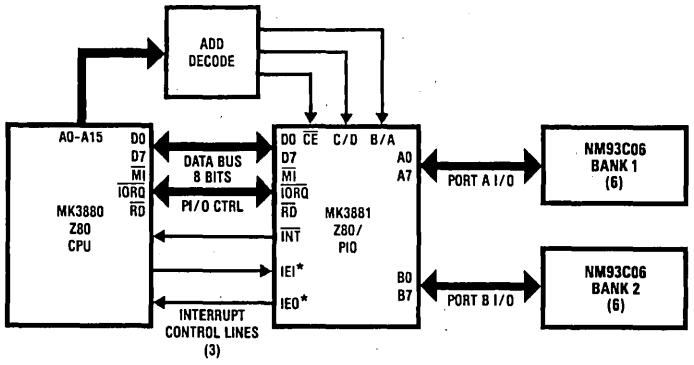
FIGURE 2. NM93CO6—Standard μP Interface Via COP Processor



PA0 → SK
PA1 → DI/DO
} Common to all 9306's
PA2–7 → 6CS for 6– 9306's

* SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.
* CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.

FIGURE 3. NSC800™ to NM93C06 Interface (also Valid for 8085/8085A and 8156)

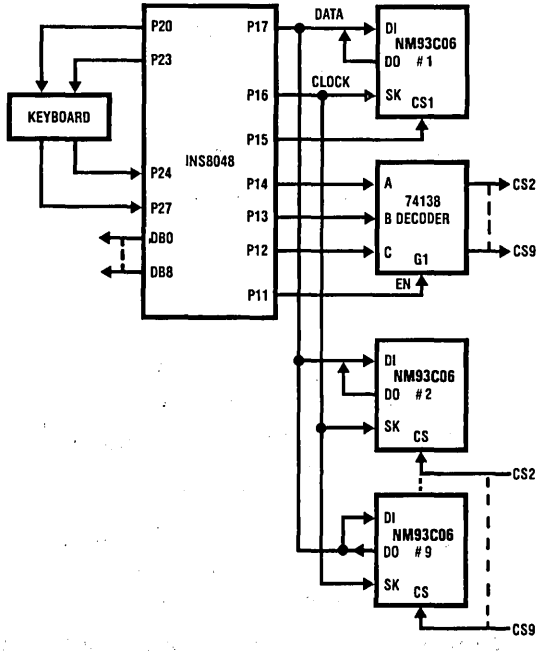


TL/D/5286–4

Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

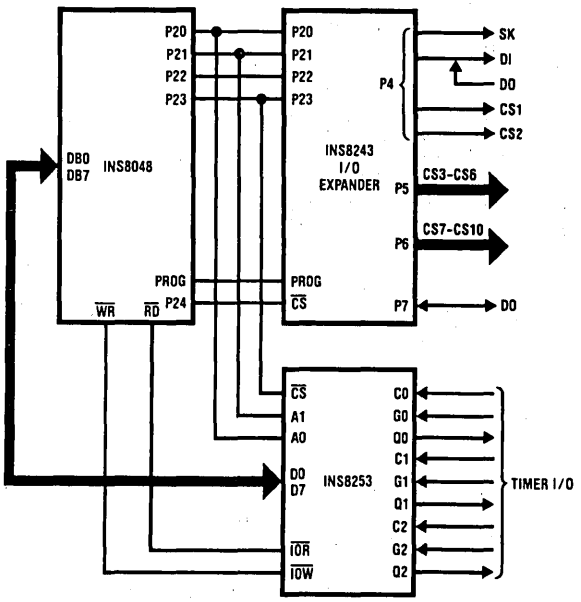
FIGURE 4. Z80—NM93C06 Interface Using Z80-PIO Chip



TL/D/5286–5

* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NM93C06 frequency range.
* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP—NM93C06 Interface

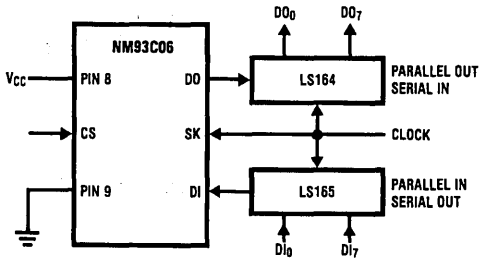


TL/D/5286-6

Expander outputs

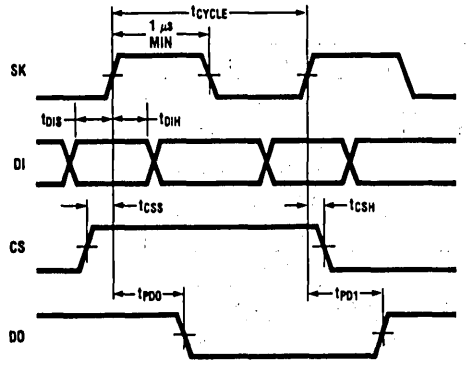
	DI SK	(COMMON)
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion



TL/D/5286-7

FIGURE 7. Converting Parallel Data into Serial Input for NM93C06



TL/D/5286–8

Min	Max
t_{CYCLE} 0	250 kHz
t_{DIS} 400	ns
t_{D1H} 400	ns
t_{CSS} 200	ns
t_{CSH} 0	ns
t_{PD0}	2 μs
t_{PD1}	2 μs

FIGURE 8. NM93C06 Timing

THE NM93C06A

Extremely simple to interface with any μP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Serial Clock input
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read, TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

*Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

**DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NM93C06

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most μPs this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard μP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 μs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for a minimum of ten years independent of V_{CC}, which may be on or off. Read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NM93C06 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

The following is a list of various systems that could use a NM93C06

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control

B. Bathroom scale
Blood analyzer
Bus interface

C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator

D. Data acquisition system
Data terminal

E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system

F. Flow computer
Frequency synthesizer
Fuel computer

G. Gas analyzer
Gasoline pump

H. Home energy management
Hotel lock

I. Industrial control
Instrumentation

J. Joulemeter

K. Keyboard -softkey

L. Laser machine tool

M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector

N. Navigation receiver
Network system
Number comparison

O. Oilfield equipment

P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter

Q. Quiescent current meter

R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer

S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer

T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller

U. Ultrasound diagnostics
Utility telemetering

V. Video games
Video tape system
Voice/data phone switch

W. Winchester disk controller

X. X-ray machine
Xenon lamp system

Y. YAG—laser controller

Z. Zone/perimeter alarm system

The NM93C46—An Amazing Device

National Semiconductor
Application Note 423
Stacy Deming

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NM93C46—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

2^{1024} = number of possible combinations

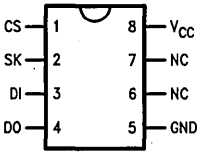
$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NM93C46 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NM93C46. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.

Dual-In-Line Package



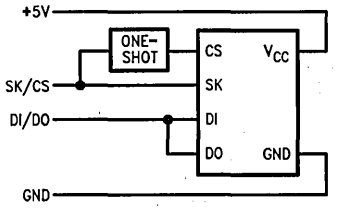
TL/D/8611–1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NM93C46 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

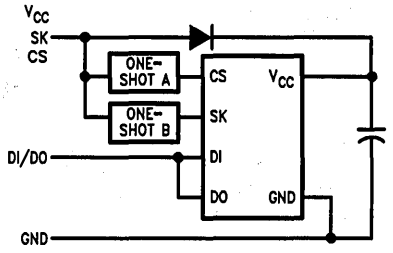


TL/D/8611–2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NM93C46 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611–3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

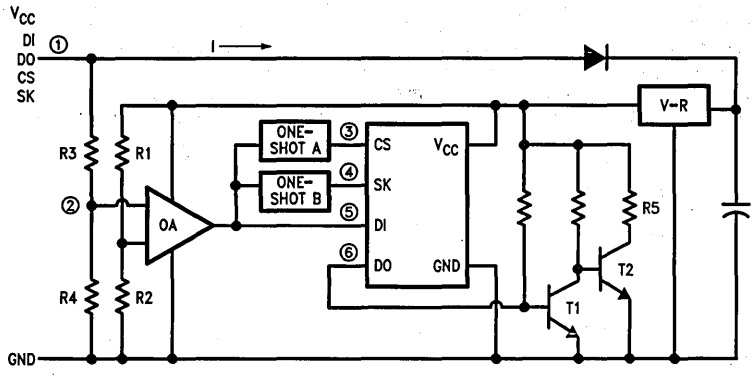
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

CONCLUSION

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

Note: The circuits in this application note feature the NM93C46. The NM93C06 is a pin-compatible part that stores 256 bits.



TL/D/8611–4

R1 = 20K

R2 = 30K

R3 = 15K

R4 = 5K

One-Shot A = ½ MM74HC123

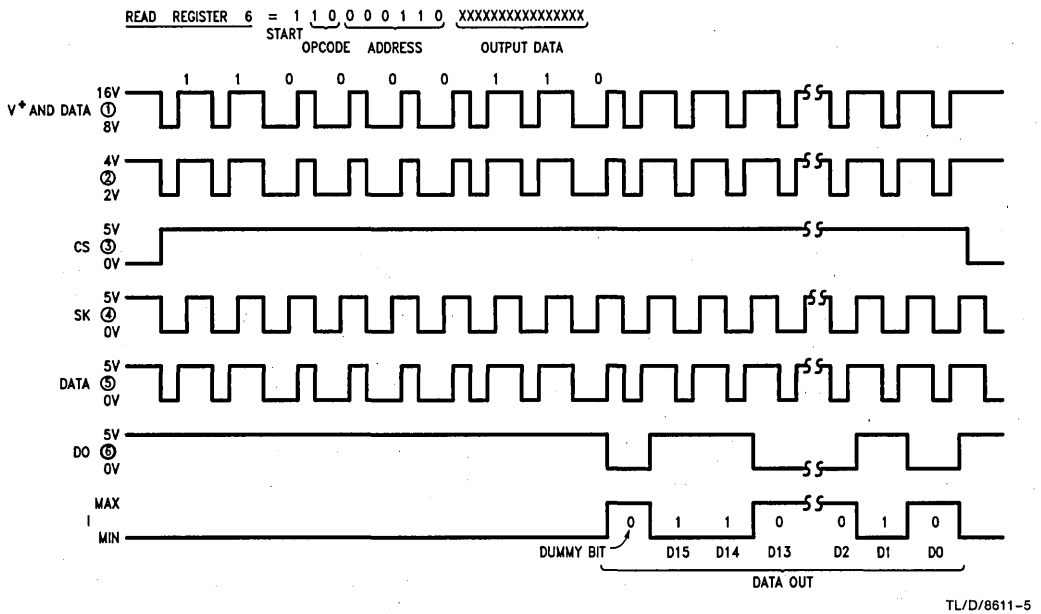
One-Shot B = ½ MM74HC123

V-R = LM2930Z-5.0

OA = LM358

R5 = 1600Ω

FIGURE 4



TL/D/8611–5

FIGURE 5

Using National's MICROWIRE™ EEPROM

National Semiconductor
Application Note 758
Paul Lubeck

National Semiconductor manufactures a wide range of low density serial EEPROMs that use the MICROWIRE interface as a means of communication. Although all of these devices use the MICROWIRE interface, there are slight variations in interfacing due to differences in memory sizes, features, and technology used to implement the device. Additionally, the MICROWIRE interface does not specifically define any protocol, it only defines a basic set of signal lines to interconnect two or more devices. Due to these reasons, additional information is necessary to fully understand how to best interface to National's family of MICROWIRE EEPROM.

The goal of this application guide is to cover a diversity of information in regard to basic timing, interfacing options, and functionality of different EEPROMs. I will use an outline approach, so the appropriate heading can be located easily. Each section attempts to be stand alone so the information can be easily extracted. The outline appears below:

OUTLINE

1.0 Description of EEPROM Families

1.1 CMOS EEPROM

National builds a range of MICROWIRE CMOS EEPROMs in memory sizes ranging from 256-bit to 4906-bit. The NM93C family is the base family and the NM93CS is a similar family with additional features, there are also other devices with slight variations on the interface. All these devices are available with certain "standard" options such as operating temperature ranges and operating voltage ranges, packaging options and test options. These options being fairly standard variations for semiconductor devices, will not be addressed beyond this. The purpose of this article is to address basic functionality and interfacing, including various tricks to simplify or modify the interface.

1.1.1 NM93C Family

The NM93C family of EEPROM is available in 256-, 1024-, 2048-, and 4096-bit sizes. All of these are internally organized in 16-bit words, therefore all data transactions deal with 16 bits. This family of EEPROMs has 7 instructions that deal with read, write, and a basic level of data protection. The instructions are listed in Table I. It is important to note that there is a basic difference in length of the instruction between the NM93C06 or NM93C46 and the NM93C56 or NM93C66. This is due to the larger devices needing additional address bits.

The NM93C family of EEPROM, like all of National's serial EEPROMs have a basic level of write protection that can be turned on or off by the use of the ERASE/WRITE DISABLE (EWDS) and ERASE/WRITE ENABLE (EWEN) instructions. Although there are two erase instructions included in the NM93C family, these are included only for compatibility with older EEPROMs that require erase before write. These EEPROMs don't require erase before write and it is recommended that in application the erase not be used as this adversely affects endurance.

1.1.2 NM93CS Family

The NM93CS EEPROMs are identical to the NM93C family in memory sizes and organization. Making them different, they have two additional functions, sequential read and user configurable write protection, and don't have either of the erase functions, ERASE and ERASE-ALL as they are not needed. Like all of the CMOS EEPROMs, these have self timed programming cycles and operate from a single external supply of either 4.5V to 5.5V or 2.0V to 5.5V. In these devices it is necessary to eliminate the erase cycles from the code as they may adversely affect the performance of the device.

As these have additional functions, the instruction set includes a total of 10 instructions, 3 that operate on the memory array, 2 that deal with the basic write protection and 5 that deal with the user configurable write protection. Refer

to the NM93CS instruction set table (Table II) for definitions of these instructions. As with the NM93C family, there is a basic difference in instruction length depending on memory size.

To further increase data security in these EEPROMs there are also two additional input signals defined, Program Enable (PE) and Protect Register Enable (PRE). These signals are on pins that are unused on the NM93C family providing upward compatibility to the NM93CS devices.

TABLE I. NM93C Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7/A5–A0		Reads data stored in memory.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

TABLE II. NM93CS Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Program address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

1.1.3 Variations

There are two variations on the standard implementation of the Microwire bus. Both variations can be viewed as enhancements. The first enhancement is a Organization (ORG) input that allows the user to select the internal configuration of the memory as either 8 bits wide or 16 bits wide. When the input is high or unconnected, the device is configured as 16 bits wide, when the ORG input is at a low level, the memory is configured as 8 bits wide, but twice as deep. The feature is present on both the NM93C46A and the NM59C11.

The second variation is the STATUS output. This is the Busy/Ready polling to indicate programming status. All other devices have this feature on the Data-Out (DO) output, the NM59C11 alone has status available as a separate output and not on the Data-Out output. This can simplify interfacing to a bidirectional data bus.

2.0 Hardware Connection

2.1 INTERFACE PIN DESCRIPTIONS

In this section, each possible input or output will be described followed by the most popular variations of bus connections. Not all devices have all of the described I/Os. The I/Os are available according to Table III, I/O Functionality.

2.1.1 CHIP SELECT (CS)

Chip Select is used to differentiate between various devices on the same Microwire bus. In the case of EEPROM it cannot be tied high even if it is the only device on the bus as it performs several additional functions. As it applies to any of the Microwire EEPROMs, the rising edge resets the internal circuitry of the device, a function necessary prior to initiating any new cycle. As shown in the functional block diagram *(Figure 1)* chip select also gates the data input and clock input, thus disabling these functions.

During the course of clocking in the start bit, op-code address and data-in or data-out, chip select must be held high continuously, otherwise the internal circuits will be reset and the cycle will have to be started again with a new start bit.

During programming cycles chip select initiates the internal programming cycle. The falling edge of chip select will start the internal programming cycle when a programming op-code has been entered (Erase, Write, Erase All, Write All) and then, in conjunction with Data-Out (DO), will indicate if programming is complete (except the NMOS NMC9306). If programming is complete, Data-Out will drive high, if incomplete it will drive low. In the case of the NMC9306, the user must provide the programming time and in this case chip select must be held low for a minimum of 10 ms, then brought high and clocked to end the programming cycle.

Several additional notes in regard to chip select:

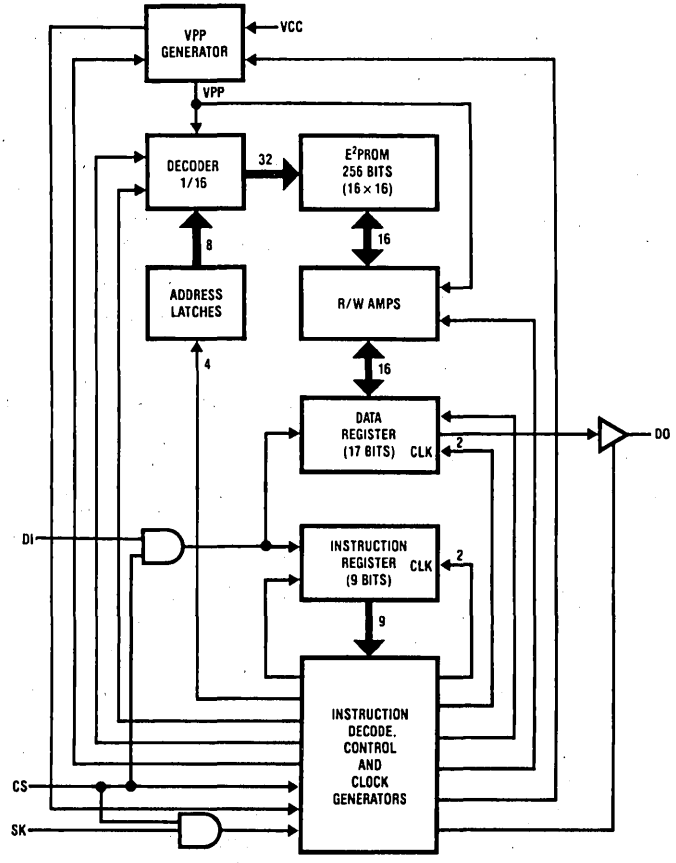
If a programming cycle is partially clocked in and then chip select dropped, the EEPROM may enter into a programming mode. This is determined by how many bits have been clocked in when chip select is dropped. If the start bit, op-code, and all of the address has been clocked in, a programming cycle will be initiated with no or partial data. If less than a complete address has been clocked in, the programming cycle will not be initiated. Refer to *Figure 2*, reference line 1.

In the case of the NM59C11, a programming cycle will not be entered unless a full data field has been clocked in. A full data field may be either 8 or 16 bits depending on the logic level present at the ORG input. A programming cycle will be entered at reference line 2 in *Figure 2* for the NM59C11.

Chip select hold time at the end of a cycle is referenced to the last rising edge of clock (SK). The hold time from the rising edge is the same as the minimum SK high time for the particular device. This is stated in the datasheets as 0 ns hold time from the falling edge of SK which assumes that SK high time is always minimum. In this case SK can be left in the high state or taken low at a later time. Internally chip select gates SK, therefore SK is not critical.

TABLE III. I/O Functionality by Device

	CS	SK	DI	DO	PE	PRE	ORG	STAT
NM93C Family	X	X	X	X				
NM93CS Family	X	X	X	X	X	X		
NM93C46A	X	X	X	X			X	
NM59C11	X	X	X	X			X	X



TL/D/11169–1

FIGURE 1. Block Diagram

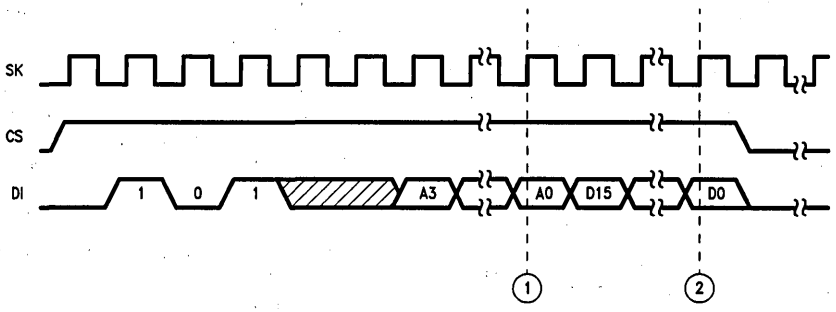


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FIGURE 2. Programming Cycle Point of No Return

2.1.2 SERIAL CLOCK (SK)

The clock input is used to clock all data, address, op-code, and start bits into or out of the EEPROMs. SK clocks both input and output on the rising edge only, the falling edge has no effect on the devices. The only function it is not necessary for is the Busy/Ready Polling which is an asynchronous function.

Since SK is gated by ship select, it is a "Don't Care" any time chip select is low. It is also don't care prior to a start bit being clocked in and during Busy/Ready Polling. During these conditions Data-In (DI) must be held at a low level, otherwise a start bit will be interpreted.

If it is desirable to insert additional clock cycles during a instruction sequence for the purpose of byte aligning the data, there are several places in the data stream they may be inserted as described below:

— On any instruction, zeros can be clocked into the DI input before the start bit. Any number of clock cycles may be added if Data-In (DI) is held at zero. The first 1 clocked in will be interpreted as the start bit. This requires special precautions if a bidirectional data bus is used (Data-In tied to Data-Out) as the Busy/Ready Polling will interfere with the Data-In if it is not cleared out at the end of each programming cycle. See Section 2.3, THREE WIRE BUS, for more information.

— During a Read instruction, it is allowable to continue to clock the device after the 16 bits of data has been clocked out. In the case of the NM93CS family this will cause the memory to increment to the next register and present its contents on the Data-Out pin. In the case of all other devices, whatever was present on the Data-In pin will become present on the Data-Out pin (Fall thru). Refer to *Figure 1,* Block Diagram.

— During a Write or Write-All, additional clock cycles may be added after address A0 and before the valid data. The EEPROM will write into the memory the most recent 16 bits, or in the case of the NM93C46A, the most recent 8 bits or 16 bits depending on the status of the ORG input. Adding additional clocks after the valid data will cause the data to be misaligned. In the case of the NM59C11, the device counts the data bits clocked in and automatically enters the programming mode when it receives a full data field, therefore bits cannot be inserted between A0 and valid data.

— During the EWEN, Erase, Erase All, EWDS, WEN, WDS cycles, it is not necessary to clock in a data field, although it is mandatory to clock in a complete address field, even if the addresses are "Don't Care". Additional clocks can be added after the address field.

2.1.3 DATA-IN (DI)

The Data-In input receives the Start-Bit, Address, and input data in a serial stream, each bit clocked in on the rising edge of SK. DI is gated by the chip select to provide a high degree of noise immunity. As shown in the block diagram, Data-In is routed to both the instruction shift register and the data shift register. When the start bit is clocked into the last bit of the instruction register, the clock is switched to the data register to receive input data and clock data out simultaneous. The Data-Out remains in high impedance unless a read cycle or Busy/Ready status is being done. The safest state is to keep the Data-In pin in a low level as a start bit is a high level.

2.1.4 DATA-OUT (DO)

The Data-Out (DO) output sends read data onto the microwire bus and is clocked out on the rising edge of SK. It also carries the programming status after a programming cycle which is an asynchronous function that does not require the clock. At all other times the Data-Out is in the high impedance state. During a Read cycle, the Data-Out output begins to drive actively after the last address bit (A0) is clocked in. During the Busy/Ready polling it begins to drive active after chip select is raised to a high level.

During the Busy/Ready Polling, the Data-Out output drives low while the device is still in the internal programming cycle. After the EEPROM has completed the internal programming cycle, the Data-Out pin will drive high when chip select is high. Subsequently, if chip select is brought high again, Data-Out will again drive high indicating it has completed the programming cycle. To clear the Busy/Ready Polling it is necessary to raise chip select and clock in a start bit. Once the start bit is clocked in, Data-Out will return to the high impedance state. It is not necessary to continue with a cycle after this start bit has been clocked in, although it is permissible to start a new cycle with this start bit. This clearing of the Busy/Ready status may be necessary if a bidirectional data bus is used (Data-In tied to Data-Out) as the Data-Out output will interfere with the new data being presented on the Data-In input.

2.1.5 PROGRAM ENABLE (PE)

The program enable (PE) input will enable all programming cycles when it is held at a high level during the duration of a programming cycle. Conversely, it will disable all programming, including programming of the protect register, while it is held low. This input has no affect on any other cycle, so it may be permanently tied high or low, or may be used in an active mode. This input is available on the NM93CS family only.

2.1.6 PROTECT REGISTER ENABLE (PRE)

The protect register enable (PRE) input is used to switch between memory operations and protect register operations since the same op-codes are used for both. With the PRE input high, the op-codes define operations in the protect register, with the PRE input low, the op-codes define operations in the memory. This pin may be tied high or low, or used in the active mode. This input is available on the NM93CS family only.

2.1.7 ORGANIZATION (ORG)

The Organization input (ORG) is used to control the internal organization of the memory. The two selectable organizations are 16-bit words and 8-bit words. Simply by holding the ORG pin at a high level, 16-bit words are selected, by holding the input at a low level 8-bit words are selected. When in the 8-bit mode, one additional address bit is required in the instruction sequence since the depth of the memory is doubled. This input is available only on certain device types, refer to the individual datasheets.

2.1.8 STATUS (RDY/BUSY)

The status output indicates the programming cycle status after a programming cycle. When the device is in the programming mode and therefore cannot accept any other cycles, this pin will be low. After completion of the cycle the STATUS pin will be driven high. When this function is present, the Busy/Ready Polling is not available on the Data-Out

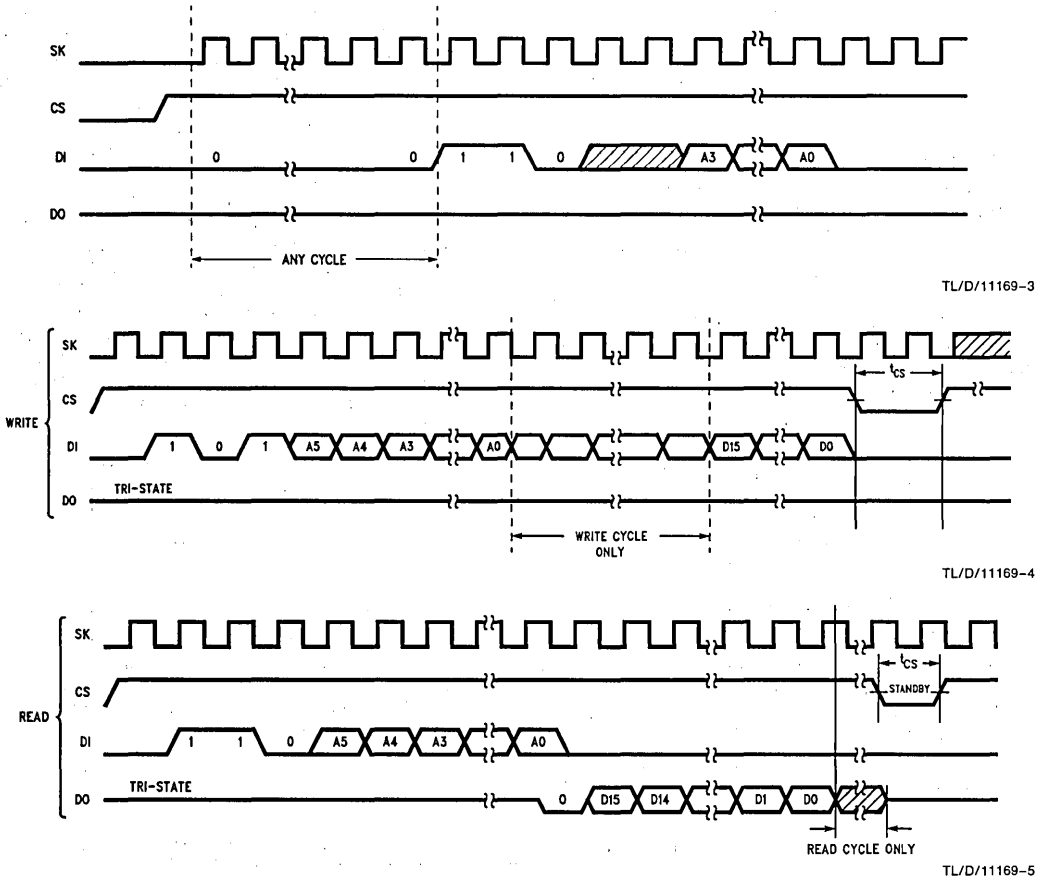

FIGURE 3. Possible Locations for Additional SK Cycles

output. In some systems, particularly those using a bi-directional data bus, this can simplify interfacing by eliminating the possible contention between the Ready indication and the incoming data from the host device. This output is available only on certain device types, refer to the individual datasheets.

2.2 FOUR WIRE BUS

The 4 wire bus is the simplest interconnection between the EEPROM and the host device. In most cases the only signals necessary to provide are clock, chip select, Data-In and Data-Out as shown in *Figure 5.* The PRE, PE, ORG, and STATUS pins are not shown as they are variations on this and the 3 wire bus connection. Multiple devices can be connected to the microwire bus, the only limitations being loading and available chip select means. In some systems it is necessary to have a bi-directional data line as described below in 3 wire bus.

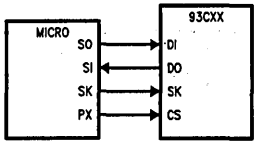

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FIGURE 5. Four Wire Connection

2.3 THREE WIRE BUS

The 3 wire bus operates in the same mode as the 4 wire bus with the exception that the Data-In and Data-Out pins on the EEPROM are tied together. When using this connection, there are two precautions that need to be observed.

— When Data-In is tied to Data-Out, there is a possible conflict between address A0 in the instruction sequence and the dummy bit. This only occurs during a READ cycle. This is not harmful to the device and the internal circuitry of the EEPROM guarantees that the device will function properly under this condition. To decrease the noise created by the condition, a resistor may be placed in the locations indicated in *Figure 6.* The timing diagram in *Figure 7* shows the bus conflict.

— The second possible area of conflict occurs when the Busy/Ready status is on the Data-Out output. Since the device will continue to indicate a Ready status indefinitely after a programming cycle (until a start-bit is clocked in), this can conflict with the beginning of the next cycle if leading zeros are clocked in (See *Figure 7*). The solution is to either use a separate cycle to clear the Ready bit or to eliminate any leading zeros from the instruction sequence. If the Busy/Ready Polling is not used in the application, the easiest solution is to use the NM59C11 that does not have the polling on Data-Out but has it on a separate output.

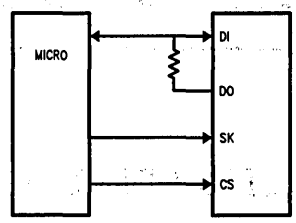

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FIGURE 6. Three Wire Connection Showing Optional Resistor

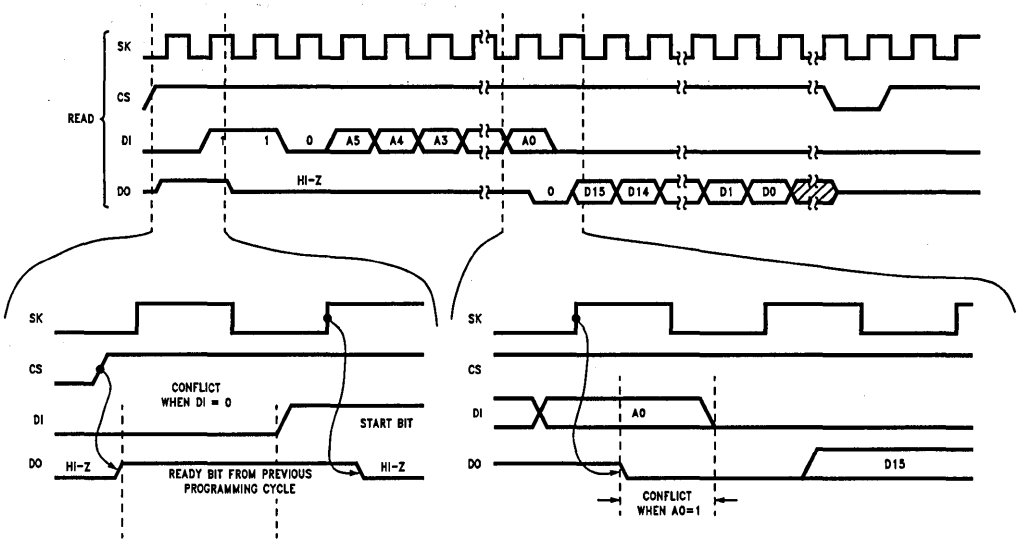

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FIGURE 7. Three Wire Connection Bus Conflict Areas

3.0 Timing Considerations

The following information describing the Microwire bus timing must be used in conjunction with the datasheet as it is an expansion and clarification of the datasheet. First, the basic timings with respect to the clock (SK) will be described, followed by instruction sequence timing, and finally, specific information in each instruction sequence.

3.1. BUS TIMING

The synchronous data timing shown in *Figure 8* is similar to that shown in the various datasheets. There is one significant modification to the timing specification though, the chip select (CS) hold time is referenced to the rising edge of the clock rather than the falling edge. With this modification, the hold time specification must be changed to be the same as the minimum clock (SK) high time. Other significant points are:

— The only active edge of the clock is the rising edge.

— The only time the clock is necessary is when clocking data into or out of the EEPROM. It is not necessary during Busy/Ready Polling.

— The clock may be left in either the high state or low state between cycles. It is safer to leave the clock in the low state.

— When chip select (CS) is high, clock (SK) is a critical signal. With the exceptions noted in Section 2.1.2 tilted SERIAL CLOCK (SK), no additional clock cycles or noise that crosses the V_{IH} or V_{IL} thresholds can be tolerated.

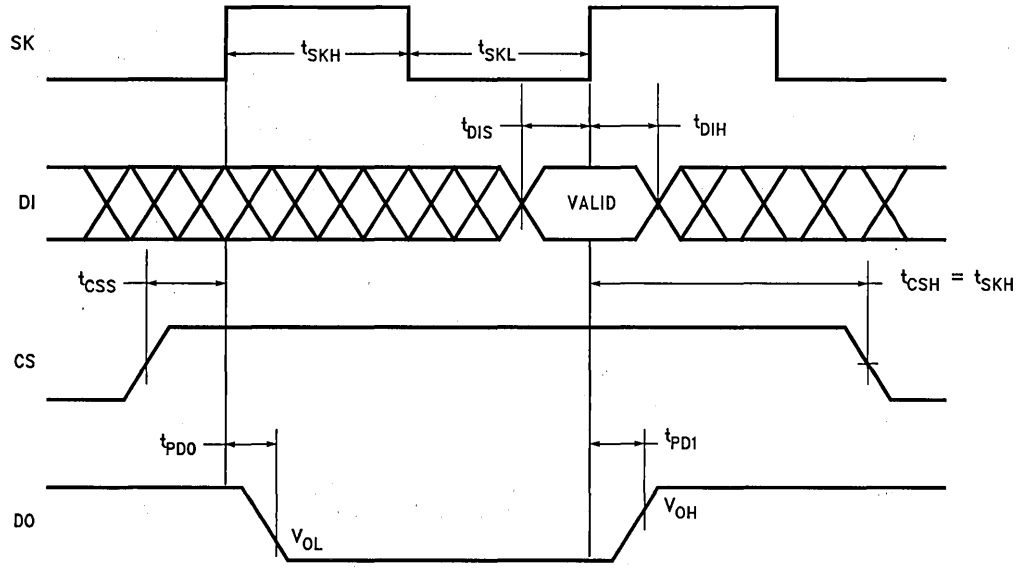

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FIGURE 8. Synchronous Timing

3.2 INSTRUCTION SEQUENCE DESCRIPTIONS

3.2.1 READ CYCLE

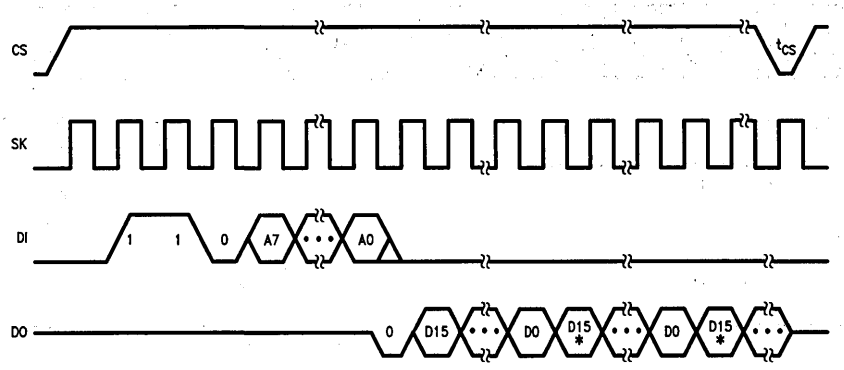
The READ cycle requires the host to raise chip select (CS) and then clock in thru the Data-In (DI) pin a start-bit, op-code, and address. Following clocking in the last address bit, the Data-Out (DO) output comes out of the high impedance state and drives a low level on the output. This is referred to as the dummy bit and is a good indication that a READ mode has been successfully entered if difficulty is encountered during initial debug of a system. The dummy bit is clocked out of the EEPROM on the same rising edge of SK that clocks in the last address bit, A0. This is shown in *Figure 9.*

3.2.2 SEQUENTIAL READ

Sequential read is a read mode available only on the NM93CS family. It is entered by entering a READ cycle and clocking out the first 16-bit word. After reading the first 16-bit word if chip select (CS) is kept high, address A + 1 may be clocked out followed by address A + 2 and so on. When the maximum address is reached, the memory continues in the sequential read mode at address 0. In this manner, the host may operate the memory in a continuous loop read. When initiating a SEQUENTIAL READ, the first data word is proceeded by a dummy bit as in a standard READ, although the dummy bit is supressed in all subsequent data words as shown in *Figure 9.*

3.2.3 ERASE AND ERASE ALL

The ERASE cycles return the contents of the EEPROM to a clear state which is read as 1's. It is not necessary for any of the CMOS EEPROM described in this article, and is included in the NM93C family, NM93C46A, and NM59C11 only for compatibility with older devices that require erasing. It is recommended that the erase cycles be eliminated from the instructions to simplify the code, speed up writing and to improve the endurance obtained in the application. These modes are entered by clocking in a start-bit, op-code, and address. It is not necessary to clock in the data field as it is assumed to be all 1's. It is necessary to clock in the address, even in the case of ERASE-ALL where it is "don't care" in all except the first two bits of the address field which is used as additional op-code bits. After the full address field has been clocked in, chip select must be returned to a low level in initiate the erase cycle. In all devices, except the NMC9306, programming completion can be determined by Polling as shown in *Figure 4,* or a simple 10 ms timeout will guarantee programming is complete if polling is not used.



TL/D/11169–12

FIGURE 9. Sequential Read Sequence

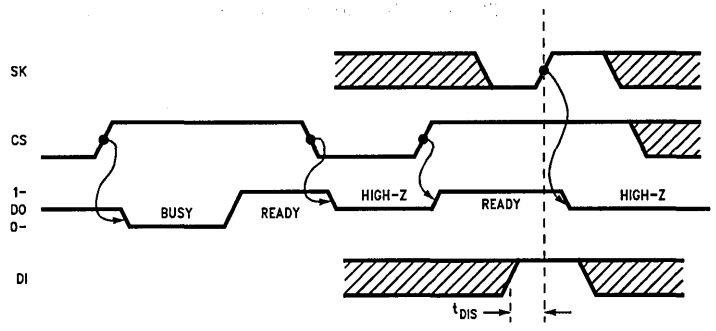


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FIGURE 4. Busy/Ready Polling Sequence

3.2.4 WRITE AND WRITE ALL

The Write and Write All cycles will write a specified data word into the specified address, or in the case of Write All, the same data pattern will be written into all locations. In all devices a new data pattern may be directly written over an existing data pattern without erasing the first data pattern. The write mode is entered by clocking in a start-bit, op-code, address, and data. The full address field must be clocked in for the Write All even though it is don't care in all but the first 2 bits. It is also necessary to clock in a full data field to assure correct alignment of data. The write cycle will be initiated after 8- or 16-bit have been clocked into the device in some of the devices and in other devices after chip select is brought low regardless of how many data bits have been clocked in. Refer to the specific datasheets to determine which method is used.

3.2.5 PROGRAM ENABLE AND PROGRAM DISABLE

Program enable and program disable are the instructions that enable or disable writing and, where included, erasing. The instruction name varies depending on the specific device but includes EWEN, EWDS, WEN, and WDS. These instructions enable or disable the entire memory array with a single instruction. All devices power up in the disable mode and once placed in the enabled mode remain enabled until a disable instruction is performed or V_{CC} is cycled. These instructions provide the most basic level of data protection. Although since most lost data is the result of the host device becoming uncontrolled and performing the "Program Subroutine" it may be helpful to structure the software such that the enable command is not included in the "Program Subroutine" but is in a separate subroutine. If a greater degree of data security is needed, a NM93CS family device is recommended, or other more elaborate schemes involving redundant data storage and polling.

3.2.6 PROTECT REGISTER READ

The protect register read (PRREAD) command is the same as a word read command except the input PRE must be held at a high level and the address is don't care. In spite of the address being don't care, the entire address field must be clocked in. On the Data-Out pin the contents of the protect register will be clocked out MSB first descending to LSB.

3.2.7 PROTECT REGISTER ENABLE

Similar to the programming enable instructions described above, the PREN instruction is necessary to perform any programming instruction the affects the Protect Register. Unlike the enable instructions described above, a PREN must immediately proceed each programming instruction that involves the protect register. The Protect Register programming instructions are PRCLEAR, PRWRITE, and PRDS.

3.2.8 PROTECT REGISTER DISABLE

The protect register disable instruction permanently disables any further programming instructions to the protect register. Therefore it can only be performed once in the lifetime of a NM93CS device. The purpose of it is to permanently configure a portion of the EEPROM as true ROM and a portion as Read/Write EEPROM. Great caution should be exercised prior to executing this instruction as there is no second chance. It is performed by sending a start-bit, op-code and an address field of all 0's while both the PRE and PE inputs are at a high level. This instruction must be immediately proceeded by a PREN instruction.

3.2.9 PROTECT REGISTER CLEAR

The protect register clear instruction will clear the contents of the Protect Register making the entire contents of the EEPROM alterable only if the PRDS instruction has not previously been executed. This is done by clocking in a start-bit, op-code, and address field of all ones. This instruction must be immediately proceeded by PREN instruction and requires that both PRE and PE inputs be held at a high level.

3.2.10 PROTECT REGISTER WRITE

The Protect Register write command (PRWRITE) allows the host to write the protect register with the address where the memory is to be segmented into ROM and EEPROM. The defined address is the first ROM address and the ROM field then continues to the top of memory. To execute this command a start-bit, op-code, and address must be clocked in, the address field containing the memory address that defines the ROM/EEPROM boundary. The PRE and PE inputs must be held at a high level.

3.3 INTERFACING SOLUTIONS

When interfacing serial microwire EEPROMs to microcontrollers there is an apparent conflict that occurs when selecting clock polarity and phase. This can be easily overcome in most situations, although when using some microcontrollers that do not allow selection of either clock polarity or clock phase, the only solution may be to resort to bit set and bit reset instructions to interface to the EEPROM rather than use of the serial interface provided on the microcontroller.

In the instance where there is a dedicated serial interface provided, the conflict typically occurs as follows. *Figure 10* demonstrates an EEPROM READ as this involves data being transferred from the micro to the EEPROM (Start bit, op-code, and address) and data transferred from the EEPROM to the micro (address contents). The conflict occurs in this example when the micros clock sets data up on the falling edge of SK and expects the EEPROM to accept it on the rising edge, but then expects the EEPROM to do the same when it sends data back to the micro.

1. The micro sets up a data bit. A propagation delay after the falling edge the data bit is valid at the EEPROM DI pin.
2. The EEPROM uses the rising edge of SK to clock the data bit into its internal register.
3. When the data direction changes the EEPROM sets the data up starting at the rising edge of SK.
4. The micro attempts to clock the data bit in that was set up on clock edge 3.

This example will work if the micro requires 20 ns or less data hold time after edge 4. If greater than 20 ns is required, an alternate strategy is needed.

1a. The micro sets up the data bit on the rising edge and a propagation delay later it is valid at the EEPROM.

2a. The EEPROM clocks the data into its internal register. The EEPROM requires only 10 ns data hold time, which can normally be guaranteed.

3a. The EEPROM sets the Data-Out up on the rising edge.

4a. The micro clocks the data into it's internal registers on the falling edge of the clock and a minimum data setup and hold time is guaranteed for the micro based on the minimum high and low time of the SK clock used in the application.

It should be noted that in the second example, CS (chip select) is asserted when SK is low. If this cannot be done, the DI input should be low when CS is asserted. If both DI and SK are high when CS is asserted the EEPROM will recognize this as a rising edge of SK. To accommodate this in a design, it is allowable to clock in any number of logic zeros prior to the start bit.

4.0 Conclusion

The serial EEPROM offered by National all share a common structure. Separating them are various features that give benefit to various applications such as the need for a bi-directional data bus or need for one byte word width. There are a number of "tricks" that may simplify interfacing to these which can easily be understood with the help of a functional block diagram. Given this information the overall job of using a serial interface EEPROM will be simpler.

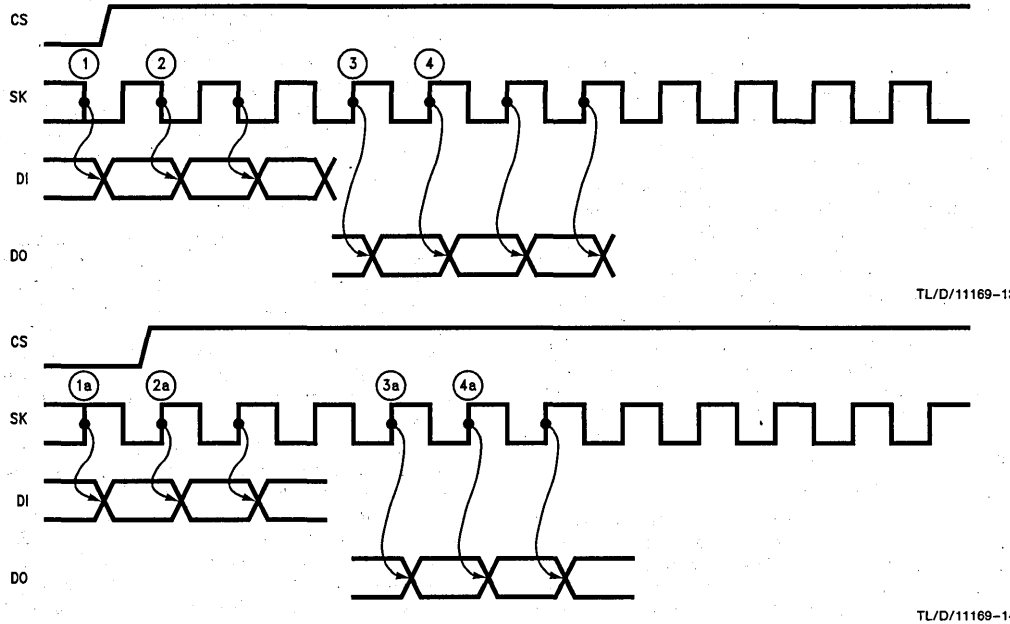


FIGURE 10

Using an EEPROM—I²C™ Interface NM24C02/03/04/05/08/09/16/17

National Semiconductor
Application Note 794
N. Brian Underwood

INTRODUCTION

National Semiconductor's NM24C EEPROMs are designed to interface with Inter-Integrated Circuit (I²C) buses and hardware. NSC's electrically erasable programmable read only memories (EEPROMs) offer valuable security features (write protection), two write modes, three read modes and a wide variety of memory sizes. Applications for the I²C bus and NM24C memories are included in SANs (small-area networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

I²C BACKGROUND

The I²C bus configuration is an amalgam of microcontrollers and peripheral controllers. By definition: a device that transmits signals onto the I²C bus is the "transmitter" and a device that receives signals is the "receiver"; a device that controls signal transfers on the line in addition to controlling the clock frequency is the "master" and a device that is controlled by the master is the "slave". The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. It is possible to combine several masters, in addition to several slaves, onto an I²C bus to form a multimaster system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16k; typical device capacitance is 10 pF. Up to eight E²PROMs can be connected to an I²C bus, depending on the size of the memory device implemented.

Simplicity of the I²C system is primarily due to the bidirectional 2-wire design, a serial data line (SDA) and serial clock line (SKL), and to the protocol format. Because of the efficient 2-wire configuration used by the I²C interface compared to that of the MICROWIRE™ and SPI interface, reduced board space and pin count allows the designer to have more creative flexibility while reducing interconnecting cost.

OPERATING NATIONAL SEMICONDUCTOR'S NM24Cs

The NM24C E²PROMs require only six simple operating codes for transmitting or receiving bits of information over the 2-wire I²C bus. These fields are explained in greater detail below and briefly described hereafter: a start bit, a 7-bit slave address, a read/write bit which defines whether the slave is a transmitter or receiver, an acknowledge bit, message bits divided into 8-bit segments and a stop bit.

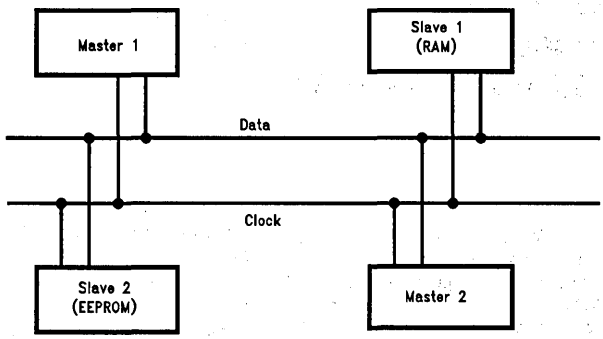
For efficient and faster serial communication between devices, the NM24C Family features page write and sequential read.

The NM24C03/C05/C09/C16/C17 Family offers a security feature in addition to standard features found in the NM24C02/C04/C08/C16 Family. The security feature is beneficial in that it allows Read Only Memory (ROM) to be implemented in the upper half of the memory to prevent any future programming in that particular chip section; the remaining memory that has not been write protected can still be programmed. The security feature in the NM24C03/C05/C09/C17 Family does not require immediate implementation when the device is interfaced to the I²C bus, which gives the designer the option to choose this feature at a later date. Table I displays the following parameters: memory content, write protect and the maximum number of individual I²C E²PROMs allowed on an I²C bus at one time if the total line capacitance is kept below 400 pF.

Code used to interface the NM24Cs with National Semiconductor's COP8 Microcontroller Family is listed in a latter section of this application note for further information to the reader.

TABLE I

Part No.	Number of 256x8 Page Blocks	Write Protect Feature	Max. Parts
NM24C02	1	No	8
NM24C03	1	Yes	8
NM24C04	2	No	4
NM24C05	2	Yes	4
NM24C08	4	No	2
NM24C09	4	Yes	2
NM24C16	8	No	1
NM24C17	8	Yes	1



TL/D/11268–1

FIGURE 1. I²C-Bus Configurations

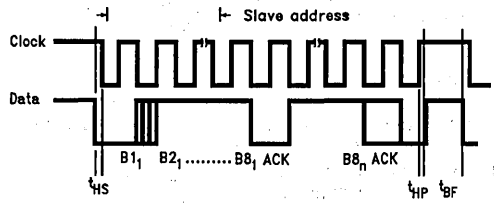


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FIGURE 2. I²C Bus Timing

Start Condition

— Clock and Data line high (Bus free)

— Change Data line from high to low

— After $t_{HS(Min)}$ = 4 μs the master supplies the clock

Acknowledge

— Transmitting device releases the Data line

— The receiving device pulls the Data line low during the ACK-clock if there is no error

— If there is no ACK, the master will generate a Stop Condition to abort the transfer

Stop Condition

— Clock line goes high

— After $t_{HP(Min)}$ = 4.7 μs the Data lines go high

— The master maintains the Data and Clock line high

— Next Start Condition after $t_{FB(Min)}$ = 4.7 μs is possible

START/STOP CONDITIONS

If both the data and clock lines are HIGH, the bus is not busy. To attain control of the bus, a start condition is needed from a master; and to release the lines, a stop condition is required.

Start Condition: HIGH-to-LOW transition of the data line while the clock line is in a HIGH state.

Stop Condition: LOW-to-HIGH transition of the data line while the clock line is in a HIGH state.

The master always generates the start and stop conditions. After the start condition the bus is in the busy state. The bus becomes free after the stop condition.

DATA BIT TRANSFER

After a start condition "S" one databit is transferred during each clock pulse. The data must be stable during the HIGH-period of the clock. The data line can only change when the clock line is at a LOW level.

Normally each data transfer is done with 8 data bits and 1 acknowledge bit (byte format with acknowledge).

ACKNOWLEDGE

Each data transfer needs to be acknowledged. The master generates the acknowledge clock pulse. The transmitter releases the data line (SDA = HIGH) during the acknowledge clock pulse. If there was no error detected, the receiver will pull down the SDA-line during the HIGH period of the acknowledge clock pulse.

If a slave receiver is not able to acknowledge, the slave will keep the SDA line HIGH and the master can then generate a STOP condition to abort the transfer.

If a master receiver keeps the SDA line HIGH, during the acknowledge clock pulse the master signals the end of data transmission and the slave transmitter release the data line to allow the master to generate a STOP-condition.

ARBITRATION

Only in multimaster systems.

If more than one device are potential masters and more than one desires access to the bus, an arbitration procedure takes place: if a master transmits a HIGH level and another master transmits a LOW level, the master with the LOW level will get the bus and the other master will release the bus; and the clock line switches immediately to the slave receiver mode. This arbitration could carry on through many bits (address bits and data bits are used for arbitration).

FORMATS

There are three data transfer formats supported:

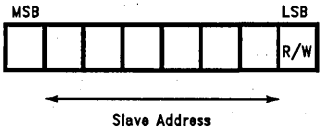
— Master transmitter writes to slave receiver; no direction change

— Master reads immediately after sending the address byte

— Combined format with multiple read or write tranfers.

ADDRESSING

The 7-bit address of an I²C device and the direction of the following data is coded in the first byte after the start condition:



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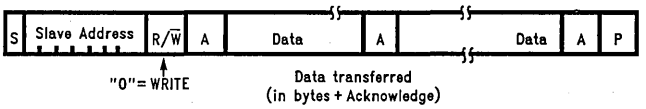
A "0" on the least significant bit indicates that the master will write information to the selected Slave address device; a "1" indicates that the master will read data from the slave.

Some slave addresses are reserved for future use. These are all addresses with the bit combinations 1111XXX and 0000XXX. The address 00000000 is used for a general call address, for example, to initialize all I²C devices (refer to I²C bus specification for detailed information).

Master Transmits to Slave, No Directon Change



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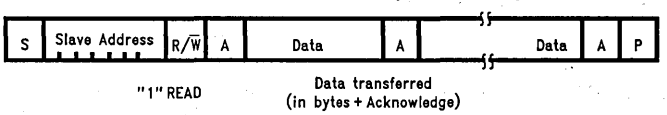
Master Reads Slave Immediately after First Byte



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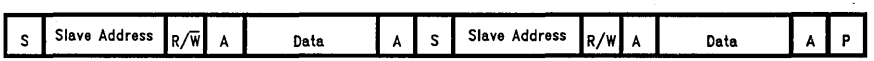
The master becomes a master receiver after first ACK

Combined Formats



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n bytes Data + ACK n bytes Data + ACK

S = Start Condition A = Acknowledge P = Stop Condition

FIGURE 3. I²C-Bus Transfer Formats

TIMING

The master can generate a maximum clock frequency of 100 KHz. The minimum LOW period is defined as 4.7 μs; the minimum HIGH period width is 4 μs; the maximum rise time on SDA and SCL is 1 μs; and the maximum fall time on SDA and SCL is 300 ns.

Figure 4 shows the detailed timing requirements.

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	100	kHz
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD;STA}$	Hold Time Start Condition. After this Period the First Clock Pulse is Generated	4.0		μs
t_{LOW}	The LOW Period of the Clock	4.7		μs
$t_{SU;STA}$	Setup Time for Start Condition (Only Relevant for a Repeated Start Condition)	4.7		μs
$t_{HD;DAT}$	Data in Hold Time	5 0*		μs μs
$t_{SU;DAT}$	Setup Time Data	250		ns
t_r	Rise Time of Both SDA and SCL Lines		1	μs
t_f	Fall time of Both SDA and SCL Lines		300	ns
$t_{SU;STO}$	Setup Time for Stop Condition	4.7		μs

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

FIGURE 4. I²C-Bus Timing Requirements

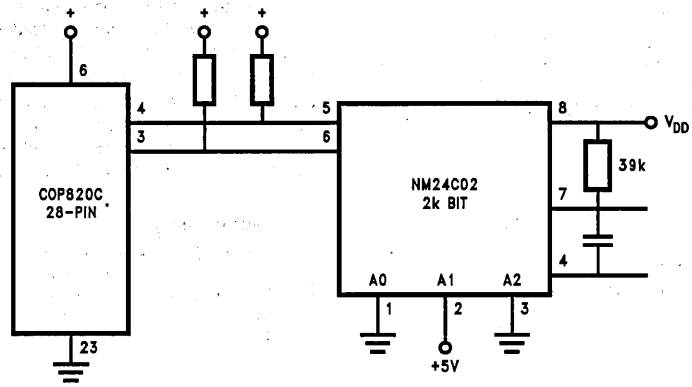

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FIGURE 5. I²C Bus EEPROM/μController Configuration Used for Sample Code

SOFTWARE TASKS

I. Write fixed values to E2PROM cells

II. Read values back from E2PROM and save in RAM locations from COP

Note: I²C Bus Modes Used:

Master Transmitter $\overset{SDA}{SCL}\rightarrow$ Slave Receiver

Master Receiver $\overset{SDA}{SCL}\rightarrow$ Slave Receiver

REMARKS

— The I²C bus, 2-wire serial interface generally requires a pull-up resistor on the SDA line and the SCL line, depending on whether TTL or CMOS hardware interfacing exists.

— I²C bus compatible μC's or peripherals have OPEN DRAIN outputs at SDA and SCL.

— COP800 does not have OPEN DRAIN outputs, but the "bus requirements" can be met by switching SDA and SCL connections into TRI-STATE® for the following cases:

The bus is not accessed

A slave has to send an acknowledge bit.

— MICROWIRE can not be used for I²C bus operations.

— Current sink capability on SDA and SCL must be 3 mA to maintain "Low Level" (an I²C bus spec.).

```
.TITLE IIC - EEPROM  ROUTINES'
.INCLD COP800.INC
.CHIP 840
.LIST X '21

        * * *TASK RELATED RAM - DECLARE* * *

EEADR                                   = 002       ;ADDRESS OF EEPROM
EEWRD                                   = 003       ;WORD ADDRESS EEPR.
EEDAT1                                  = 004       ;DATA TO EECELL
EEDAT2                                  = 005       ;SECOND BYTE
FLAG                                    = 010       ;FLAG–WORD
EEREAD                                  = 012       ;READ–DATA FROM EE
                                        = 013       ;SECOND BYTE
                                        = 014       ; THIRD BYTE
                                        = 015       ;FOURTH BYTE
BITCO                                   = 0F0       ;COUNTER FOR BITSHFT

INIT:
   LD SP,                               #06F
   LD B,                                PORTLD      ; INIT LS, L3 FOR EE-
   LD  [B+],                            #00C        ;OPERATIONS
   LD  [B],                             #00C
   LD B,                                #EEDAT2     ; INIT RAMS
   LD  [B-],                            #034        ;FIXEED VALUES FOR
   LD  [B-],                            #012        ; EEWRITE (2 BYTES)
   LD  [B-],                            #0A0        ; MIRROR OF #05
   LD  [B]                              #025        ; MIRROR OF "A5"

      ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
      ; EXAMPLE: IF ADDRESS BYTES IS    "1010 010X THEN          *
      ; STORE:                          "X010 0101               *
      ; INTO RAM (X=0/1; WRITE/READ)                             *
      ;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

   LD PSW,                              #00         ;LOAD PSW
   LD CNTRL,                            #00         ;AND CNTRL REG.
   LD FLAG,                             # 0
   .FORM

            ;  * * * * * * * * * * * * * * * * * * * * * * * * * * *
            ;  * * * *    DO WRITE TO EE-PROM    * * * *
            ;  * * * * * * * * * * * * * * * * * * * * * * * * * * *

         ; (2 BYTE SUCCESSIVE WRITE)

   SBIT 0,                              FLAG        ;SET FLAG FOR WRITE
   LD B,                                PORTLD      ;POINT LPORT DAT REG.
                                                    ;TO MODIFY "SDA, SCL"
   RBIT 2 [B],                                      ;PREPARE FOR START
   JSR STACON                                       ;CONDITION.
   JSR WAIT                                         ;AFTER WRITE TO EE.
                                                    ;WAIT FOR > THAT 40
```

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```
                ;**********************
                ;** DO THE START CONDITION **
                ;** AND SHIFT OUT ADRESS - **
                ;** BYTE AND WORD-ADRESS **
                ;**********************

STACON:
    RBIT 3,                         PORTLD      ;FINISH START COND.
    LD B,                           #EEADR      ;PREPARE TO CLOCK
                                                ;OUT ADDRESS.
LOPA:
    LD BITCO,                       #008        ;DO SETS OF 8 BITS

LOPA 1:
    IFBIT 0, [B]                                ;SWITCH SDA BEFORE
    JP ONE,                                     ;SCL
    RBIT 2,                         PORTLD      ;SET BIT LEVLE "0"
    JP CLK

ONE:
    SBIT 2,                         PORTLD      ;SET BIT LEVEL "1"
    JP CLK                                      ;ENSURE SAME BIT
                                                ;LENGTH

CLK:
    SBIT 3,                         PORTLD      ;DO CLOCK PULSE
    NOP
    NOP
    RBIT 3,                         PORTLD      ;ENSURE> 4USEC
    RBIT 2,                         PORTLD      ;SWITCH ALSO SDA LOW
    .FORM

    LD A, [B]                                   ;ROTATE BYTE ONE
    RRC A,                                      ;BIT POS. RIGHT
    X A, [B]                                    ;AND SAVE
    DRSZ BITCO                                  ;CHECK IF 8 BITS
    JP LOPA1,                                   ;SHIFTED
    LD A, [B+],                                 ;DECREMENT 8
    IFBIT 1,                        FLAG        ;CHECK IF READ
    JMP,                            GETDAT      ;3RD BYTE IS NEXT?
                                                ;IF SO, THEN READ.
    JSR ACK,                                    ;GET ACKNOWLEDGED
                                                ;WHEN 8 BITS ARE
                                                ;SHIFTED.
    IFBIT 0,                        FLAG        ;CHECK IF READ
    JP CEC1,                                    ;OR WRITE OPERATION.
    IFBNE                           #04         ;ON READ (HERE)
    JMP LOPA,                                   ;IF NOT 2 BYTES YET
    RET                                         ;AFTER EE-ADDRESS AND
                                                ;WORD ADDRESS ARE SHFT.

CEC1:
    IFBNE,                          #06         ;1ST AND 2ND DATA-
    JMP LOPA,                                   ;BYTE (3RD + 4TH)
```

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```
                                                    ;NSEC TO PROPERLY
                                                    ; ERASE WRITE.

LD B,                                  #EEDAT2      ; INIT RAMS
LD  [B-],                              #078         ;ANOTHER 2 BYTES
LD  [B-],                              #056         ;OF FIXED DATA
LD  [B-],                              #0E0         ; MIRROR OF #07
LD [B],                                #025         ; MIRROR OF "A5"
LD B,                                  PORTLD       ;POINT LPORT DAT REG.
                ; TO MODIFY "SDA, SCL"
RBIT 2, [B],                                        ;PREPARE FOR START
JSR STACON,                                         ;CONDITION.
JSR WAIT,                                           ;AFTER WRITE TO EE.
                                                    ; WAIT FOR > THAN 40
                                                    ;MSEC TO PROPERLY
                                                    ; ERASE WRITE.

.FORM

        ; ****************************
        ; **** DO READ FROM EE-PROM ****
        ; ****************************

            (READ 4 SUCCESSIVE BYTES)
RBIT 0                                 FLAG         ; INDICATE READ
LD B,                                  #EEWRD       ; INIT RAMS
LD  [B-],                              #0A0         ; MIRROR OF #05
LD [B],                                #025         ; MIRROR OF "A5"

        ; ****************************
        ; ** FIRST 2 BYTES SAME AS IF WRITE **
        ; ****************************

                                (IN TERMS OF TRNSMIT)
LD B,                                  #PRTLD       ;PREPARE
RBIT 2 [B]                                          ;FOR
JSR STACON,                                         ;START COND.
                                                    ; AND SHIFT 1ST
                                                    ;2 BYTES.
SBIT 2,                                PORTLD       ;PREPARE FOR
NOP,                                                ;ANOTHER START–
NOP,                                                ;CONDITION,
SBIT 3,                                PORTLD       ;SDA HIGH FIRST.
SBIT 1,                                FLAG         ;INDICATE THAT
                                                    ;3RD BYTE IS NEXT
LD B,                                  #EEWRD       ; INIT RAMS
LD  [B-],                              #0A0         ; MIRROR OF #05
LD [B],                                #0A5         ;MIRROR OF "A5"
                                                    ;PERFORM ANOTHER
RBIT 2, [B],                           PORTLD       ;START
JSR STACON
RBIT 1,                                FLAG
JMP INIT                                            ;CLOSE THE LOOP WHEN
.FORM                                               ;FINISHED
```

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```
STP:
    SBIT 3,                          PORTLD      ; ESTABLISH STOP-
    NOP,                                         ; CONDITION
    SBIT 2,                          PORTLD
    RET,
    .FORM

        ********************************
        ;**  GET 8BIT OF DATA FROM EE-PROM **
        ********************************

GETDAT:
    JSR ACK,                                     ; GET ACKNOWLEDGMENT
    LD B,                            #EEREAD     ; POINT FIRST READ RAM
    JP                               GETDT1      ; AND READ IN

GETDAT:
    JSR ACK,                                     ; ACKNOWLEDGMENT TO EE-
                                                 ; PROM WHEN 8 BITS
                                                 ; ARE SHIFTED IN.

GETDAT1:
    LD BITCO,                        #008        ; INIT BIT COUNTER
    RBIT 2,                          PORTLC      ; BEFORE READING, PUT
    RBIT 2,                          PORTLD      ; 'SDA' INTO HIGH-Z.

LOPB:
    SBIT 3,                          PORTLD      ; DO CLOCK HIGH
    RBIT 7, [B]                                  ; READ IN EEDATA
    IFBIT 2,                         PORTLD      ; IN SETS OF 8 BITS
    SBIT 7, [B]
    RBIT 3,                          PORTLD      ; DO CLOCK LOW
    DRSZ BITCO,                                  ; CHECK IF 8 BITS
    JP SHFT                                      ; ARE SHIFTED
    LD A, [B+],                                  ; INCREMENT B
    IFBNE                            #06         ; CHECK IF 4 BYTES
    JMP GETDT,                                   ; ARE SHIFTED IN?
    SBIT 2,                          PORTLC      ; PUT L2=0
    JMP STP                                      ; WHEN TRUE, DO STOP
                                                 ; CONDITION AND
                                                 ; RETURN

    .FORM

SHFT:
    LD A, [B],                                   ; ROTATE BITS ONE
    RRC A                                        ; POSITION RIGHT
    X A, [B]
    JP LOPB

        ************************************
        ; ** SIMPLE ROUTING TO DO 40 MSEC DELAY **
        ************************************
```

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```
WAIT:
    LD 0F1              #0.20       ;SIMPLE WAIT LOOP

LOPD:
                                    ;TO PRODUCE>40MSEC
    LD 0F2,             #OFF        ;TIMEOUT

LOPC:
                                    ;TO PROPERLY PROGRAM
    DRSZ 0F2,                       ;EEPROM. TIME REQUIRED
    JP LOPC,                        ;TO ERASE/WRITE
    DRSZ0F1,                        ;THE EEPART.
    JP LOPD
    RET

ACK1:
    SBIT 2,             PORTLC      ;INDICATE TO EE-PROM
    JP ACLK,                        ;(PUT DATA LINE LOW)

ACK:
    RBIT 2,             PORTLC      ; PUT DATA-LINE HI-Z

ACLK:
                                    ;AND GET ACKNOWLEDGE
    SBIT 3,             PORTLD      ;8 BITS ARE SHIFTED,
    NOP                             ;DO A DUMMY CLOCK
    NOP
    NOP
    RBIT 3,             PORTLD      ;(FOR ACKNOWLEDGE)

    SBIT 2,             PORTLC
    RET
    .END
```

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Enhancing the Performance of Serial CMOS EEPROMs

National Semiconductor
Application Note 822
Sean Long

TABLE OF CONTENTS

INTRODUCTION

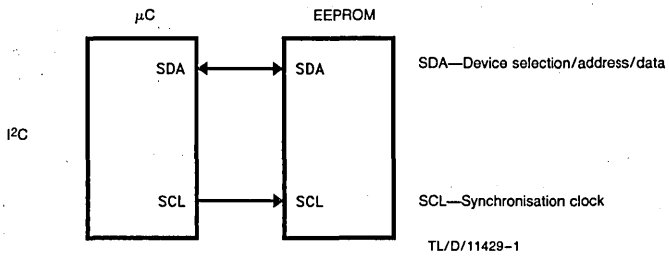
This application note presents a number of solutions to help a system designer overcome some possible limitations of serial Electrically Erasable PROMs (EEPROMs) to obtain greater system performance and flexibility.

This note assumes that the reader is familiar with National Semiconductor's range of MICROWIRE EEPROMs (NM93Cxx and NM93CSxx) and I²C (NM24Cxx) devices.

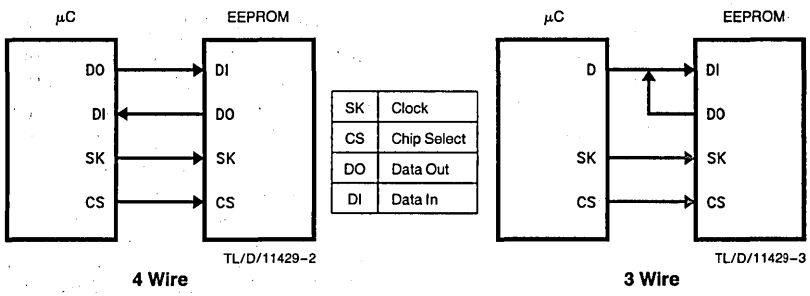
1.0 COMPARING SERIAL EEPROM INTERFACE STANDARDS

The two industry standard serial interfaces for EEPROMs are the MICROWIRE and I²C-bus specifications. The key features of these two interfaces are shown in *Figure 1.*

Serial Interface Standards



MICROWIRE



	MICROWIRE	I²C
Max Bus Speed	1 MHz	100 kHz
Number of Active Pins	4	2
Maximum Memory	N/A	16 kbit
Acknowledge	No	Yes
Data Size	8- or 16-Bit	8-Bit
Block Write	No	Yes
Sequential Read	Yes	Yes
Number of Devices on Bus	Limited by Port Pins	32 Functions, 256 Total Devices

FIGURE 1. MICROWIRE vs I²C

The key advantages of the MICROWIRE interface compared to the I²C-bus are:

- Higher system speed (1 MHz vs 100 kHz)
- Greater memory size (unlimited vs 16 kbit maximum)
- Address programming pins are not required on peripherals

The key advantages of the I²C-bus are:

- Only requires 2 pins (SDA and SCL)
- Allows easy implementation of a multi-master system

Both interface standards are supported by a variety of microcomputers; some have dedicated interfaces built-in (for example National Semiconductor's COPS™), while other microcomputers can interface to either standard by toggling I/O port pins as required.

2.0 I²C-BUS MEMORY SIZE

2.1 I²C-Bus Concept

The I²C-bus uses two wires, serial data (SDA) and serial clock (SCL) to carry information between various integrated circuits connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver depending on the function of the individual device. A typical I²C-bus system is shown in *Figure 2*.

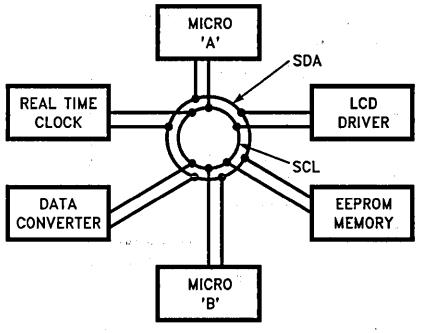


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FIGURE 2. A Typical I²C-Bus System

In addition to transmitters and receivers, devices can also be defined as masters or slaves when performing data transfers.

A master is: — the device which initiates data transfer
— generates clock signals
— terminates a data transfer
— e.g., a microcomputer

A slave is: — the device addressed by a master
— e.g., a memory

Note: The I²C-bus is a multi-master bus; each master generates its own clock signals when transferring data on the bus.

2.2 EEPROM Memory on the I²C-Bus

The I²C-bus specification allows a maximum of 16 kbits of EEPROM. The 4-bit device type identifier string which follows the START condition is 1010 for EEPROMs. National Semiconductor manufactures a range of different size I²C EEPROMs (2k, 4k, 8k, and 16 kbits) to allow a system designer to select the amount of memory required.

EEPROMs on the I²C-bus may be configured in any manner required, providing the total memory addressed does not exceed 16 kbits. EEPROM memory Addressing is controlled by two methods:

- Hardware configuring the A0, A1, and A2 pins (device address pins) with pull-up or pull-down resistors
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the slave address string)

Pin Descriptions

Serial Clock (**SCL**)	an input used to clock data into and out of the memory
Serial Data (**SDA**)	a bidirectional pin used to transfer data into and out of the device
Device Address Inputs	connected to V_{CC} or V_{SS} to configure EEPROM address

Device	A0	A1	A2	Effect of Address	
NM24C02/03	ADR	ADR	ADR	$2^3 = 8$	(8) × (2k) = 16k
NM24C04/05	X	ADR	ADR	$2^2 = 4$	(4) × (4k) = 16k
NM24C08/09	X	X	ADR	$2^1 = 2$	(4) × (8k) = 16k
NM24C16/17	X	X	X	$2^0 = 1$	(1) × (16k) = 16k

ADR—active pin used for device addressing

X—not used for addressing (must be tied to ground/V_{SS})

Many applications now require greater than 16 kbits of EEPROM on an I²C system. For the purpose of this application note we will consider how to use multiple 16 kbit (NM24C16/17) devices in an I²C bus system to increase the total memory size.

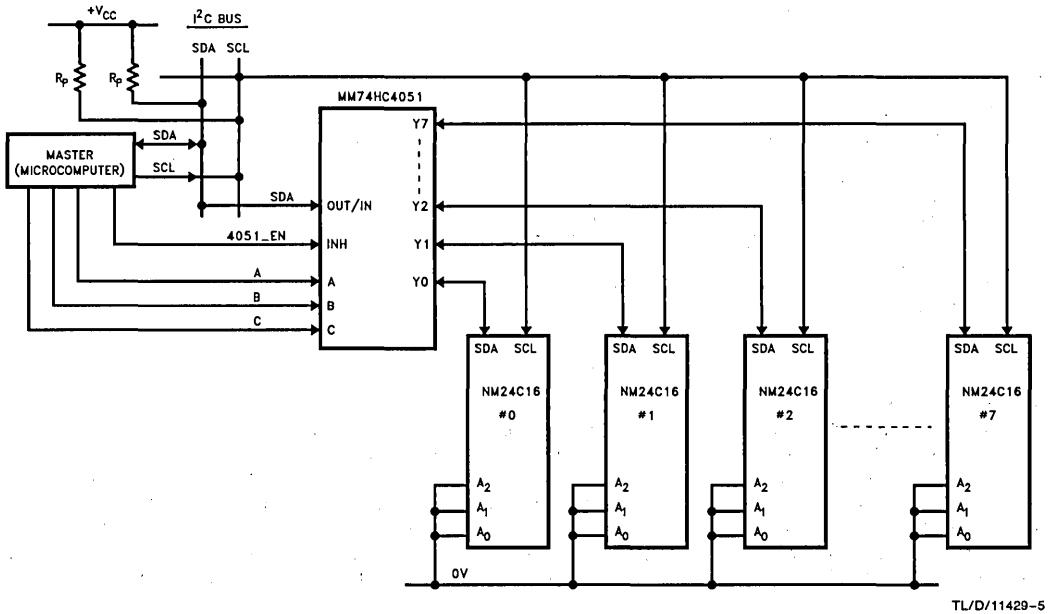


FIGURE 3. Increasing I²C-Bus EEPROM → 16 kbits

2.3 Bank Switching I²C EEPROMs

A circuit to increase the EEPROM memory size of the I²C bus, while still maintaining full software and hardware compatibility, is shown in *Figure 3*.

The circuit connects the serial clock (SCL) to each memory device, but the serial data (SDA) is connected by a multiplexed, bidirectional analog switch (MM74HC4051). The MM74HC4051 is an 8-channel analog multiplexer which connects together the outputs of 8 digitally controlled analog switches, thus achieving an 8-channel multiplexer. These switches are bidirectional, allowing any analog input to be used as an output and vice-versa. They have a low "on" resistance, typically 50Ω or less.

The MM74HC4051 is controlled by four inputs; INH which enables the switches to be "on" and inputs A, B and C which select one of the eight switches. The master (microcontroller) generates these four control signals to the MM74HC4051 directly.

In this case a typical software flow would be:

— set microcontroller port pins to select the NM24C16/17 required

— [DEVICE TYPE] → [DEVICE ADDRESS] → [PAGE BLOCK ADDRESS] → [BYTE ADDRESS]

This means that this low cost solution still maintains full I²C-bus compatibility.

Worst Case Analysis

I²C-Bus Specification	MM74HC4051 Solution Specification
C_{max} = 400 pF (Note 1)	C_{IN} = 90 pF max
f_{max} = 100 kHz (Note 2)	t_{PD} = 15 ns max
= 10 μs Period	= 5 ns typical
I_{OL} max = 3 mA	R_{ON} max = 140Ω

Note 1: The maximum number of devices connected to the I²C-bus is controlled by the maximum allowable capacitance which is 400 pF per line.

Note 2: The maximum I_2C system clock is 100 kHz. The propagation delay through the MM74HC4051 is small enough to ensure that data set-up time of 250 ns min is not violated.

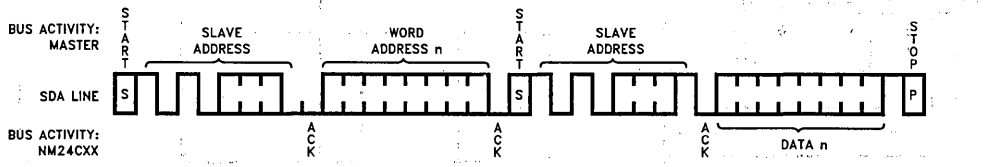
3.0 ACCESSING SERIAL EEPROMs

3.1 I²C System

READ Operations

3.1.1. Random Read

Random read allows the master to access any memory location in a random manner. The master first performs a "dummy" write operation, then issues a start condition followed by the slave address and then the word address to be read. (See *Figure 4.*)



TL/D/11429–6

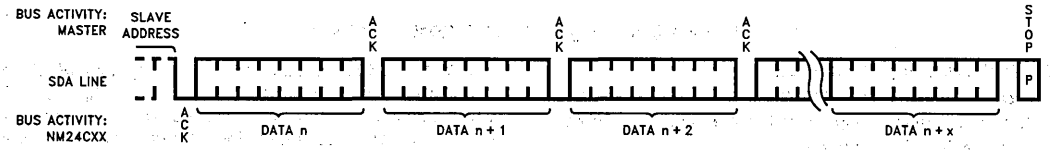
FIGURE 4. Random Read

3.1.2 Sequential Read

A sequential read operation allows the master to read a continuous stream of data from the memory without having to keep clocking in the word address and waiting for the memory to assert the ACK signal.

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as normal, however, the master now responds with an acknowledge (ACK) to indicate that it requires additional data. The memory continues to output data for each ACK received until the master does not send an ACK and generates a STOP condition.

The address counter increments all word address bits, allowing the entire memory contents to be read during one operation. When the top memory address is reached then the counter "rolls-over" to zero and continues counting. (See *Figure 5.*)

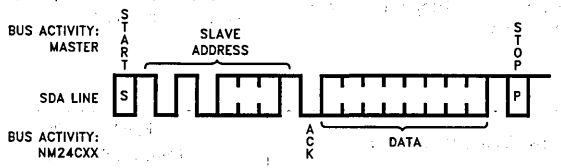


TL/D/11429–7

FIGURE 5. Sequential Read

3.1.3. Current Address Read

Internally the NM24Cxx devices contain an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address *n*, the next read operation would access data from address *n* + *1*, without the need for the master to transmit the 8-bit word address and then wait for the NM24Cxx acknowledge signal before transmitting the data. (See *Figure 6.*)



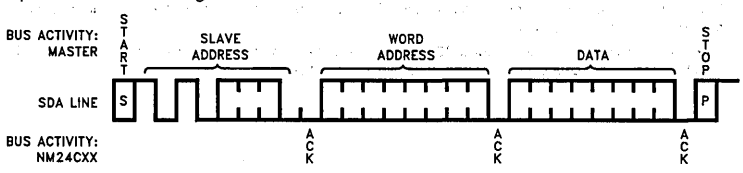
TL/D/11429–8

FIGURE 6. Current Address Read

Write Operations

3.1.4 Byte Write

The normal write sequence is shown in *Figure 7.*



TL/D/11429–9

FIGURE 7. Byte Write

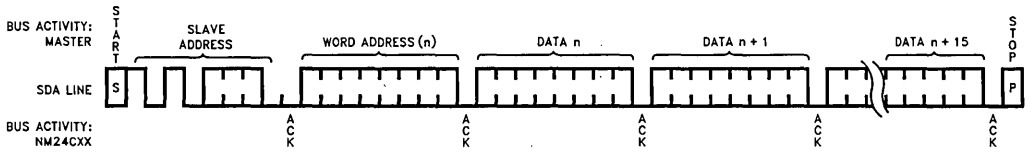
The master clocks the data into the NM24Cxx, and upon receipt of the ACK generates a STOP condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master.

All NM24Cxx EEPROMs have a Write cycle time of T_{wr} = 10 ms MAXIMUM for 5V systems.

3.1.5 Page Write

The NM24Cxx devices are capable of a sixteen byte page write. The master starts the operation in the same manner as the byte write but instead of terminating it continues to transmit up to fifteen more words. The internal address counter in the memory automatically increments to the next address. When the master has finished writing data to the memory, it terminates the write cycle in the usual way when an internal write cycle occurs in the memory.

This method results in a single T_{wr} delay instead of sixteen. This is useful for applications such as saving data after detecting a power failure when speed of writing is critical.



TL/D/11429–10

FIGURE 8. Page Write

3.1.6 Typical T_{wr} vs Maximum T_{wr}

Good design practice recommends using "worst-case" timing calculations rather than typical figures. After a master had initiated an internal write cycle in the memory there are two options before the next cycle can begin:

1. Master waits T_{wr} MAX = 10 ms
   — this ensures that all "worst-case" write cycles will be finished

   or

2. Master "polls" memory to detemine if the write cycle is complete T_{wr} TYP = 5 ms

With option 2 the master can start polling immediately after starting the internal memory write cycle as follows:

[STOP] → [START] → [SLAVE ADDRESS FOR WRITE OPERATION] → [POLL ACK]

IF no ACK then NM24Cxx still BUSY doing internal write
else NM24Cxx completed write cycle
master can proceed with next read or write operation.

This method can make significant improvements to overall system performance.

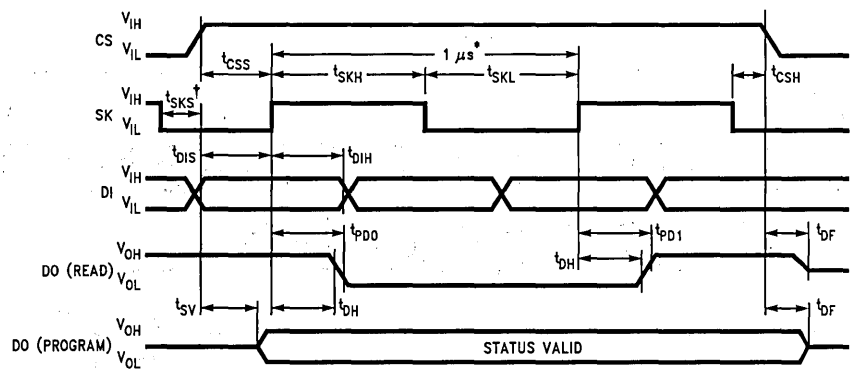
Note: After receiving a no acknowledge the master should output a stop condition to free the I²C-bus for other operations.

3.2 MICROWIRE Systems

3.2.1 Read Mode

A typical Read access is shown in *Figure 9*. The rising edge of CS is used to select and reset the EEPROM. Then the microcomputer clocks in the start bit and opcode for a read cycle using serial clock (SK) and Data In (DI pins). This is followed by the address where data is to be read from, after which the data is output via Data Out (DO) pin.

SYNCHRONOUS DATA TIMING



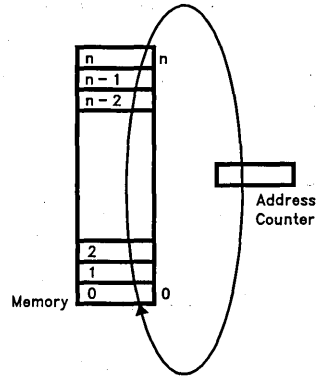
TL/D/11429–11

— Chip Select (CS) used to differentiate between various devices on bus.
— Rising edge of CS resets internal circuitry of EEPROM.
— Low-to-High transition of shift clock (SK) shifts all data in and out.
— CS brought low before next rising edge of SK to initiate self-timed programming cycle.

FIGURE 9. Read Mode

3.2.2. Sequential Read

All National's NM93CSxx devices support sequential read allowing the complete memory array to be read in a single operation.



TL/D/11429–12

CMOS: Sequential Read

Allows the user to obtain an endless loop of data simply by entering the read mode.

→ Reduces overhead

→ 50% faster read

Note: The NM93Cxx devices do NOT support sequential read.

FIGURE 10. Sequential Read

3.2.3 Write Mode

A write cycle is entered in a similar way to a read cycle; first the start bit and opcode for a write cycle are clocked in via DI, followed by the address and data to be written. The self timed programming cycle is initiated by bringing CS low before the next rising edge of SK as shown in *Figure 11.*

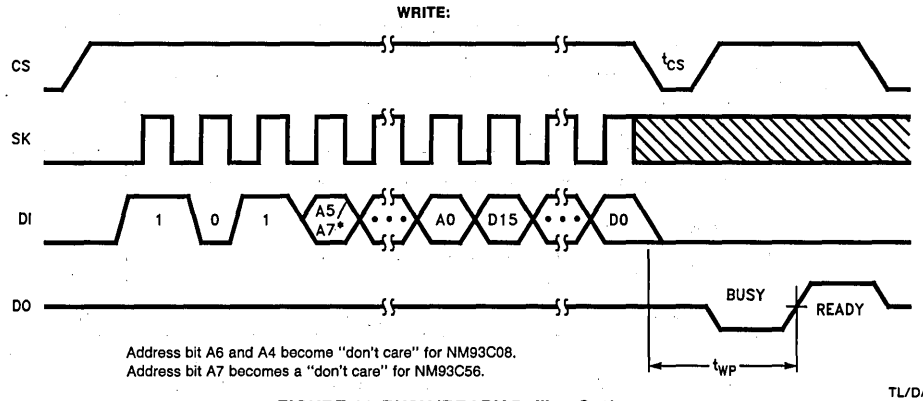
3.2.4 Typical T_{wp} vs Maximum T_{wp}

When the MICROWIRE EEPROMs the designer has three options to determine when the device has finished a programming cycle (either a write or erase instruction) as shown in *Figure 11.*

Option 1: μprocessor/μcontroller waits for $T_{wp(max)}$ = **10 ms**

Option 2: μprocessor/μcontroller polls Data-Out (DO) for Busy/Ready status $T_{wp(typ)}$ = **3 ms**

Option 3: if using the NM59C11 there is a separate RDY/BUSY pin: $T_{wp(typ)}$ = **3 ms**



TL/D/11429–13

FIGURE 11. BUSY/READY Polling Options

All MICROWIRE EEPROMs can use options 1 or 2, and in the case of the NM59C11 there is a separate RDY/BUSY pin which the microcontroller/microprocessor can poll to determine the programming status.

4.0 WRITE PROTECTED MEMORY

4.1 I²C EEPROMs

National Semiconductor manufactures two versions of I²C EEPROMs: a "standard" version (NM24C02/04/08/16) and a "secure" version (NM24C03/05/09/17). The "secure" devices are fully software compatible with the standard devices plus they use one of the unused pins to implement a hardware write protect for the upper half block of the memory array.

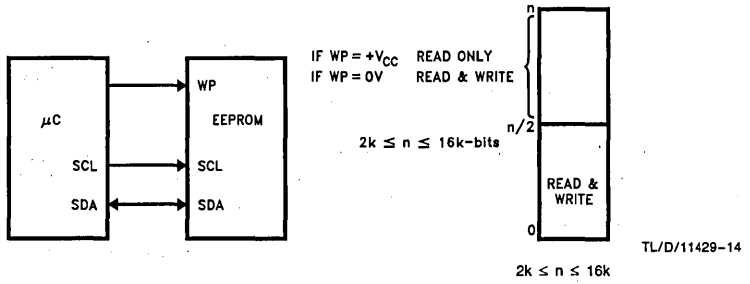


FIGURE 12. I²C Secure Memory System

If the master does attempt to write to the protected memory, then the NM24C03/05/09/17 will accept the slave and word addresses, but will not generate an ACK, thus the programming cycle will not be started when the STOP condition is asserted.

4.2 MICROWIRE EEPROMs

All NM93CSxx devices have the security feature which allows the user to define a portion of the memory to be write protected, either permanently or temporarily. This is useful for storing secure information in a system, such as calibration data. To control the secure memory involves a combination of setting a hardware pin and various software instructions as shown in *Figure 13*.

- — Protect Register:
  Input PRE must be high and PREN instruction executed before a write to protect register
- — Disable Cell:
  Set via PRDS instruction, input PRE must be high and PREN instruction executed
  PRDS is a one time only instruction
- — Address in register defines first location to be protected
- — Protect register may be altered unless PRDS is executed

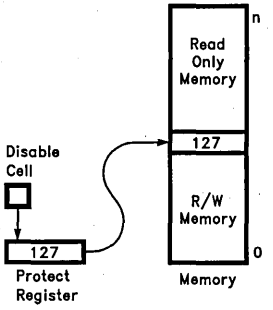
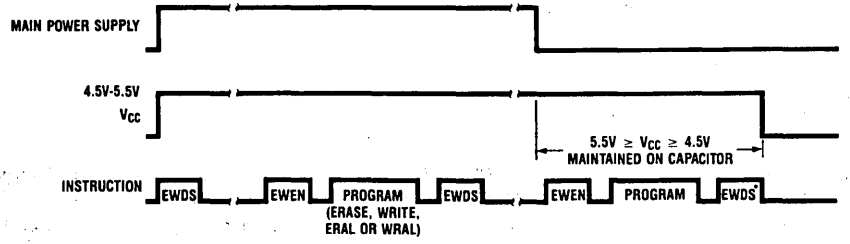


FIGURE 13. Memory Protect Register

Data in serial MICROWIRE EEPROMs is further protected from spurious write cycles (especially during power transitions) by including a program disable mode which will automatically abort any requested Erase or Write cycles. *Figure 14* shows the suggested instruction flow for maximum data integrity with National's MICROWIRE EEPROMs.



*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 14. Protecting Data in Serial EEPROMs

Typical Instruction flow for Maximum Data Protection

— Although EEPROM in non-volatile, the problem exists that stored data can be destroyed during power transitions.

— All National Semiconductor serial EEPROMs when initially powered up are in Program Disable Mode. In this mode it will abort any requested Erase or Write cycles.

5.0 EEPROM ENDURANCE AND SYSTEM LIFETIME

5.1 EEPROM Definitions

The two main specifications which determine the system reliability and lifetime of an EEPROM are Endurance and Data Retention.

Endurance: The number of data changes of an EEPROM before any bit fails to write correctly.

Data Retention: The ability of an EEPROM cell to retain charge once it has been programmed for extended periods under static or dynamic conditions of voltage or temperature.

Parameters which affect Endurance are:

- **Programming Duty Cycle and Waveform:** Although the NM93Cxx devices can have a F_{SK} (max) 1 MHz, it is important to make sure that the duty cycle is such that t_{SKH} (SK high time) and t_{SKL} (SK low time) have a minimum value of 250 ns.
- **Ambient Write Cycle Temperature:** The colder the operating temperature the better the endurance will be. For example 25°C vs 90°C will show approximately a 2:1 improvement.
- **Programming Time:** All National EEPROMs are self-timed and the programming time cannot be varied by the user, guaranteeing reliable system and lifetime performance.
- **Programming Voltage:** The lower the programming voltage V_{PP} the longer the required timing period T_{wp}. All National's EEPROMs operate from a single V_{CC} supply and have an on-board V_{PP} generator which is V_{CC} independent. This ensures that all National EEPROMs are both easy to use and highly reliable. The programming voltage cannot be varied by the user.

5.2 Read Cycles

Read cycles are non-destructive so all EEPROMs have the capability for an infinite number of reads.

5.3 Data Changes

With an EEPROM it is important to look at the endurance or number of write cycles the device can support. There are three types of write sequence to consider with EEPROM technology:

1) **Erase before Write**

As the names suggests, a memory location must be erased before it can be written to. A typical software flow for a write instruction is:

— send ERASE instruction to memory address *n*

— send WRITE instruction to memory address *n*

Disadvantages

— must perform 2 dedicated instructions

— slower system performance (2 instruction cycles, 2 T_{WP} delays)

— each write operation requires 2 data changes;
i.e., endurance specification is effectively halved

2) **Autoerase**

— send WRITE instruction

— EEPROM automatically performs ERASE instruction, then performs the WRITE operation

Disadvantages

— still need 2 data changes for each WRITE cycle, thus reducing system performance and halving endurance rating

3) **Direct Write**

— single WRITE instruction, no ERASE needed

— writes over existing memory contents

— eliminates ERASE cycles

Advantages

— single instruction, faster system performance

— single data change for each WRITE instruction

All National Semiconductor CMOS EEPROMs (both MICROWIRE and I²C) use Direct Write method giving the highest system performance, reliability and endurance characteristics of CMOS EEPROMs available on the market today.

When looking at EEPROM endurance specifications it is necessary to look more specifically at the number of data changes (ERASE & WRITE) per write cycle. National specifies 1 write cycle to be 2 data changes (to be consistent with other manufacturer's datasheets whose products are either Erase before Write or Auto Erase), so the figure of 500k Write cycles is actually equivalent to an endurance figure of 1 Million (10^6) data changes.

National Semiconductor produce full product qualification booklets giving process performance and reliability characteristics; for a copy contact your local National Sales representative.

6.0 CONCLUSION

National Semiconductor offer the widest range of serial EEPROMs covering two main industry standard serial interfaces;

MICROWIRE:
- e.g. NM93Cxx, NM93CSxx
- size: 256-bit → 4 kbit (16 kbit coming)

I^2C:
- e.g. NM24Cxx
- size: 2k → 16 kbits

All these EEPROMs offer the same high specifications of:

Endurance:	10^6 data changes
Direct Write:	no erase cycle required
Data Retention:	greater than 40 years
Self-Timed Write Cycle:	typical write cycle time 5 ms
Sequential Read:	NM93CSxx, NM24Cxx devices
Memory Protect:	NM93CSxx, NM24C03/05/09/17

These features make them easy to use, allowing the system designer to achieve high performance, highly reliable systems.

REFERENCES

National Semiconductor Memory Databook
National Semiconductor CMOS Logic Databook

Software for Interfacing the COP800 Family Microcontrollers to National's MICROWIRE™ EEPROMs

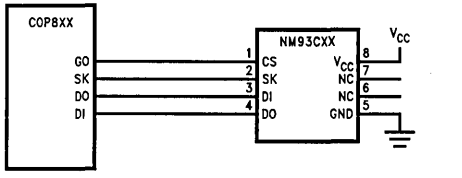
National Semiconductor
Application Note 841
Robert Stodieck

ABSTRACT

National's NM93Cxx and NM93CSxx family of serial EEPROMs have MICROWIRE "slave" interfaces that directly connect to the MICROWIRE "master" interfaces on the COP800 family of 8-bit microcontrollers. Peak data transfer rates are as high as 1 MB on the 4 wire MICROWIRE bus. This application note includes the essential assembly language software to address MICROWIRE EEPROMs.

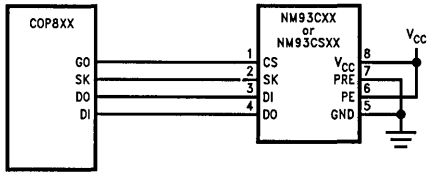
HARDWARE INTERFACE

A schematic for connecting a COP800 family microcontroller to one of Nationals NM93Cxx family MICROWIRE EEPROMs via the microcontrollers dedicated MICROWIRE port is shown in *Figure 1*. National makes two basic families of MICROWIRE EEPROMs, the classic NM93**C**xx series and the newer full featured NM93**CS**xx series. The NM93CSxx series EEPROMs have a sequential read capability and the "S" in "CS" stands for sequential (the "C" implies CMOS). As can be seen the "CS" series devices have two additional pins which control write protect features (consult a data sheet for information on their function). By connection these pins to V_{CC} and GND as shown in *Figure 2*, it becomes possible to use either "C" or "CS" family parts in the same physical socket. This would be desirable if a change from a "C" series part to a "CS" series part is possible for reasons of product upgrades or simply manufacturing inventory control. Pins 6 and 7 on the "C" series parts are true no connects and thus can be tied to V_{CC} or ground harmlessly.



TL/D/11491–1

FIGURE 1. Basic National MICROWIRE Interconnection to a COP800 Family Part



TL/D/11491–2

FIGURE 2. This schematic allows either a NM93Cxx or NM93CSxx part to be used in the same socket. Software can then be adjusted to take advantage of the "CS" series advantages without making changes to the board.

If it's desirable to use both types in the same socket without being forced to make software changes, one must be careful not to use the sequential read capability of the "CS" series. Both types of parts should be tested in the socket before the software is frozen.

NM93C06 to COP8XX Family Software Details

Always consult the latest data sheets for information about timing variables mentioned in the text that follows. These numbers were correct at the time that this application note was written but are subject to change.

1. The SK clock frequency must not exceed 1 MHz. Consult the processor data sheet for details.
2. The CS low time following a write must exceed 250 ns. This starts the internally timed write operation. The DO line will leave the high impedance state if CS goes high again and will drive low until the internal write cycle is complete. After DO returns high, indicating "ready" the first rising edge of SK with CS high and DI high will return the DO pin to the high impedance condition. This condition is normally the start bit of the next instruction.

   The DO pin will be low for up to 10 ms and then go high to indicate that the write is complete. If a new instruction is attempted before the DO pin returns high it will be ignored and the DO pin will not go tristate. The DO pin will always go to the tristate condition when CS is low.
3. Opcodes are either 2-bits or 4-bits long depending on the instruction type and are always preceded by a "start-bit" of a logic one. Any number of leading zeros can be clocked in before the start-bit (the sample assembly code inserts seven). Addresses are either 6 or 8-bits long depending on the density of the device. The combined opcode and address field is 8-bits for the smaller devices (93C06 and 93C46) and 10-bits for the larger devices (93C56 and 93C66). On the opcode types that do not use addresses, all of the "dummy" address bits must be clocked anyway (the combined opcode/address field is constant number of clock cycles).
4. On read operations the data out stream starts with a dummy zero. On NM93Cxx family EEPROMs, it is acceptable but not required to have extra clocks after the 16th actual data bit. On NM93CSxx family EEPROMs, extra clocks after the 16th actual data bit will begin to read the next data word.

Notes on the Assembly Code:

The subroutines that follow are adequate to quickly pilot the programmers task of addressing a serial EEPROM of the NM93Cxx family. Additional subroutines can very easily be adapted from these to handle the additional opcode types of the NM93CSxx series parts. Enough code has been included to allow the code to operate in a stand-alone fashion. However, when integrating the routines in to another program, initialization statements affecting global variables such as initializing the stack point or the X or B registers will need to be moved, deleted or replaced by statements in the main program.

The assembly code uses a software timer loop to time out the write time of the EEPROM. The programmer should be aware that it is possible to use the EEPROMs own internal timer to accomplish this task. This is done by monitoring the EEPROMs DO line after taking the EEPROMs CS line low to start a write and then setting CS high again to re-enable the DO output. The write is complete when the DO (of the EEPROM) drives high. Using the EEPROMs internal timer will allows the microcontroller time to accomplish some other task in the 10 ms that the write or erase operation requires. If the DO line is to be used to indicate that the write is complete, other MICROWIRE components on the bus must wait for the EEPROM writes to time out before being accessed (the DO line is in use).

The code was tested on a COP820 device via a Metalink In Circuit Emulator. The code should translate to other COP800 devices with little or no modification.

NM93C06 and NM93C46 Opcodes and Address Fields*

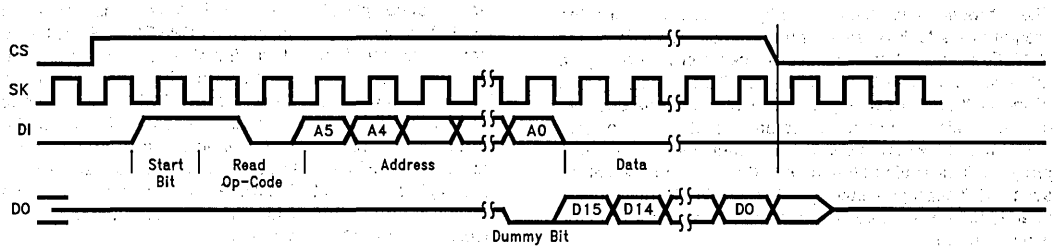
WREN	Write Enable	0	0	1	1	X	X	X	X
WRDI	Write Disable	0	0	0	0	X	X	X	X
ERAL	Erase All	0	0	1	0	X	X	X	X
WRAL	Write All	0	0	0	1	X	X	X	X
READ	Read	1	0	A5	A4	A3	A2	A1	A0
WRITE	Write	0	1	A5	A4	A3	A2	A1	A0

NM93C56 and NM93C66 Opcodes and Address Fields*

WREN	Write Enable	0	0	1	1	X	X	X	X	X	X
WRDI	Write Disable	0	0	0	0	X	X	X	X	X	X
ERAL	Erase All	0	0	1	0	X	X	X	X	X	X
WRAL	Write All	0	0	0	1	X	X	X	X	X	X
READ	Read	1	0	A7	A6	A5	A4	A3	A2	A1	A0
WRITE	Write	0	1	A7	A6	A5	A4	A3	A2	A1	A0

***Note:** All Opcode/Address Fields must be preceded with a leading "1" as a start-bit.

Read Cycle



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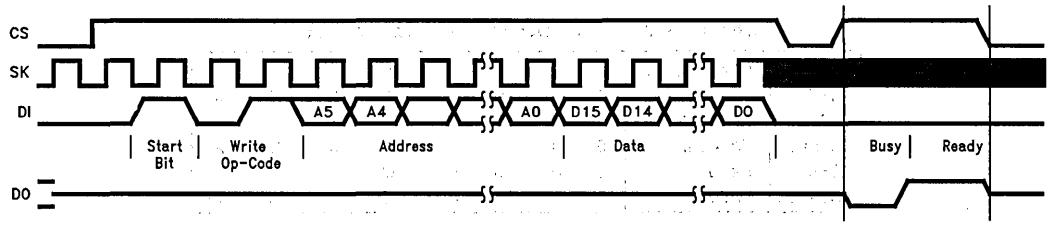
Write Cycle



TL/D/11491–4

FIGURE 3. Read and Write cycle waveforms. Notice that one leading zero is shown before the start-bit. The actual code inserts seven.

```
;*******************************************************
; THIS PROGRAM PROVIDES SUBROUTINES TO HANDLE COP820 OPERATIONS ON
; THE NM93C06 EEPROM I.E., WRITES, READS, ERASES, ENABLES AND DISABLES
;*******************************************************
;
 .INCLD COP820.INC
;Reserving RAM locations for key variables
 RDATL = 1   ;LOWER BYTE OF THE NM93C06 MEMORY DATA READ
 RDATH = 2   ;UPPER BYTE OF THE NM93C06 MEMORY DATA READ
 WDATL = 3   ;LOWER BYTE OF THE DATA TO BE WRITTEN TO NM93C06
 WDATH = 4   ;UPPER BYTE OF THE DATA TO BE WRITTEN TO NM93C06
 ADRESS = 5  ;THE LOWER 4-BITS OF THIS LOCATION CONTAINS THE ADDRESS
             ;OF THE NM93C06 MEMORY LOCATIONS TO BE READ/WRITTEN
             ;THE UPPER NIBBLE MUST BE ZEROS
 SNDBUF = 0  ;USED FOR THE COMMAND BYTE TO BE WRITTEN (Local Scratch Pad)
 DLYH = 0F0  ;LOCATIONS RESERVED FOR WRITE TIMEOUT VALUES
 DLYL = 0F1
 FLAGS = 6   ;USED FOR PROGRAM FLAGS (Local Scratch Pad)
             ;
             ;FLAG VALUE DEFINITIONS
             ;00         ERASE, ENABLE, DISABLE, ERASE ALL
             ;01         READ CONTENTS OF NM93C06 REGISTER
             ;03         WRITE TO NM93C06 REGISTER
             ;OTHERS     ILLEGAL COMBINATION
```

```
;THE INTERFACE BETWEEN THE COP820C/840C AND THE NM93C06 (256-BIT EEPROM)
;CONSISTS OF FOUR LINES. THE G0(CHIP SELECT LINE), G4(SERIAL OUT SO);
;G5(SERIAL CLOCK SK) AND G6(SERIAL IN SI).
;**************************************
;
;INITIALIZATION, MODIFY MOVE OR DELETE WHEN INTEGRATING INTO MAIN PROGRAM
                    ;USE ONLY IF SP WAS NOT PREVIOUSLY INITIALIZED
      LD  SP,#02F     ;INITIALIZE STACK POINTER
      LD  PORTGC,#031;SETUP G0, G4, G5 AS OUTPUT
      LD  PORTGD,#000;INITIALIZE G DATA REG TO ZERO
      LD  CNTRL,#008 ;ENABLE MSEL, SELECT MW RATE OF 2TC

      LD  X,#SIOR     ;SET THE X REGISTER TO POINT TO SIOR
      LD  B,#PSW      ;SET THE B REGISTER TO POINT TO PSW

;EXAMPLE SUBROUTINE CALLS ONLY, DO NOT INCLUDE IN FINAL CODE LOAD
;ADDRESS IN LOCATION "ADRESS" HIGH AND LOW BYTE TO BE WRITTEN INTO
;WDATH AND WDATL AND CALL THE SUBROUTINE,
      JSR EWEN
      JSR WRITE
      JSR EWDS
      JSR READ
DONE: JP  DONE

;THIS ROUTINE ERASES THE MEMORY LOCATION POINTED TO BY THE ADDRESS
;CONTAINED IN THE LOCATION "ADRESS". THE LOWER NIBBLE OF THE VALUE
;IN THE LOCATION "ADRESS" IS THE NM93C06 REGISTER ADDRESS. THE UPPER
;NIBBLE SHOULD BE SET TO ZERO.
;

ERASE: LD  A,ADRESS
       OR  A,#0C0
       X   A,SNDBUF
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE ENABLES PROGRAMMING THE NM93C06 (EWEN).
;
EWEN:  LD  SNDBUF,#030
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE DISABLES PROGRAMMING OF NM93C06.
;
EWDS:  LD  SNDBUF,#00
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE ERASES ALL REGISTERS OF NM93C06.
;
ERAL:  LD  SNDBUF,#020
       LD  FLAGS,#00
       JSR INIT
       RET
```

```
;
;THIS ROUTINE READS THE CONTENTS OF THE NM93C06 REGISTER. THE ADDRESS
;IS SPECIFIED IN THE LOWER NIBBLE OF LOCATION "ADRESS". THE UPPER
;NIBBLE SHOULD BE SET TO ZERO. THE 16-BIT CONTENTS OF NM93C06 REGISTER ARE
;STORED IN RDATL AND RDATH.
;
READ:  LD    A,ADRESS
       OR    A,#080
       X     A,SNDBUF
       LD    FLAGS,#01
       JSR   INIT
       RET
;
;THIS WRITES A 16-BIT VALUE STORED IN WDATL AND WDADTH TO THE EEPROM
;REGISTER WHOSE ADDRESS IS CONTAINED IN THE LOWER NIBBLE OF THE
;LOCATION "ADRESS". THE UPPER NIBBLE OF THE ADDRESS SHOULD BE SET TO ZERO.
;
WRITE: LD    A,ADRESS
       OR    A,#040
       X     A,SNDBUF
       LD    FLAGS,#03
       JSR   INIT
       RET
;
;THIS ROUTINE SENDS OUT THE START BIT AND COMMAND BYTE. IT ALSO
;DECIPHERS THE CONTENTS OF THE FLAG LOCATION AND MAKES A DECISION
;REGARDING WRITE, READ OR RETURN TO THE CALLING ROUTINE.
;
INIT:  SBIT  0,PORTGD     ;SET CHIP SELECT HIGH
       LD    SIOR,#001    ;LOAD SIOR WITH START BIT
       SBIT  BUSY,[B]     ;SEND OUT THE START BIT
PUNT1: IFBIT BUSY,[B]
       JP    PUNT1
       LD    A,SNDBUF
       X     A,[X]        ;LOAD SIOR WITH COMMAND BYTE
       SBIT  BUSY,[B]     ;SEND OUT COMMAND BYTE
PUNT2: IFBIT BUSY,[B]
       JP    PUNT2
       IFBIT 0,FLAGS      ;ANY FURTHER PROCESSING?
       JP    NOTDON       ;YES
       RBIT  0,PORTGD     ;NO, RESET CS AND RETURN
       RET
;
NOTDON:IFBIT 1,FLAGS      ;READ OR WRITE?
       JP    WR93C        ;JMP TO WRITE ROUTINE
       LD    SIOR,#000    ;NO READ NM93C06
       SBIT  BUSY,PSW     ;DUMMY CLOCK TO READ ZERO
       RBIT  BUSY,[B]
       SBIT  BUSY,[B]
PUNT3: IFBIT BUSY,[B]
       JP    PUNT3
       X     A,[X]
       SBIT  BUSY,[B]
       X     A,RDATH
```

```
PUNT4: IFBIT BUSY,[B]
       JP    PUNT4
       LD    A,[X]
       X     A,RDATL
       RBIT  0,PORTGD
       RET
WR93C: LD    A,WDATH
       X     A,[X]
       SBIT  BUSY,[B]
PUNT5: IFBIT BUSY,[B]
       JP    PUNT5
       LD    A,WDATL
       X     A,[X]
       SBIT  BUSY,[B]
PUNT6: IFBIT BUSY,[B]
       JP    PUNT6
       RBIT  0,PORTGD
       JSR   TOUT
       RET
;
;ROUTINE TO GENERATE DELAY FOR WRITE
;***************************************
;
TOUT:  LD    DLYH,#007    ;CHECK YOUR OSCILLATOR--PROCESSOR COMBINATION
                          ;TUNE FOR 10 MS DELAY
WAIT:  LD    DLYL,#OFF
WAIT1: DRSZ  DLYL
       JP    WAIT1
       DRSZ  DLYH
       JP    WAIT
       RET
       .END
```

Upgrade to National's Wide Voltage Range, Zero Standby Current EEPROMs

National Semiconductor
Application Note 870
Robert Stodieck

ABSTRACT

National's NM93C06L, NM93C46L, and NM93C56L EEPROMs and the new NM93C06/46/56LZ series devices operate across a 2.0V to 5.5V range suitable for unregulated battery powered operation. In addition, the new NM93C06/46/56LZ devices have ultra-low standby currents ideal for portable applications using very small batteries.

PERSONAL ELECTRONICS GAIN SOPHISTICATION

Many personal electronic items have moved from being perceived as trendy novelties to being viewed as mainstream personal or business appliances. Consumer familiarity, in turn, produces sophistication in the market for features. The ability to retain memory through battery changes and other types of power failure is highly desirable. Implementation of such sophisticated features requires RAM with battery back up or EEPROM memory.

Battery backed up RAM is usually far more expensive and functionally less attractive than EEPROM memory. Battery backed up RAM requires:

1. RAM
2. Battery holder
3. Battery
4. A door or other method to allow the battery to be replaced
5. New batteries to be located and replaced by the owner

EEPROM on the other hand requires:

1. EEPROM.

Serial EEPROM is invariably the cheapest and most compact solution for memory requirements up to 16 kbits.

CORDLESS PHONES

Memory dialing, noise reduction signal processing, and multi-channel operation with low noise channel selection capability, are now standard features for better quality cordless phones. Cordless phones are now moving to serial EEPROMs which can retain memory dial phone numbers and other parameters even through the inevitable dead battery and line power outage events.

Cordless phones have limited battery life. Memory dial data and other feature settings stored in RAM are subject to loss from dead batteries if implemented in the hand unit, or line power outages if maintained in the base unit. Reprogramming ten or more numbers for a memory dialer each time this happens is not desirable. Implementation of memory dialing and other features in the environment of a cordless phone requires RAM with a battery back up or EEPROM memory.

The length of time a phone can be left off its charger when not in use without the battery going dead is called standby. The cordless phone in standby normally leaves the radio receiver on to listen for incoming calls so that it can ring locally.

Standby and off hook time power consumption are dominated by the linear circuitry of the radio transmitter and receiver. Furthermore, the batteries in this application are relatively large and are frequently recharged. Thus, this application does not usually require the extremely low standby currents that can be achieved with the "LZ" series serial EEPROMs. But a broad range of V_{CC} voltages are encountered in this application. Most cordless phones use a stack of three Ni-Cad batteries for power. This produces a nominal voltage of 3.6V, but during charging this may go as high as 4.0V, and may drop into the 2.7V range in use. Some types of cordless phones use other battery technologies and battery counts. For example, stacks of 2 lead acid cells are also used producing a 4V nominal V_{CC}. The 2.0V to 5.5V V_{CC} range allowed by the "L" series of serial EEPROMs accommodates all the common V_{CC} ranges.

PAGERS

Paging units are a second example of high technology electronics gone blasé. Unlike cordless phones, pagers use regulated batteries for power and thus, do not need wide V_{CC} range EEPROMs. Since the batteries are small and power is a concern, low voltage operation is an advantage, as are very low standby currents used by the "LZ" series.

ELECTRONIC CAMERAS

All electronic cameras also make use of the NM93C46LZ and NM93C56LZ devices. This application generally uses regulated batteries to guarantee a constant 5V. But the batteries tend to be small and the camera spends much of its life on the shelf. Parameters stored in the electronic memory on these new cameras include shutter speed and focus calibrations that must never be lost in the life of the camera, and the frame counts and other details that change in service but which must not be lost when the battery dies.

The parameters connected with the many features found on these cameras are best retained in EEPROM. The small batteries and the long periods of inactivity involved require an EEPROM with very low standby currents to avoid running down the battery when not in use. With a standby current of less than 1 μA, the "LZ" series parts handle these applications with ease.

LEARNING REMOTE CONTROL UNITS

Alas, you have taught your new remote control unit to control the volume on your TV, it has mastered the slow advance on the video cassette recorder, it turns on and off the CD player, and your local soap opera is recorded daily

thanks to VCR Plus™ function. If the designer hasn't stored the critical information required in an EEPROM, one had better hope the battery never dies, or one will again become a slave to his "personal assistant" while retraining the beast. Owners of many first generation VCRs and televisions with digital random access tuners know the feeling well. Random access tuners allow their owners to skip over all the channels that could not be accessed in the area or that the owner simply did not like. But, if the power cord was even briefly disturbed or if the power went down, the tuner had to be retrained, a time consuming operation.

Both learning remote controls and digital tuners are more likely now to cure these problems by using EEPROM. TV and VCRs do not need low voltage, wide V_{CC} range, or low standby current parts, but the remote control units frequently do. The scenario is familiar:

1. Unregulated batteries are used.
2. The batteries are not large or frequently recharged.
3. The units spend relatively little time actually in use.
4. Long battery life is desirable.

Smart remote controls benefit from the wide V_{CC} range and low standby characteristics of the NM93C46LZ and NM93C56LZ serial EEPROMs.

SUMMARY

Serial EEPROMs offer by far the most compact and low cost non-volatile memory solutions for common consumer applications. The need for serial EEPROMs continues to grow with increasing consumer sophistication and growth of the personal electronics market. National's LZ products have wide operating voltage ranges and very low standby power and are particularly appropriate for battery powered applications of all types.

Interfacing the NM29N16 in a Microcontroller Environment

National Semiconductor
Application Note 910
Cliff Zitlaw
Rob Frizzell

INTRODUCTION

The NM29N16 is a 2Mbyte NAND Flash EEPROM memory that operates from a single 5V supply. This device does not have the parallel data, address, and control bus interfaces traditionally found on memory devices. The NM29N16 uses a byte wide serial interface with internal address, data, and control registers. The serial interface dramatically reduces the number of pins required to interface to the NM29N16. While the interface is nontraditional, it can easily be interfaced to standard microcontrollers. This application note describes how the NM29N16 can be interfaced to the Motorola 68HC11 microcontroller.

68HC11 INTERFACE

The NM29N16 can be interfaced to a microcontroller using the data bus, control bus, and a few I/O port bits. *Figure 1* shows the NM29N16 interfaced to a minimal 68HC11 system. The 68HC11 is configured in the expanded multiplexed mode which allows access to external memory devices. Most microcontrollers offer a mode that allows access to external memory and the NM29N16 should fit easily into all of these environments.

The I/Os of the NM29N16 were connected directly to the 68HC11 data bus. The NM29N16 occupies addresses C000H to DFFFH in the 68HC11 memory map due to the use of a three to eight (74HCT138) address decoder. While 8Kbytes of memory is taken in this design, the NM29N16 only requires a single address (C000H) out of that block. Due to timing constraints, the $\overline{RE}$ (Read Enable) and $\overline{WE}$ (Write Enable) signals must be ORed with the C000H address decode signal. $\overline{CE}$ (Chip Enable), CLE (Command Latch Enable), and ALE (Address Latch Enable) are controlled directly from three 68HC11 I/O port bits. The R/$\overline{B}$ (Ready/Busy) status output of the NM29N16 is polled by one I/O port bit.

A MAX707 μP supervisory chip is used to drive the $\overline{RESET}$ input of the 68HC11. The MAX707 forces its $\overline{RESET}$ output low until V_{CC} reaches 4.75V. Once V_{CC} exceeds 4.75V the $\overline{RESET}$ output remains low for an additional 200 ms before going high. This $\overline{RESET}$ output is also used to drive the $\overline{WP}$ (Write Protect) input of the NM29N16 to insure against inadvertent writes when V_{CC} is below 4.75V.

68HC11 TO NM29N16 COMMUNICATION

Information is transferred back and forth with a series of read and write operations that access the NM29N16 data, address and control registers. Loading the address register is accomplished by bringing $\overline{CE}$ low, ALE high and then loading data through the data bus with write operations to address C000H. Control register access is performed in a similar manner except that CLE is brought high instead of ALE. Data register access is performed when both ALE and CLE are low.

The EEPROM array in the NM29N16 is not directly accessible from the controller. An intermediate data register is used to transfer a page (264 bytes) of information back and forth between the EEPROM memory and the external controller. There are three basic forms of data transfers; erase operations that operate on a 16 page block, program operations that alter the contents of a single page, and read operations. During these three operations the R/$\overline{B}$ output goes low until the transfer or erase has completed.

A read operation is performed with a four step sequence. The command register is first loaded with the read instruction. The address register is then loaded with the page and byte address to access. At this point an internal recall operation is performed to transfer the contents of an EEPROM page to the 264 byte data register. After the recall has completed the accessed data is finally accessible by reading the contents of the data register. This is accomplished by pulsing $\overline{RE}$ low to read out sequential bytes.

Erase and program operations are performed similarly by accessing the data, control, and address registers. The simple access to these registers allow software routines that are as simple as that required to interface with a traditional parallel memory device.

SOFTWARE DRIVERS FOR A 68HC11 TO NM29N16 INTERFACE

A software listing is provided to demonstrate several features of the NM29N16. Different subroutines were developed that perform the basic read and write functions. These routines can be used with only minor modifications to interface the NM29N16 to any microcontroller.

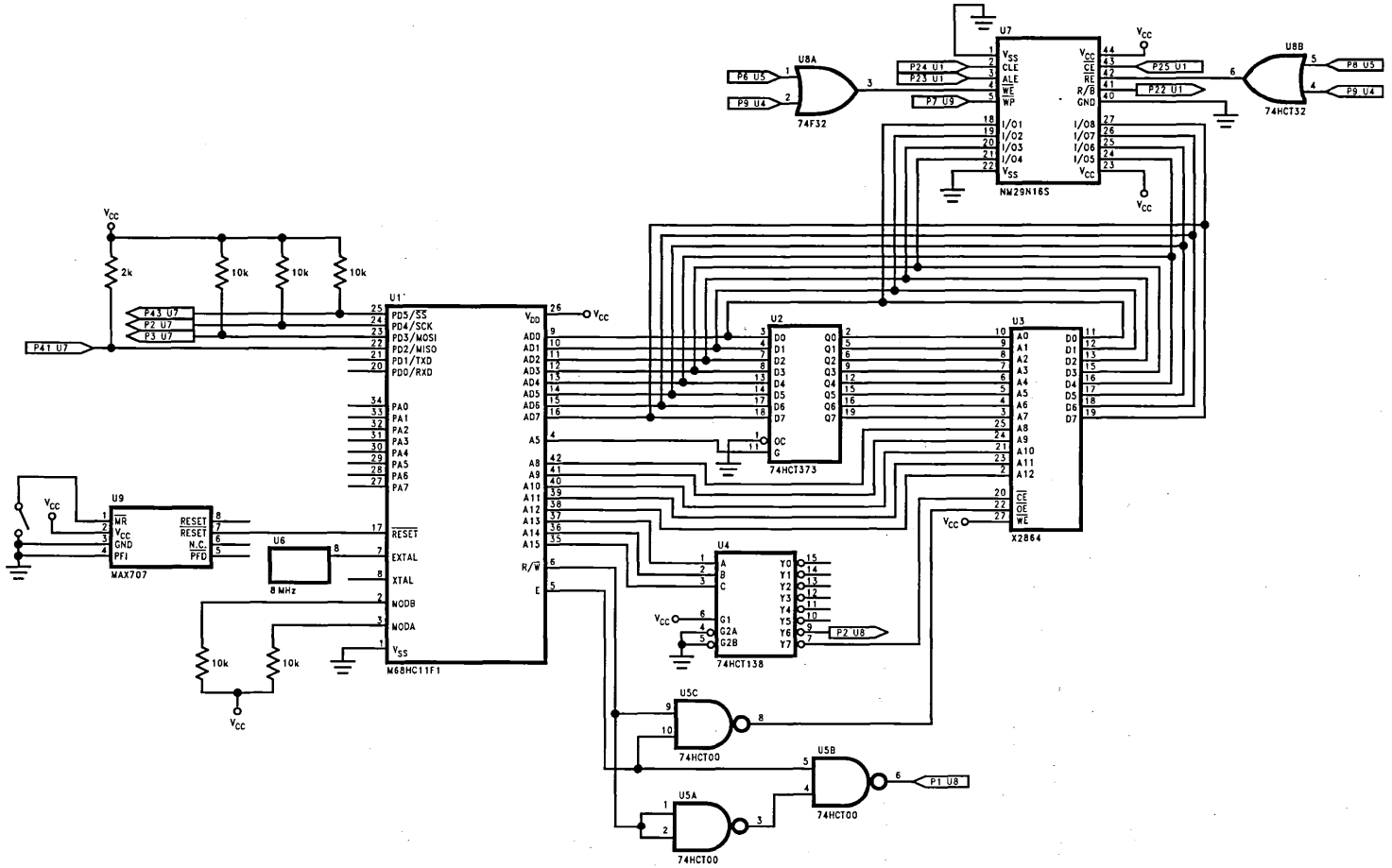


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FIGURE 1

```
*****************************************************************************
* This code was developed to demonstrate how the NM29N16 EEPROM can be      *
* interfaced to the MC68HC11 microcontroller.  The software includes        *
* several subroutines that perform various interface functions.  The        *
* subroutines include:                                                      *
*                                                                           *
*    RDPAG  : Read a page of information (264 bytes) out of the NM29N16     *
*    RDDAT1 : Read a byte from data memory                                  *
*    RDRED1 : Read a byte from redundancy memory                            *
*    PGMRED : Program a byte in redundancy memory                           *
*    PGMDAT : Program a byte in data memory                                 *
*    PGMPAG : Program an entire page (256 bytes data, 8 redundancy)         *
*    ERASE1 : Erase a block (16 pages)                                      *
*    STATUS : Read the Status Register                                      *
*    READID : Read the manufacturer code and the device code                *
*    INIT   : Tag blocks that are not fully functional                      *
*                                                                           *
* The 68HC11 interfaces to the NM29N16 by using the data bus, control       *
* bus, and a few I/O port lines.  The NM29N16 requires only one address    *
* location when configured in this manner.  The data bus is directly        *
* connected to the EEPROM.  Three I/O lines drive CLE, ALE, and CE.         *
* One I/O line is used to monitor the R/B output.                           *
*                                                                           *
* The mainline was used to test the functionality of the subroutines.       *
* The subroutines can be copied directly into a customer's program and      *
* be expected to operate as described.  The final mainline only             *
* performs a block erase and verify.                                        *
*****************************************************************************

****************************
* ADDRESS LOCATION EQUATES *
****************************

DDRD    EQU     $09                 port D direction register = $1009
PORTD   EQU     $08                 port D data register      = $1008
FLASH   EQU     $C000               NM29N16 = $C000 to $DFFF

************************
* BIT POSITION EQUATES *
************************

CEBIT   EQU     $20                 CE position in port D  = bit 5
CLEBIT  EQU     $10                 CLE position in port D = bit 4
ALEBIT  EQU     $08                 ALE position in port D = bit 3

****************************
* VARIABLE ADDRESS EQUATES *
****************************

HIPG    EQU     $0180               high order page pointer
LOPG    EQU     $0181               low order page pointer
ADD     EQU     $0182               byte pointer within a page
DATVAL  EQU     $0183               data transfer register
BLOCK   EQU     $0184
BLOCKL  EQU     $0185

****************
* RESET VECTOR *
****************
```

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```
        ORG     $FFFE                   reset vector to $E000
        FDB     $E000

*****************************
* PROGRAM STARTING LOCATION *
*****************************

        ORG     $E000                   program execution begins at $E000
BEGIN:  LDS     #$01FF                  initialize stack pointer
        LDX     #$1000                  initialize "address index register"
        LDAA    #$FF                    initialize I/O ports
        STAA    PORTD,X
        LDAA    #$3B
        STAA    DDRD,X
        BCLR    PORTD,X #CLEBIT
        BCLR    PORTD,X #ALEBIT         CE=1 CLE=0 ALE=0 initially

************
* MAINLINE *
************

        LDAA    #$00
        STAA    LOPG
        STAA    HIPG
        JSR     ERASE1
        JSR     STATUS

LOOP:   BRA     LOOP                    wait until reset loop

*************************************************************************
* RDPAGE copies a page from the NM29N16 into SRAM memory on the 68HC11.*
* All 264 bytes (data and redundancy) are copied into the SRAM buffer. *
* The page number to be transfered is passed in the variables LOPG and *
* HIPG.  The EEPROM data is copied into the 68HC11 SRAM between        *
* addresses 0000H and 0107H.                                           *
*************************************************************************

RDPAGE: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00
        STAA    FLASH                   load READ(1) instruction into
        BSET    PORTD,X #CEBIT           the command register
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00                    load the byte pointer in the address
        STAA    FLASH                    register with 00H (start of page)
        LDAA    LOPG
        STAA    FLASH                   load low order page number
        LDAA    HIPG
        STAA    FLASH                   load high order page number
        BCLR    PORTD,X #ALEBIT
        JSR     WAIT                    wait for recall into data register
        LDY     #$0000
NEXTR:  LDAA    FLASH                   read data from EEPROM and fill SRAM
        STAA    $00,Y                    buffer with data register contents
        INY
        CPY     #$0108                  loop until all 264 bytes have
        BNE     NEXTR                    been transfered
        BSET    PORTD,X #CEBIT
```

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```
        JSR     WAIT                    pause to assure EEPROM is idle
        RTS

*********************************************************************
* RDDAT1 and RDRED1 are used to read the contents of a single address *
* in the EEPROM array.  Data can be read from either the DATA portion *
* of the array (RDDAT1) or the REDUNDANT portion (RDRED1).  The       *
* location to be accessed is defined in the variables ADD, LOPG, and  *
* HIPAG.  LOPG and HIPG define the page to be accessed and ADD        *
* indicates a position within the page.  ADD can range between 0 and  *
* 255 for DATA accesses or between 0 and 7 for REDUNDANT accesses.    *
* The value in the chosen location is returned in the variable DATVAL.*
*********************************************************************

RDDAT1: LDAA    #$00                    READ(1) command
        BRA     RDJMP
RDRED1: LDAA    #$50                    READ(2) command
RDJMP:  BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        STAA    FLASH                   load appropriate READ command into
        BSET    PORTD,X #CEBIT           the command retister
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    ADD                     load the byte address into the
        STAA    FLASH                    address register
        LDAA    LOPG
        STAA    FLASH                   load the low order page number
        LDAA    HIPG
        STAA    FLASH                   load the high order page number
        BCLR    PORTD,X #ALEBIT
        JSR     WAIT                    wait for recall to data register
        LDAA    FLASH                   load the value from the chosen

        LDAA    FLASH

        STAA    DATVAL                   address and save the result in DATVAL
        BSET    PORTD,X #CEBIT
        JSR     WAIT                    pause until EEPROM is idle
        RTS

*********************************************************************
* PGMRED, PGMDAT, and PGMPAG are used to program either a single byte  *
* or an entire page.  During program operations the entire data register*
* must be loaded and then the contents transfered to an EEPROM page.   *
* EEPROM bits can only be flipped from a one (erased state) to a zero  *
* (programmed state) during a program operation.  To program a single  *
* byte the entire data register must be filled with FFH except for the *
* byte that is to be programmed.  During the programming cycle bits    *
* that are zero in the data register will force the corresponding bits *
* in the chosen page to the zero state, other bits will remain         *
* unchanged.                                                           *
*                                                                      *
* These routines use a SRAM data array located on the 68HC11 between   *
* address 0000H and 0107H.  This array is transfered byte for byte into *
* the NM29N16 data register during the data load portion of the        *
* programming cycle.  If single byte is to be altered the location     *
* in the SRAM array corresponding to the address to be programmed is   *
* loaded with the new data and all other addresses in the array are    *
* filled with FFH.                                                     *
```

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```
*                                                                     *
* The routines PGMRED and PGMDAT are used to program a single byte in *
* redundant or data memory respectively.  The data value to be updated *
* is contained in the variable DATVAL, the page number is contained in *
* PGLO and PGHI, and the byte position within the page is contained in *
* ADD.                                                                *
*                                                                     *
* The routine PGMPAG assumes that the SRAM array already has the data *
* that will be programmed into the EEPROM.  PGLO and PGHI contain the *
* page number to be programmed.                                       *
***********************************************************************

PGMRED: JSR     FILLFF                  fill SRAM array with FFH
        LDY     #$0100                  load Y with redundant memory offset
        BRA     PGMB
PGMDAT: JSR     FILLFF                  fill SRAM array with FFH
        LDY     #$0000                  load Y with data memory offset
PGMB:   LDAB    ADD                     data or redundant address to alter
        ABY                             calculate absolute address in page
        LDAA    DATVAL
        STAA    $00,Y                   write new data byte into SRAM array
PGMPAG: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$80                    load command register with
        STAA    FLASH                    data input command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        LDAA    #$00                    load address register with
        STAA    FLASH                    start of page
        LDAA    LOPG
        STAA    FLASH                   load low order page number
        LDAA    HIPG
        STAA    FLASH                   load high order page number
        BCLR    PORTD,X #ALEBIT
        LDY     #$0000
LOADB:  LDAA    $00,Y                   transfer data from SRAM array
        STAA    FLASH                    into the NM29N16 data register
        INY
        CPY     #$0108                  loop until all 264 bytes have
        BNE     LOADB                    been transfered
        BSET    PORTD,X #CLEBIT
        LDAA    #$10                    load command register with
        STAA    FLASH                    start program command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        JSR     WAIT                    pause to make sure EEPROM idle
        RTS

FILLFF: LDY     #$0000                  fill SRAM addresses 0000H to
        LDAA    #$FF                     0107H with FFH
LOOPF:  STAA    $00,Y
        INY
        CPY     #$0108
        BNE     LOOPF
        RTS

***********************************************************************
* ERASE1 performs an erase operation on a single block (16 pages).  The *
* block to be erased is specified in the variables LOPG and HIPG.  The  *
* lower 4 bits of LOPG are not used so that the least significant bit of*
```

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```
* the block number is the 5th bit of LOPG.  The block number is         *
* specified in LOPG (bits 4-7) and HIPG (bits 0-4).                     *
*************************************************************************

ERASE1: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$60                    load command register with
        STAA    FLASH                    block erase command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        LDAA    LOPG                    load low order block number
        STAA    FLASH                    (XXXX0123)
        LDAA    HIPG                    load high order block number
        STAA    FLASH                    (45678XXX)
        BCLR    PORTD,X #ALEBIT
        BSET    PORTD,X #CLEBIT
        LDAA    #$D0                    load command register with erase
        STAA    FLASH                    execution command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #CEBIT
        JSR     WAIT                    pause until EEPROM is idle
        RTS

*************************************************************************
* STATUS is used to read the NM29N16 status register.  This command can *
* be used after erase and program cycles to determine if the results    *
* were successfull.  The contents of the status register are returned in*
* the variable DATVAL.                                                  *
*************************************************************************

STATUS: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$70                    load command register with
        STAA    FLASH                    status read command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    FLASH                   read status register
        STAA    DATVAL                  save results
        BSET    PORTD,X #CEBIT
        RTS

*********************************************************************
* READID is used to read the NM29N16 device and manufacturer codes. *
* The manufacturer code is returned in the A register and the device*
* code is returned in the B register.                               *
*********************************************************************

READID: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$90                    load the command register with
        STAA    FLASH                    the ID read command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00                    load the address register with
        STAA    FLASH                    address 0
        BCLR    PORTD,X #ALEBIT
        LDAA    FLASH                   read the manufacturer code
```

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```
        LDAB    FLASH                   read the device code
        BSET    PORTD,X #CEBIT
        RTS

*********************************************************************
* WAIT is used to pause until the NM29N16 returns to the ready mode. *
* The routine polls the R/B (ready/busy) pin until it returns high.  *
*********************************************************************

WAIT:   LDAA    PORTD,X                 check bit 2 of port D (R/B line)
        ANDA    #$04
        CMPA    #$00
        BEQ     WAIT                    loop until R/B returns high
        RTS

*************************************************************************
* INIT is used to determine which blocks in the NM29N16 are usable.  The *
* sequence is as follows:                                                *
*                                                                        *
*  1      Start with block 0                                             *
*  2      Erase and verify block                                         *
*  3      Write $AA to each page in the block and verify                 *
*  4      Erase and verify block                                         *
*  5      Write $55 to each page in the block and verify                 *
*  6      Erase and verify block                                         *
*  7      If steps 1-5 were successful tag the good block with data $F0  *
*          in address 0 of the redundancy memory in page 0 of the block  *
*          just verified                                                 *
*  8      Step through all 512 blocks                                    *
*************************************************************************

INIT:   LDY     #$0000                  start with block 0
        STY     BLOCK
LOOP1:  LDY     BLOCK
        STY     HIPG
        JSR     ERASE1                  erase block
        JSR     STATUS                  see if erase was successful
        LDAA    DATVAL
        ANDA    #$01
        BEQ     NXTSTP                  jump to BADBLK if erase unsuccessful
        JMP     BADBLK
NXTSTP: LDAA    #$AA                    verify that $AA can be written
        JSR     FILLXX                   to all pages in the block
        LDY     BLOCK
        LDAB    #$0F                    start with page 15 and work down
        CLC                              to page 0
        ABY
        STY     HIPG
        LDAA    #$00
        STAA    ADD
LOOPAA: JSR     PGMPAG                  program page with $AA
        JSR     STATUS                  see if programming is successful
        LDAA    DATVAL
        ANDA    #$01
        BNE     BADBLK                  jump to BADBLK if bad page found
        LDAA    LOPG
        ANDA    #$0F                    loop until all pages have been
        BEQ     DONEAA                   tested
        DEC     LOPG                    step to next page in the block
        BRA     LOOPAA                   being verified
```

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```
DONEAA: JSR     ERASE1              erase block
        JSR     STATUS              see if erase was successful
        LDAA    DATVAL
        ANDA    #01
        BNE     BADBLK              jump to BADBLK if erase unsuccessful
        LDAA    #$55                verify that $55 can be written to
        JSR     FILLXX               all pages in the block
        LDY     BLOCK
        LDAB    #$0F                start with page 15
        CLC
        ABY
        STY     HIPG
        LDAA    #$00
        STAA    ADD
LOOP55: JSR     PGMPAG              program page with $55
        JSR     STATUS              see if programming is successful
        LDAA    DATVAL
        ANDA    #$01
        BNE     BADBLK              jump to BADBLK if bad page found
        LDAA    LOPG
        ANDA    #$0F                loop until all pages in block
        BEQ     DONE55               have been verified
        DEC     LOPG                step to next page
        BRA     LOOP55
DONE55: JSR     ERASE1              erase block
        JSR     STATUS              see if erase is successful
        LDAA    DATVAL              jump to DATVAL if bad block found
        ANDA    #01
        BNE     BADBLK              jump to BADBLK if erase unsuccessful
        LDAA    #$F0                tag good block by writing $F0 into
        STAA    DATVAL               byte 0, page 0 (redundancy memory)
        LDY     BLOCK                of the block just verified
        STY     HIPG
        LDAA    #$00
        STAA    ADD
        JSR     PGMRED
BADBLK: LDY     BLOCK               exit routine if all 512 blocks
        CPY     #$1FF0               have been tested
        BEQ     DONE
        CLC                         step to next block (16 pages)
        LDAB    #$10
        ABY
        STY     BLOCK
        JMP     LOOP1               go verify next block
DONE:   RTS

FILLXX: LDY     #$0000              fill SRAM addresses 0000H to
LOOPF2: STAA    $00,Y                0107H with value in A reg
        INY
        CPY     #$0108
        BNE     LOOPF2
        RTS
```

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SUMMARY

The NM29N16 provides an extremely flexible interface for many systems. By not utilizing address lines, the device gives designers the ability to incorporate multiple megabytes of memory without the use of an expensive processor or system bus. The application described here is only one example of this. With this architecture, the NM29N16 should enable new types of portable systems to be developed.

National Flash Memories— Hardware Design Guide

National Semiconductor
Application Note 921
P. Mohan Prasad

National offers two types of Flash Devices, namely NOR type and NAND type. The device densities ranging from 1 Mbit to 16 Mbit, suited for various kinds of applications like BIOS code storage, Solid state file storage, Image file storage, etc. Some of the devices also feature Auto program/erase operations which aid in elegant, compact programming code.

This note describes the various hardware considerations that a system designer has to consider when using National's Flash devices.

ORGANIZATION

1. DEVICE CONSIDERATIONS

   This section addresses the various issues like programming voltage (V_{PP}) generation and control, V_{CC} considerations, etc.

2. NOR DEVICES

   The NOR Flash device section covers the individual design considerations for the following Flash devices

   NM28F010: 1 Mbit, byte wide device.

   NM28F040: 4 Mbit, byte wide device.

   NM28F044: 4 Mbit, byte wide device.

3. NAND DEVICE

   This section covers NAND type NM29N16 device, which is a 16 Mbit, 5V only device ideally suited for large file storage type of applications, like Solid state Disk, PCMCIA based Memory cards, etc.

4. ICP (In-Circuit Programming)

   Finally, this note also discusses the In-Circuit Programming (ICP) in general, and the various types of ICP configurations available today.

1.0 DEVICE CONSIDERATIONS

V_{PP} Specifications: National's Flash devices have ±5% tolerance specification on the 12V level that is required for V_{PP}. This specification is guaranteed by most of the off-the-shelf industry standard power supplies. In fact the PC-AT® system power supply has a +5% and −4% tolerance specification on the +12V level.

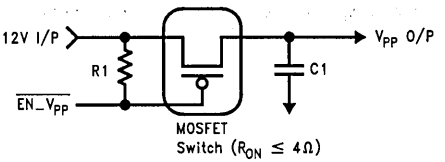

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FIGURE 1

The *Figure 1* represents a typical MOSFET Switch for the 12V line in the interface design towards Flash devices. MOSFET of the above configuration is available from a number of vendors, and MTD4P05 Motorola device is one good example. The only consideration is that the ON-RESISTANCE of the selected Switch should be low enough to keep the V_{PP} o/p within ±5% tolerance range.

The 12V V_{PP} programming voltage required for Programming/Erasing operations on the device is gated from the source (power supply's +12V TAP) through an enabling circuitry (e.g., a MOSFET Switch) to the Flash memory's V_{PP} pin. An enable signal from the system's control circuitry, say, "$\overline{V_{PP}\_EN}$" could then be used to switch ON/OFF the 12V path to the Flash memory's V_{PP} Pin.

Usage of this 12V Switch achieves two purposes:

1. Having the Switch turned off during power up ensures that V_{PP} voltage at the V_{PP} Pin of the device doesn't ramp up before the V_{CC} ramps to the required 5V level, which is a basic requirement for the Flash device.
2. In systems, especially laptop portables, having 12V supply enabled ON continuously is not a favourable choice in terms of the power drain of the Battery, since the need for 12V on the V_{PP} Pin is only during Programming/Erasing, etc. operations and not for the typical Read operation. Hence a Switch to turn on the 12V for V_{PP} only during the required limited times saves considerable power.

Additional Considerations: The *Figure 2* shows a typical circuit of a power control circuitry. This kind of a circuitry helps in improving the data integrity. The power sensing device in essence monitors the power supply's 5V output and

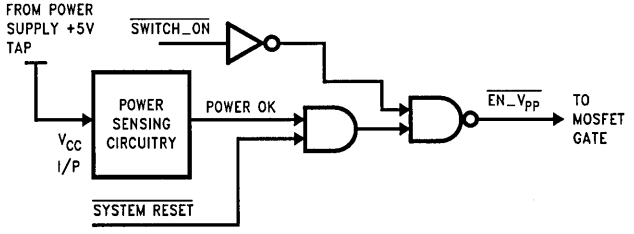

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FIGURE 2

asserts a "power OK" signal only when the input V_{CC} is within the tolerance limits. When the input V_{CC} levels cross the tolerance level, the "power OK" signal is deasserted (driven low) which in turn switches off the MOSFET switch and thus disabling the 12V from reaching the V_{PP} Pin anymore. System's reset signal is also coupled along with this "power OK" signal to take care of power_up and warm reset conditions. "Switch ON" signal is an output from system control circuitry which determines when to apply 12V at the V_{PP} pins of the Flash device under normal operations.

V_{PP} Generation: In the above discussion it is assumed that the 12V ±5% supply is readily available in the system, but for systems where this tolerance requirement is not met or when the 12V ±5% supply is not available at all from the system power supply there are ample V_{PP} Generation circuits available which generally employ one of the following techniques.

1. DC to DC conversion.
2. Regulation from a higher voltage (Down conversion).
3. Voltage boosters (5V to 12V).

A number of solutions employing the above mentioned techniques are available from National Semiconductor. Please refer to the listing given at the end of this note for the source.

V_{CC} Specifications: NSC Flash devices have a tolerance specification of ±5% on the 5V V_{CC} line. Though most of the available Power supplies have a ±5% tolerance specification on their +5V line, variation of this voltage within this tolerance range is dictated by the system loading and switching frequency of the devices at any given instant of time. Proper consideration should be given in choosing a matched Power supply in terms of the Power wattage against the total expected maximum load on the 5V line. Also adequate powerline decoupling especially around the memory devices and high speed switching devices should be ensured, which would take care of the V_{CC} droop caused by device switching to be within the tolerant limits.

Power Sequencing: To protect the device against any data corruption during Power cycling the following power sequencing is required.

Power On Condition: V_{PP} must be applied only after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high.

Power Off Condition: V_{PP} must be turned off after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high. V_{CC} can only be turned off after V_{PP} has reached 0V.

The sample circuit shown in *Figure 2* employing a power sensing unit inherently takes care of the Power-Sequencing required, without any additional logic.

2.0 NOR DEVICES

1. NM28F010 (128k x 8)

The following note describes the In-circuit programming aspects for a system using National's NM28F010 Flash memory device.

NM28F010 is a 1,048,576 bit Flash Electrically Erasable and Programmable Non-volatile memory device. It features single command for typical operations like READ, CHIP ERASE and PROGRAM allowing ease of use for in-circuit programming from within a system.

Software Considerations: The following two tables depict the various modes of NM28F010 Flash device operation and the command definitions to set to a particular mode.

Mode Selection Table

Mode		Signals							
		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Address	Data	V_{CC}	V_{PP}	Power
READ	Read	L	H	L	Read Address	Data Output	5V	0~V_{CC} or 12V	Active
	Output Deselect	L	*	H	*	High Impedance			
	Standby	H	*	*	*				Standby
COMMAND INPUT	$\overline{WE}$ Control	L	⊓	H	(Note 1)	Command Data	5V	12V	Active
	$\overline{CE}$ Control	⊓	L	H	(Note 1)	Command Data			
PROGRAM/ERASE		*	H	H	H				
PROGRAM/ERASE VERIFY		L	H	L	(Note 1)	Data Output			
ID READ		L	H	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer Command Definition Table

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Chip Erase	2	WRITE	*	20H	WRITE	*	20H
Erase Verify	2	WRITE	Byte Address	A0H	READ	*	EV Data
Program Setup/ Begin	2	WRITE	*	40H	WRITE	Byte Address	WR Data
Program Verify	2	WRITE	Byte Address	C0H	READ	*	WV Data
Reset	2	WRITE	*	FFH	WRITE	*	FFH

*H or L

Interface Block Diagram

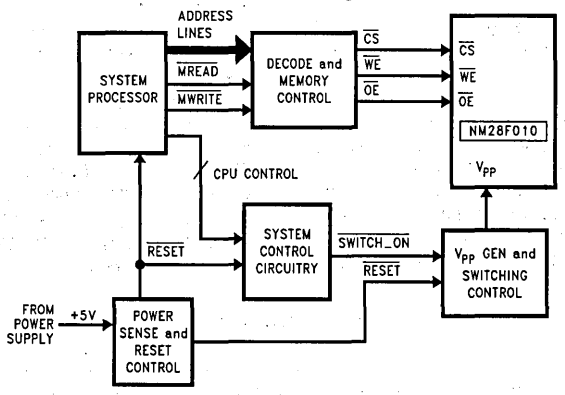

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FIGURE 3

Operating Modes: NM28F010 features seven modes of operation as shown in COMMAND DEFINITION TABLE. Setting the device to any particular mode is by writing an appropriate opcode to the Command register of the device. Note that the Command register by itself doesn't occupy any address range of the device and write to the Command register is enabled only when V_{PP} is at 12V level.

A detailed description of the various operating modes can be found in NM28F010 data sheets.

Figure 3 depicts a typical wiring diagram of control signals for a system using National's NM28F010 FLASH Memory with a block level specifications of the integral functional units discussed earlier.

Description: Interface to NM28F010 Flash memory is very much similar to that of conventional 27C010 EPROM except that the system's memory write enable $\overline{MWRITE}$ is also considered.

The DECODE and MEMORY CONTROL logic could be a simple combinatorial PAL®, like 16L8, which takes in the higher order address lines, memory read and memory write control signals as input and generates Flash memory chip select ($\overline{CS}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$).

2. NM28F040/NM28F044

NM28F040 and NM28F044 are 4,194,304 bit (512 x 8) CMOS Flash devices featuring single command for Read, Auto Chip erase, Auto Block erase and Auto Program/Verify allowing ease of use for in-circuit programming. NM28F040 is a 32 pin device whereas NM28F044 is a 44 pin device.

UNIQUE FEATURES

Block Mode Erase: These Flash devices can either be full chip erased or in terms of a specific block of 16 kbyte. This block mode erase feature allows ease of management of code blocks.

Auto Function: Both these devices feature a unique "AUTO-FINISH" facility for commands like Chip erase, Block erase and Program/Verify. Once after issuing any of the above commands to the device, all that is required is to sample the device data lines, D7 for operation completion (RDY/BUSY) and D4 for status of completion (FAIL/PASS). These devices have the necessary logic built-in inside the chip to do all of the iterative routines of the programming software. Looping through the same part of the code till operation proves to be a success or failure becomes unnecessary and all those iterative functions can now be removed from the code, resulting in a compact elegant programming algorithm.

Software Considerations: The following two tables outline the various operational modes and the command definition to set the various modes.

Mode Selection Table

Mode		Signals						
		$\overline{CE}$	$\overline{OE}$	Address	Data	V_{CC}	V_{PP}	Power
READ	Read	L	L	Read Address	Data Output	5V	0~V_{CC} or 12V	Active
	Output Deselect	L	H	*	High Impedance			
	Standby	H	*	*				Standby
COMMAND INPUT		⊓	H	(Note 1)	Command Data	5V	12V	Active
PROGRAM/ERASE		*	*	*				
PROGRAM/ERASE STATUS POLLING		L	L	*	DO~3,5,6:Z D4-fail/pass D7-rdy/busy			
ID READ		L	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer COMMAND DEFINITION TABLE

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Auto Byte Program	2	WRITE	*	10H	WRITE	Byte Address	WR Data
Auto Chip Erase	2	WRITE	*	30H	WRITE	*	30H
Auto Block Erase	2	WRITE	*	20H	WRITE	Block Address	D0H
Reset	2	WRITE	*	FFH	WRITE	*	FFH

Operating Modes: Both NM28F044 and NM28F040 feature same modes of operation, viz., Read, ID Read, Reset, Auto Byte Program, Auto Chip Erase and Auto Block Erase.

The Read, ID Read and Reset modes of operation of these two devices are the same as that of NM28F010, however the Program and Erase modes are significantly different from NM28F010.

A more detailed description of the various operating modes can be found in the relevant device data sheets.

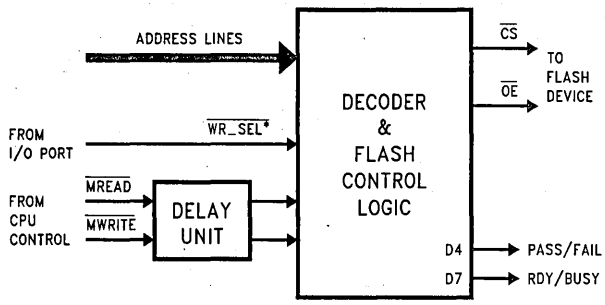
HARDWARE CONSIDERATIONS

1. NM28F044

Designing around NM28F044 is very much similar to NM28F010 which we discussed earlier, but with the following difference:

Two of the data lines, D7 and D4, signify the operation completion and status of completion respectively. Once after issuing any of the Auto Byte Program, Auto Chip Erase and Auto Block Erase commands to the device, all that is required is to do a read on the device after a specified time (depending on the command issued). A High (High logic level) on the data line D7 signifies that the operation for the issued command was completed. The data line stays at Low (Low logic level) if the operation is not completed yet. Similarly, when D7 has become high, a Low (Low logic level) on the D4 line signifies success of the operation and a High (High logic level) signifies failure.

2. NM28F040



(*"WR_SEL" signal could be same as "EN_V_{PP}" signal)

FIGURE 4

NM28F040 Flash device is different from NM28F044 Flash device in sense that it doesn't have a "$\overline{WE}$" signal. The "$\overline{CS}$" signal in this device acts as a multiplexed pin for both chip select (in the case of a read from the device) and write enable (in the case of a write to the device). Write mode is differentiated from the READ mode by the following conditions:

$\overline{CS}$	$\overline{OE}$	Operation on the Device
L	L	READ
*	H	WRITE

* → $\overline{CS}$ pulsing when $\overline{OE}$ is held high

But "$\overline{CS}$" signal continues to behave like a chip select signal (read mode) as long as V_{PP} voltage remains below V_{CC}, no matter whatever operation (READ or WRITE) is done on the device. *Figure 4* shows one possible way of interfacing NM28F040 Flash device in a system.

"$\overline{CS}$" Generation: The potential problem of chip select ($\overline{CS}$) signal glitching and thus leading to the possibilities of corrupting any valid data in the Flash device can be easily surmounted with simple logic. Data corruption chances are possible in NS28F040 Flash device only when 12V power is enabled to the V_{PP} pin of the device and then there is an extraneous cycle happening on the bus (bus cycle to a device other than the Flash device).

Memory decode designs in general incorporate a mechanism of gating the decoded signal (from the address bus) with Memory control signals ($\overline{MREAD}$ and $\overline{MWRITE}$) to generate a valid chip select to the memory. **Glitches become apparent when the total time for the address bus to get stabilized to valid logic levels (say, Tsb) and the time to decode the address lines (say, Td) is longer than the Memory control signal ($\overline{MREAD}$ or $\overline{MWRITE}$) driven valid delay (say, Tv).**

In systems where both the Address lines and the memory control signals are driven simultaneously this "glitching" scenario is inherent and one common way of eliminating the glitches in the output (chip select) signal is to delay the memory control signal by an amount greater than **Tsb + Td** and using this delayed signal for gating purpose. Simple DELAY LINE devices can be used to delay the control signals, as shown in *Figure 4*.

Processors like I80486, output Address, Memory control (M/IO) and Read Write (PW/R) control signals all at the same instant whenever an external cycle is started on the system bus. In this scenario, generating the chip select signal from address and M/IO and PW/R control signals all gated together would have the output chip select signal glitching for a period equal to the above mentioned **Tsb + Td.** But by using a delayed (by an amount **Tsb + Td)** memory READ/WRITE signal for final gating, chances for glitches in the chip select signal is eliminated.

"$\overline{WE}$_SEL" Signal: The "$\overline{WE}$_SEL" signal shown in *Figure 4* is a signal from one of the available general purpose I/O ports. This signal in most cases is the same as the "EN_V_{PP}" signal which was discussed earlier.

Prior to doing any write operation on the Flash device, the V_{PP} circuitry must be turned on so that V_{PP} voltage at the V_{PP} pin is 12V. "EN_V_{PP}" is a signal generated for this purpose. The same signal can be used in the $\overline{CS}$ generation logic to gate the decoded address signal with either of the memory control signals ($\overline{MREAD}$ and $\overline{MWRITE}$) which ever becomes valid during a particular Flash device access. The need for having to do this is due to the multiplexed nature of the chip select pin of the Flash device.

The following representative schematic *(Figure 5)* explains the above discussion.

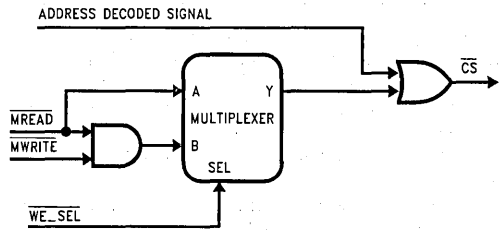


FIGURE 5

Common Considerations: In all the three Flash devices discussed so far, it is essential that proper command codes are entered in proper sequence. Inputting any command code other than those described could render an improper device functionality. Also accidental removal of V_{PP} supply during any Erase or Program operation in progress should be taken care of, for in some cases the valid data in the device could get corrupted. It's also essential to employ a POWER ON/OFF sequence as described earlier to safeguard the valid data against any corruption possibilities during power cycling.

3.0 NAND DEVICE

NM29N16 (2M x 8-Bit)

GENERAL DESCRIPTION

National's NM29N16 is 16.5 Mbit NAND Electrically Erasable and Programmable device. NM29N16 is a 5V only device, which does not require 12V for any of the Programming or Erase operations.

Organization: NM29N16 is organized as (256 + 8) bytes x 16 Pages x 512 Blocks. Programming is done in terms of a Page (264 Bytes each) while Erasing is done in terms of a Block or multiples of Blocks (16 Pages each). *Figure 6* depicts a conceptual organization of the Device.

NM29N16 is a byte_wide serial type of device in which the Address and Data are time multiplexed on the same I/O pins as there are no separate Address pins. Address in input as three bytes of Data during Address input cycles. The Program and Erase operations are handled automatically by the device, resulting in minimal Processor intervention and elegant programming code.

Additionally, the device aids in mapping out bad memory locations by providing an extra 8 bytes of redundant memory for every page in the device. This feature makes NM29N16 Flash device as an ideal candidate for SOLID STATE FILE STORAGE applications. Alternatively, this redundant 8 byte space per page can be used for normal storage resulting in extra capacity (16.5 Mbits instead of 16 Mbits).

Applications: NM29N16 is ideally suited for applications like,

1. Solid State File Storage
2. Voice Recording
3. Image File Storage, etc.

NM29N16 type of a device is the most sought after in Solid State File Storage where large data is stored and retrieved at a single access (Normally in terms of some specified Blocks Size). With the advent of PCMCIA based systems, Solid State Data Storage has become an intelligent form of Data storage and NM29N16 with its unique features is the ideal candidate for PCMCIA based Solid State Disk.

Device Specific Details: NM29N16 has the following control signals, whose combination, as depicted in the following truth table, signify the various operations that can be performed on the device. The control signals are **CLE** (command latch enable), **ALE** (address latch enable), $\overline{CE}$ (chip enable), $\overline{WE}$ (write enable), $\overline{RE}$ (read enable) and $\overline{WP}$ (write protect).

Truth Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⌇	H	X
Data Input	L	L	L	⌇	H	X
Address Input	L	H	L	⌇	H	X
Address Output	L	H	L	H	⌇	X
Serial Data Output	L	L	L	H	⌇	X
During Programming (BUSY)	X	X	X	X	X	H
During Erasing (BUSY)	X	X	X	X	X	H
Program/Erase Inhibit	X	X	X	X	X	L

H: V_{IH} L: V_{IL} X: V_{IL} or V_{IH}

Operating Modes: The device supports the following modes of operation, viz., Read Mode-1, Read Mode-2, Status Read, ID Read, Auto Page Program, Auto Block Erase, Auto Multi-Block Erase, Suspend/Resume and Reset.

The device is set into any of the above modes by writing an appropriate opcode into the device Command Register. Then if needed the Address and Data registers are updated. Thus programming the device for any mode of operation involves anything from one step to four step process, depending on the mode. Various Command codes (opcodes) needed for those above mentioned modes are listed in the Command Table.

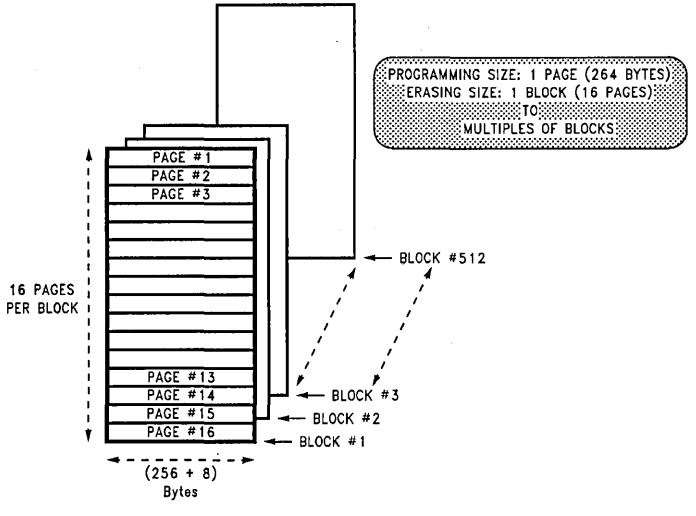


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FIGURE 6

Command Table

Modes of Operation	First Cycle (opcode)	Second Cycle #
Read Mode-1	00	
Read Mode-2	50	
Reset	FF	
Auto Program	80	10
Auto Block Erase	60	D0
Auto Multi Block Erase	60*	D0
Erase Suspend	B0	
Erase Resume	D0	
Status Read	70	
Register Read	E0	
ID Read	90	

Note: Second cycle shown above for the Program/Erase operations is a confirmatory cycle. The actual execution begins only after this command write. This feature is to safeguard against any inadvertent erasures, especially during Power Up.

*For Multi-Block erase operations, Command code (60) is repeated for every block to be erased. Typical sequence for a three block erasure would be, <OPCODE "60"> <Add of Block#1> <OPCODE "60"> <Add of Block #2> <OPCODE "60"> <Add of Block#3> <OPCODE "D0">.

DESCRIPTION OF OPERATIONS: There are basically two types of operations performed on the device, viz., READ and WRITE.

READ Type Operations: Read mode-1, Read mode-2, Status read, Register read and ID read are the operations which conform to Read type. For all these modes the appropriate command code is first written into the device Command register (first cycle). Then depending on the mode issued, address information is written into the Address register, which is essentially three write cycles following the Command input cycle. Then after a specified delay data is read off the Data register through a typical read cycle. Address information is not input for a Status Read operation. All these Registers, viz., Command, Data, Address and Status, do not occupy any of the device's memory location. They are indeed selected by the combination of logic levels of the control signals ALE and CLE. Note also that the Command Register cannot be read back for the contents.

The starting address is composed of 3 bytes, which are entered right after the command input in three successive write cycles. The format of the address is input as shown below:

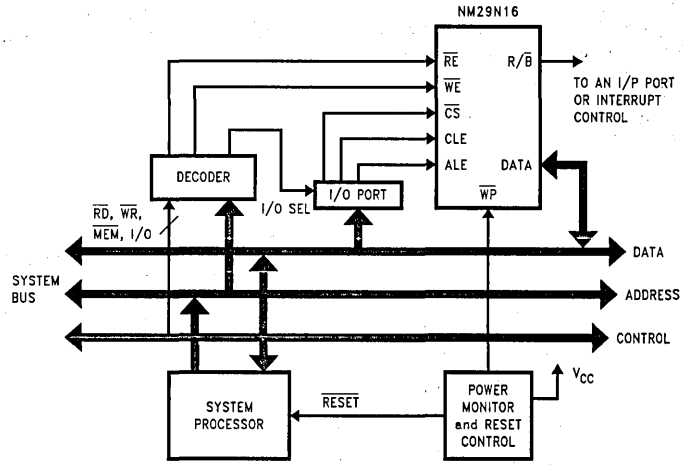
	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8
First Address Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Address Cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third Address Cycle	A16	A17	A18	A19	A20	L	L	L

Note: I/O bits 6, 7 and 8 should be set to low level during the third address cycle.

A12 to A20 form the Block address (selects one out of 512 Blocks).

A11 to A8 form the Page address (selects one out of 16 pages) within a selected Block.

A0 to A7 form the column address (selects the starting address of the data transfer within a page).



TL/D/11952–7

FIGURE 7

WRITE Type Operations: Operations like Program, Erase, Erase suspend, and Reset conform to Write type of command. Setting the device for these operating modes is similar to earlier described READ type operations. In these modes the device is updated with some new information.

A more detailed description of the various operating modes are found in the Device data sheets. Refer to the table given at the end of this note.

Hardware Interface: The *Figure 7* shows one of the methods of interfacing NM28N16 Flash device in a system. A generic Processor (Micro-controller) is assumed in this discussion. The external interface attributes (Bus Control Interface) of this generic processor is commonly found in almost all of the available Processors.

Types of Cycles: The cycle types that are typically performed on NM29N16 Flash device fall into three categories, viz., Command, Address and Data cycles. The following table explains the control signal configuration during these three cycles.

Cycle Types		CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$
Command	Input	H	L	L	⌇	H
Address	Input	L	H	L	⌇	H
	Output	L	H	L	H	⌇
Data	Input	L	L	L	⌇	H
	Output	L	L	L	H	⌇

The Input/Output cycles (in Address and Data cycles) are differentiated by $\overline{WE}$ and $\overline{RE}$ pulsing respectively with other being stable. In general all these three cycles happen either $\overline{RE}$ or $\overline{WE}$ pulsing during a stable window of the other control signals as shown in the above table.

I/O Port: Having an I/O Port type of interface is necessitated by the fact that the NM29N16 Flash Device control signals are not of the same type which are normally found in common Flash Devices. NM29N16 device is meant for large data storage applications (Memory cards, Solid state disk, etc.) where the device form factor is also crucial. In view of this, the device features an optimized Pinout, resulting in a compact device and yet with a much larger capacity. The control signals of this NM29N16 Flash device is not directly compatible to existing Micro-controller interface control. An I/O Port type of interface between this Flash device and any common Micro-controller normally considered for this type of an application, simplifies the interfacing task without any complex logic.

The I/O Port shown in the above diagram is any general purpose I/O port, normally found in a system. One such I/O port is availed to establish the key interface to the NM29N16 Flash device. Three control signals, viz., "$\overline{CS}$", "CLE" and "ALE" are driven by this I/O port as shown. Before doing an actual NM29N16 access, the system CPU initially writes to this I/O Port with the needed signal configuration for the type of the cycle (Command, Address or Data). Then a normal Read or Write cycle to the Flash device memory space would do an actual Read or Write cycle on the device.

Decoder: The decoder unit generates the Read/Write control signals for the Flash device. System address, memory control signals form the input to this unit. This unit could be a combination of discrete devices like 'LS139 or just a combinatorial $\overline{PAL}$ like 16L8 device.

Power Monitor: This unit basically monitors the V_{CC} power point for the required operating level. Whenever the system V_{CC} falls out of the ±5% tolerance range, this unit generates the system Reset as well as the write protect signal ($\overline{WP}$). This unit takes care of the POWERON condition also by keeping the system Reset and $\overline{WP}$ asserted till the system V_{CC} reaches the proper required level and thus protecting the data against corruption. Power monitor unit is available from numerous vendors in the form of a single device. One typical example of such a device would be Dallas Semiconductor component DS1231.

Ready/Busy Signal: This status output signal can be routed to an Input Port, which the CPU can keep polling for the status of operation completion or alternatively to the system's Interrupt control so as to generate an interrupt upon operation completion.

4.0 ICP (IN-CIRCUIT PROGRAMMING)

In-circuit programming (ICP) as opposed to device level programming is an efficient method of programming the most widely used programmable devices like, PROM, EPROM, PAL, PLD, Micro-controllers, FPGA, FLASH memory, etc. ICP is a means of programming these devices after they have been assembled into their target boards. There are broadly two categories of In-circuit programming, one being *Production oriented* and the other being *End user oriented.*

ICP Benefits: Obvious advantages of ICP over the traditional device-level programming are streamlined manufacturing flow, simplified handling, lesser inventory overheads and reduced production costs. ICP has become a preferred method of programming the device with the gaining usage of surface-mount devices (SMDs) and the Just-in-time production methods.

ICP Configurations: Different configurations are available today to achieve the programming of these devices in their target enclosure.

1. *Standalone In-circuit Programmers:* This is the Production oriented type of configuration and in this, the target (device assembled) board(s) get plugged on to slots assigned for programming purpose in the Standalone In-circuit Programmer, much like individual devices (ICs) getting plugged into the IC sockets of a Device Programmer. Then the relevant programming algorithm, resident in the In-circuit Programmer, is executed by the In-circuit Programmer to program the device with the proper data. A typical example of this kind of programmer would be DATA I/O's BoardSite. In this case the target boards usually have additional circuitry to isolate the programmable device(s) from the onboard's logic which is essential during the device programming. The level of complexity of this additional logic varies depending on the type of the device and the number of such devices.

This kind of configuration is well suited for production site programming where assembled boards are directly programmed for the devices present instead of programming the individual devices and house keeping them before assembly into a particular board.

2. *Programming via serial link:* In this configuration the target board has a serial link interface for the purpose of programming (or reprogramming) the device(s) on board. This target board is hooked to a conventional Device programmer via the serial interface, in which case the Device Programmer does the programming job as it would program an individual device.

Compared to the earlier discussed *Production type ICP*, this falls into *End-user type of ICP*, and this method eases the task of any code update at customer site without having to disassemble the target board from the system. But then a device programmer is required to be carried to the customer site to do any re-programming.

3. *In-System Programming:* In this configuration, typically a remote host downloads the software to be updated onto the target system through, say, a serial link. Then the target system executes the resident programming algorithm to program the mounted device. Instead of a serial link, a floppy diskette containing the updated code could be downloaded into the target system for programming purposes.

This approach of In-circuit Programming is preferred where frequent code change is involved, especially in customer field locations, where dismantling the whole system for device replacement purposes is not welcomed and it is not required to carry any device programmer to the customer site.

Flash Memory: An In-circuit Programmable device of particular concern here is a FLASH device which as byfar come in as a drop in replacement for the conventional EPROMs. Apart from delivering the "functional compatibilities", they feature a significant advantage over EPROMs in terms of Re-programming conveniences whenever a code_update is necessitated. Unlike EPROMs which have to be removed from the target board, Ultra-Violet erased, programmed with the new code and then plugged back into the target board, the FLASH devices are erased instantly and re-programmed with the new code all performed when the device is in the target board only, thus bringing all the benefits of ICP.

NAND FLASH Operation

National Semiconductor
Application Note 922
Rob Frizzell

INTRODUCTION

The NM29N16 is a 16Mb FLASH memory that utilizes the NAND architecture. The device incorporates a number of features that make it suitable for numerous portable applications that need large amounts of data storage but can not use a disk drive due to power or weight considerations. While making such systems possible, the NM29N16 also offers greater performance over disk drives in the area of data transfer time, program time, and endurance.

The following sections give a general overview of the NM29N16 and describe how it operates. The operation of the three basic functions: read, write and program, is gone over in detail followed by the physics behind the device operation.

GENERAL DESCRIPTION

The NM29N16 is a unique memory device that does not operate like normal EPROM or SRAM memory devices. All data that is read and written to the device is done in pages, which contain 264 bytes. Data is transferred from/to an on-chip buffer that stores the page. When the data is read out, it is read out sequentially, byte after byte, in order. This data transfer method allows the NM29N16 to not have any address pins which simplifies both board layout and the system interface. The device is easily interfaced to high end microprocessors and low end microcontrollers.

The NM29N16 is organized as 8192 pages of data with each page consisting of 264 bytes. *Figure 1* gives a three-dimensional view of how the device is organized. Each page allows for 256 bytes of data storage plus an additional 8 bytes that may be used for error correction or redundancy.

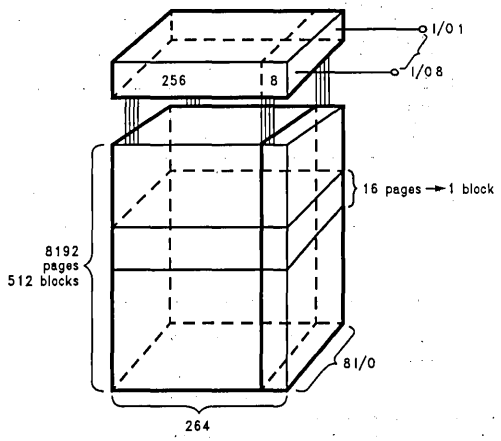


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FIGURE 1. NM29N16 Conceptual Layout

There are 16 pages to a block (512 blocks in a device). The block is the smallest unit which can be erased (4 kbytes).

Each block within the array consists of a chain of 16 NAND cells connected in series. *Figure 2* shows a typical cell.

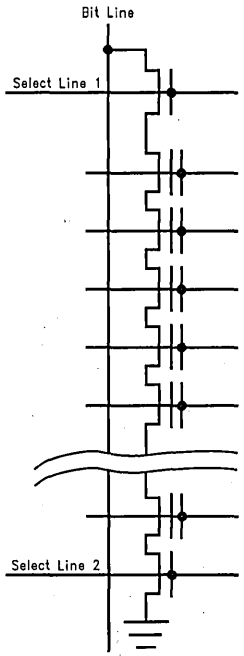

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FIGURE 2. NAND Cell Architecture

A block makes up the collection of 16 pages times the 264 bytes per page.

The NM29N16 is not read and written to like normal memory devices. There are no address or data pins for the NAND device as can be seen in Table I. There are only I/O pins,

TABLE I. Pinout of NM29N16

I/O1–8	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready/Busy
V_{CC}/V_{SS}	Power Supply/Ground

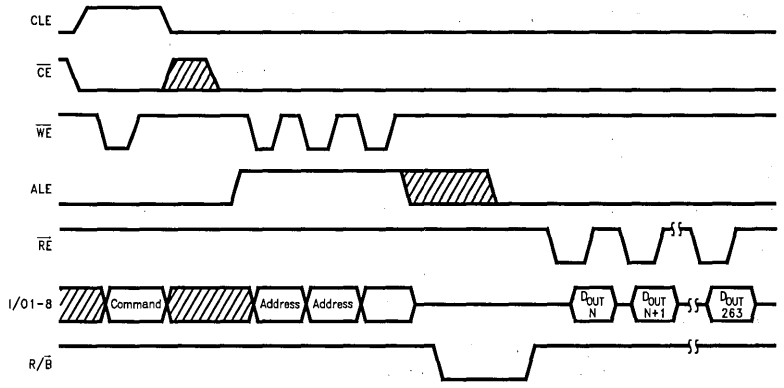

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FIGURE 3. General Timing Sequence

similar to peripheral ICs used in PC's before the advent of chip sets. Like the peripheral ICs, commands are sent to the NAND device to initialize it for the desired operation, be it a read, erase, or program. Address information follows the command to tell the device on which page or block the operation should take place. *Figure 3* shows the basic timing sequence of most operations.

In the following sections each of the main operations and their command sequence will be discussed.

READ

The NM29N16 offers a number of different Read modes. These enhance the ease with which the device may fit into numerous designs. Table II lists the different Read modes for the NM29N16 along with the other command modes. These will now be explained in detail.

The default mode of the NM29N16 is Read Mode 1. This mode uses the command 00H. A Read is initiated by writing the 00H command to the device followed by an address. The address tells the device what page to pull from the array and at what point within the page to set the pointer. On the rising edge of $\overline{WE}$, the page will be pulled out of the array and into an on-chip buffer. During this time the R/$\overline{B}$ pin goes low. This allows the system to do other operations while polling the R/$\overline{B}$ pin to return high. The time to pull the page from the array into the buffer is typically 25 μs. Once the page is stored in the buffer it can be read out sequentially. Sending consecutive $\overline{RE}$ pulses will read out sequential bytes of data starting at the byte set by the address inputted. For example, sending in address 05H-5FH-1FH would result in reading block 501 (1F5H), page 16(FH) starting at byte 6(05H) of 264 bytes. *Figure 4* graphically shows this example.

TABLE II. NM29N16 Command Modes

Mode	First Cycle	Second Cycle	Acceptable Command during Busy
Serial Data Input	80		
Read Mode (1)	00		
Read Mode (2)	50		
Reset	FF		Yes
Auto Program	10		
Auto Block Erase	60	D0	
Auto Multi Block Erase	60...60	D0	
Suspend in Erasing	B0		Yes
Resume	D0		
Status Read	70		Yes
Register Read	E0		
ID Read	90		

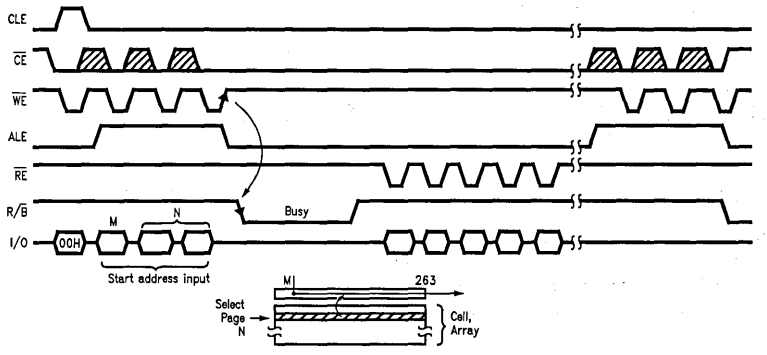

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FIGURE 4. Read Mode 1 Operation

The NM29N16 has a wraparound when the end of a page is met by a $\overline{RE}$ pulse. After reading out byte 263 and sending in another $\overline{RE}$ pulse, the device will pull the next consecutive page out of the array. Again, R/$\overline{B}$ will go low for approximately 25 μs until the next page is in the on-chip buffer. In this manner the entire device can be read out, page after page. *Figure 5* depicts this wraparound feature.

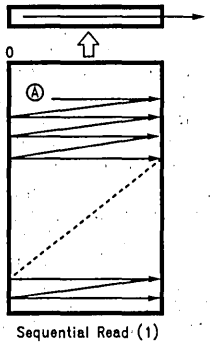

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FIGURE 5. Read Mode 1 Wraparound

Upon reaching the final byte in the final page, additional $\overline{RE}$ pulses will only read out the last byte over and over. In other words, the device will not wrap around to the first page of the array.

The NM29N16 provides eight additional bytes at the end of each page to be used for various functions. A special command, 50H, is used to read out only these last eight bytes from the page. This is achieved by writing the 50H command to the device followed by the three part address. The first byte determines the pointer location but in this case only the first three bits (I/O1–3) are recognized. The remaining bits (I/O4–8) are ignored. Again, the device will go through a 25 μs delay before the data can be read out with strobes of $\overline{RE}$.

The wraparound feature also works with the 50H command. However, instead of reading out all of the following pages, only the redundant eight bytes are read. *Figure 6* shows this action.

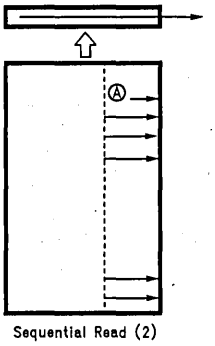

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FIGURE 6. Read Mode 2 Wraparound

A method of checking the status of the NM29N16 is provided via the 70H command. This command provides automatic program and erase verification. No software is needed to check each of the bytes individually to see if they have been programmed or erased properly. The 70H command offers the end user the ability to check if the program or erase operation was carried out successfully. This is accomplished after the R/$\overline{B}$ pin has returned high during a program/erase operation. By issuing the 70H command following R/$\overline{B}$ going high, the status of the device will be outputted on I/O1–8. *Figure 7* shows this operation for a page program operation.

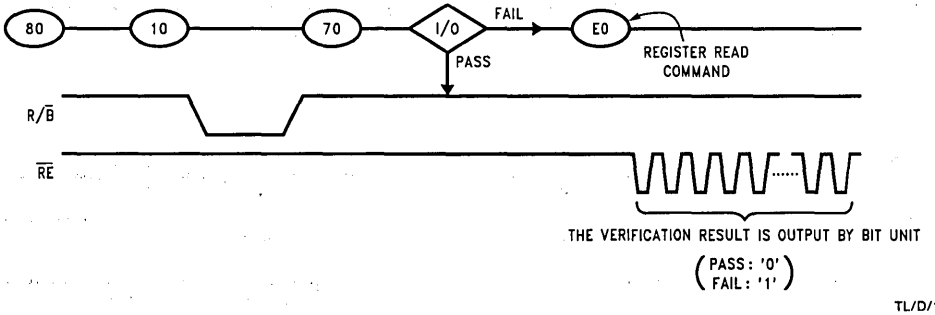

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FIGURE 7. Auto Page Program Verify

If I/O 1 is a "0", the operation was successful. If a "1" is outputted on I/O1, then the program or erase failed. If an erase failed, then the block that was erased should be mapped by the system as bad and should not be used again. If a page program fails, then the data should be written to another block and again the block should be mapped as bad by the system.

The Register Read command, E0H, allows the system to determine which bits did not program successfully. The E0H command is only used after a failed program attempt. This is done by writing the E0H command followed by consecutive $\overline{RE}$ pulses. A "0" outputted on I/O1 means the bit was programmed successfully while a "1" means the programmed bit failed. This information can be used for error correction to increase the accuracy of the data stored.

The final Read mode is the ID Read. Like all FLASH products, the NM29N16 offers a way to identify the manufacturer of the device and the type of device. This is accomplished by issuing the 90H command followed by the 00H address. This is a single address input, not a three part input like the other commands. Issuing two $\overline{RE}$ pulses will output the manufacture code (8FH for National Semiconductor) followed by the device code (64H for the 16 Mb NAND). *Figure 8* shows the timing sequence. Applications such as PCMCIA cards will use this data to identify the card and determine which driver to use for the interface.

PROGRAM

The NM29N16 implements an automatic programming algorithm which greatly simplifies the system software. The software for programming the device consists of writing three commands and the data. Programming must be done from the lowest page in the block to the highest. For example, page 16(1FH) in block 1 must be programmed before page 15(1EH) in block 1.

The program mode begins by issuing the 80H command to the device. This is followed by the three part address of the page and block. The data is then input sequentially starting with the lowest byte. The Program command, 10H, is then input to start the program operation. The R/$\overline{B}$ line will go low to signal the commencement of the programming as shown in *Figure 9*. Program time is typically around 300 μs.

Upon R/$\overline{B}$ going high a Status Read command, 70H, can be written to the device. This allows the system to verify if the program was a success or not. A "0" on I/O1 reports a successful program and a "1" on I/O1 means a failed program attempt. If the program does fail, the block should be mapped out as a bad block and not written to anymore. Also, the data that was in the on-chip buffer will be lost and will have to be rewritten into the buffer before programming it into a different block. *Figure 10* shows this sequence of commands.

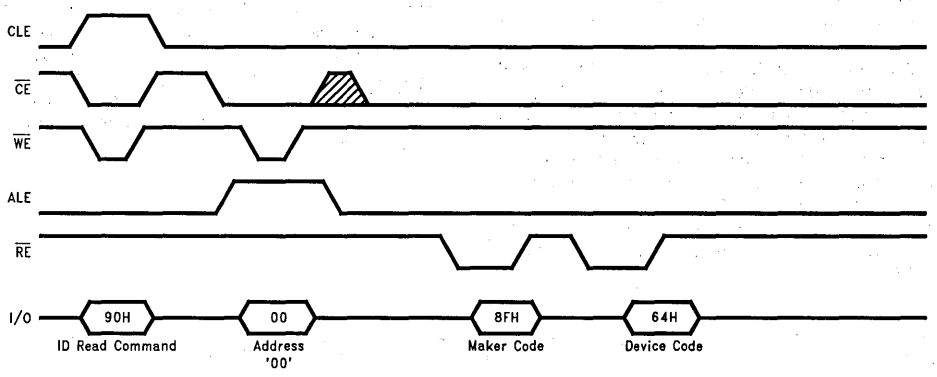

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FIGURE 8. ID Read Timing Sequence

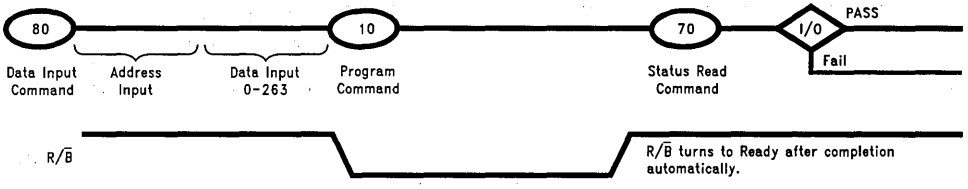

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FIGURE 9. Auto Page Program Sequence

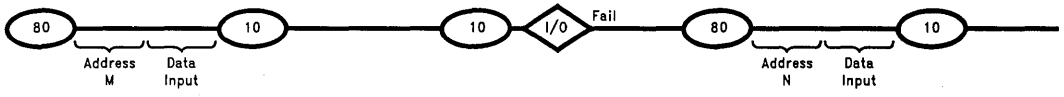

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FIGURE 10. Program Fail Sequence

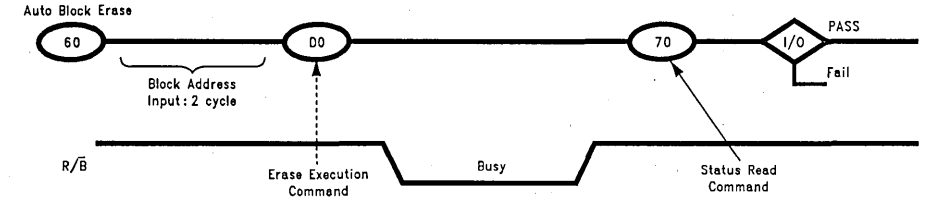

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FIGURE 11. Auto Block Erase Command Sequence

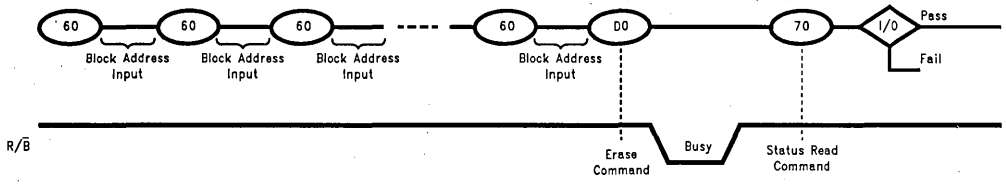

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FIGURE 12. Auto Multi-Block Erase Command Sequence

The NM29N16 allows data to be written to a page when there is less than 264 bytes. Up to 10 sections of the same page may be written to at different times. For example, the system may write 25 bytes to the first part of the page, call them D0–D24. The rest of the page of filled with "1" (FFH) and then programmed. A second 25 bytes can then be stored at D24–D49. Again the rest of the page is filled with "1" along with D0–D24. In this manner, the data that was previously programmed into D0–D24 is masked out from being reprogrammed. The benefit to the system designer is the ability to be able to store small amounts of data in a page and not to waste memory space.

Finally, the NM29N16 allows page to page transfers. However, when this is done the data that is reprogrammed into the new page is inverted ("0" → "1" and "1" → "0").

ERASE

The NM29N16 has two modes for block erasure. These are Auto Block Erase and Auto Multi-Block Erase. Two different commands are used in the erase procedure to prevent accidental erasure. These are 60H to set up the Auto Block Erase and D0H to execute the Erase command. The NM29N16 provides one of the smallest erase block sizes in the industry at 4 kbytes.

The Auto Block Erase, like the Program command, uses an algorithm to handle the entire erase procedure. This helps minimize the work load on the processor. The command sequence for a single block erase is shown in *Figure 11.*

It starts by writing the 60H command to the device followed by the two cycle address, which represents the block to be erased. The Erase Execution (D0H) command is then written to confirm the erasure. The R/$\overline{B}$ signal line will drop low for approximately 6 ms while the erase operation is in progress. When the R/$\overline{B}$ line returns high, the status of the erasure can be checked by issuing the Status Read (70H) command. If the erasure fails (I/O1 outputs "1") then the block should be marked as bad and no further operations should take place on this block.

The Auto Multi-Block Erase operation allows the system to mark multiple random blocks to be erased. A similar sequence as the single block erasure is followed as seen in *Figure 12.*

After the first address is inputted, it is followed by another 60H command and a second two cycle block address. This process can be repeated to mark as many blocks for erasure as is desired. When all the blocks have been marked the D0H command is finally inputted and the erasure commences (R/$\overline{B}$ goes low). The total erase time will be 6 ms plus 15 μs times the number of blocks that have been marked for erasure.

PHYSICS OF OPERATION

The NM29N16 utilizes a different architecture and programming method than the traditional NOR FLASH devices. The main difference in the programming method is the use of Fowler-Nordhiem tunneling for both programming and erasure of the cells. The physical operation behind reading, writing and erasing the NAND device at the cell level is explained in the following sections.

First an explanation of how Fowler-Nordhiem (F-N) tunneling operates is necessary. *Figure 13* shows a typical cross-section of a single NAND FLASH cell.

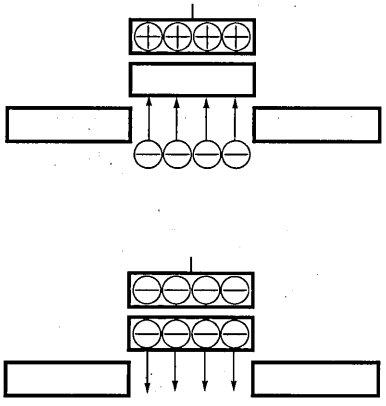

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FIGURE 13. NAND Cell Program/Erase

During program operation the substrate is grounded while the control gate is raised to V_{PP} (V_{PP} is approximately 20V). This pulls charges from the substrate, tunneling through the oxide to the floating gate where the charge is stored. During erasure the reverse operation is performed with the substrate at V_{PP} and the control gate grounded. This allows charge to tunnel through the oxide back into the substrate.

In contrast to NAND FLASH operation, NOR FLASH uses Hot-Electron Injection (HEI) for programming. In HEI, V_{PP} is applied to both the drain and the control gate while the source is grounded. In this case the charge is injected through the oxide and then collected by the floating gate as shown in *Figure 14.*

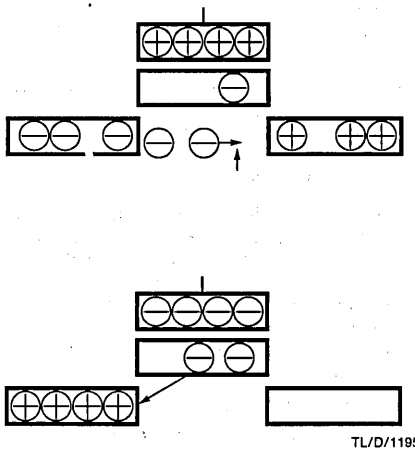

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FIGURE 14. NOR FLASH Cell Program/Erase

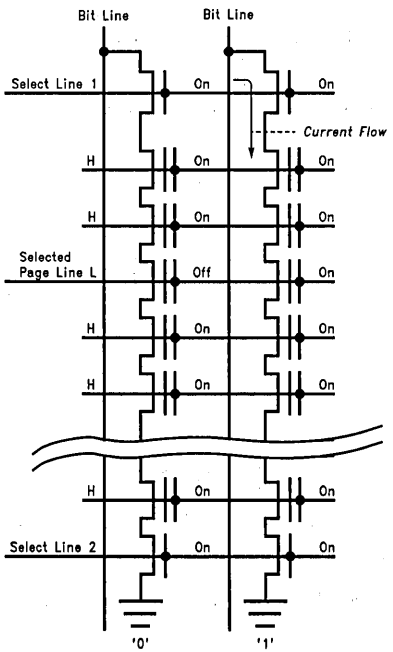

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FIGURE 15. NAND FLASH Read Operation

In this case, V_{PP} is typically on the order of 12V. The main disadvantage that HEI has versus F-N tunneling is that it requires more current to inject the electrons into the floating gate. Therefore it is easier to build NAND FLASH devices that use less power and a single power supply.

The read operation of the NAND cell is displayed in *Figure 15.* The first part of the read operation involves biasing of the page lines that are not selected along with select line 1 and 2. This way the 16 NAND cells are connected to ground and the bit line. The selected page line is biased at 0V. If the floating gate transistor cell is programmed "1", current is allowed to flow from the pre-charged bit line to ground. A cell that is programmed "0" does not allow current to flow and the bit line stays charged at the same level (thus the NAND name). Sense amps at the end of the bit line sense the voltage difference and reading out the data into the on-chip buffer.

The erase operation of the NAND cell is exhibited in *Figure 16.* In the erase operation an entire 4 kbyte block is

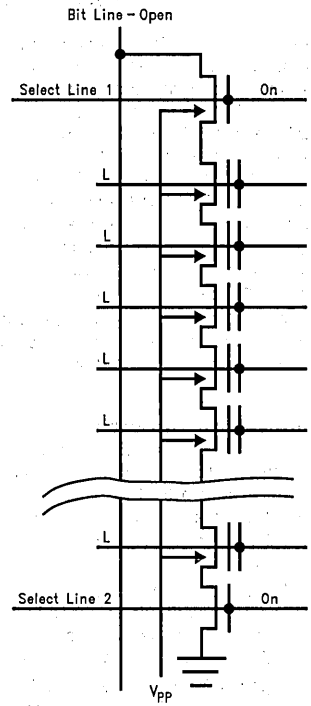

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FIGURE 16. NAND FLASH Erase Operation

erased at once. As shown in the diagram, all page select lines are set low while the substrate is set at V_{PP}. The bit line is left open and floats. Electrons tunnel from the floating gate to the substrate thus erasing the cells. An algorithm monitors that all cells in the block are adequately erased.

The NAND FLASH program operation also uses an algorithm to monitor the procedure. *Figure 17* shows the operation. First, select line 1 is turned on connecting the 16 NAND cells to the bit line while select line 2 is set low disconnecting the line from ground. Next, a high voltage (approximately 10V) is applied to all the page lines of the block except the page line that is to be programmed. The page line that is to be programmed is set at V_{PP} (approximately 20V). If data is to be programmed into the cell, the bit line is set low. This causes a differential of approximately 20V between the control gate and the substrate, allowing for tunneling into the floating gate. If the cell is not to be programmed, the bit line is set at approximately 10V. This causes the differential between the control gate and channel to be only 10V which is not enough to cause tunneling. Again the automatic program algorithm monitors the process for complete programming of the cells.

POTENTIAL APPLICATIONS

It should be clear from the above description of the NM29N16 that the device is very flexible in the manner in which it may be used. This makes it an ideal device for numerous applications that require large amounts of bulk data storage or secondary memory storage. Systems that need to store audio, visual or data files, and need to be portable are prime candidates to use NAND FLASH.

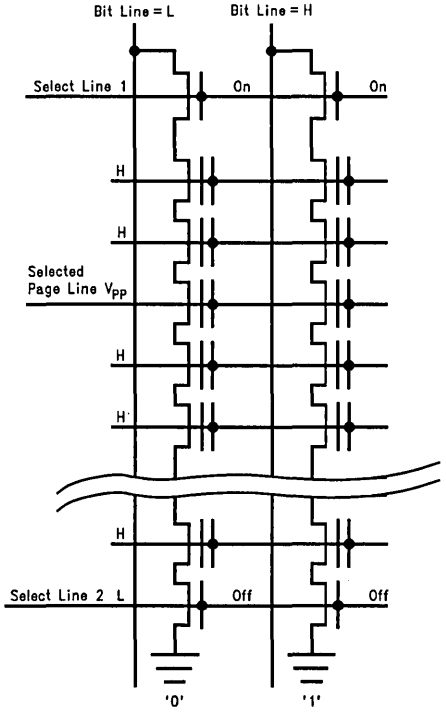

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FIGURE 17. NAND FLASH Program Operation

Section 5

Audio Interface Components

Section 5 Contents

National Semiconductor

LM4861 Boomer® Audio Power Amplifier Series
½W Audio Power Amplifier with Shutdown Mode

General Description

The LM4861 is a bridge-connected audio power amplifier capable of delivering 500 mW of continuous average power to an 8Ω load with less than 1% (THD+N) over the audio spectrum using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4861 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The LM4861 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4861 can be configured by external gain-setting resistors for differential gains of 1 to 10 without the use of external compensation components.

Key Specifications

- THD+N at 500 mW continuous average output power into 8Ω — 1% (max)
- Instantaneous peak output power — >1W
- Shutdown current — 0.6 μA (typ)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External Gain Configuration Capability

Applications

- Personal computers
- Portable consumer products
- Cellular phones
- Self-powered speakers
- Toys and games

Typical Application

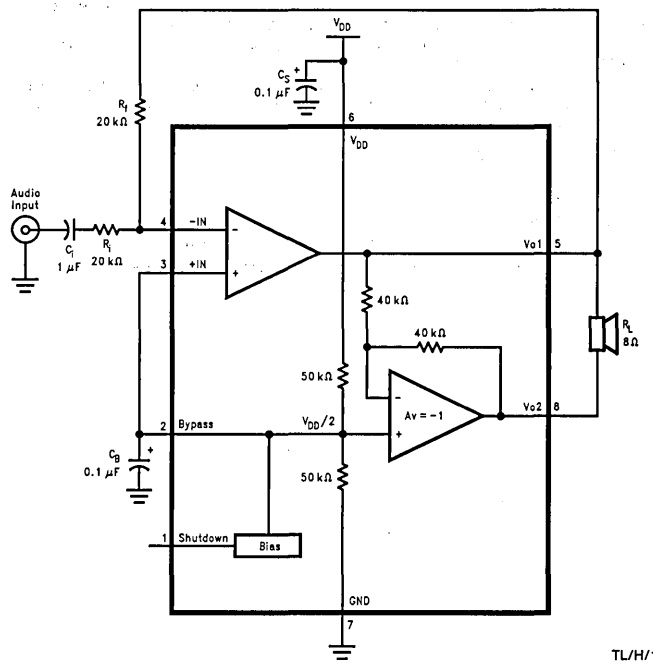

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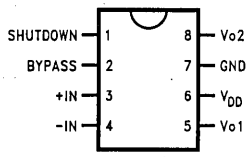
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



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Top View

Order Number LM4861M
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	3000V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150°C

Soldering Information

Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 *"Surface Mounting and their Effects on Product Reliability"* for other methods of soldering surface mount devices.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics (Notes 1, 2)

The following specifications apply for V_{DD} = 5V, R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4861		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage			2.7 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (Note 8)	6.5	10.0	mA (max)
I_{SD}	Shutdown Current	$V_{pin1} = V_{DD}$ (Note 9)	0.6		μA
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	50.0	mV (max)
P_O	Output Power	THD+N = 1% (max); f = 1 kHz		0.50	W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 500 mWrms; 20 Hz ≤ f ≤ 20 kHz	0.45		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V	65		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4861, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 170°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 9: Shutdown current has a wide distribution. For power management sensitive designs, contact your local National Semiconductor Sales Office.

High Gain Application Circuit

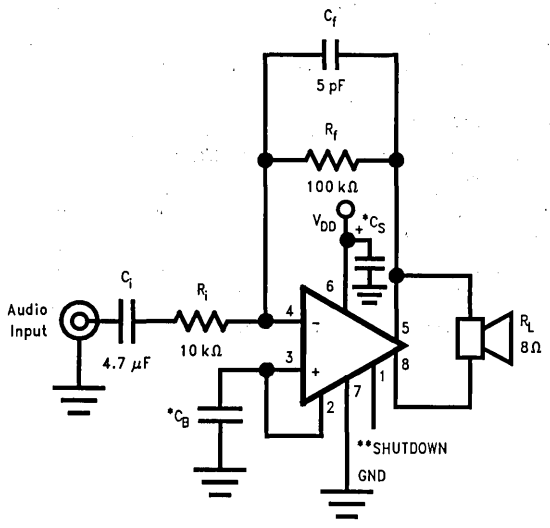


FIGURE 2. Audio Amplifier with $A_{VD} = 20$

Single Ended Application Circuit

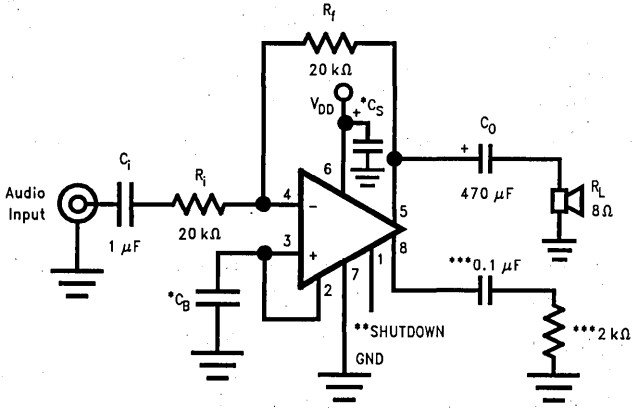


FIGURE 3. Single-Ended Amplifier with $A_V = -1$

*C_S and C_B size depend on specific application requirements and constraints. Typical values of C_S and C_B are 0.1 μF.

**Pin 1 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. This pin should not be left floating.

***These components create a "dummy" load for pin 8 for stability purposes.

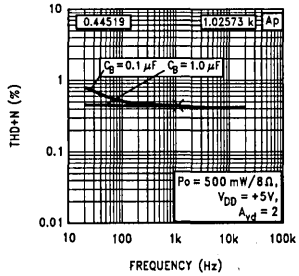
External Components Description *(Figures 1, 2)*

Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$.
3. R_f	Feedback resistance which sets closed-loop gain in conjunctien with R_i.
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half supply filtering. Refer to the **Application Information** section for proper placement and selection of bypass capacitor.
6. C_f*	Used when a differential gain of over 10 is desired. C_f in conjunction with R_f creates a low-pass filter which bandwidth limits the amplifier and prevents high frequency oscillation bursts. $f_C = 1/(2\pi R_f C_f)$

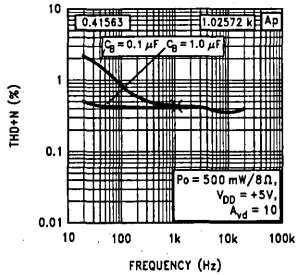
*Optional component dependent upon specific design requirements. Refer to the **Application Information** section for more information.

Typical Performance Characteristics

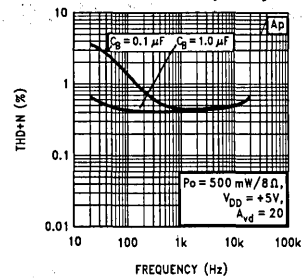
THD + N vs Frequency



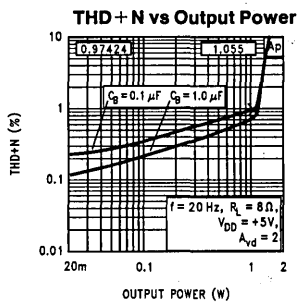
THD + N vs Frequency



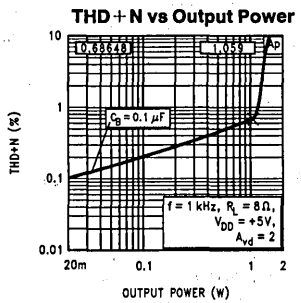
THD + N vs Frequency



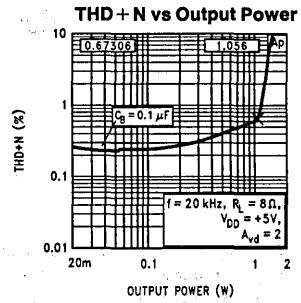
THD + N vs Output Power



THD + N vs Output Power



THD + N vs Output Power



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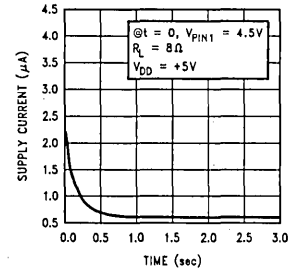
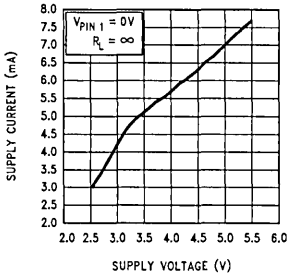
Typical Performance Characteristics (Continued)

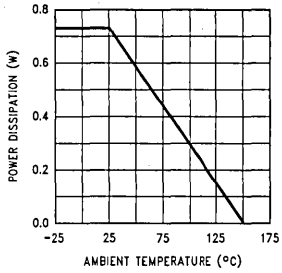
Supply Current vs Time in Shutdown Mode



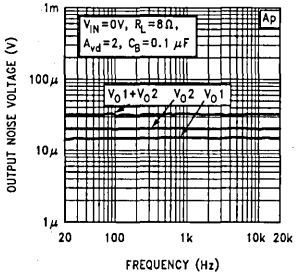
Supply Current vs Supply Voltage



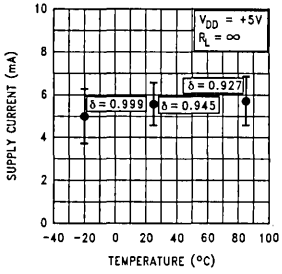
Power Derating Curve



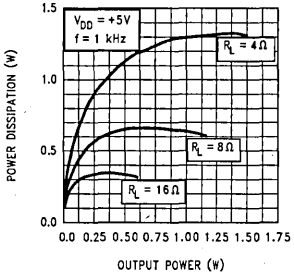
Noise Floor vs Frequency



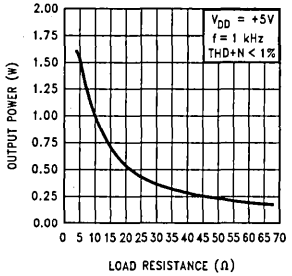
Supply Current Distribution vs Temperature



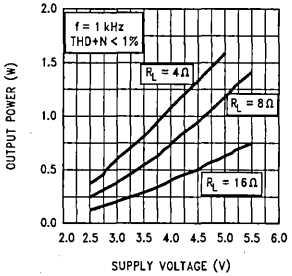
Power Dissipation vs Output Power



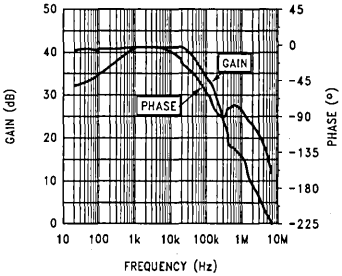
Output Power vs Load Resistance



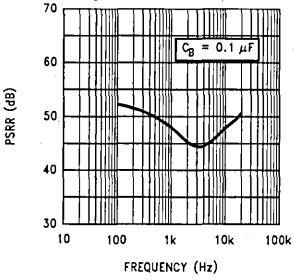
Output Power vs Supply Voltage



Open Loop Frequency Response



Power Supply Rejection Ratio



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Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4861 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 40 kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase 180°. Consequently, the differential gain for the IC is:

$$A_{vd} = 2 * (R_f/R_i)$$

By driving the load differentially through outputs V_{O1} and V_{O2}, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping which will damage high frequency transducers used in loudspeaker systems, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in Boomer Audio Power Amplifiers, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{O1} and V_{O2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor in a single supply, single-ended amplifier, the half-supply bias across the load would result in both increased internal IC power dissipation and also permanent loudspeaker damage. An output coupling capacitor forms a high pass filter with the load requiring that a large value such as 470 μF be used with an 8Ω load to preserve low frequency response. This combination does not produce a flat response down to 20 Hz, but does offer a compromise between printed circuit board size and system cost, versus low frequency response.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 1 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

Since the LM4861 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4861 does not require heatsinking. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625 mW. The maximum power dissipation point obtained from Equation 1 must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (2)$$

For the LM4861 surface mount package, θ_{JA} = 170°C/W and T_{JMAX} = 150°C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased or the load impedance increased. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 44°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the **Typical Performance Characteristics** section, the effect of a larger half supply bypass capacitor is improved low frequency THD + N due to increased half-supply stability. Typical applications employ a 5V regulator with 10 μF and a 0.1 μF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4861. The selection of bypass capacitors, especially C_B, is thus dependant upon desired low frequency THD + N, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4861 contains a shutdown pin to externally turn off the amplifier's bias circuitry. The shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. Upon going into shutdown, the output is immediately disconnected from the speaker. There is a built-in threshold which produces a drop in quiescent current to 500 μA typically. For a 5V power supply, this threshold occurs when 2V-3V is applied to the shutdown pin. A typical quiescent current of 0.6 μA results when the supply voltage is applied to the shutdown pin. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch that when closed, is connected to ground and enables the amplifier. If the switch is open, then a soft pull-up resistor of 47 kΩ will disable the LM4861. There are no soft pull-down resistors inside the LM4861, so a definite shutdown pin voltage must be applied externally, or the internal logic gate will be left floating which could disable the amplifier unexpectedly.

Application Information (Continued)

HIGHER GAIN AUDIO AMPLIFIER

The LM4861 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, then a feedback capacitor is needed, as shown in *Figure 2*, to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates unwanted high frequency oscillations. Care should be taken when calculating the −3 dB frequency in that an incorrect combination of R_f and C_f will cause rolloff before 20 kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_f = 100 kΩ and C_f = 5 pF. These components result in a −3 dB point of approximately 320 kHz. Once the differential gain of the amplifier has been calculated, a choice of R_f will result, and C_f can then be calculated from the formula stated in the **External Components Description** section.

VOICE-BAND AUDIO AMPLIFIER

Many applications, such as telephony, only require a voice-band frequency response. Such an application usually requires a flat frequency response from 300 Hz to 3.5 kHz. By adjusting the component values of *Figure 2*, this common application requirement can be implemented. The combination of R_i and C_i form a highpass filter while R_f and C_f form a lowpass filter. Using the typical voice-band frequency range, with a passband differential gain of approximately 100, the following values of R_i, C_i, R_f, and C_f follow from the equations stated in the **External Components Description** section.

R_i = 10 kΩ, R_f = 510k ,C_i = 0.22 µF, and C_f = 15 pF

Five times away from a −3 dB point is 0.17 dB down from the flatband response. With this selection of components, the resulting −3 dB points, f_L and f_H, are 72 Hz and 20 kHz, respectively, resulting in a flatband frequency response of better than ±0.25 dB with a rolloff of 6 dB/octave outside of the passband. If a steeper rolloff is required, other common bandpass filtering techniques can be used to achieve higher order filters.

SINGLE-ENDED AUDIO AMPLIFIER

Although the typical application for the LM4861 is a bridged monoaural amp, it can also be used to drive a load single-endedly in applications, such as PC cards, which require that one side of the load is tied to ground. *Figure 3* shows a common single-ended application, where V_{O1} is used to drive the speaker. This output is coupled through a 470 µF capacitor, which blocks the half-supply DC bias that exists in all single-supply amplifier configurations. This capacitor, designated C_O in *Figure 3*, in conjunction with R_L, forms a highpass filter. The −3 dB point of this high pass filter is $1/(2\pi R_L C_O)$, so care should be taken to make sure that the product of R_L and C_O is large enough to pass low frequencies to the load. When driving an 8Ω load, and if a full audio spectrum reproduction is required, C_O should be at least 470 µF. V_{O2}, the output that is not used, is connected through a 0.1 µF capacitor to a 2 kΩ load to prevent instability. While such an instability will not affect the waveform of V_{O1}, it is good design practice to load the second output.

AUDIO POWER AMPLIFIER DESIGN

Design a 500 mW / 8Ω Audio Amplifier

Given:

Power Output	500 mWrms
Load Impedance	8Ω
Input Level	1 Vrms(max)
Input Impedance	20 kΩ
Bandwidth	20 Hz–20 kHz ±0.25 dB

A designer must first determine the needed supply rail to obtain the specified output power. Calculating the required supply rail involves knowing two parameters, V_{opeak} and also the dropout voltage. The latter is typically 0.7V. V_{opeak} can be determined from equation 3.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (3)$$

For 500 mW of output power into an 8Ω load, the required V_{opeak} is 2.83V. A minumum supply rail of 3.53V results from adding V_{opeak} and V_{od}. But 3.53V is not a standard voltage that exists in many applications and for this reason, a supply rail of 5V is designated. Extra supply voltage creates dynamic headroom that allows the LM4861 to reproduce peaks in excess of 500 mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{vd} \geq 2^* \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$R_f/R_i = A_{vd}/2 \quad (5)$$

From equation 4, the minimum A_{vd} is: A_{vd} = 2

Since the desired input impedance was 20 kΩ, and with a A_{vd} of 2, a ratio of 1:1 of R_f to R_i results in an allocation of R_i = R_f = 20 kΩ. Since the A_{vd} was less than 10, a feedback capacitor is not needed. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 db point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified. This fact results in a low and high frequency pole of 4 Hz and 100 kHz respectively. As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1 / (2\pi^*20\ k\Omega^*4\ Hz) = 1.98\ \mu F$; use 2.2 µF.

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the differential gain, A_{vd}. With a A_{vd} = 2 and f_H = 100 kHz, the resulting GBWP = 100 kHz which is much smaller than the LM4861 GBWP of 7 MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4861 can still be used without running into bandwidth problems.

Section 6

Support Circuitry

Section 6 Contents

National Semiconductor

LMC7101 Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/4 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

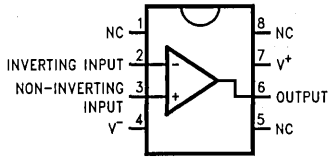
- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/4
- Input common-mode range includes V^- and V^+
- Tiny package outside dimensions—120 x 118 x 56 mils, 3.05 x 3.00 x 1.43 mm

Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

Connection Diagrams

8-Pin DIP



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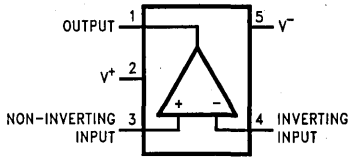
Top View

5-Pin SOT23-5



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Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied As
8-Pin DIP	LMC7101AIN	N08E	LMC7101AIN	Rails
8-Pin DIP	LMC7101BIN	N08E	LMC7101BIN	Rails
5-Pin SOT 23-5	LMC7101AIM5	MA05A	A00A	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5	MA05A	A00B	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101AIM5X	MA05A	A00A	3k Units Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5X	MA05A	A00B	3k Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Difference Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Recommended Operating Conditions (Note 1)

Supply Voltage	$2.7V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC7101AI, LMC7101BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M05A Package, 5-Pin Surface Mt.	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.11	6	9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			µV/°C
I_B	Input Bias Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$ $V^+ = 2.7V$	70	55	50	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = V$ For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.0	2.7	2.7	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.35V$ to $1.65V$ $V^- = -1.35V$ to $-1.65V$ $V_{CM} = 0$	60	50	45	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\ k\Omega$	2.45	2.15	2.15	V min
			0.25	0.5	0.5	V max
		$R_L = 10\ k\Omega$	2.68	2.64	2.64	V min
			0.025	0.06	0.06	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max
SR	Slew Rate	(Note 8)	0.7			V/µs
GBW	Gain-Bandwidth Product		0.6			MHz

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = 1.5V, V_O = $V^+/2$ and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	4 **6**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			μV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V V^+ = 3V	74	64	60	db min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.3	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	V^+ = 1.5V to 7.5V V^- = −1.5V to −7.5V V_O = V_{CM} = 0	80	68	60	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	R_L = 2 kΩ	2.8	2.6	2.6	V min
			0.2	0.4	0.4	V max
		R_L = 600Ω	2.7	2.5	2.5	V min
			0.37	0.6	0.6	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = $V^+/2$ and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 5V	0.11	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			µV/°C
I_B	Input Current		1	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	82	65 **60**	60 **55**	db min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			5.3	5.20 **5.00**	5.20 **5.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	R_L = 2 kΩ	4.9	4.7 **4.6**	4.7 **4.6**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	V max
		R_L = 600Ω	4.7	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	24	16 **11**	16 **11**	mA min
		Sinking, V_O = 5V	19	11 **7.5**	11 **7.5**	mA min
I_S	Supply Current		0.5	0.85 **1.0**	0.85 **1.0**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = $V^+/2$ and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.0 V_{PP}	0.01			%
SR	Slew Rate		1.0			V/μs
GBW	Gain_Bandwidth Product		1.0			MHz

15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = $V^+/2$ and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11			mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			μV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 15V	82	70 **65**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			15.3	15.20 **15.00**	15.20 **15.00**	V max
A_V	Large Signal Voltage Gain	R_L = 2 kΩ Sourcing (Note 7) Sinking	340 24	80 **40** 15 **10**	80 **40** 15 **10**	V/mV
		R_L = 600Ω Sourcing (Note 7) Sinking	300 15	34 6	34 6	V/mV
C_{IN}	Input Capacitance		3			pF
V_O	Output Swing	V^+ = 15V R_L = 2 kΩ	14.7	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω	14.1	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (Note 9)	50	30 **20**	30 **20**	mA min
		Sinking, V_O = 12V (Note 9)	50	30 **20**	30 **20**	mA min
I_S	Supply Current		0.8	1.50 **1.71**	1.50 **1.71**	mA max

15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = $V^+/2$ and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
SR	Slew Rate	V^+ = 15V (Note 8)	1.1	0.5 **0.4**	0.5 **0.4**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.1			MHz
ϕ_m	Phase Margin		45			Deg
G_m	Gain Margin		10			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	37			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	1.5			$\frac{fA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP}	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 1.5V and R_L connect to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 12.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

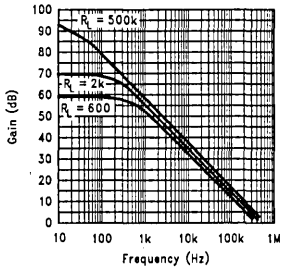
Note 8: V^+ = 15V. Connected as a Voltage Follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5V. Amp excited with 1 kHz to produce V_O = 10 V_{PP}.

Note 9: Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.

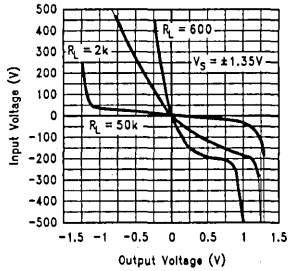
Typical Performance Characteristics V_S = +2.7V, Single Supply, T_A = 25°C unless specified

2.7V PERFORMANCE

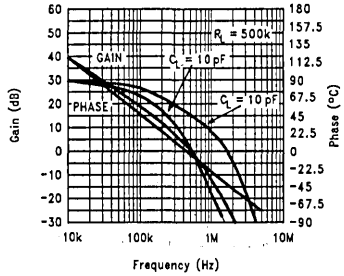
Open Loop Frequency Response (2.7V)



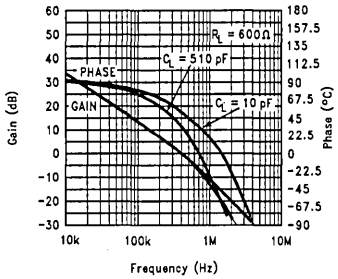
Input Voltage vs Output Voltage (2.7V)



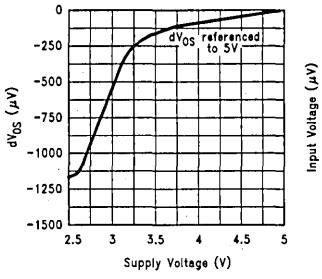
Gain and Phase vs Capacitance Load (2.7V)



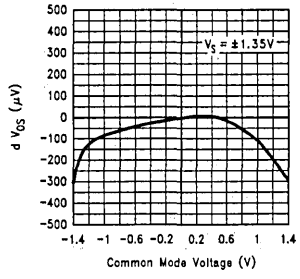
Gain and Phase vs Capacitance Load (2.7V)



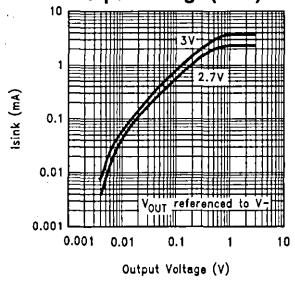
dV_{OS} vs Supply Voltage



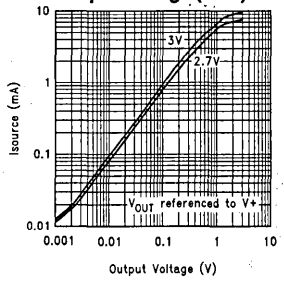
dV_{OS} vs Common Mode Voltage (2.7V)



Sinking Current vs Output Voltage (2.7V)



Sourcing Current vs Output Voltage (2.7V)



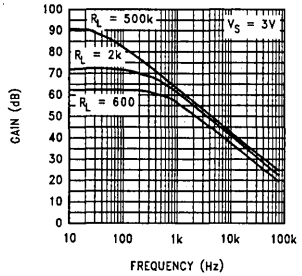
TL/H/11991–15

Typical Performance Characteristics

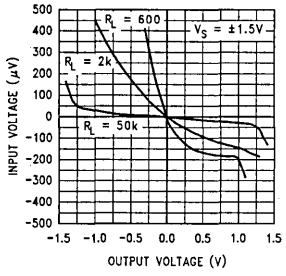
Single Supply, T_A = 25°C unless specified (Continued)

3V PERFORMANCE

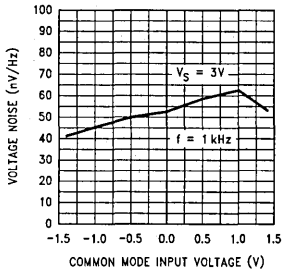
Open Loop Frequency Response (3V)



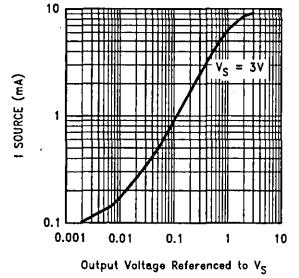
Input Voltage vs Output Voltage (3V)



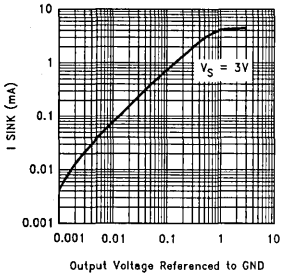
Input Voltage Noise vs Input Voltage (3V)



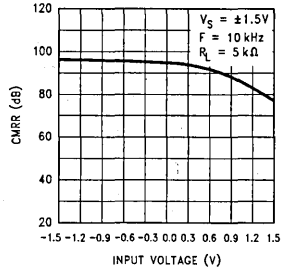
Sourcing Current vs Output Voltage (3V)



Sinking Current vs Output Voltage (3V)

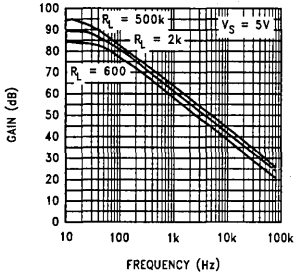


CMRR vs Input Voltage (3V)

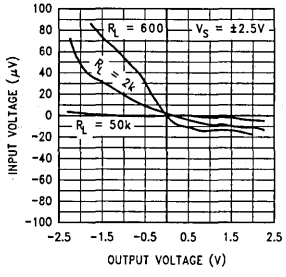


5V PERFORMANCE

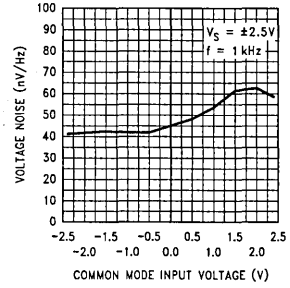
Open Loop Frequency Response (5V)



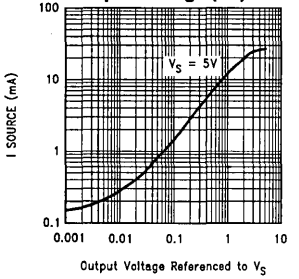
Input Voltage vs Output Voltage (5V)



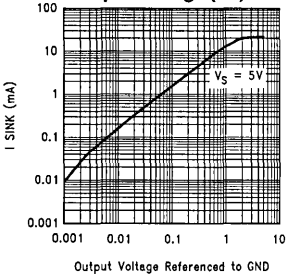
Input Voltage Noise vs Input Voltage (5V)



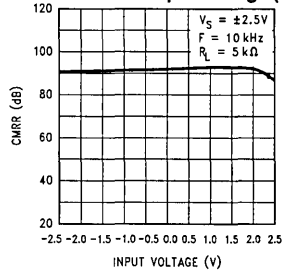
Sourcing Current vs Output Voltage (5V)



Sinking Current vs Output Voltage (5V)



CMRR vs Input Voltage (5V)

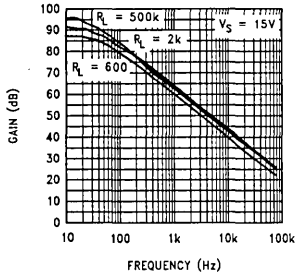


TL/H/11991–3

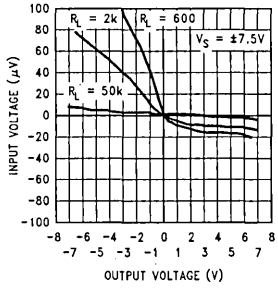
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless specified (Continued)

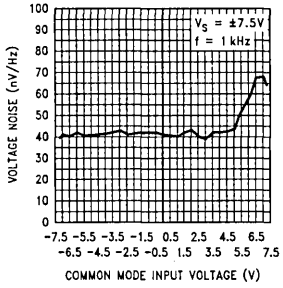
Open Loop Frequency Response (15V)



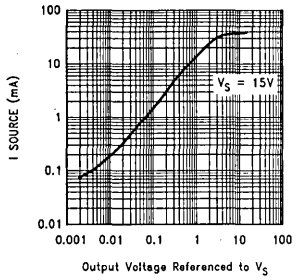
Input Voltage vs Output Voltage (15V)



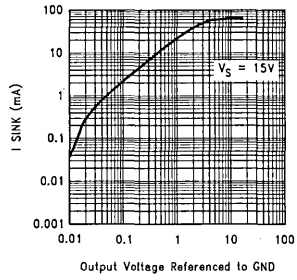
Input Voltage Noise vs Input Voltage (15V)



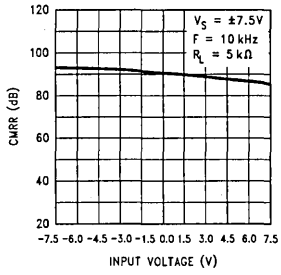
Sourcing Current vs Output Voltage (15V)



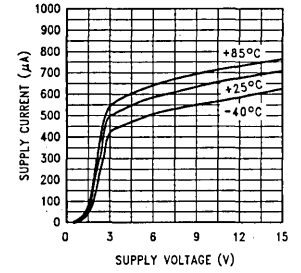
Sinking Current vs Output Voltage (15V)



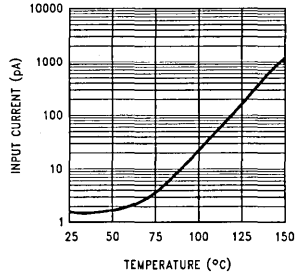
CMRR vs Input Voltage (15V)



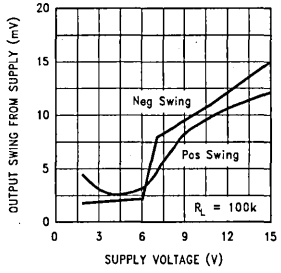
Supply Current vs Supply Voltage



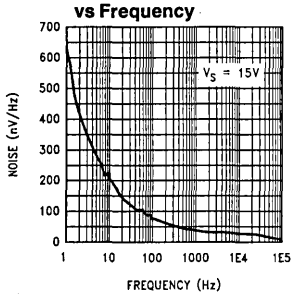
Input Current vs Temperature



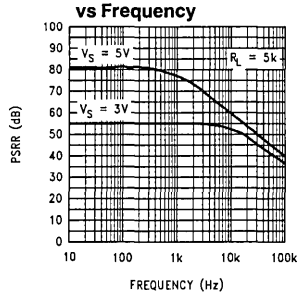
Output Voltage Swing vs Supply Voltage



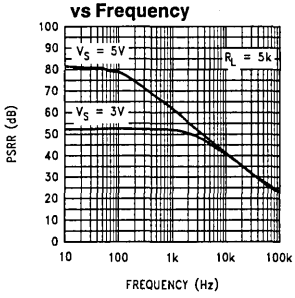
Input Voltage Noise vs Frequency



Positive PSRR vs Frequency



Negative PSRR vs Frequency



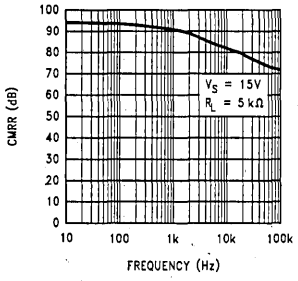
TL/H/11991–4

6

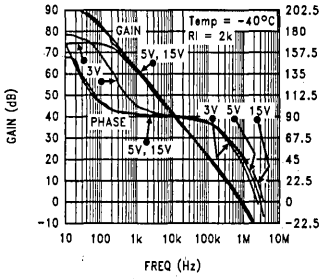
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless specified (Continued)

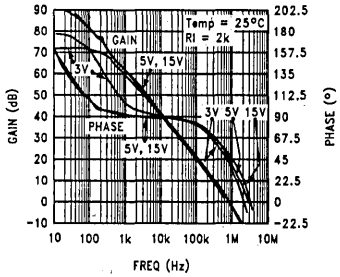
CMRR vs Frequency



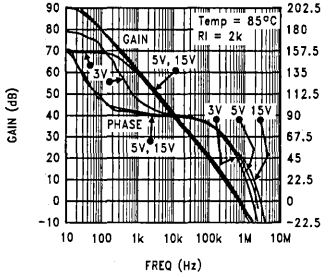
Open Loop Frequency Response @ −40°C



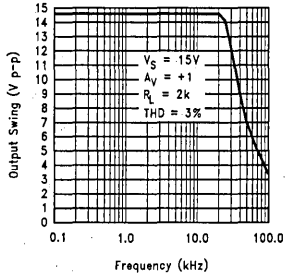
Open Loop Frequency Response @ 25°C



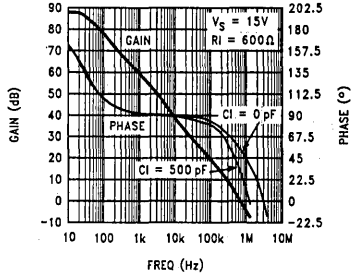
Open Loop Frequency Response @ 85°C



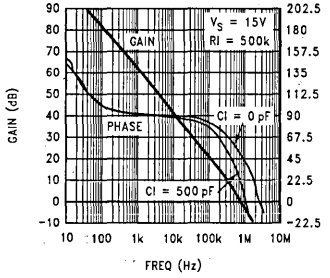
Maximum Output Swing vs Frequency



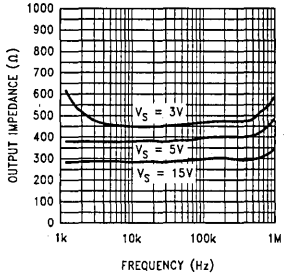
Gain and Phase vs Capacitive Load



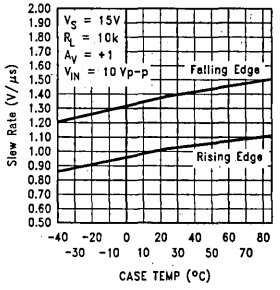
Gain and Phase vs Capacitive Load



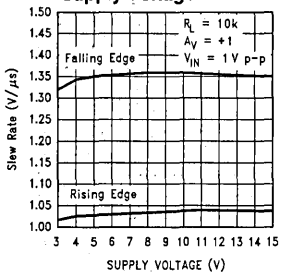
Output Impedance vs Frequency



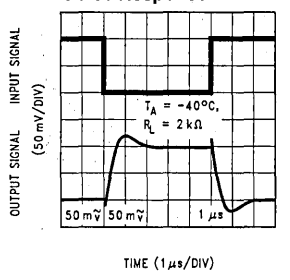
Slew Rate vs Temperature



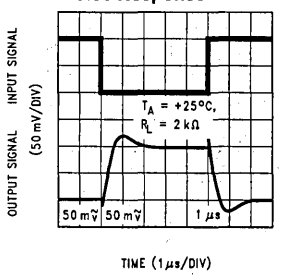
Slew Rate vs Supply Voltage



Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response

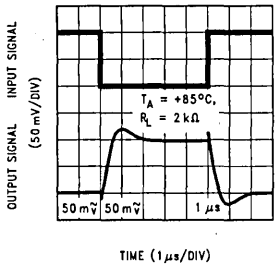


TL/H/11991-5

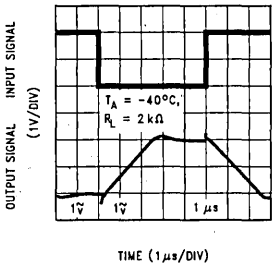
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless specified (Continued)

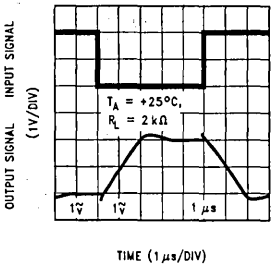
Inverting Small Signal Pulse Response



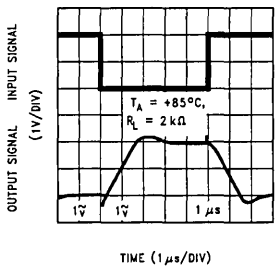
Inverting Large Signal Pulse Response



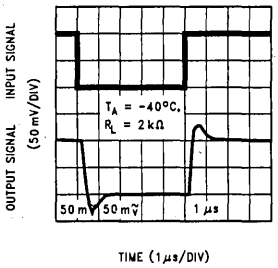
Inverting Large Signal Pulse Response



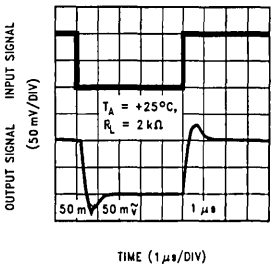
Inverting Large Signal Pulse Response



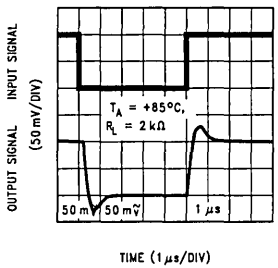
Non-Inverting Small Signal Pulse Response



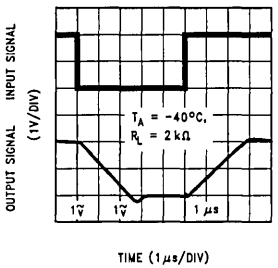
Non-Inverting Small Signal Pulse Response



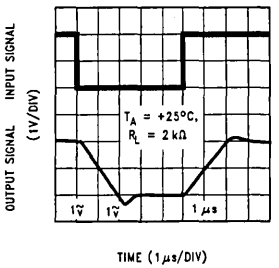
Non-Inverting Small Signal Pulse Response



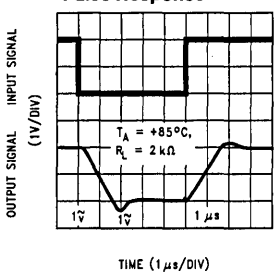
Non-Inverting Large Signal Pulse Response



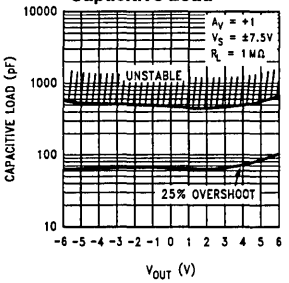
Non-Inverting Large Signal Pulse Response



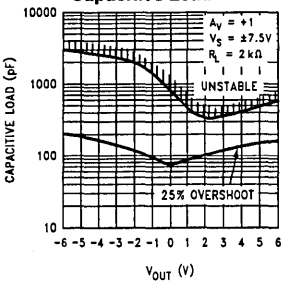
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load

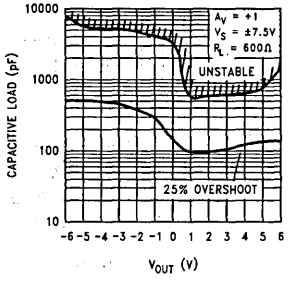


TL/H/11991–6

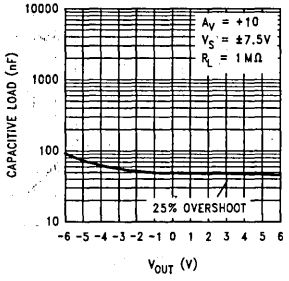
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless specified (Continued)

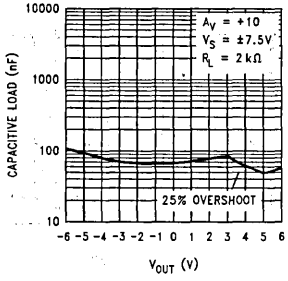
Stability vs Capacitive Load



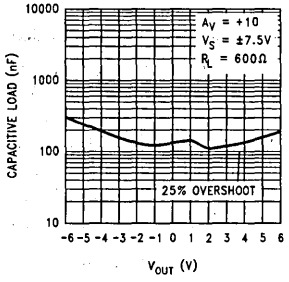
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11991–7

Application Information

1.0 Benefits of the LMC7101 Tiny Amp

Size. The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity. Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout. The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7101 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Tapes of ten for prototyping. The SOT23-5 packaged devices are available in convenient and economical ten unit tapes for prototypes, evaluation, and small production runs.

Low THD. The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10 kΩ load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

Low Supply Current. The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

2.0 Input Common Mode Voltage Range

The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

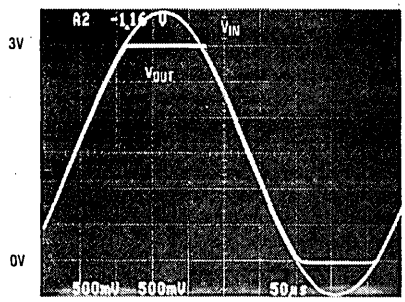


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FIGURE 1. An Input Voltage Signal Exceeds the LMC7101 Power Supply Voltages with No Output Phase Inversion

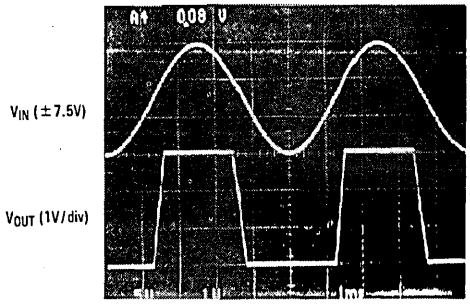

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FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in *Figure 3*.

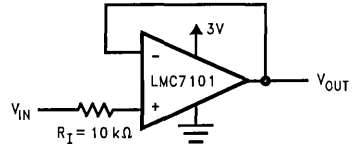

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FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Rail-To-Rail Output

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 80Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC7101 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

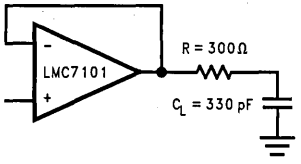

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FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

5.0 Compensating for Input Capacitance when Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 5*), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

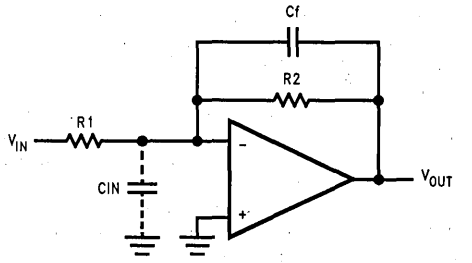

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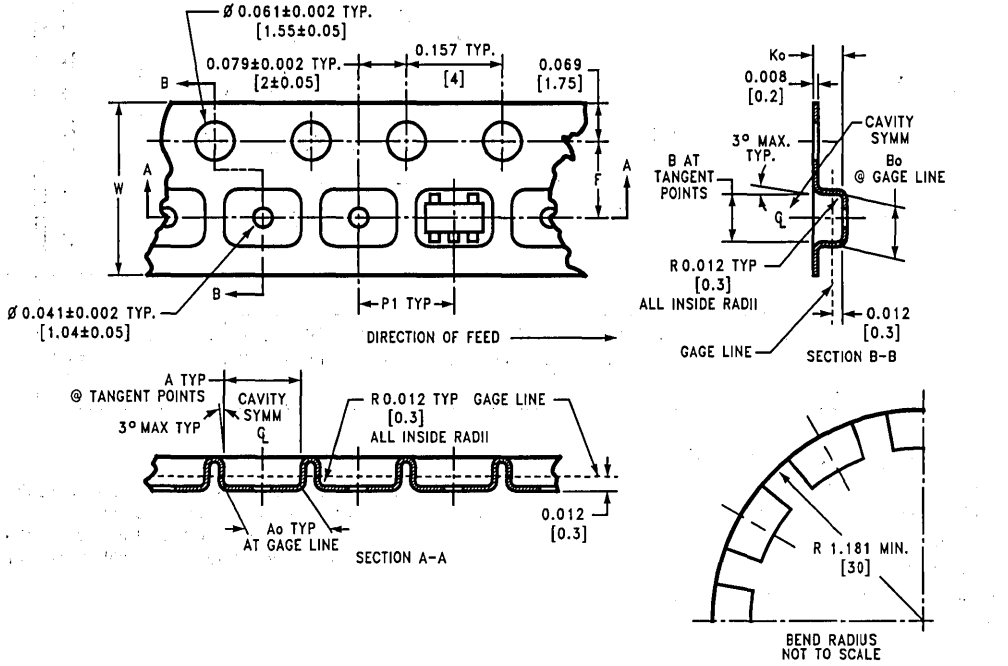
FIGURE 5. Cancelling the Effect of Input Capacitance

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



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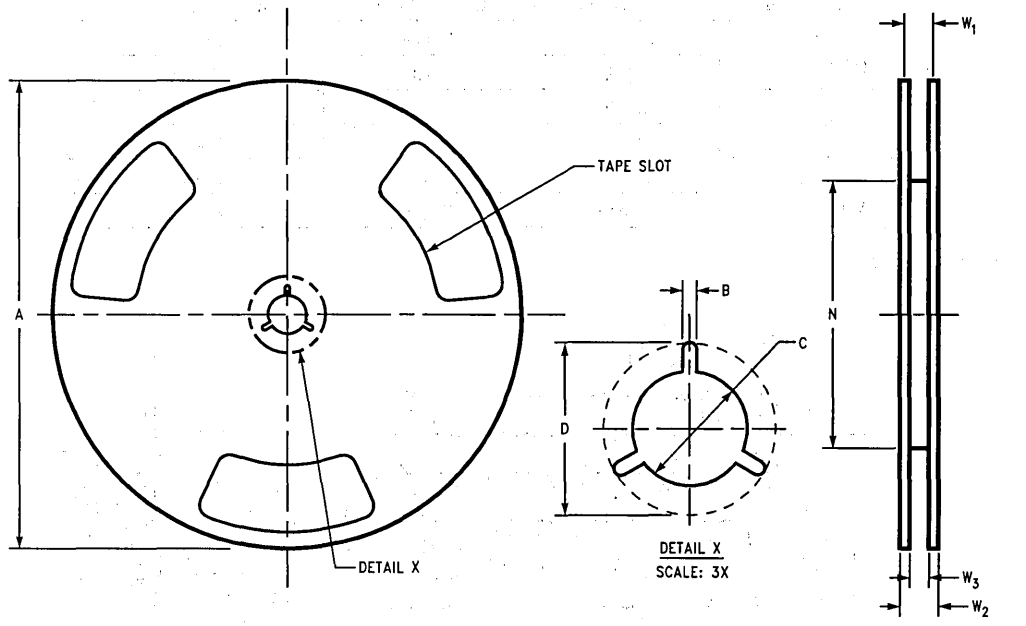
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

6

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



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8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

6.0 SPICE Macromodel

A SPICE macromodel is available for the LMC7101. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

National Semiconductor

LMC7111
Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

General Description

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT 23-5 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V^+ supply. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

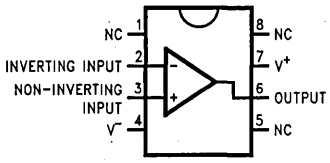
- Tiny SOT23-5 package saves space
- Very wide common mode input range
- Specified at 2.7V, 5V, and 10V
- Typical supply current 25 μA at 5V
- 50 kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20 mV of supply rail at 100k load
- Good capacitive load drive

Applications

- Mobile communications
- Portable computing
- Current sensing for battery chargers
- Voltage reference buffering
- Sensor interface
- Stable bias for GaAs RF amps

Connection Diagrams

8-Pin DIP



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Top View

Actual Size

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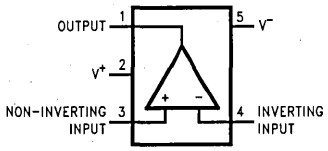
5-Pin SOT23-5



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Top View

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7111AIN	N08E	LMC7111AIN	Rails
8-Pin DIP	LMC7111BIN	N08E	LMC7111BIN	Rails
5-Pin SOT23-5	LMC7111BIM5X	MA05A	A01B	3k Units on Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance SOT23-5 (Note 2)	2000V
ESD Tolerance DIP Package (Note 2)	1500V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	11V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±30 mA
Current at Power Supply Pin	30 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.5V \le V^+ \le 11V$
Junction Temperature Range	
LMC7111AI, LMC7111BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.9	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			µV/°C
I_B	Input Bias Current	(Note 9)	0.1	1 **20**	1 **20**	pA max
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5 **10**	0.5 **10**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \le V^+ \le 5.0V$, $V^- = 0V$, $V_O = 2.5V$	60	55 **50**	55 **50**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-2.7V \le V^- \le -5.0V$, $V^- = 0V$, $V_O = 2.5V$	60	55 **50**	55 **50**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$ For CMRR ≥ 50 dB	−0.10	0.0 **0.40**	0.0 **0.40**	V min
			2.8	2.7 **2.25**	2.7 **2.25**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$V^+ = 2.7V$ $R_L = 100\ k\Omega$	2.69	2.68 **2.4**	2.68 **2.4**	V min
			0.01	0.02 **0.08**	0.02 **0.08**	V max
		$V^+ = 2.7V$ $R_L = 10\ k\Omega$	2.65	2.6 **2.4**	2.6 **2.4**	V min
			0.03	0.1 **0.3**	0.1 **0.3**	V max

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	7	1 **0.7**	1 **0.7**	mA min
		Sinking, V_O = 2.7V	7	1 **0.7**	1 **0.7**	mA min
A_{VOL}	Voltage Gain	Sourcing	400			V/mv min
		Sinking	150			V/mv min
I_S	Supply Current	V^+ = +2.7V, V_O = $V^+/2$	20	45 **60**	50 **65**	μA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.015			V/μs
GBW	Gain-Bandwidth Product		40			kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 2.7V, V_{CM} = 1.35V and R_L connected to 1.35V. For Sourcing tests, 1.35V ≤ V_O ≤ 2.7V. For Sinking tests, 0.5V ≤ V_O ≤ 1.35V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, V^+ = 2.7V and R_L = 100 kΩ connected to 1.35V. Amp excited with 1 kHz to produce V_O = 1 V_{PP}.

Note 9: Bias Current guaranteed by design and processing.

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	V^+ = 3V For CMRR ≥ 50 dB	−0.25	0.0	0.0	V min
			3.2	3.0 **2.8**	3.0 **2.8**	V max

3.3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	V^+ = 3.3V For CMRR ≥ 50 dB	−0.25	−0.1 **0.00**	−0.1 **0.00**	V min
			3.5	3.4 **3.2**	3.4 **3.2**	V max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 5V	0.9			mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			µV/°C
I_B	Input Bias Current	(Note 9)	0.1	1 **20**	1 **20**	pA max
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5 **10**	0.5 **10**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	85	70	60	dB min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤10V, V^- = 0V, V_O = 2.5V	85	70	60	dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤ −10V, V^- = 0V, V_O = −2.5V	85	70	60	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			5.25	5.20 **5.00**	5.20 **5.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	V^+ = 5V	4.99	4.98	4.98	Vmin
		R_L = 100 kΩ	0.01	0.02	0.02	Vmax
		V^+ = 5V	4.98	4.9	4.9	Vmin
		R_L = 10 kΩ	0.02	0.1	0.1	Vmin
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	7	5 **3.5**	5 **3.5**	mA min
		Sinking, V_O = 3V	7	5 **3.5**	5 **3.5**	mA min
A_{VOL}	Voltage Gain	Sourcing	500			V/mv min
		Sinking	200			V/mv min
I_S	Supply Current	V^+ = +5V, V_O = $V^+/2$	25			µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	Positive Going Slew Rate (Note 8)	0.027	0.015	0.010	V/μs
GBW	Gain-Bandwidth Product		50			kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 5V, V_{CM} = 2.5V and R_L connected to 2.5V. For Sourcing tests, 2.5V ≤ V_O ≤ 5.0V. For Sinking tests, 0.5V ≤ V_O ≤ 2.5V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive slew rate. The negative slew rate is faster. Input referred, V^+ = 5V and R_L = 100 kΩ connected to 1.5V. Amp excited with 1 kHz to produce V_O = 1 V_{PP}.

Note 9: Bias Current guaranteed by design and processing.

10V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 10V	0.9	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			µV/°C
I_B	Input Bias Current		0.1	1 **20**	1 **20**	pA max
I_{OS}	Input Offset Current		0.01	0.5 **10**	0.5 **10**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤10V, V^- = 0V, V_O = 2.5V	80			dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤ −10V, V^- = 0V, V_O = 2.5V	80			dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 10V For CMRR ≥ 50 dB	−0.2	−0.15 **0.00**	−0.15 **0.00**	V min
			10.2	10.15 **10.00**	10.15 **10.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
I_{SC}	Output Short Circuit Current (Note 9)	Sourcing, V_O = 0V	30	20 **7**	20 **7**	mA min
		Sinking, V_O = 10V	30	20 **7**	20 **7**	mA min
A_{VOL}	Voltage Gain 100 kΩ Load	Sourcing	500			V/mv min
		Sinking	200			V/mv min
I_S	Supply Current	V^+ = +10V, V_O = $V^+/2$	25	50 **65**	60 **75**	µA max
V_O	Output Swing	V^+ = 10V	9.99	9.98	9.98	Vmin
		R_L = 100 kΩ	0.01	0.02	0.02	Vmax
		V^+ = 10V	9.98	9.9	9.9	Vmin
		R_L = 10 kΩ	0.02	0.1	0.1	Vmin

10V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.03			V/μs
GBW	Gain-Bandwidth Product		50			kHz
ϕ_m	Phase Margin		50			deg
G_m	Gain Margin		15			dB
	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	110			$\frac{nV}{\sqrt{Hz}}$
	Input-Referred Current Noise	f = 1 kHz	0.03			$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

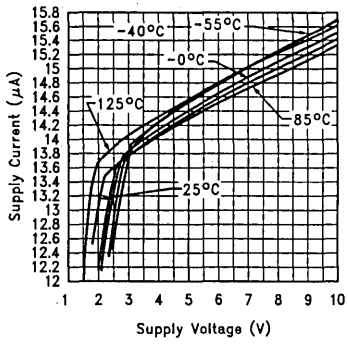
Note 7: V^+ = 10V, V_{CM} = 5V and R_L connected to 5V. For Sourcing tests, 5V ≤ V_O ≤ 10V. For Sinking tests, 0.5V ≤ V_O ≤ 5V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, V^+ = 10V and R_L = 100 kΩ connected to 5V. Amp excited with 1 kHz to produce V_O = 2 V_{PP}.

Note 9: Operation near absolute maximum limits will adversely affect reliability.

Typical Performance Characteristics T_A = 25°C unless specified, Single Supply

Supply Current vs Supply Voltage



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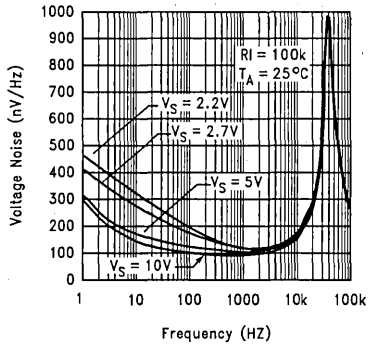
Voltage Noise vs Frequency



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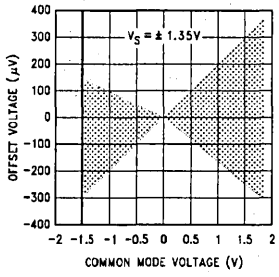
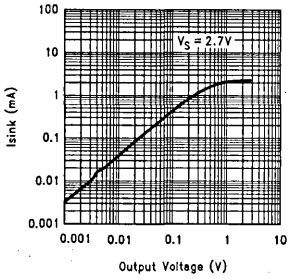
2.7V PERFORMANCE

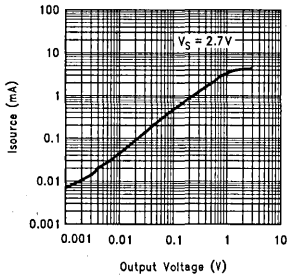
Offset Voltage vs Common Mode Voltage @ 2.7V



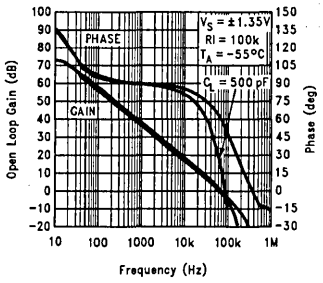
Sinking Output vs Output Voltage



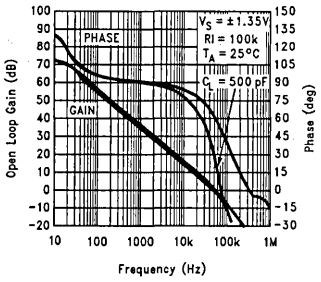
Sourcing Output vs Output Voltage



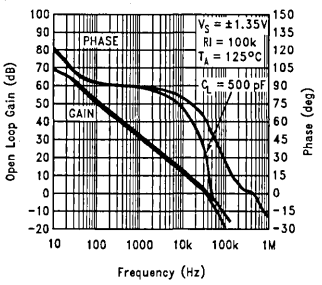
Gain and Phase vs Capacitive Load @ 2.7V



Gain and Phase vs Capacitive Load @ 2.7V



Gain and Phase vs Capacitive Load @ 2.7V

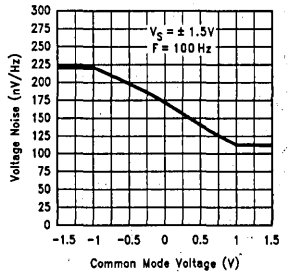


TL/H/12352-7

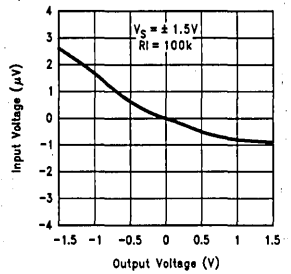
Typical Performance Characteristics T_A = 25°C unless specified, Single Supply (Continued)

3V PERFORMANCE

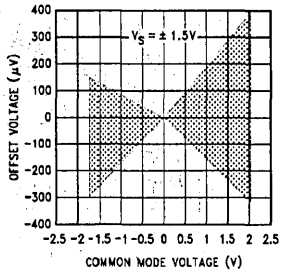
Voltage Noise vs Common Mode Voltage @ 3V



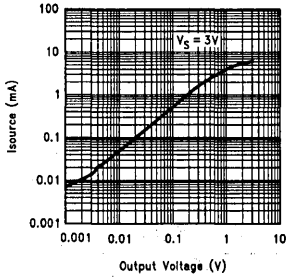
Output Voltage vs Input Voltage @ 3V



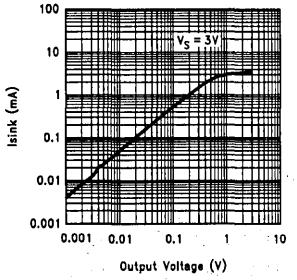
Offset Voltage vs Common Mode Voltage @ 3V



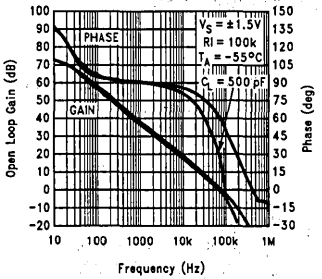
Sourcing Output vs Output Voltage



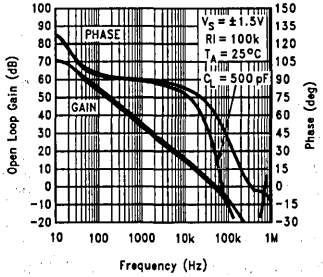
Sinking Output vs Output Voltage



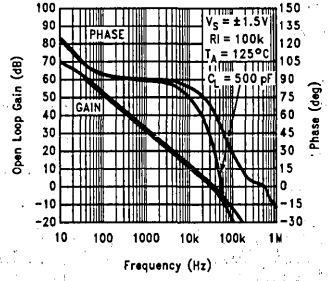
Gain and Phase vs Capacitive Load @ 3V



Gain and Phase vs Capacitive Load @ 3V



Gain and Phase vs Capacitive Load @ 3V

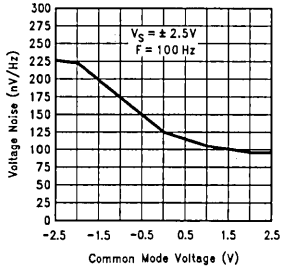


TL/H/12352–8

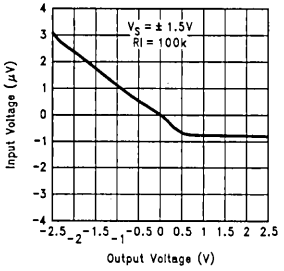
Typical Performance Characteristics T_A = 25°C unless specified, Single Supply (Continued)

5V PERFORMANCE

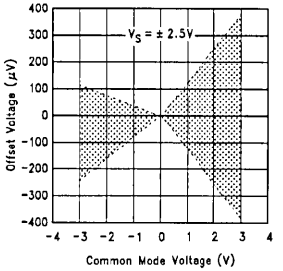
Voltage Noise vs Common Mode Voltage @ 5V



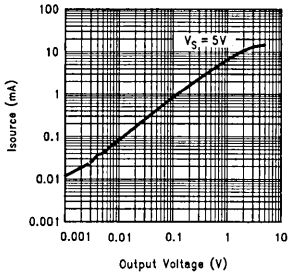
Output Voltage vs Input Voltage @ 5V



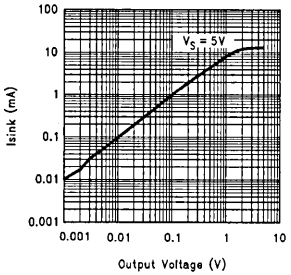
Offset Voltage vs Common Mode Voltage @ 5V



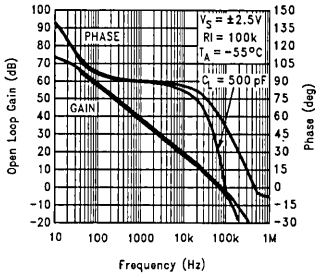
Sourcing Output vs Output Voltage



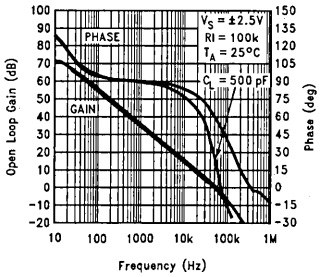
Sinking Output vs Output Voltage



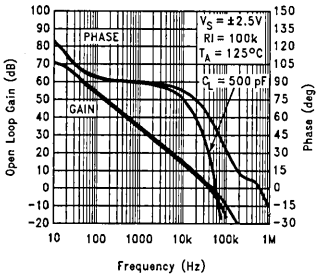
Gain and Phase vs Capacitive Load @ 5V



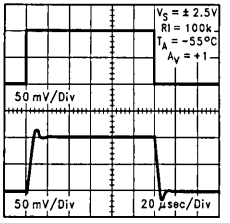
Gain and Phase vs Capacitive Load @ 5V



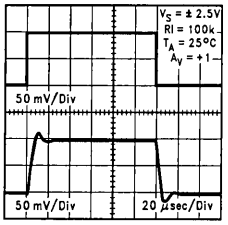
Gain and Phase vs Capacitive Load @ 5V



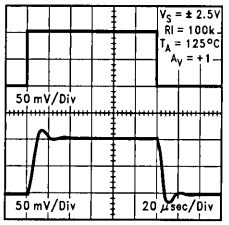
Non-Inverting Small Signal Pulse Response at 5V



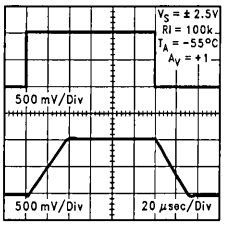
Non-Inverting Small Signal Pulse Response at 5V



Non-Inverting Small Signal Pulse Response at 5V



Non-Inverting Large Signal Pulse Response at 5V

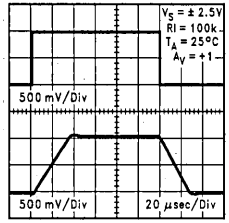


TL/H/12352–9

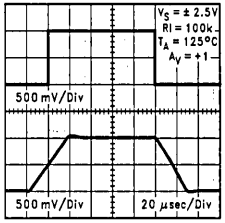
Typical Performance Characteristics T_A = 25°C unless specified, Single Supply (Continued)

5V PERFORMANCE (Continued)

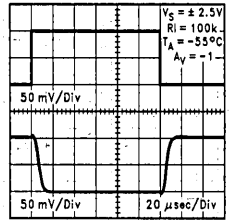
Non-Inverting Large Signal Pulse Response at 5V



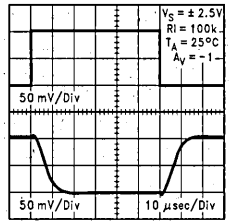
Non-Inverting Large Signal Pulse Response at 5V



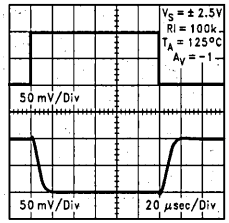
Inverting Small Signal Pulse Response at 5V



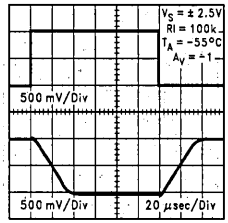
Inverting Small Signal Pulse Response at 5V



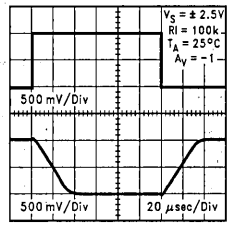
Inverting Small Signal Pulse Response at 5V



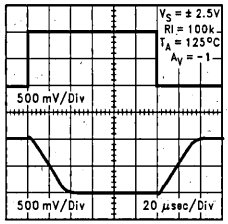
Inverting Large Signal Pulse Response at 5V



Inverting Large Signal Pulse Response at 5V



Inverting Large Signal Pulse Response at 5V

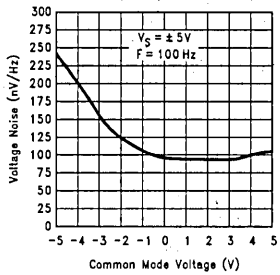


TL/H/12352–10

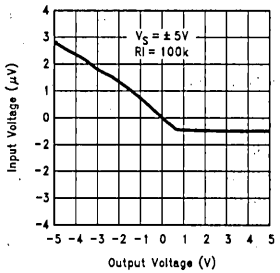
Typical Performance Characteristics T_A = 25°C unless specified, Single Supply (Continued)

10V PERFORMANCE

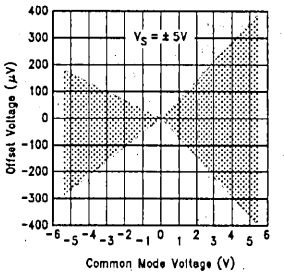
Voltage Noise vs Common Mode Voltage @ 10V



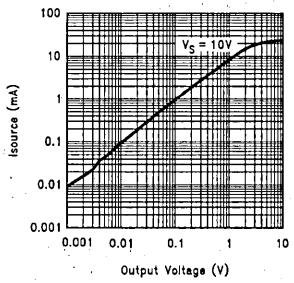
Output Voltage vs Input Voltage @ 10V



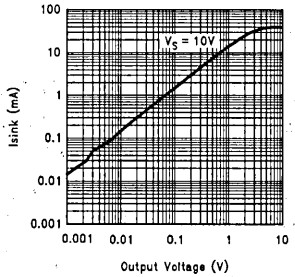
Offset Voltage vs Common Mode Voltage @ 10V



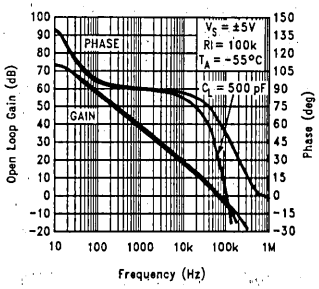
Sourcing Output vs Output Voltage



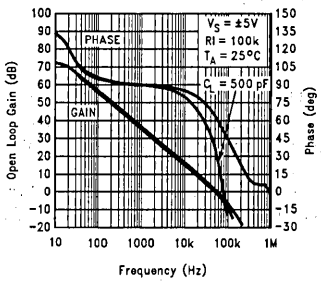
Sinking Output vs Output Voltage



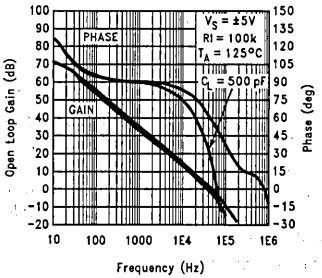
Gain and Phase vs Capacitive Load @ 10V



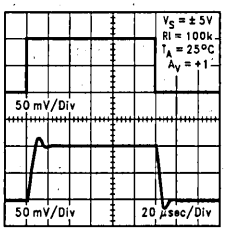
Gain and Phase vs Capacitive Load @ 10V



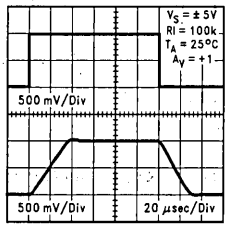
Gain and Phase vs Capacitive Load @ 10V



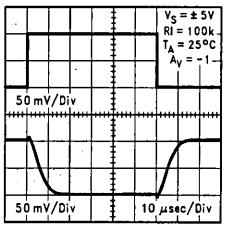
Non-Inverting Small Signal Pulse Response at 10V



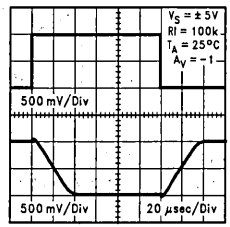
Non-Inverting Large Signal Pulse Response at 10V



Inverting Small Signal Pulse Response at 10V



Inverting Large Signal Pulse Response at 10V



TL/H/12352–11

Application Information

1.0 Benefits of the LMC7111 Tiny Amp

Size. The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity. Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout. The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7111 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current. The typical 25 μA supply current of the LMC7111 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage may vary over the life of the batteries.

2.0 Input Common Mode Voltage Range

The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor as shown in *Figure 1.*

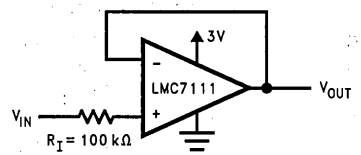


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FIGURE 1. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Capacitive Load Tolerance

The LMC7111 can typically directly drive a 300 pF load with V_S = 10V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 2.* This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

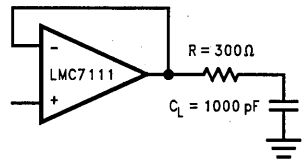

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FIGURE 2. Resistive Isolation of a 330 pF Capacitive Load

4.0 Compensating for Input Capacitance when Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 3*), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

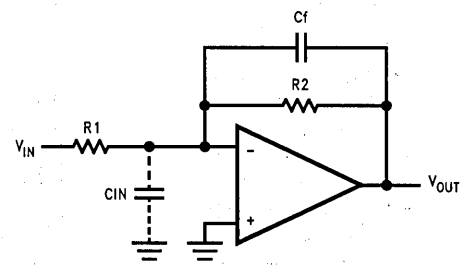

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FIGURE 3. Cancelling the Effect of Input Capacitance

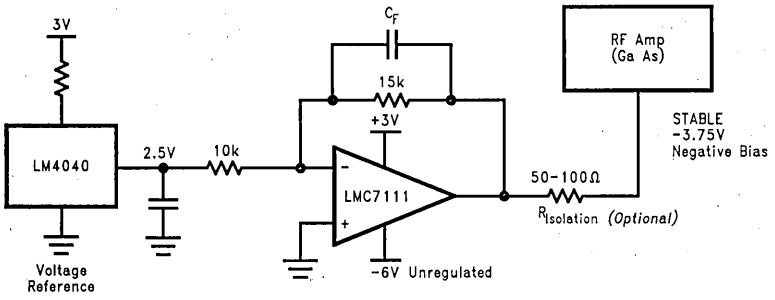
5.0 Output Swing

The output of the LMC7111 will go to within 100 mV of either power supply rail for a 10 kΩ load and to 20 mV of the rail for a 100 kΩ load. This makes the LMC7111 useful for driving transistors which are connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or all the way off.

6.0 Biasing GaAs RF Amplifiers

The capacitive load capability, low current draw, and small size of the SOT23-5 LMC7111 make it a good choice for providing a stable negative bias to other integrated circuits.

The very small size of the LMC7111 and the LM4040 reference take up very little board space.



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C_F and $R_{isolation}$ prevent oscillations when driving capacitive loads.

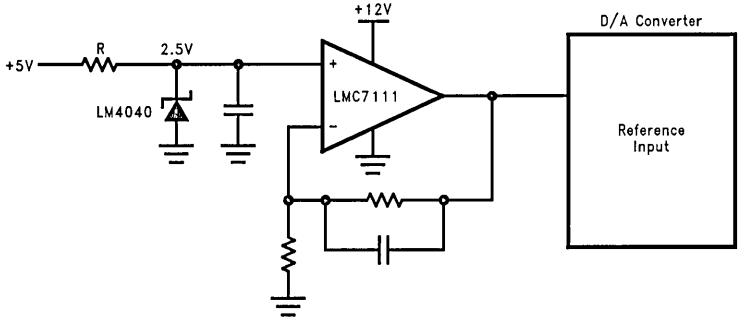
FIGURE 4. Stable Negative Bias

7.0 Reference Buffer for A-to-D Converters

The LMC7111 can be used as a voltage reference buffer for analog-to-digital converters. This works best for A-to-D converters whose reference input is a static load, such as dual slope integrating A-to-Ds. Converters whose reference input is a dynamic load (the reference current changes with time) may need a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows it to be placed close to the reference input. The low supply current (25 μA typical) saves power.

For A-to-D reference inputs which require higher accuracy and lower offset voltage, please see the LMC6462 datasheet. The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.



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8.0 Dual and Quad Devices with Similar Performance

The LMC6462 and LMC6464 are dual and quad devices with performance similar to the LMC7111. They are available in both conventional through-hole and surface mount packaging. Please see the LMC6462/4 datasheet for details.

9.0 SPICE Macromodel

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

10.0 Additional SOT23-5 Tiny Devices

National Semiconductor has additional parts available in the space saving SOT23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—

LMC7101 1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain, 700 μA typical current 2.7V, 3V, 5V and 15V specifications.

LM7131 Tiny Video amp with 70 MHz gain bandwidth. Specified at 3V, 5V and ± 5V supplies.

LMC7211 Comparator in a tiny package with rail-to-rail input and push-pull output. Typical supply current of 7 μA. Typical propagation delay of 7 μs. Specified at 2.7V, 5V and 15V supplies.

LMC7221 Comparator with an open drain output for use in mixed voltage systems. Similar to the LMC7211, except the output can be used with a pull-up resistor to a voltage different than the supply voltage.

LP2980 Micropower SOT 50 mA Ultra Low-Dropout Regulator.

LM4040 Precision micropower shunt voltage reference. Fixed voltages of 2.5000V, 4.096V, 5.000V, 8.192V and 10.000V.

LM4041 Precision micropower shunt voltage reference 1.225V and adjustable.

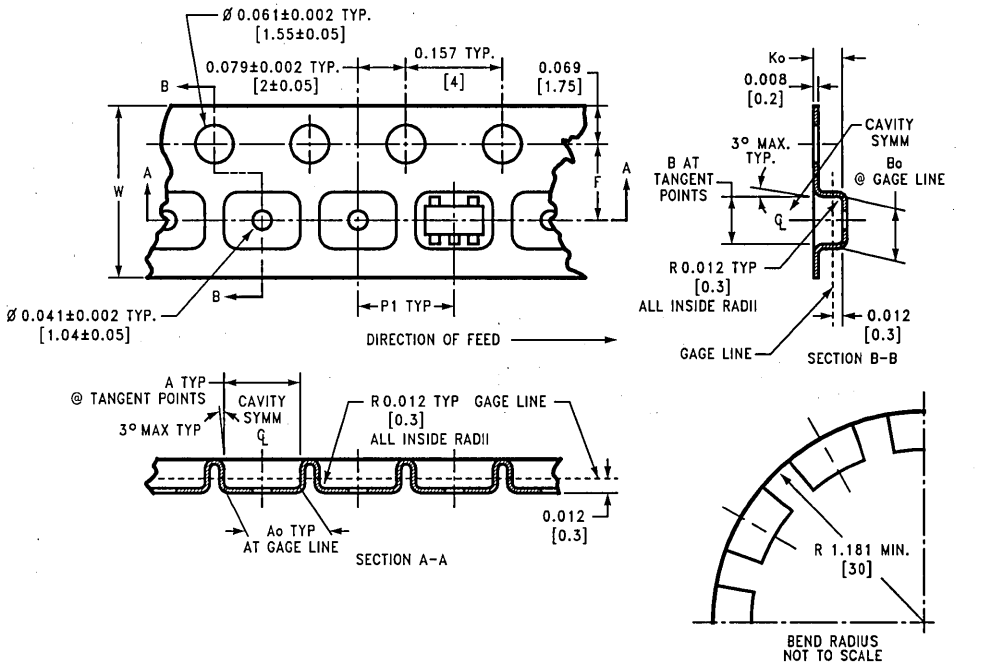
Contact your National Semiconductor representative for the latest information.

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



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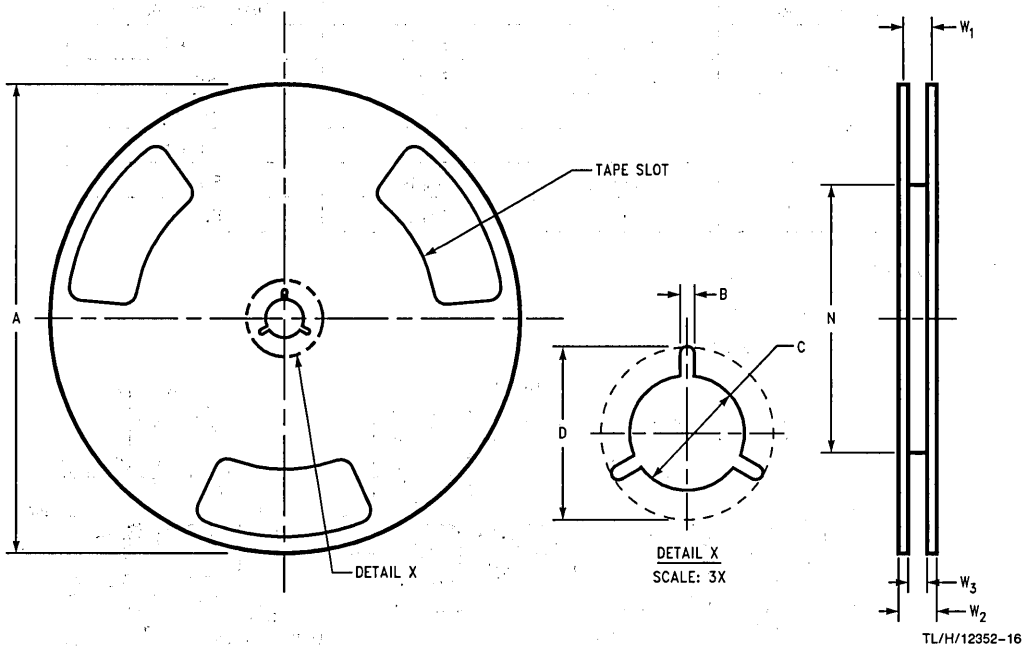
8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ±0.002 (3.5 ±0.05)	0.055 ±0.004 (1.4 ±0.11)	0.157 (4)	0.315 ±0.012 (8 ±0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



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8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

National Semiconductor

LMC7211
Tiny CMOS Comparator with Rail-to-Rail Input

General Description

The LMC7211 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes the comparator ideal for space and weight critical designs. The LMC7211 is available in SO-8 surface mount packages and in conventional 8-pin DIP packages. The LMC7211 is supplied in two offset voltage grades, 5 mV and 15 mV.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the LMC7211 a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

The Tiny Comparator's outside dimensions (length x width x height) of 3.05mm x 3.00mm x 1.43mm allow it to fit into tight spaces on PC boards.

Features

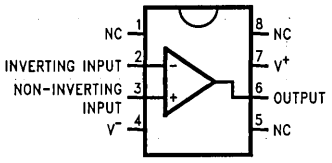
- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 7 μA at 5V
- Response time of 4 μs at 5V
- LMC7211—push-pull output
- Input common-mode range beyond V− and V+
- Low input current

Applications

- Battery Powered Products
- Notebooks and PDAs
- PCMCIA cards
- Mobile Communications
- Alarm and Security circuits
- Direct Sensor Interface
- Replaces amplifiers used as comparators with better performance and lower current

Connection Diagrams

8-Pin DIP/SO-8



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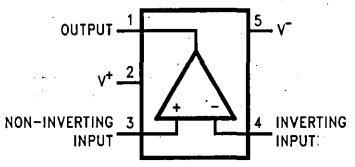
Top View

5-Pin SOT23-5



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Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7211AIN	N08E	LMC7211AIN	rails
8-Pin DIP	LMC7211BIN	N08E	LMC7211BIN	rails
8-Pin SO-8	LMC7211AIM	M08A	LM7211AIM	rails
8-Pin SO-8	LMC7211BIM	M08A	LM7211BIM	rails
8-Pin SO-8	LMC7211AIMX	M08A	LM7211AIM	2.5k units tape and reel
8-Pin SO-8	LMC7211BIMX	M08A	LM7211BIM	2.5k units tape and reel
5-Pin SOT 23-5	LMC7211AIM5X	MA05A	C00A	3k units tape and reel
5-Pin SOT 23-5	LMC7211BIM5X	MA05A	C00B	3k units tape and reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	(V_{CC}) +0.3V to $(-V_{CC})$ −0.3V
Voltage at Input/Output Pin	(V_{CC}) + 0.3V to $(-V_{CC})$ −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 7)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \le V_{CC} \le 15V$
Junction Temperature Range	
LMC7211AI, LMC7211BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-pin Molded DIP	112°C/W
SO-8 Package, 8-Pin Surface Mount	180°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		1.0			µV/°C
	Input Offset Voltage Average Drift	(Note 10)	3.3			µV/Month
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$	75			dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 15V$	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
		CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	I_{load} = 2.5 mA	2.5	2.4 **2.3**	2.4 **2.3**	V min
V_{OL}	Output Voltage Low	I_{load} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	V_{OUT} = Low	7	12 **14**	12 **14**	µA max

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	1.0			µV/°C
		V^+ = 15V	4.0			
	Input Offset Voltage Average Drift	V^+ = 5V	3.3			µV/Month
		V^+ = 15V	4.0			
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ration	V+ = 5.0V	75			dB
		V+ = 15.0V	82			dB
PSRR	Power Supply Rejection Ratio	$5V \le V^+ \le 10V$	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	V+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	V min
		V+ = 5.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
		V+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	V min
		V+ = 15.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	V+ = 5V I_{load} = 5 mA	4.8	4.6 **4.45**	4.6 **4.45**	mV min
		V+ = 15V I_{load} = 5 mA	14.8	14.6 **14.45**	14.6 **14.45**	mV min
V_{OL}	Output Voltage Low	V+ = 5V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV max
		V+ = 15V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV max
I_S	Supply Current	V_{OUT} = Low	7	14 **18**	14 **18**	µA max
I_{SC}	Short Circuit Current	Sourcing	30			mA
		Sinking (Note 8)	45			mA

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
t_{rise}	Rise Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV (Note 9)		0.3			µs
t_{fall}	Fall Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV (Note 9)		0.3			µs
t_{PHL}	Propagation Delay (High to Low) (Note 11)	f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			
t_{PLH}	Propagation Delay (Low to High) (Note 11)	f = 10 kHz, Cl = 50p (Note 9)	10 mV	6			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	7			µs
			100 mV	4			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage rating.

Note 8: Do not short circuit output to V+, when V+ is greater than 12V or reliability will be adversely affected.

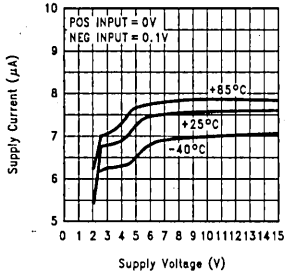
Note 9: C_L includes the probe and jig capacitance.

Note 10: Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst case input conditions and includes the first 30 days of drift.

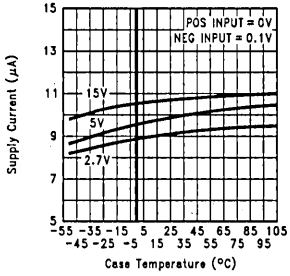
Note 11: Input step voltage for propagation delay measurement is 2V.

Typical Performance Characteristics Single Supply T_A = 25°C unless specified

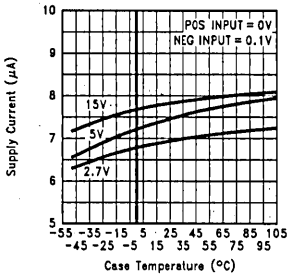
Supply Current vs Supply Voltage



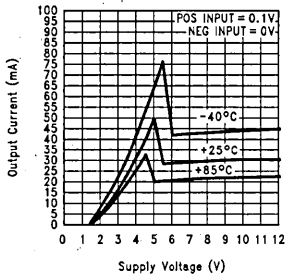
Supply Current vs Temperature while Sourcing



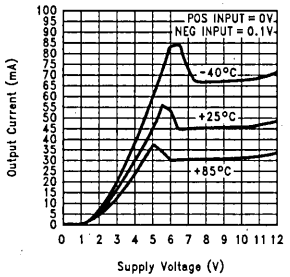
Supply Current vs Temperature while Sinking



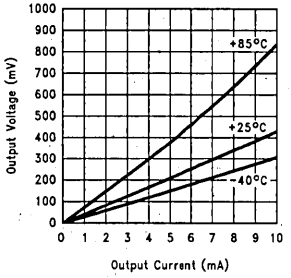
Output Sourcing Current vs Supply Voltage



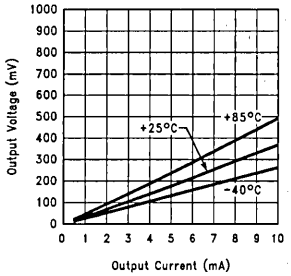
Output Sinking Current vs Supply Voltage



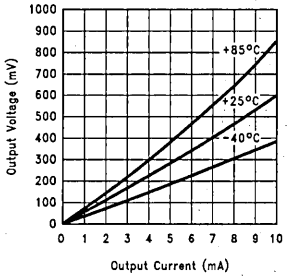
Output Sourcing Current vs Output Voltage @ 5V



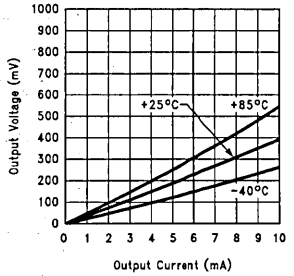
Output Sinking Current vs Output Voltage @ 5V



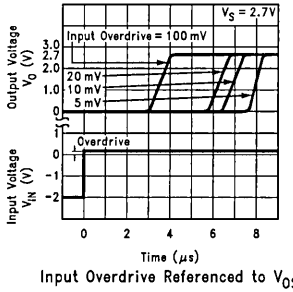
Output Sourcing Current vs Output Voltage @ 15V



Output Sinking Current vs Output Voltage @ 15V

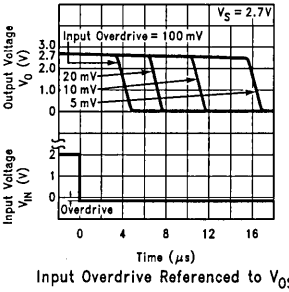


Response Time for Various Input Overdrives — t_{PLH}



Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives — t_{PHL}

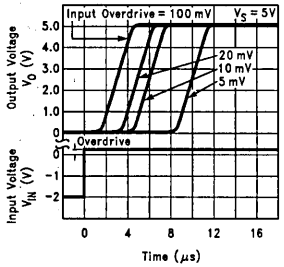


Input Overdrive Referenced to V_{OS}

TL/H/12337-3

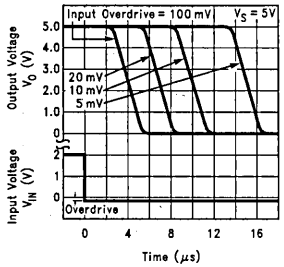
Typical Performance Characteristics Single Supply, T_A = 25°C unless specified (Continued)

Response Time for Various Input Overdrives — t_{PLH}



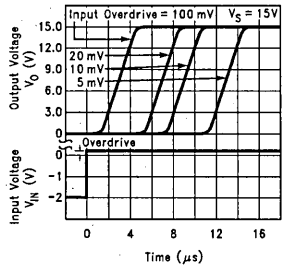
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives — t_{PHL}



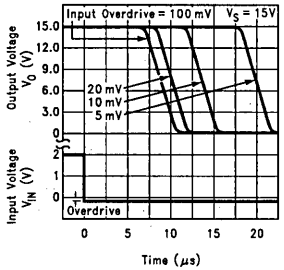
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives — t_{PLH}



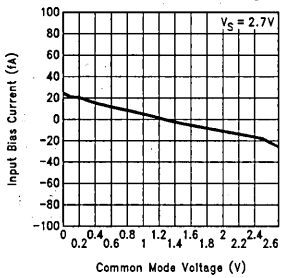
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives — t_{PHL}

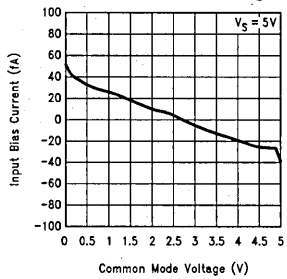


Input Overdrive Referenced to V_{OS}

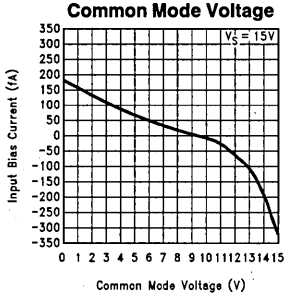
Input Bias Current vs Common Mode Voltage



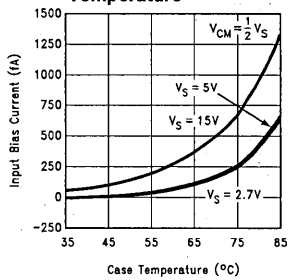
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature



TL/H/12337–4

Application Information

1.0 Benefits of the LMC7211 Tiny Comparator

Size. The small footprint of the SOT 23-5 packaged Tiny Comparator, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny Comparator makes it possible to use it in PCMCIA type III cards.

Simplified Board Layout. The Tiny Comparator can simplify board layout in several ways. First, by placing a comparator where comparators are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny Comparators instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7211 comparators packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current. The typical 7 μA supply current of the LMC7211 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7211 is characterized at 15V, 5V and 2.7V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7211 a good choice for devices where the voltage may vary over the life of the batteries.

Digital Outputs Representing Signal Level. Comparators provide a high or low digital output depending on the voltage levels of the (+) and (−) inputs. This makes comparators useful for interfacing analog signals to microprocessors and other digital circuits. The LMC7211 can be thought of as a one-bit a/d converter.

Push-Pull Output. The push-pull output of the LMC7211 is capable of both sourcing and sinking milliamp level currents even at a 2.7 volt supply. This can allow the LMC7211 to drive multiple logic gates.

Driving LEDs (Light Emitting Diodes). With a 5 volt power supply, the LMC7211's output sinking current can drive small, high efficiency LEDs for indicator and test point circuits. The small size of the Tiny package makes it easy to find space to add this feature to even compact designs.

Input range to Beyond Rail to Rail. The input common mode range of the LMC7211 is slightly larger than the actual power supply range. This wide input range means that the comparator can be used to sense signals close to the power supply rails. This wide input range can make design easier by eliminating voltage dividers, amplifiers, and other front end circuits previously used to match signals to the limited input range of earlier comparators. This is useful to power supply monitoring circuits which need to sense their own power supply, and compare it to a reference voltage which is close to the power supply voltage. The wide input range can also be useful for sensing the voltage drop across a current sense resistor for battery chargers.

Zero Crossing Detector. Since the LMC7211's common mode input range extends below ground even when powered by a single positive supply, it can be used with large input resistors as a zero crossing detector.

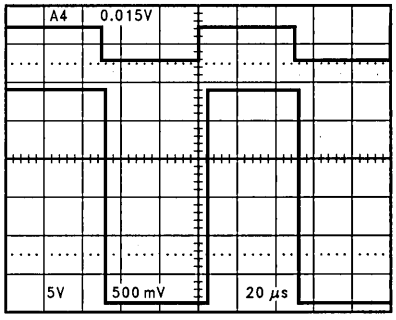
Low Input Currents and High Input Impedance. These characteristics allow the LMC7211 to be used to sense high impedance signals from sensors. They also make it possible to use the LMC7211 in timing circuits built with large value resistors. This can reduce the power dissipation of timing circuits. For very long timing circuits, using high value resistors can reduce the size and cost of large value capacitors for the same R-C time constant.

Direct Sensor Interfacing. The wide input voltage range and high impedance of the LMC7211 may make it possible to directly interface to a sensor without the use of amplifiers or bias circuits. In circuits with sensors which can produce outputs in the tens to hundreds of millivolts, the LMC7211 can compare the sensor signal with an appropriately small reference voltage. This may be done close to ground or the positive supply rail. Direct sensor interfacing may eliminate the need for an amplifier for the sensor signal. Eliminating the amplifier can save cost, space, and design time.

2.0 Low Voltage Operation

Comparators are the common devices by which analog signals interface with digital circuits. The LMC7211 has been designed to operate at supply voltages of 2.7V without sacrificing performance to meet the demands of 3V digital systems.

At supply voltages of 2.7V, the common-mode voltage range extends 200 mV (guaranteed) below the negative supply. This feature, in addition to the comparator being able to sense signals near the positive rail, is extremely useful in low voltage applications.



TL/H/12337–5

FIGURE 1. Even at Low-Supply Voltage of 2.7V, an Input Signal which Exceeds the Supply Voltages Produces No Phase Inversion at the Output

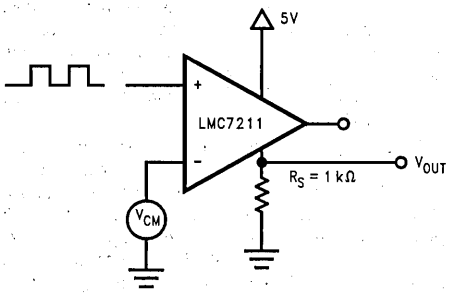
At V^+ = 2.7V propagation delays are t_{PLH} = 4 μs and t_{PHL} = 4 μs with overdrives of 100 mV.

Please refer to the performance curves for more extensive characterization.

Application Information (Continued)

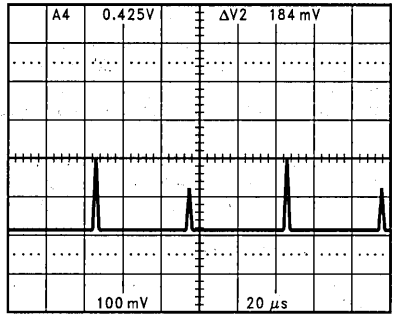
3.0 Shoot-Through Current

The shoot-through current is defined as the current surge, above the quiescent supply current, between the positive and negative supplies of a device. The current surge occurs when the output of the device switches states. The shoot-through current results in glitches in the supply voltages. Usually, glitches in the supply lines are prevented by bypass capacitors. When the glitches are minimal, the value of the bypass capacitors can be reduced.



TL/H/12337-6

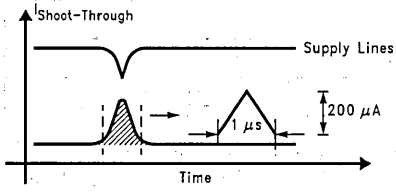
FIGURE 2. Circuit for Measurement of the Shoot-Through Current



TL/H/12337-7

FIGURE 3. Measurement of the Shoot-Through Current

From *Figure 3*, the shoot-through current for the LMC7211 can be calculated to be 0.2 mA (typical), and the duration is 1 μs. The values needed for the bypass capacitors can be calculated as follows:



TL/H/12337-8

Area of Δ = ½ (1 μs × 200 μA)
= 100 pC

The capacitor needs to supply 100 picocolumb. To avoid large shifts in the comparator threshold due to changes in the voltage level, the voltage drop at the bypass capacitor should be limited to 100 mV or less.

The charge needed (100 picocolumb) and the allowable voltage drop (100 mV) will give us the minimum capacitor value required.

$\Delta Q = C(\Delta V)$

$C = \Delta Q/\Delta V = 100$ picocolumb/100 mV

$C = 10^{-10}/10^{-1} = 10^{-9} = 1$ nF = 0.001 μF

$10^{-9} = 1$ nF = 0.001 μF

The voltage drop of ~100 mV will cause a threshold shift in the comparator. This threshold shift will be reduced by the power supply rejection ratio, (PSRR). The PSRR which is applicable here is not the DC value of PSRR (~80 dB), but a transient PSRR which will be usually about 20 dB–40 dB, depending on the circuit and the speed of the transient. This will result in an effective threshold shift of about 1 mV to 10 mV.

For precision and level sensing circuits, it is generally a good goal to reduce the voltage delta on the power supply to a value equal to or less than the hysteresis of the comparator circuit. If the above circuit was to be used with 50 mV of hysteresis, it would be reasonable to increase the bypass capacitor to 0.01 μF to reduce the voltage delta to 10 mV. Larger values may be useful for obtaining more accurate and consistent switching.

Note that the switching current of the comparator can spread to other parts of the board as noise. The bypass capacitor reduces this noise. For low noise systems this may be reason to make the capacitor larger.

For non-precision circuits, such as using a comparator to determine if a push-button switch is on or off, it is often cheaper and easier to use a larger value of hysteresis and a small value or bypass capacitance. The low shoot-through current of the LMC7211 can allow the use of smaller and less expensive bypass capacitors in non-critical circuits.

4.0 Output Short Circuit Current

The LMC7211 has short circuit protection of 40 mA. However, it is not designed to withstand continuous short circuits, transient voltage or current spikes, or shorts to any voltage beyond the supplies. A resistor in series with the output should reduce the effect of shorts. For outputs which send signals off PC boards additional protection devices, such as diodes to the supply rails, and varistors may be used.

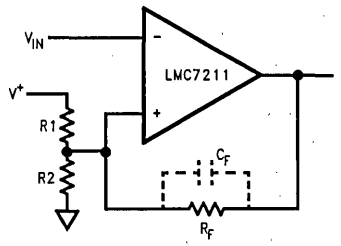
5.0 Hysteresis

If the input signal is very slow or very noisy, the comparator output might trip several times as the input signal passes through the threshold. Using positive feedback to add hysteresis to the switching can reduce or eliminate this problem. The positive feedback can be added by a high value resistor (R_F). This will result in two switching thresholds, one for increasing signals and one for decreasing signals. A capacitor can be added across R_F to increase the switching speed and provide more short term hysteresis. This can result in greater noise immunity for the circuit.

See *Figures 4, 5* and *6*.

Application Information (Continued)

Note that very heavy loading of the comparator output, such as LED drive or bipolar logic gates, will change the output voltage and shift the voltage thresholds.



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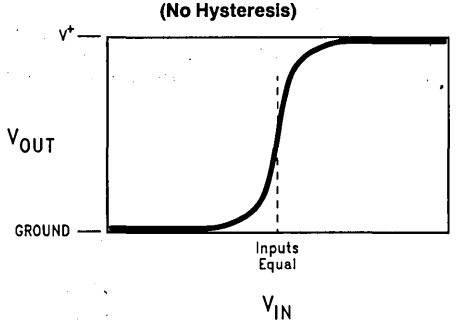
$R_F \gg R_1$ and
$R_F \gg R_2$

FIGURE 4. Positive Feedback for Hysteresis

Without Positive Feedback (No Hysteresis)



TL/H/12337–10

FIGURE 5

With Positive Feedback (Hysteresis or Memory)

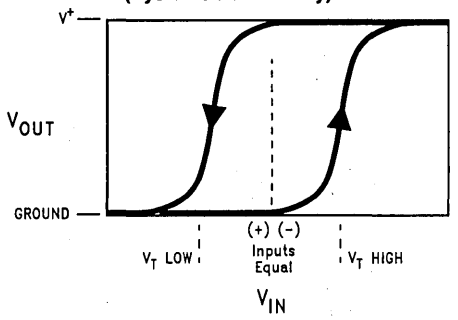


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FIGURE 6

6.0 Input Protection

If input signals are like to exceed the common mode range of the LMC7211, or it is likely that signals may be present when power is off, damage to the LMC7211 may occur. Large value (100 kΩ to MΩ) input resistors may reduce the likelihood of damage by limiting the input currents. Since the LMC7211 has very low input leakage currents, the effect on accuracy will be small. Additional protection may require the use of diodes, as shown in *Figure 7*. Note that diode leakage current may affect accuracy during normal operation. The R-C time constant of R_{IN} and the diode capacitance may also slow response time.

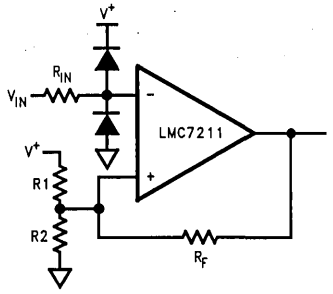

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FIGURE 7

7.0 Layout Considerations

The LMC7211 is not an especially fast comparator, so high speed design practices are not required. The LMC7211 is capable of operating with very high impedance inputs, so precautions should be taken to reduce noise pickup with high impedance (~ 100 kΩ and greater) designs and in electrically noisy environments.

Keeping high value resistors close to the LMC7211 and minimizing the size of the input nodes is a good practice. With multilayer designs, try to avoid long loops which could act as inductors (coils). Sensors which are not close to the comparator may need twisted pair or shielded connections to reduce noise.

8.0 Open Drain Output, Dual Versions

The LMC7221 is a comparator similar to the LMC7211, but with an open drain output which allows the output voltage to be different (higher or lower) than the supply voltage. The open drain output is like the open collector output of a logic gate. This makes the LMC7221 very useful for mixed voltage systems. Many systems will have different voltages for the analog and microprocessor sections. Please see the LMC7221 datasheet for details.

The performance of the LMC7211 is available in dual devices. Please see the LMC6762 datasheet for details on a dual push-pull output device. For a dual device with open drain outputs, please see the LMC6772 datasheet.

Application Information (Continued)

Rail-to-Rail Input Low Power Comparators—

Push-Pull Output

LMC7211	Tiny, SOT23-5, DIP	Single
LMC6762	SO-8, DIP	Dual

Open Drain Output

LMC7221	Tiny, SOT23-5, DIP	Single
LMC6772	SO-8, DIP	Dual

9.0 Additional SOT23-5 Tiny Devices

National Semiconductor has additional parts available in the space saving SOT23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—

LMC7101 1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain 700 μA typical current 2.7V, 3V, 5V and 15V specifications.

LMC7111 Low power 50 kHz gain-bandwidth rail-to-rail input and output amplifier with 25 μA typical current specified at 2.7V, 3.0V, 3.3V, 5V and 10V.

LM7131 Tiny Video amp with 70 MHz gain bandwidth 3V, 5V and ±5V specifications.

LP2980 Micropower SOT 50 mA Ultra Low-Dropout Regulator.

LM4040 Precision micropower shunt voltage reference. Fixed voltages of 2.500V, 4.096V, 5.000V, 8.192V and 10.000V.

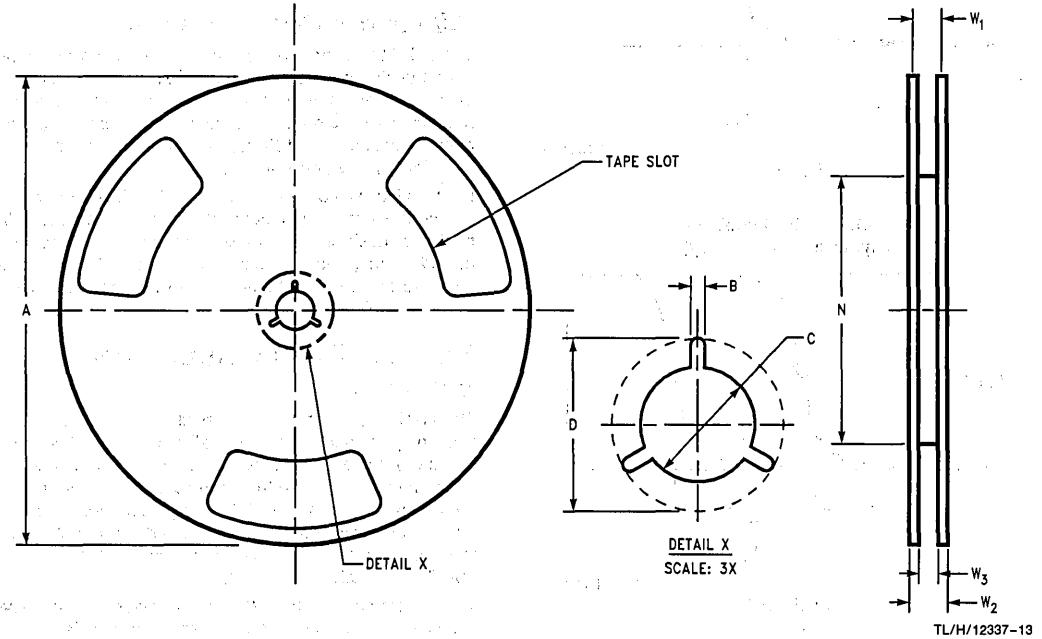
LM4041 Precision micropower shut voltage reference 1.225V and adjustable.

Contact your National Semiconductor representative for the latest information.

10.0 Spice Macromodel

A Spice Macromodel is available for the LMC7211 comparator on the National Semiconductor Amplifier Macromodel disk. Contact your National Semiconductor representative to obtain the latest version.

REEL DIMENSIONS



TL/H/12337–13

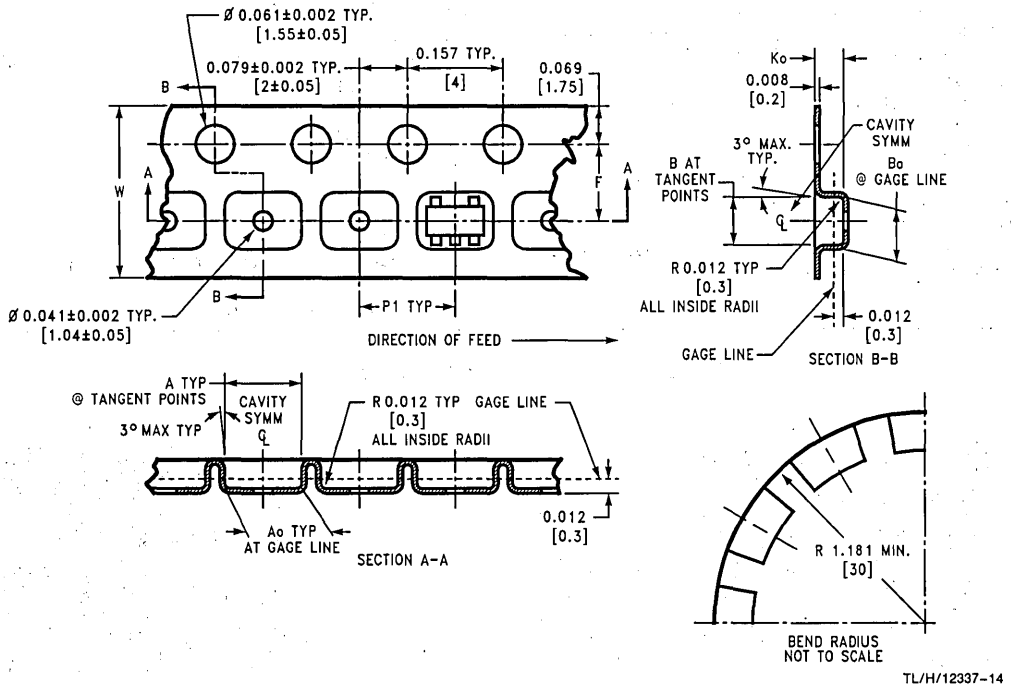
8 mm	7.00 330.00	0.059 1.50	0.512 13.00	0.795 20.20	2.165 55.00	0.331 + 0.059/−0.000 8.40 + 1.50/−0.00	0.567 14.40	W1+ 0.078/−0.039 W1 + 2.00/−1.00
Tape Size	A	B	C	D	N	W1	W2	W3

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS



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8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ±0.012 (8 ± 0.3)
Tape Size	DIM A	DIM Ao	DIM B	DIM Bo	DIM F	DIM Ko	DIM P1	DIM W

National Semiconductor

LMC6482 CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

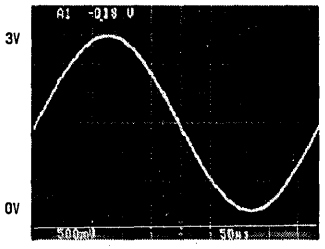
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR 82 dB
- Ultra Low Input Current 20 fA
- High Voltage Gain (R_L = 500 kΩ) 130 dB
- Specified for 2 kΩ and 600Ω loads

Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

3V Single Supply Buffer Circuit

Rail-To-Rail Input



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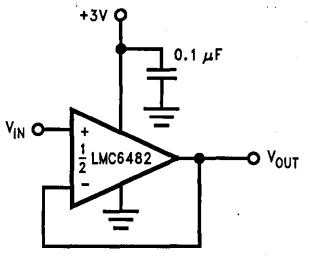

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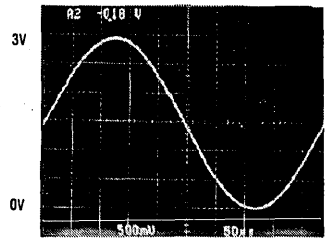
Rail-To-Rail Output



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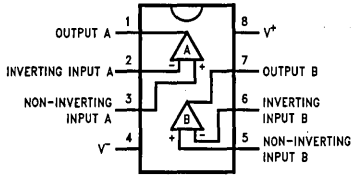
Connection Diagram



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Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6482MN	LMC6482AIN LMC6482IN	N08E	Rail
8-pin Small Outline		LMC6482AIM LMC6482IM	M08A	Rail Tape and Reel
8-pin Ceramic DIP	LMC6482AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	1.5 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V+ \le 15.5V$
Junction Temperature Range	
LMC6482AM	$-55°C \le T_J \le +125°C$
LMC6482AI, LMC6482I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	90°C/W
M Package, 8-Pin Surface Mount	155°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.11	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**10.0**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**5.0**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$ $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V, V^- = 0V$ $V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V, V^+ = 0V$ $V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V For CMRR ≥ 50 dB		$V^- - 0.3$	− 0.25 **0**	− 0.25 **0**	− 0.25 **0**	V max
				$V^+ + 0.3V$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		R_L = 600Ω (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, V_O = 5V	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, V_O = 12V (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	Both Amplifiers V^+ = +5V, V_O = $V^+/2$	1.0	1.4 **1.8**	1.4 **1.8**	1.4 **1.9**	mA max
		Both Amplifiers V^+ = 15V, V_O = $V^+/2$	1.3	1.6 **1.9**	1.6 **1.9**	1.6 **2.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{cm} = 1V	37				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.03				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01				%
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	V^- −0.25	0	0	0	V max
			V^+ + 0.25	V^+	V^+	V^+	V min
V_O	Output Swing	R_L = 2 kΩ to $V^+/2$	2.8				V
			0.2				V
		R_L = 600Ω to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	Both Amplifiers	0.825	1.2 **1.5**	1.2 **1.5**	1.2 **1.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/µs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}	0.01				%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

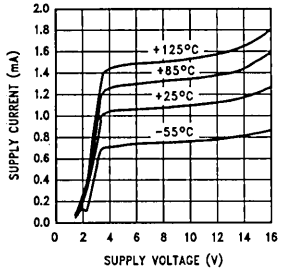
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature parameters see RETS6482X.

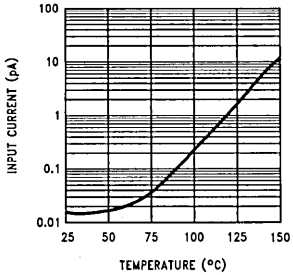
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

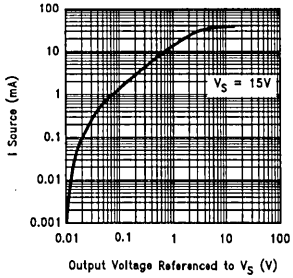
Supply Current vs Supply Voltage



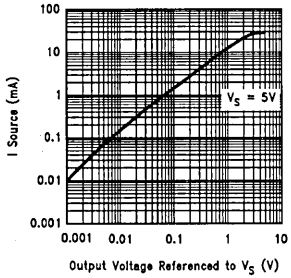
Input Current vs Temperature



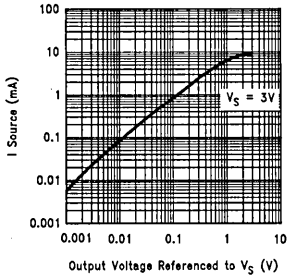
Sourcing Current vs Output Voltage



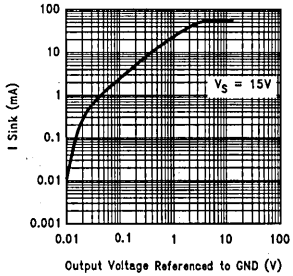
Sourcing Current vs Output Voltage



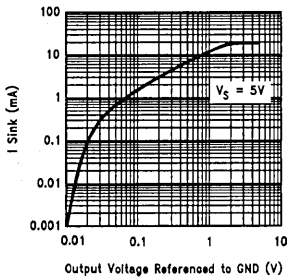
Sourcing Current vs Output Voltage



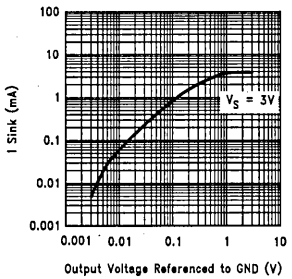
Sinking Current vs Output Voltage



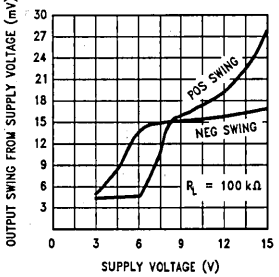
Sinking Current vs Output Voltage



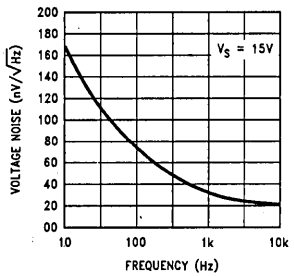
Sinking Current vs Output Voltage



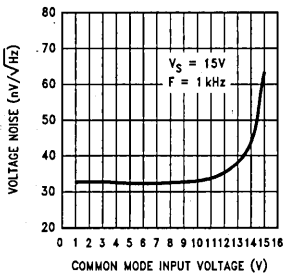
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency



Input Voltage Noise vs Input Voltage



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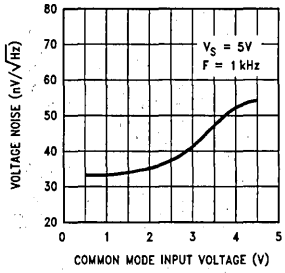
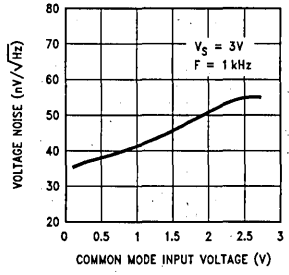
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

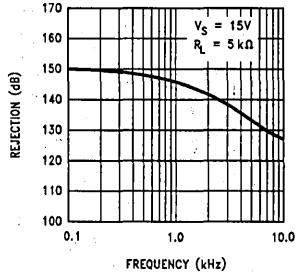
Input Voltage Noise vs Input Voltage



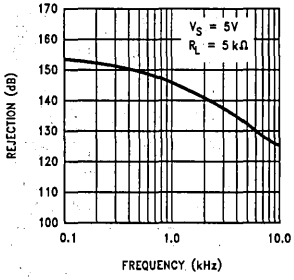
Input Voltage Noise vs Input Voltage



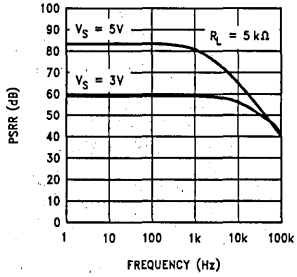
Crosstalk Rejection vs Frequency



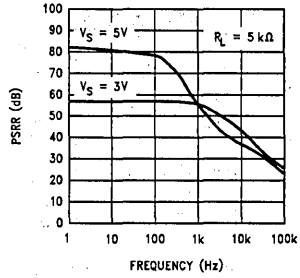
Crosstalk Rejection vs Frequency



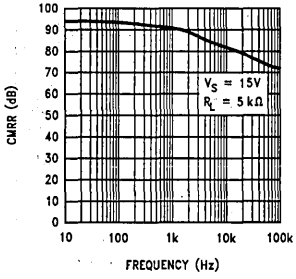
Positive PSRR vs Frequency



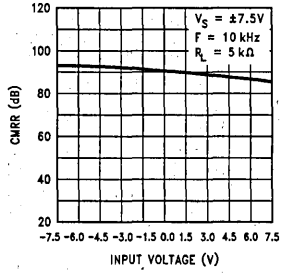
Negative PSRR vs Frequency



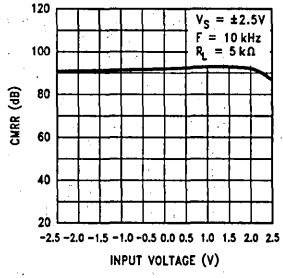
CMRR vs Frequency



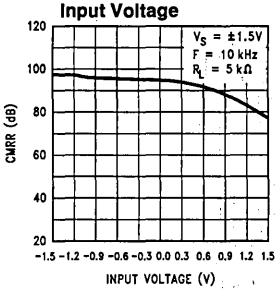
CMRR vs Input Voltage



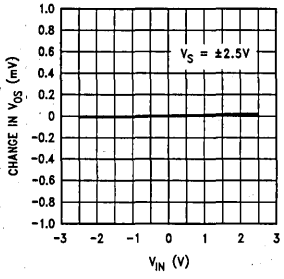
CMRR vs Input Voltage



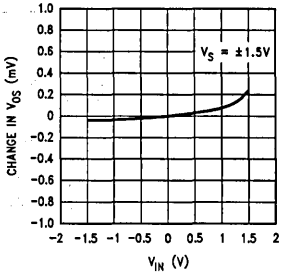
CMRR vs Input Voltage



ΔV_{OS} vs CMR



ΔV_{OS} vs CMR

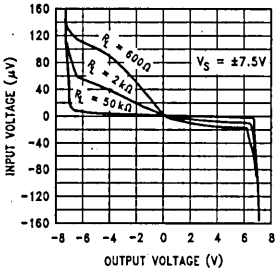


TL/H/11713–6

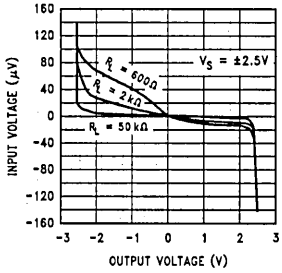
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

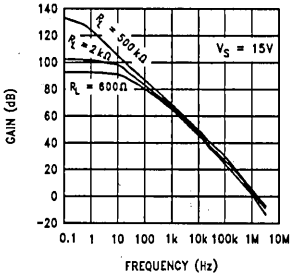
Input Voltage vs Output Voltage



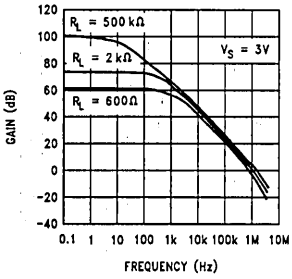
Input Voltage vs Output Voltage



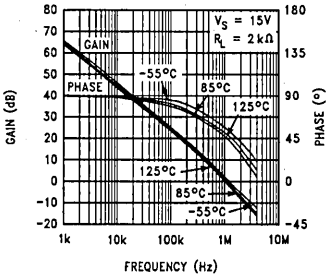
Open Loop Frequency Response



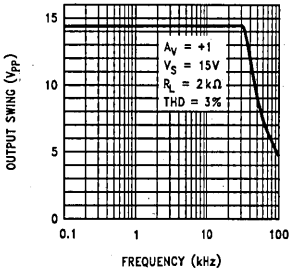
Open Loop Frequency Responce



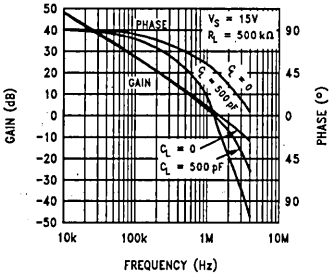
Open Loop Frequency Response vs Temperature



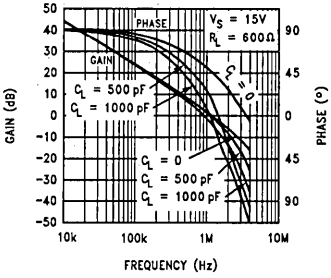
Maximum Output Swing vs Frequency



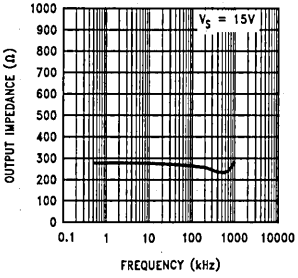
Gain and Phase vs Capacitive Load



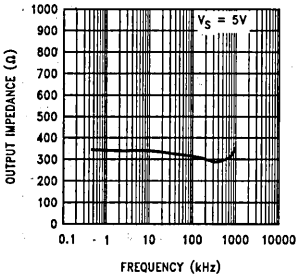
Gain and Phase vs Capacitive Load



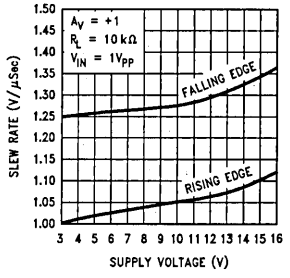
Open Loop Output Impedance vs Frequency



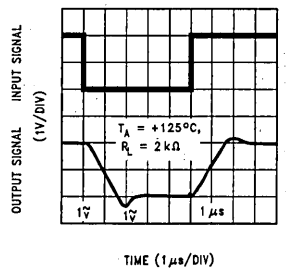
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response

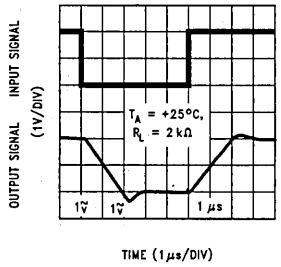


TL/H/11713–7

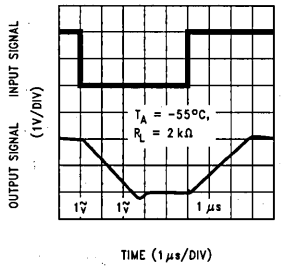
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

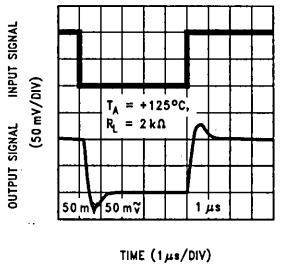
Non-Inverting Large Signal Pulse Response



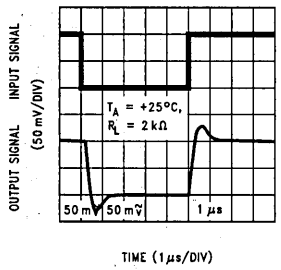
Non-Inverting Large Signal Pulse Response



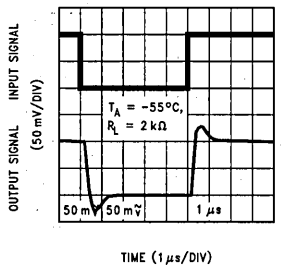
Non-Inverting Small Signal Pulse Response



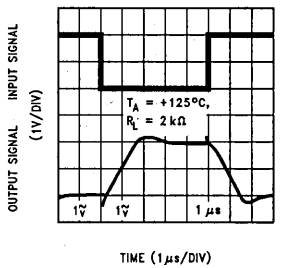
Non-Inverting Small Signal Pulse Response



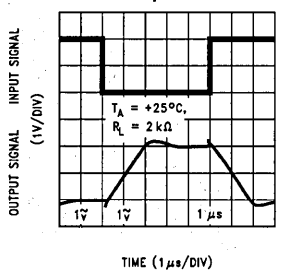
Non-Inverting Small Signal Pulse Response



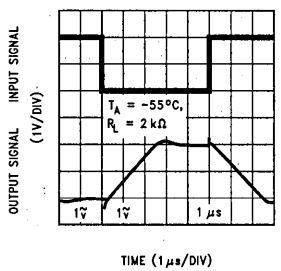
Inverting Large Signal Pulse Response



Inverting Large Signal Pulse Response



Inverting Large Signal Pulse Response



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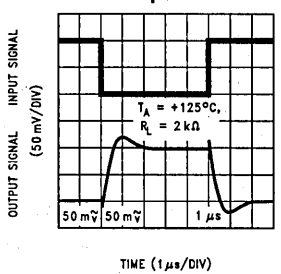

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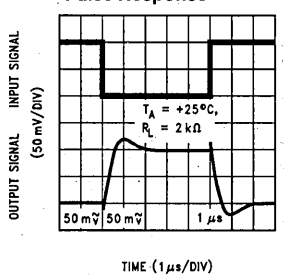
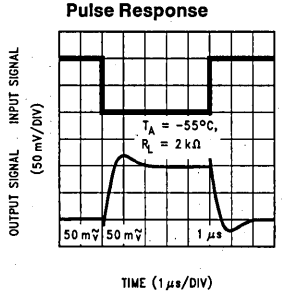
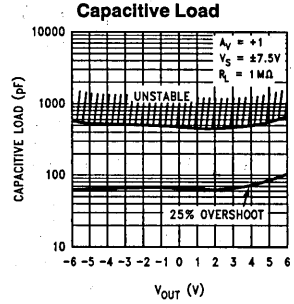


Inverting Small Signal Pulse Response



Stability vs Capacitive Load

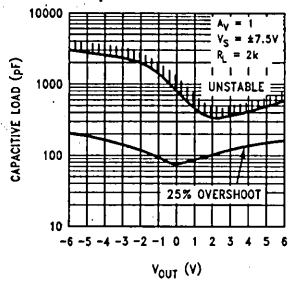


TL/H/11713–8

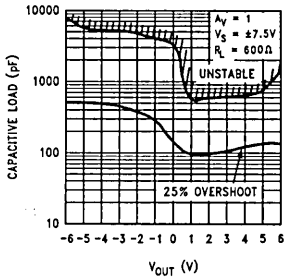
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

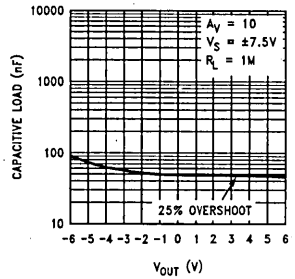
Stability vs Capacitive Load



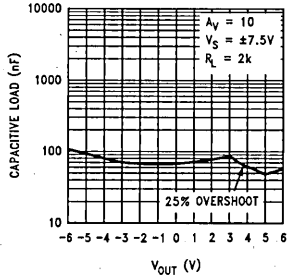
Stability vs Capacitive Load



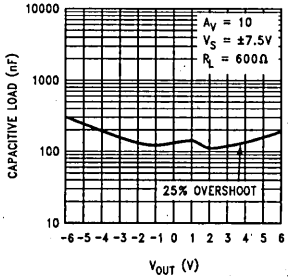
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11713–9

Application Information

1.0 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

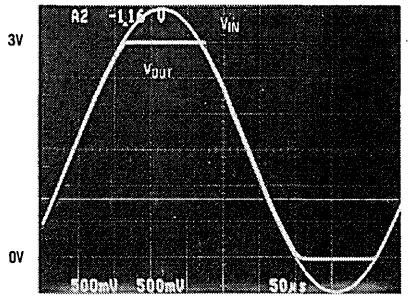


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FIGURE 1. An Input Voltage Signal Exceeds the LMC6482 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

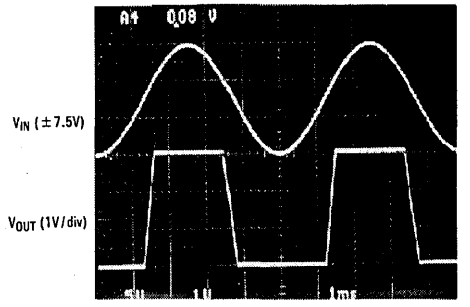

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FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in *Figure 3*.

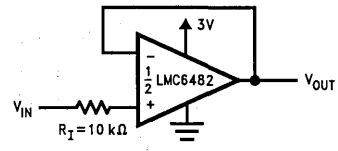

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FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

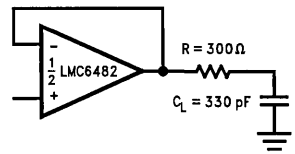
3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6482 is 180Ω sourcing and 130Ω sinking at Vs = 3V and 110Ω sourcing and 80Ω sinking at Vs = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

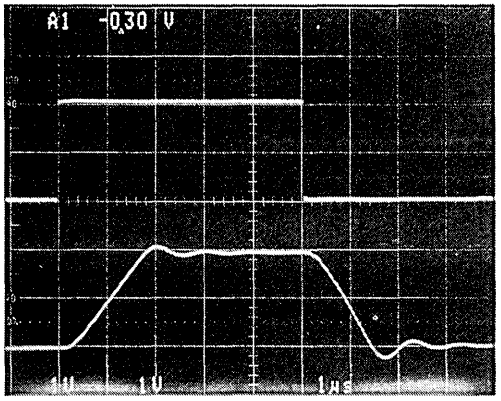
Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.



TL/H/11713–17

FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

Application Information (Continued)



TL/H/11713–18

FIGURE 5. Pulse Response of the LMC6482 Circuit in *Figure 4*

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in *Figure 6*.

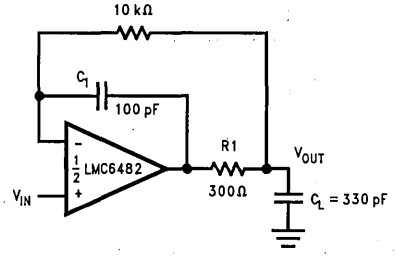


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FIGURE 6. LMC6482 Noninverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in *Figure 7*.

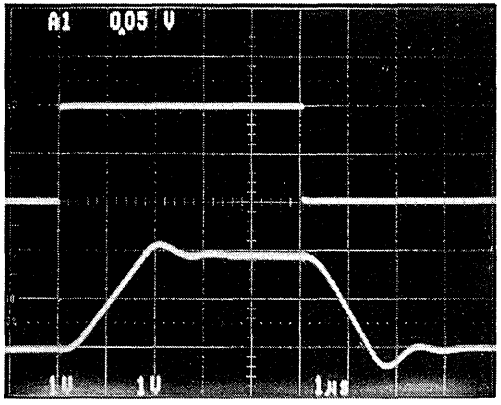

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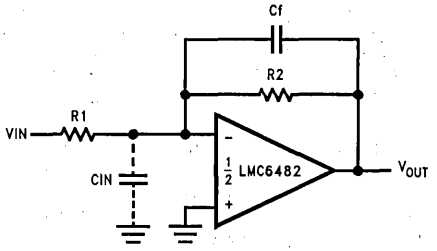
FIGURE 7. Pulse Response of LMC6482 Circuit in *Figure 6*

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.



TL/H/11713–19

FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operrate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 10a, 10b, 10c* for typical connections of guard rings for standard op-amp configurations.

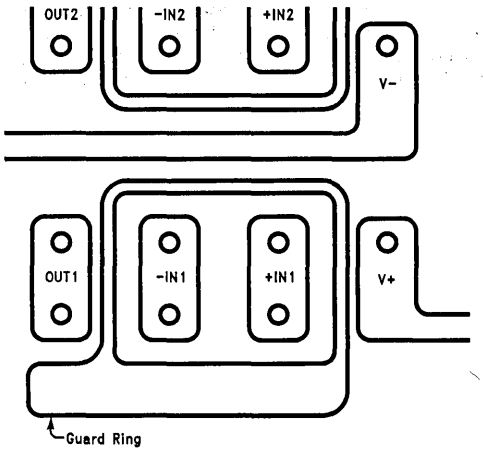


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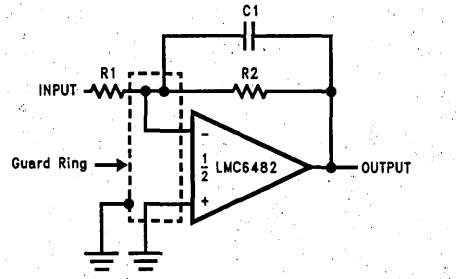
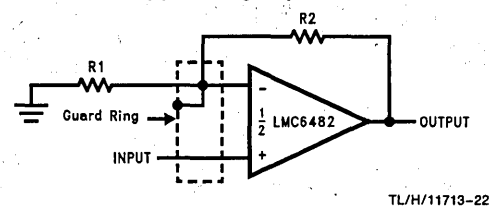
FIGURE 9. Example of Guard Ring in P.C. Board Layout



TL/H/11713-21

(a) Inverting Amplifier



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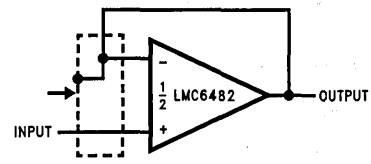
(b) Non-Inverting Amplifier

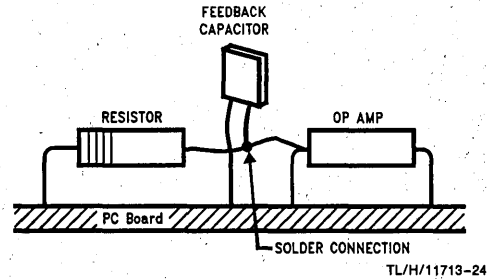


TL/H/11713-23

(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11*.



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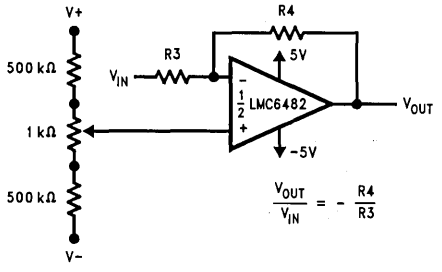
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figure 12* and *13*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5V$.



TL/H/11713-25

FIGURE 12. Inverting Configuration Offset Voltage Adjustment

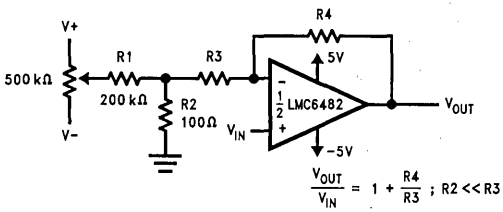


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FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

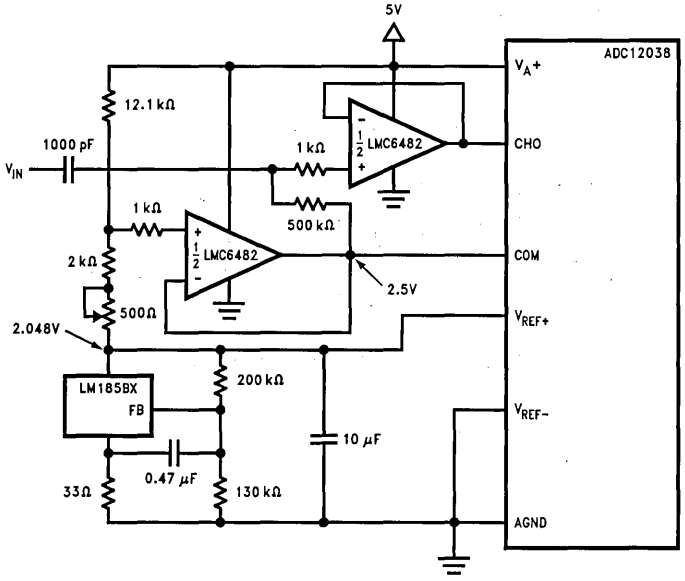
8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482's features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inverison or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 *(Figure 14)*. Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



TL/H/11713-28

FIGURE 14. Operating from the same Supply Voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy

Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based tranducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

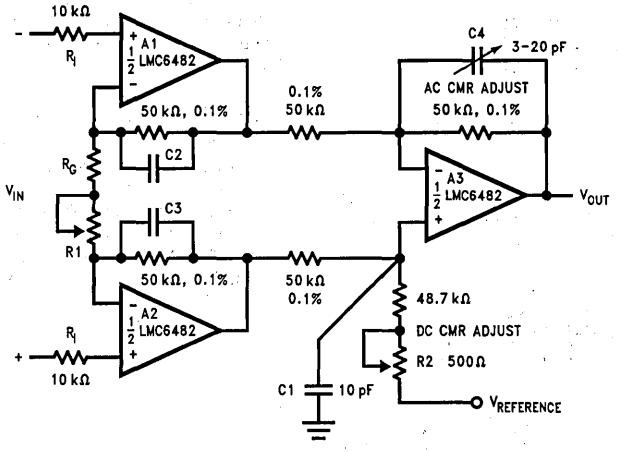


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FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

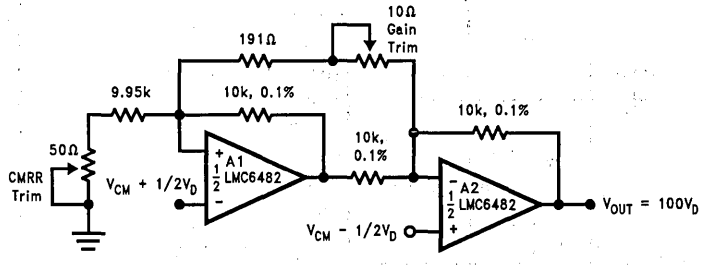

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FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

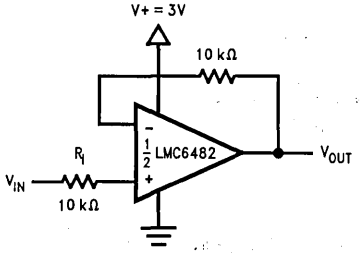

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FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)

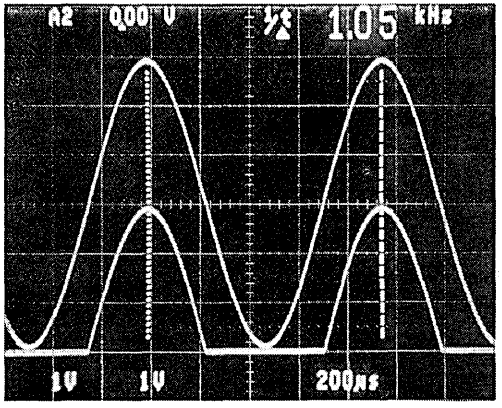

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FIGURE 17A. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 18*.

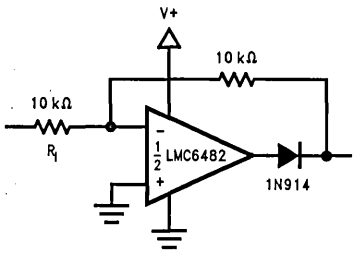

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FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)

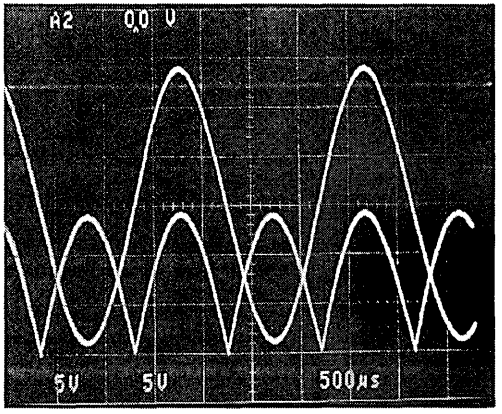

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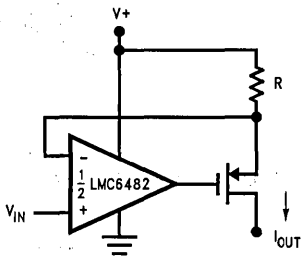
FIGURE 18A. Full Wave Rectifier Waveform



$$I_{OUT} = \left(\frac{V+ - V_{IN}}{R}\right)$$

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FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications

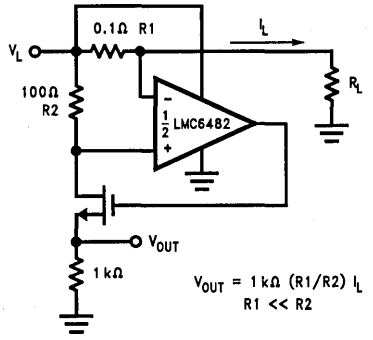

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FIGURE 20. Positive Supply Current Sense

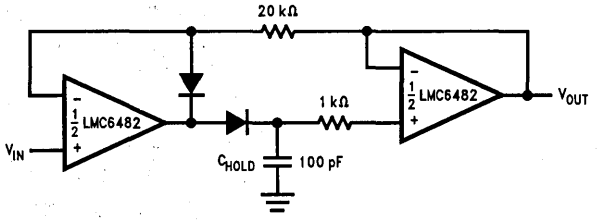

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FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In *Figure 21* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

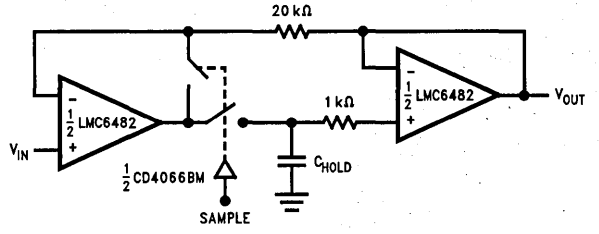

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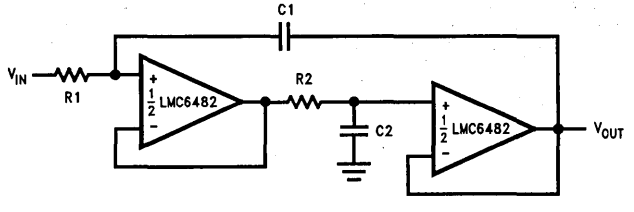
FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6482's high CMRR (82 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



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$$R1 = R2,\ C1 = C2;\ f = \frac{1}{2\pi R1\ C1};\ DF = \tfrac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 23* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

National Semiconductor

LMC6484 CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

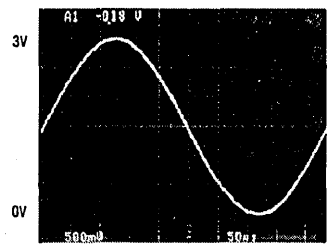
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR 82 dB
- Ultra Low Input Current 20 fA
- High Voltage Gain (R_L = 500 kΩ) 130 dB
- Specified for 2 kΩ and 600Ω loads

Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

3V Single Supply Buffer Circuit

Rail-to-Rail Input



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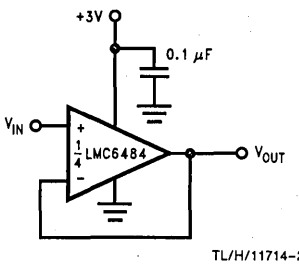

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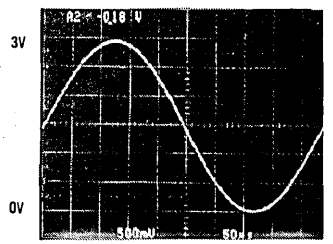
Rail-to-Rail Output



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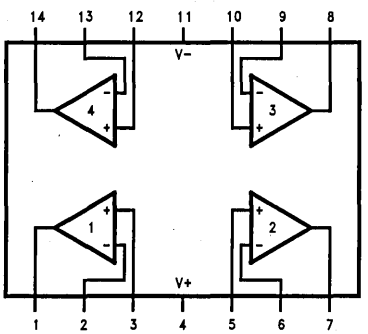
Connection Diagram



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Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
14-pin Molded DIP	LMC6484MN	LMC6484AIN LMC6484IN	N14A	Rail
14-pin Small Outline		LMC6484AIM LMC6484IM	M14A	Rail Tape and Reel
14-pin Ceramic DIP	LMC6484AMJ/883		J14A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6484AM	$-55°C \le T_J \le +125°C$
LMC6484AI, LMC6484I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 14-Pin Molded DIP	70°C/W
M Package, 14-Pin Surface Mount	110°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.110	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**100**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**50**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$, $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V$, $V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V$, $V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		$V^- - 0.3$	−0.25 **0**	−0.25 **0**	−0.25 **0**	V max
				$V^+ + 0.3$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	$R_L = 2k\Omega$ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		$R_L = 600\Omega$ (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, V_O = 5V	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, V_O = 12V (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, V_O = $V^+/2$	2.0	2.8 **3.6**	2.8 **3.6**	2.8 **3.8**	mA max
		All Four Amplifiers V^+ = +15V, V_O = $V^+/2$	2.6	3.0 **3.8**	3.0 **3.8**	3.0 **4.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484A Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	37				nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				pA/√Hz
T.H.D.	Total Harmonic Distortion	f = 1 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01				%
		f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	V^- − 0.25	0	0	0	V max
			V^+ + 0.25	V^+	V^+	V^+	V min
V_O	Output Swing	R_L = 2 kΩ to $V^+/2$	2.8				V
			0.2				V
		R_L = 600Ω to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	All Four Amplifiers	1.65	2.5 **3.0**	2.5 **3.0**	2.5 **3.2**	mA max

AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/µs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

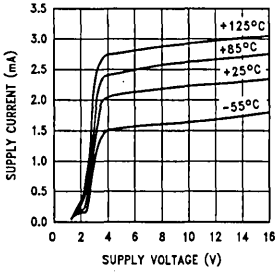
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6484X.

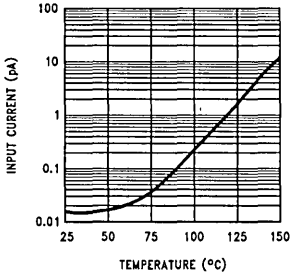
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

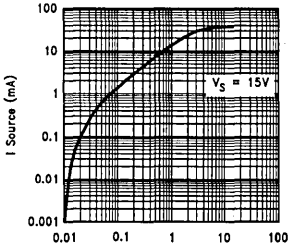
Supply Current vs Supply Voltage



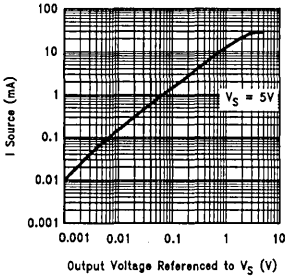
Input Current vs Temperature



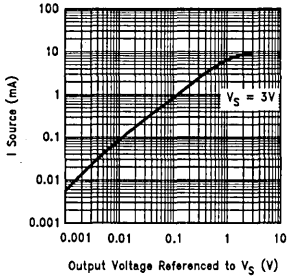
Sourcing Current vs Output Voltage



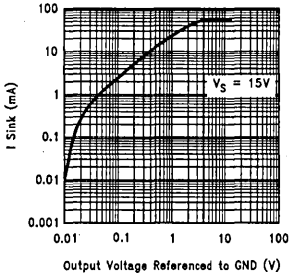
Sourcing Current vs Output Voltage



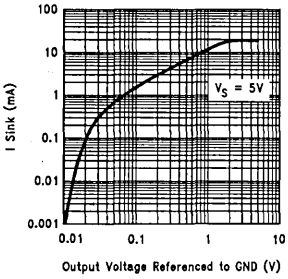
Sourcing Current vs Output Voltage



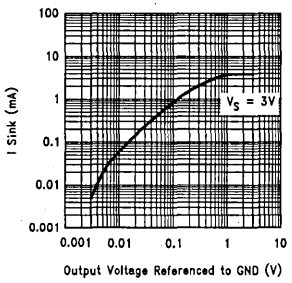
Sinking Current vs Output Voltage



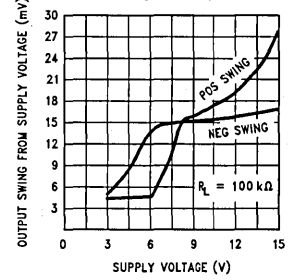
Sinking Current vs Output Voltage



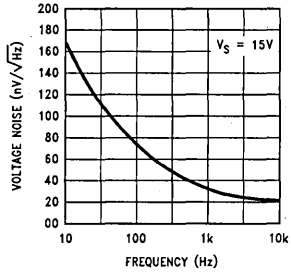
Sinking Current vs Output Voltage



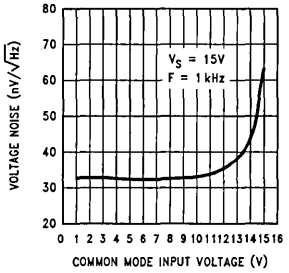
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency



Input Voltage Noise vs Input Voltage



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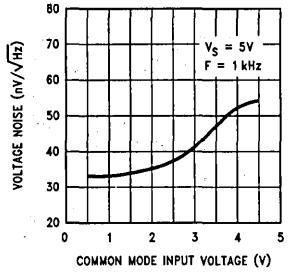
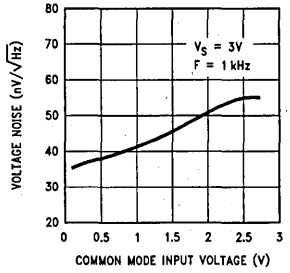
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

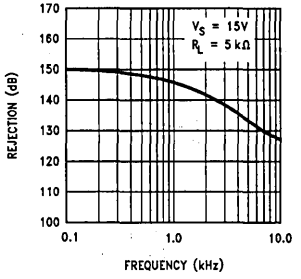
Input Voltage Noise vs Input Voltage



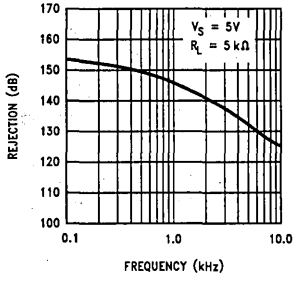
Input Voltage Noise vs Input Voltage



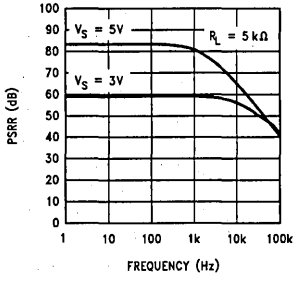
Crosstalk Rejection vs Frequency



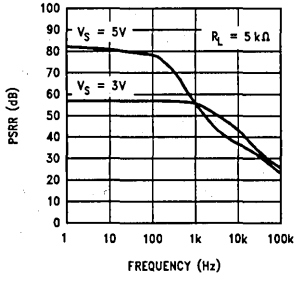
Crosstalk Rejection vs Frequency



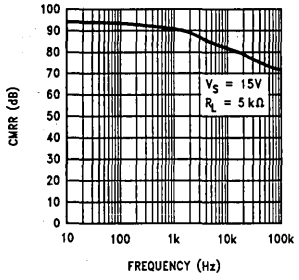
Positive PSRR vs Frequency



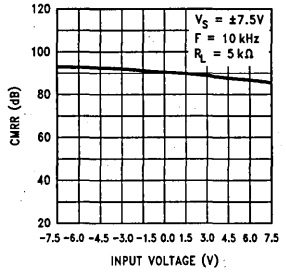
Negative PSRR vs Frequency



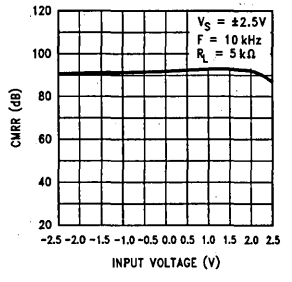
CMRR vs Frequency



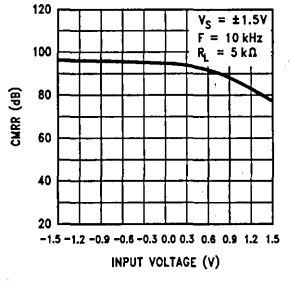
CMRR vs Input Voltage



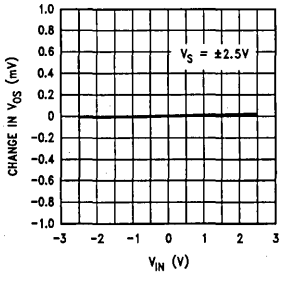
CMRR vs Input Voltage



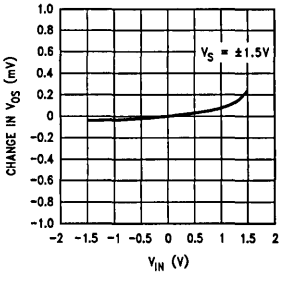
CMRR vs Input Voltage



ΔV_{OS} vs CMR



ΔV_{OS} vs CMR



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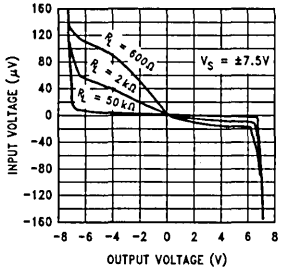
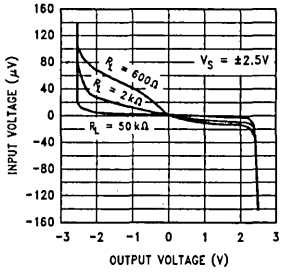
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

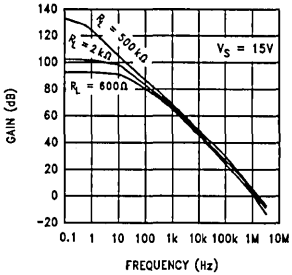
Input Voltage vs Output Voltage



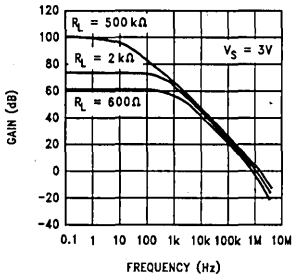
Input Voltage vs Output Voltage



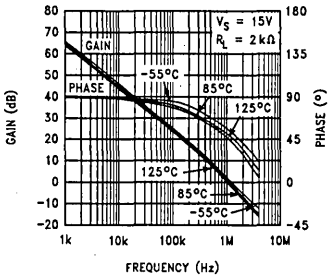
Open Loop Frequency Response



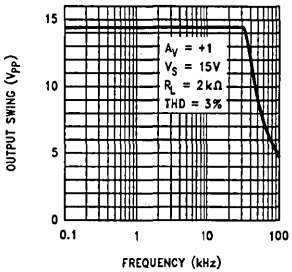
Open Loop Frequency Response



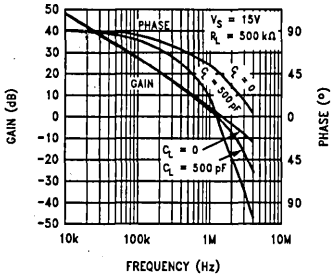
Open Loop Frequency Response vs Temperature



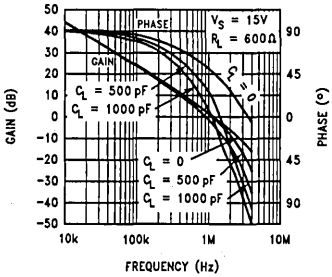
Maximum Output Swing vs Frequency



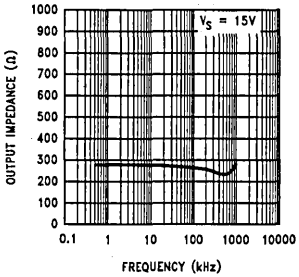
Gain and Phase vs Capacitive Load



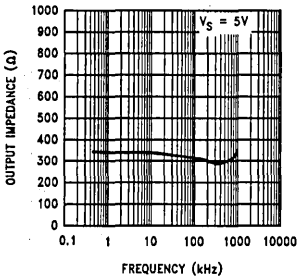
Gain and Phase vs Capacitive Load



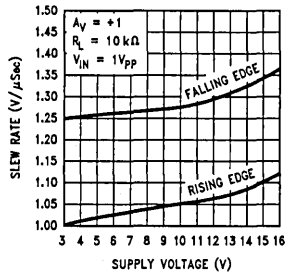
Open Loop Output Impedance vs Frequency



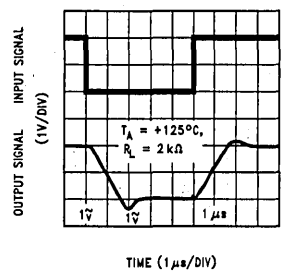
Open Loop Output Impedance vs Frequency



Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response

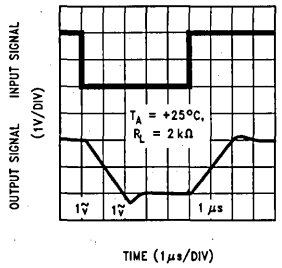


TL/H/11714–7

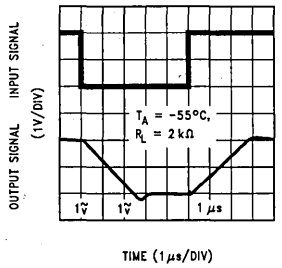
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

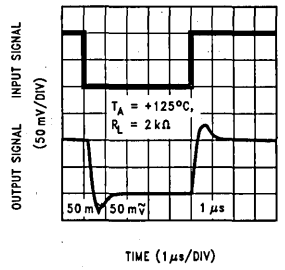
Non-Inverting Large Signal Pulse Response



Non-Inverting Large Signal Pulse Response



Non-Inverting Small Signal Pulse Response



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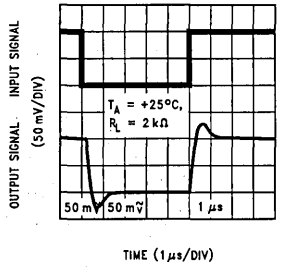
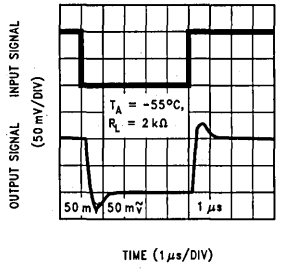
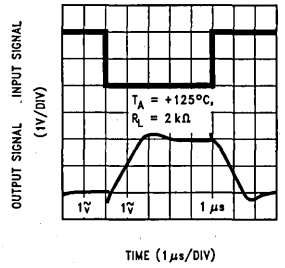


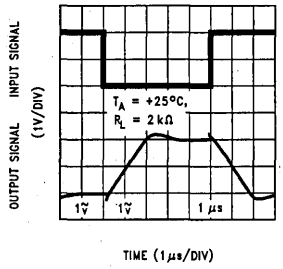
Non-Inverting Small Signal Pulse Response



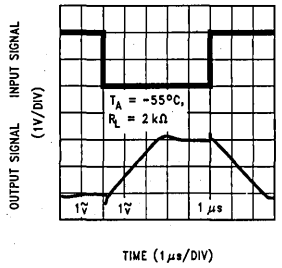
Inverting Large Signal Pulse Response



Inverting Large Signal Pulse Response



Inverting Large Signal Pulse Response



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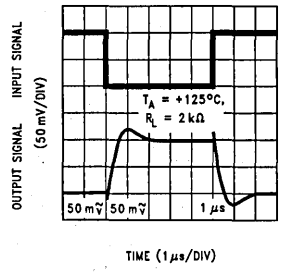
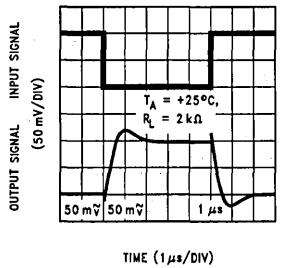
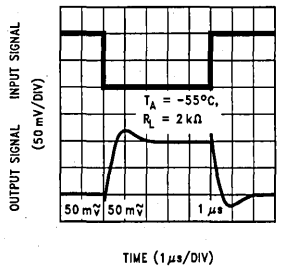


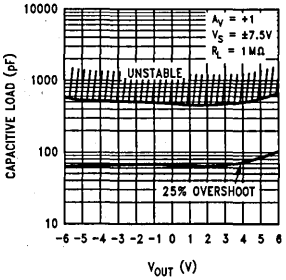
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response



Stability vs Capacitive Load

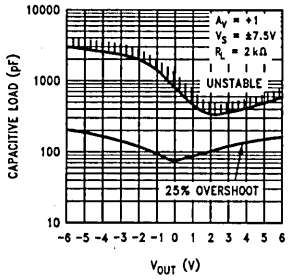


TL/H/11714–8

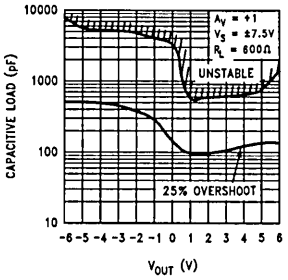
Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified (Continued)

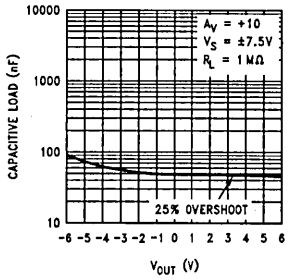
Stability vs Capacitive Load



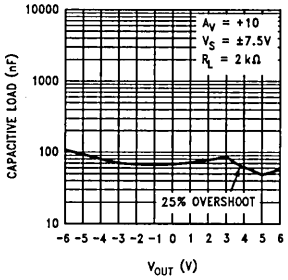
Stability vs Capacitive Load



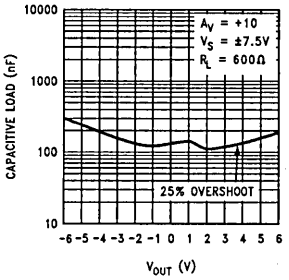
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/11714–9

Application Information (Continued)

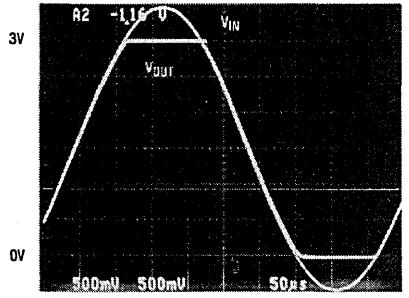
1.0 Amplifier Topology

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.



TL/H/11714–10

FIGURE 1. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

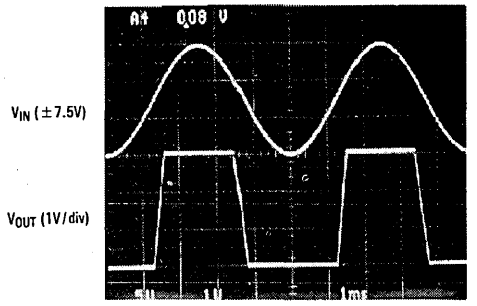


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FIGURE 2. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in *Figure 3*.

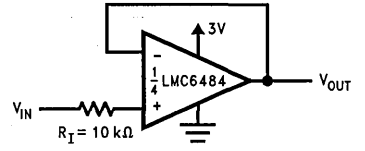

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FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6484 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 83Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6484 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

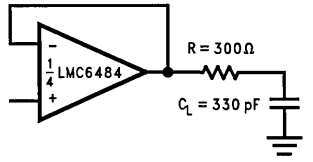

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FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

Application Information (Continued)

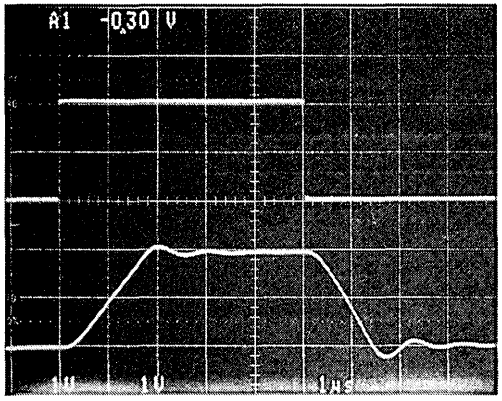

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FIGURE 5. Pulse Response of the LMC6484 Circuit in *Figure 4*

Improved frequency response is achieved by indirectly driving capacitive loads as shown in *Figure 6*.

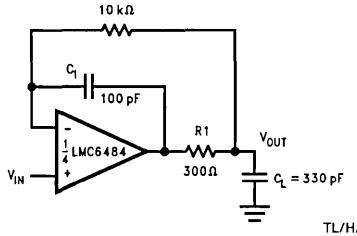

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FIGURE 6. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in *Figure 7*.

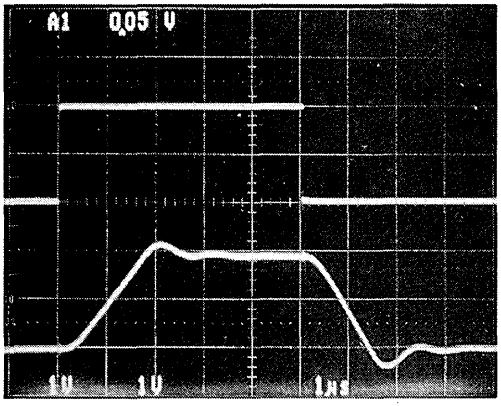

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FIGURE 7. Pulse Response of LMC6484 Circuit in *Figure 6*

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

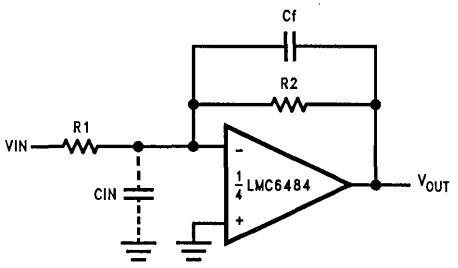

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FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 8*), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 9*. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 10a*, *10b* and *10c* for typical connections of guard rings for standard op-amp configurations.

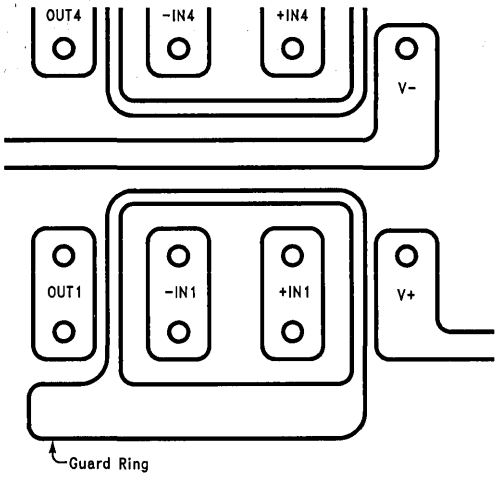

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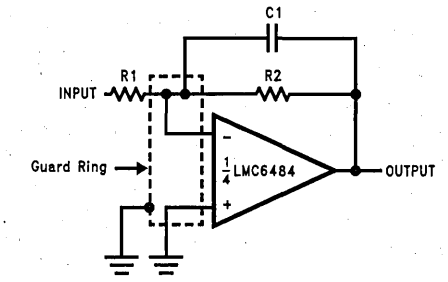
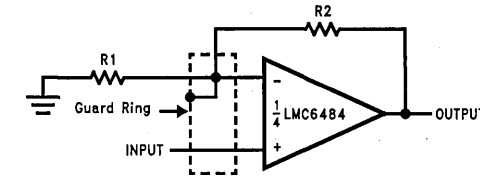
FIGURE 9. Example of Guard Ring in P.C. Board Layout



TL/H/11714-21

(a) Inverting Amplifier



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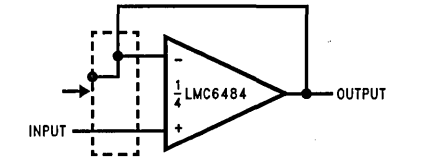
(b) Non-Inverting Amplifier



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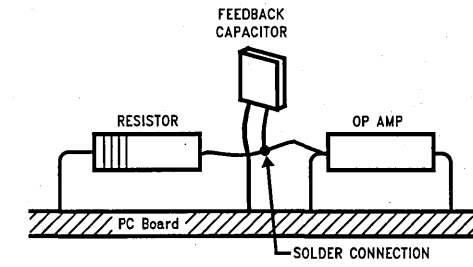
(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 11*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

Application Information (Continued)

7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figures 13* and *14*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5V$.

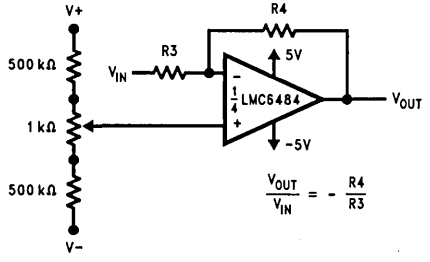

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FIGURE 12. Inverting Configuration Offset Voltage Adjustment

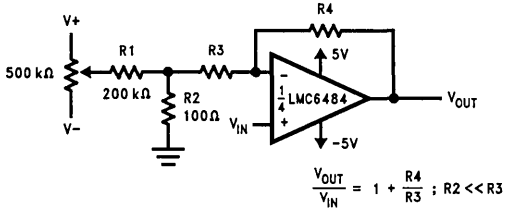

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FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6484's features. The key benefit of designing in the LMC6484 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6484 *(Figure 14)*. Capable of using the full supply range, the LMC6484 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC6484 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

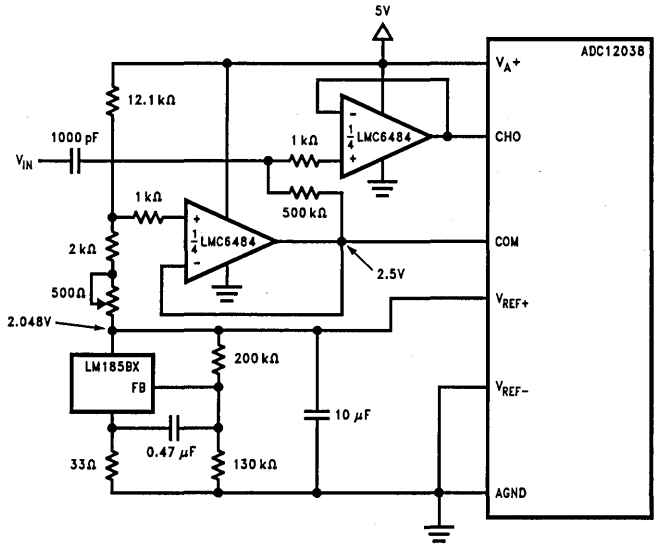

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FIGURE 14. Operating from the same Supply Voltage, the LMC6484 buffers the ADC12038 maintaining excellent accuracy

Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6484 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6484 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6484 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with Rg to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

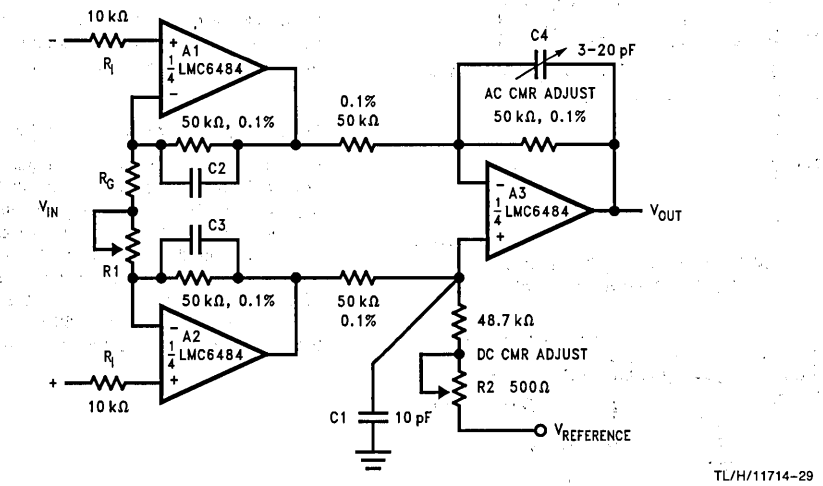


FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

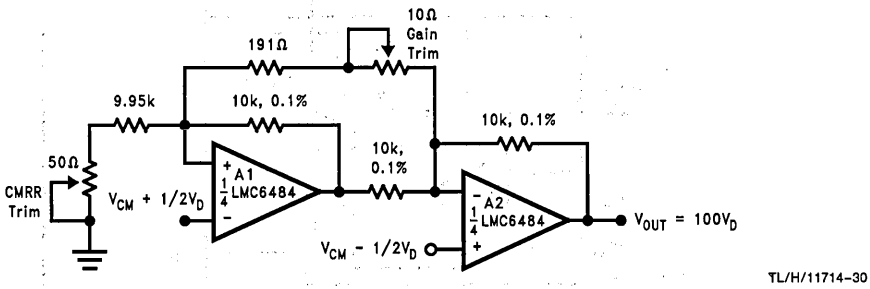


FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

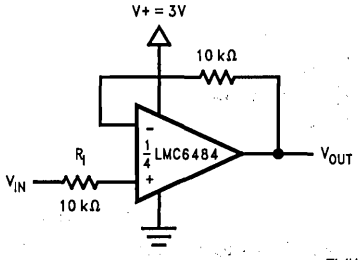
A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

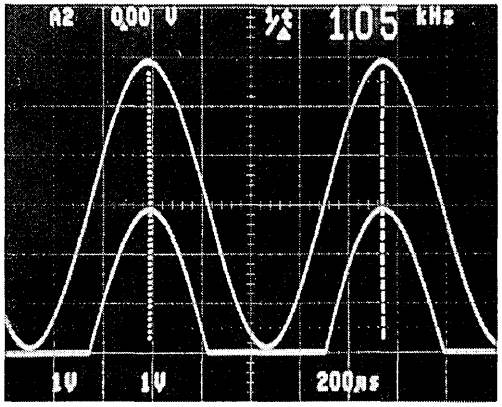
Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications



TL/H/11714–31

FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)



TL/H/11714–32

FIGURE 17a. Half-Wave Rectifier Waveform

The circuit in *Figure 17* uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in *Figure 18*.

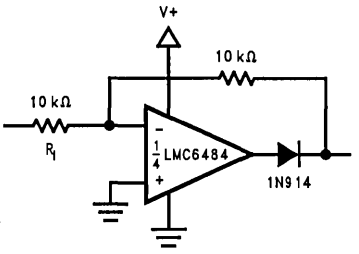


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FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)

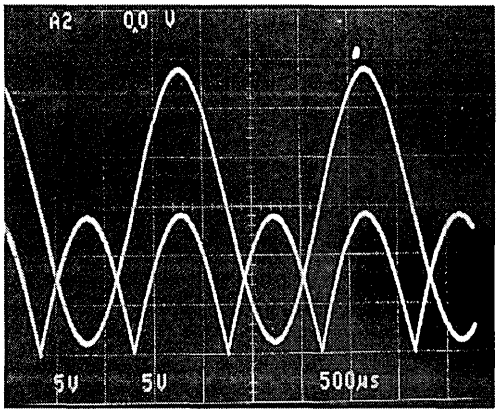

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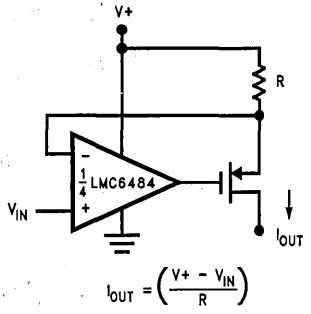
FIGURE 18a. Full Wave Rectifier Waveform



TL/H/11714–35

FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications (Continued)

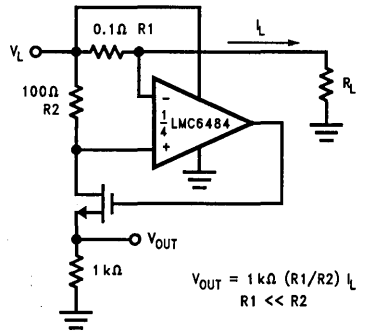


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FIGURE 20. Positive Supply Current Sense

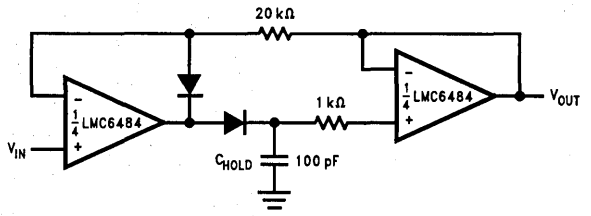

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FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In *Figure 21* dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.

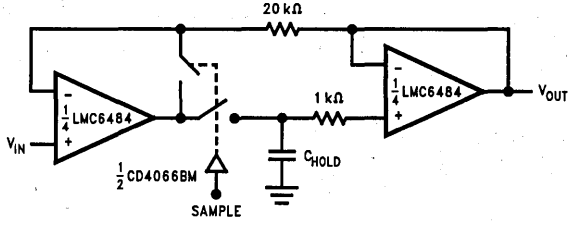

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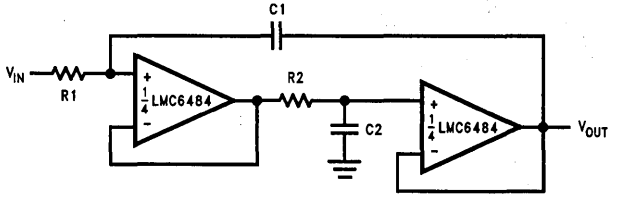
FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6484's high CMRR (85 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



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$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1C1}; DF = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in *Figure 23* can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

National Semiconductor

LM6142 Dual and LM6144 Quad High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 μA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Features At V_S = 5V. Typ unless noted.

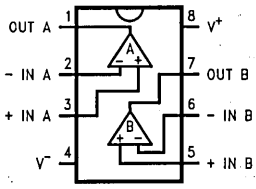
- Rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
  - Small signal, 5V/μs
  - Large signal, 30V/μs
- Low supply current 650 μA/Amplifier
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with R_L = 10k
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

Connection Diagrams

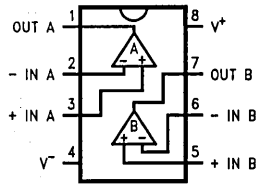
8-Pin CDIP



TL/H/12057–14

Top View

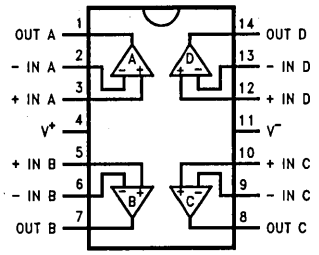
8-Pin DIP/SO



TL/H/12057–1

Top View

14-Pin DIP/SO



TL/H/12057–2

Top View

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	Temperature Range Military −55°C to +125°C	NSC Drawing
8-Pin Molded DIP	LM6142AIN, LM6142BIN		N08E
8-Pin Small Outline	LM6142AIM, LM6142BIM		M08A
14-Pin Molded DIP	LM6144AIN, LM6144BIN		N14A
14-Pin Small Outline	LM6144AIM, LM6144BIM		M14A
8-Pin CDIP		LM6142AMJ/883	D08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±25 mA
Current at Power Supply Pin	50 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V^+ \le 24V$
Junction Temperature Range	
LM6142, LM6144	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to V+/2. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.3	1.0 **2.2**	2.5 **3.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**3**			µV/°C
I_B	Input Bias Current		170	250	300	nA max
		$0V \le V_{CM} \le 5V$	180	280 **526**	**526**	nA max
I_{OS}	Input Offset Current		3	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance, C_M		126			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$	107	84 **78**	84 **78**	dB min
		$0V \le V_{CM} \le 5V$	82 **79**	66 **64**	66 **64**	dB min
PSRR	Power Supply Rejection Ratio	$5V \le V^+ \le 24V$	**87**	80 **78**	80 **78**	dB min
V_{CM}	Input Common-Mode Voltage Range		−0.25	**0**	**0**	V
			5.25	**5.0**	**5.0**	V
A_V	Large Signal Voltage Gain	$R_L = 10k$	270 **70**	100 **33**	80 **25**	V/mV min
V_O	Output Swing	$R_L = 100k$	0.005	0.01 **0.013**	0.01 **0.013**	V max
			4.995	4.98 **4.93**	4.98 **4.93**	V min
		$R_L = 10k$	0.02			V max
			4.97			V min
		$R_L = 2k$	0.06	0.1 **0.133**	0.1 **0.133**	V max
			4.90	4.86 **4.80**	4.86 **4.80**	V min

5.0V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extremes. (Continued)

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current LM6142	Sourcing	13	10 **4.9**	8 **4**	mA min
				35	**35**	mA max
		Sinking	24	10 **5.3**	10 **5.3**	mA min
				35	**35**	mA max
I_{SC}	Output Short Circuit Current LM6144	Sourcing	8	6 **3**	6 **3**	mA min
				35	**35**	mA max
		Sinking	22	8 **4**	8 **4**	mA min
				35	**35**	mA max
I_S	Supply Current	Per Amplifier	650	800 **880**	800 **880**	μA max

5.0V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V_S/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
SR	Slew Rate	8 V_{p-p} @ V_{CC} 12V $R_S > 1\ k\Omega$	25	15 **13**	13 **11**	V/μs min
GBW	Gain-Bandwidth Product	f = 50 kHz	17	10 **6**	10 **6**	MHz min
ϕ_m	Phase Margin		38			Deg
	Amp-to-Amp Isolation		130			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	16			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.22			$\frac{pA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	f = 10 kHz, R_L = 10 kΩ,	0.003			%

2.7V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.4	1.8 **4.3**	2.5 **4.3**	mV max
I_B	Input Bias Current		150	250 **526**	300 **526**	nA max
I_{OS}	Input Offset Current		4	30 **80**	30 **80**	nA max
R_{IN}	Input Resistance		128			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	90			dB min
		0V ≤ V_{CM} ≤ 2.7V	76			
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	79			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			2.95	2.7	2.7	V max
A_V	Large Signal Voltage Gain	R_L = 10k	55			V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.019	0.08 **0.112**	0.08 **0.112**	V max
			2.67	2.66 **2.25**	2.66 **2.25**	V min
I_S	Supply Current	Per Amplifier	510	800 **880**	800 **880**	μA max

2.7V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
GBW	Gain-Bandwidth Product	f = 50 kHz	9			MHz
ϕ_m	Phase Margin		36			Deg
G_m	Gain Margin		6			dB

24V Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V^+ = 24V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1.3	2 **4.8**	3.8 **4.8**	mV max
I_B	Input Bias Current		174			nA max
I_{OS}	Input Offset Current		5			nA max
R_{IN}	Input Resistance		288			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 23V	114			dB min
		0V ≤ V_{CM} ≤ 24V	100			
PSRR	Power Supply Rejection Ratio	0V ≤ V_{CM} ≤ 24V	87			
V_{CM}	Input Common-Mode Voltage Range		−0.25	0	0	V min
			24.25	24	24	V max
A_V	Large Signal Voltage Gain	R_L = 10k	500			V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.15 **0.185**	0.15 **0.185**	V max
			23.85	23.81 **23.62**	23.81 **23.62**	V min
I_S	Supply Current	Per Amplifier	750	1100 **1150**	1100 **1150**	μA max
GBW	Gain-Bandwidth Product	f = 50 kHz	18			MHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Charactenstics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

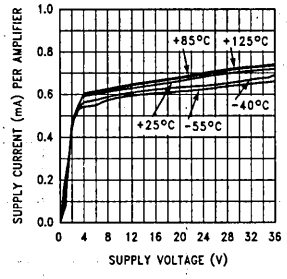
Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

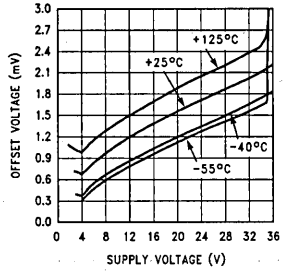
Note 7: For guaranteed military specifications see military datasheet MNLM6142AM-X.

Typical Performance Characteristics $T_A = 25°C$, $R_L = 10\ k\Omega$ Unless Otherwise Specified

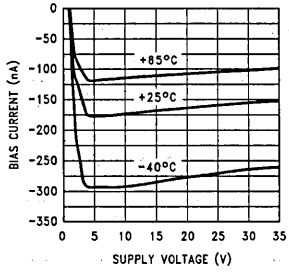
Supply Current vs Supply Voltage



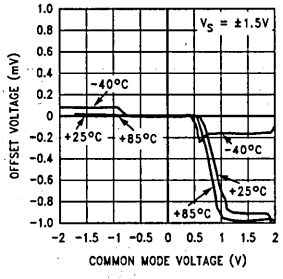
Offset Voltage vs Supply Voltage



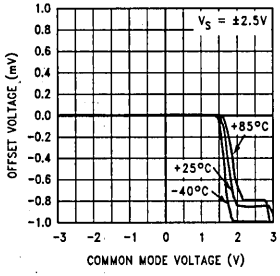
Bias Current vs Supply Voltage



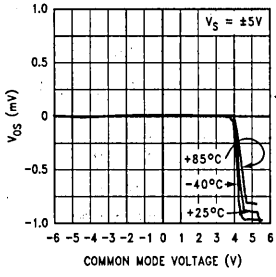
Offset Voltage vs V_{CM}



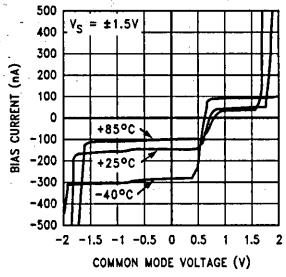
Offset Voltage vs V_{CM}



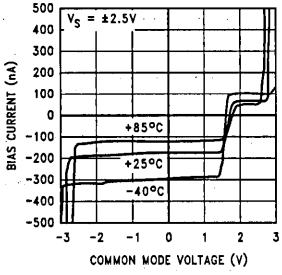
Offset Voltage vs V_{CM}



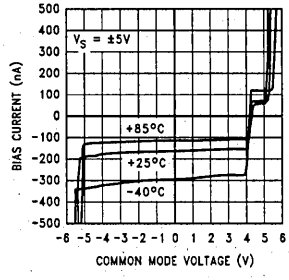
Bias Current vs V_{CM}



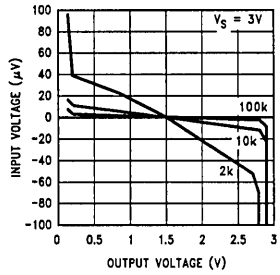
Bias Current vs V_{CM}



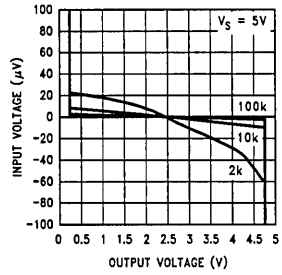
Bias Current vs V_{CM}



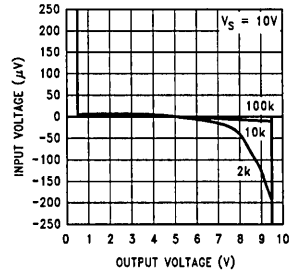
Open-Loop Transfer Function



Open-Loop Transfer Function



Open-Loop Transfer Function

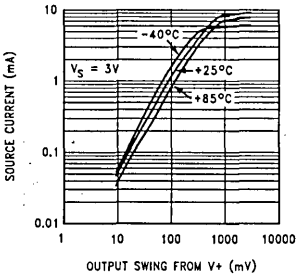


TL/H/12057–3

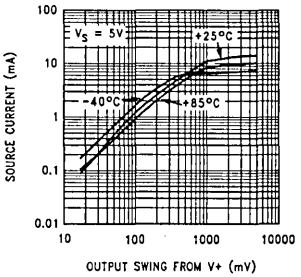
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified (Continued)

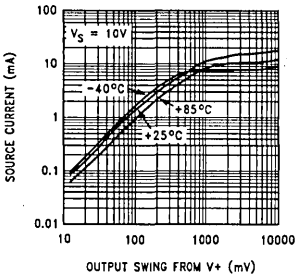
Output Voltage vs Source Current



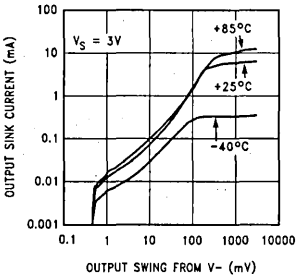
Output Voltage vs Source Current



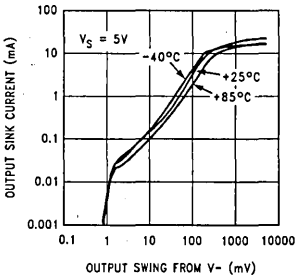
Output Voltage vs Source Current



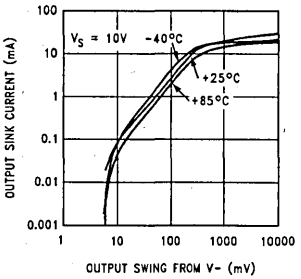
Output Voltage vs Sink Current



Output Voltage vs Sink Current

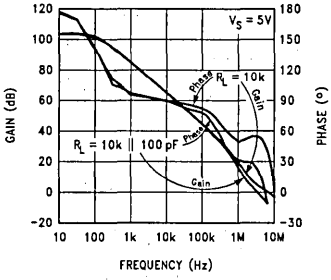


Output Voltage vs Sink Current

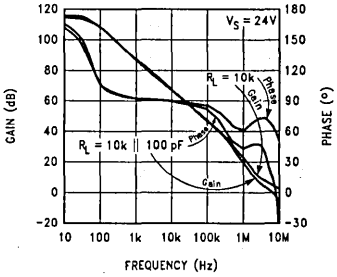


TL/H/12057–4

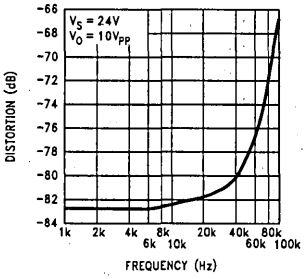
Gain and Phase vs Load



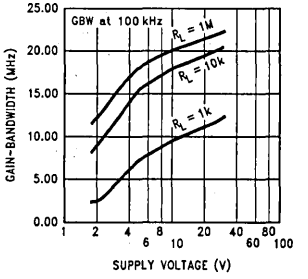
Gain and Phase vs Load



Distortion + Noise vs Frequency



GBW vs Supply

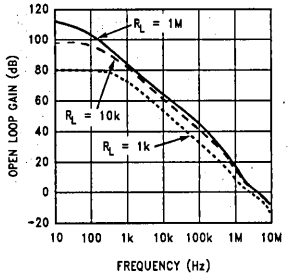


TL/H/12057–11

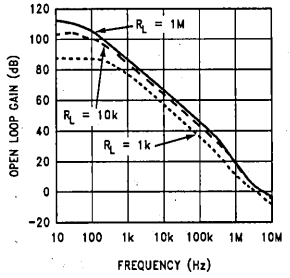
Typical Performance Characteristics

T_A = 25°C, R_L = 10 kΩ Unless Otherwise Specified (Continued)

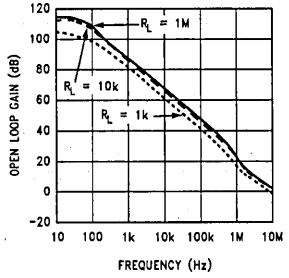
Open Loop Gain vs Load, 3V Supply



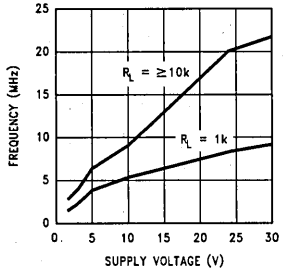
Open Loop Gain vs Load, 5V Supply



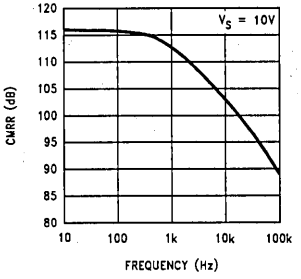
Open Loop Gain vs Load, 24V Supply



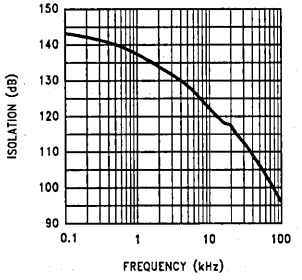
Unity Gain Freq vs V_S



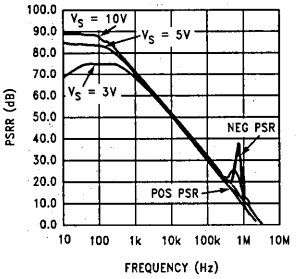
CMRR vs Frequency



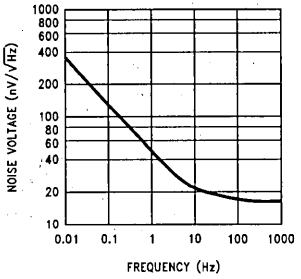
Crosstalk vs Frequency



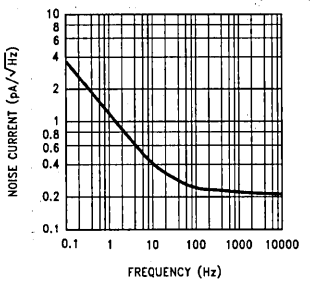
PSRR vs Frequency



Noise Voltage vs Frequency



Noise Current vs Frequency



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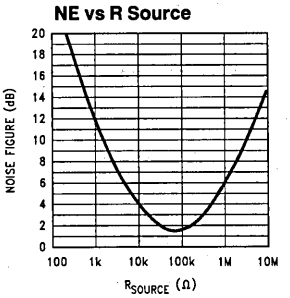
NE vs R Source



TL/H/12057–12

LM6142/44 Application Ideas

The LM6142 brings a new level of ease of use to opamp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar opamps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

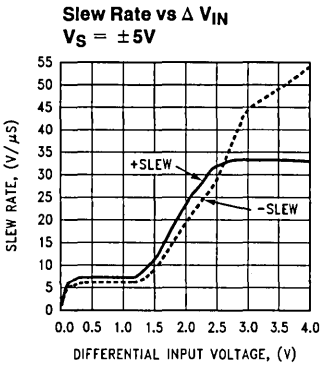
Figure 1 shows how excess input signal, is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142/44 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See *Figure 2*.)

As the overdrive increases, the opamp reacts better than a conventional opamp. Large fast pulses will raise the slew-rate to around 30V to 60V/μs.



TL/H/12057–7

FIGURE 2

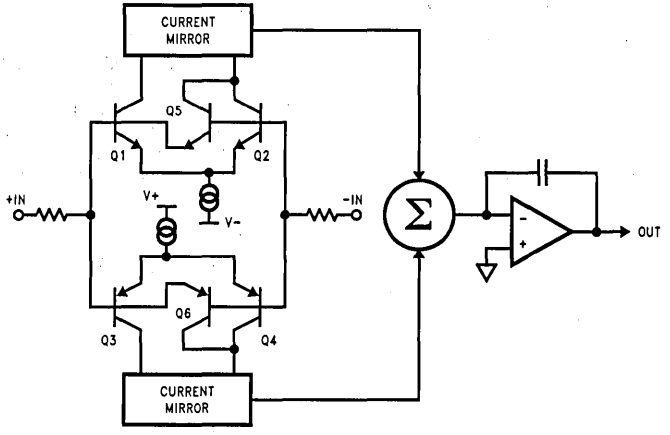
This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many opamps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all opamps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most opamps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.



TL/H/12057–6

FIGURE 1

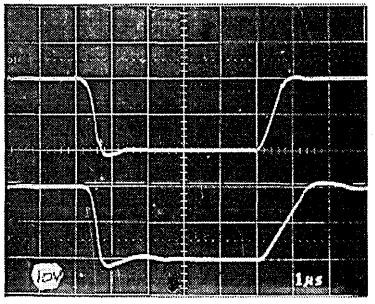
LM6142/44 Application Ideas

(Continued)

These features allow the LM6142 to drive capacitive loads as large as 1000 pF at unity gain and not oscillate. The scope photos (*Figure 3a* and *3b*) above show the LM6142 driving a l000 pF load. In *Figure 3a*, the upper trace is with no capacitive load and the lower trace is with a 1000 pF load. Here we are operating on ±12V supplies with a 20 Vp-p pulse. Excellent response is obtained with a C_f of l0 pF. In *Figure 3b*, the supplies have been reduced to ±2.5V, the pulse is 4 Vp-p and C_f is 39 pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

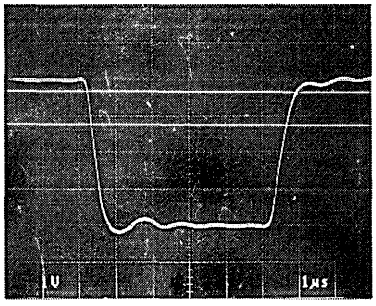
Another effect that is common to all opamps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in *Figure 4* was used for these scope photos.



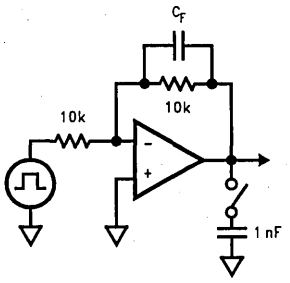
TL/H/12057–8

FIGURE 3a



TL/H/12057–9

FIGURE 3b



TL/H/12057–10

FIGURE 4

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/44 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

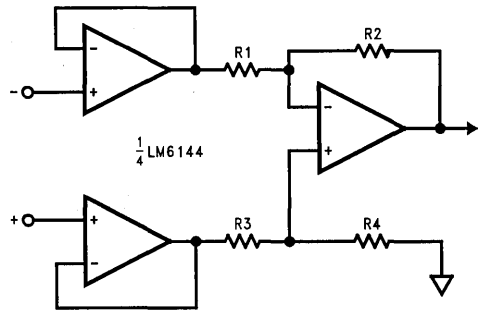
The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/44 a good choice for buffering the inputs of A to D converters.

3 OPAMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage *(Figure 5)*. These buffers assure that the input impedance is over 100 MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.



TL/H/12057–13

FIGURE 5

The gain is set by the ratio of R2/R1 and R3 should equal R1 and R4 equal R2. Making R4 slightly smaller than R2 and adding a trim pot equal to twice the difference between R2 and R4 will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor opamps is available at no charge from the NSC Customer Response Group at 800-272-9959.

National Semiconductor

MOSFET Selection Guide

SO-8 DMOS

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Configuration
		V_{GS} @10V	V_{GS} @4.5V			
N-Channel						
NDS9410	30	0.03	0.05	7.2	2.5	Single
NDS9936	30	0.05	0.08	5	2	Dual
NDS9945	60	0.1	0.2	3.5	2	Dual
NDS9955	50	0.13	0.2	3	2	Dual
NDS9956	20	0.1	0.2	3.5	2	Dual
NDS9959	50	0.3	0.5	2	2	Dual
P-Channel						
NDS9400	−20	0.25	0.4	−2.5	2.5	Single
NDS9405	−20	0.1	0.16	−4.3	2.5	Single
NDS9407	−60	0.15	0.24	−3.3	2.5	Single
NDS9430	−20	0.06	0.115	−5.3	2.5	Single
NDS9435	−30	0.07	0.13	−4.6	2.5	Single
NDS9947	−20	0.1	0.19	−3.5	2	Dual
NDS9948	−60	0.25	0.5	−2.3	2	Dual
NDS9953	−20	0.25	0.4	−2.3	2	Dual
Complementary N-P Channel						
NDS9942	20 −20	0.125 0.2	0.25 0.35	3 −2.5	2 2	N-Channel P-Channel
NDS9943	20 −20	0.125 0.16	0.25 0.3	3 −2.8	2 2	N-Channel P-Channel
NDS9952	25 −25	0.1 0.25	0.15 0.4	3 −2.3	2 2	N-Channel P-Channel
NDS9958	20 −20	0.1 0.1	0.15 0.19	3.5 −3	2 2	N-Channel P-Channel

SOT-23

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)
		V_{GS} @10V	V_{GS} @4.5V		
N-Channel					
2N7002	60	7.5		0.115	0.2
BSS123	100	6		0.17	0.36
BSS138	50	3.5	6	0.22	0.36
MMBF170	60	5		0.5	0.3
NDS7002A	60	2		0.28	0.3
P-Channel					
BSS84*	−50	10		−0.13	0.3
NDS0605	−60	5	7.5	−0.18	0.36
NDS0610	−60	10		−0.12	0.36

SOT-23 SUPERSOT™-3

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)
		V_{GS} @10V	V_{GS} @4.5V		
N-Channel					
NDS351N	30		0.25	1.1	0.5
NDS355N	30		0.125	1.6	0.5
P-Channel					
NDS352P	−20		0.5	−0.85	0.5
NDS356P	−20		0.3	−1.1	0.5

SOT-223 POWERSOT

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)
		V_{GS} @10V	V_{GS} @4.5V		
N-Channel					
NDT014	60	0.2		2.7	3
NDT451N	30	0.05	0.1	5.5	3
NDT3055	60	0.12		3.7	3
NDT3055L	60		0.15	3.5	3
P-Channel					
NDT452P	−30	0.18	0.32	−3	3
NDT2955	−60	0.3	0.5	−2.5	3

*Preliminary information, please contact Discrete POWER & Signal Technologies Marketing for updated information.

National Semiconductor

NDS351N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

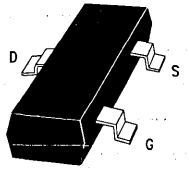
General Description

These N-channel logic level enhancement mode power field effect transistors are produced using National's proprietary high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.1A, 30V, $R_{DS(ON)}$ = 0.25Ω @ V_{GS} = 4.5V
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Compact industry standard SOT-23 surface mount package

SOT-23
(TO-236AB)



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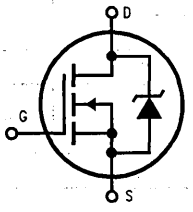

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Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS351N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage	— Continuous	±20	V
I_D	Maximum Drain Current	— Continuous	±1.1	A
		— Pulsed	±10	
P_D	Maximum Power Dissipation	@T_A = 25°C	500 (Note 1)	mW
		@T_C = 25°C	1.7 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		250 (Note 1)	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		75 (Note 1)	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250 μA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		T_J = 125°C			10	μA
I_{GSSF}	Gate—Body Leakage, Forward	V_{GS} = 12V, V_{DS} = 0V			100	nA
I_{GSSR}	Gate—Body Leakage, Reverse	V_{GS} = −12V, V_{DS} = 0V			−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.8	1.6	2	V
		T_J = 125°C	0.5	1.3	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 1.1A		0.185	0.25	Ω
		T_J = 125°C		0.26	0.37	
		V_{GS} = 10V, I_D = 1.4A		0.135	0.16	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5V, V_{DS} = 5V	5			A
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 1.1A	2	2.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1.0 MHz		140		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			18		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 50Ω		9	15	ns
t_r	Turn-On Rise Time			16	30	ns
$t_{D(OFF)}$	Turn-Off Delay Time			26	50	ns
t_f	Turn-Off Fall Time			19	40	ns
Q_g	Total Gate Charge	V_{DD} = 10V, I_D = 1.1A, V_{GS} = 5V		2	3.5	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 1.1A (Note 2)		0.8	1.2	V

Note 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. In this case, $R_{\theta CA}$ of 175°C/W can be achieved with a drain thermal pad of approximately 0.01 square inch of 2 ounce copper.

Note 2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

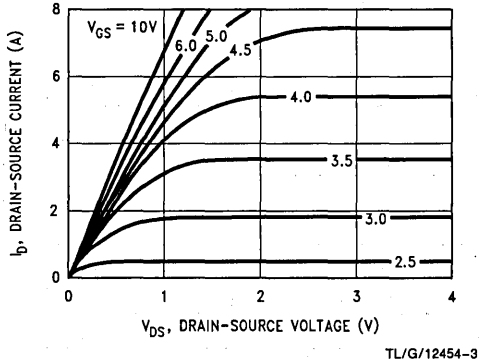

FIGURE 1. On-Region Characteristics

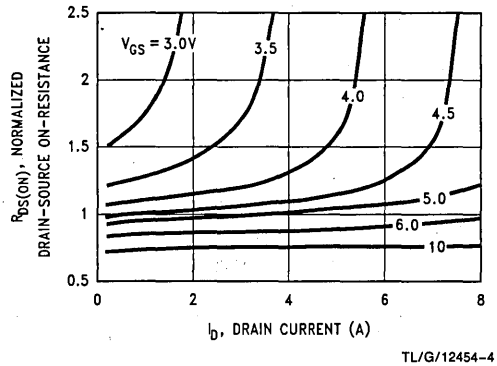

FIGURE 2. On-Resistance Variation with Gate Voltage and Drain Current

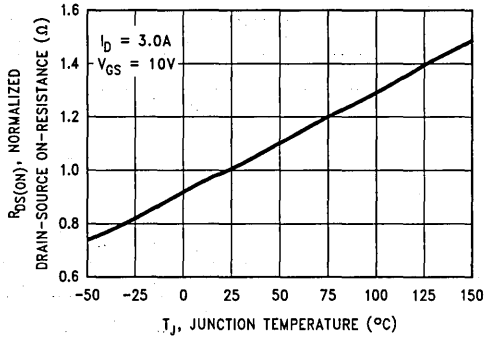

FIGURE 3. On-Resistance Variation with Temperature

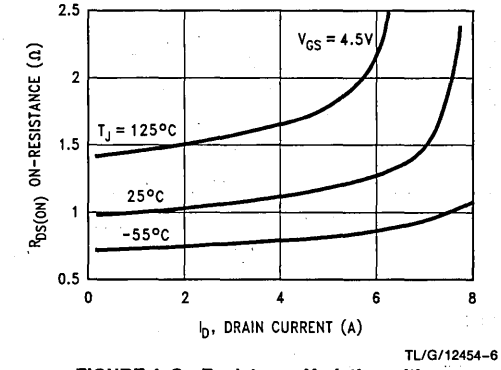

FIGURE 4. On-Resistance Variation with Drain Current and Temperature

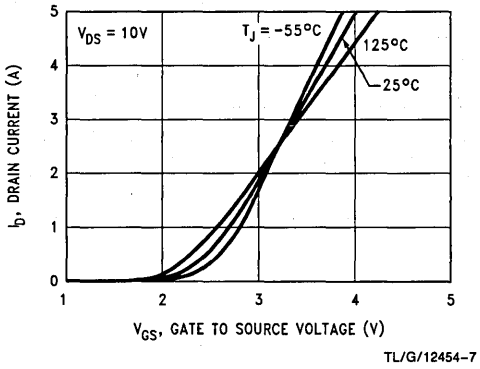

FIGURE 5. Transfer Characteristics

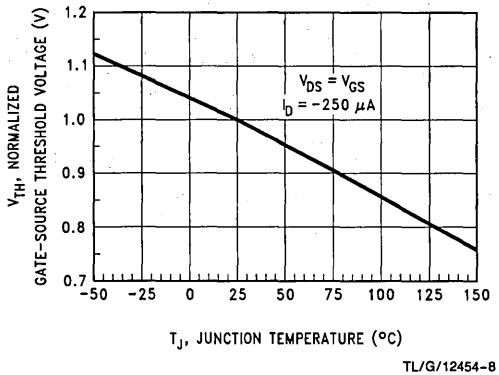

FIGURE 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (Continued)

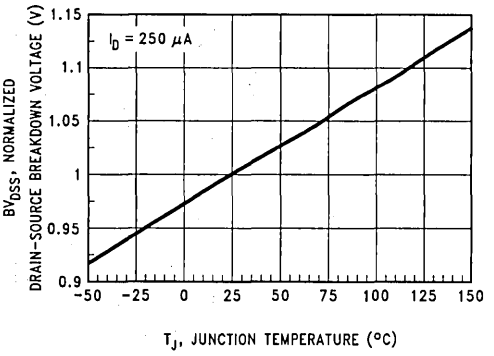

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FIGURE 7. Breakdown Voltage Variation with Temperature

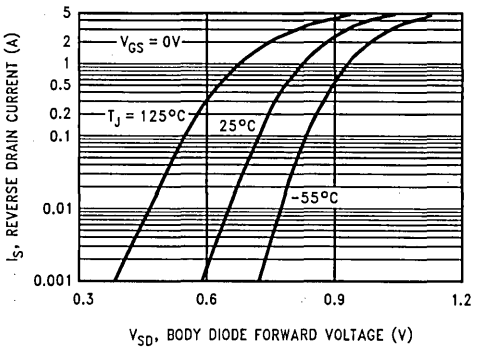

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FIGURE 8. Body Diode Forward Voltage Variation with Current and Temperature

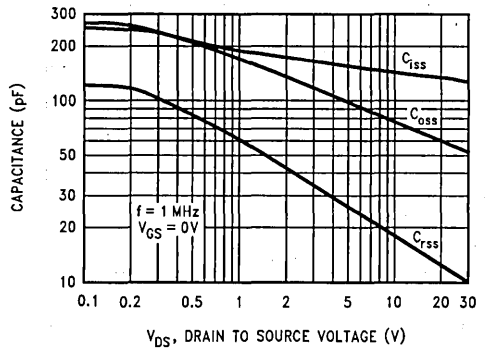

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FIGURE 9. Capacitance Characteristics

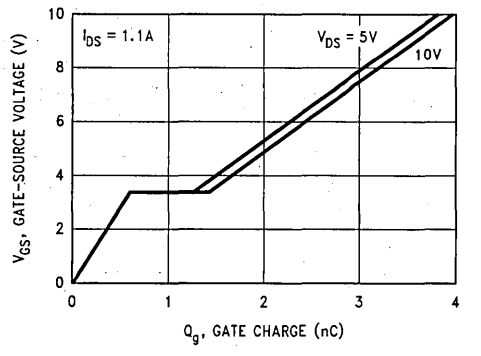

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FIGURE 10. Gate Charge Characteristics

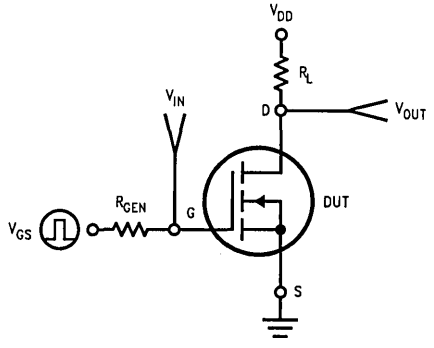

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FIGURE 11. Switching Test Circuit

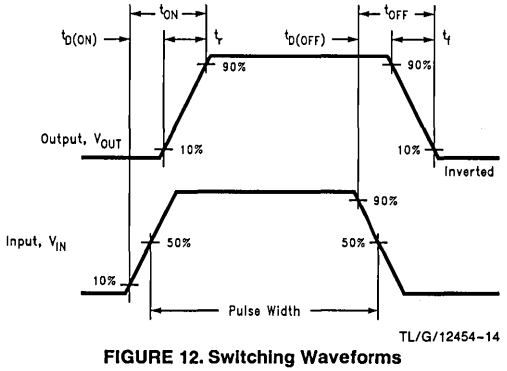

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FIGURE 12. Switching Waveforms

Typical Electrical Characteristics (Continued)

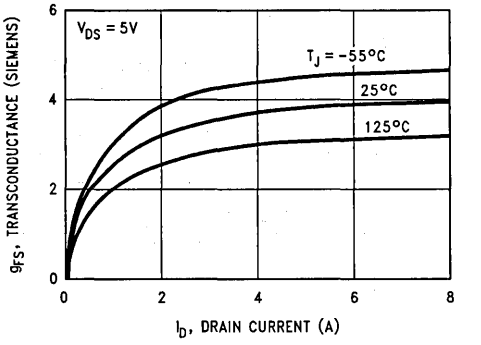

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FIGURE 13. Transconductance Variation with Drain Current and Temperature

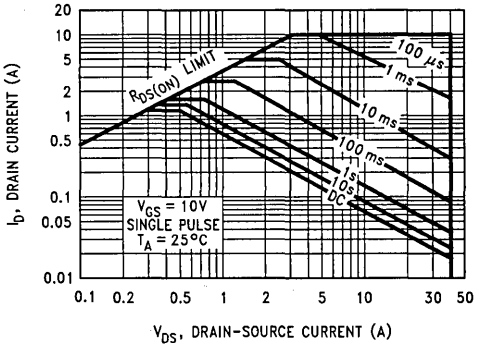

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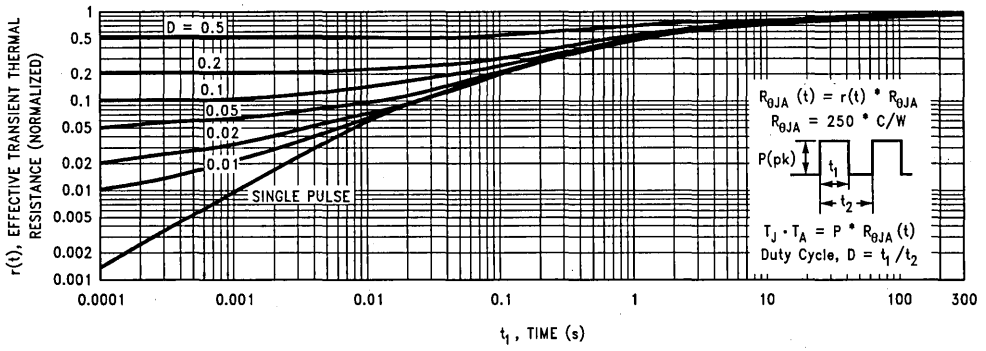
FIGURE 14. Maximum Safe Operating Area



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Note: Characterization performed using a circuit board with 175°C/W typical case-to-ambient thermal resistance.

FIGURE 15. Transient Thermal Response Curve

National Semiconductor

NDS352P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

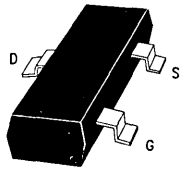
General Description

These P-channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- −850 mA, −20V, $R_{DS(ON)}$ = 0.5Ω, @ V_{GS} = −4.5V
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Compact industry standard SOT-23 surface mount package

SOT-23
(TO-236AB)



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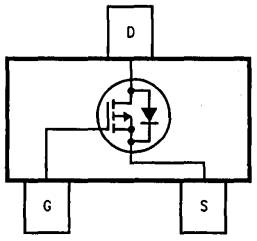

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Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS352P	Units
V_{DSS}	Drain-Source Voltage		−20	V
V_{GSS}	Gate-Source Voltage	— Continuous	±12	V
I_D	Maximum Drain Current	— Continuous	±850	mA
		— Pulsed	±10	A
P_D	Maximum Power Dissipation	@ T_A = 25°C	500 (Note 1)	mW
		@ T_C = 25°C	1.7 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds		300	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		250 (Note 1)	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		75 (Note 1)	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = −250 μA	−20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16V, V_{GS} = 0V			−5	μA
		T_J = 125°C			−50	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 12V, V_{DS} = 0V			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = −12V, V_{DS} = 0V			−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.8	−1.6	−2	V
		T_J = 125°C	−0.5	−1.3	−1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = −4.5V, I_D = −0.85A		0.46	0.5	Ω
		T_J = 125°C		0.59	0.7	
		V_{GS} = −10V, I_D = −1A			0.35	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = −4.5V, V_{DS} = −5V	−2			A
g_{FS}	Forward Transconductance	V_{DS} = −5V, I_D = −0.85A		1.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10V, V_{GS} = 0V, f = 1.0 MHz		125		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = −10V, I_D = −1A, V_{GS} = −10V, R_{GEN} = 50Ω		8	15	ns
t_r	Turn-On Rise Time			19	30	ns
$t_{D(OFF)}$	Turn-Off Delay Time			64	90	ns
t_f	Turn-Off Fall Time			61	90	ns
Q_g	Total Gate Charge	V_{DS} = −10V, I_D = −0.85A, V_{GS} = −5V		2.2	4	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				−0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				−5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GD} = 0V, I_S = −0.85A (Note 2)		−0.92	−1.2	V

Note 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. In this case, $R_{\theta CA}$ of 175°C/W can be achieved with a drain thermal pad of approximately 0.01 square inch of 2 ounce copper.

Note 2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

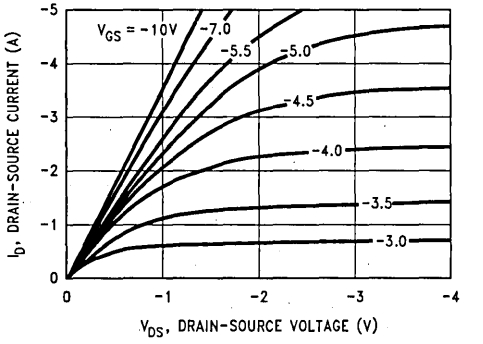

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FIGURE 1. On-Region Characteristics

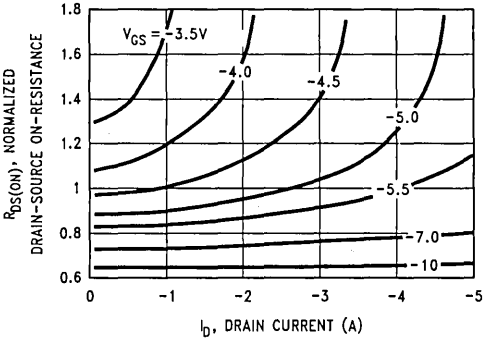

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FIGURE 2. On-Resistance Variation with Drain Current and Gate Voltage

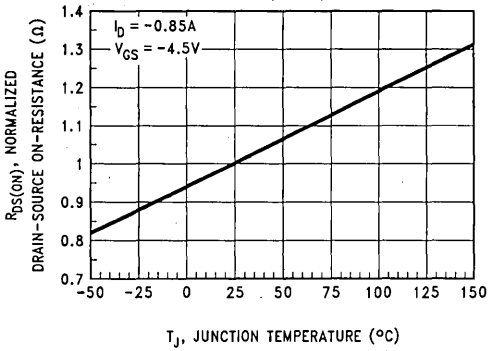

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FIGURE 3. On-Resistance Variation with Temperature

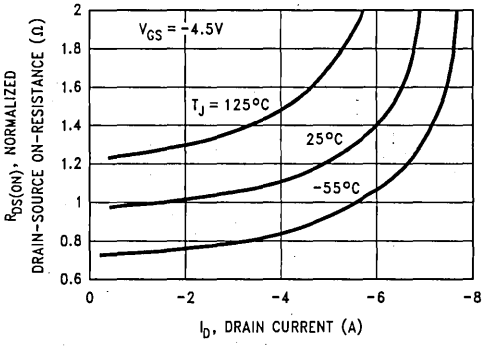

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FIGURE 4. On-Resistance Variation with Drain Current and Temperature

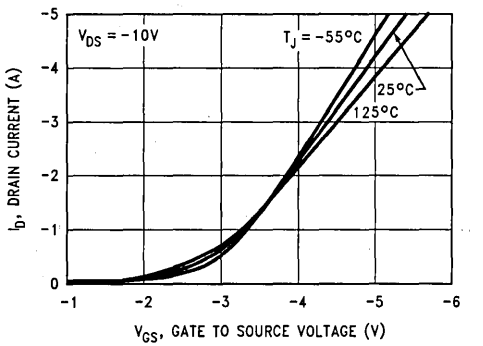

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FIGURE 5. Transfer Characteristics

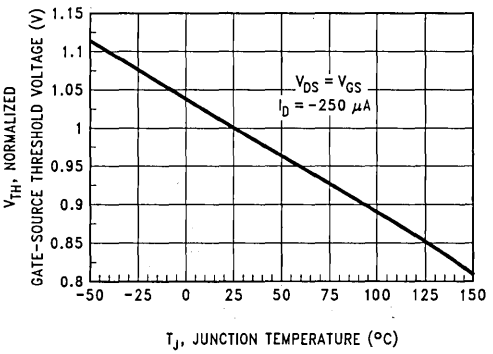

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FIGURE 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (Continued)

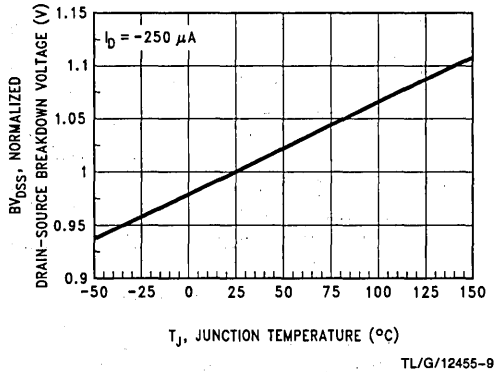

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FIGURE 7. Breakdown Voltage Variation with Temperature

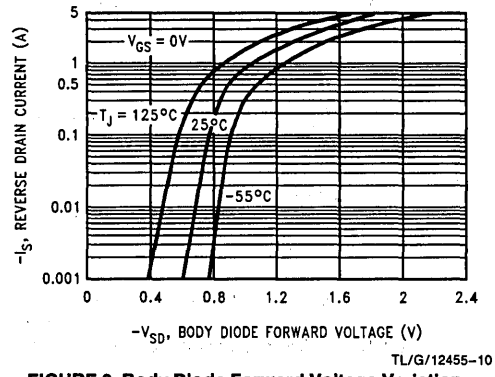

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FIGURE 8. Body Diode Forward Voltage Variation with Source Current and Temperature

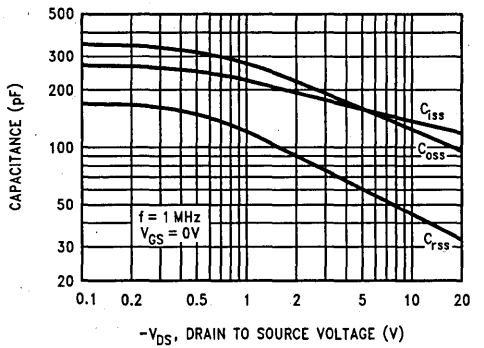

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FIGURE 9. Capacitance Characteristics

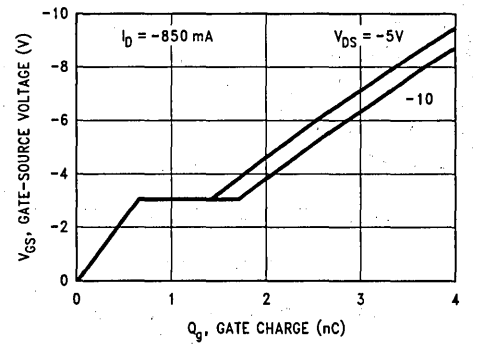

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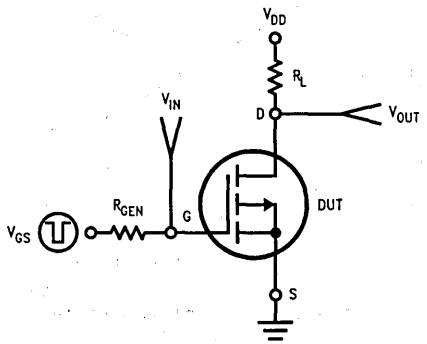
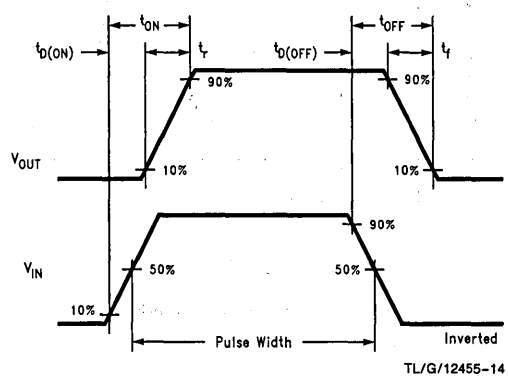
FIGURE 10. Gate Charge Characteristics



TL/G/12455–13

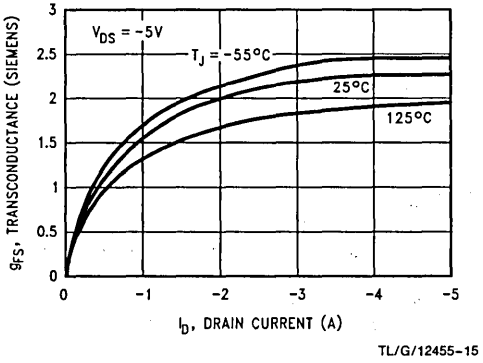
FIGURE 11. Switching Test Current



TL/G/12455–14

FIGURE 12. Switching Waveforms

Typical Electrical Characteristics (Continued)



TL/G/12455-15

FIGURE 13. Transconductance Variation with Drain Current and Temperature

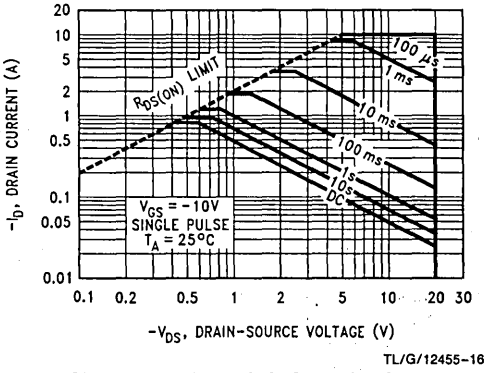


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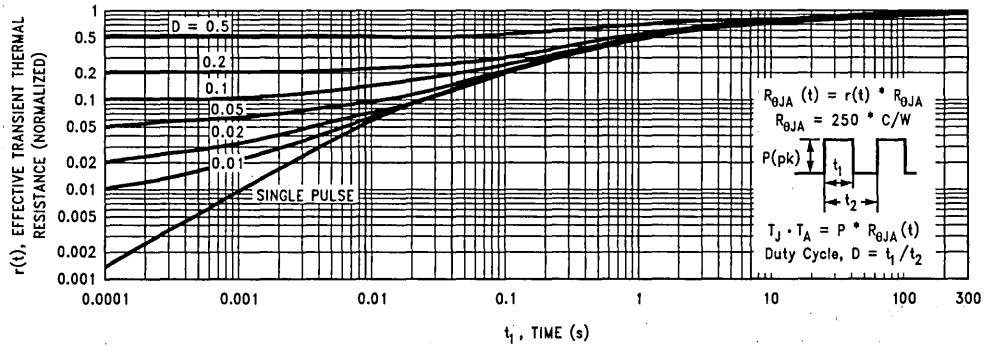
FIGURE 14. Maximum Safe Operating Area



TL/G/12455-17

Note: Characterization performed using a circuit board with 175°C/W typical case-to-ambient thermal resistance.

FIGURE 15. Transient Thermal Response Curve

National Semiconductor

NDS355N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

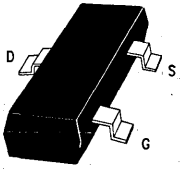
General Description

These N-channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.6A, 30V, $R_{DS(ON)}$ = 0.125Ω @ V_{OS} = 4.5V
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Compact industry standard SOT-23 surface mount package

SOT-23
(TO-236AB)



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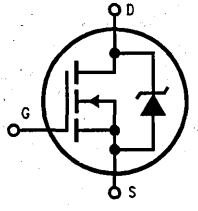


TL/G/12456–2

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDS355N	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage—Continuous	±20	V
I_D	Drain Current—Continuous	1.6	A
	—Pulsed	10	
P_D	Maximum Power Dissipation @ T_A = 25°C	500 (Note 1)	mW
	@ T_A = 25°C	1.7 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	250 (Note 1)	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	75 (Note 1)	°C/W

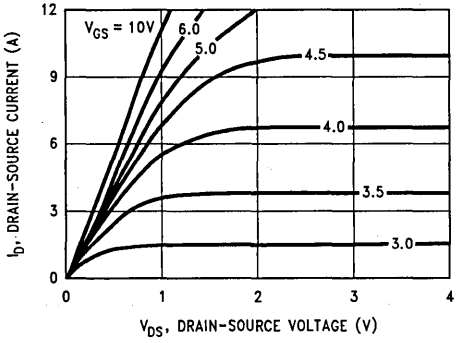
Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250 μA		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V				1	μA
			T_J = 125°C			10	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 12V, V_{DS} = 0V				100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = −12V, V_{DS} = 0V				−100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA		1	1.6	2	V
			T_J = 125°C	0.5	1.3	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 1.6A				0.125	Ω
			T_J = 125°C			0.25	
		V_{GS} = 10V, I_D = 1.9A				0.085	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5V, V_{DS} = 5V		6			A
G_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 1.6A			3.5		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1.0 MHz			245		pF
C_{oss}	Output Capacitance				128		pF
C_{rss}	Reverse Transfer Capacitance				21		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω			15	30	ns
t_r	Turn-On Rise Time				14	30	ns
$t_{D(OFF)}$	Turn-Off Delay Time				12	25	ns
t_f	Turn-Off Fall Time				4	10	ns
O_g	Total Gate Charge	V_{DS} = 10V, I_D = 1.6A, V_{GS} = 5V			3.5	5	nC
O_{gs}	Gate-Source Charge					1	nC
O_{gd}	Gate-Drain Charge					2	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Source Current					0.6	A
I_{SM}	Maximum Pulse Source Current (Note 2)					6	A
V_{SD}	Drain-Source Diode Foward Voltage	V_{GS} = 0V, I_S = 1.6A			0.8	1.2	V

Note 1: $R_{\theta JA}$ is the sum of the junction-to-case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. In this case, $R_{\theta JA}$ of 175° C/W can be achieved with a drain thermal pad of approximately 0.01 square inch of 2 ounce copper.

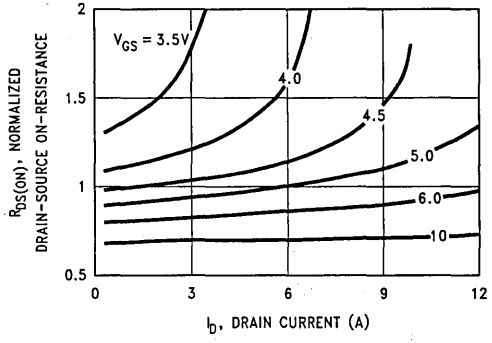
Note 2: Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics



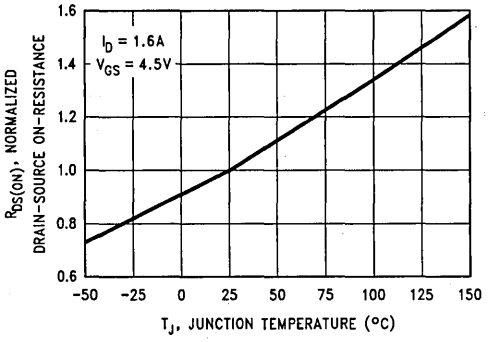
TL/G/12456–3

FIGURE 1. On-Region Characteristics



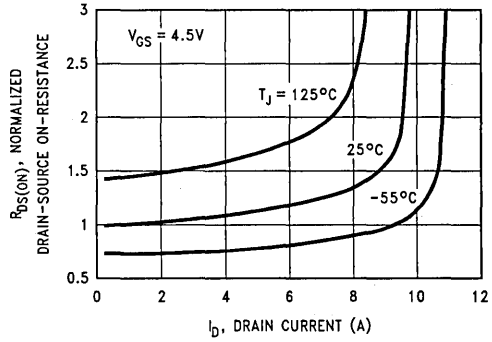
TL/G/12456–4

FIGURE 2. On-Resistance Variation with Gate Voltage and Drain Current



TL/G/12456–5

FIGURE 3. On-Resistance Variation with Temperature



TL/G/12456–6

FIGURE 4. On-Resistance Variation with Drain Current and Temperature

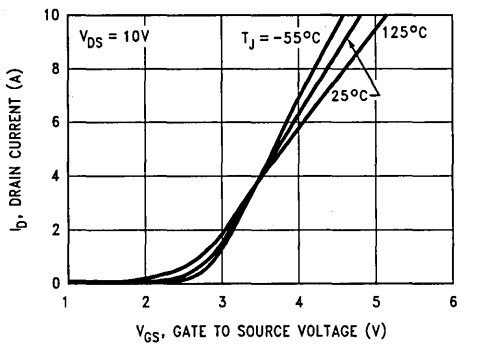


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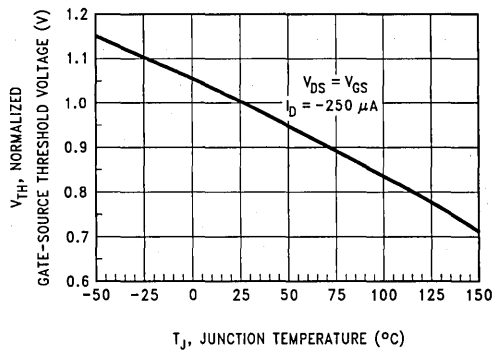
FIGURE 5. Transfer Characteristics



TL/G/12456–8

FIGURE 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (Continued)

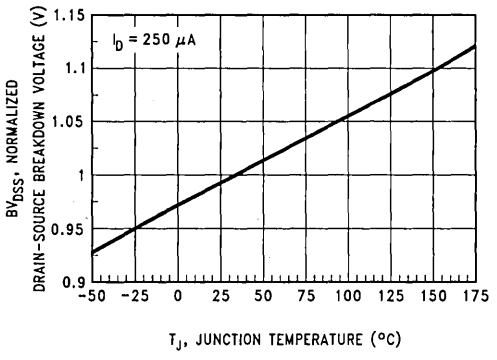


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FIGURE 7. Breakdown Voltages Variation with Temperature

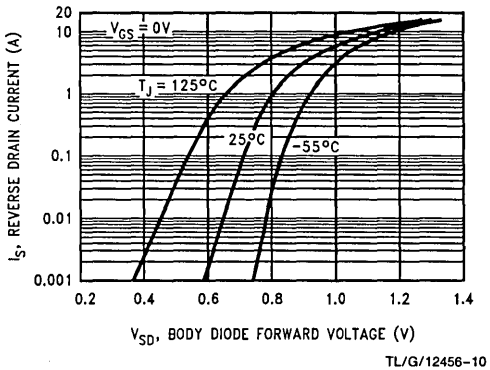

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FIGURE 8. Body Diode Forward Voltage Variation with Current and Temperature

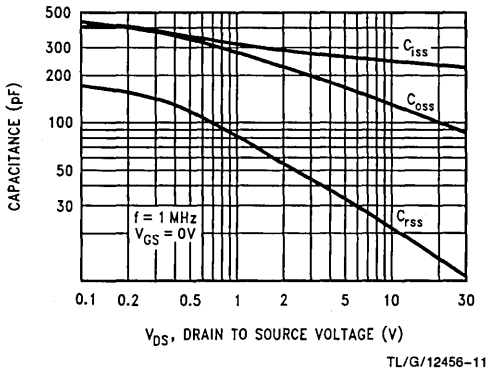

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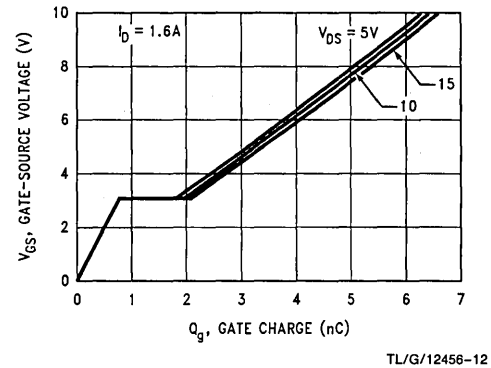
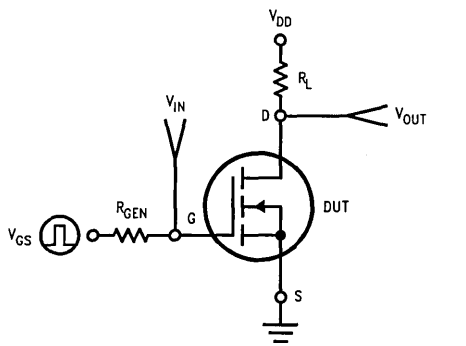
FIGURE 9. Capacitance Characteristics



TL/G/12456-12

FIGURE 10. Gate Charge Characteristics



TL/G/12456-13

FIGURE 11. Switching Test Circuit

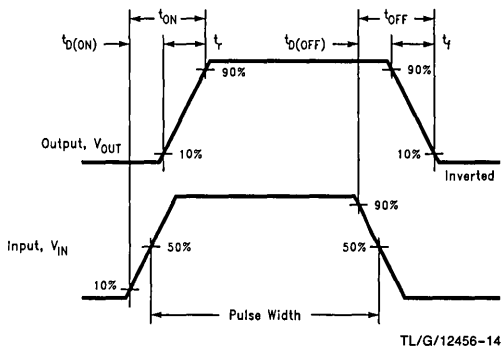


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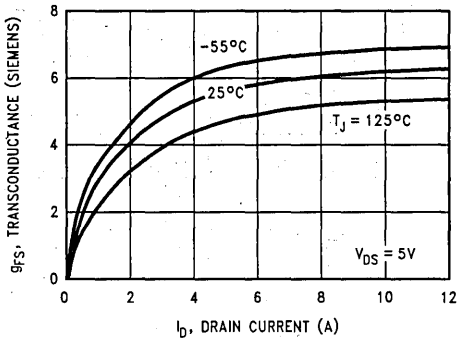
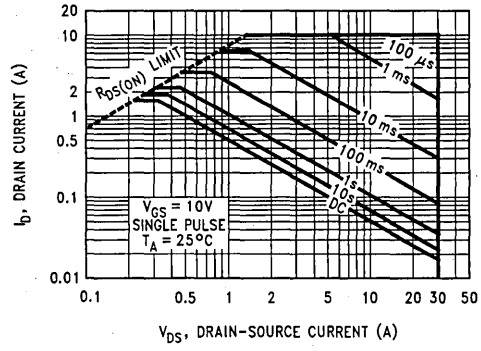
FIGURE 12. Switching Waveforms

Typical Electrical Characteristics (Continued)



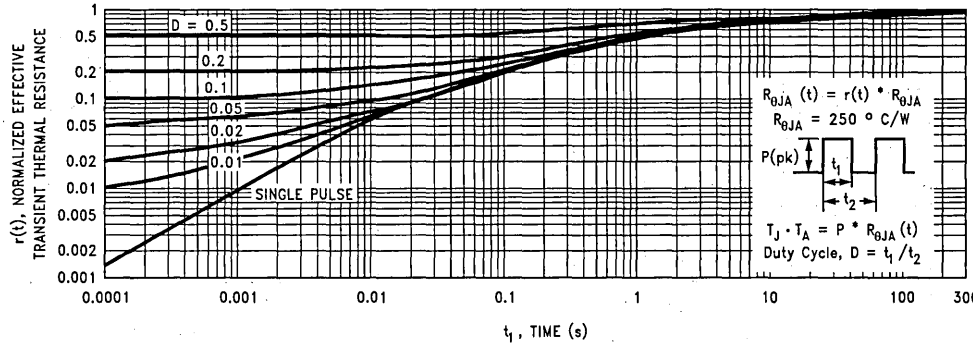
TL/G/12456-15

FIGURE 13. Transconductance Variation with Drain Current and Temperature



TL/G/12456-16

FIGURE 14. Maximum Safe Operating Area



TL/G/12456-17

FIGURE 15. Transient Thermal Response Curve

Note: Characterization performed using a circuit board with 175° C/W typical case-to-ambient thermal resistance.

National Semiconductor

NDS356P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

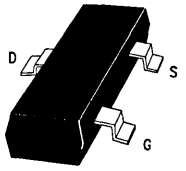
General Description

These P-channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- −1.1A, −20V, $R_{DS(ON)}$ = 0.3Ω @ V_{GS} = −4.5V
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Compact industry standard SOT-23 surface mount package

SOT-23
(TO-236AB)



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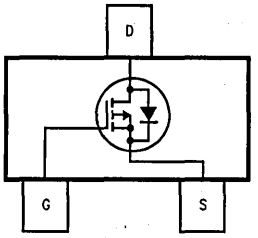


TL/G/12457–2

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDS356P	Units
V_{DSS}	Drain-Source Voltage	−20	V
V_{GSS}	Gate-Source Voltage—Continuous	±12	V
I_D	Maximum Drain Current—Continuous	±1.1	A
	—Pulsed	±10	
P_D	Maximum Power Dissipation @ T_A = 25°C	500 (Note1)	mW
	@ T_C = 25°C	1.7 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	250 (Note 1)	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	75 (Note 1)	°C/W

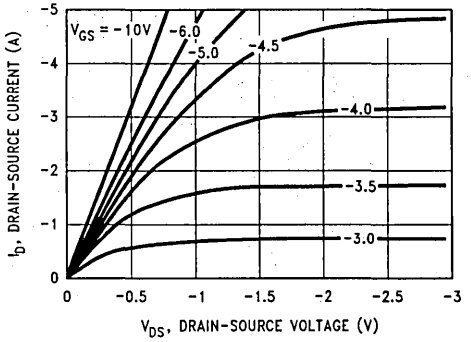
Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = −250 μA	−20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16V, V_{GS} = 0V			−5	μA
		T_J = 125°C			−20	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 12V, V_{DS} = 0V			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = −12V, V_{DS} = 0V			−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.8	−1.6	−2	V
		T_J = 125°C	−0.5	−1.3	−1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = −4.5V, I_D = −1.1A			0.3	Ω
		T_J = 125°C			0.4	
		V_{GS} = 10V, I_D = −1.3A			0.21	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = −4.5V, V_{DS} = −5V	−3			A
g_{FS}	Forward Transconductance	V_{DS} = −5V, I_D = −1.1A		1.8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10V, V_{GS} = 0V, f = 1.0 MHz		180		pF
C_{oss}	Output Capacitance			255		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = −10V, I_D = −1A, V_{GS} = −10V, R_{GEN} = 50Ω		7	15	ns
t_r	Turn-On Rise Time			17	30	ns
$t_{D(OFF)}$	Turn-Off Delay Time			56	90	ns
t_f	Turn-Off Fall Time			41	80	ns
O_g	Total Gate Charge	V_{DS} = −10V, I_D = −1.1A, V_{GS} = −5V		3.5	5	nC
O_{gs}	Gate-Source Charge				1.5	nC
O_{gd}	Gate-Drain Charge				2	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				−0.6	A
I_{SM}	Maximum Pulse Drain-Source Diode Forward Current				−4	A
V_{SD}	Drain-Source Diode Foward Voltage	V_{GS} = 0V, I_S = −1.1A (Note 2)		−0.85	−1.2	V

Note 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. In this case, $R_{\theta CA}$ of 175°C/W can be achieved with a drain thermal pad of approximately 0.01 square inch of 2 ounce copper.

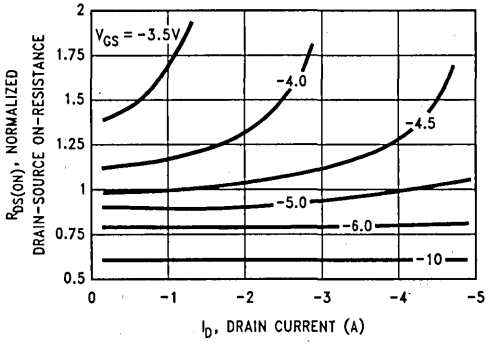
Note 2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics



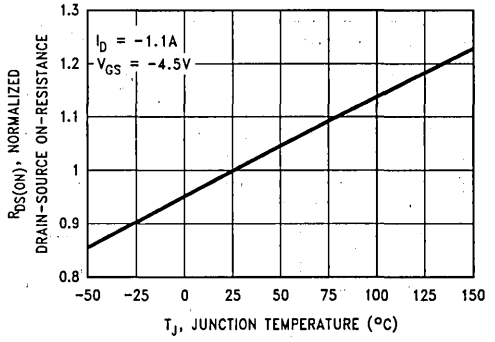
TL/G/12457-3

FIGURE 1. On-Region Characteristics



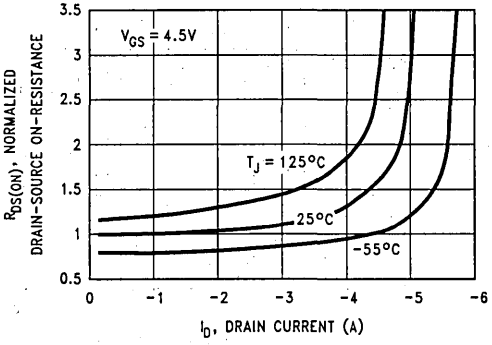
TL/G/12457-4

FIGURE 2. On-Resistance Va.iation with Drain Current and Gate Voltage



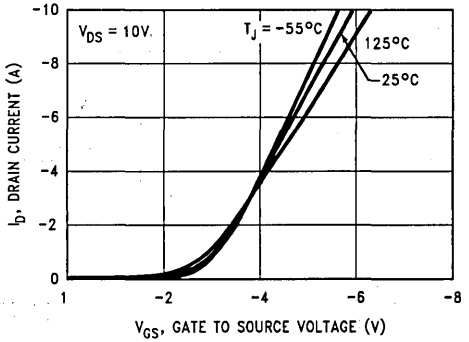
TL/G/12457-5

FIGURE 3. On-Resistance Variation with Temperature



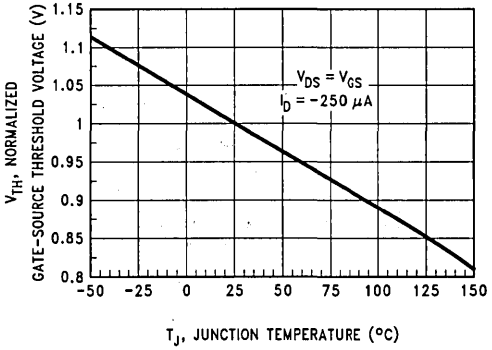
TL/G/12457-6

FIGURE 4. On-Resistance Variation with Drain Current and Temperature



TL/G/12457-7

FIGURE 5. Transfer Characteristics



TL/G/12457-8

FIGURE 6. Gate Threshold Variation with Temperature

6

Typical Electrical Characteristics (Continued)

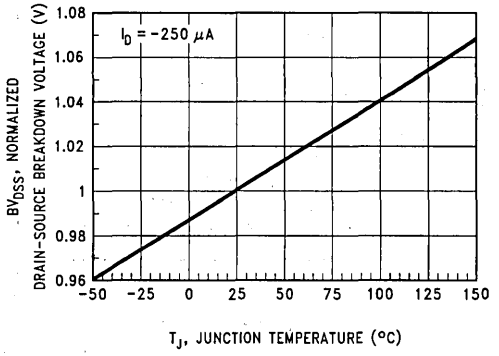


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FIGURE 7. Breakdown Voltage Variation with Temperature

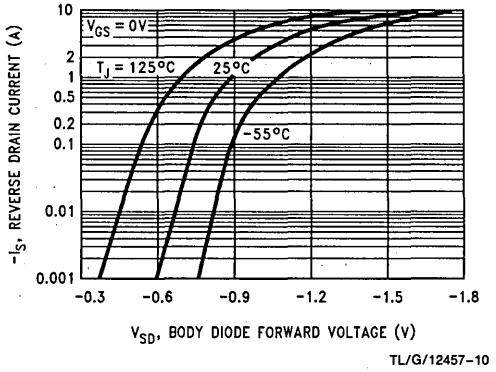

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FIGURE 8. Body Diode Forward Voltage Variation with Source Current and Temperature

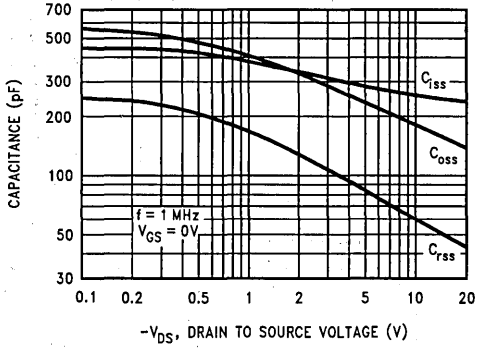

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FIGURE 9. Capacitance Characteristics

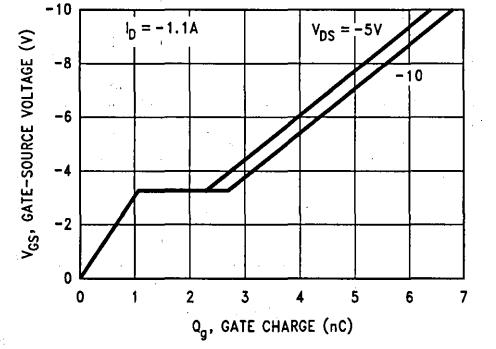

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FIGURE 10. Gate Charge Characteristics

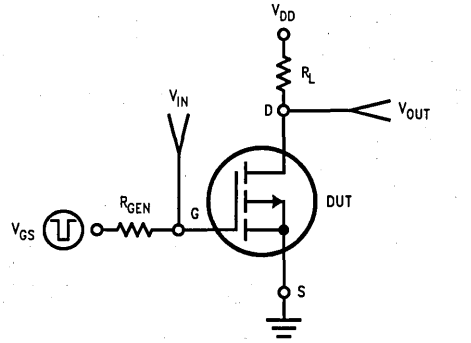

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FIGURE 11. Switching Test Circuit

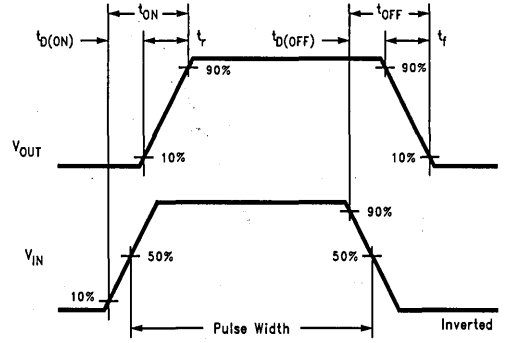

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FIGURE 12. Switching Waveforms

Typical Electrical Characteristics (Continued)

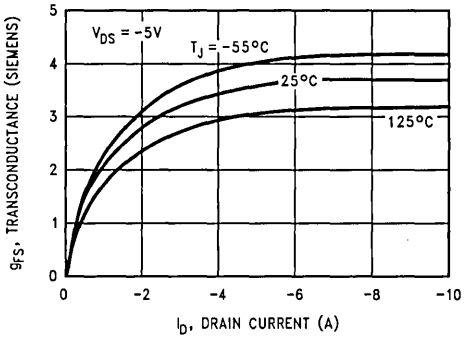


FIGURE 13. Transconductance Variation with Drain Current and Temperature

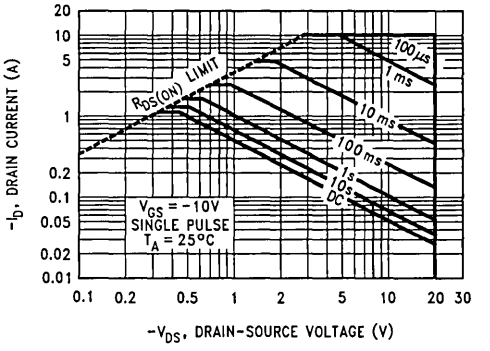
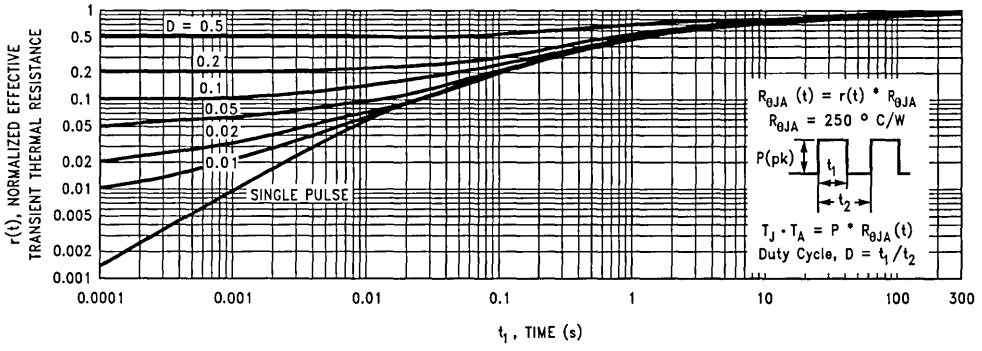


FIGURE 14. Maximum Safe Operating Area



Note: Characterization performed using a circuit board with 175°C/W typical case-to-ambient thermal resistance.

FIGURE 15. Transient Thermal Response Curve

Section 7

Power Management

Section 7 Contents

National Semiconductor

LM45B/LM45C
SOT-23 Precision Centigrade Temperature Sensors

General Description

The LM45 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM45 does not require any external calibration or trimming to provide accuracies of ±2°C at room temperature and ±3°C over a full −20 to +100°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM45's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with a single power supply, or with plus and minus supplies. As it draws only 120 μA from its supply, it has very low self-heating, less than 0.2°C in still air. The LM45 is rated to operate over a −20° to +100°C temperature range.

Applications

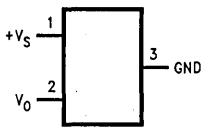
- Battery Management
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules
- Disk Drives
- Computers
- Automotive

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±3°C accuracy guaranteed
- Rated for full −20° to +100°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.0V to 10V
- Less than 120 μA current drain
- Low self-heating, 0.20°C in still air
- Nonlinearity only ±0.8°C max over temp
- Low impedance output, 20Ω for 1 mA load

Connection Diagram

SOT-23



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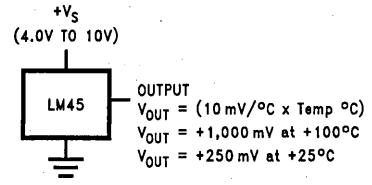
Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

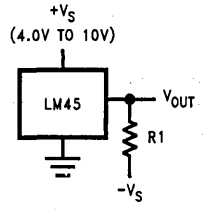
Order Number	SOT-23 Device Marking	Supplied As
LM45BIM3	T4B	250 Units on Tape and Reel
LM45BIM3X	T4B	3000 Units on Tape and Reel
LM45CIM3	T4C	250 Units on Tape and Reel
LM45CIM3X	T4C	3000 Units on Tape and Reel

Typical Applications



TL/H/11754–3

FIGURE 1. Basic Centigrade Temperature Sensor (+2.5°C to +100°C)



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Choose $R_1 = -V_S/50\ \mu A$
V_{OUT} = (10 mV/°C × Temp °C)
V_{OUT} = +1,000 mV at +100°C
= +250 mV at +25°C
= −200 mV at −20°C

FIGURE 2. Full-Range Centigrade Temperature Sensor (−20°C to +100°C)

Absolute Maximum Ratings (Note 1)

Supply Voltage	+12V to −0.2V
Output Voltage	$+V_S$ + 0.6V to −1.0V
Output Current	10 mA
Storage Temperature	−65°C to +150°C
Lead Temperature	
SOT Package (Note 2):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 3):	
Human Body Model	2000V
Machine Model	TBD

Operating Ratings (Note 1)

Specified Temperature Range (Note 4)	T_{MIN} to T_{MAX}
LM45B, LM45C	−20°C to +100°C
Operating Temperature Range	
LM45B, LM45C	−40°C to +125°C
Supply Voltage Range ($+V_S$)	+4.0V to +10V

Electrical Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = +5Vdc and I_{LOAD} = +50 μA, in the circuit of *Figure 2*. These specifications also apply from +2.5°C to T_{MAX} in the circuit of *Figure 1* for $+V_S$ = +5Vdc. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = +25°C, unless otherwise noted.

Parameter	Conditions	LM45B		LM45C		Units (Limit)
		Typical	Limit (Note 5)	Typical	Limit (Note 5)	
Accuracy (Note 6)	T_A = +25°C T_A = T_{MAX} T_A = T_{MIN}		±2.0 ±3.0 ±3.0		±3.0 ±4.0 ±4.0	°C (max) °C (max) °C (max)
Nonlinearity (Note 7)	$T_{MIN} \le T_A \le T_{MAX}$		**±0.8**		**±0.8**	°C (max)
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$		**+9.7** **+10.3**		**+9.7** **+10.3**	mV/°C (min) mV/°C (max)
Load Regulation (Note 8)	$0 \le I_L \le +1$ mA		**±35**		**±35**	mV/mA (max)
Line Regulation (Note 8)	$+4.0V \le +V_S \le +10V$		±0.80 **±1.2**		±0.80 **±1.2**	mV/V (max) mV/V (max)
Quiescent Current (Note 9)	$+4.0V \le +V_S \le +10V$, +25°C $+4.0V \le +V_S \le +10V$		120 **160**		120 **160**	μA (max) μA (max)
Change of Quiescent Current (Note 8)	$4.0V \le +V_S \le 10V$		**2.0**		**2.0**	μA (max)
Temperature Coefficient of Quiescent Current		**+2.0**		**+2.0**		μA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0		+2.5		+2.5	°C (min)
Long Term Stability (Note 10)	T_J = T_{MAX}, for 1000 hours	±0.12		±0.12		°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

Note 4: Thermal resistance of the SOT-23 package is 260°C/W, junction to ambient when attached to a printed circuit board with 2 oz. foil as shown in *Figure 3*.

Note 5: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Accuracy is defined as the error between the output voltage and 10 mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 7: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 8: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

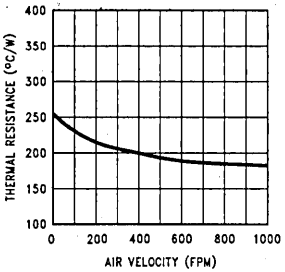
Note 9: Quiescent current is measured using the circuit of *Figure 1*.

Note 10: For best long-term stability, any precision circuit will give best results if the unit is aged at a warm temperature, and/or temperature cycled for at least 46 hours before long-term life test begins. This is especially true when a small (Surface-Mount) part is wave-soldered; allow time for stress relaxation to occur.

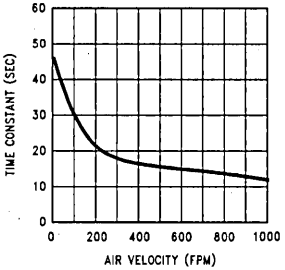
Typical Performance Characteristics

To generate these curves the LM45 was mounted to a printed circuit board as shown in *Figure 3*.

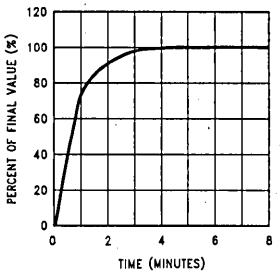
Thermal Resistance Junction to Air



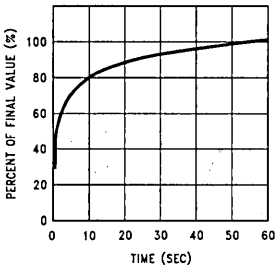
Thermal Time Constant



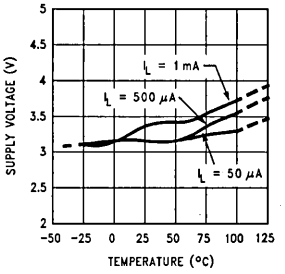
Thermal Response in Still Air with Heat Sink (*Figure 3*)



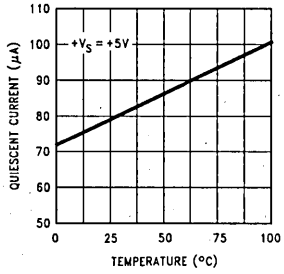
Thermal Response in Stirred Oil Bath with Heat Sink



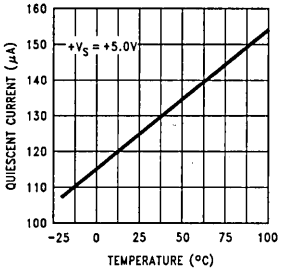
Start-Up Voltage vs Temperature



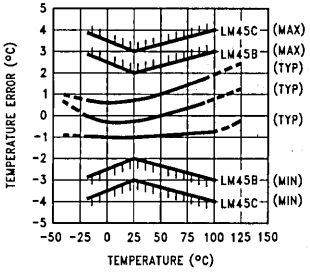
Quiescent Current vs Temperature (In Circuit of *Figure 1*)



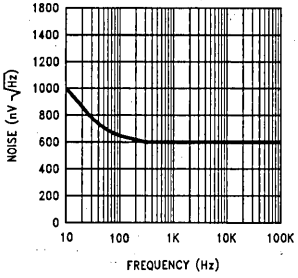
Quiescent Current vs Temperature (In Circuit of *Figure 2*)



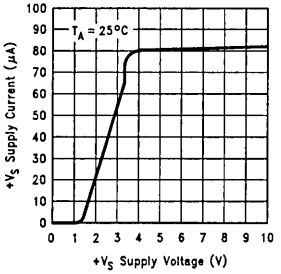
Accuracy vs Temperature (Guaranteed)



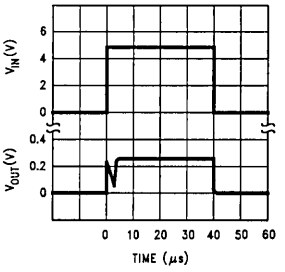
Noise Voltage



Supply Voltage vs Supply Current



Start-Up Response



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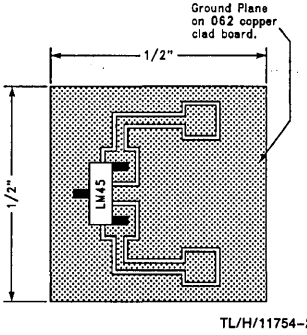

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FIGURE 3. Printed Circuit Board Used for Heat Sink to Generate All Curves. ½" Square Printed Circuit Board with 2 oz. Foil or Similar

Applications

The LM45 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.2°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM45 die would be at an intermediate temperature between the surface temperature and the air temperature.

To ensure good thermal conductivity the backside of the LM45 die is directly attached to the GND pin. The lands and traces to the LM45 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured. These printed circuit board lands and traces will not cause the LM45s temperature to deviate from the desired temperature.

Alternatively, the LM45 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM45 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM45 or its connections.

Temperature Rise of LM45 Due to Self-Heating (Thermal Resistance)

	SOT-23** no heat sink	SOT-23 small heat fin*
Still air	450°C/W	260°C/W
Moving air		180°C/W

* Heat sink used is ½" square printed circuit board with 2 oz. foil with part attached as shown in *Figure 3.*

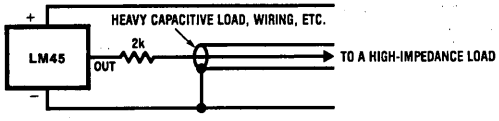
** Part soldered to 30 gauge wire.

Typical Applications

CAPACITIVE LOADS

Like most micropower circuits, the LM45 has a limited ability to drive heavy capacitive loads. The LM45 by itself is able to drive 500 pF without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 4.* Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 5.*

Any linear circuit connected to wires in a hostile environment can have its performance affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground, as shown in *Figure 5*, are often useful.



TL/H/11754–8

FIGURE 4. LM45 with Decoupling from Capacitive Load

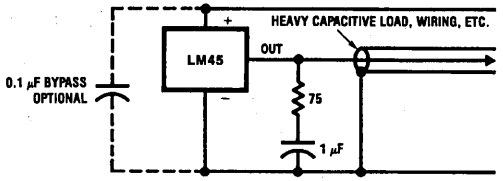


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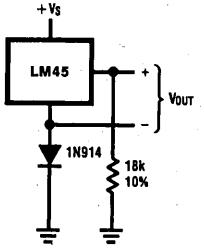
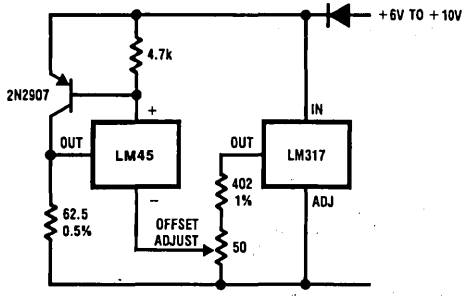
FIGURE 5. LM45 with R-C Damper



TL/H/11754–12

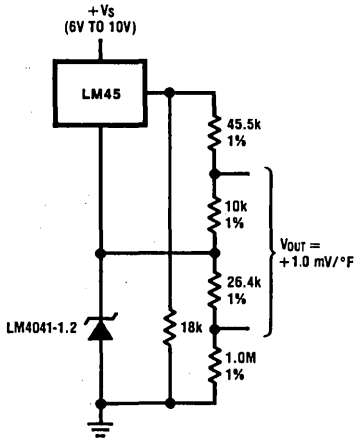
FIGURE 6. Temperature Sensor, Single Supply, −20°C to +100°C

Typical Applications (Continued)



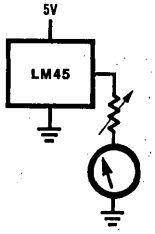
TL/H/11754–14

FIGURE 7. 4-to-20 mA Current Source (0°C to +100°C)



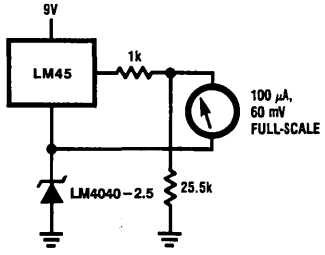
TL/H/11754–15

FIGURE 8. Fahrenheit Thermometer



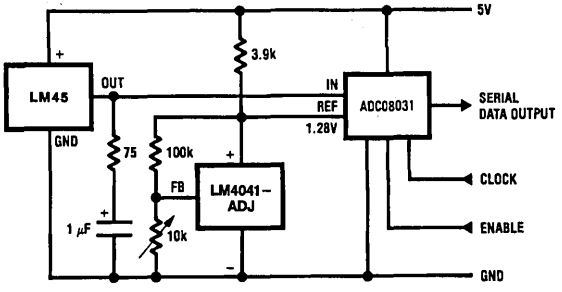
TL/H/11754–16

FIGURE 9. Centigrade Thermometer (Analog Meter)



TL/H/11754–17

FIGURE 10. Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)

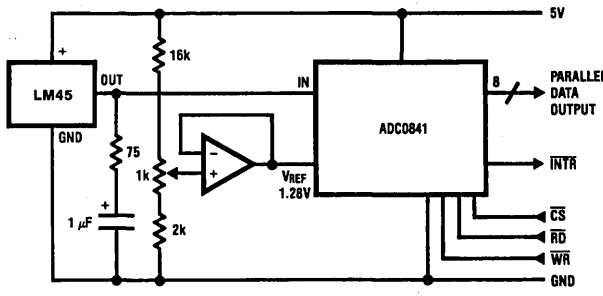


TL/H/11754–18

FIGURE 11. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

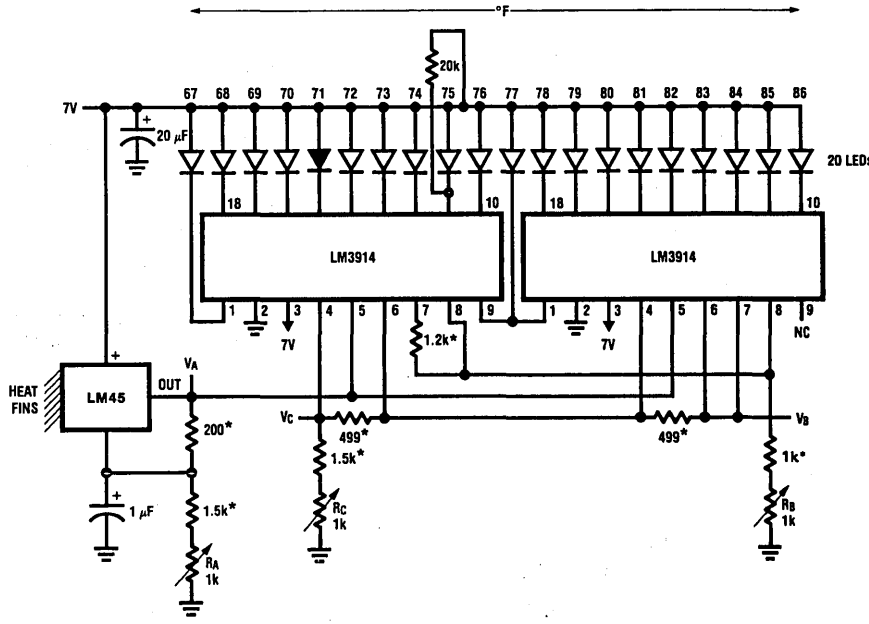
7

Typical Applications (Continued)



TL/H/11754–19

FIGURE 12. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)

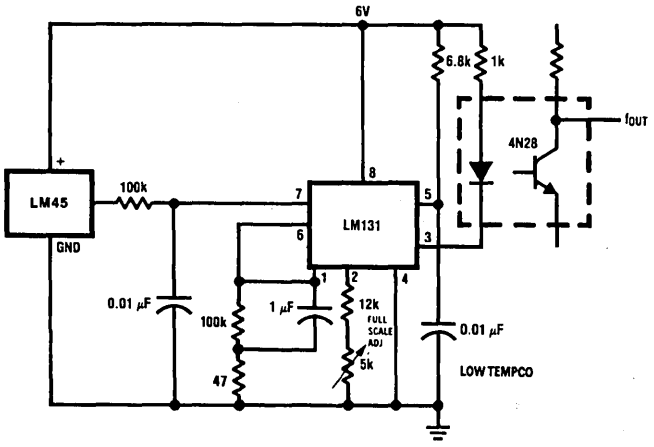


TL/H/11754–20

*=1% or 2% film resistor
-Trim R_B for V_B=3.075V
-Trim R_C for V_C=1.955V
-Trim R_A for V_A=0.075V + 100mV/°C × $T_{ambient}$
-Example, V_A=2.275V at 22°C

FIGURE 13. Bar-Graph Temperature Display (Dot Mode)

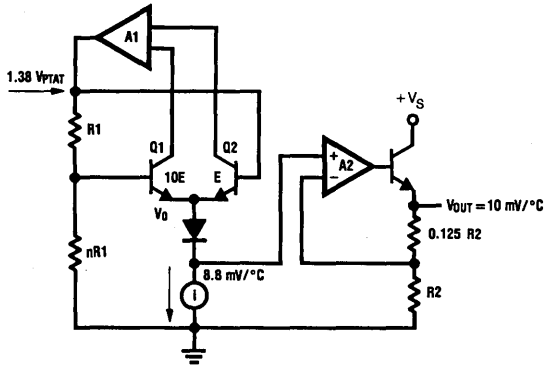
Typical Applications (Continued)



TL/H/11754–21

FIGURE 14. LM45 With Voltage-To-Frequency Converter And Isolated Output (2.5°C to +100°C; 25 Hz to 1000 Hz)

Block Diagram



TL/H/11754–22

National Semiconductor

LM50B/LM50C
SOT-23 Single-Supply Centigrade Temperature Sensor

General Description

The LM50 is a precision integrated-circuit temperature sensor that can sense a −40°C to +125°C temperature range using a single positive supply. The LM50's output voltage is linearly proportional to Celsius (Centigrade) temperature (+10 mV/°C) and has a DC offset of +500 mV. The offset allows reading negative temperatures without the need for a negative supply. The ideal output voltage of the LM50 ranges from +100 mV to +1.75V for a −40°C to +125°C temperature range. The LM50 does not require any external calibration or trimming to provide accuracies of ±3°C at room temperature and ±4°C over the full −40°C to +125°C temperature range. Trimming and calibration of the LM50 at the wafer level assure low cost and high accuracy. The LM50's linear output, +500 mV offset, and factory calibration simplify circuitry required in a single supply environment where reading negative temperatures is required. Because the LM50's quiescent current is less than 130 μA, self-heating is limited to a very low 0.2°C in still air.

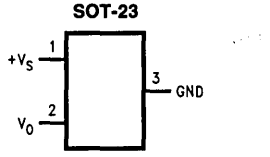
Applications

- Computers
- Disk Drives
- Battery Management
- Automotive
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±2°C accuracy guaranteed at +25°C
- Specified for full −40° to +125°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.5V to 10V
- Less than 130 μA current drain
- Low self-heating, less than 0.2°C in still air
- Nonlinearity less than 0.8°C over temp

Connection Diagram



Top View

See NS Package Number M03B (JEDEC Registration TO-236AB)

Order Number	SOT-23 Device Marking	Supplied As
LM50BIM3	T5B	250 Units on Tape and Reel
LM50CIM3	T5C	250 Units on Tape and Reel
LM50BIM3X	T5B	3000 Units on Tape and Reel
LM50CIM3X	T5C	3000 Units on Tape and Reel

Typical Applications

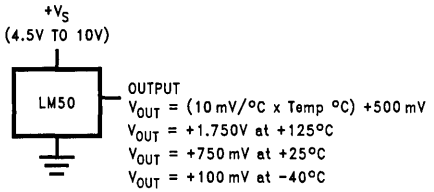


FIGURE 1. Full-Range Centigrade Temperature Sensor (−40°C to +125°C)

Absolute Maximum Ratings (Note 1)

Supply Voltage	+12V to −0.2V
Output Voltage	(+V_S + 0.6V) to −1.0V
Output Current	10 mA
Storage Temperature	−65°C to +150°C
Lead Temperature	
SOT Package (Note 2):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 3):	
Human Body Model	2000V
Machine Model	200V

Operating Ratings (Note 1)

Specified Temperature Range:	
T_{MIN} to T_{MAX} (Note 4)	
LM50C	−40°C to +125°C
LM50B	−25°C to +100°C
Operating Temperature Range	−40°C to +125°C
Supply Voltage Range (+V_S)	+4.5V to +10V

Electrical Characteristics

Unless otherwise noted, these specifications apply for V_S = +5 V_{DC} and I_{LOAD} = +0.5 μA, in the circuit of *Figure 1*. **Boldface limits apply for the specified T_A = T_J = T_{MIN} to T_{MAX}**; all other limits T_A = T_J = +25°C, unless otherwise noted.

Parameter	Conditions	LM50B		LM50C		Units (Limit)
		Typical	Limit (Note 5)	Typical	Limit (Note 5)	
Accuracy (Note 6)	T_A = +25°C		±2.0		±3.0	°C (max)
	T_A = T_{MAX}		±3.0		±4.0	°C (max)
	T_A = T_{MIN}		+3.0, −3.5		±4.0	°C (max)
Nonlinearity (Note 7)			**±0.8**		**±0.8**	°C (max)
Sensor Gain (Average Slope)			**+9.7**		**+9.7**	mV/°C (min)
			+10.3		**+10.3**	mV/°C (max)
Output Resistance		2000	**4000**	2000	**4000**	Ω (max)
Line Regulation (Note 8)	4.5V ≤ V_S ≤ 10V		±0.8		±0.8	mV/V (max)
			±1.2		**±1.2**	mV/V (max)
Quiescent Current (Note 9)	+4.5V ≤ V_S ≤ +10V		130		130	μA (max)
			180		**180**	μA (max)
Change of Quiescent Current (Note 8)	4.5V ≤ V_S ≤ 10V		**2.0**		**2.0**	μA (max)
Temperature Coefficient of Quiescent Current		**+1.0**		**+2.0**		μA/°C
Long Term Stability	T_J = T_{MAX}, for 1000 hours	±0.08		±0.08		°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 3: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

Note 4: Thermal resistance of the SOT-23 package is 450°C without a heat sink, junction to ambient.

Note 5: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 7: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

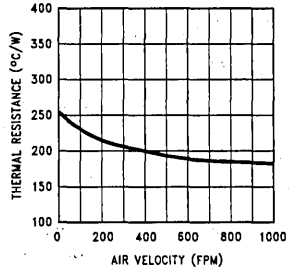
Note 8: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

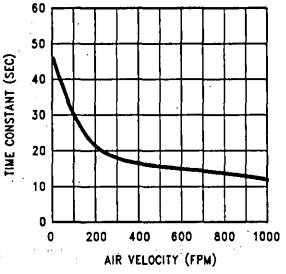
Typical Performance Characteristics

To generate these curves the LM45 was mounted to a printed circuit board as shown in *Figure 2.*

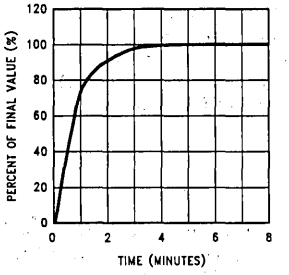
Thermal Resistance Junction to Air



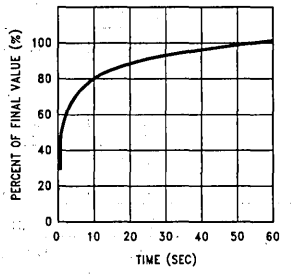
Thermal Time Constant



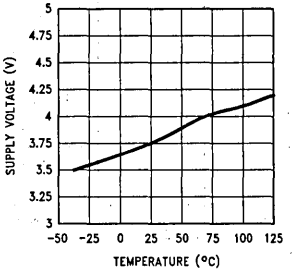
Thermal Response in Still Air with Heat Sink (*Figure 2*)



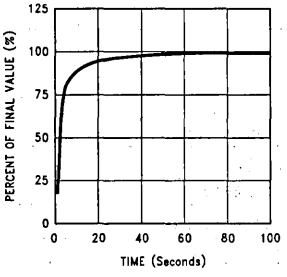
Thermal Response in Stirred Oil Bath with Heat Sink



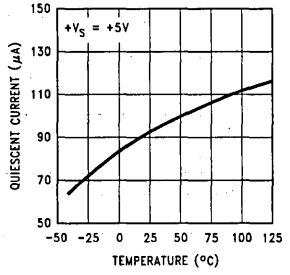
Start-Up Voltage vs Temperature



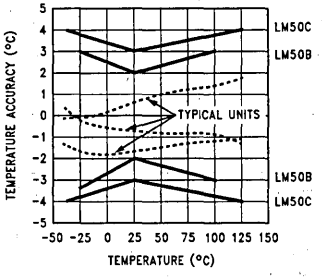
Thermal Response in Still Air without a Heat Sink



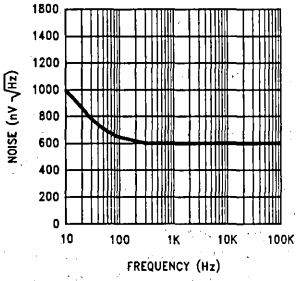
Quiescent Current vs Temperature (*Figure 1*)



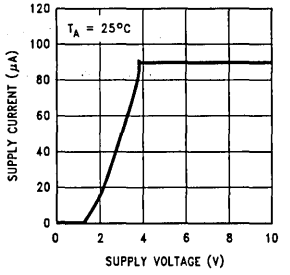
Accuracy vs Temperature



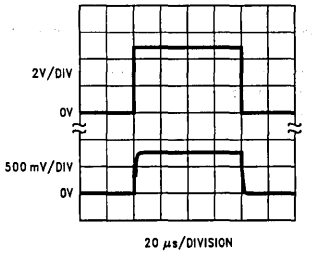
Noise Voltage



Supply Voltage vs Supply Current



Start-Up Response



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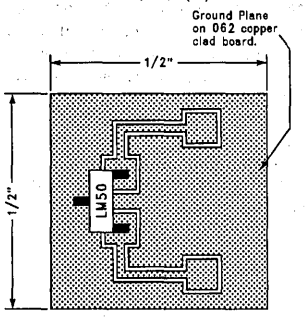

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FIGURE 2. Printed Circuit Board Used for Heat Sink to Generate All Curves. ½" Square Printed Circuit Board with 2 oz. Foil or Similar

1.0 Mounting

The LM50 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.2°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM50 die would be at an intermediate temperature between the surface temperature and the air temperature.

To ensure good thermal conductivity the backside of the LM50 die is directly attached to the GND pin. The lands and traces to the LM50 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured. These printed circuit board lands and traces will not cause the LM50s temperature to deviate from the desired temperature.

Alternatively, the LM50 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM50 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM50 or its connections.

Temperature Rise of LM50 Due to Self-Heating (Thermal Resistance)

	SOT-23** no heat sink	SOT-23 small heat fin*
Still air	450°C/W	260°C/W
Moving air		180°C/W

* Heat sink used is ½" square printed circuit board with 2 oz. foil with part attached as shown in *Figure 2*.

** Part soldered to 30 gauge wire.

2.0 Capacitive Loads

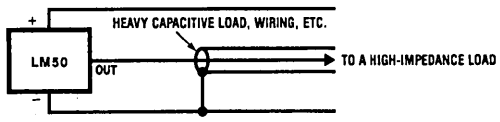

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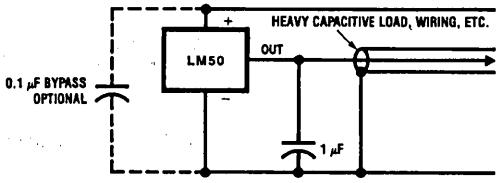
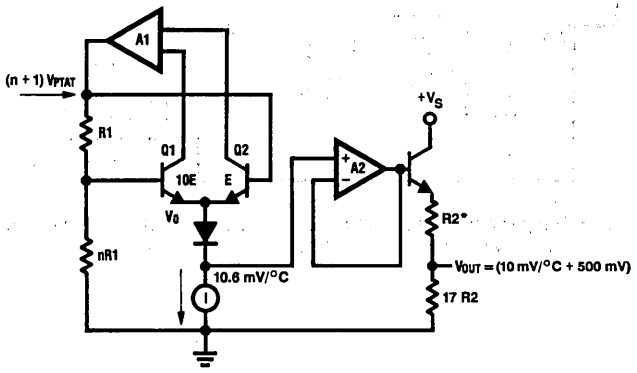
FIGURE 3. LM50 No Decoupling Required for Capacitive Load



TL/H/12030–8

FIGURE 4. LM50C with Filter for Noisy Environment

The LM50 handles capacitive loading very well. Without any special precautions, the LM50 can drive any capacitive load. The LM50 has a nominal 2 kΩ output impedance (as can be seen in the block diagram). The temperature coefficient of the output resistors is around 1300 ppm/°C. Taking into account this temperature coefficient and the initial tolerance of the resistors the output impedance of the LM50 will not exceed 4 kΩ. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that 0.1 μF be added from V_{IN} to GND to bypass the power supply voltage, as shown in *Figure 4*. In a noisy environment it may be necessary to add a capacitor from the output to ground. A 1 μF output capacitor with the 4 kΩ output impedance will form a 40 Hz lowpass filter. Since the thermal time constant of the LM50 is much slower than the 25 ms time constant formed by the RC, the overall response time of the LM50 will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM50.



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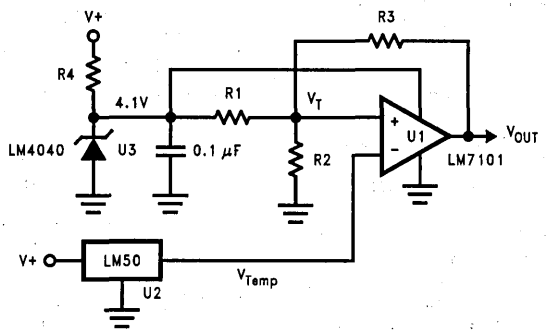
*R2 ≈ 2k with a typical 1300 ppm/°C drift.

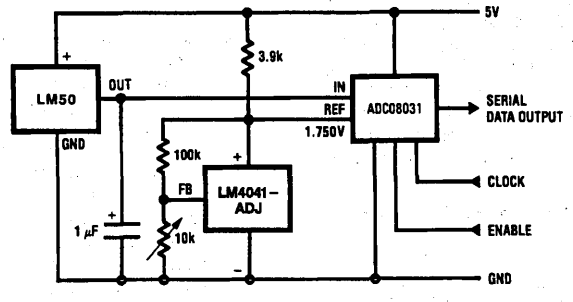
FIGURE 5. Block Diagram

3.0 Typical Applications



TL/H/12030–11

FIGURE 6. Centigrade Thermostat/Fan Controller



TL/H/12030–13

FIGURE 7. Temperature To Digital Converter (Serial Output) (+ 125°C Full Scale)

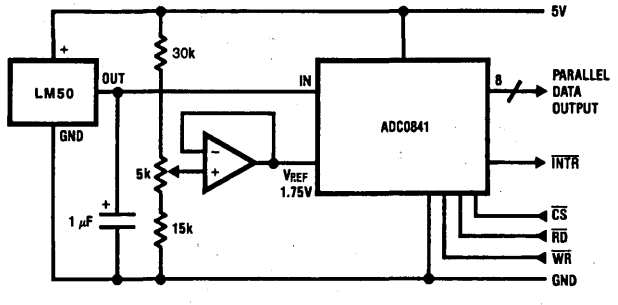


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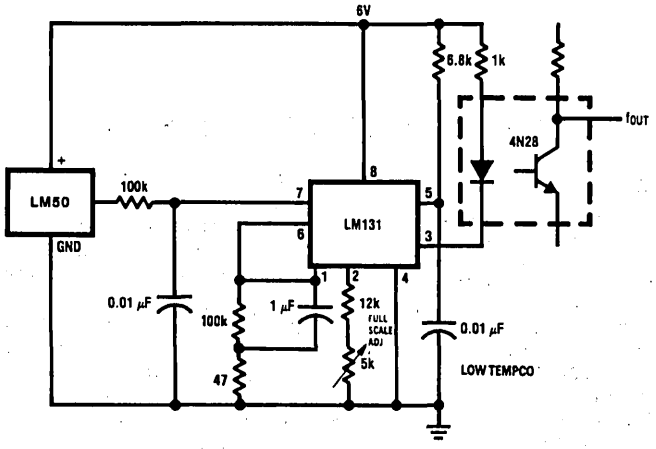
FIGURE 8. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (125°C Full Scale)

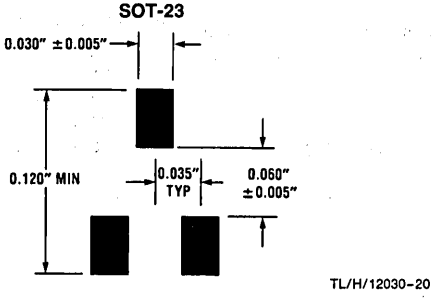
3.0 Typical Applications (Continued)



TL/H/12030–16

FIGURE 9. LM50 With Voltage-To-Frequency Converter And Isolated Output (−40°C to +125°C; 100 Hz to 1750 Hz)

4.0 Recommended Solder Pads for SOT-23 Package



TL/H/12030–20

National Semiconductor

LM4040
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4040 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4040's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4040 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

The LM4040 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Also available is the LM4041 with two reverse breakdown voltage versions: adjustable and 1.2V. Please see the LM4041 data sheet.

Features

- Small packages: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V
- Contact National Semiconductor Analog Marketing for parts with extended temperature range

Key Specifications (LM4040-2.5)

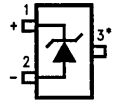
- Output voltage tolerance (A grade, 25°C) ±0.1% (max)
- Low output noise (10 Hz to 10 kHz) 35 μV_{rms} (typ)
- Wide operating current range 60 μA to 15 mA
- Industrial temperature range −40°C to +85°C
- Low temperature coefficient 100 ppm/°C (max)
- Contact National Semiconductor Analog Marketing for parts with lower temperature coefficient

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SOT-23



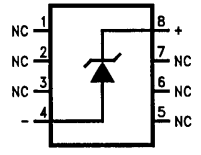
TL/H/11323-1

*This pin must be left floating or connected to pin 3.

Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

SO-8

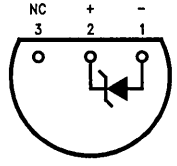


TL/H/11323-2

Top View

See NS Package Number M08A

TO-92



TL/H/11323-3

Bottom View

See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package		
	M3 (SOT-23)	Z (TO-92)	M (SO-8)
±0.1%, 100 ppm/°C max (A grade)	LM4040AIM3-2.5, LM4040AIM3-4.1, LM4040AIM3-5.0, LM4040AIM3-8.2, LM4040AIM3-10.0 **See NS Package Number M03B**	LM4040AIZ-2.5, LM4040AIZ-4.1, LM4040AIZ-5.0, LM4040AIZ-8.2, LM4040AIZ-10.0 **See NS Package Number Z03A**	LM4040AIM-2.5, LM4040AIM-4.1, LM4040AIM-5.0, LM4040AIM-8.2, LM4040AIM-10.0 **See NS Package Number M08A**
±0.2%, 100 ppm/°C max (B grade)	LM4040BIM3-2.5, LM4040BIM3-4.1, LM4040BIM3-5.0, LM4040BIM3-8.2, LM4040BIM3-10.0 **See NS Package Number M03B**	LM4040BIZ-2.5, LM4040BIZ-4.1, LM4040BIZ-5.0, LM4040BIZ-8.2, LM4040BIZ-10.0 **See NS Package Number Z03A**	LM4040BIM-2.5, LM4040BIM-4.1, LM4040BIM-5.0, LM4040BIM-8.2, LM4040BIM-10.0 **See NS Package Number M08A**
±0.5%, 100 ppm/°C max (C grade)	LM4040CIM3-2.5, LM4040CIM3-4.1, LM4040CIM3-5.0, LM4040CIM3-8.2, LM4040CIM3-10.0 **See NS Package Number M03B**	LM4040CIZ-2.5, LM4040CIZ-4.1, LM4040CIZ-5.0, LM4040CIZ-8.2, LM4040CIZ-10.0 **See NS Package Number Z03A**	LM4040CIM-2.5, LM4040CIM-4.1, LM4040CIM-5.0, LM4040CIM-8.2, LM4040CIM-10.0 **See NS Package Number M08A**
±1.0%, 150 ppm/°C max (D grade)	LM4040DIM3-2.5, LM4040DIM3-4.1, LM4040DIM3-5.0, LM4040DIM3-8.2, LM4040DIM3-10.0 **See NS Package Number M03B**	LM4040DIZ-2.5, LM4040DIZ-4.1, LM4040DIZ-5.0, LM4040DIZ-8.2, LM4040DIZ-10.0, **See NS Package Number Z03A**	LM4040DIM-2.5, LM4040DIM-4.1, LM4040DIM-5.0, LM4040DIM-8.2, LM4040DIM-10.0 **See NS Package Number M08A**
±2.0%, 150 ppm/°C max (E grade)	LM4040EIM3-2.5 **See NS Package Number M03B**	LM4040EIZ-2.5 **See NS Package Number Z03A**	

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R2A R4A R5A R8A R0A	First Field: R = Reference Second Field: 2 = 2.500V Voltage Option 4 = 4.096V Voltage Option 5 = 5.000V Voltage Option 8 = 8.192V Voltage Option 0 = 10.000V Voltage Option Third Field: A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = +0.5%, D = ±1.0%, E = ±2.0%
R2B R4B R5B R8B R0B	
R2C R4C R5C R8C R0C	
R2D R4D R5D R8D R0D	
R2E	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Power Dissipation (T_A = 25°C) (Note 2)	
M Package	540 mW
M3 Package	306 mW
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M and M3 Packages	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Z Package	
Soldering (10 seconds)	+260°C

ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range	
($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM4040-2.5	60 μA to 15 mA
LM4040-4.1	68 μA to 15 mA
LM4040-5.0	74 μA to 15 mA
LM4040-8.2	91 μA to 15 mA
LM4040-10.0	100 μA to 15 mA

LM4040-2.5

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±2.5 **±19**	±5.0 **±21**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.3	 0.8 **1.0**	 0.8 **1.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.3	 0.8	 0.8	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-2.5 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C, D and E designate initial Reverse Breakdown Voltage tolerances of ±0.5%, ±1.0% and ±2.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	LM4040EIM3 LM4040EIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	2.500				V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±12 **±29**	±25 **±49**	±50 **±74**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	 65 **70**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	 **±100**	 **±150**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.4	 0.8 **1.0**	 1.0 **1.2**	 1.0 **1.2**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	2.5	 6.0 **8.0**	 8.0 **10.0**	 8.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz $I_{AC} = 0.1\ I_R$	0.3	 0.9	 1.1	 1.1	Ω Ω(max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	35				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120				ppm

LM4040-4.1

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±4.1 **±31**	±8.2 **±35**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 68 **73**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 0.9 **1.2**	 0.9 **1.2**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.0	 7.0 **10.0**	 7.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	 1.0	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-4.1 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	4.096			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±20 **±47**	±41 **±81**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		50	 68 **73**	 73 **78**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 0.9 **1.2**	 1.2 **1.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.0	 7.0 **10.0**	 9.0 **13.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.0	 1.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-5.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	5.000			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±5.0 **±38**	±10 **±43**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 74 **80**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±30 ±20 ±20	 **±100** 	 **±100** 	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \leq I_R \leq$ 1 mA	0.5	 1.0 **1.4**	 1.0 **1.4**	mV mV (max) mV (max)
		1 mA ≤ $I_R \leq$ 15 mA	3.5	 8.0 **12.0**	 8.0 **12.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.1	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4040-5.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 µA	5.000			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 µA		±25 **±58**	±50 **±99**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		54	 74 **80**	 79 **85**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 µA	±30 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.5	 1.0 **1.3**	 1.3 **1.8**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	3.5	 8.0 **12.0**	 10.0 **15.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.1	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz	80			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA	120			ppm

LM4040-8.2

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±8.2 **±61**	±16 **±70**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 91 **95**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	**±100**	**±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.6	 1.3 **2.5**	 1.3 **2.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	7.0	 10.0 **18.0**	 10.0 **18.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-8.2 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	8.192			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±41 **±94**	±82 **±162**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		67	 91 **95**	 96 **100**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.6	 1.3 **2.5**	 1.7 **3.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	7.0	 10.0 **18.0**	 15.0 **24.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.6	 1.5	 1.9	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	130			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

LM4040-10.0

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040AIM LM4040AIM3 LM4040AIZ Limits (Note 5)	LM4040BIM LM4040BIM3 LM4040BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 µA	10.00			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 µA		±10 **±75**	±20 **±85**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 100 **103**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 µA	±40 ±20 ±20	 **±100**	 **±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.8	 1.5 **3.5**	 1.6 **3.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	8.0	 12.0 **23.0**	 12.0 **23.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	 1.7	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 µA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 µA	120			ppm

LM4040-10.0 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C and D designate initial Reverse Breakdown Voltage tolerances of ±0.5% and ±1.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4040CIM LM4040CIM3 LM4040CIZ Limits (Note 5)	LM4040DIM LM4040DIM3 LM4040DIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 150 μA	10.00			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 150 μA		±50 **±115**	±100 **±198**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		75	 100 **103**	 110 **113**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 150 μA	±40 ±20 ±20	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.8	 1.5 **3.5**	 2.0 **4.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 15 mA	8.0	 12.0 **23.0**	 18.0 **29.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.7	 1.7	 2.3	Ω Ω (max)
e_N	Wideband Noise	I_R = 150 μA 10 Hz ≤ f ≤ 10 kHz	180			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 150 μA	120			ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4040, T_{Jmax} = 125°C, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4" lead length and 170°C/W with 0.125" lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at T_J = 25°C and represent most likely parametric norm.

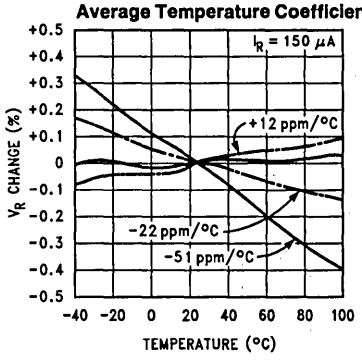
Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ± [($\Delta V_R/\Delta T$)(65°C)(V_R)]. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades is shown below:

A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C
Therefore, as an example, the A-grade LM4040-2.5 has an over-temperature Reverse Breakdown Voltage tolerance of ±2.5V × 0.75% = ±19 mV.

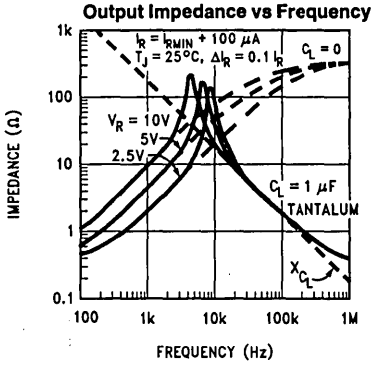
Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



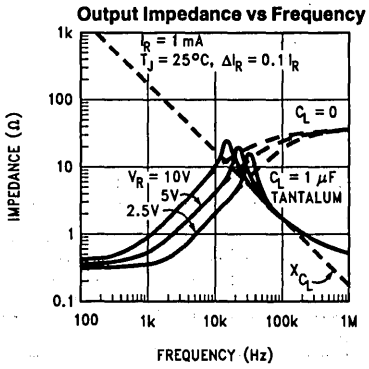
TL/H/11323-4

Output Impedance vs Frequency



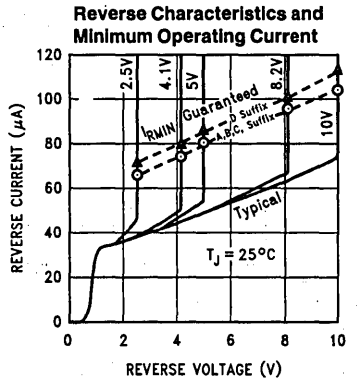
TL/H/11323-10

Output Impedance vs Frequency



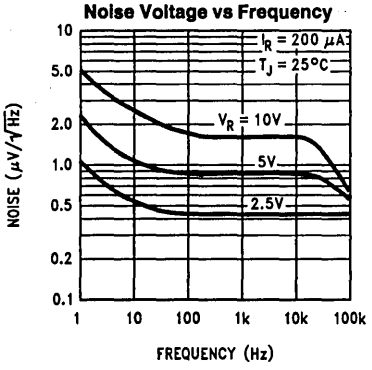
TL/H/11323-11

Reverse Characteristics and Minimum Operating Current



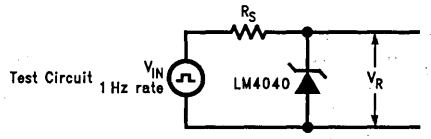
TL/H/11323-12

Noise Voltage vs Frequency

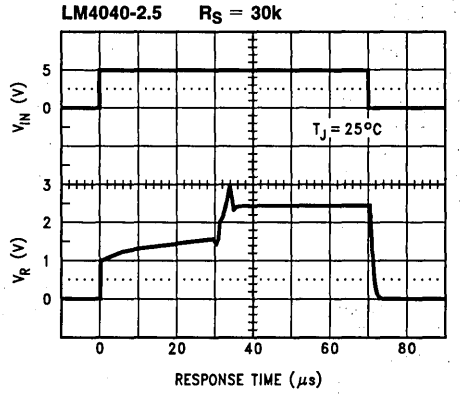


TL/H/11323-13

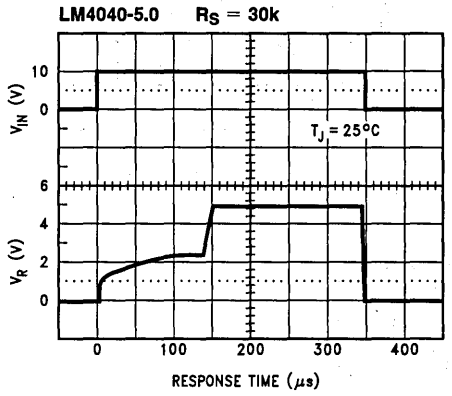
Start-Up Characteristics



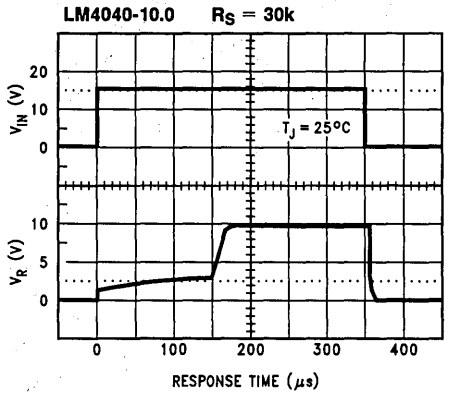
TL/H/11323–5



TL/H/11323–7

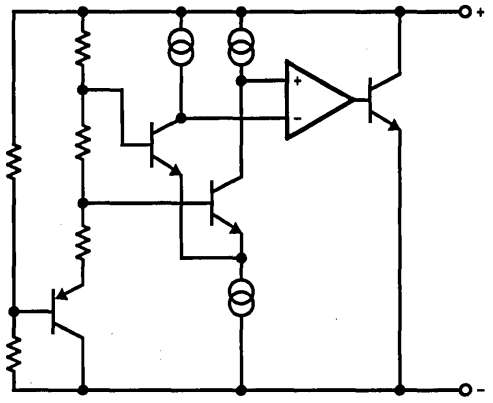


TL/H/11323–8



TL/H/11323–9

Functional Block Diagram



TL/H/11323–14

Applications Information

The LM4040 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4040 is available in the sub-miniature SOT-23 surface-mount package. The LM4040 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4040 remains stable. Reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 μA for the LM4040-2.5 to 100 μA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

LM4040s in the SOT-23 packages have a parasitic Schottky diode between pin 3 (−) and pin 1 (Die attach interface contact). Therefore, pin 1 of the SOT-23 package must be left floating or connected to pin 3.

The 4.096V version allows single +5V 12-bit ADCs or DACs to operate with an LSB equal to 1 mV. For 12-bit ADCs or DACs that operate on supplies of 10V or greater, the 8.192V version gives 2 mV per LSB.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4040. R_S determines the current that flows through the load (I_L) and the LM4040 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4040 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4040 is less than 15 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4040's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

Typical Applications

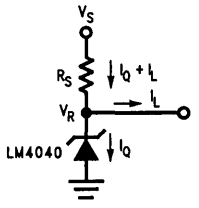


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FIGURE 1. Shunt Regulator

Typical Applications (Continued)

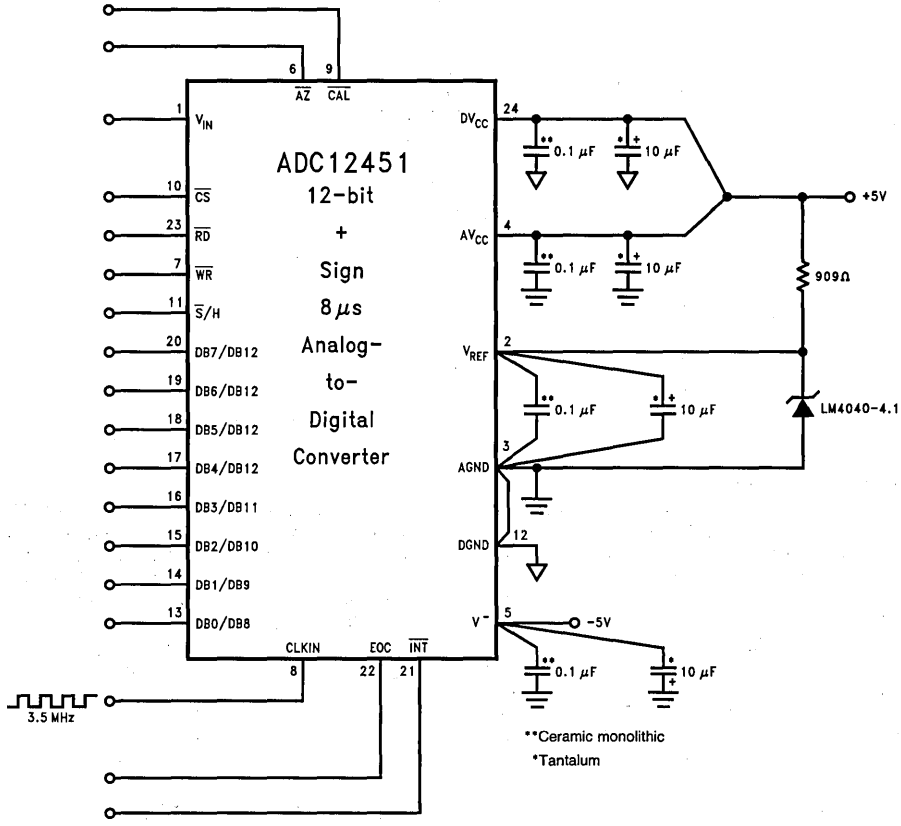
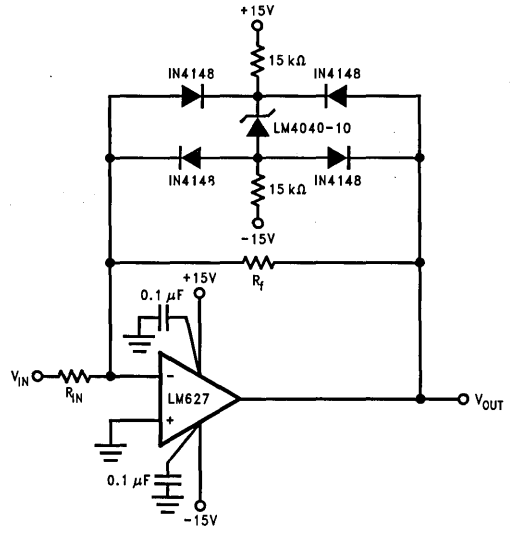


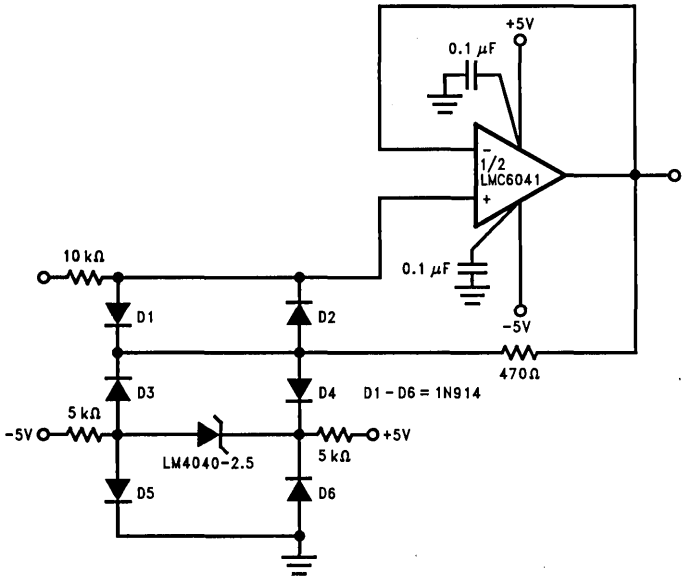
FIGURE 2. LM4040-4.1's Nominal 4.096 breakdown voltage gives ADC12451 1 mV/LSB TL/H/11323-16



TL/H/11323-17

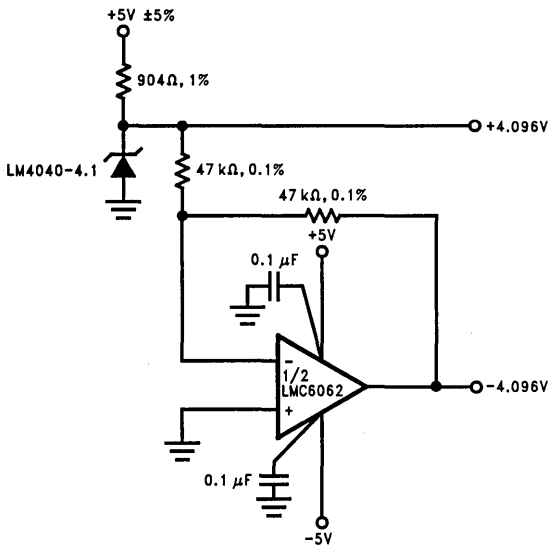
FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is ±11.5V (LM4040's reverse breakdown voltage +2 diode V_F).

Typical Applications (Continued)



TL/H/11323–18

FIGURE 4. Protecting Op Amp Input. The bounding voltage is ±4V with the LM4040-2.5 (LM4040's reverse breakdown voltage + 3 diode V_F).



TL/H/11323–19

FIGURE 5. Precision ±4.096V Reference

Typical Applications (Continued)

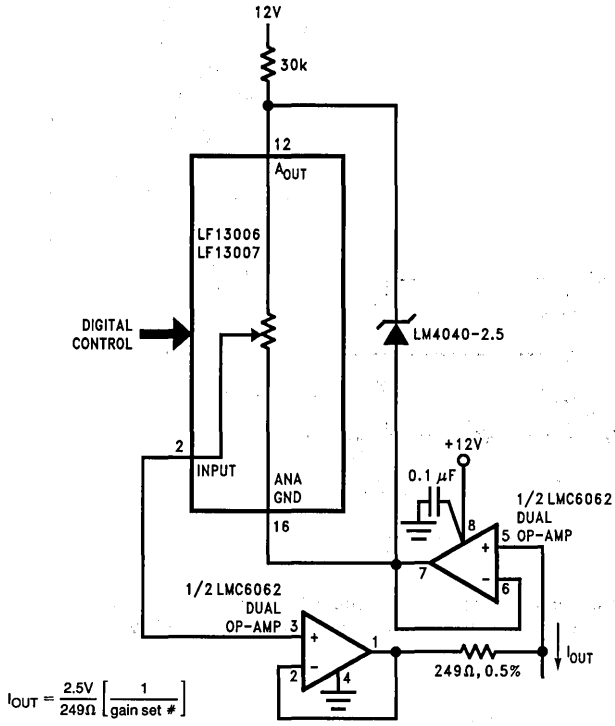


FIGURE 6. Programmable Current Source

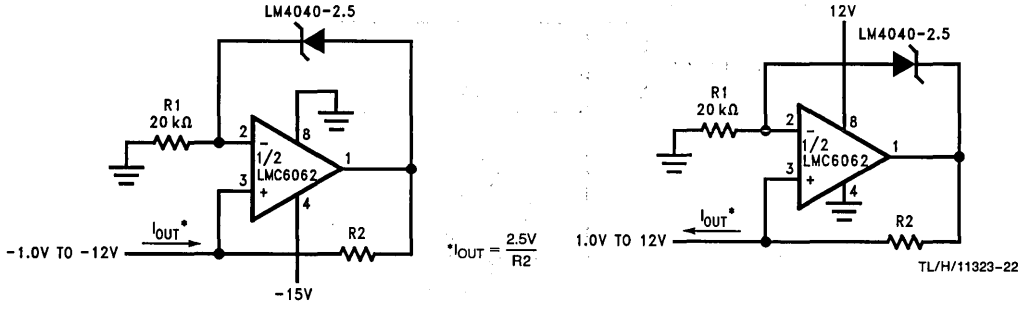


FIGURE 7. Precision 1 μA to 1 mA Current Sources

National Semiconductor

LM4041
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4041 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4041's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4041 easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60 μA for the LM4041-1.2 and the LM4041-ADJ. Both versions have a maximum operating current of 12 mA.

The LM4041 utilizes fuse and zener-zap reverse breakdown or reference voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Small packages: SOT-23, TO-92, and SO-8
- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable
- Contact National Semiconductor Analog Marketing for parts with extended temperature range

Key Specifications (LM4041-1.2)

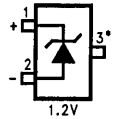
- Output voltage tolerance (A grade, 25°C) ±0.1% (max)
- Low output noise (10 Hz to 10 kHz) 20 μV_{rms} (typ)
- Wide operating current range 60 μA to 12 mA
- Industrial temperature range −40°C to +85°C
- Low temperature coefficient 100 ppm/°C (max)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

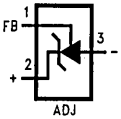
Connection Diagrams

SOT-23



TL/H/11392-1

*This pin must be left floating or connected to pin 3.

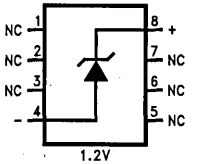


TL/H/11392-40

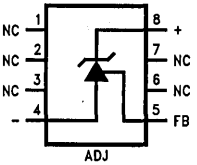
Top View

See NS Package Number M03B
(JEDEC Registration TO-236AB)

SO-8



TL/H/11392-2

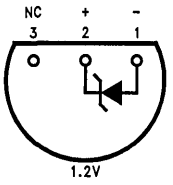


TL/H/11392-31

Top View

See NS Package Number M08A

TO-92



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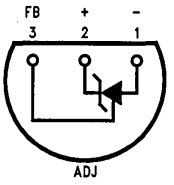


TL/H/11392-32

Bottom View
See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package		
	M3 (SOT-23)	Z (TO-92)	M (SO-8)
±0.1%, 100 ppm/°C max (A grade)	LM4041AIM3-1.2 **See NS Package Number M03B**	LM4041AIZ-1.2 **See NS Package Number Z03A**	LM4041AIM-1.2 **See NS Package Number M08A**
±0.2%, 100 ppm/°C max (B grade)	LM4041BIM3-1.2 **See NS Package Number M03B**	LM4041BIZ-1.2 **See NS Package Number Z03A**	LM4041BIM-1.2 **See NS Package Number M08A**
±0.5%, 100 ppm/°C max (C grade)	LM4041CIM3-1.2 LM4041CIM3-ADJ **See NS Package Number M03B**	LM4041CIZ-1.2, LM4041CIZ-ADJ **See NS Package Number Z03A**	LM4041CIM-1.2, LM4041CIM-ADJ **See NS Package Number M08A**
±1.0%, 150 ppm/°C max (D grade)	LM4041DIM3-1.2 LM4041DIM3-ADJ **See NS Package Number M03B**	LM4041DIZ-1.2, LM4041DIZ-ADJ **See NS Package Number Z03A**	LM4041DIM-1.2, LM4041DIM-ADJ **See NS Package Number M08A**
±2.0%, 150 ppm/°C max (E grade)	LM4041EIM3-1.2 **See NS Package Number M03B**	LM4041EIZ-1.2 **See NS Package Number Z03A**	

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R1A R1B R1C R1D R1E	First Field: R = Reference Second Field: 1 = 1.225V Voltage Option A = Adjustable Third Field: A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = ±0.5%, D = ±1.0%, E = ±2.0%
RAC RAD	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Maximum Output Voltage (LM4041-ADJ)	15V
Power Dissipation (T_A = 25°C) (Note 2)	
M Package	540 mW
M3 Package	306 mW
Z Package	550 mW
Storage Temperature	−65°C to +150°C
Lead Temperature	
M and M3 Packages	
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Z Package	
Soldering (10 seconds)	+260°C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 & 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	$-40°C \le T_A \le +85°C$
Reverse Current	
LM4041-1.2	60 μA to 12 mA
LM4041-ADJ	60 μA to 12 mA
Output Voltage Range	
LM4041-ADJ	1.24V to 10V

LM4041-1.2

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25°C. The grades A and B designate initial Reverse Breakdown Voltage tolerances of ±0.1% and ±0.2%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041AIM LM4041AIM3 LM4041AIZ Limits (Note 5)	LM4041BIM LM4041BIM3 LM4041BIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 μA	1.225			V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 μA		±1.2 **±9.2**	±2.4 **±10.4**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 60 **65**	μA μA (max) μA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 μA	±20 ±15 ±15	**±100**	**±100**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.7	 1.5 **2.0**	 1.5 **2.0**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 12 mA	4.0	 6.0 **8.0**	 6.0 **8.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$	0.5	 1.5	 1.5	Ω Ω (max)
e_N	Wideband Noise	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	20			μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 μA	120			ppm

LM4041-1.2 (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. The grades C, D and E designate initial Reverse Breakdown Voltage tolerances of ±0.5%, ±1.0% and ±2.0%, respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ Limits (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ Limits (Note 5)	LM4041EIM3 LM4041EIZ Limits (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 µA	1.225				V
	Reverse Breakdown Voltage Tolerance (Note 6)	I_R = 100 µA		±6 **±14**	±12 **±24**	±25 **±36**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	 65 **70**	µA µA (max) µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient	I_R = 10 mA I_R = 1 mA I_R = 100 µA	±20 ±15 ±15	 **±100**	 **±150**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.7	 1.5 **2.0**	 2.0 **25**	 2.0 **2.5**	mV mV (max) mV (max)
		1 mA ≤ $I_R \le$ 12 mA	2.5	 6.0 **8.0**	 8.0 **10.0**	 8.0 **10.0**	mV mV (max) mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz I_{AC} = 0.1 I_R	0.5	 1.5	 2.0	 2.0	Ω Ω(max)
e_N	Wideband Noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz	20				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	t = 1000 hrs T = 25°C ±0.1°C I_R = 100 µA	120				ppm

LM4041-ADJ (Adjustable)

Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C unless otherwise specified (SOT-23, see Note 7), $I_{RMIN} \le I_R \le$ 12 mA, $V_{REF} \le V_{OUT} \le$ 10V. The grades C and D designates initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for V_{OUT} = 5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ (Note 5)	Units (Limit)
V_{REF}	Reference Voltage	I_R = 100 µA, V_{OUT} = 5V	1.233			V
	Reference Voltage Tolerance (Note 8)	I_R = 100 µA, V_{OUT} = 5V		±6.2 **±14**	±12 **±24**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		45	 60 **65**	 65 **70**	µA µA (max) µA (max)

LM4041-ADJ (Adjustable) (Continued)

Electrical Characteristics (Continued)

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$ unless otherwise specified (SOT-23, see Note 7), $I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10V$. The grades C and D designates initial Reference Voltage Tolerances of ±0.5% and ±1%, respectively for $V_{OUT} = 5V$.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4041CIM LM4041CIM3 LM4041CIZ (Note 5)	LM4041DIM LM4041DIM3 LM4041DIZ (Note 5)	Units (Limit)
$\Delta V_{REF}/\Delta I_R$	Reference Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le 1$ mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	0.7	 1.5 **2.0**	 2.0 **2.5**	mV mV (max) mV (max)
		1 mA $\le I_R \le$ 12 mA SOT-23: $V_{OUT} \ge 1.6V$ (Note 7)	2	 4 **6**	 6 **8**	mV mV (max) mV (max)
$\Delta V_{REF}/\Delta V_O$	Reference Voltage Change with Output Voltage Change	$I_R = 1$ mA	−1.3	 −2.0 **−2.5**	 −2.5 **−3.0**	mV/V mV/V (max) mV/V (max)
I_{FB}	Feedback Current		60	 100 **120**	 150 **200**	nA nA (max) nA (max)
$\Delta V_{REF}/\Delta T$	Average Reference Voltage Temperature Coefficient (Note 8)	$V_{OUT} = 5V$, $I_R = 10$ mA $I_R = 1$ mA $I_R = 100\ \mu A$	20 15 15	 **±100**	 **±150**	ppm/°C ppm/°C (max) ppm/°C
Z_{OUT}	Dynamic Output Impedance	$I_R = 1$ mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$ $V_{OUT} = V_{REF}$ $V_{OUT} = 10V$	 0.3 2			 Ω Ω
e_N	Wideband Noise	$I_R = 100\ \mu A$ $V_{OUT} = V_{REF}$ 10 Hz ≤ f ≤ 10 kHz	20			μV_{rms}
ΔV_{REF}	Reference Voltage Long Term Stability	t = 1000 hrs, $I_R = 100\ \mu A$ T = 25°C ±0.1°C	120			ppm

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4041, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}), when board mounted, is 185°C/W for the M package, 326°C/W for the SOT-23 package, and 180°C/W with 0.4" lead length and 170°C/W with 0.125" lead length for the TO-92 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 5: Limits are 100% production tested at 25°C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance ±[($\Delta V_R/\Delta T$)(65°C)(V_R)]. $\Delta V_R/\Delta T$ is the V_R temperature coefficient, 65°C is the temperature range from −40°C to the reference point of 25°C, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades is shown below:

A-grade: ±0.75% = ±0.1% ±100 ppm/°C × 65°C
B-grade: ±0.85% = ±0.2% ±100 ppm/°C × 65°C
C-grade: ±1.15% = ±0.5% ±100 ppm/°C × 65°C
D-grade: ±1.98% = ±1.0% ±150 ppm/°C × 65°C
E-grade: ±2.98% = ±2.0% ±150 ppm/°C × 65°C

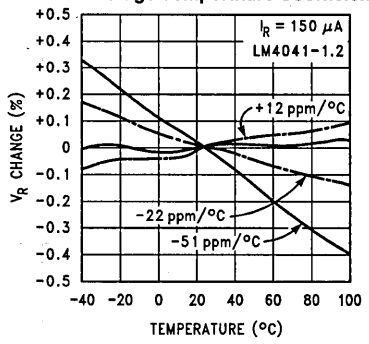
Therefore, as an example, the A-grade LM4041-1.2 has an over-temperature Reverse Breakdown Voltage tolerance of ±1.2V × 0.75% = ±9.2 mV.

Note 7. When $V_{OUT} \le 1.6V$, the LM4041-ADJ in the SOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (-) output and the package (-) output pin. See the Output Saturation (SOT-23 only) curve in the Typical Performance Characteristics section.

Note 8. Reference voltage and temperature coefficient will change with output voltage. See Typical Performance Characteristics curves.

Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient



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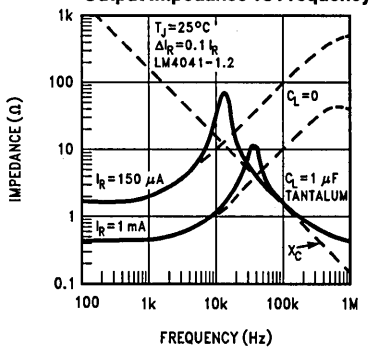
Output Impedance vs Frequency



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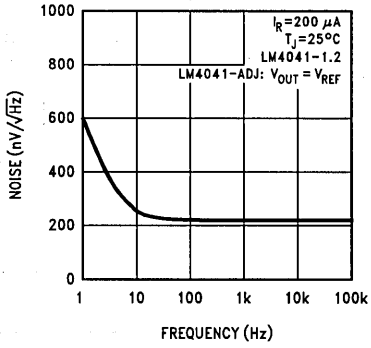
Noise Voltage



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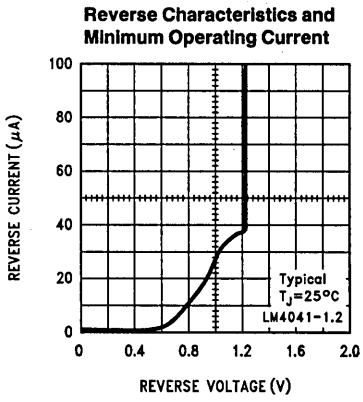
Reverse Characteristics and Minimum Operating Current



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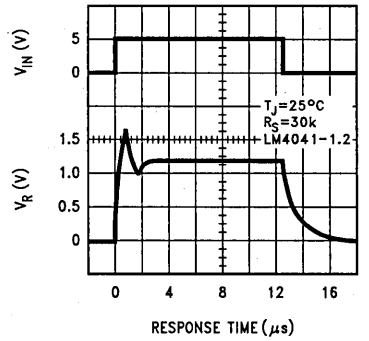

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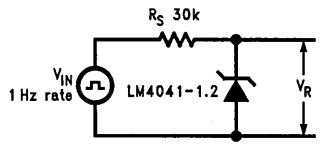

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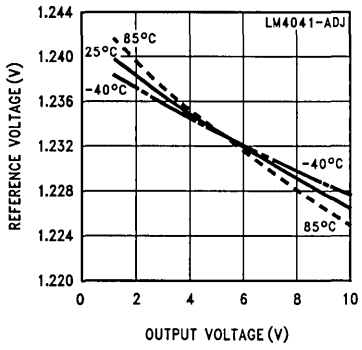
Typical Performance Characteristics (Continued)

Reference Voltage vs Output Voltage and Temperature



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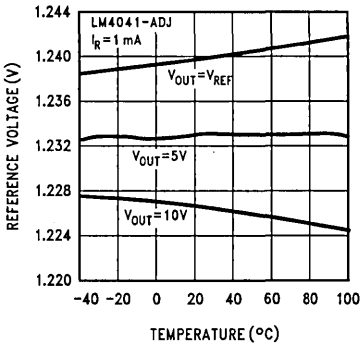
Reference Voltage vs Temperature and Output Voltage



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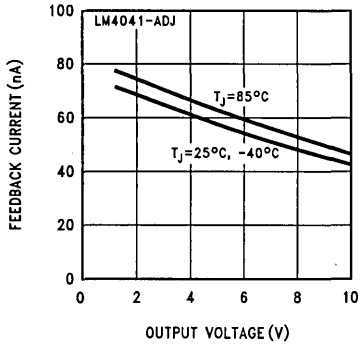
Feedback Current vs Output Voltage and Temperature



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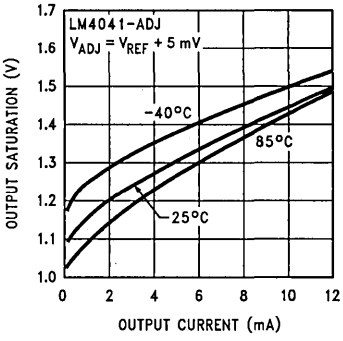
Output Saturation (SOT-23 Only)



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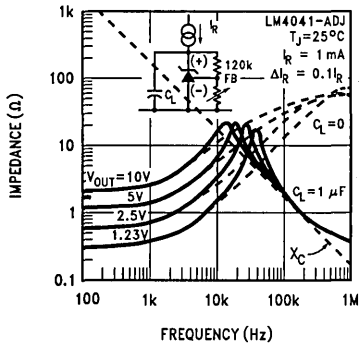
Output Impedance vs Frequency



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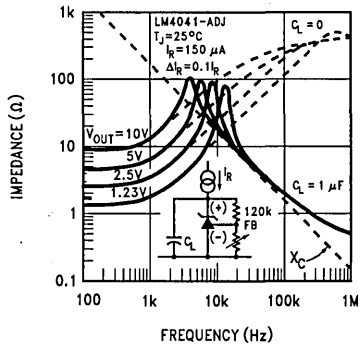
Output Impedance vs Frequency



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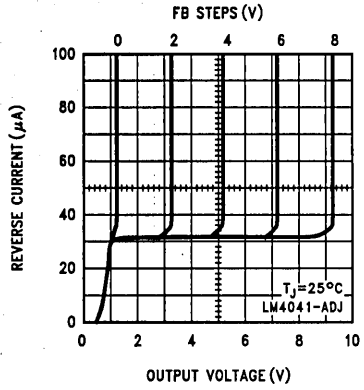
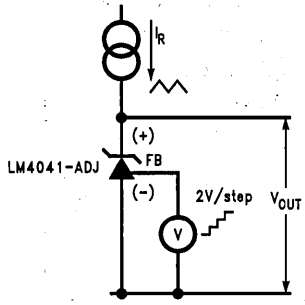
Typical Performance Characteristics (Continued)

Reverse Characteristics



TL/H/11392–15



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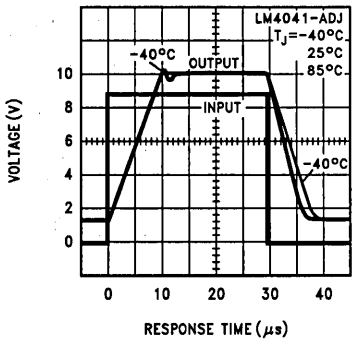
Large Signal Response



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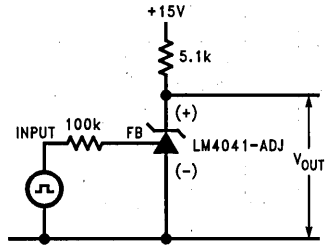

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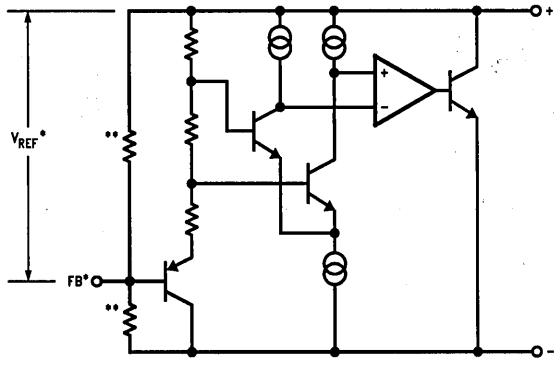
Functional Block Diagram



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*LM4041-ADJ only
**LM4041-1.2 only

Applications Information

The LM4041 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4041 is available in the sub-miniature SOT-23 surface-mount package. The LM4041 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4041 remains stable. Design effort is further reduced with the choice of either a fixed 1.2V or an adjustable reverse breakdown voltage. The minimum operating current is 60 μA for the LM4041-1.2 and the LM4041-ADJ. Both versions have a maximum operating current of 12 mA.

LM4041s using the SOT-23 package have pin 1 connected as the (-) output through the package's die attach interface. Therefore, the LM4041-1.2's pin 1 must be left floating or connected to pin 3 and the LM4041-ADJ's pin 1 is the (-) output.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4041. R_S determines the current that flows through the load (I_L) and the LM4041 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4041 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4041 is less than 12 mA.

R_S is determined by the supply voltage, (V_S), the load and operating current, (I_L and I_Q), and the LM4041's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

The LM4041-ADJ's output voltage can be adjusted to any value in the range of 1.24V through 10V. It is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in *Figure 2*. The output is found using the equation

$$V_O = V_{REF}' \left(\frac{R2}{R1} + 1\right) \quad (1)$$

where V_O is the desired output voltage. The actual value of the internal V_{REF} is a function of V_O. The "corrected" V_{REF} is determined by

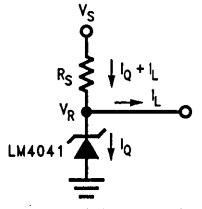
$$V_{REF}' = V_O (\Delta V_{REF}/\Delta V_O) + V_Y \quad (2)$$

where V_O is the desired output voltage. $\Delta V_{REF}/\Delta V_O$ is found in the Electrical Characteristics and it typically −1.3 mV/V and V_Y is equal to 1.240V. Replace the value of V_{REF}' in equation (1) with the value found using equation (2).

Note that the actual output voltage can deviate from that predicted using the typical $\Delta V_{REF}/\Delta V_O$ in equation (2): for C-grade parts, the worst-case $\Delta V_{REF}/\Delta V_O$ is −2.5 mV/V and V_Y = 1.246V. For D-grade parts, the worst-case $\Delta V_{REF}/\Delta V_O$ is −3.0 mV/V and V_Y = 1.248V.

The following example shows the difference in output voltage resulting from the typical and worst case values of $\Delta V_{REF}/\Delta V_O$. Let V_O = +9V. Using the typical value of $\Delta V_{REF}/\Delta V_O$, V_{REF} is 1.228V. Choosing a value of R1 = 10 kΩ, R2 = 63.272 kΩ. Using the worst case $\Delta V_{REF}/\Delta V_O$ for the C-grade and D-grade parts, the output voltage is actually 8.965V and 8.946V, respectively. This results in possible errors as large as 0.39% for the C-grade parts and 0.59% for the D-grade parts. Once again, resistor values found using the typical value of $\Delta V_{REF}/\Delta V_O$ will work in most cases, requiring no further adjustment.

Typical Applications



TL/H/11392-22

FIGURE 1. Shunt Regulator

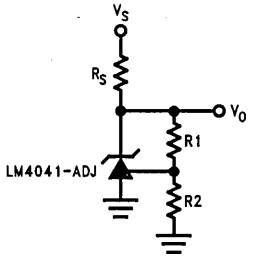


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FIGURE 2. Adjustable Shunt Regulator

Typical Applications (Continued)

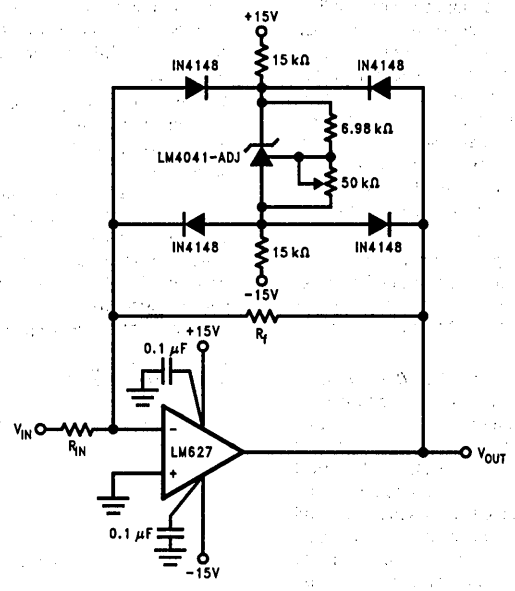

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FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is $\pm V_O$ (LM4041's reverse breakdown voltage) + 2 diode V_F.

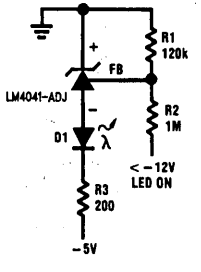

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FIGURE 4. Voltage Level Detector

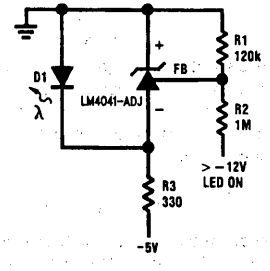

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FIGURE 5. Voltage Level Detector

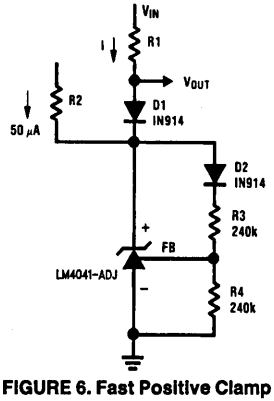

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FIGURE 6. Fast Positive Clamp
2.4V + ΔV_{D1}

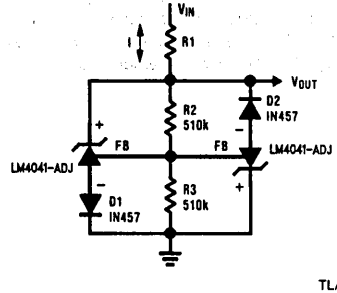

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FIGURE 7. Bidirectional Clamp ±2.4V

Typical Applications (Continued)

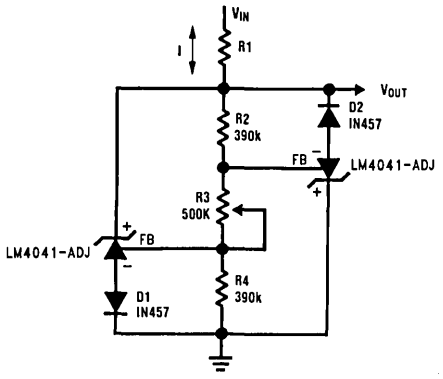

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FIGURE 7. Bidirectional Adjustable Clamp ±18V to ±2.4V

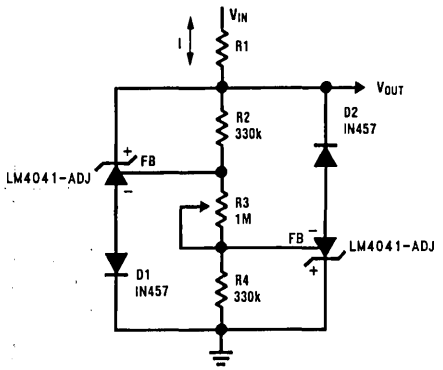

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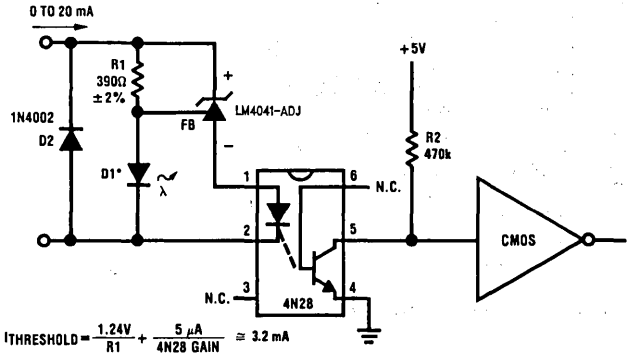
FIGURE 8. Bidirectional Adjustable Clamp ±2.4V to ±6V



TL/H/11392-37

FIGURE 9. Simple Floating Current Detector

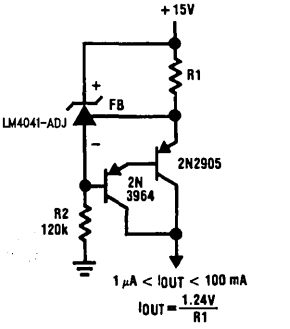


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FIGURE 10. Current Source

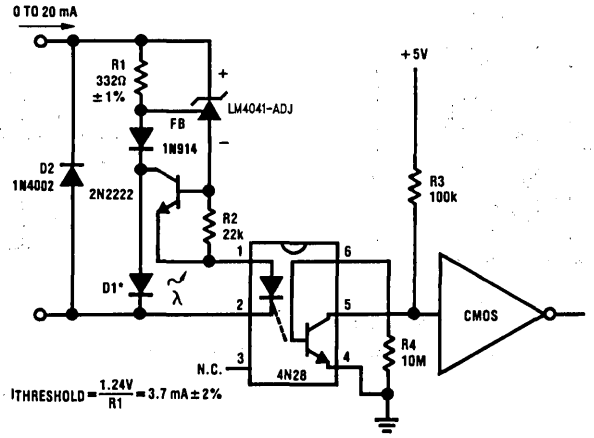

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FIGURE 11. Precision Floating Current Detector

*D1 can be any LED, V_F = 1.5V to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

Typical Applications (Continued)

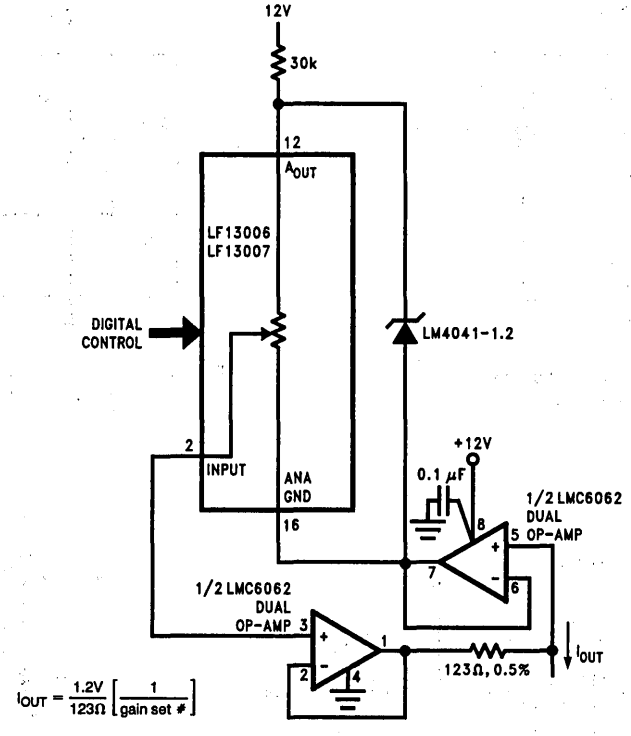


FIGURE 12. Programmable Current Source

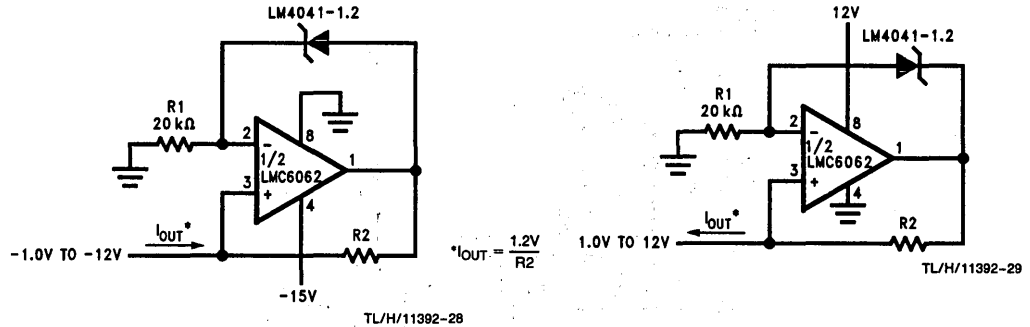


FIGURE 13. Precision 1 μA to 1 mA Current Sources

National Semiconductor

LP2950/A-XX and LP2951/A-XX Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 μA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 in the popular 3-pin TO-92 package is pin-compatible with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Features

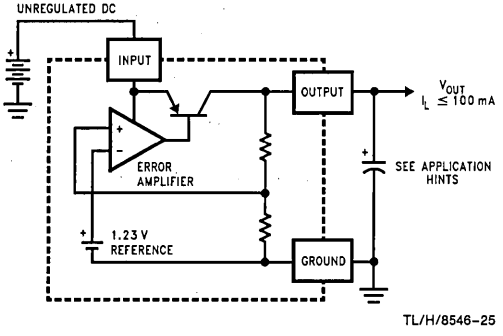
- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting

LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Typical Applications

LP2950/A-XX



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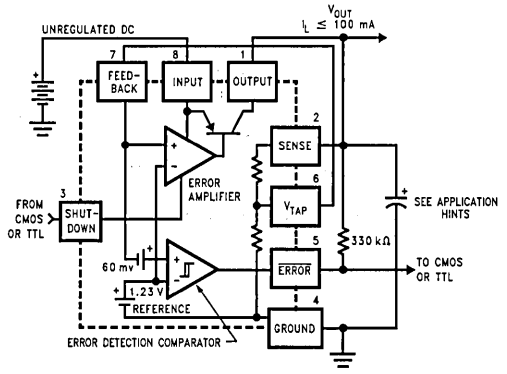
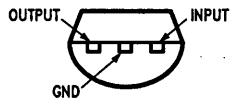
LP2951/A-XX



TL/H/8546–1

Connection Diagrams

TO-92 Plastic Package (Z)

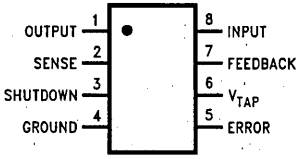


TL/H/8546-2

Bottom View

Order Number LP2950ACZ-3.0, LP2950CZ-3.0, LP2950ACZ-3.3, LP2950CZ-3.3 LP2950ACZ-5.0 or LP2950CZ-5.0
See NS Package Number Z03A

Dual-In-Line Packages (N, J)
Surface-Mount Package (M)



TL/H/8546-26

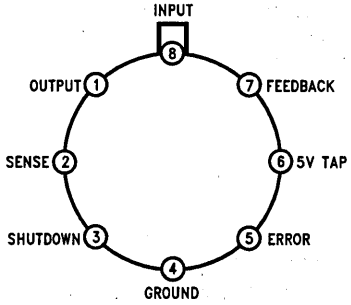
Top View

Order Number LP2951CJ, LP2951ACJ, LP2951J, LP2951J/883 or 5962-3870501MPA
See NS Package Number J08A

Order Number LP2951ACN, LP2951CN, LP2951ACN-3.0, LP2951CN-3.0, LP2951ACN-3.3 or LP2951CN-3.3
See NS Package Number N08E

Order Number LP2951ACM, LP2951CM, LP2951ACM-3.0, LP2951CM-3.0, LP2951ACM-3.3 or LP2951CM-3.3
See NS Package Number M08A

Metal Can Package (H)

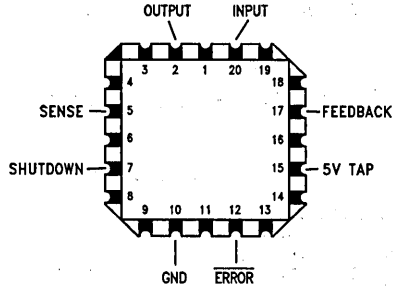


TL/H/8546-19

Top View

Order Number LP2951H/883 or 5962-3870501MGA
See NS Package Number H08C

Leadless Chip Carrier (E)



TL/H/8546-24

Top View

Order Number LP2951E/883 or 5962-3870501M2A
See NS Package Number E20A

Ordering Information

Package	Output Voltage			Temperature (°C)
	3.0V	3.3V	5.0V	
TO-92 (Z)	LP2950ACZ-3.0 LP2950CA-3.0	LP2950ACZ-3.3 LP2950CZ-3.3	LP2950ACZ-5.0 LP2950CZ-5.0	$-40 < T_J < 125$
N (N-08E)	LP2951ACN-3.0 LP2951CN-3.0	LP2951ACN-3.3 LP2951CN-3.3	LP2951ACN LP2950CN	$-40 < T_J < 125$
M (M08A)	LP2951ACM-3.0 LP2951CM-3.0	LP2951ACM-3.3 LP2951CM-3.3	LP2951ACM LP2951CM	$-40 < T_J < 125$
J (J08A)			LP2951ACJ LP2951CJ LP2951J LP2951J/883 5926-3870501MPA	$-40 < T_J < 125$ $-55 < T_J < 150$
H (H08C)			LP2951H/883 5962-3870501MGA	$-55 < T_J < 150$
E (E20A)			LP2951E/883 5962-3870501M2A	$-55 < T_J < 150$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	−65° to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951	−55° to +150°C
LP2950AC-XX, LP2950C-XX, LP2951AC-XX, LP2951C-XX	−40° to +125°C
Input Supply Voltage	−0.3 to +30V
Feedback Input Voltage (Notes 9 and 10)	−1.5 to +30V
Shutdown Input Voltage (Note 9)	−0.3 to +30V
Error Comparator Output Voltage (Note 9)	−0.3 to +30V
ESD Rating is to be determined.	

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
3V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	3.0	3.015 2.985	3.0	3.015 2.985		3.0	3.030 2.970		V max V min
	−25°C ≤ T_J ≤ 85°C	3.0		3.0		3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	**3.036** **2.964**	3.0		**3.036** **2.964**	3.0		**3.060** **2.940**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.0	**3.045** **2.955**	3.0		**3.042** **2.958**	3.0		**3.072** **2.928**	V max V min
3.3V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	3.3	3.317 3.284	3.3	3.317 3.284		3.3	3.333 3.267		V max V min
	−25°C ≤ T_J ≤ 85°C	3.3		3.3		3.333 3.267	3.3		3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	**3.340** **3.260**	3.3		**3.340** **3.260**	3.3		**3.366** **3.234**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	3.3	**3.350** **3.251**	3.3		**3.346** **3.254**	3.3		**3.379** **3.221**	V max V min
5V VERSIONS (Note 17)										
Output Voltage	T_J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	−25°C ≤ T_J ≤ 85°C	5.0		5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	**5.06** **4.94**	5.0		**5.06** **4.94**	5.0		**5.1** **4.9**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ T_{JMAX}	5.0	**5.075** **4.925**	5.0		**5.075** **4.925**	5.0		**5.12** **4.88**	V max V min
ALL VOLTAGE OPTIONS										
Output Voltage Temperature Coefficient	(Note 12)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation (Note 14)	(V_ONOM + 1)V ≤ V_{in} ≤ 30V (Note 15)	0.03	0.1 **0.5**	0.03	0.1	**0.2**	0.04	0.2	**0.4**	% max % max
Load Regulation (Note 14)	100 μA ≤ I_L ≤ 100 mA	0.04	0.1 **0.3**	0.04	0.1	**0.2**	0.1	0.2	**0.3**	% max % max

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
ALL VOLTAGE OPTIONS (Continued)										
Dropout Voltage (Note 5)	I_L = 100 µA	50	80 **150**	50	80	 **150**	50	80	 **150**	mV max mV max
	I_L = 100 mA	380	450 **600**	380	450	 **600**	380	450	 **600**	mV max mV max
Ground Current	I_L = 100 µA	75	120 **140**	75	120	 **140**	75	120	 **140**	µA max µA max
	I_L = 100 mA	8	12 **14**	8	12	 **14**	8	12	 **14**	mA max mA max
Dropout Ground Current	V_{in} = (V_ONOM − 0.5)V I_L = 100 µA	110	170 **200**	110	170	 **200**	110	170	 **200**	µA max µA max
Current Limit	V_{out} = 0	160	200 **220**	160	200	 **220**	160	200	 **220**	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 KHz	C_L = 1 µF (5V Only)	430		430			430			µV rms
	C_L = 200 µF	160		160			160			µV rms
	C_L = 3.3 µF (Bypass = 0.01 µF Pins 7 to 1 (LP2951))	100		100			100			µV rms
8-PIN VERSIONS ONLY		LP2951		LP2951AC-XX			LP2951C-XX			
Reference Voltage		1.235	1.25 **1.26** 1.22 **1.2**	1.235	1.25 1.22	 **1.26** **1.2**	1.235	1.26 1.21	 **1.27** **1.2**	V max V max V min V min
Reference Voltage	(Note 7)		**1.27** **1.19**			**1.27** **1.19**			**1.285** **1.185**	V max V min
Feedback Pin Bias Current		20	40 **60**	20	40	 **60**	20	40	 **60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1 **2**	0.01	1	 **2**	0.01	1	 **2**	µA max µA max
Output Low Voltage	V_{in} = (V_ONOM − 0.5)V I_{OL} = 400 µA	150	250 **400**	150	250	 **400**	150	250	 **400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	 **25**	60	40	 **25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	 **140**	75	95	 **140**	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2951AC-XX			LP2951C-XX			Units
		Typ	Tested Limit (Notes 3, 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
8-PIN VERSIONS ONLY (Continued)										
Shutdown Input										
Input Logic Voltage	Low (Regulator ON)	1.3	**0.6**	1.3		**0.7**	1.3		**0.7**	V V max
	High (Regulator OFF)		**2.0**			**2.0**			**2.0**	V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50 **100**	30	50	 **100**	30	50	 **100**	µA max µA max
	$V_{shutdown}$ = 30V	450	600 **750**	450	600	 **750**	450	600	 **750**	µA max µA max
Regulator Output Current in Shutdown	(Note 11)	3	10 **20**	3	10	 **20**	3	10	 **20**	µA max µA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for T_J = 25°C, V_{in} = (V_ONOM + 1)V, I_L = 100 µA and C_L = 1 µF for 5V versions, and 2.2 µF for 3V and 3.3V versions. Additional conditions for the 8-pin versions are Feedback tied to V_{TAP}, Output tied to Output Sense and $V_{shutdown} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V **(2.3V over temperature)** must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V_ONOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, $2.3V \leq V_{in} \leq 30V$, 100 µA $\leq I_L \leq$ 100 mA, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistance of the 8-pin DIP packages is 105°C/W for the molded plastic (N) and 130°C/W for the cerdip (J) junction to ambient when soldered directly to a PC board. Thermal resistance for the metal can (H) is 160°C/W junction to ambient and 20°C/W junction to case. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W. Thermal resistance for the leadless chip carrier (E) package is 95°C/W junction to ambient and 24°C/W junction to case.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \geq 2V$, $V_{in} \leq 30V$, V_{out} = 0, Feedback pin tied to V_{TAP}.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10 ms.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

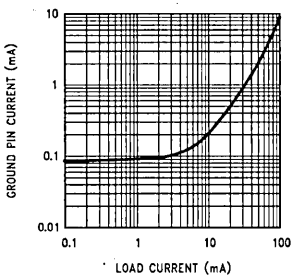
Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1 mA. For I_L = 100 µA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Note 16: A Military RETS spec is available on request. At time of printing, the LP2951 RETS spec complied with the boldface limits in this column. The LP2951H, E, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, M2A, or MPA.

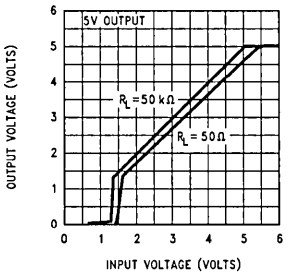
Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).

Typical Performance Characteristics

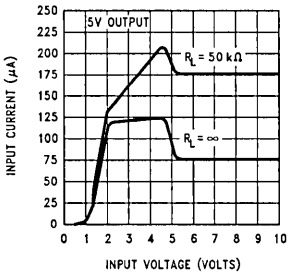
Quiescent Current



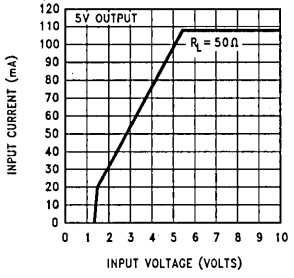
Dropout Characteristics



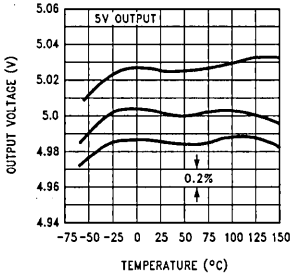
Input Current



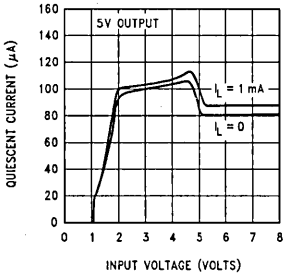
Input Current



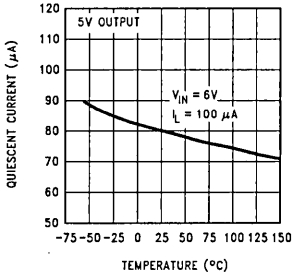
Output Voltage vs. Temperature of 3 Representative Units



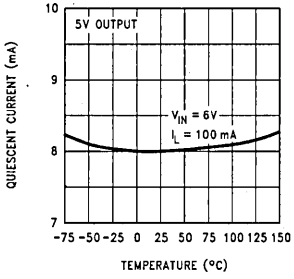
Quiescent Current



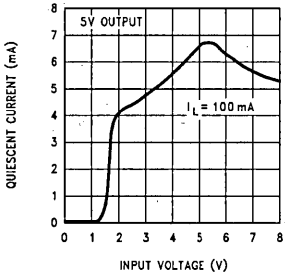
Quiescent Current



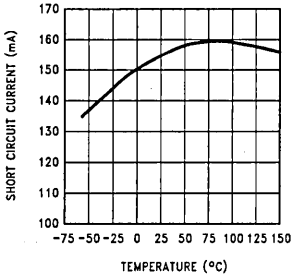
Quiescent Current



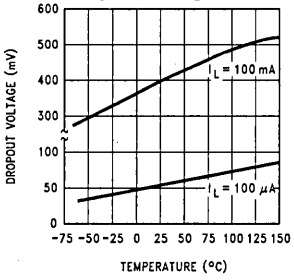
Quiescent Current



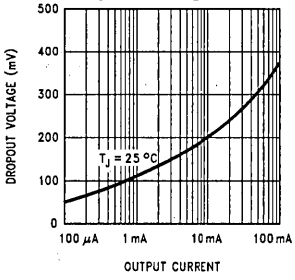
Short Circuit Current



Dropout Voltage



Dropout Voltage



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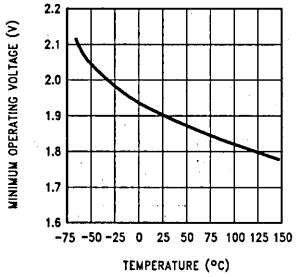
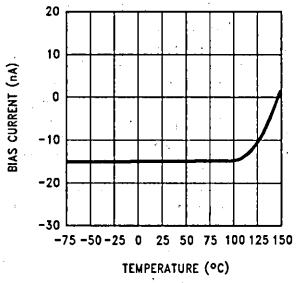
7

Typical Performance Characteristics (Continued)

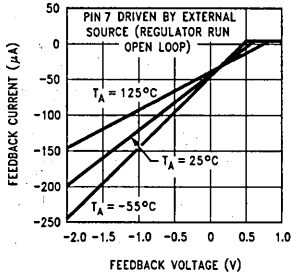
LP2951
Minimum Operating Voltage



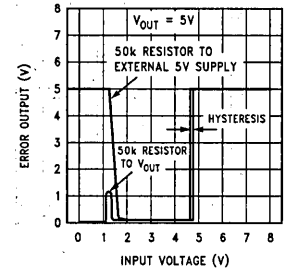
LP2951
Feedback Bias Current



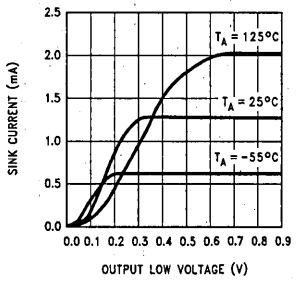
LP2951
Feedback Pin Current



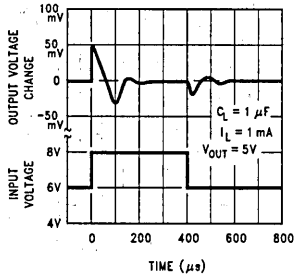
LP2951
Error Comparator Output



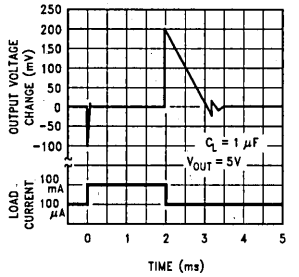
LP2951
Comparator Sink Current



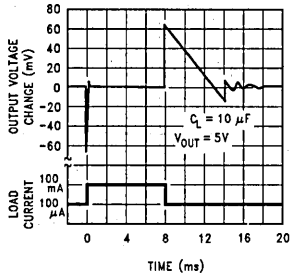
Line Transient Response



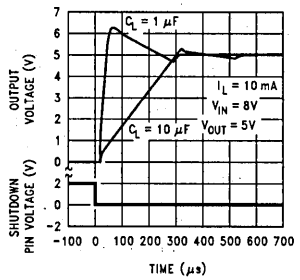
Load Transient Response



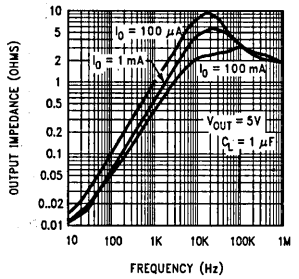
Load Transient Response



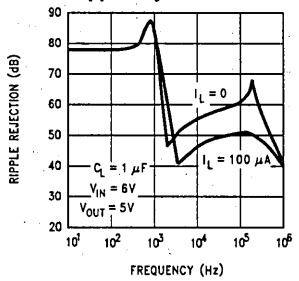
LP2951
Enable Transient



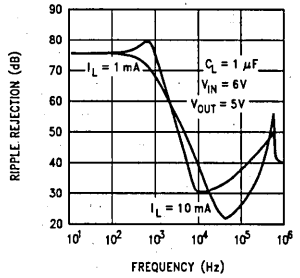
Output Impedance



Ripple Rejection



Ripple Rejection



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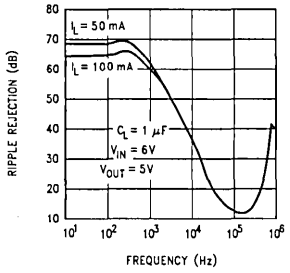
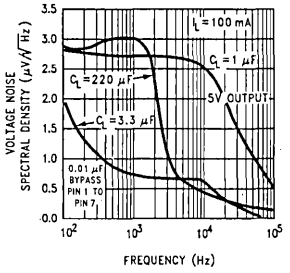
Typical Performance Characteristics (Continued)

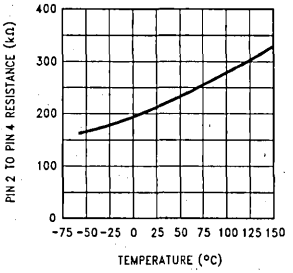
Ripple Rejection



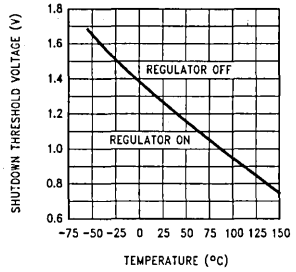
LP2951 Output Noise



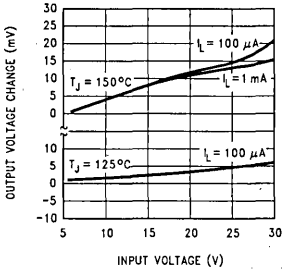
LP2951 Divider Resistance



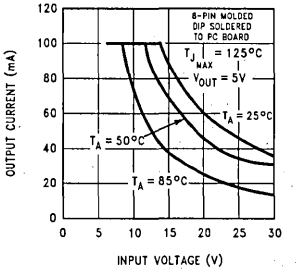
Shutdown Threshold Voltage



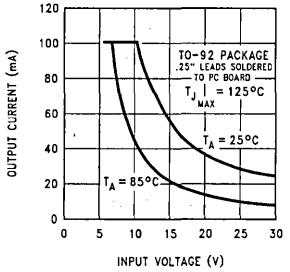
Line Regulation



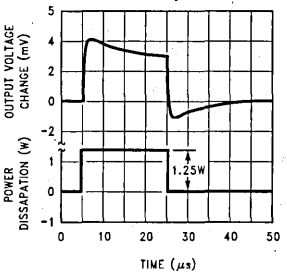
LP2951 Maximum Rated Output Current



LP2950 Maximum Rated Output Current



Thermal Response



TL/H/8546–5

Application Hints

EXTERNAL CAPACITORS

A 1.0 µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required (2.2 µF or more is recommended for 3V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µF for currents below 10 mA or 0.1 µF for currents below 1 mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 µF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 versions with external resistors, a minimum load of 1 µA is recommended.

A 1 µF tantalum or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Application Hints (Continued)

Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μF will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

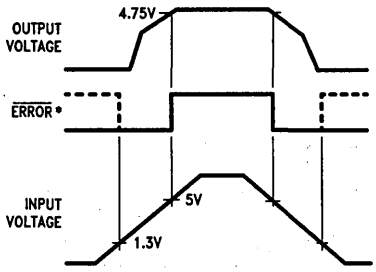
The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **Input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2*, an external pair of resistors is required.



TL/H/8546–20

*When $V_{IN} \leq$ 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see *Figure 2*), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

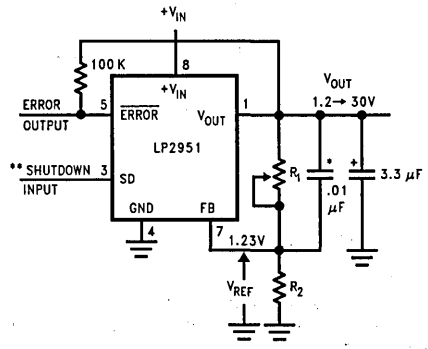
REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 μV to 160 μV rms for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ \text{Hz}}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



TL/H/8546–7

FIGURE 2. Adjustable Regulator

*See Application Hints

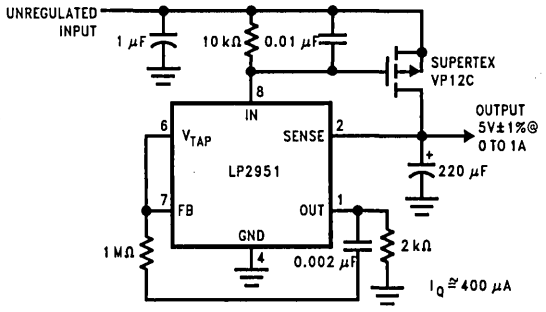
$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

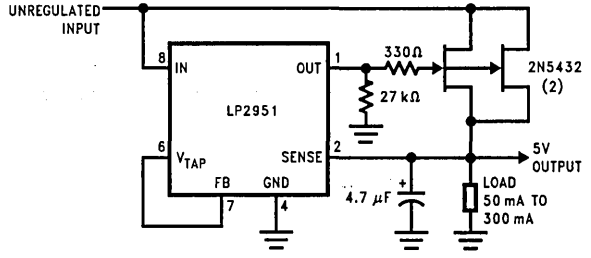
Typical Applications

1A Regulator with 1.2V Dropout



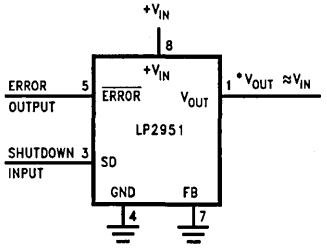
TL/H/8546-22

300 mA Regulator with 0.75V Dropout



TL/H/8546-21

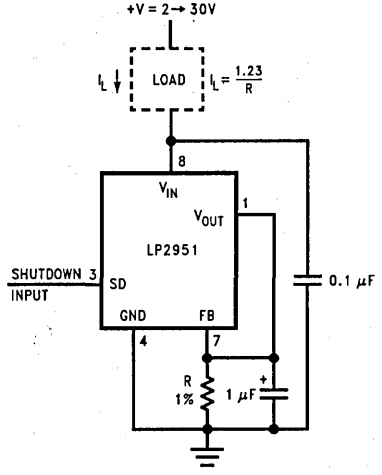
Wide Input Voltage Range Current Limiter



TL/H/8546-9

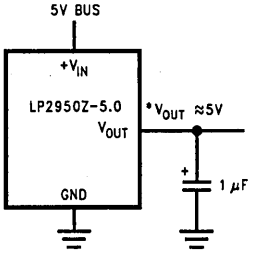
*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Low Drift Current Source



TL/H/8546-8

5 Volt Current Limiter

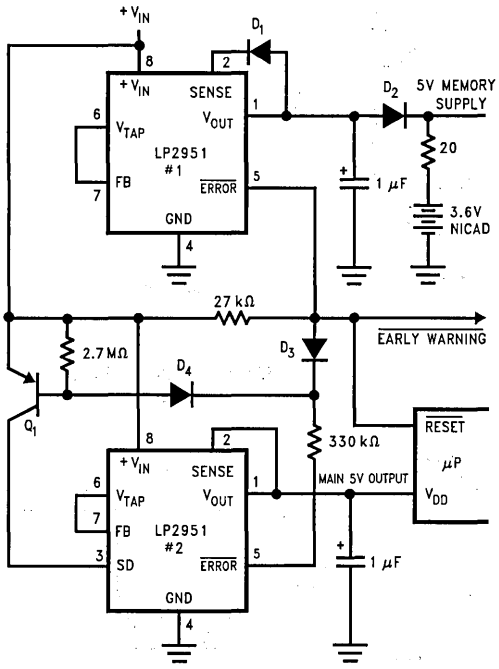


TL/H/8546-10

*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Typical Applications (Continued)

Regulator with Early Warning and Auxiliary Output

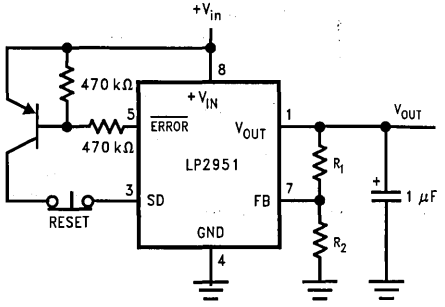


TL/H/8546-11

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

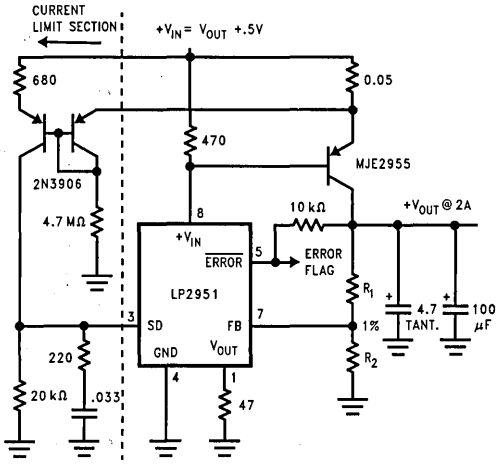
Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Latch Off When Error Flag Occurs



TL/H/8546-12

2 Ampere Low Dropout Regulator



$$V_{out} = 1.23V\left(1 + \frac{R_1}{R_2}\right)$$

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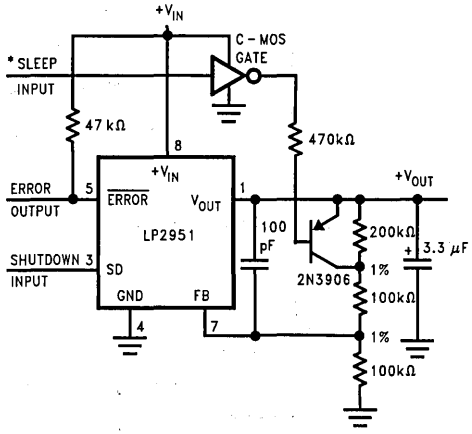
For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 2 to $+V_{out}$ Buss.

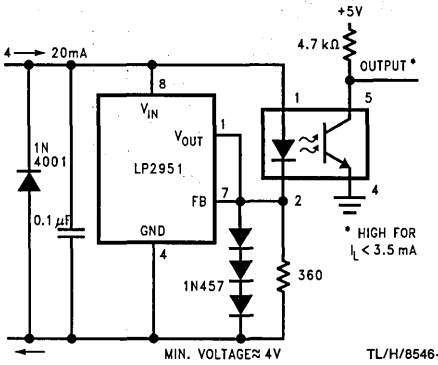
5V Regulator with 2.5V Sleep Function



*High input lowers V_{out} to 2.5V

TL/H/8546-14

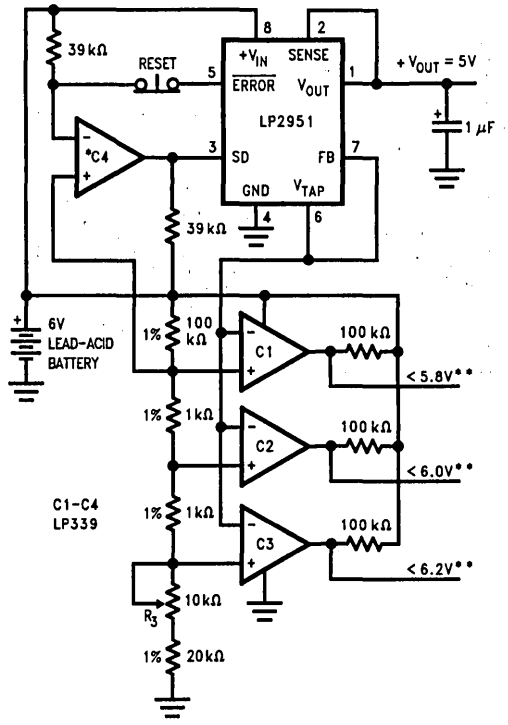
Open Circuit Detector for 4 → 20 mA Current Loop



TL/H/8546-15

Typical Applications (Continued)

Regulator with State-of-Charge Indicator



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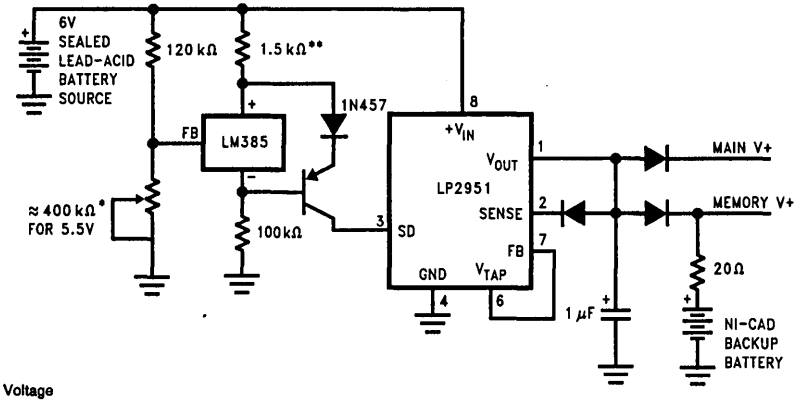
*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

Low Battery Disconnect

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 μA.



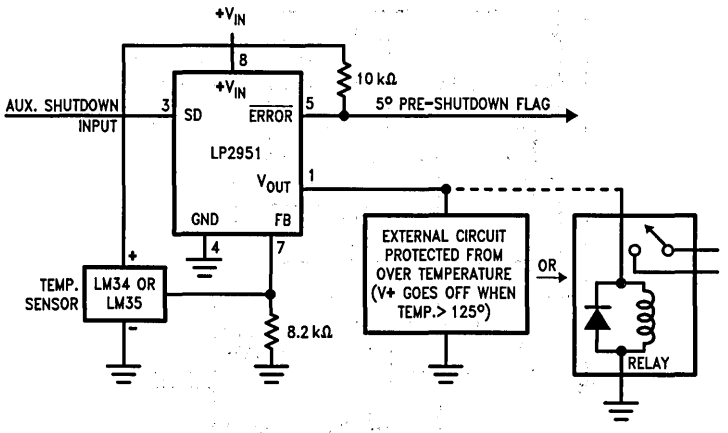
TL/H/8546–17

*Sets disconnect Voltage

**Sets disconnect Hysteresis

Typical Applications (Continued)

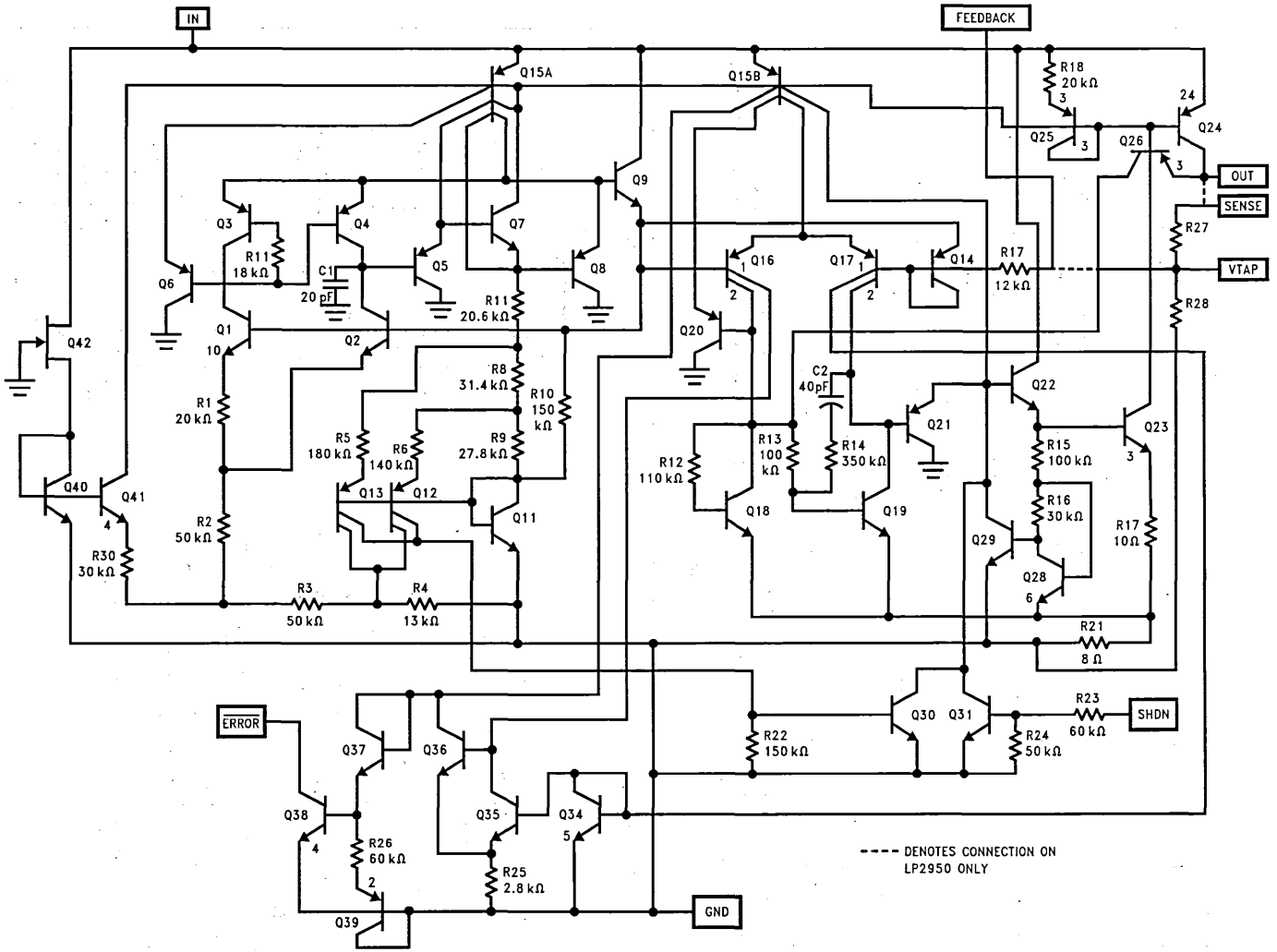
System Overtemperature Protection Circuit



TL/H/8546–18

LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Schematic Diagram



TL/H/8546–23

National Semiconductor

LP2956/LP2956A
Dual Micropower Low-Dropout Voltage Regulators

General Description

The LP2956 is a micropower voltage regulator with very low quiescent current (170 μA typical at light loads) and very low dropout voltage (typically 60 mV at 1 mA load current and 470 mV at 250 mA load current on the main output).

The LP2956 retains all the desirable characteristics of the LP2951, but offers increased output current (main output), an auxiliary LDO adjustable regulated output (75 mA), and additional features.

The auxiliary output is always on (regardless of main output status), so it can be used to power memory circuits.

Quiescent current increases only slightly at dropout, which prolongs battery life.

The error flag goes low if the main output voltage drops out of regulation.

An open-collector auxiliary comparator is included, whose inverting input is tied to the 1.23V reference.

Reverse battery protection is provided.

The parts are available in plastic DIP and surface mount packages.

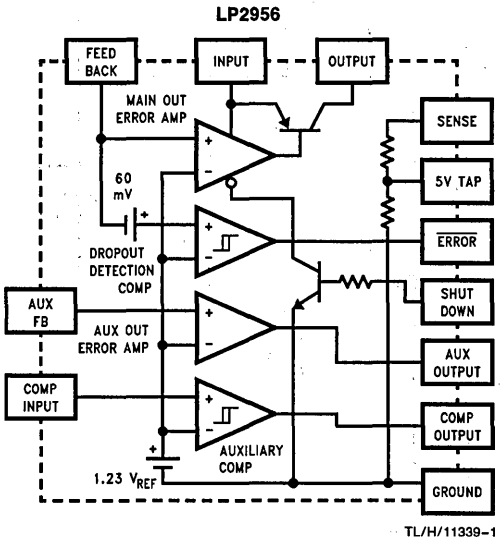
Features

- Output voltage adjusts from 1.23V to 29V
- Guaranteed 250 mA current (main output)
- Auxiliary LDO (75 mA) adjustable output
- Auxiliary comparator with open-collector output
- Shutdown pin for main output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse battery protection

Applications

- High-efficiency linear regulator
- Low dropout battery-powered regulator
- μP system regulator with switchable high-current V_{CC}

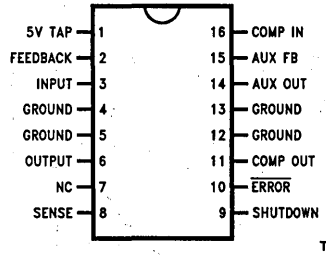
Block Diagram



TL/H/11339–1

Connection Diagrams

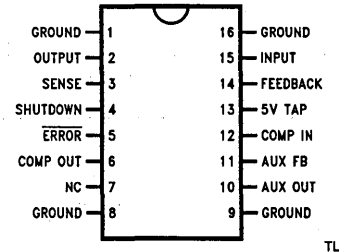
16-Pin DIP



TL/H/11339–2

Order Number LP2956IN or LP2956AIN
See NS Package Number N16A

16-Pin Surface Mount



TL/H/11339–3

Order Number LP2956IM or LP2956AIM
See NS Package Number M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage	−20V to +30V
Feedback Input Voltage (Note 3)	−0.3V to +5V
Aux. Feedback Input Voltage (Note 3)	−0.3V to +5V
Shutdown Input Voltage (Note 3)	−0.3V to +30V
Comparator Input Voltage (Notes 3, 4)	−0.3V to +30V
Comparator Output Voltage (Notes 3, 4)	−0.3V to +30V
ESD Rating (Note 16)	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback pin is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary regulator output has a 100 μA load.

Symbol	Parameter	Conditions	Typical	LP2956AI		LP2956I		Units
				Min	Max	Min	Max	
MAIN OUTPUT								
V_O	Output Voltage		5.0	4.975 **4.940**	5.025 **5.060**	4.950 **4.900**	5.050 **5.100**	V
		1 mA ≤ I_L ≤ 250 mA	5.0	**4.930**	**5.070**	**4.880**	**5.120**	
$\frac{\Delta V_O}{\Delta T}$	Temperature Coefficient	(Note 5)	**20**		**100**		**150**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Line Regulation	V_{IN} = 6V to 30V	0.03		0.1 **0.2**		0.2 **0.4**	%
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 1 mA to 250 mA I_L = 0.1 mA to 1 mA (Note 6)	0.04		0.16 **0.20**		0.20 **0.30**	%
$V_{IN}-V_O$	Dropout Voltage (Note 7)	I_L = 1 mA	60		100 **150**		100 **150**	mV
		I_L = 50 mA	240		300 **420**		300 **420**	
		I_L = 100 mA	310		400 **520**		400 **520**	
		I_L = 250 mA	470		600 **800**		600 **800**	
I_{LIMIT}	Current Limit	R_L = 1Ω	380		500 **530**		500 **530**	mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 8)	0.05		0.2		0.2	%/W
e_n	Output Noise Voltage (10 Hz to 100 KHz) I_L = 100 mA	C_L = 2.2 μF	400					μV RMS
		C_L = 33 μF	260					
		C_L = 33 μF (Note 9)	80					

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Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback pin is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary regulator output has a 100 μA load. (Continued)

Symbol	Parameter	Conditions	Typical	LP2956AI		LP2956I		Units
				Min	Max	Min	Max	
MAIN OUTPUT (Continued)								
V_{FB}	Feedback Pin Voltage		1.23	1.215	1.245	1.205	1.255	V
I_{FB}	Feedback Pin Bias Current		20		40 **60**		40 **60**	nA
I_O (OFF)	Output Leakage In Shutdown	$I_{(SD\ IN)} \geq 1$ μA V_{IN} = 30V, V_{OUT} = 0V	3		10 **20**		10 **20**	μA
AUXILIARY OUTPUT								
V_{FB}	Feedback Pin Voltage		1.23	1.22 **1.21**	1.25 **1.26**	1.21 **1.20**	1.26 **1.27**	V
$\frac{\Delta V_{FB}}{\Delta T}$	Feedback Voltage Temperature Coefficient		**20**					ppm/°C
I_{FB}	Feedback Pin Bias Current		10		20 **30**		20 **30**	nA
$\frac{\Delta V_O}{V_O}$	Line Regulation	6V ≤ V_{IN} ≤ 30V	0.07		0.3 **0.5**		0.4 **0.6**	%
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 0.1 mA to 1 mA I_L = 1 mA to 75 mA (Note 10)	0.1		0.3 **0.6**		0.4 **1.0**	%
$V_{IN}-V_O$	Dropout Voltage	I_L = 1 mA	100		200 **300**		200 **300**	mV
		I_L = 50 mA	400		600 **700**		600 **700**	mV
		I_L = 75 mA	500		700 **850**		700 **850**	mV
e_n	Output Noise (10 Hz–100 KHz) I_L = 10 mA	C_L = 10 μF	300					μV RMS
		C_L = 33 μF (Note 9)	100					
I_{LIM}	Current Limit	V_{OUT} = 0V (Note 13)	80		200 **250**		200 **250**	mA
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 8)	0.2		0.5		0.5	%/W
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V	0.01		1 **2**		1 **2**	μA
V_{OL}	Output "LOW" Voltage	V_{IN} = 4V I_O (COMP) = 400 μA	150		250 **400**		250 **400**	mV
V_{THR} (max)	Upper Threshold Voltage	(Note 11)	−240	−320 **−380**	−150 **−100**	−320 **−380**	−150 **−100**	mV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback pin is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary regulator output has a 100 μA load. (Continued)

Symbol	Parameter	Conditions	Typical	LP2956AI		LP2956I		Units
				Min	Max	Min	Max	
DROPOUT DETECTION COMPARATOR (Continued)								
V_{THR} (min)	Lower Threshold Voltage	(Note 11)	−350	−450 **−640**	−230 **−160**	−450 **−640**	−230 **−160**	mV
HYST	Hysteresis	(Note 11)	110					mV
SHUTDOWN INPUT								
I_{IN}	Input Current to Disable Output	(Note 12)	0.03		**0.5**		**0.5**	μA
V_{IH}	Shutdown Input High Threshold	$I_{(SD\ IN)} \geq 1$ μA		900 **1200**		900 **1200**		mV
V_{IL}	Shutdown Input Low Threshold	$V_O \geq 4.5V$			400 **200**		400 **200**	mV
AUXILIARY COMPARATOR								
V_T(high)	Upper Trip Point	(Note 14)	1.236	1.20 **1.19**	1.28 **1.29**	1.20 **1.19**	1.28 **1.29**	V
V_T(low)	Lower Trip Point	(Note 14)	1.230	1.19 **1.18**	1.27 **1.28**	1.19 **1.18**	1.27 **1.28**	V
HYST	Hysteresis		6					mV
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V V_{IN} (COMP) = 1.3V	0.01		1 **2**		1 **2**	μA
V_{OL}	Output "LOW" Voltage	V_{IN} (COMP) = 1.1V I_O(COMP) = 400 μA	150		250 **400**		250 **400**	mV
I_B	Input Bias Current	$0 \leq V_{IN}$ (COMP) $\leq 5V$	10	−30 **−50**	30 **50**	−30 **−50**	30 **50**	nA
GROUND PIN CURRENT								
I_{GND}	Ground Pin Current (Note 15)	I_L (Main Out) = 1 mA I_L (Aux. Out) = 0.1 mA	170		250 **280**		250 **280**	μA
		I_L (Main Out) = 50 mA I_L (Aux. Out) = 1 mA	1.1		2 **2.5**		2 **2.5**	mA
		I_L (Main Out) = 100 mA I_L (Aux. Out) = 1 mA	3		6 **8**		6 **8**	
		I_L (Main Out) = 250 mA I_L (Aux. Out) = 1 mA	16		28 **33**		28 **33**	
		I_L (Main Out) = 1 mA I_L (Aux. Out) = 50 mA	3		6 **8**		6 **8**	
		I_L (Main Out) = 1 mA I_L (Aux. Out) = 75 mA	6		8 **10**		8 **10**	

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback pin is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary regulator output has a 100 μA load. (Continued)

Symbol	Parameter	Conditions	Typical	LP2956AI		LP2956I		Units
				Min	Max	Min	Max	
GROUND PIN CURRENT (Continued)								
I_{GND}	Ground Pin Current at Dropout (Note 15)	V_{IN} = 4.5V I_L (Main Out) = 0.1 mA I_L (Aux. Out) = 0.1 mA	270		325 **350**		325 **350**	μA
I_{GND}	Ground Pin Current at Shutdown (Note 15)	No Load on Either Output $I_{(SD\ IN)} \geq 1$ μA	120		180 **200**		180 **200**	

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(max), the junction-to-ambient thermal resistance, $\theta_{J\text{-}A}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(max) = \frac{T_J(max) - T_A}{\theta_{J\text{-}A}}$.

Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See Application Hints for additional information on heat sinking and thermal resistance.

Note 3: When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.

Note 4: May exceed the input supply voltage.

Note 5: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 6: Load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the range of 100 μA to 1 mA and one for the 1 mA to 250 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V **(2.3V over temperature)** must be observed.

Note 8: Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at V_{IN} = 20V (3W pulse) for T = 10 ms on the Main regulator output. For the Auxiliary regulator output, specifications are for a 66 mA load pulse at V_{IN} = 20V (1W pulse) for T = 10 ms.

Note 9: Connect a 0.1 μF capacitor from the output to the feedback pin.

Note 10: Load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the range of 100 μA to 1 mA and one for the 1 mA to 75 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 11: Dropout dectection comparator thresholds are expressed as changes in a 5V output. To express the threshold voltages in terms of a differential at the Feedback terminal, divide by the error amplifier gain = V_{OUT}/V_{REF}.

Note 12: The shutdown input equivalent circuit is the base of a grounded-emitter NPN transistor in series with a current-limiting resistor. Pulling the shutdown input high turns off the main regulator. For more details, see Application Hints.

Note 13: The auxiliary regulator output has foldback limiting, which means the output current reduces with output voltage. The tested limit is for V_{OUT} = 0V, so the output current will be higher at higher output voltages.

Note 14: This test is performed with the auxiliary comparator output sinking 400 μA of current. At the upper trip point, the comparator output must be ≥2.4V. At the low trip point, the comparator output must be ≤ 0.4V.

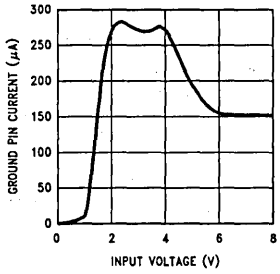
Note 15: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive dividers (if used).

Note 16: All pins are rated for 2 kV, except for the auxiliary feedback pin which is rated for 1.2 kV (human body model, 100 pF discharged through 1.5 kΩ).

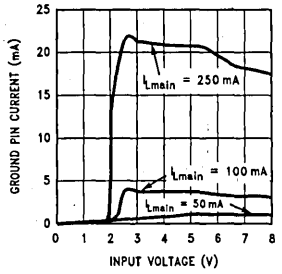
Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary output has a 100 μA load.

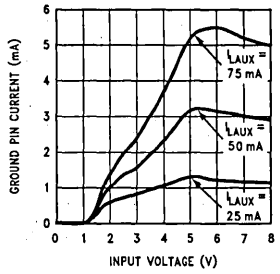
Ground Pin Current



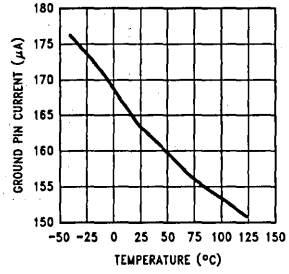
Ground Pin Current



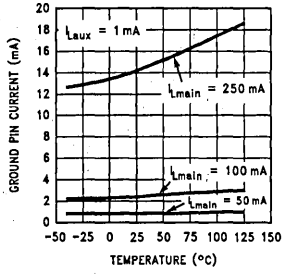
Ground Pin Current



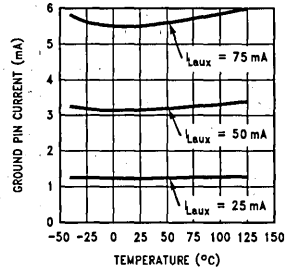
Ground Pin Current



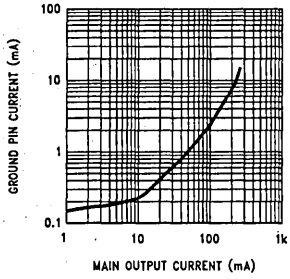
Ground Pin Current



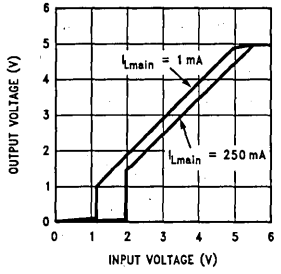
Ground Pin Current



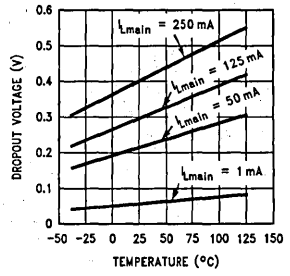
Ground Pin Current vs Main Load



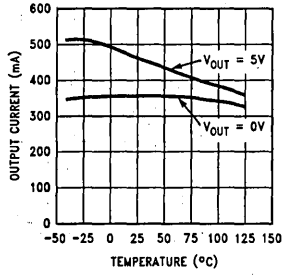
Dropout Characteristics (Main Regulator)



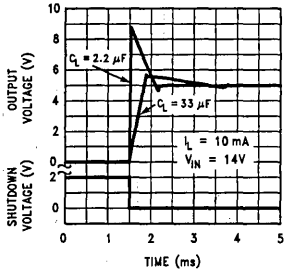
Dropout Voltage vs Temperature (Main Regulator)



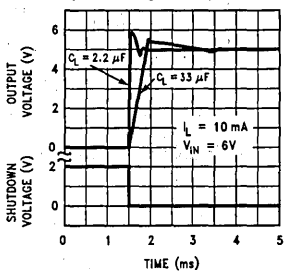
Current Limit vs Regulator (Main Regulator)



Enable Transient (Main Regulator)



Enable Transient (Main Regulator)



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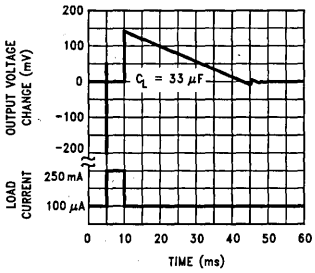
7

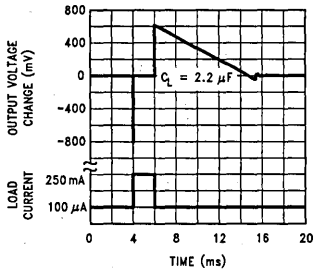
Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 µF (Main Output) and 10 µF (Auxiliary Output), Feedback is tied to 5V Tap pin, C_{IN} = 1 µF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary output has a 100 µA load. (Continued)

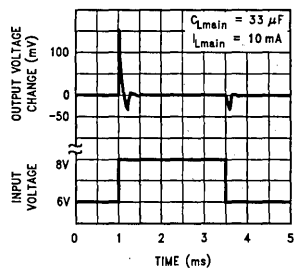
Load Transient Response (Main Regulator)



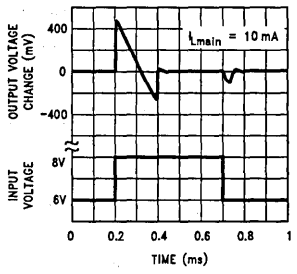
Load Transient Response (Main Regulator)



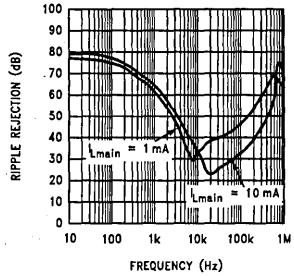
Line Transient Response (Main Regulator)



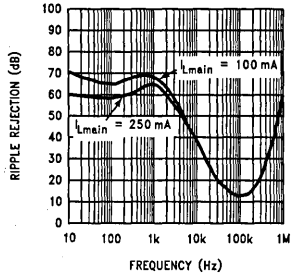
Line Transient Response (Main Regulator)



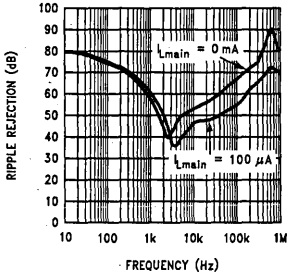
Ripple Rejection (Main Regulator)



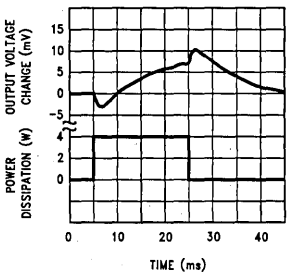
Ripple Rejection (Main Regulator)



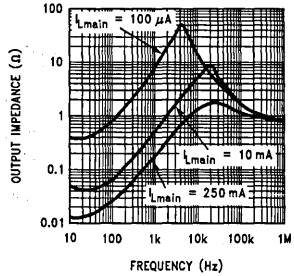
Ripple Rejection (Main Regulator)



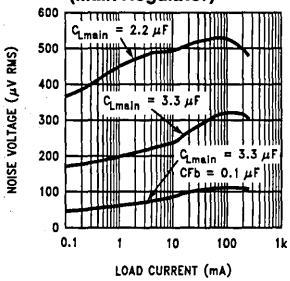
Thermal Regulation (Main Regulator)



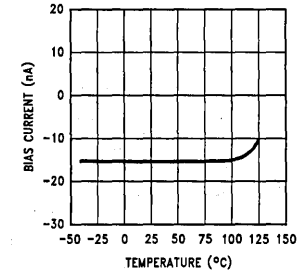
Output Impedance (Main Regulator)



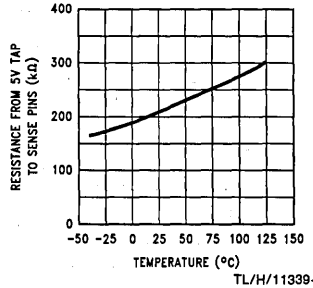
Output Noise Voltage (Main Regulator)



Feedback Bias Current



Divider Resistance



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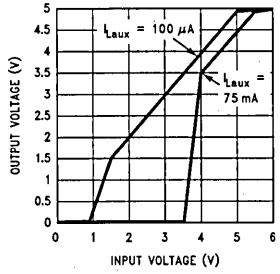
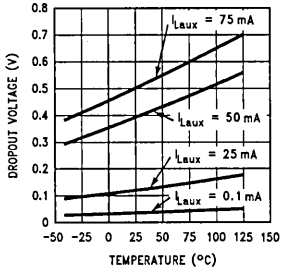
Typical Performance Characteristics Unless otherwise specified: V_{IN} = 6V, C_L = 2.2 μF (Main Output) and 10 μF (Auxiliary Output), Feedback is tied to 5V Tap pin, C_{IN} = 1 μF, V_{SD} = 0V, Main Output pin is tied to Output Sense pin, Auxiliary Output is programmed for 5V. The main regulator output has a 1 mA load, the auxiliary output has a 100 μA load. (Continued)

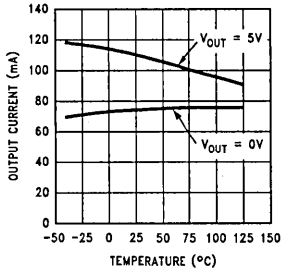
Dropout Characteristics (Auxiliary Regulator)



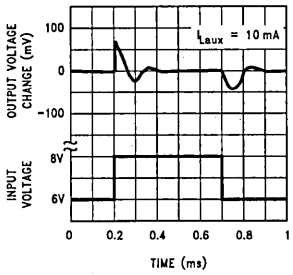
Dropout vs Temperature (Auxiliary Regulator)



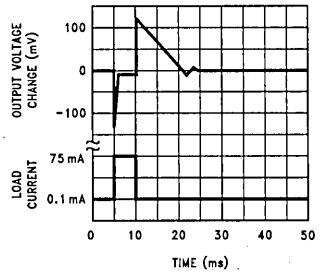
Current Limit vs Temperature (Auxiliary Regulator)



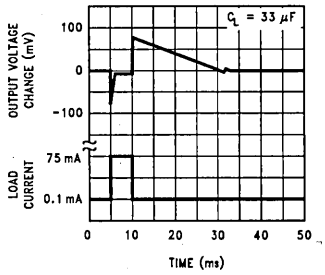
Line Transient Response (Auxiliary Regulator)



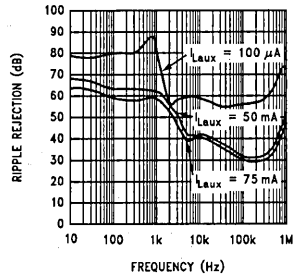
Load Transient Response (Auxiliary Regulator)



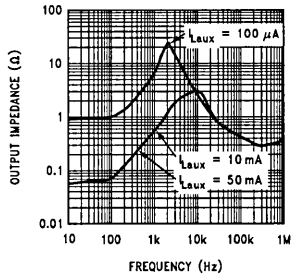
Load Transient Response (Auxiliary Regulator)



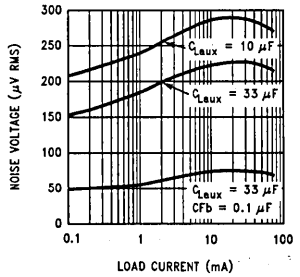
Ripple Rejection (Auxiliary Regulator)



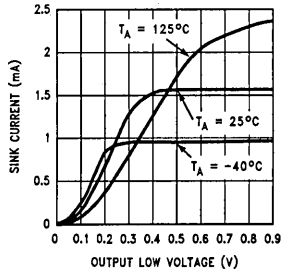
Output Impedance (Auxiliary Regulator)



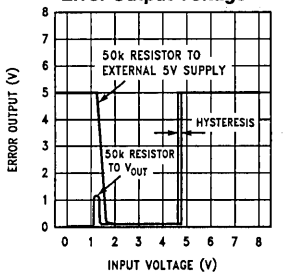
Output Noise Voltage (Auxiliary Regulator)



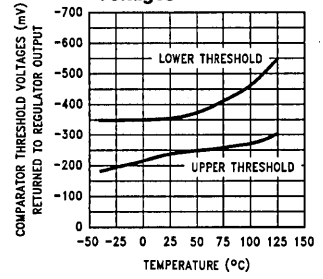
Auxiliary Comparator Sink Current



Error Output Voltage



Dropout Detection Comparator Threshold Voltages



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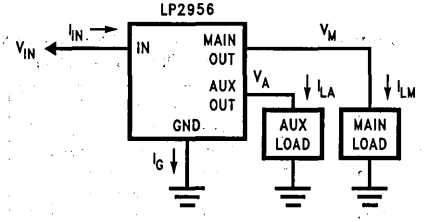
7

Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LP2956 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all expected operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the regulator, P(max), must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the **maximum specified AC input voltage** must be used (since this produces the maximum DC input voltage to the regulator). *Figure 1* shows the voltages and currents which are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in *Figure 1* (the currents and power due to external resistive dividers are not included, and are typically negligible).



$$P_{TOTAL} = (V_{IN} - V_M)\,I_{LM} + (V_{IN} - V_A)\,I_{LA} + (V_{IN})\,I_G$$

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FIGURE 1. Current/Voltage Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$. This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)$$

where: $T_J(max)$ is the maximum allowable junction temperature

$T_A(max)$ is the maximum ambient temperature

Using the calculated values for $T_R(max)$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

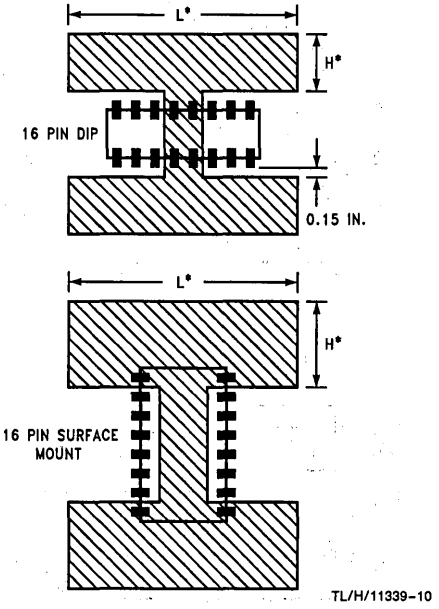
$$\theta_{(J-A)} = T_R(max)/P(max)$$

The heatsink for the LP2956 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are shown in Table I.

TABLE I

Part	Package	Pins
LP2956IN	16-Pin DIP	4, 5, 12, 13
LP2956AIN	16-Pin DIP	4, 5, 12, 13
LP2956IM	16-Pin Surface Mt.	1, 8, 9, 16
LP2956AIM	16-Pin Surface Mt.	1, 8, 9, 16

Figure 2 shows copper patterns which may be used to dissipate heat from the LP2956:



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*For best results, use L = 2H

FIGURE 2. Copper Heatsink Patterns

Table II shows some typical values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W (1 oz. copper).

TABLE II

Package	L (In.)	H (In.)	θ_{J-A} (°C/W)
16-Pin DIP	1	0.5	70
	2	1	60
	3	1.5	58
	4	0.19	66
	6	0.19	66
16-Pin Surface Mount	1	0.5	83
	2	1	70
	3	1.5	67
	6	0.19	69
	4	0.19	71
	2	0.19	73

Application Hints (Continued)

EXTERNAL CAPACITORS

A 2.2 μF (or greater) capacitor is required between the main output pin and ground to assure stability. The auxiliary output requires 10 μF to ground. Without these capacitors, the part may oscillate. Most types of tantalum or aluminum electrolytics will work here. Film types will work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important characteristic of the capacitors is an ESR of 5Ω (or less) on the main regulator output and an ESR of 1Ω (or less) on the auxiliary regulator output (the ESR may increase by a factor of **20** or **30** as the temperature is reduced from +25°C to −30°C). The value of these capacitors may be increased without limit.

The main output requires less capacitance at lighter load currents. This capacitor can be reduced to 0.68 μF for currents below 10 mA or 0.22 μF for currents below 1 mA.

Programming the main output for voltages below 5V requires *more* output capacitance for stability. For the worst-case condition of 1.23V output and 250 mA of load current, a 6.8 μF (or larger) capacitor should be used.

A 1 μF capacitor should be placed from the input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Stray capacitance to the Feedback terminal can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitance to 6.8 μF (or greater) will cure the problem.

MINIMUM LOAD ON MAIN OUTPUT

When setting the main output voltage using an external resistive divider, a minimum current of 10 μA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so the specified value must be used to obtain test limit correlation.

PROGRAMMING THE MAIN OUTPUT VOLTAGE

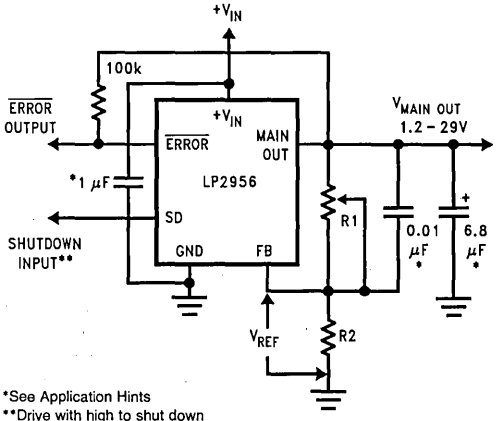
The main output may be pin-strapped for 5V operation using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and 5V Tap pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 29V maximum rating using an external pair of resistors (see *Figure 3*). The complete equation for the output voltage is:

$$V_{MAIN\ OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1)$$

where V_{REF} is the 1.23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 1 μA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see **MINIMUM LOAD**).

If I_{FB} is ignored in the calculation of the output voltage, it will produce a small error in $V_{MAIN\ OUT}$. Choosing R2 = 100 kΩ will reduce this error to 0.16% (typical) while increasing the resistor program current to 12 μA. Since the typical quiescent current is 130 μA, this added current is negligible.



*See Application Hints
**Drive with high to shut down

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FIGURE 3. Adjustable Regulator

DROPOUT VOLTAGE

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

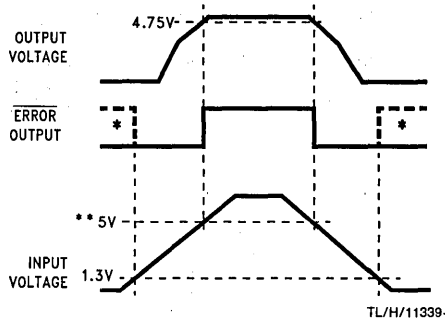
DROPOUT DETECTION COMPARATOR

This comparator produces a logic "LOW" whenever the main output falls out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to block diagram). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 4 gives a timing diagram showing the relationship between the main output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator whose main output is programmed for 5V. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3V input. It goes high at about 5V input, where the main output equals 4.75V. Since the dropout voltage is load dependent, the **input** voltage trip points will vary with load current. The **main output** voltage trip point does not vary.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the regulator main output or some other supply voltage. Using the main output prevents an invalid "HIGH" on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3V. In selecting a value for the pull-up resistor, note that while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. The resistor is not required if the output is unused.

Application Hints (Continued)



*In shutdown mode, ERROR will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.

**Exact value depends on dropout voltage. (See Application Hints)

FIGURE 4. ERROR Output Timing

If a single pull-up resistor is used to the regulator output, the error flag may briefly rise up to about 1.3V as the input voltage ramps up or down through the 0V to 1.3V region.

In some cases, this 1.3V signal may be mis-interpreted as a false high by a μP which is still "alive" with 1.3V applied to it.

To prevent this, the user may elect to use **two** resistors which are equal in value on the error output (one connected to ground and the other connected to the regulator output).

If this two-resistor divider is used, the error output will only be pulled up to about 0.6V (not 1.3V) during power-up or power-down, so it can not be interpreted as a high signal. When the regulator output is at 5V, the error output will be 2.5V, which is still clearly a high signal.

OUTPUT ISOLATION

The regulator outputs can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, as long as the regulator ground pin is connected to ground. If the ground pin is left floating, damage to the regulator can occur if the output is pulled up by an external voltage source.

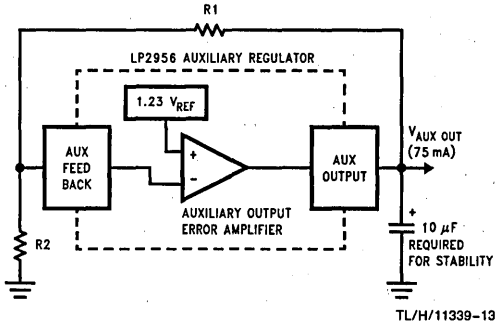
REDUCING MAIN OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present on the main output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to *Figure 3*). The formula for selecting the capacitor to be used is:

$$CB = \frac{1}{2\pi\, R1 \times 20\ Hz}$$

This gives a value of about 0.1μF. When this is used, the output capacitor must be 6.8 μF (or greater) to maintain stability. The 0.1 μF capacitor reduces the high frequency noise gain of the circuit to unity, lowering the output noise from 260 μV to 80 μV using a 10 Hz to 100 kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at higher output voltages.



$$V_{AUX\,OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1)$$

where: V_{REF} = 1.23V and I_{FB} = −10 nA (typical)

FIGURE 5. Auxiliary Adjustable Regulator

AUXILIARY LDO OUTPUT

The LP2956 has an auxiliary LDO regulator output (which can source up to 75 mA) that is adjustable for voltages from 1.23V to 29V.

The output voltage is set by an external resistive divider, as shown in *Figure 5*. The maximum output current is 75 mA, and the output requires 10 μF from the output to ground for stability, regardless of load current.

SHUTDOWN INPUT

The shutdown input equivalent circuit is shown in *Figure 6*. The main regulator output is shut down when the NPN transistor is turned ON.

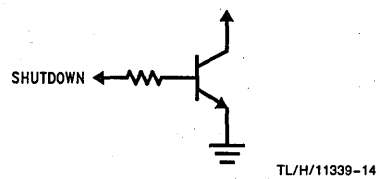


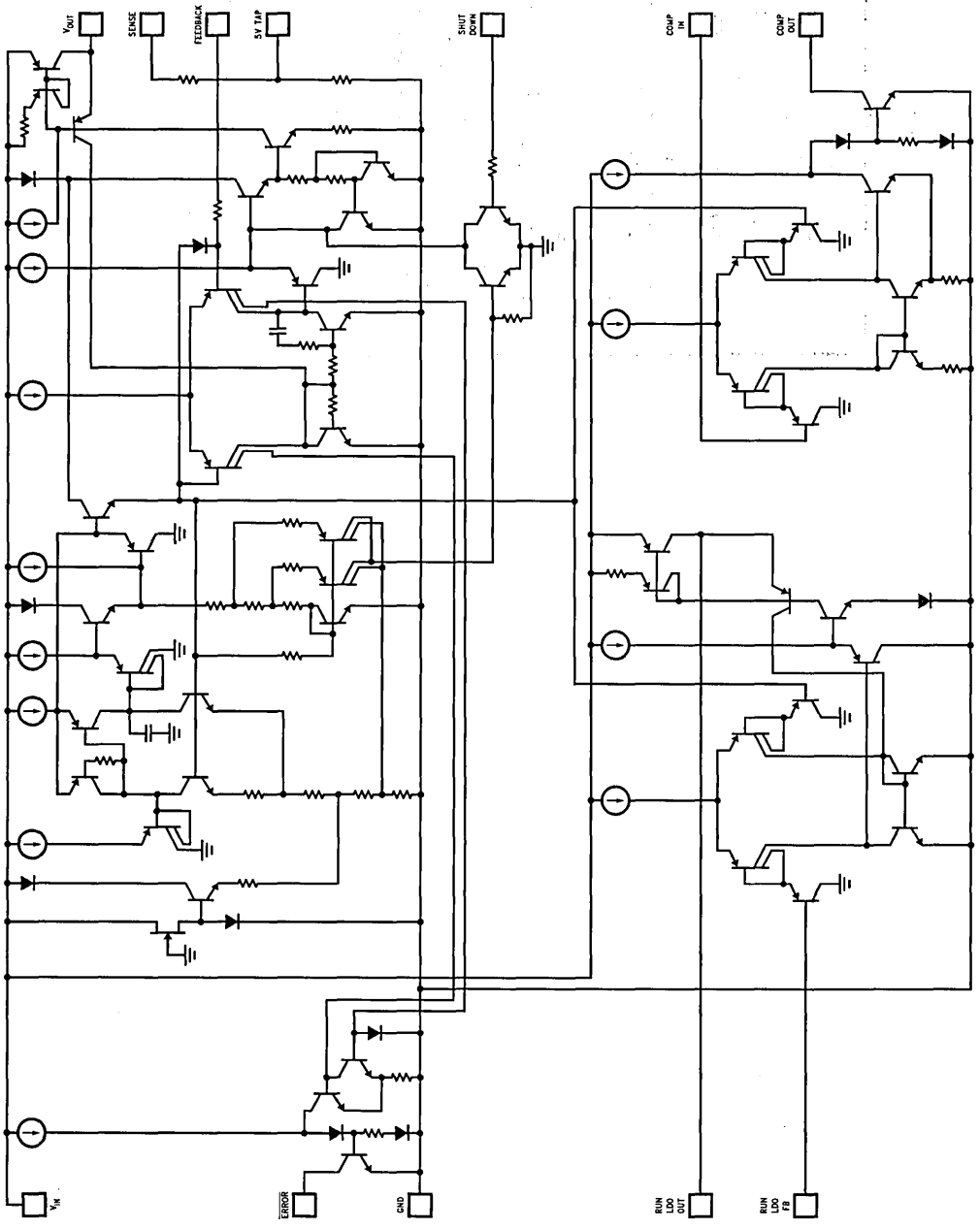
FIGURE 6. Shutdown Circuitry

The current into the input should be at least 0.5 μA to assure the output shutdown function. A resistor may be placed in series with the input to minimize current draw in shutdown mode, provided this minimum input current requirement is met.

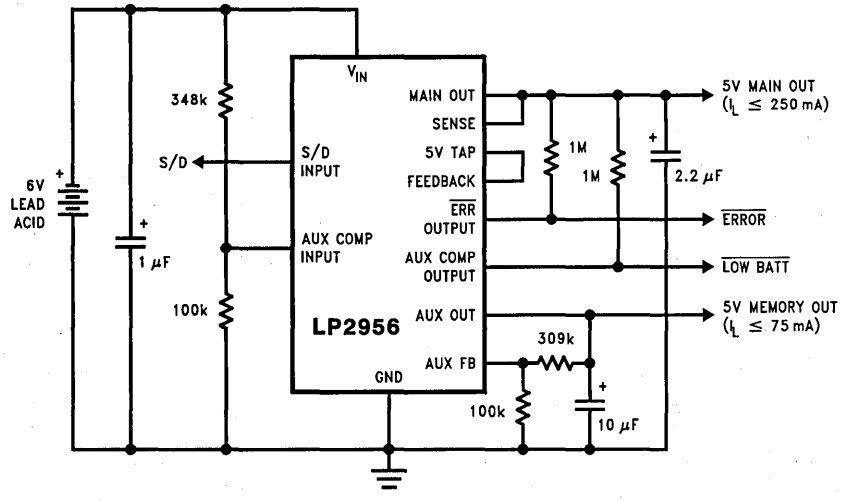
IMPORTANT:

The shutdown input must not be left floating: a pull-down resistor (10 kΩ to 50 kΩ recommended) must be connected between the shutdown input and ground in cases where the input is not actively pulled low.

Schematic Diagram



Typical Applications



TL/H/11339–16

National Semiconductor

LP2960
Adjustable Micropower 0.5A Low-Dropout Regulators

General Description

The LP2960 is a micropower voltage regulator with very low dropout voltage (12 mV typical at 1 mA load and 470 mV typical at 500 mA load) and very low quiescent current (450 μA typical at 1 mA load).

The LP2960 is ideally suited for battery-powered systems: the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2960 retains all the desirable characteristics of the LP2953, and offers increased output current.

The error flag goes low any time the output drops more than 5% out of regulation.

Reverse battery protection is provided.

The LP2960 requires only 10 μF of output capacitance for stability (5V version).

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good regulation characteristics.

The parts are available in 16-pin plastic DIP and 16-pin surface mount packages.

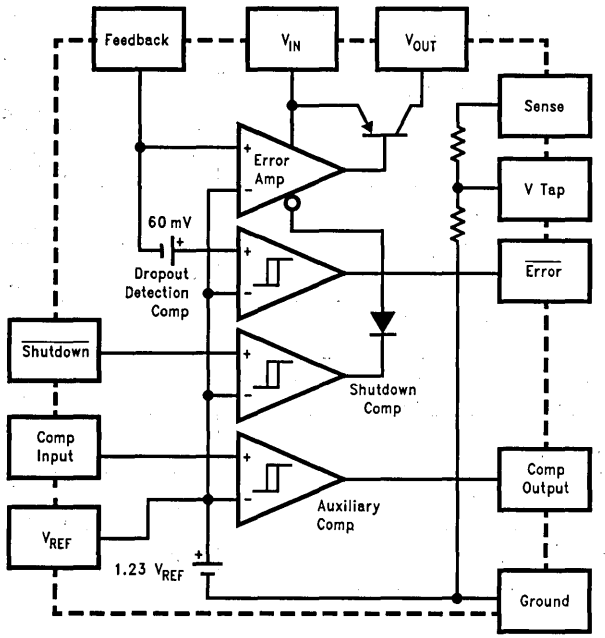
Features

- Output voltage adjusts from 1.23V–29V
- Guaranteed 500 mA output current
- 5V and 3.3V versions available
- 16-pin DIP and 16-pin SO packages
- Low dropout voltage
- Low quiescent current
- Tight line and load regulation
- Low temperature coefficient
- Current limiting and thermal protection
- Logic-level shutdown
- Can be wired for snap-ON and snap-OFF
- Reverse battery protection

Applications

- High-efficiency linear regulator
- Regulator with under-voltage shutdown
- Low dropout battery-powered regulator
- Cellular telephones

Block Diagram



TL/H/11962–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
LP2960AI/LP2960I	−40°C to +125°C
Lead Temperature (Soldering, 5 sec.)	260°C
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage	−20V to +30V
Feedback Input Voltage (Note 3)	−0.3V to +5V
Comparator Input Voltage (Note 4)	−0.3V to +30V
Comparator Output Voltage (Note 4)	−0.3V to +30V
ESD Rating (Note 15)	1.5 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 10 µF for 5V parts or C_{OUT} = 22 µF for 3.3V parts, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2960AI (Note 14)		LP2960I (Note 14)		Units
				Min	Max	Min	Max	
V_O	Output Voltage (5V Versions)	1 mA ≤ I_L ≤ 500 mA	5.0	4.962 **4.930**	5.038 **5.070**	4.925 **4.880**	5.075 **5.120**	V
	Output Voltage (3.3V Versions)	1 mA ≤ I_L ≤ 500 mA	3.3	3.275 **3.254**	3.325 **3.346**	3.250 **3.221**	3.350 **3.379**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coefficient	(Note 5)	**20**		**130**		**160**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Output Voltage Line Regulation	V_{IN} = [V_O(NOM) + 1V] to 30V	0.06		0.2 **0.5**		0.4 **0.8**	%
$\frac{\Delta V_O}{V_O}$	Output Voltage Load Regulation	(Note 6)	0.08		0.16 **0.30**		0.20 **0.40**	%
V_{IN}−V_O	Dropout Voltage (Note 7)	I_L = 1 mA	12		30 **50**		30 **50**	mV
		I_L = 100 mA	180		250 **350**		250 **350**	
		I_L = 200 mA	260		350 **450**		350 **450**	
		I_L = 500 mA	470		600 **800**		600 **800**	
I_{GND}	Ground Pin Current (Note 8)	I_L = 1 mA	450		600 **750**		600 **750**	µA
		I_L = 100 mA	2.6		4.0 **5.0**		4.0 **5.0**	mA
		I_L = 200 mA	5.5		8 **10**		8 **10**	
		I_L = 500 mA	21		35 **40**		35 **40**	
I_{GND}	Ground Pin Current at Dropout (Note 8)	V_{IN} = V_O(NOM) − 0.5V I_L = 100 µA	1.8		3 **5**		3 **5**	mA
	Ground Pin Current at Shutdown (Note 8)	V_{SD} ≤ 1.1V	300		400		400	µA
I_{LIMIT}	Current Limit	R_L = 0.5Ω	1000		1500 **1600**		1500 **1600**	mA
$\frac{\Delta V_O}{P_D}$	Thermal Regulation	(Note 10)	0.05		0.2		0.2	%/W

Electrical Characteristics Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 10 µF for 5V parts or C_{OUT} = 22 µF for 3.3V parts, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V. (Continued)

Symbol	Parameter	Conditions	Typ	LP2960AI (Note 14)		LP2960I (Note 14)		Units
				Min	Max	Min	Max	
e_n	Output Noise Voltage @ I_L = 100 mA (10 Hz–100 kHz)	C_{OUT} = 10 µF	300					µV RMS
		C_{OUT} = 47 µF	210					
		C_{OUT} = 47 µF (Note 11)	130					
V_{REF}	Reference Voltage		1.235	1.220 **1.210**	1.250 **1.265**	1.210 **1.195**	1.260 **1.275**	V
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Line Regulation	(Note 13)	0.05		0.1 **0.30**		0.2 **0.4**	%
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Load Regulation	I_{REF} = 0–200 µA	0.45		0.6 **0.9**		1.2 **1.5**	%
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temperature Coefficient	(Note 5)	**20**					ppm/°C
I_B(FB)	Feedback Pin Bias Current		−20		−50 **−70**		−50 **−70**	nA
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output HIGH Leakage	V_{OH} = 30V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output LOW Voltage	V_{IN} = V_O(NOM) − 1V I_O(COMP) = 400 µA	125		250 **400**		250 **400**	mV
V_{THR}(max)	Upper Threshold Voltage	(Note 9)	−60	−80 **−100**	−35 **−25**	−80 **−100**	−35 **−25**	mV
V_{THR}(min)	Lower Threshold Voltage	(Note 9)	−85	−130 **−200**	−70 **−35**	−130 **−200**	−70 **−35**	mV
HYST	Hysteresis	(Note 9)	25					mV
SHUTDOWN INPUT								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±5	−18 **−24**	18 **24**	−18 **−24**	18 **24**	mV
HYST	Hysteresis	(Referred to V_{REF})	10					mV
I_B	Input Bias Current	$V_{S/D}$ = 0–5V	−20	−60 **−100**	60 **100**	−60 **−100**	60 **100**	nA
I_{OUT}(S/D)	Regulator Output Current in Shutdown	(Note 12)	3		12 **20**		12 **20**	µA
AUXILIARY COMPARATOR								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±5	−15 **−20**	15 **20**	−15 **−20**	15 **20**	mV
HYST	Hysteresis	(Referred to V_{REF})	10					mV
I_B	Input Bias Current	V_{COMP} = 0–5V	−20	−60 **−100**	60 **100**	−60 **−100**	60 **100**	nA
I_{OH}	Output HIGH Leakage	V_{OH} = 30V V_{COMP} = 1.3V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output LOW Voltage	V_{COMP} = 1.1V I_O = 400 µA	125		250 **400**		250 **400**	mV

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (max), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P\,(max) = \frac{T_J\,(max) - T_A}{\theta_{J-A}}$$

Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See APPLICATION HINTS for additional information on heatsinking and thermal resistance.

Note 3: When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.

Note 4: May exceed the input supply voltage.

Note 5: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 6: Output voltage load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the load current range of 100 μA to 1 mA and one for the 1 mA to 500 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V **(2.3V over temperature)** must be observed.

Note 8: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).

Note 9: Dropout detection comparator threshold voltages are expressed in terms of a voltage differential measured at the Feedback terminal below the *nominal* reference voltage, which is the reference voltage measured with $V_{IN} = V_O(NOM) + 1V$. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain which is $V_O/V_{REF} = (R1 + R2)/R2$ (see *Basic Application Circuit*).

Note 10: Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 400 mA load pulse at $V_{IN} = V_O(NOM) + 15V$ (6W pulse) for T = 10 ms.

Note 11: Connect a 0.1 μF capacitor from the output to the feedback pin.

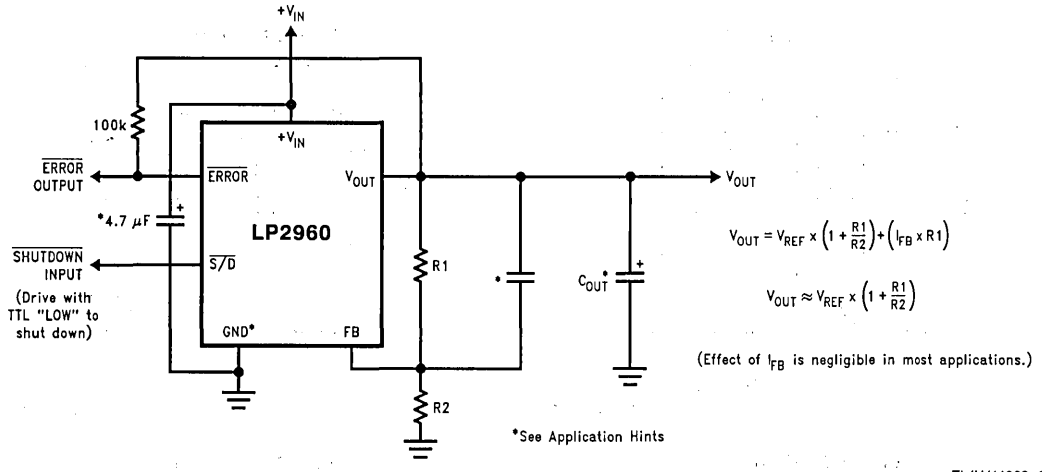
Note 12: Vshutdown $\leq$ 1.1V, $V_{IN} < 30V$, $V_{OUT} = 0V$.

Note 13: Two separate tests are performed for reference voltage line regulation, one covering $2.5V \leq V_{IN} \leq V_O(NOM) + 1V$ and the other test for $V_O(NOM) + 1V \leq V_{IN} \leq 30V$.

Note 14: All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level.

Note 15. Human Body Model, 200 pF discharged through 1.5 kΩ.

Basic Application Circuit



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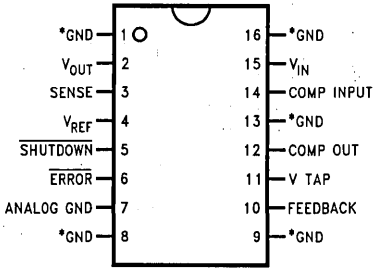
Connection Diagrams and Ordering Information

16-Pin Surface Mount Package



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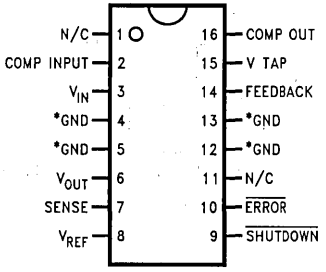
*Internally Connected to Power Ground

Top View

Order Number LP2960IM-5.0, LP2960AIM-5.0, LP2960IM-3.3 or LP2960AIM-3.3
See NS Package Number M16A

16-Pin DIP Package



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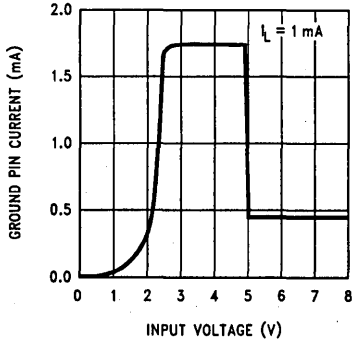
Top View

Order Number LP2960IN-5.0, LP2960AIN-5.0, LP2960IN-3.3 or LP2960AIN-3.3
See NS Package Number N16G

Typical Performance Characteristics

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V.

Ground Pin Current



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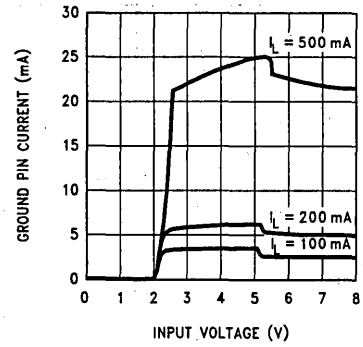
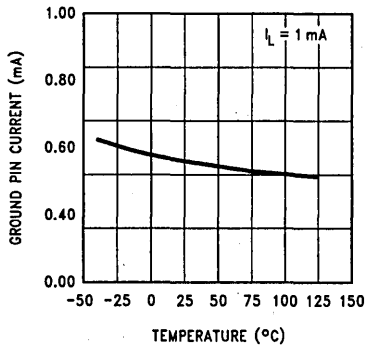
Ground Pin Current



TL/H/11962-6

Ground Pin Current



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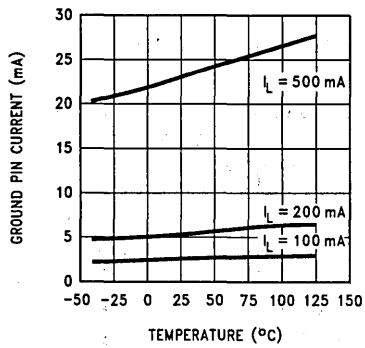
Ground Pin Current



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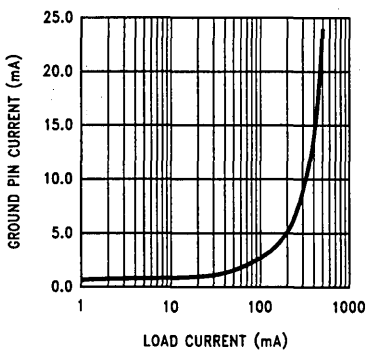
Ground Pin Current



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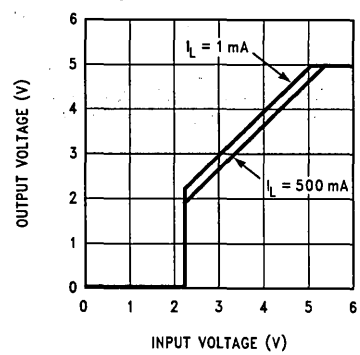
Dropout Characteristics



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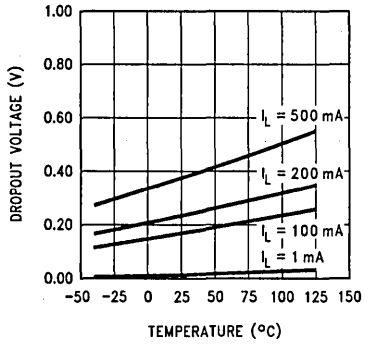
Typical Performance Characteristics

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V. (Continued)

Dropout Voltage vs Temperature



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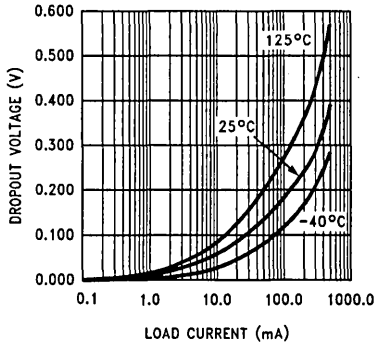
Dropout Voltage vs Load Current



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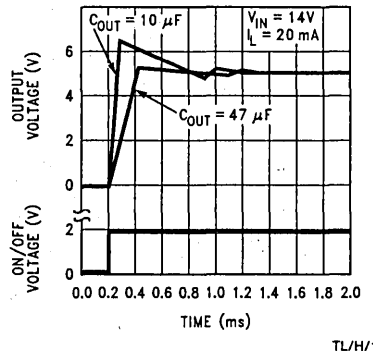
Enable Transient



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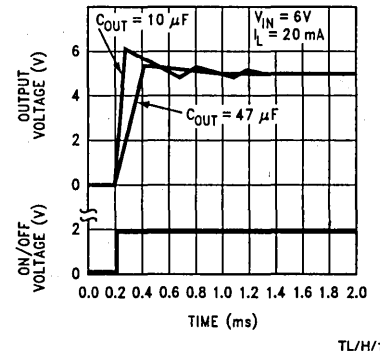
Enable Transient



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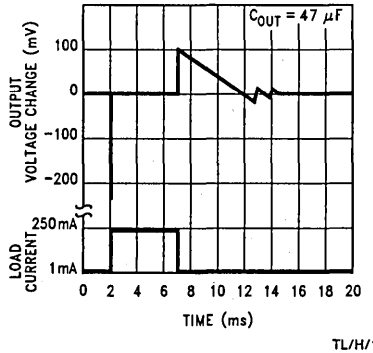
Load Transient



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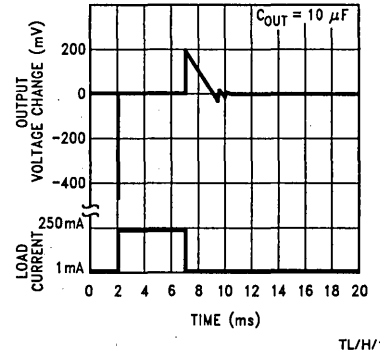
Load Transient

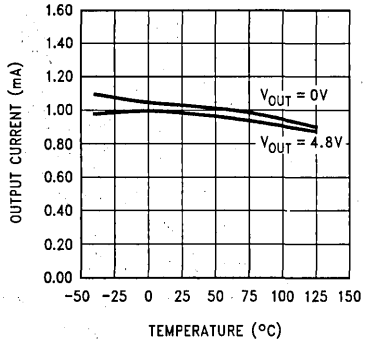


TL/H/11962-16

Typical Performance Characteristics

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V. (Continued)

Current Limit vs Temperature



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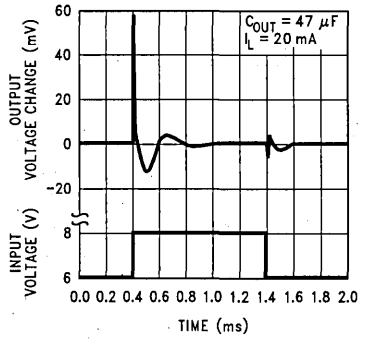
Line Transient Response



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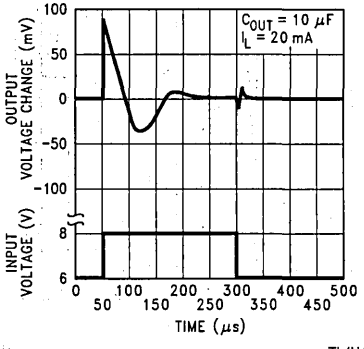
Line Transient Response



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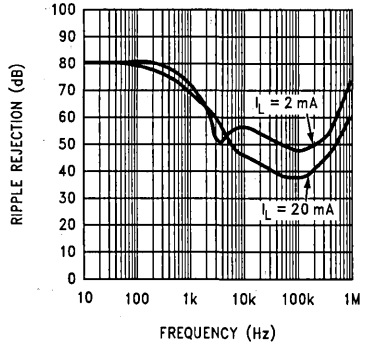
Ripple Rejection



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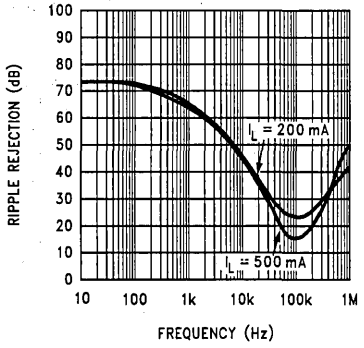
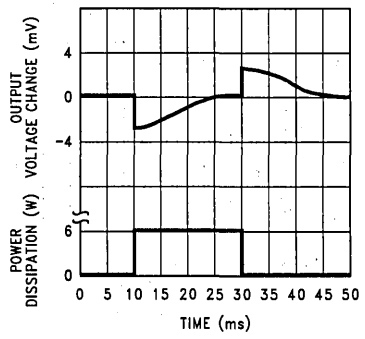
Ripple Rejection



TL/H/11962-21

Thermal Regulation

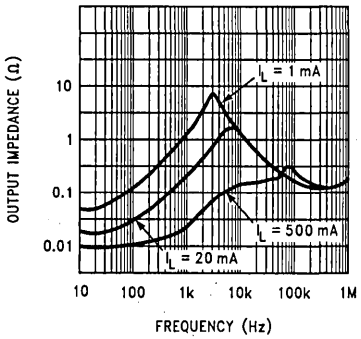


TL/H/11962-22

Typical Performance Characteristics

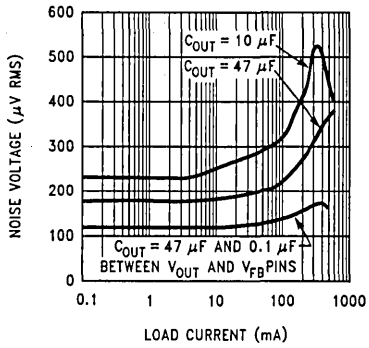
Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V. (Continued)

Output Impedance



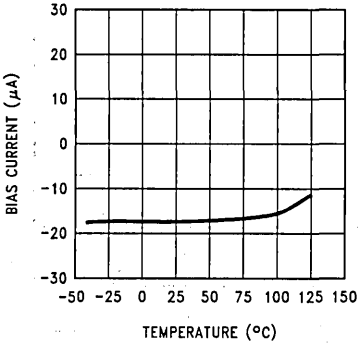
TL/H/11962-23

Output Noise Voltage



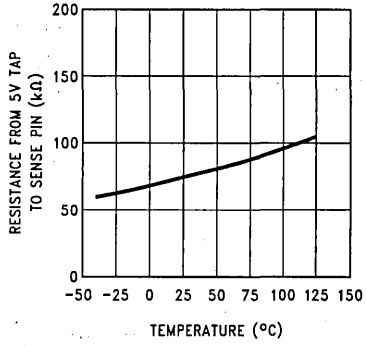
TL/H/11962-24

Feedback Bias Current



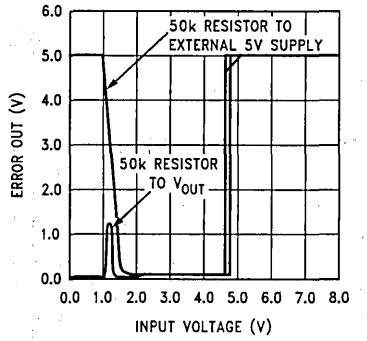
TL/H/11962-25

Divider Resistance



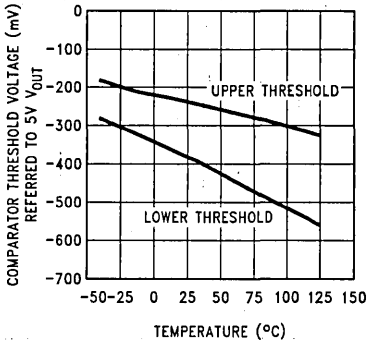
TL/H/11962-26

Error Output Voltage vs Input Voltage



TL/H/11962-27

Dropout Detection Comparator Threshold Voltage



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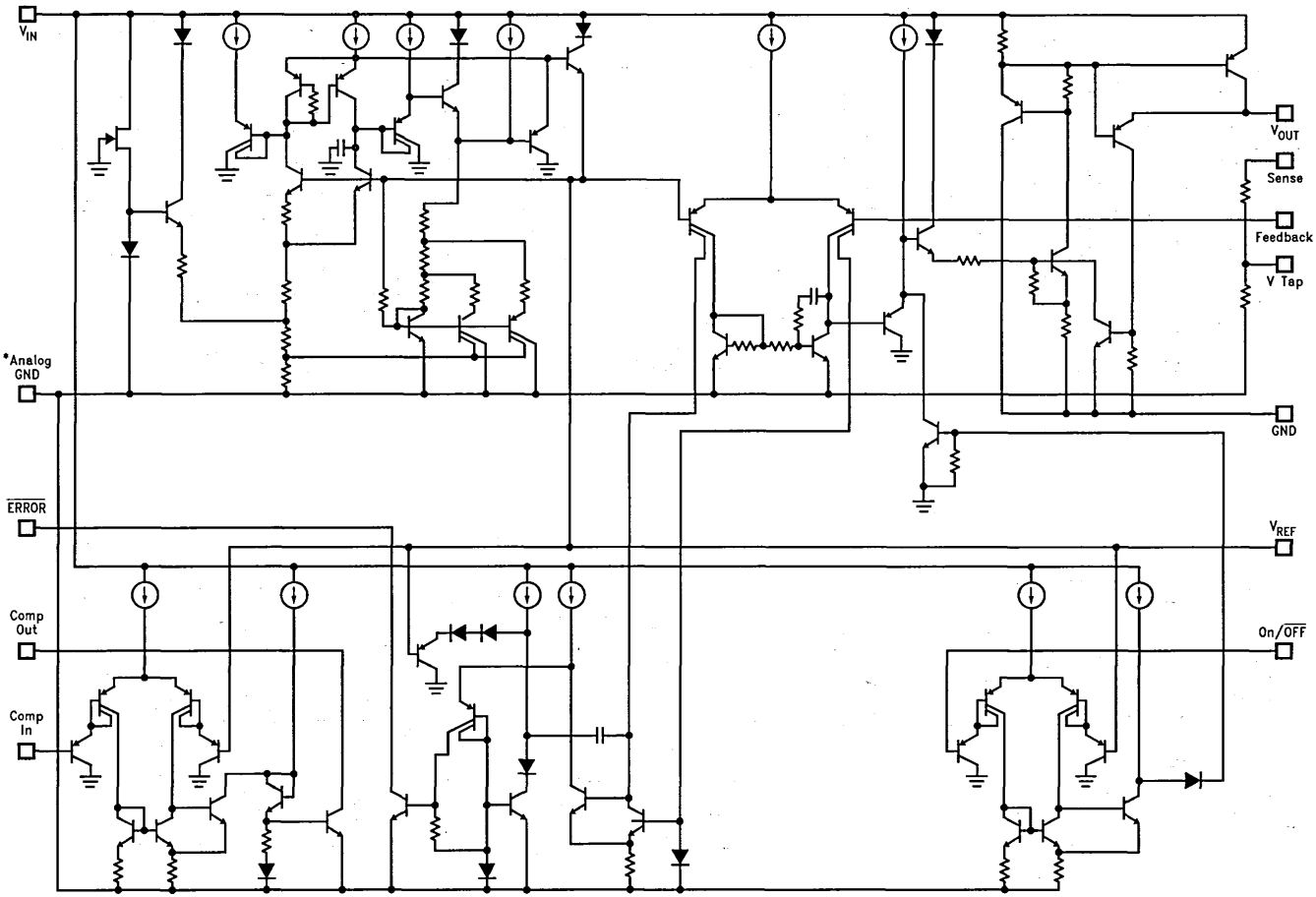
Schematic Diagram



*In the 16-pin DIP devices, the "Analog GND" point is internally connected to the "GND" point.
In the 16-pin surface-mount devices, "Analog GND" is brought out on a separate pin.

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Application Hints

EXTERNAL CAPACITORS

Bypass capacitors on the input and output of the LP2960 are required: without these capacitors, *the part will oscillate.*

A capacitor (whose value is *at least* 4.7μF) must be connected from the V_{IN} pin to ground. If the input capacitor is located more than one inch away from the LP2960, the capacitor may have to be increased to 22 μF to assure stability. A capacitor is also required between V_{OUT} and Ground, and the minimum amount of capacitance required here depends on output voltage.

If the output voltage of the LP2960 is set to 5V, a minimum of 10 μF is needed in output capacitance. At 3.3V output, at least 22 μF is required to assure stability.

ESR LIMIT: The ESR of the capacitor used on the LP2960 must be less than 0.7Ω *throughout the entire operating temperature range* to assure stability.

The ESR of an aluminum electrolytic capacitor is typically only specified at 25°C, and does not reflect the maximum ESR that can be expected to occur over the entire temperature range of the capacitor.

Aluminum electrolytics show a marked increase in ESR at low temperatures (ESR can increase by a factor of 30 or more when going from 25°C to −30°C) which could lead to oscillation problems in applications with very low ambient temperatures. Solid tantalum capacitors are recommended for use in such cases.

Regulator instability can be caused by stray (board layout) capacitance appearing at the Feedback terminal. Oscillations from this effect are most likely to occur when very high value resistors are used to set the output voltage.

Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitor to at least 22 μF will stop the oscillations.

MINIMUM LOAD

The internal resistive divider in the LP2960 provides sufficient output loading for proper regulation. If external resistors are used to set the LP2960 output voltage, a minimum current of 5 μA through the external resistive divider is recommended.

It should be noted that a minimum load current is specified in several of the test conditions listed under *Electrical Characteristics,* and this value of load current must be used to get correlation on these test limits.

PROGRAMMING THE OUTPUT VOLTAGE

The LP2960 regulator may be pin-strapped for operation at the nominal output voltage using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and V_{TAP} pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see Basic Application Circuit).

The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times (1 + R1/R2) + (I_{FB} \times R1)$$

The term V_{REF} is the 1 .23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 5 μA sets an upper limit of 240 kΩ on the value of R2 in cases where the regulator must work with no load (see *Minimum Load*).

For best output accuracy, choosing R2 = 100 kΩ will reduce the error resulting from I_{FB} to 0.17% while increasing the resistive divider current to 12 μA. Since the typical quiescent current of the LP2960 is 450 μA, this added current through R2 is negligible.

DROPOUT VOLTAGE

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

OUTPUT ISOLATION

If the LP2960 output is connected to an active voltage source (such as a battery) the regulator input should not be shorted to ground, as this will cause a large current to flow from the battery into the LP2960 output lead.

If the LP2960 input is *left floating* with the output connected to a battery, a small current (a few mA) will flow into the output lead.

The "reverse" current flowing from the battery into the LP2960 output can be prevented by using a blocking diode between the output and the battery.

REDUCING OUTPUT NOISE

In reference applications it may be desirable to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to *Basic Application Circuit*).

A 0.1 μF capacitor connected across R1 will reduce the high frequency gain of the circuit to unity, lowering the RMS output noise voltage from 210 μV to 130 μV (typical) using a 10 Hz–100 kHz bandwidth test measurement.

Also, output noise is no longer proportional to the output voltage, so improvements are more pronounced at higher output voltages.

IMPORTANT: Since the 0.1 μF capacitor reduces the AC gain of the LP2960 to unity, the output capacitance must be increased to at least 33 μF to assure regulator stability.

Application Hints (Continued)

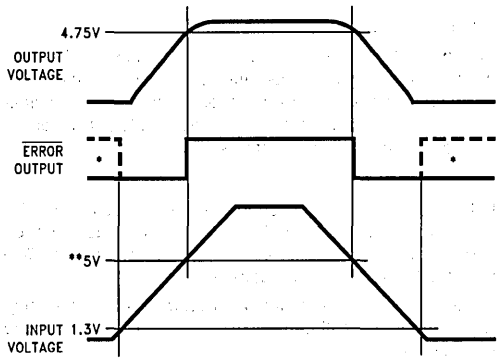
DROPOUT DETECTION COMPARATOR

The dropout detection comparator produces a logic "LOW" on the Error output whenever the LP2960 output drops out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to block diagram).

The "5% below nominal" trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

The figure below gives a timing diagram showing the relationship between the output voltage, the Error output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output.

Error Output Timing Diagram



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*In shutdown mode, ERROR will go high if it has been pulled up to an external supply. To avoid this invalid response, pull-up to regulator output.

**Exact value depends on dropout voltage. (See Application Hints)

The Error signal becomes low as V_{IN} exceeds about 1.3V. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the *input voltage* trip points will vary with load current, but the *output voltage* trip point does not.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the LP2960 output or another supply voltage.

Best operation is obtained by connecting the pull-up to the LP2960 output. If the pull-up resistor is connected to an external 5V supply, the error flag will incorrectly signal "HIGH" whenever $V_{IN} < 1.3V$ (see *Error Output Timing Diagram*).

In selecting a value for the pull-up resistor, note that while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ–1 MΩ. The resistor is not required if the output is unused.

If a large output capacitance is used, a false logic "HIGH" can be generated when $V_{IN} \approx 1.3V$. In this case, the error output becomes a high impedance, causing the voltage at the error output to rise to its pull-up value. If the pull-up resistor is connected to V_{OUT}, the error output can rise to 1.2V (which is a logic "HIGH" signal *incorrectly* signifying the output is in regulation).

The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

AUXILIARY COMPARATOR

The LP2960 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

SHUTDOWN INPUT

A logic-level signal will shut off the regulator output when a "LOW" (< 1.2V) is applied to the Shutdown input.

To prevent possible mis-operation, the Shutdown input must be actively terminated. If the input is driven from open-collector logic, a pull-up resistor (20 kΩ–100 kΩ recommended) should be connected from the Shutdown input to the regulator input.

If the Shutdown input is driven from a source which actively pulls low and high (like an op-amp), the pull-up resistor is not required, but may be used.

If the Shutdown input is to be unused, the cost of the pull-up resistor can be saved by tying the Shutdown input directly to the regulator input.

IMPORTANT: Since the Absolute Maximum Ratings state that the Shutdown input can not go more than 0.3V below ground, the reverse-battery protection feature which protects the regulator input is sacrificed if the Shutdown input is tied directly to the regulator input.

If reverse-battery protection is required in an application, *the pull-up resistor between the Shutdown input and the regulator input must be used.*

GROUND CONNECTIONS

The pins designated GND (see *Connection Diagrams*) must be connected to the high-current ground point in the circuit.

The GND pins are electrically connected (through the lead frame) to the die substrate, making them ideal for conducting ground current or heat (see *Heatsinking*).

The parts in the surface-mount (M) package also have an Analog Ground pin, which is the ground point on the die for the regulator reference circuitry.

Along with the Sense pin, the availability of the Analog Ground pin allows the designer the ability to use "remote" sensing and eliminate output voltage errors due to IR drops occurring along PC board traces.

IMPORTANT: The Analog Ground pin must be connected to circuit ground at some point for the regulator to operate.

If remote sensing is not needed, the Analog Ground pin can simply be pin-strapped to the adjacent GND pin.

HEATSINKING

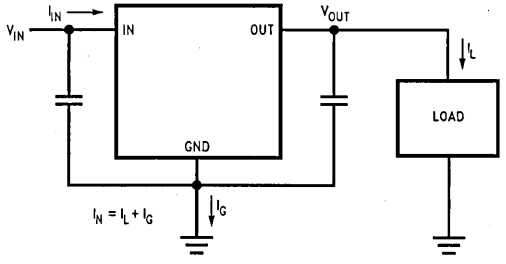
A heatsink may be required with the LP2960 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

Application Hints (Continued)

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:

Power Dissipation Diagram



$$P_D = (V_{IN} - V_{OUT})\, I_L + (V_{IN})\, I_G$$

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The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$$T_R\,(\text{max}) = T_J\,(\text{max}) - T_A\,(\text{max})$$

where:

T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts.

T_A (max) is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T_R (max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

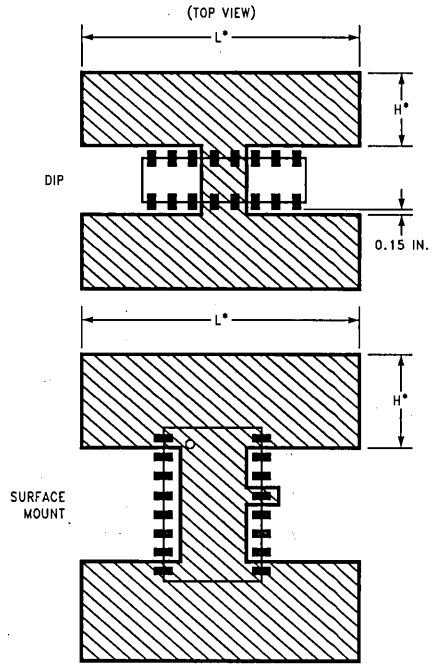
$$\theta_{(J-A)} = T_R\,(\text{max})/P_D$$

The heatsink for the LP2960 is made using the PC board copper, with the heat generated on the die being conducted through the lead frame and out to the pins which are soldered to the PC board.

The GND pins are the only ones capable of conducting any significant amount of heat, as they are internally attached to the lead frame on which the die is mounted.

The figure below shows recommended copper foil patterns to be used for heatsinking the DIP and Surface Mount packages:

Heat Sink Foil Patterns



*FOR BEST RESULTS, USE L = 2H

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The table below shows measured values of $\theta_{(J-A)}$ for a PC board with 1 ounce copper weight:

Package	L (in.)	H (in.)	θ_{J-A}(°C/W)
DIP	1	0.5	50
	2	0.2	52
Surface Mount	1	0.5	72
	2	0.2	74

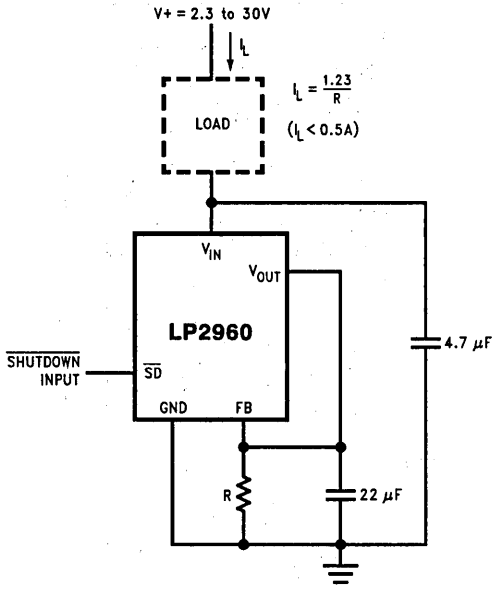
As the heat must transfer from the copper to the surrounding air, best results (lowest θ_{J-A}) will be obtained by using a *surface* copper layer with the solder resist opened up over the heatsink area.

If an *internal* copper layer of a multi-layer board is used for heatsinking, the board material acts as an insulator, inhibiting heat transfer and increasing θ_{J-A}.

As with any heatsink, increasing the airflow across the board will significantly improve the heat transfer.

Typical Applications

Low T.C. Current Sink



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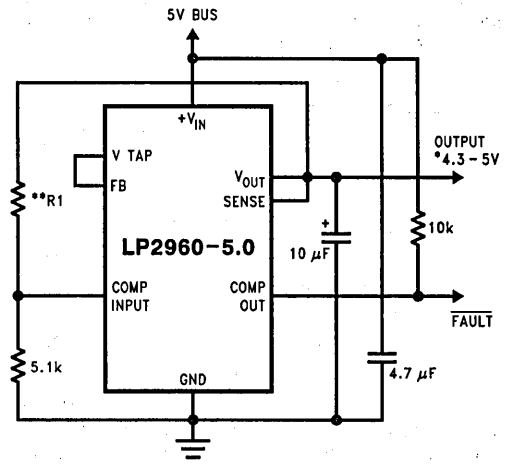
5V Bus Current Limiter with Load Fault Indicator



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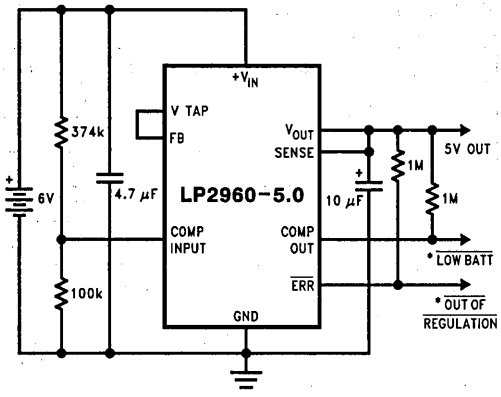
*Output voltage equals +V_{IN} minus dropout voltage, which varies with output current. Current limits at a maximum of 1000 mA (typical).

**Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION



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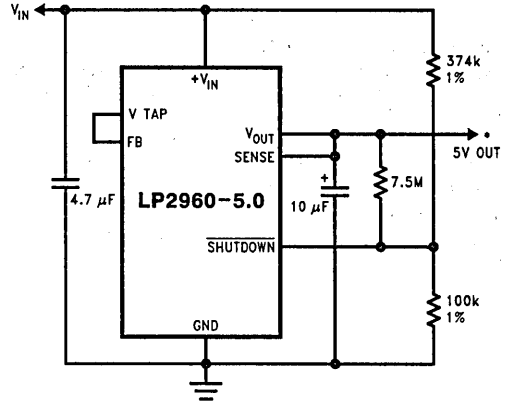
*Connect to Logic or µP control inputs.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power-down some hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

5V Regulator with Snap-ON/Snap-OFF Feature and Hysteresis



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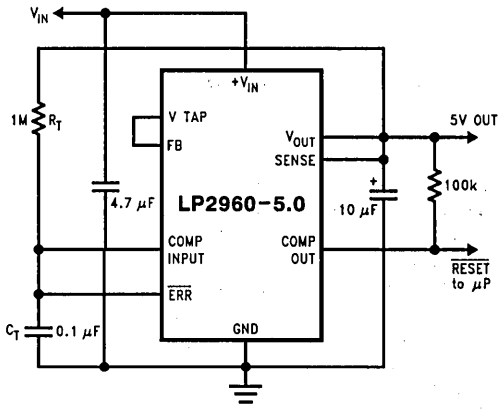
*Turns ON at V_{IN} = 5.87V
Turns OFF at V_{IN} = 5.64V
(for component values shown)

Typical Applications (Continued)

5V Regulator with Timed Power-On Reset



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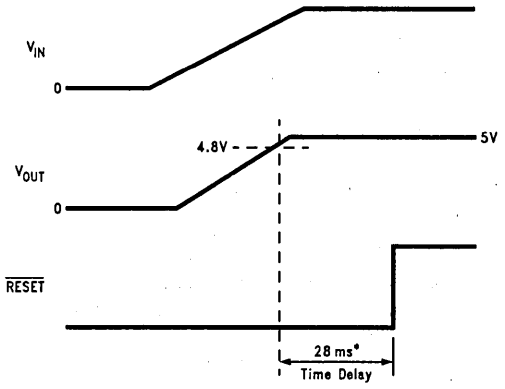
Timing Diagram for Timed Power-On Reset



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*R_T = 1 Meg, C_T = 0.1 μF

National Semiconductor

LP2980
Micropower SOT, 50 mA Ultra Low-Dropout Regulator

General Description

The LP2980 is a 50 mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2980 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage. Typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current. Typically 375 μA @ 50 mA load, and 80 μA @ 1 mA load.

Sleep Mode. Less than 1 μA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size. SOT-23 package uses an absolute minimum of board space.

Minimum Part Count. Requires only 1 μF of external capacitance on the regulator output.

Precision Output. 0.5% tolerance output voltages available (A grade).

5.0V, 3.3V, and 3.0V versions available as standard products.

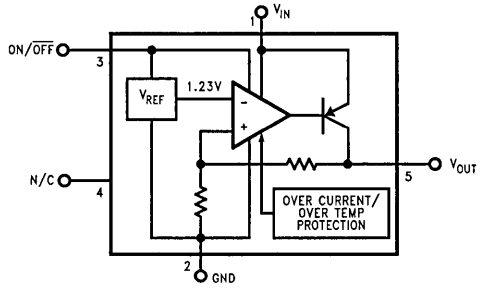
Features

- Ultra low dropout voltage
- Output voltage accuracy 0.5% (A Grade)
- Guaranteed 50 mA output current
- Smallest possible size (SOT-23 Package)
- Requires only 1 μF external capacitance
- < 1 μA quiescent current when shutdown
- Low ground pin current at all load currents
- High peak current capability (150 mA typical)
- Wide supply voltage range (16V max)
- Fast dynamic response to line and load
- Low Z_{OUT} over wide frequency range
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

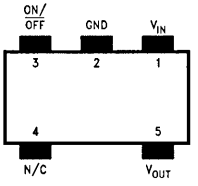
Block Diagram



TL/H/12078–1

Connection Diagram and Ordering Information

5-Lead Small Outline Package (M5)



TL/H/12078–3

Top View

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Actual Size

For Ordering Information See Table I in this Datasheet
See NS Package Number MA05A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 5 sec.)	260°C
ESD Rating (Note 2)	2 kV
Power Dissipation (Note 3)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Shutdown Input Voltage (Survival)	−0.3V to +16V
Output Voltage (Survival, Note 4)	−0.3V to +9V
I_{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival, Note 5)	−0.3V to +16V

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1V$, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/OFF}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2980AI-XX (Note 6)		LP2980I-XX (Note 6)		Units
				Min	Max	Min	Max	
V_O	Output Voltage (5.0V Versions)	$V_{IN} = V_{O(NOM)} + 1V$	5.0	4.975	5.025	4.950	5.050	V
		1 mA < I_L < 50 mA	5.0	4.962 **4.875**	5.038 **5.125**	4.925 **4.825**	5.075 **5.175**	
	Output Voltage (3.3V Versions)	$V_{IN} = V_{O(NOM)} + 1V$	3.3	3.283	3.317	3.267	3.333	
		1 mA < I_L < 50 mA	3.3	3.275 **3.217**	3.325 **3.383**	3.250 **3.184**	3.350 **3.416**	
	Output Voltage (3.0V Versions)	$V_{IN} = V_{O(NOM)} + 1V$	3.0	2.985	3.015	2.970	3.030	
		1 mA < I_L < 50 mA	3.0	2.977 **2.925**	3.023 **3.075**	2.955 **2.895**	3.045 **3.105**	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Output Voltage Line Regulation	$V_{O(NOM)} + 1V \le V_{IN} \le 16V$	0.007		0.014 **0.032**		0.014 **0.032**	%/V
$V_{IN}-V_O$	Dropout Voltage (Note 7)	I_L = 0	1		3 **5**		3 **5**	mV
		I_L = 1 mA	7		10 **15**		10 **15**	
		I_L = 10 mA	40		60 **90**		60 **90**	
		I_L = 50 mA	120		150 **225**		150 **225**	
I_{GND}	Ground Pin Current	I_L = 0	65		95 **125**		95 **125**	µA
		I_L = 1 mA	80		110 **170**		110 **170**	
		I_L = 10 mA	140		220 **460**		220 **460**	
		I_L = 50 mA	375		600 **1200**		600 **1200**	
		$V_{ON/OFF}$ < 0.18V	0		**1**		**1**	
$V_{ON/OFF}$	ON/OFF Input Voltage (Note 8)	High = O/P ON	1.4	**2.0**		**2.0**		V
		Low = O/P OFF	0.55		**0.18**		**0.18**	
$I_{ON/OFF}$	ON/OFF Input Current	$V_{ON/OFF}$ = 0	0		**−1**		**−1**	µA
		$V_{ON/OFF}$ = 5V	5		**15**		**15**	

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1V$, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/OFF}$ = 2V. (Continued)

Symbol	Parameter	Conditions	Typ	LP2980AI-XX (Note 6)		LP2980I-XX (Note 6)		Units
				Min	Max	Min	Max	
$I_{O(PK)}$	Peak Output Current	$V_{OUT} \geq V_{O(NOM)} - 5\%$	150	100		100		mA
e_n	Output Noise Voltage (RMS)	BW = 300 Hz–50 kHz, C_{OUT} = 10 µF	160					µV
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Ripple Rejection	f = 1 kHz C_{OUT} = 10 µF	63					dB
$I_{O(MAX)}$	Short Circuit Current	R_L = 0 (Steady State) (Note 9)	150					mA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The ESD rating of pins 3 and 4 is 1 kV.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P\,(MAX) = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

The value of θ_{JA} for the SOT-23 package is 300°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980 output must be diode-clamped to ground.

Note 5: The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode (see Application Hints).

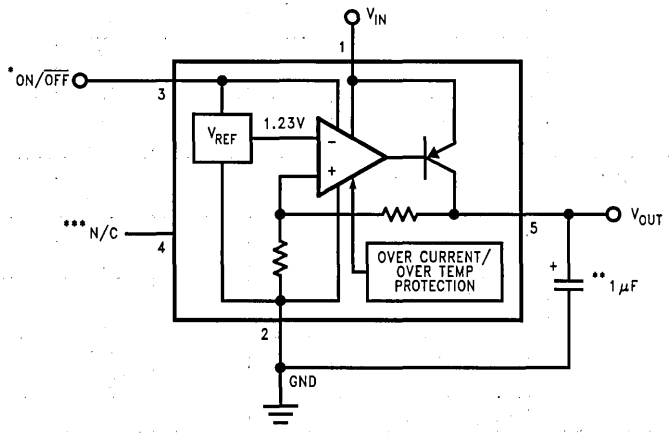
Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Averaging Outgoing Level (AOQL).

Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.

Note 8: The ON/OFF inputs must be properly driven to prevent misoperation. For details, refer to Application Hints.

Note 9: See Typical Performance Characteristics curves.

Basic Application Circuit



TL/H/12078–2

*ON/$\overline{\text{OFF}}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used.

**Minimum Output Capacitance is 1 µF to insure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin (see Application Hints).

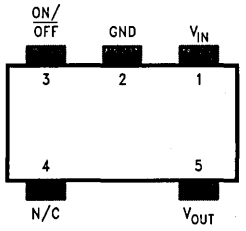
***Do not make connections to this pin.

Ordering Information

TABLE I. Package Marking and Order Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5.0	A	LP2980AIM5X-5.0	L01A	3k Units on Tape and Reel
5.0	A	LP2980AIM5-5.0	L01A	250 Units on Tape and Reel
5.0	STD	LP2980IM5X-5.0	L01B	3k Units on Tape and Reel
5.0	STD	LP2980IM5-5.0	L01B	250 Units on Tape and Reel
3.3	A	LP2980AIM5X-3.3	L00A	3k Units on Tape and Reel
3.3	A	LP2980AIM5-3.3	L00A	250 Units on Tape and Reel
3.3	STD	LP2980IM5X-3.3	L00B	3k Units on Tape and Reel
3.3	STD	LP2980IM5-3.3	L00B	250 Units on Tape and Reel
3.0	A	LP2980AIM5X-3.0	L02A	3k Units on Tape and Reel
3.0	A	LP2980AIM5-3.0	L02A	250 Units on Tape and Reel
3.0	STD	LP2980IM5X-3.0	L02B	3k Units on Tape and Reel
3.0	STD	LP2980IM5-3.0	L02B	250 Units on Tape and Reel

Connection Diagram



TL/H/12078–3

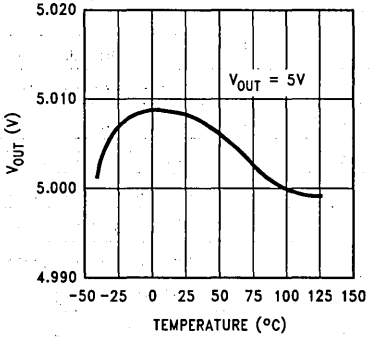
Top View

See NS Package Number MA05A

Typical Performance Characteristics

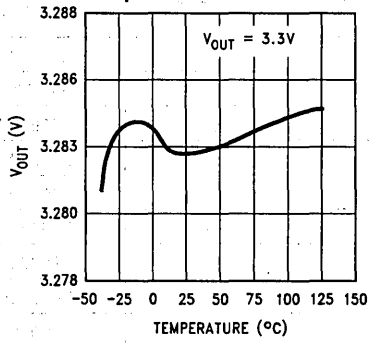
Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Output Voltage vs Temperature



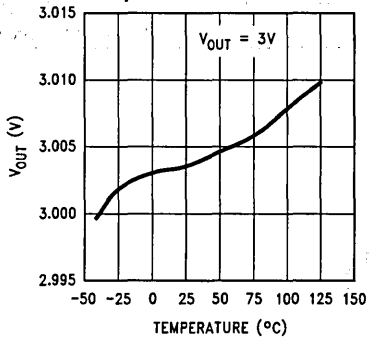
TL/H/12078-9

Output Voltage vs Temperature



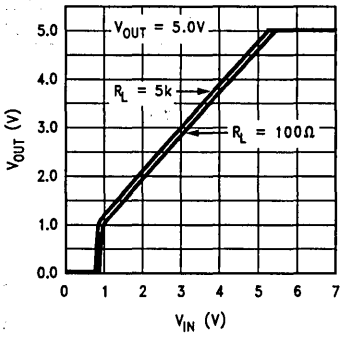
TL/H/12078-39

Output Voltage vs Temperature



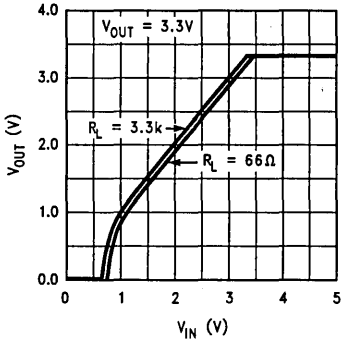
TL/H/12078-40

Dropout Characteristics



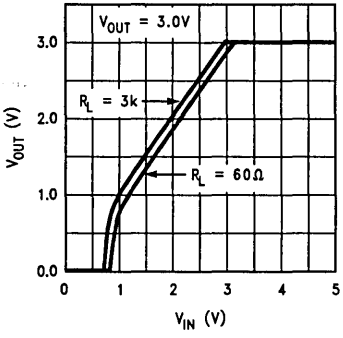
TL/H/12078-16

Dropout Characteristics



TL/H/12078-15

Dropout Characteristics

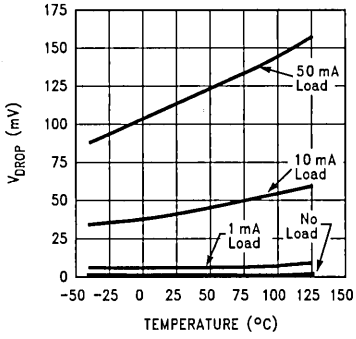


TL/H/12078-14

Typical Performance Characteristics (Continued)

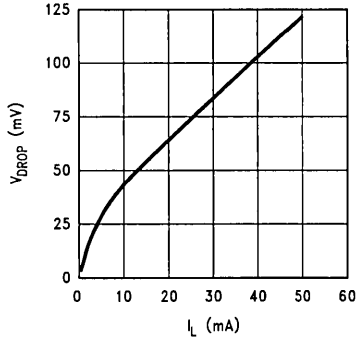
Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Dropout Voltage vs Temperature



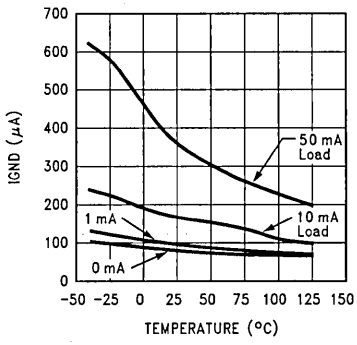
TL/H/12078–11

Dropout Voltage vs Load Current



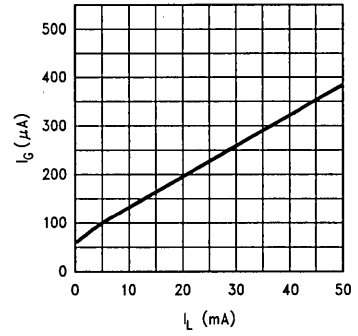
TL/H/12078–20

Ground Pin Current vs Temperature



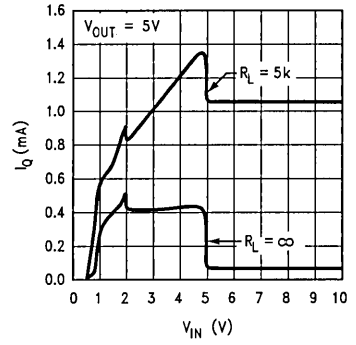
TL/H/12078–10

Ground Pin Current vs Load Current



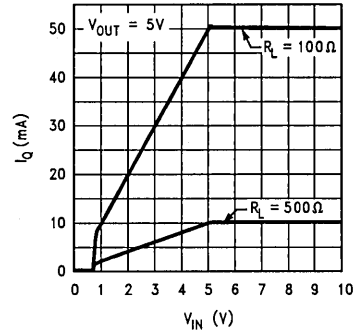
TL/H/12078–19

Input Current vs V_{IN}



TL/H/12078–17

Input Current vs V_{IN}

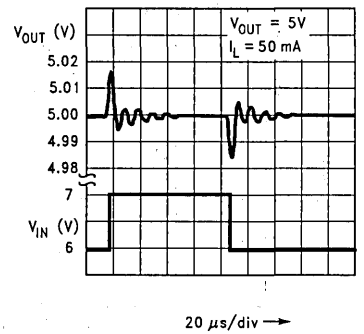


TL/H/12078–18

Typical Performance Characteristics (Continued)

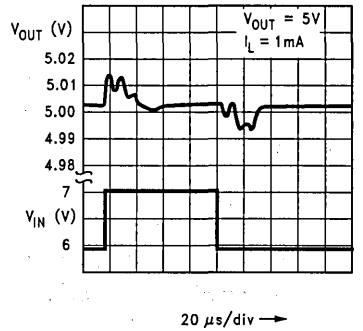
Unless otherwise specified: $T_A = 25°C$, $V_{IN} = V_{O(NOM)} + 1V$, $C_{OUT} = 2.2\ \mu F$, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Line Transient Response



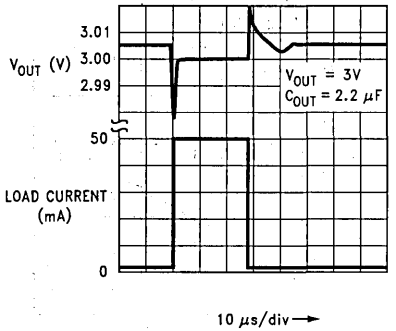
TL/H/12078–21

Line Transient Response



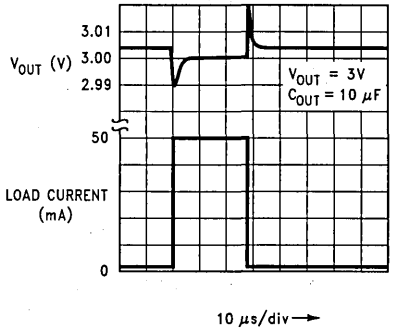
TL/H/12078–22

Load Transient Response



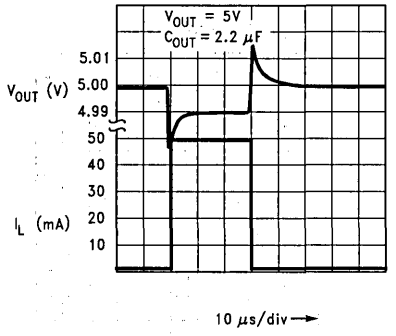
TL/H/12078–41

Load Transient Response



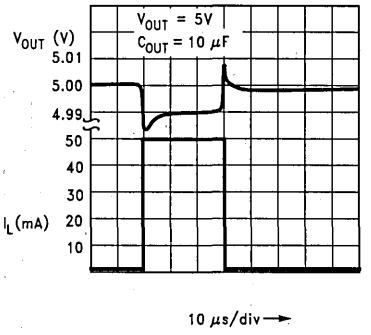
TL/H/12078–42

Load Transient Response



TL/H/12078–23

Load Transient Response

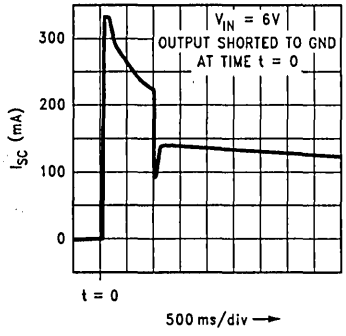


TL/H/12078–24

Typical Performance Characteristics (Continued)

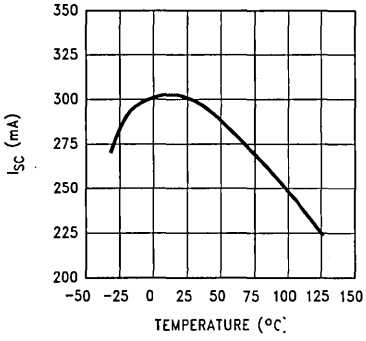
Unless otherwise specified: $T_A = 25°C$, $V_{IN} = V_{O(NOM)} + 1V$, $C_{OUT} = 2.2\ \mu F$, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Short Circuit Current



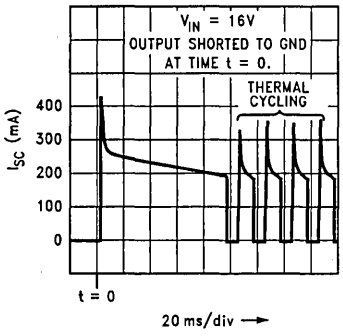
TL/H/12078-32

Instantaneous Short Circuit Current vs Temperature



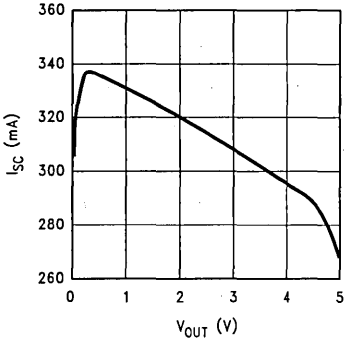
TL/H/12078-12

Short Circuit Current



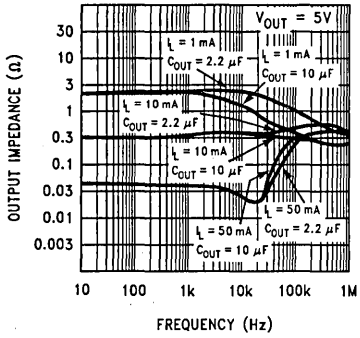
TL/H/12078-33

Instantaneous Short Circuit Current vs Output Voltage



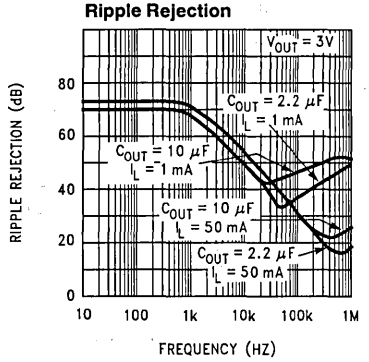
TL/H/12078-43

Output Impedance vs Frequency



TL/H/12078-44

Ripple Rejection

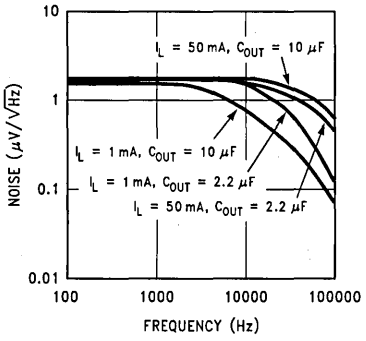


TL/H/12078-25

Typical Performance Characteristics (Continued)

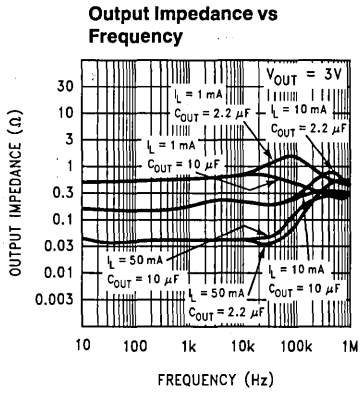
Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

Output Noise Density



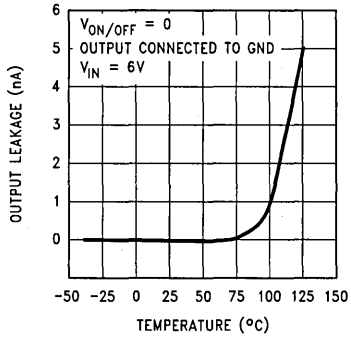
TL/H/12078-27

Output Impedance vs Frequency



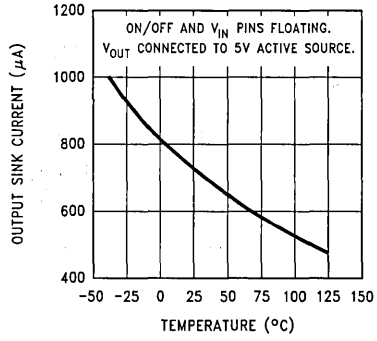
TL/H/12078-26

Input to Output Leakage vs Temperature



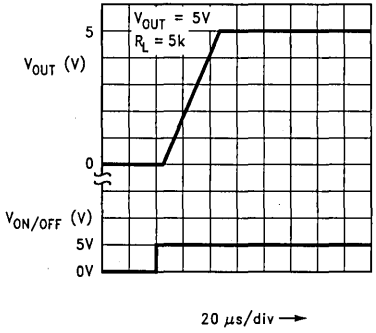
TL/H/12078-28

Output Reverse Leakage vs Temperature



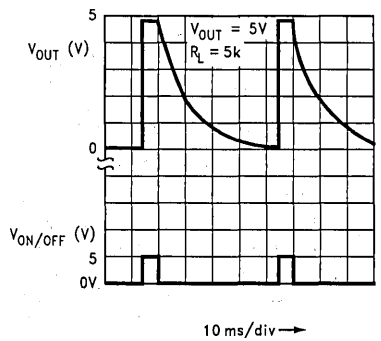
TL/H/12078-29

Turn-On Waveform



TL/H/12078-30

Turn-Off Waveform

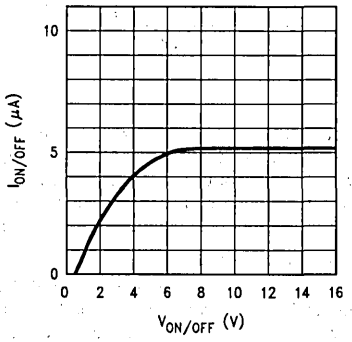


TL/H/12078-31

Typical Performance Characteristics (Continued)

Unless otherwise specified:
T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1V, C_{OUT} = 2.2 µF, all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

ON/OFF Pin Current vs $V_{ON/OFF}$



TL/H/12078–45

Application Hints

OUTPUT CAPACITOR

Like any low-dropout regulator, the LP2980 requires an output capacitor to maintain regulator loop stability. This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance (ESR) range. It is not difficult to find capacitors which meet the criteria of the LP2980, as the acceptable capacitance and ESR ranges are wider than for most other LDOs.

In general, the capacitor value must be at least 1 µF (over the actual ambient operating temperature), and the ESR must be within the range indicated in *Figures 1, 2,* and *3*. It should be noted that, although a maximum ESR is shown in these Figures, it is very unlikely to find a capacitor with ESR that high.

Tantalum Capacitors

Surface-mountable solid tantalum capacitors offer a good combination of small physical size for the capacitance value, and ESR in the range needed by the LP2980.

The results of testing the LP2980 stability with surface-mount solid tantalum capacitors show good stability with values of at least 1 µF. The value can be increased to 2.2 µF (or more) for even better performance, including transient response and noise.

Small value tantalum capacitors that have been verified as suitable for use with the LP2980 are shown in Table II. Capacitance values can be increased without limit.

Aluminum Electrolytic Capacitors

Although probably not a good choice for a production design, because of relatively large physical size, an aluminum electrolytic capacitor can be used in the design prototype for an LP2980 regulator. A value of at least 1 µF should be used, and the ESR must meet the conditions of *Figures 1, 2,* and *3*. If the operating temperature drops below 0°C, the regulator may not remain stable, as the ESR of the aluminum electrolytic capacitor will increase, and may exceed the limits indicated in the Figures.

TABLE II. Surface-Mount Tantalum Capacitor Selection Guide

1 µF Surface-Mount Tantalums	
Manufacturer	**Part Number**
Kemet	T491A105M010AS
NEC	NRU105M10
Siemens	B45196-E3105-K
Nichicon	F931C105MA
Sprague	293D105X0016A2T
2.2 µF Surface-Mount Tantalums	
Manufacturer	**Part Number**
Kemet	T491A225M010AS
NEC	NRU225M06
Siemens	B45196/2.2/10/10
Nichicon	F930J225MA
Sprague	293D225X0010A2T

Multilayer Ceramic Capacitors

Surface-mountable multilayer ceramic capacitors may be an attractive choice because of their relatively small physical size and excellent RF characteristics. However, they sometimes have ESR values lower than the minimum required by the LP2980, and relatively large capacitance change with temperature. The manufacturer's datasheet for the capacitor should be consulted before selecting a value.

Test results of LP2980 stability using multilayer ceramic capacitors show that a minimum value of 2.2 µF is usually needed for the 5V regulator. For the lower output voltages, or for better performance, a higher value should be used, such as 4.7 µF.

Multilayer ceramic capacitors that have been verified as suitable for use with the LP2980 are shown in Table III.

TABLE III. Surface-Mount Multilayer Ceramic Capacitor Selection Guide

2.2 µF Surface-Mount Ceramic	
Manufacturer	**Part Number**
Tokin	1E225ZY5U-C203
Murata	GRM42-6Y5V225Z16
4.7 µF Surface-Mount Ceramic	
Manufacturer	**Part Number**
Tokin	1E475ZY5U-C304

Application Hints (Continued)

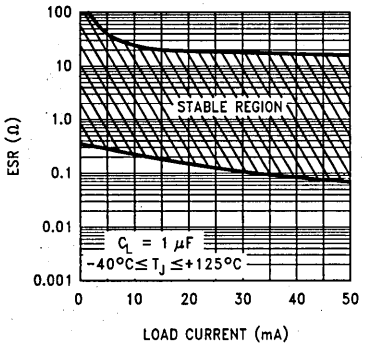


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FIGURE 1. 1 μF ESR Range

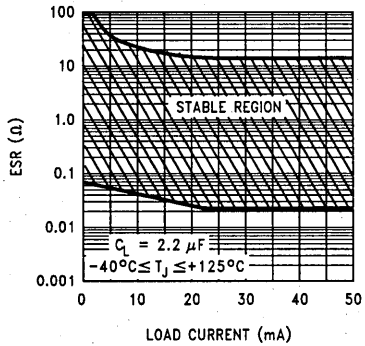

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FIGURE 2. 2.2 μF ESR Range

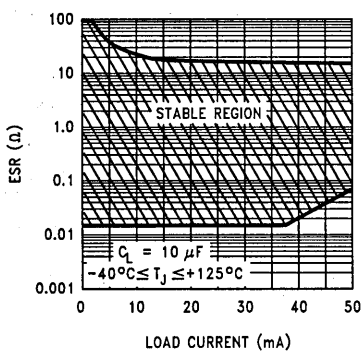

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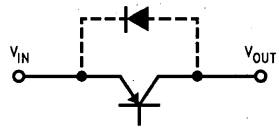
FIGURE 3. 10 μF ESR Range

REVERSE CURRENT PATH

The power transistor used in the LP2980 has an inherent diode connected between the regulator input and output (see below).



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If the output is forced above the input by more than a V_{BE}, this diode will become forward biased and current will flow from the V_{OUT} terminal to V_{IN}. No damage to the LP2980 will occur under these conditions as long as the current flowing into the output pin does not exceed 100 mA.

ON/OFF INPUT OPERATION

The LP2980 is shut off by pulling the ON/OFF input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input should be tied to V_{IN} to keep the regulator on at all times (the ON/OFF input must **not** be left floating).

To ensure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which guarantee an ON or OFF state (see Electrical Characteristics).

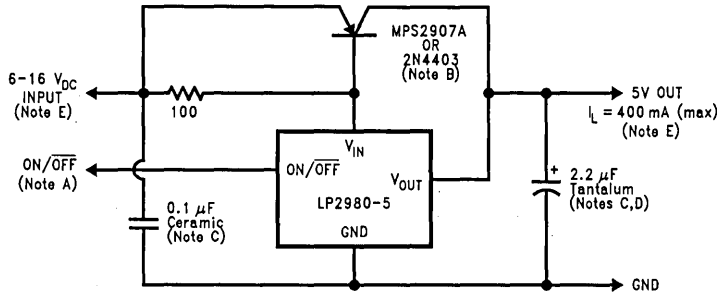
The ON/OFF signal may come from either a totem-pole output, or an open-collector output with pull-up resistor to the LP2980 input voltage or another logic supply. The high-level voltage may exceed the LP2980 input voltage, but must remain within the Absolute Maximum Ratings for the ON/OFF pin.

It is also important that the turn-on/turn-off voltage signals applied to the ON/OFF input have a slew rate which is greater than 40 mV/μs.

Important: the regulator shutdown function will operate incorrectly if a slow-moving signal is applied to the ON/OFF input.

Typical Applications

5V/400 mA Regulator



TL/H/12078-51

The LP2980 can be used to control higher-current regulators, by adding an external PNP pass device. With the PNP transistors shown, the output current can be as high as 400 mA, as long as the input voltage is held within the Safe Operation Boundary Curves shown below.

To ensure regulation, the minimum input voltage of this regulator is 6V. This "headroom" is the sum of the V_{BE} of the external transistor and the dropout voltage of the LP2980.

Notes:

A. Drive this input with a logic signal (see Application Hints). If the shutdown function is not to be used, tie the ON/OFF pin directly to the V_{IN} pin.

B. Recommended devices (other PNP transistors can be used if the current gain and voltage ratings are similar).

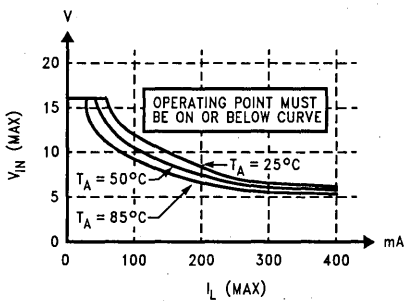
C. Capacitor is required for regulator stability. Minimum size is shown, and may be increased without limit.

D. Increasing the output capacitance improves transient response and increases phase margin.

E. Maximum safe input voltage and load current are limited by power dissipation in the PNP pass transistor and the maximum ambient temperature for the specific application. If a TO-92 transistor such as the MPS2907A is used, the thermal resistance from junction-to-ambient is 180°C/W in still air.

Assuming a maximum allowable junction temperature of 150°C for the MPS2907A device, the following curves show the maximum V_{IN} and I_L values that may be safely used for several ambient temperatures.

Safe Operation Boundary Curves



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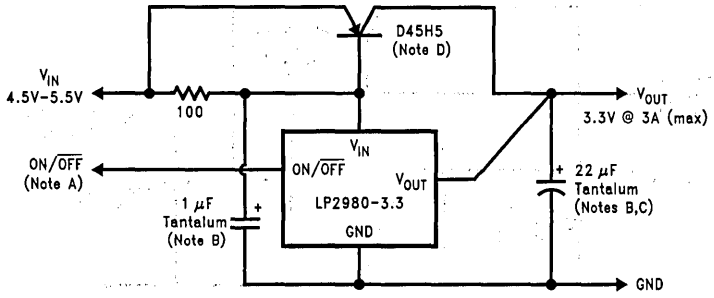
Typical Applications (Continued)

5V to 3.3V @ 3A Converter



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With limited input voltage range, the LP2980 can control a 3.3V, 3A regulator with the use of a high current-gain external PNP pass transistor. If the regulator is to be loaded with the full 3A, heat sinking will be required on the pass transistor to keep it within its rated temperature range. Refer to the Heatsink Thermal Resistance Requirements, below. For best load regulation at the high load current, the LP2980 output voltage connection should be made as close to the load as possible.

Although this regulator can handle a much higher load current than can the LP2980 alone, it can be shut down in the same manner as the LP2980. When the ON/OFF control is brought low, the converter will be in shutdown, and will draw less than 1 μA from the source.

Notes:

A. Drive this input with a logic signal (see Application Hints). If the shutdown function is not to be used, tie the ON/OFF pin directly to the V_{IN} pin.

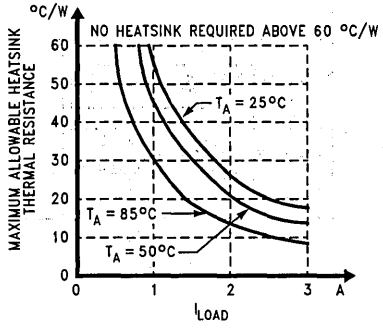
B. Capacitor is required for regulator stability. Minimum size is shown, and may be increased without limit.

C. Increasing the output capacitance improves transient response and increases phase margin.

D. A heatsink may be required for this transistor. The maximum allowable value for thermal resistance of the heatsink is dependent on ambient temperature and load current (see curves below). Once the value is obtained from the graph, a heatsink must be selected which has a thermal resistance equal to or lower than this value. If the value is above 60°C/W, no heatsink is required (the TO-220 package alone will safely dissipate this).

For these curves, a maximum junction temperature of 150°C is assumed for the pass transistor. The case-to-heatsink attachment thermal resistance is assumed to be 1.5°C/W. All calculations are for 5.5V input voltage (which is worst-case for power dissipation).

Heatsink Thermal Resistance Requirements



TL/H/12078–54

National Semiconductor

LP2952/LP2952A/LP2953/LP2953A
Adjustable Micropower Low-Dropout Voltage Regulators

General Description

The LP2952 and LP2953 are micropower voltage regulators with very low quiescent current (130 μA typical at 1 mA load) and very low dropout voltage (typ. 60 mV at light load and 470 mV at 250 mA load current). They are ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2952 and LP2953 retain all the desirable characteristics of the LP2951, but offer increased output current, additional features, and an improved shutdown function.

The internal crowbar pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery protection is provided.

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good line and load regulation.

The parts are available in DIP and surface mount packages.

Features

- Output voltage adjusts from 1.23V to 29V
- Guaranteed 250 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse battery protection
- 50 mA (typical) output pulldown crowbar
- 5V and 3.3V versions available

LP2953 Versions Only

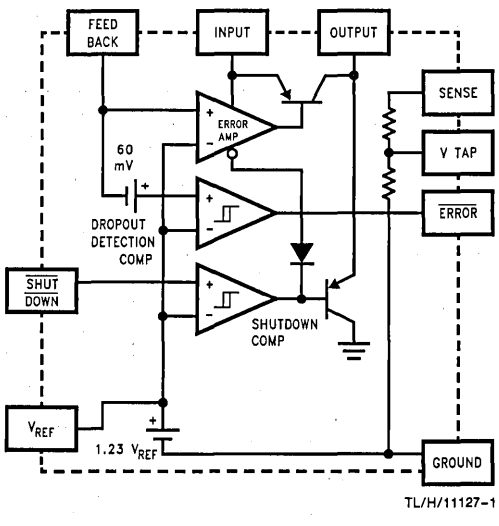
- Auxiliary comparator included with CMOS/TTL compatible output levels. Can be used for fault detection, low input line detection, etc.

Applications

- High-efficiency linear regulator
- Regulator with under-voltage shutdown
- Low dropout battery-powered regulator
- Snap-ON/Snap-OFF regulator

Block Diagrams

LP2952



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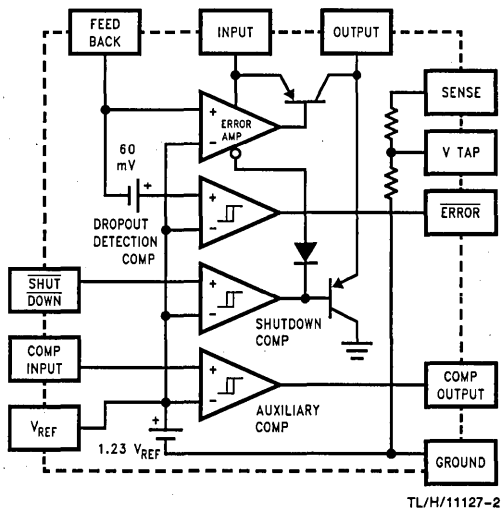
LP2953



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7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range $-65°C \le T_A \le +150°C$

Operating Temperature Range
LP2952I, LP2953I, LP2952AI, LP2953AI, LP2952I-3.3, LP2953I-3.3, LP2952AI-3.3, LP2953AI-3.3 $-40°C \le T_J \le +125°C$
LP2953AM $-55°C \le T_A \le +125°C$

Maximum Junction Temperature
LP2952I, LP2953I, LP2952AI, LP2953AI, LP2952I-3.3, LP2953I-3.3, LP2952AI-3.3, LP2953AI-3.3 +125°C
LP2953AM +150°C

Lead Temp. (Soldering, 5 seconds)	260°C
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage	−20V to +30V
Feedback Input Voltage (Note 3)	−0.3V to +5V
Comparator Input Voltage (Note 4)	−0.3V to +30V
Shutdown Input Voltage (Note 4)	−0.3V to +30V
Comparator Output Voltage (Note 4)	−0.3V to +30V
ESD Rating (Note 15)	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin.

3.3V Versions

Symbol	Parameter	Conditions	Typical	LP2952AI-3.3, LP2953AI-3.3		LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
V_O	Output Voltage		3.3	3.284 **3.260**	3.317 **3.340**	3.267 **3.234**	3.333 **3.366**	V
		1 mA ≤ I_L ≤ 250 mA	3.3	**3.254**	**3.346**	**3.221**	**3.379**	

5V Versions

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2953AM (Note 17)		LP2952I, LP2953I		Units
				Min	Max	Min	Max	
V_O	Output Voltage		5.0	4.975 **4.940**	5.025 **5.060**	4.950 **4.900**	5.050 **5.100**	V
		1 mA ≤ I_L ≤ 250 mA	5.0	**4.930**	**5.070**	**4.880**	**5.120**	

All Voltage Options

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (Note 17)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temp. Coefficient	(Note 5)	**20**		**100**		**150**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Output Voltage Line Regulation	$V_{IN} = V_O(NOM) + 1V$ to 30V	0.03		0.1 **0.2**		0.2 **0.4**	%
$\frac{\Delta V_O}{V_O}$	Output Voltage Load Regulation (Note 6)	I_L = 1 mA to 250 mA I_L = 0.1 mA to 1 mA	0.04		0.16 **0.20**		0.20 **0.30**	%
$V_{IN}-V_O$	Dropout Voltage (Note 7)	I_L = 1 mA	60		100 **150**		100 **150**	mV
		I_L = 50 mA	240		300 **420**		300 **420**	
		I_L = 100 mA	310		400 **520**		400 **520**	
		I_L = 250 mA	470		600 **800**		600 **800**	

Electrical Characteristics Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin. (Continued)

All Voltage Options (Continued)

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (Note 17)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
I_{GND}	Ground Pin Current (Note 8)	I_L = 1 mA	130		170 **200**		170 **200**	µA
		I_L = 50 mA	1.1		2 **2.5**		2 **2.5**	mA
		I_L = 100 mA	4.5		6 **8**		6 **8**	
		I_L = 250 mA	21		28 **33**		28 **33**	
I_{GND}	Ground Pin Current at Dropout (Note 8)	$V_{IN} = V_O(NOM) - 0.5V$ I_L = 100 µA	165		210 **240**		210 **240**	µA
I_{GND}	Ground Pin Current at Shutdown (Note 8)	(Note 9)	105		140		140	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0	380		500 **530**		500 **530**	mA
$\frac{\Delta V_O}{\Delta Pd}$	Thermal Regulation	(Note 10)	0.05		0.2		0.2	%/W
e_n	Output Noise Voltage (10 Hz to 100 kHz) I_L = 100 mA	C_L = 4.7 µF	400					µV RMS
		C_L = 33 µF	260					
		C_L = 33 µF (Note 11)	80					
V_{REF}	Reference Voltage	(Note 12)	1.230	1.215 **1.205**	1.245 **1.255**	1.205 **1.190**	1.255 **1.270**	V
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Line Regulation	$V_{IN} = 2.5V$ to $V_O(NOM) + 1V$ $V_{IN} = V_O(NOM) + 1V$ to 30V (Note 13)	0.03		0.1 **0.2**		0.2 **0.4**	%
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Load Regulation	I_{REF} = 0 to 200 µA	0.25		0.4 **0.6**		0.8 **1.0**	%
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temp. Coefficient	(Note 5)	**20**					ppm/°C
$I_{B(FB)}$	Feedback Pin Bias Current		20		40 **60**		40 **60**	nA
I_O (SINK)	Output "OFF" Pulldown Current	(Note 9)	50	30 **20**		30 **20**		mA

Electrical Characteristics Limits in standard typeface are for T_J = 25°C, **bold typeface** applies over the full operating temperature range. Limits are guaranteed by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, I_L = 1 mA, C_L = 2.2 µF for 5V parts and 4.7µF for 3.3V parts. Feedback pin is tied to V Tap pin, Output pin is tied to Output Sense pin. (Continued)

Symbol	Parameter	Conditions	Typical	LP2952AI, LP2953AI, LP2952AI-3.3, LP2953AI-3.3, LP2953AM (Note 17)		LP2952I, LP2953I, LP2952I-3.3, LP2953I-3.3		Units
				Min	Max	Min	Max	
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output "LOW" Voltage	$V_{IN} = V_O(NOM) - 0.5V$ $I_O(COMP)$ = 400 µA	150		250 **400**		250 **400**	mV
V_{THR} (MAX)	Upper Threshold Voltage	(Note 14)	−60	−80 **−95**	−35 **−25**	−80 **−95**	−35 **−25**	mV
V_{THR} (MIN)	Lower Threshold Voltage	(Note 14)	−85	−110 **−160**	−55 **−40**	−110 **−160**	−55 **−40**	mV
HYST	Hysteresis	(Note 14)	15					mV
SHUTDOWN INPUT (Note 16)								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±3	−7.5 **−10**	7.5 **10**	−7.5 **−10**	7.5 **10**	mV
HYST	Hysteresis		6					mV
I_B	Input Bias Current	V_{IN}(S/D) = 0V to 5V	10	−30 **−50**	30 **50**	−30 **−50**	−30 **50**	nA
		LP2953AM	10	−30 **−75**	30 **75**			
AUXILIARY COMPARATOR (LP2953 Only)								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±3	−7.5 **−10**	7.5 **10**	−7.5 **−10**	7.5 **10**	mV
		LP2953AM	±3	−7.5 **−12**	7.5 **12**			
HYST	Hysteresis		6					mV
I_B	Input Bias Current	V_{IN}(COMP) = 0V to 5V	10	−30 **−50**	30 **50**	−30 **−50**	30 **50**	nA
		LP2953AM	10	−30 **−75**	30 **75**			
I_{OH}	Output "HIGH" Leakage	V_{OH} = 30V V_{IN}(COMP) = 1.3V	0.01		1 **2**		1 **2**	µA
		LP2953AM	0.01		1 **2.2**			
V_{OL}	Output "LOW" Voltage	V_{IN}(COMP) = 1.1V $I_O(COMP)$ = 400 µA	150		250 **400**		250 **400**	mV
		LP2953AM	150		250 **420**			

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$.

Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See APPLICATION HINTS for additional information on heatsinking and thermal resistance.

Note 3: When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.

Note 4: May exceed the input supply voltage.

Note 5: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 6: Load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the range of 100 μA to 1 mA and one for the 1 mA to 250 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 7: Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V **(2.3V over temperature)** must be observed.

Note 8: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).

Note 9: $V_{SHUTDOWN} \leq 1.1V$, $V_{OUT} = V_O(NOM)$.

Note 10: Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 200 mA load pulse at $V_{IN} = V_O(NOM) + 15V$ (3W pulse) for $T = 10$ ms.

Note 11: Connect a 0.1 μF capacitor from the output to the feedback pin.

Note 12: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1V)$, $2.3V \leq V_{IN} \leq 30V$, $100\ \mu A \leq I_L \leq 250$ mA.

Note 13: Two separate tests are performed, one covering $2.5V \leq V_{IN} \leq V_O(NOM) + 1V$ and the other test for $V_O(NOM) + 1V \leq V_{IN} \leq 30V$.

Note 14: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at $V_{IN} = V_O(NOM) + 1V$. To express these thresholds in terms of output voltage change, multiply by the Error amplifier gain, which is $V_{OUT}/V_{REF} = (R1 + R2)/R2$ (refer to Figure 4).

Note 15: Human body model, 200 pF discharged through 1.5 kΩ.

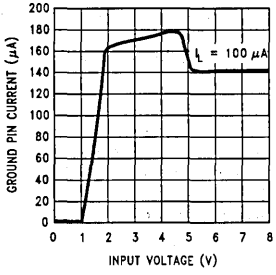
Note 16: Drive $\overline{\text{Shutdown}}$ pin with TTL or CMOS-low level to shut regulator OFF, high level to turn regulator ON.

Note 17: A military RETS specification is available upon request. At the time of printing, the LP2953AMJ/883C RETS specification complied with the **boldface** limits in this column.

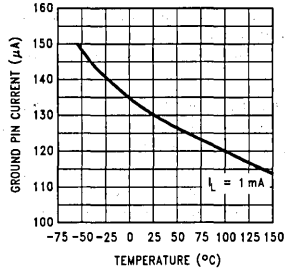
Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V.

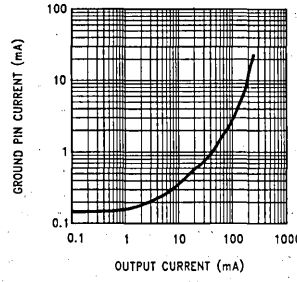
Quiescent Current



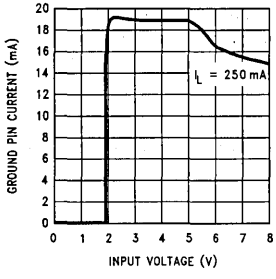
Quiescent Current



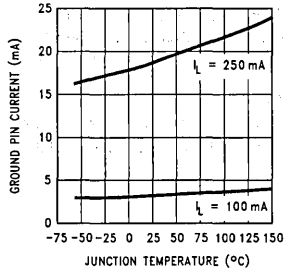
Ground Pin Current vs Load



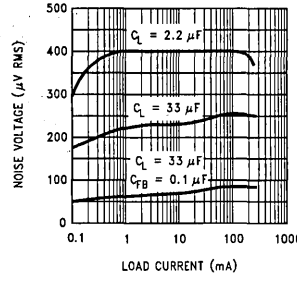
Ground Pin Current



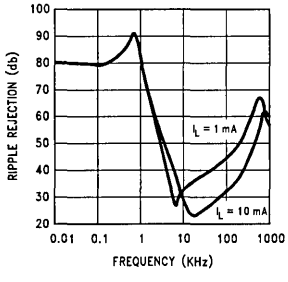
Ground Pin Current



Output Noise Voltage



Ripple Rejection



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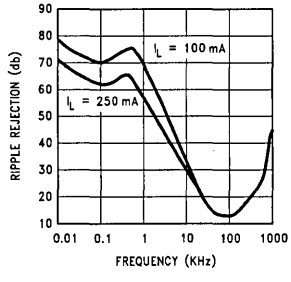
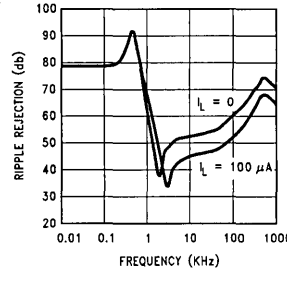
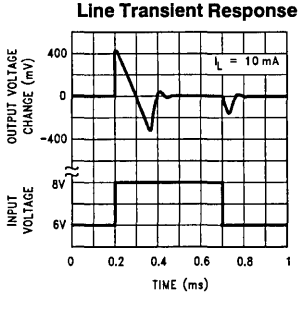


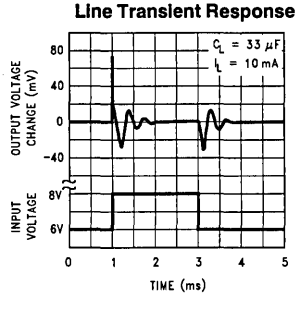
Ripple Rejection



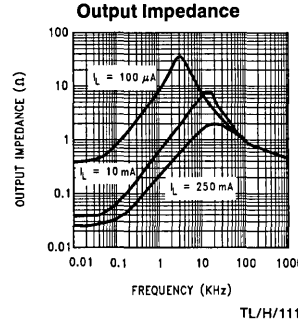
Line Transient Response



Line Transient Response



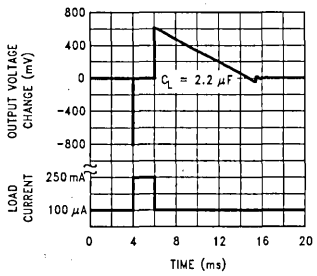
Output Impedance



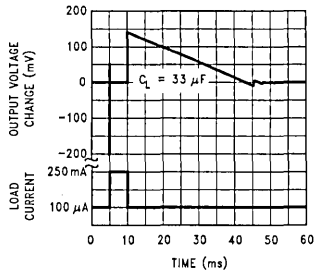
TL/H/11127–3

Typical Performance Characteristics Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V. (Continued)

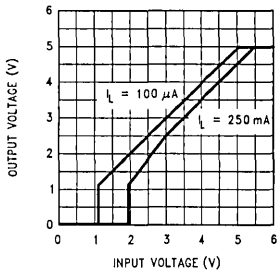
Load Transient Response



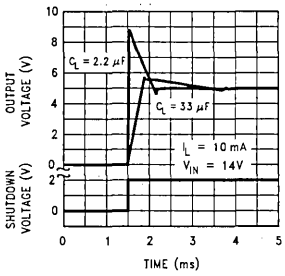
Load Transient Response



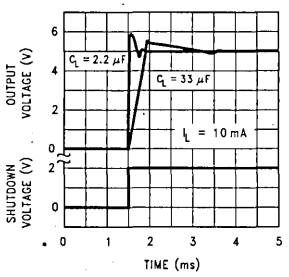
Dropout Characteristics



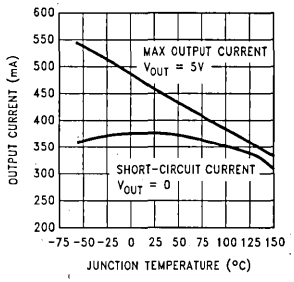
Enable Transient



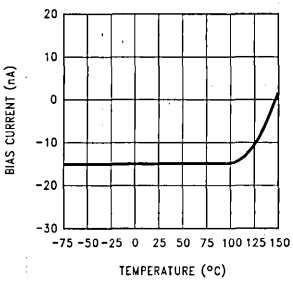
Enable Transient



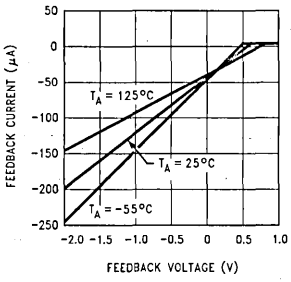
Short-Circuit Output Current and Maximum Output Current



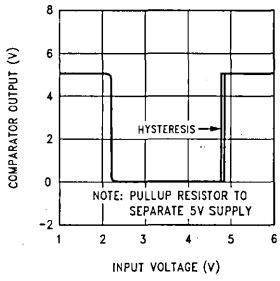
Feedback Bias Current



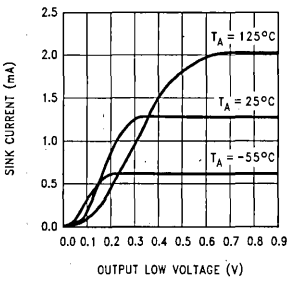
Feedback Pin Current



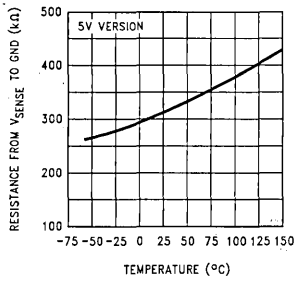
Error Output



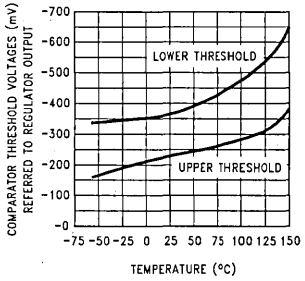
Comparator Sink Current



Divider Resistance



Dropout Detection Comparator Threshold Voltages



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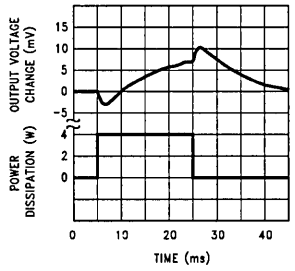
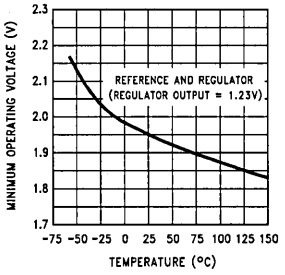
7

Typical Performance Characteristics Unless otherwise specified: V_{IN} = 6V, I_L = 1 mA, C_L = 2.2 µF, V_{SD} = 3V, T_A = 25°C, V_{OUT} = 5V. (Continued)

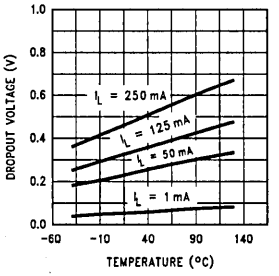
Thermal Regulation



Minimum Operating Voltage



Dropout Voltage



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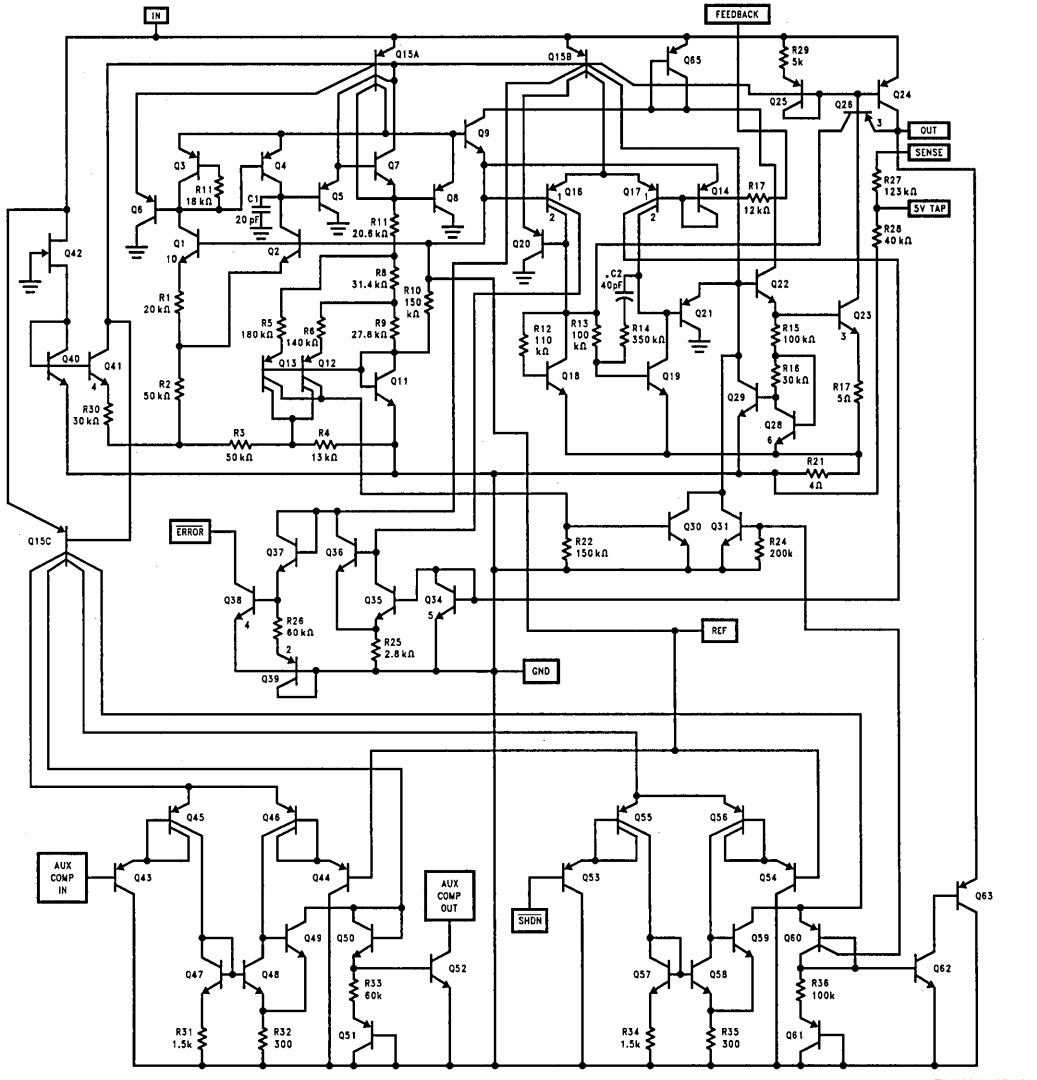
Schematic Diagram



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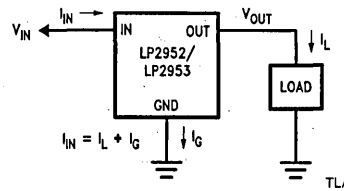
Application Hints

HEATSINK REQUIREMENTS (Industrial Temperature Range Devices)

The maximum allowable power dissipation for the LP2952/LP2953 is limited by the maximum junction temperature (+125°C) and the external factors that determine how quickly heat flows away from the part: the *ambient temperature* and the *junction-to-ambient thermal resistance* for the specific application.

The industrial temperature range ($-40°C \leq T_J \leq +125°C$) parts are manufactured in plastic DIP and surface mount packages which contain a copper lead frame that allows heat to be effectively conducted away from the die, through the ground pins of the IC, and into the copper of the PC board. Details on heatsinking using PC board copper are covered later.

To determine if a heatsink is required, the maximum power dissipated by the regulator, P(max), must be calculated. It is important to remember that if the regulator is powered from a transformer connected to the AC line, the **maximum specified AC input voltage** must be used (since this produces the maximum DC input voltage to the regulator). *Figure 1* shows the voltages and currents which are present in the circuit. The formula for calculating the power dissipated in the regulator is also shown in *Figure 1*:



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$$P_{TOTAL} = (V_{IN} - V_{OUT})\, I_L + (V_{IN})\, I_G$$

FIGURE 1. Current/Voltage Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$. This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)$$

where: $T_J(max)$ is the maximum allowable junction temperature

$T_A(max)$ is the maximum ambient temperature

Using the calculated values for $T_R(max)$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

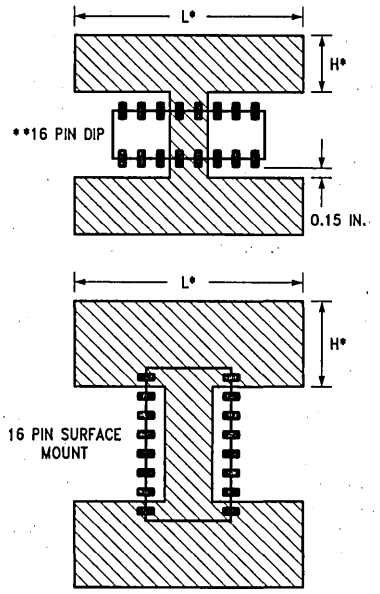
$$\theta_{(J-A)} = T_R(max)/P(max)$$

The heatsink is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

Part	Package	Pins
LP2952IN, LP2952AIN, LP2952IN-3.3, LP2952AIN-3.3	14-Pin DIP	3, 4, 5, 10, 11, 12
LP2953IN, LP2953AIN, LP2953IN-3.3, LP2953AIN-3.3	16-Pin DIP	4, 5, 12, 13
LP2952IM, LP2952AIM, LP2952IM-3.3, LP2952AIM-3.3, LP2953IM, LP2953AIM, LP2953IM-3.3, LP2953AIM-3.3	16-Pin Surface Mount	1, 8, 9, 16

Figure 2 shows copper patterns which may be used to dissipate heat from the LP2952 and LP2953:



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*For best results, use L = 2H

**14-Pin DIP is similar, refer to Table I for pins designated for heatsinking.

FIGURE 2. Copper Heatsink Patterns

Table II shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 1 oz. copper:

TABLE II

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
16-Pin DIP	1	0.5	70
	2	1	60
	3	1.5	58
	4	0.19	66
	6	0.19	66
14-Pin DIP	1	0.5	65
	2	1	51
	3	1.5	49
Surface Mount	1	0.5	83
	2	1	70
	3	1.5	67
	6	0.19	69
	4	0.19	71
	2	0.19	73

Application Hints (Continued)

HEATSINK REQUIREMENTS (Military Temperature Range Devices)

The maximum allowable power dissipation for the LP2953AMJ is limited by the maximum junction temperature (+150°C) and the two parameters that determine how quickly heat flows away from the die: *the ambient temperature and the junction-to-ambient thermal resistance of the part.*

The military temperature range ($-55°C \leq T_J \leq +150°C$) parts are manufactured in ceramic DIP packages which contain a KOVAR lead frame (unlike the industrial parts, which have a copper lead frame). The KOVAR material is necessary to attain the hermetic seal required in military applications.

The KOVAR lead frame does not conduct heat as well as copper, which means that the PC board copper can not be used to significantly reduce the overall junction-to-ambient thermal resistance in applications using the LP2953AMJ part.

The power dissipation calculations for military applications are done exactly the same as was detailed in the previous section, with one important exception: the value for $\theta_{(J-A)}$, the junction-to-ambient thermal resistance, is fixed at 95°C/W and can not be changed by adding copper foil patterns to the PC board. This leads to an important fact: The *maximum allowable power dissipation in any application using the LP2953AMJ is dependent only on the ambient temperature:*

$$P(max) = T_{R(max)} / \theta_{(J-A)}$$

$$P(max) = \frac{T_{J(max)} - T_{A(max)}}{\theta_{(J-A)}}$$

$$P(max) = \frac{150 - T_{A(max)}}{95}$$

Figure 3 shows a graph of maximum allowable power dissipation vs. ambient temperature for the LP2953AMJ, made using the 95°C/W value for $\theta_{(J-A)}$ and assuming a maximum junction temperature of 150°C (caution: the *maximum* ambient temperature which will be reached in a given application must always be used to calculate maximum allowable power dissipation).

EXTERNAL CAPACITORS

A 2.2 μF (or greater) capacitor is required between the output pin and ground to assure stability when the output is set to 5V. Without this capacitor, the part will oscillate. Most type of tantalum or aluminum electrolytics will work here. Film types will work, but are more expensive. Many aluminum electrolytics contain electrolytes which freeze at −30°C, which requires the use of solid tantalums below −25°C. The important parameters of the capacitor are an ESR of about 5Ω or less and a resonant frequency above 500 kHz (the ESR may increase by a factor of **20** or **30** as the temperature is reduced from 25°C to −30°C). The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.68 μF for currents below 10 mA or 0.22 μF for currents below 1 mA.

Programming the output for voltages below 5V runs the error amplifier at lower gains requiring *more* output capacitance for stability. At 3.3V output, a minimum of 4.7 μF is required. For the worst-case condition of 1.23V output and 250 mA of load current, a 6.8 μF (or larger) capacitor should be used.

A 1 μF capacitor should be placed from the input pin to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery input is used.

Stray capacitance to the Feedback terminal can cause instability. This problem is most likely to appear when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitance to 6.8 μF (or greater) will cure the problem.

MINIMUM LOAD

When setting the output voltage using an external resistive divider, a minimum current of 1 μA is recommended through the resistors to provide a minimum load.

It should be noted that a minimum load current is specified in several of the electrical characteristic test conditions, so this value must be used to obtain correlation on these tested limits.

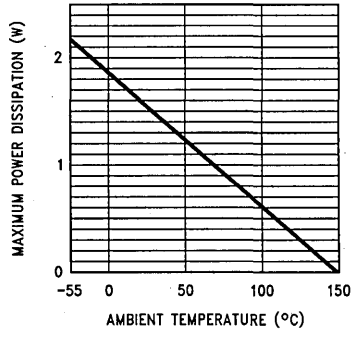

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FIGURE 3. Power Derating Curve for LP2953AMJ

Application Hints (Continued)

PROGRAMMING THE OUTPUT VOLTAGE

The regulator may be pin-strapped for 5V operation using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and 5V Tap pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see *Figure 4*). The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) + (I_{FB} \times R1)$$

where V_{REF} is the 1.23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 1 μA sets an upper limit of 1.2 MΩ on the value of R2 in cases where the regulator must work with no load (see **MINIMUM LOAD**). I_{FB} will produce a typical 2% error in V_{OUT} which can be eliminated at room temperature by trimming R1. For better accuracy, choosing R2 = 100 kΩ will reduce this error to 0.17% while increasing the resistor program current to 12 μA. Since the typical quiescent current is 120 μA, this added current is negligible.

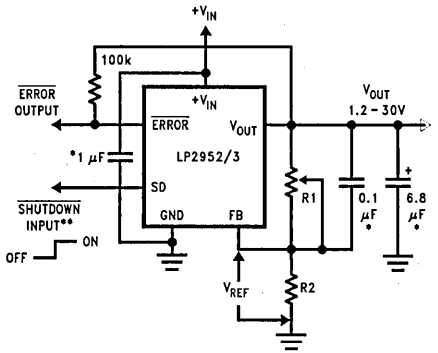

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FIGURE 4. Adjustable Regulator

*See Application Hints

**Drive with TTL-low to shut down

DROPOUT VOLTAGE

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

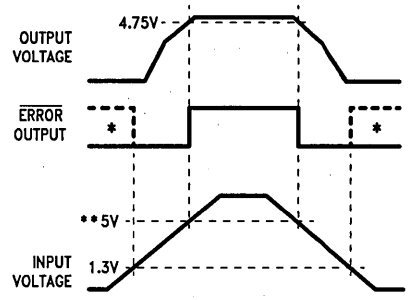
DROPOUT DETECTION COMPARATOR

This comparator produces a logic "LOW" whenever the output falls out of regulation by more than about 5%. This figure results from the comparator's built-in offset of 60 mV divided by the 1.23V reference (refer to block diagrams on page 1). The 5% low trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

Figure 5 gives a timing diagram showing the relationship between the output voltage, the $\overline{\text{ERROR}}$ output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output. The $\overline{\text{ERROR}}$ signal becomes low at about 1.3V input. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the **input** voltage trip points will vary with load current. The **output** voltage trip point does not vary.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the regulator output or some other supply voltage. Using the regulator output prevents an invalid "HIGH" on the comparator output which occurs if it is pulled up to an external voltage while the regulator input voltage is reduced below 1.3V. In selecting a value for the pull-up resistor, note that while the output can sink 400 μA, this current adds to battery drain. Suggested values range from 100 kΩ to 1 MΩ. This resistor is not required if the output is unused.

When $V_{IN} \leq 1.3V$, the error flag pin becomes a high impedance, allowing the error flag voltage to rise to its pull-up voltage. Using V_{OUT} as the pull-up voltage (rather than an external 5V source) will keep the error flag voltage below 1.2V (typical) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.



TL/H/11127–10

FIGURE 5. $\overline{\text{ERROR}}$ Output Timing

*In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, pull up to regulator output.

**Exact value depends on dropout voltage. (See Application Hints)

OUTPUT ISOLATION

The regulator output can be left connected to an active voltage source (such as a battery) with the regulator input power shut off, **as long as the regulator ground pin is connected to ground.** If the ground pin is left floating, **damage to the regulator can occur** if the output is pulled up by an external voltage source.

Application Hints (Continued)

REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to *Figure 4*). The formula for selecting the capacitor to be used is:

$$C_B = \frac{1}{2\pi\ R1 \times 20\ Hz}$$

This gives a value of about 0.1 μF. When this is used, the output capacitor must be 6.8 μF (or greater) to maintain stability. The 0.1 μF capacitor reduces the high frequency gain of the circuit to unity, lowering the output noise from 260 μV to 80 μV using a 10 Hz to 100 kHz bandwidth. Also, noise is no longer proportional to the output voltage, so improvements are more pronounced at high output voltages.

AUXILIARY COMPARATOR (LP2953 only)

The LP2953 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

SHUTDOWN INPUT

A logic-level signal will shut off the regulator output when a "LOW" (<1.2V) is applied to the $\overline{\text{Shutdown}}$ input.

To prevent possible mis-operation, the $\overline{\text{Shutdown}}$ input must be actively terminated. If the input is driven from open-collector logic, a pull-up resistor (20 kΩ to 100 kΩ recommended) should be connected from the $\overline{\text{Shutdown}}$ input to the regulator input.

If the $\overline{\text{Shutdown}}$ input is driven from a source that actively pulls high and low (like an op-amp), the pull-up resistor is not required, but may be used.

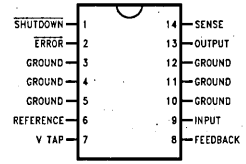
If the shutdown function is not to be used, the cost of the pull-up resistor can be saved by simply tying the $\overline{\text{Shutdown}}$ input directly to the regulator input.

IMPORTANT: Since the Absolute Maximum Ratings state that the $\overline{\text{Shutdown}}$ input can not go more than 0.3V below ground, the reverse-battery protection feature which protects the regulator input is sacrificed if the $\overline{\text{Shutdown}}$ input is tied directly to the regulator input.

If reverse-battery protection is required in an application, *the pull-up resistor between the $\overline{\text{Shutdown}}$ input and the regulator input must be used.*

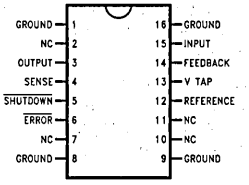
Pinout Drawings

LP2952 14-Pin DIP



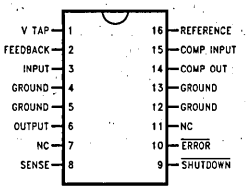
TL/H/11127–11

LP2952 16-Pin SO



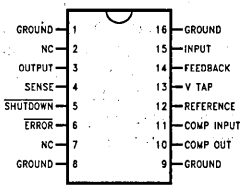
TL/H/11127–12

LP2953 16-Pin DIP



TL/H/11127–13

LP2953 16-Pin SO



TL/H/11127–14

Ordering Information

LP2952

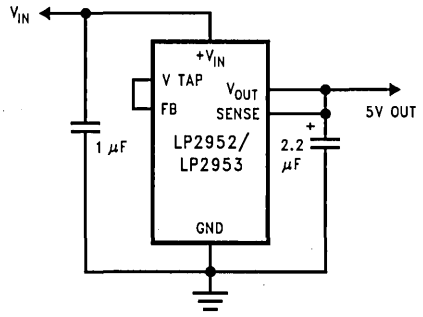
Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2952IN, LP2952AIN, LP2952IN-3.3, LP2952AIN-3.3	−40 to +125	14-Pin Molded DIP	N14A
LP2952IM, LP2952AIM, LP2952IM-3.3, LP2952AIM-3.3	−40 to +125	16-Pin Surface Mount	M16A

LP2953

Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2953IN, LP2953AIN, LP2953IN-3.3, LP2953AIN-3.3	−40 to +125	16-Pin Molded DIP	N16A
LP2953IM, LP2953AIM, LP2953IM-3.3, LP2953AIM-3.3	−40 to +125	16-Pin Surface Mount	M16A
LP2953AMJ/883	−55 to +150	16-Pin Ceramic DIP	J16A

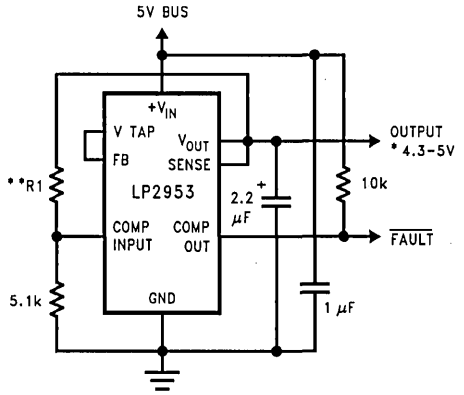
Typical Applications

Basic 5V Regulator



TL/H/11127–15

5V Current Limiter with Load Fault Indicator

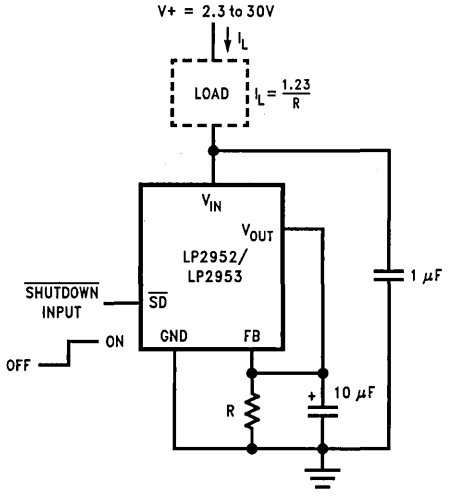


TL/H/11127–16

*Output voltage equals $+V_{IN}$ minum dropout voltage, which varies with output current. Current limits at a maximum of 380 mA (typical).

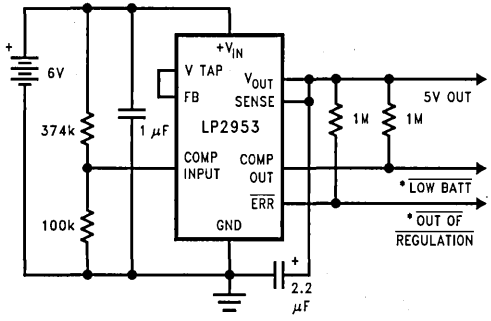
**Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

Low T.C. Current Sink



TL/H/11127–17

5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION



TL/H/11127–18

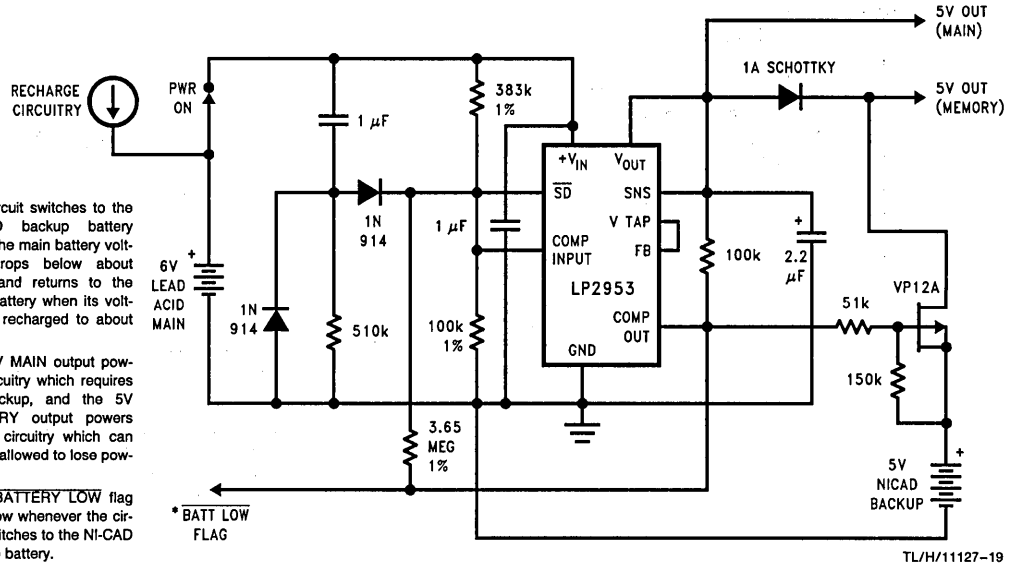
*Connect to Logic or μP control inputs.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power down some hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

Typical Applications (Continued)

5V Battery Powered Supply with Backup and Low Battery Flag



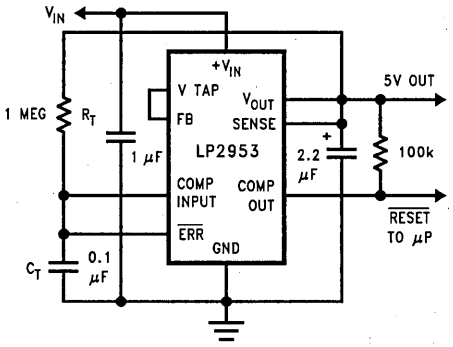
The circuit switches to the NI-CAD backup battery when the main battery voltage drops below about 5.6V, and returns to the main battery when its voltage is recharged to about 6V.

The 5V MAIN output powers circuitry which requires no backup, and the 5V MEMORY output powers critical circuitry which can not be allowed to lose power.

*The $\overline{\text{BATTERY LOW}}$ flag goes low whenever the circuit switches to the NI-CAD backup battery.

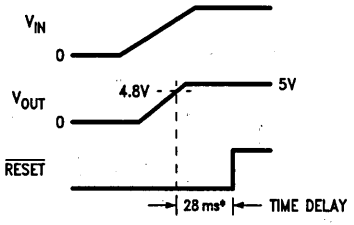
TL/H/11127–19

5V Regulator with Timed Power-On Reset



TL/H/11127–20

Timing Diagram for Timed Power-On Reset

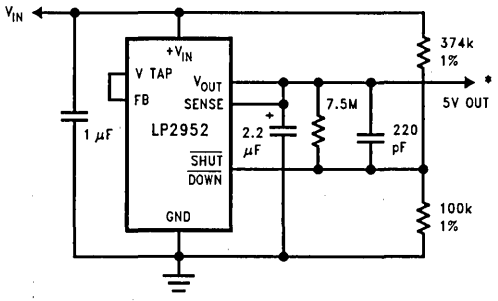


TL/H/11127–21

*R_T = 1 MEG, C_T = 0.1 μF

Typical Applications (Continued)

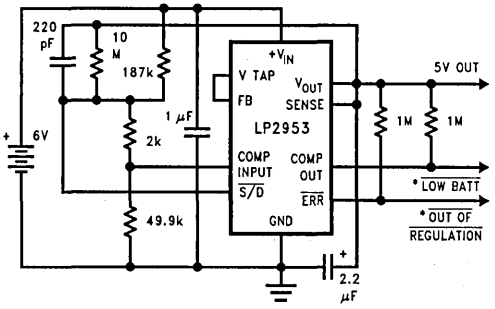
5V Regulator with Snap-On/Snap-Off Feature and Hysteresis



TL/H/11127–22

*Turns ON at V_{IN} = 5.87V
Turns OFF at V_{IN} = 5.64V
(for component values shown)

5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION with SNAP-ON/SNAP-OFF Output



TL/H/11127–23

*Connect to Logic or μP control inputs.

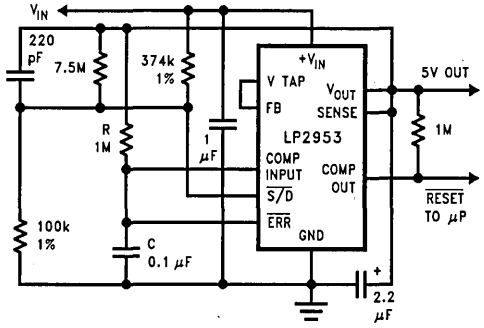
OUTPUT has SNAP-ON/SNAP-OFF feature.

LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or shut down hardware with high power requirements. The output is still in regulation at this time.

OUT OF REGULATION flag goes low if the output goes below about 4.7V, which could occur from a load fault.

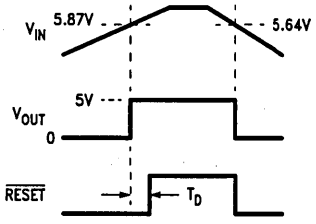
OUTPUT has SNAP-ON/SNAP-OFF feature. Regulator snaps ON at about 5.7V input, and OFF at about 5.6V.

5V Regulator with Timed Power-On Reset, Snap-On/Snap-Off Feature and Hysteresis



TL/H/11127–24

Timing Diagram



TL/H/11127–25

Td = (0.28) RC = 28 ms for components shown.

National Semiconductor

LM2574/LM2574HV Series
SIMPLE SWITCHER™ 0.5A Step-Down Voltage Regulator

General Description

The LM2574 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, 15V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2574 series offers a high-efficiency replacement for popular three-terminal linear regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors optimized for use with the LM2574 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring 50 μA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

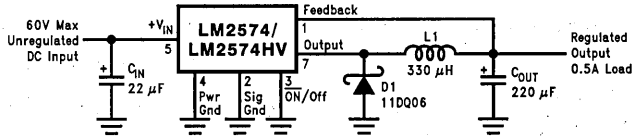
Features

- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Adjustable version output voltage range, 1.23V to 37V (57V for HV version) ±4% max over line and load conditions
- Guaranteed 0.5A output current
- Wide input voltage range, 40V, up to 60V for HV version
- Requires only 4 external components
- 52 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (Buck-Boost)

Typical Application (Fixed Output Voltage Versions)

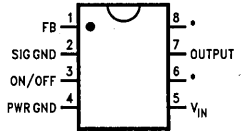


TL/H/11394–1

Note: Pin numbers are for 8-pin DIP package.

Connection Diagrams

8-Lead DIP (N)



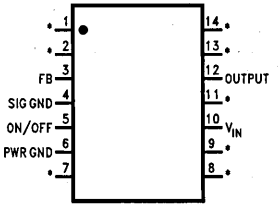
Top View

*No internal connection, but should be soldered to PC board for best heat transfer.

TL/H/11394–2

Order Number LM2574-3.3HVN, LM2574HVN-5.0, LM2574HVN-12, LM2574HVN-15, LM2574HVN-ADJ, LM2574N-3.3, LM2574N-5.0, LM2574N-12, LM2574N-15 or LM2574N-ADJ
See NS Package Number N08A

14-Lead Wide Surface Mount (WM)



Top View

TL/H/11394–3

Order Number LM2574HVM-3.3, LM2574HVM-5.0, LM2574HVM-12, LM2574HVM-15, LM2574HVM-ADJ, LM2574M-3.3 LM2574M-5.0, LM2574M-12, LM2574M-15 or LM2574M-ADJ
See NS Package Number M14B

Patent Pending

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage	
LM2574	45V
LM2574HV	63V
$\overline{ON}$/OFF Pin Input Voltage	$-0.3V \le V \le +V_{IN}$
Output Voltage to Ground (Steady State)	−1V
Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Minimum ESD Rating (C = 100 pF, R = 1.5 kΩ)	2 kV
Lead Temperature (Soldering, 10 seconds)	260°C
Maximum Junction Temperature	150°C

Operating Ratings

Temperature Range	
LM2574/LM2574HV	$-40°C \le T_J \le +125°C$
Supply Voltage	
LM2574	40V
LM2574HV	60V

LM2574-3.3, LM2574HV-3.3

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.**

Symbol	Parameter	Conditions	LM2574-3.3 LM2574HV-3.3		Units (Limits)
			Typ	Limit (Note 2)	
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{LOAD} = 100 mA	3.3	3.234 3.366	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574	4.75V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A	3.3	3.168/**3.135** 3.432/**3.465**	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574HV	4.75V ≤ V_{IN} ≤ 60V, 0.1A ≤ I_{LOAD} ≤ 0.5A	3.3	3.168/**3.135** 3.450/**3.482**	V(Min) V(Max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	72		%

LM2574-5.0, LM2574HV-5.0

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.**

Symbol	Parameter	Conditions	LM2574-5.0 LM2574HV-5.0		Units (Limits)
			Typ	Limit (Note 2)	
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{LOAD} = 100 mA	5	4.900 5.100	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574	7V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A	5	4.800/**4.750** 5.200/**5.250**	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574HV	7V ≤ V_{IN} ≤ 60V, 0.1A ≤ I_{LOAD} ≤ 0.5A	5	4.800/**4.750** 5.225/**5.275**	V(Min) V(Max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	77		%

LM2574-12, LM2574HV-12

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.**

Symbol	Parameter	Conditions	LM2574-12 LM2574HV-12		Units (Limits)
			Typ	Limit (Note 2)	
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	V_{IN} = 25V, I_{LOAD} = 100 mA	10	 11.76 12.24	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574	15V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A	12	 11.52/**11.40** 12.48/**12.60**	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574HV	15V ≤ V_{IN} ≤ 60V, 0.1A ≤ I_{LOAD} ≤ 0.5A	12	 11.52/**11.40** 12.54/**12.66**	 V(Min) V(Max)
η	Efficiency	V_{IN} = 15V, I_{LOAD} = 0.5A	88		%

LM2574-15, LM2574HV-15

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.**

Symbol	Parameter	Conditions	LM2574-15 LM2574HV-15		Units (Limits)
			Typ	Limit (Note 2)	
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	V_{IN} = 30V, I_{LOAD} = 100 mA	15	 14.70 15.30	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574	18V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A	15	 14.40/**14.25** 15.60/**15.75**	V V(Min) V(Max)
V_{OUT}	Output Voltage LM2574HV	18V ≤ V_{IN} ≤ 60V, 0.1A ≤ I_{LOAD} ≤ 0.5A	15	 14.40/**14.25** 15.68/**15.83**	 V(Min) V(Max)
η	Efficiency	V_{IN} = 18V, I_{LOAD} = 0.5A	88		%

LM2574-ADJ, LM2574HV-ADJ

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V, I_{LOAD} = 100 mA.

Symbol	Parameter	Conditions	LM2574-ADJ LM2574HV-ADJ		Units (Limits)
			Typ	Limit (Note 2)	
SYSTEM PARAMETERS (Note 3) Test Circuit *Figure 2*					
V_{FB}	Feedback Voltage	V_{IN} = 12V, I_{LOAD} = 100 mA	1.230	 1.217 1.243	V V(Min) V(Max)
V_{FB}	Feedback Voltage LM2574	7V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A V_{OUT} Programmed for 5V. Circuit of *Figure 2*	1.230	 1.193/**1.180** 1.267/**1.280**	V V(Min) V(Max)
V_{FB}	Feedback Voltage LM2574HV	7V ≤ V_{IN} ≤ 60V, 0.1A ≤ I_{LOAD} ≤ 0.5A V_{OUT} Programmed for 5V. Circuit of *Figure 2*	1.230	 1.193/**1.180** 1.273/**1.286**	 V(Min) V(Max)
η	Efficiency	V_{IN} = 12V, V_{OUT} = 5V, I_{LOAD} = 0.5A	77		%

All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V for the 3.3V, 5V, and Adjustable version, V_{IN} = 25V for the 12V version, and V_{IN} = 30V for the 15V version. I_{LOAD} = 100 mA.

Symbol	Parameter	Conditions	LM2574-XX LM2574HV-XX		Units (Limits)
			Typ	Limit (Note 2)	
DEVICE PARAMETERS					
I_b	Feedback Bias Current	Adjustable Version Only, V_{OUT} = 5V	50	100/**500**	nA
f_O	Oscillator Frequency	(see Note 10)	52	 47/**42** 58/**63**	kHz kHz(Min) kHz(Max)
V_{SAT}	Saturation Voltage	I_{OUT} = 0.5A (Note 4)	0.9	 1.2/**1.4**	V V(max)
DC	Max Duty Cycle (ON)	(Note 5)	98	 93	% %(Min)
I_{CL}	Current Limit	Peak Current, (Notes 4, 10)	1.0	 0.7/**0.65** 1.6/**1.8**	A A(Min) A(Max)
I_L	Output Leakage Current	(Notes 6, 7) Output = 0V Output = −1V Output = −1V	 7.5	2 30	mA(Max) mA mA(Max)
I_Q	Quiescent Current	(Note 6)	5	 10	mA mA(Max)
I_{STBY}	Standby Quiescent Current	$\overline{ON}$/OFF Pin= 5V (OFF)	50	 200	μA μA(Max)
θ_{JA} θ_{JA} θ_{JA} θ_{JA}	Thermal Resistance	N Package, Junction to Ambient (Note 8) N Package, Junction to Ambient (Note 9) M Package, Junction to Ambient (Note 8) M Package, Junction to Ambient (Note 9)	92 72 102 78		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 2*					
V_{IH}	$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V	1.4	2.2/**2.4**	V(Min)
V_{IL}		V_{OUT} = Nominal Output Voltage	1.2	1.0/**0.8**	V(Max)
I_H	$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF)	12	 30	μA μA(Max)
I_{IL}		$\overline{ON}$/OFF Pin = 0V (ON)	0	 10	μA μA(Max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (Standard type face) and at **temperature extremes (bold type face).** All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level.

Note 3: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2574 is used as shown in the *Figure 2* test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.

Note 4: Output pin sourcing current. No diode, inductor or capacitor connected to output pin.

Note 5: Feedback pin removed from output and connected to 0V.

Note 6: Feedback pin removed from output and connected to +12V for the Adjustable, 3.3V, and 5V versions, and +25V for the 12V and 15V versions, to force the output transistor OFF.

Note 7: V_{IN} = 40V (60V for high voltage version).

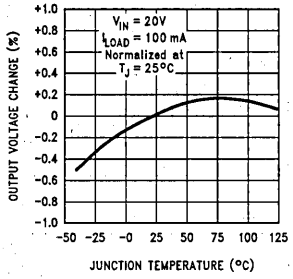
Note 8: Junction to ambient thermal resistance with approximately 1 square inch of printed circuit board copper surrounding the leads. Additional copper area will lower thermal resistance further. See application hints in this data sheet and the thermal model in ***Switchers Made Simple*** software.

Note 9: Junction to ambient thermal resistance with approximately 4 square inches of 1 oz. (0.0014 in. thick) printed circuit board copper surrounding the leads. Additional copper area will lower thermal resistance further. (See Note 8.)

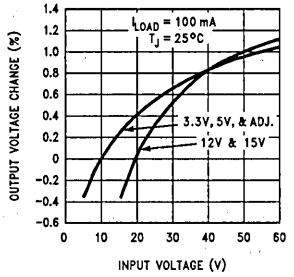
Note 10: The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.

Typical Performance Characteristics (Circuit of *Figure 2*)

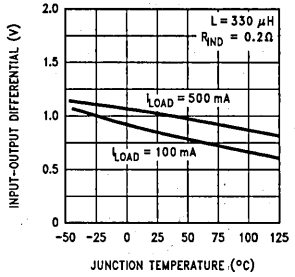
Normalized Output Voltage



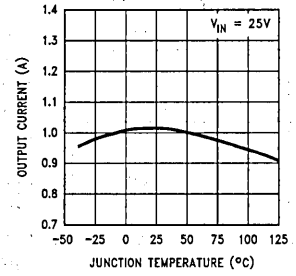
Line Regulation



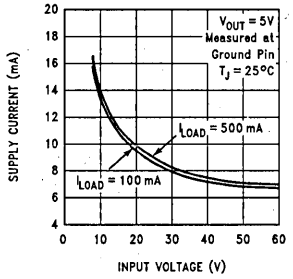
Dropout Voltage



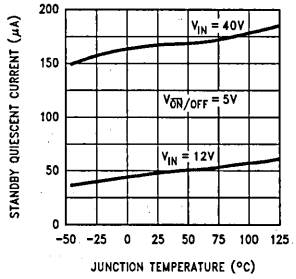
Current Limit



Supply Current



Standby Quiescent Current



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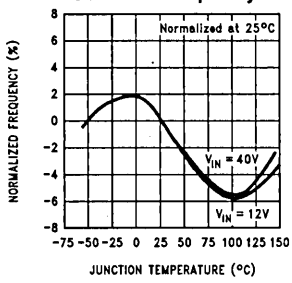
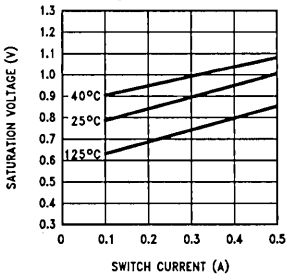
Typical Performance Characteristics (Circuit of *Figure 2*) (Continued)

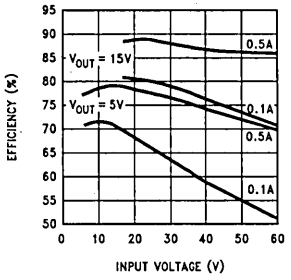
Oscillator Frequency



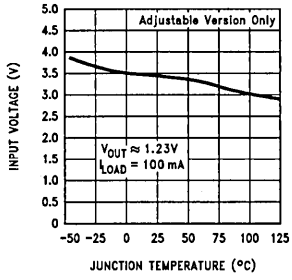
Switch Saturation Voltage



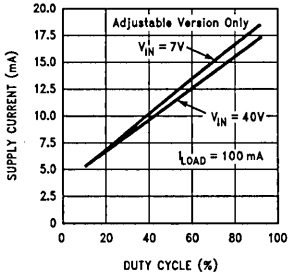
Efficiency



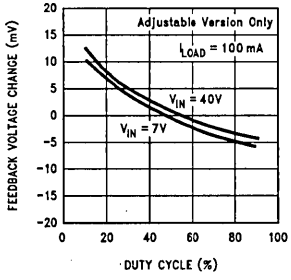
Minimum Operating Voltage



Supply Current vs Duty Cycle



Feedback Voltage vs Duty Cycle



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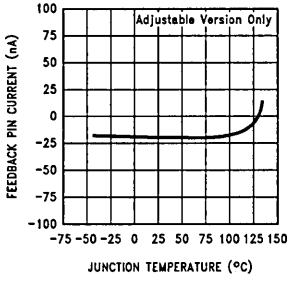
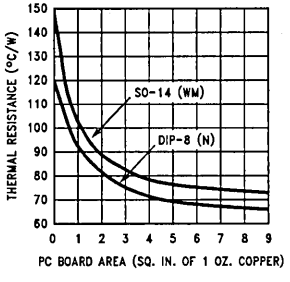
Feedback Pin Current



Junction to Ambient Thermal Resistance



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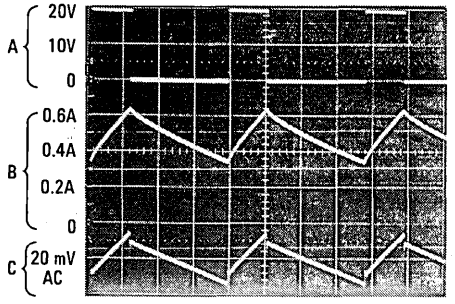
Typical Performance Characteristics (Circuit of *Figure 2*) (Continued)

Continuous Mode Switching Waveforms
V_{OUT} = 5V, 500 mA Load Current, L = 330 μH



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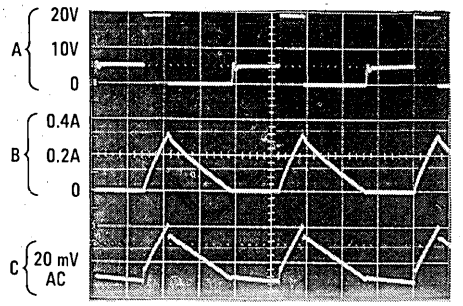
A: Output Pin Voltage, 10V/div
B: Inductor Current, 0.2 A/div
C: Output Ripple Voltage, 20 mV/div, AC-Coupled
Horizontal Time Base: 5μs/div

Discontinuous Mode Switching Waveforms
V_{OUT} = 5V, 100 mA Load Current, L = 100 μH



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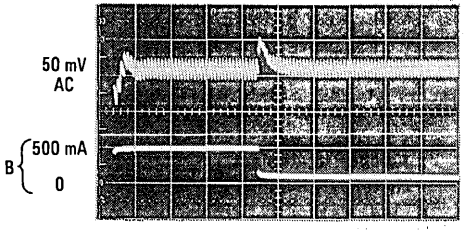
A: Output Pin Voltage, 10V/div
B: Inductor Current, 0.2 A/div
C: Output Ripple Voltage, 20 mV/div, AC-Coupled
Horizontal Time Base: 5 μs/div

500 mA Load Transient Response for Continuous Mode Operation, L = 330 μH, C_{OUT} = 300 μF



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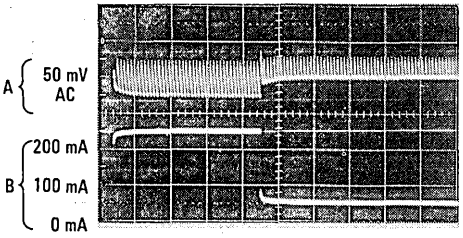
A: Output Voltage, 50 mV/div. AC Coupled
B: 100 mA to 500 mA Load Pulse
Horizontal Time Base: 200 μs/div

250 mA Load Transient Response for Discontinuous Mode Operation. L = 68 μH, C_{OUT} = 470 μF



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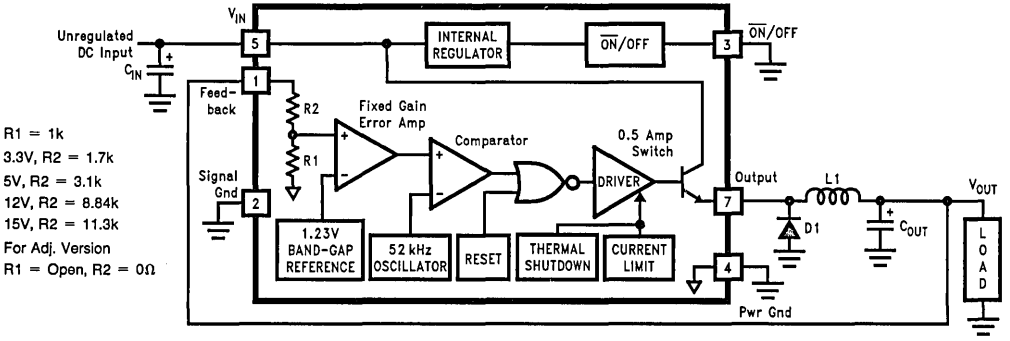
A: Output Voltage, 50 mV/div. AC Coupled
B: 50 mA to 250 mA Load Pulse
Horizontal Time Base: 200 μs/div

Block Diagram



R1 = 1k
3.3V, R2 = 1.7k
5V, R2 = 3.1k
12V, R2 = 8.84k
15V, R2 = 11.3k
For Adj. Version
R1 = Open, R2 = 0Ω

Note: Pin numbers are for the 8-pin DIP package.

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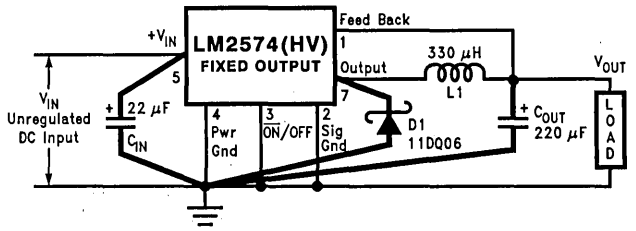
FIGURE 1

Test Circuit and Layout Guidelines

Fixed Output Voltage Versions



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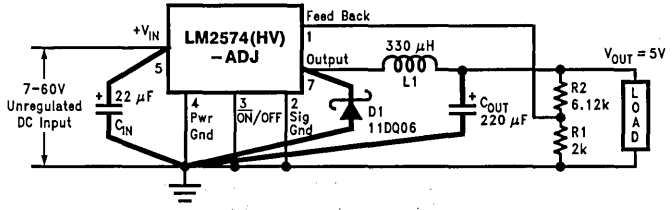
C_{IN}— 22 µF, 75V Aluminum Electrolytic
C_{OUT}— 220 µF, 25V Aluminum Electrolytic
D1— Schottky, 11DQ06
L1— 330 µH, 52627 (for 5V in, 3.3V out, use 100 µH, RL-1284-100)
R1— 2k, 0.1%
R2— 6.12k, 0.1%

Adjustable Output Voltage Version



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$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$$

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} = 1.23V, R1 between 1k & 5k.

FIGURE 2

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, the length of the leads indicated by **heavy lines should be kept as short as possible**. Single-point grounding (as indicated) or ground plane construction should be used for best results. When using the Adjustable version, physically locate the programming resistors near the regulator, to keep the sensitive feedback wiring short.

Inductor Value	Pulse Eng. (Note 1)	Renco (Note 2)	NPI (Note 3)
68 µH	*	RL-1284-68	NP5915
100 µH	*	RL-1284-100	NP5916
150 µH	52625	RL-1284-150	NP5917
220 µH	52626	RL-1284-220	NP5918/5919
330 µH	52627	RL-1284-330	NP5920/5921
470 µH	52628	RL-1284-470	NP5922
680 µH	52629	RL-1283-680	NP5923
1000 µH	52631	RL-1283-1000	*
1500 µH	*	RL-1283-1500	*
2200 µH	*	RL-1283-2200	*

FIGURE 3. Inductor Selection by Manufacturer's Part Number

U.S. Source

Note 1: Pulse Engineering, (619) 674-8100
P.O. Box 12236, San Diego, CA 92112

Note 2: Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

*Contact Manufacturer

European Source

Note 3: NPI/APC +44 (0) 634 290588
47 Riverside, Medway City Estate
Strood, Rochester, Kent ME2 4DP. UK

*Contact Manufacturer

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LM2574 Series Buck Regulator Design Procedure

PROCEDURE (Fixed Output Voltage Versions)	EXAMPLE (Fixed Output Voltage Versions)
Given: V_{OUT} = Regulated Output Voltage (3.3V, 5V, 12V, or 15V) V_{IN}(Max) = Maximum Input Voltage I_{LOAD}(Max) = Maximum Load Current	**Given:** V_{OUT} = 5V V_{IN}(Max) = 15V I_{LOAD}(Max) = 0.4A
1. Inductor Selection (L1) **A.** Select the correct Inductor value selection guide from *Figures 4, 5, 6* or *7*. (Output voltages of 3.3V, 5V, 12V or 15V respectively). For other output voltages, see the design procedure for the adjustable version. **B.** From the inductor value selection guide, identify the inductance region intersected by V_{IN}(Max) and I_{LOAD}(Max). **C.** Select an appropriate inductor from the table shown in *Figure 3*. Part numbers are listed for three inductor manufacturers. The inductor chosen must be rated for operation at the LM2574 switching frequency (52 kHz) and for a current rating of 1.5 × I_{LOAD}. For additional inductor information, see the inductor section in the Application Hints section of this data sheet.	**1. Inductor Selection (L1)** **A.** Use the selection guide shown in *Figure 5*. **B.** From the selection guide, the inductance area intersected by the 15V line and 0.4A line is 330. **C.** Inductor value required is 330 μH. From the table in *Figure 3*, choose Pulse Engineering PE-52627, Renco RL-1284-330, or NPI NP5920/5921.
2. Output Capacitor Selection (C_{OUT}) **A.** The value of the output capacitor together with the inductor defines the dominate pole-pair of the switching regulator loop. For stable operation and an acceptable output ripple voltage, (approximately 1% of the output voltage) a value between 100 μF and 470 μF is recommended. **B.** The capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5V regulator, a rating of at least 8V is appropriate, and a 10V or 15V rating is recommended. Higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason it may be necessary to select a capacitor rated for a higher voltage than would normally be needed.	**2. Output Capacitor Selection (C_{OUT})** **A.** C_{OUT} = 100 μF to 470 μF standard aluminum electrolytic. **B.** Capacitor voltage rating = 20V.
3. Catch Diode Selection (D1) **A.** The catch-diode current rating must be at least 1.5 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2574. The most stressful condition for this diode is an overload or shorted output condition. **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example, a 1A current rating is adequate. **B.** Use a 20V 1N5817 or SR102 Schottky diode, or any of the suggested fast-recovery diodes shown in *Figure 9*.
4. Input Capacitor (C_{IN}) An aluminum or tantalum electrolytic bypass capacitor located close to the regulator is needed for stable operation.	**4. Input Capacitor (C_{IN})** A 22 μF aluminum electrolytic capacitor located near the input and ground pins provides sufficient bypassing.

LM2574 Series Buck Regulator Design Procedure (Continued)

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)

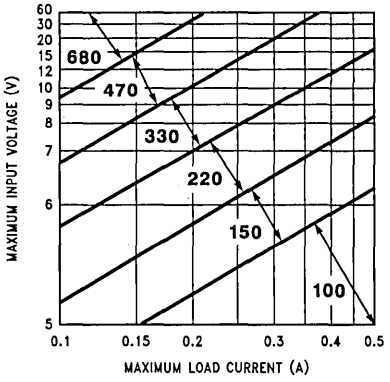

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FIGURE 4. LM2574HV-3.3 Inductor Selection Guide

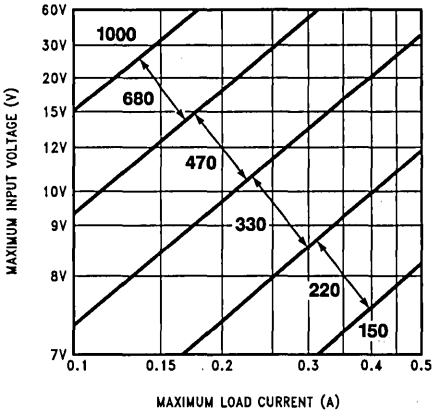

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FIGURE 5. LM2574HV-5.0 Inductor Selection Guide

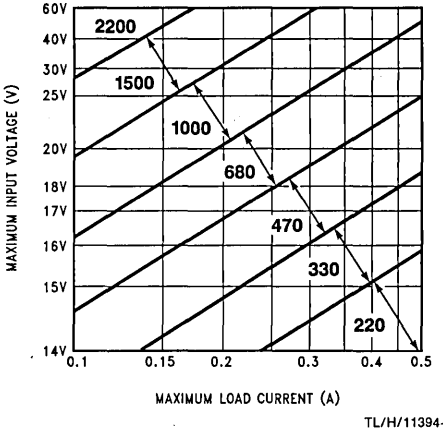

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FIGURE 6. LM2574HV-12 Inductor Selection Guide

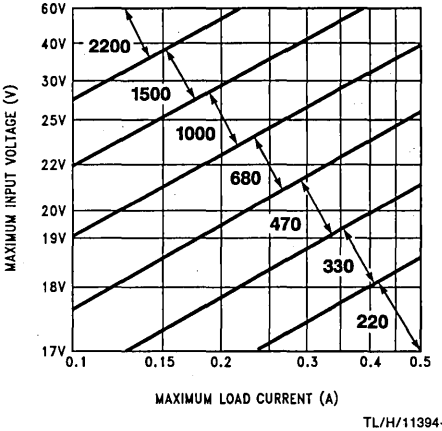

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FIGURE 7. LM2574HV-15 Inductor Selection Guide

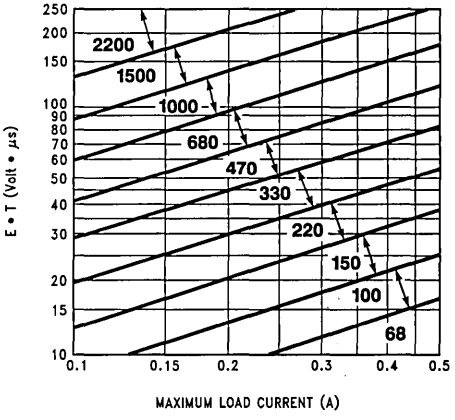

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FIGURE 8. LM2574HV-ADJ Inductor Selection Guide

LM2574 Series Buck Regulator Design Procedure (Continued)

PROCEDURE (Adjustable Output Voltage Versions)	EXAMPLE (Adjustable Output Voltage Versions)
Given: V_{OUT} = Regulated Output Voltage V_{IN}(Max) = Maximum Input Voltage I_{LOAD}(Max) = Maximum Load Current F = Switching Frequency *(Fixed at 52 kHz)*	**Given:** V_{OUT} = 24V V_{IN}(Max) = 40V I_{LOAD}(Max) = 0.4A F = 52 kHz
1. Programming Output Voltage *(Selecting R1 and R2, as shown in Figure 2)* Use the following formula to select the appropriate resistor values. $V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$ where V_{REF} = 1.23V R_1 can be between 1k and 5k. *(For best temperature coefficient and stability with time, use 1% metal film resistors)* $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$	**1. Programming Output Voltage** *(Selecting R1 and R2)* $V_{OUT} = 1.23\left(1 + \frac{R_2}{R_1}\right)$ Select R1 = 1k $R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{24V}{1.23V} - 1\right)$ R_2 = 1k (19.51 − 1) = 18.51k, closest 1% value is 18.7k
2. Inductor Selection (L1) **A.** Calculate the inductor Volt • microsecond constant, E • T (V • μs), from the following formula: $E \bullet T = (V_{IN} - V_{OUT})\frac{V_{OUT}}{V_{IN}} \bullet \frac{1000}{F\ (in\ kHz)}$ (V • μs) **B.** Use the E • T value from the previous formula and match it with the E • T number on the vertical axis of the **Inductor Value Selection Guide** shown in *Figure 8*. **C.** On the horizontal axis, select the maximum load current. **D.** Identify the inductance region intersected by the E • T value and the maximum load current value, and note the inductor value for that region. **E.** Select an appropriate inductor from the table shown in *Figure 3*. Part numbers are listed for three inductor manufacturers. The inductor chosen must be rated for operation at the LM2574 switching frequency (52 kHz) and for a current rating of 1.5 × I_{LOAD}. For additional inductor information, see the inductor section in the application hints section of this data sheet.	**2. Inductor Selection (L1)** **A.** Calculate E • T (V • μs) $E \bullet T = (40 - 24) \bullet \frac{24}{40} \bullet \frac{1000}{52} = 185\ V \bullet \mu s$ **B.** E • T = 185 V • μs **C.** I_{LOAD}(Max) = 0.4A **D.** Inductance Region = 1000 **E.** Inductor Value = 1000 μH *Choose from **Pulse Engineering** Part #PE-52631, or **Renco** Part #RL-1283-1000.*
3. Output Capacitor Selection (C_{OUT}) **A.** The value of the output capacitor together with the inductor defines the dominate pole-pair of the switching regulator loop. For stable operation, the capacitor must satisfy the following requirement: $C_{OUT} \geq 13{,}300\frac{V_{IN}(Max)}{V_{OUT} \bullet L(\mu H)}$ (μF) The above formula yields capacitor values between 5 μF and 1000 μF that will satisfy the loop requirements for stable operation. But to achieve an acceptable output ripple voltage, (approximately 1% of the output voltage) and transient response, the output capacitor may need to be several times larger than the above formula yields. **B.** The capacitor's voltage rating should be at last 1.5 times greater than the output voltage. For a 24V regulator, a rating of at least 35V is recommended. Higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reasion it may be necessary to select a capacitor rate for a higher voltage than would normally be needed.	**3. Output Capacitor Selection (C_{OUT})** **A.** $C_{OUT} > 13{,}300\frac{40}{24 \bullet 1000} = 22.2\ \mu F$ However, for acceptable output ripple voltage select $C_{OUT} \geq 100\ \mu F$ C_{OUT} = 100 μF electrolytic capacitor

LM2574 Series Buck Regulator Design Procedure (Continued)

PROCEDURE (Adjustable Output Voltage Versions)	EXAMPLE (Adjustable Output Voltage Versions)
4. Catch Diode Selection (D1) **A.** The catch-diode current rating must be at least 1.5 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2574. The most stressful condition for this diode is an overload or shorted output condition. Suitable diodes are shown in the selection guide of *Figure 9*. **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**4. Catch Diode Selection (D1)** **A.** For this example, a 1A current rating is adequate. **B.** Use a 50V MBR150 or 11DQ05 Schottky diode, or any of the suggested fast-recovery diodes in *Figure 9*.
5. Input Capacitor (C_{IN}) An aluminum or tantalum electrolytic bypass capacitor located close to the regulator is needed for stable operation.	**5. Input Capacitor (C_{IN})** A 22 μF aluminum electrolytic capacitor located near the input and ground pins provides sufficient bypassing.

V_R	1 Amp Diodes	
	Schottky	Fast Recovery
20V	1N5817 SR102 MBR120P	The following diodes are all rated to 100V 11DF1 10JF1 MUR110 HER102
30V	1N5818 SR103 11DQ03 MBR130P 10JQ030	
40V	1N5819 SR104 11DQ04 11JQ04 MBR140P	
50V	MBR150 SR105 11DQ05 11JQ05	
60V	MBR160 SR106 11DQ06 11JQ06	
90V	11DQ09	

FIGURE 9. Diode Selection Guide

To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher line of switching regulators. ***Switchers Made Simple*** *(version 3.3) is available on a (3½") diskette for IBM compatible computers from a National Semiconductor sales office in your area.*

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Application Hints

INPUT CAPACITOR (C_{IN})

To maintain stability, the regulator input pin must be bypassed with at least a 22 μF electrolytic capacitor. The capacitor's leads must be kept short, and located near the regulator.

If the operating temperature range includes temperatures below −25°C, the input capacitor value may need to be larger. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures and age. Paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures. For maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be greater than

$$1.2 \times \left(\frac{t_{ON}}{T}\right) \times I_{LOAD}$$

where $\frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$ for a buck regulator

and $\frac{t_{ON}}{T} = \frac{|V_{OUT}|}{|V_{OUT}| + V_{IN}}$ for a buck-boost regulator.

INDUCTOR SELECTION

All switching regulators have two basic modes of operation: continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements.

The LM2574 (or any of the Simple Switcher family) can be used for both continuous and discontinuous modes of operation.

In many cases the preferred mode of operation is in the continuous mode. It offers better load regulation, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require relatively large inductor values to keep the inductor current flowing continuously, especially at low output load currents.

To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see *Figures 4* through *8*). This guide assumes continuous mode operation, and selects an inductor that will allow a peak-to-peak inductor ripple current (ΔI_{IND}) to be a certain percentage of the maximum design load current. In the LM2574 SIMPLE SWITCHER, the peak-to-peak inductor ripple current percentage (of load current) is allowed to change as different design load currents are selected. By allowing the percentage of inductor ripple current to increase for lower current applications, the inductor size and value can be kept relatively low.

INDUCTOR RIPPLE CURRENT

When the switcher is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input voltage and output voltage, the peak-to-peak amplitude of this inductor current waveform remains constant. As the load current rises or falls, the entire sawtooth current waveform also rises or falls. The average DC value of this waveform is equal to the DC load current (in the buck regulator configuration).

If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will change to a discontinuous mode of operation. This is a perfectly acceptable mode of operation. Any buck switching regulator (no matter how large the inductor value is) will be forced to run discontinuous if the load current is light enough.

The curve shown in *Figure 10* illustrates how the peak-to-peak inductor ripple current (ΔI_{IND}) is allowed to change as different maximum load currents are selected, and also how it changes as the operating point varies from the upper border to the lower border within an inductance region (see Inductor Selection guides).

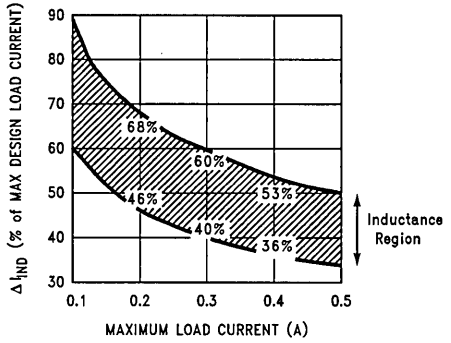

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FIGURE 10. Inductor Ripple Current (ΔI_{IND}) Range Based on Selection Guides from *Figures 4–8*.

Consider the following example:

V_{OUT} = 5V @ 0.4A

V_{IN} = 10V minimum up to 20V maximum

The selection guide in *Figure 5* shows that for a 0.4A load current, and an input voltage range between 10V and 20V, the inductance region selected by the guide is 330 μH. This value of inductance will allow a peak-to-peak inductor ripple current (ΔI_{IND}) to flow that will be a percentage of the maximum load current. For this inductor value, the ΔI_{IND} will also vary depending on the input voltage. As the input voltage increases to 20V, it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in *Figure 10*, it can be seen that at the 0.4A load current level, and operating near the upper border of the 330 μH inductance region, the ΔI_{IND} will be 53% of 0.4A, or 212 mA p-p.

This ΔI_{IND} is important because from this number the peak inductor current rating can be determined, the minimum load current required before the circuit goes to discontinuous operation, and also, knowing the ESR of the output capacitor, the output ripple voltage can be calculated, or conversely, measuring the output ripple voltage and knowing the ΔI_{IND}, the ESR can be calculated.

Application Hints (Continued)

From the previous example, the Peak-to-peak Inductor Ripple Current (ΔI_{IND}) = 212 mA p-p. Once the Δ_{IND} value is known, the following three formulas can be used to calculate additional information about the switching regulator circuit:

1. Peak Inductor or peak switch current

$$= \left(I_{LOAD} + \frac{\Delta I_{IND}}{2}\right) = \left(0.4A + \frac{212}{2}\right) = 506\ mA$$

2. Mimimum load current before the circuit becomes discontinuous

$$= \frac{\Delta I_{IND}}{2} = \frac{212}{2} = 106\ mA$$

3. Output Ripple Voltage = (ΔI_{IND}) × (ESR of C_{OUT})

The selection guide chooses inductor values suitable for continuous mode operation, but if the inductor value chosen is prohibitively high, the designer should investigate the possibility of discontinuous operation. The computer design software ***Switchers Made Simple*** will provide all component values for discontinuous (as well as continuous) mode of operation.

Inductors are available in different styles such as pot core, toroid, E-frame, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin core type, consists of wire wrapped on a ferrite rod core. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more electromagnetic interference (EMI). This EMI can cause problems in sensitive circuits, or can give incorrect scope readings because of induced voltages in the scope probe.

The inductors listed in the selection chart include powdered iron toroid for Pulse Engineering, and ferrite bobbin core for Renco.

An inductor should not be operated beyond its maximum rated current because it may saturate. When an inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the inductor current to rise very rapidly and will affect the energy storage capabilities of the inductor and could cause inductor overheating. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor. The inductor manufacturers' data sheets include current and energy limits to avoid inductor saturation.

OUTPUT CAPACITOR

An output capacitor is required to filter the output voltage and is needed for loop stability. The capacitor should be located near the LM2574 using short pc board traces. Standard aluminum electrolytics are usually adequate, but low ESR types are recommended for low output ripple voltage and good stability. The ESR of a capacitor depends on many factors, some which are: the value, the voltage rating, physical size and the type of construction. In general, low value or low voltage (less than 12V) electrolytic capacitors usually have higher ESR numbers.

The amount of output ripple voltage is primarily a function of the ESR (Equivalent Series Resistance) of the output capacitor and the amplitude of the inductor ripple current (ΔI_{IND}). See the section on inductor ripple current in Application Hints.

The lower capacitor values (100 μF– 330 μF) will allow typically 50 mV to 150 mV of output ripple voltage, while larger-value capacitors will reduce the ripple to approximately 20 mV to 50 mV.

Output Ripple Voltage = (ΔI_{IND}) (ESR of C_{OUT})

To further reduce the output ripple voltage, several standard electrolytic capacitors may be paralleled, or a higher-grade capacitor may be used. Such capacitors are often called "high-frequency," "low-inductance," or "low-ESR." These will reduce the output ripple to 10 mV or 20 mV. However, when operating in the continuous mode, reducing the ESR below 0.03Ω can cause instability in the regulator.

Tantalum capacitors can have a very low ESR, and should be carefully evaluated if it is the only output capacitor. Because of their good low temperature characteristics, a tantalum can be used in parallel with aluminum electrolytics, with the tantalum making up 10% or 20% of the total capacitance.

The capacitor's ripple current rating at 52 kHz should be at least 50% higher than the peak-to-peak inductor ripple current.

CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch is off. This diode should be located close to the LM2574 using short leads and short printed circuit traces.

Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best efficiency, especially in low output voltage switching regulators (less than 5V). Fast-Recovery, High-Efficiency, or Ultra-Fast Recovery diodes are also suitable, but some types with an abrupt turn-off characteristic may cause instability and EMI problems. A fast-recovery diode with soft recovery characteristics is a better choice. Standard 60 Hz diodes (e.g., 1N4001 or 1N5400, etc.) are also **not suitable.** See *Figure 9* for Schottky and "soft" fast-recovery diode selection guide.

OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply will contain a sawtooth ripple voltage at the switcher frequency, typically about 1% of the output voltage, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is due mainly to the inductor sawtooth ripple current multiplied by the ESR of the output capacitor. (See the inductor selection in the application hints.)

The voltage spikes are present because of the the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. To minimize these voltage spikes, special low inductance capacitors can be used, and their lead lengths must be kept short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

An additional small LC filter (20 μH & 100 μF) can be added to the output (as shown in *Figure 16*) to further reduce the amount of output ripple and transients. A 10 × reduction in output ripple voltage and transients is possible with this filter.

Application Hints (Continued)

FEEDBACK CONNECTION

The LM2574 (fixed voltage versions) feedback pin must be wired to the output voltage point of the switching power supply. When using the adjustable version, physically locate both output voltage programming resistors near the LM2574 to avoid picking up unwanted noise. Avoid using resistors greater than 100 kΩ because of the increased chance of noise pickup.

$\overline{ON}$/OFF INPUT

For normal operation, the $\overline{ON}$/OFF pin should be grounded or driven with a low-level TTL voltage (typically below 1.6V). To put the regulator into standby mode, drive this pin with a high-level TTL or CMOS signal. The $\overline{ON}$/OFF pin can be safely pulled up to $+V_{IN}$ without a resistor in series with it. The $\overline{ON}$/OFF pin should not be left open.

GROUNDING

The 8-pin molded DIP and the 14-pin surface mount package have separate power and signal ground pins. Both ground pins should be soldered directly to wide printed circuit board copper traces to assure low inductance connections and good thermal properties.

THERMAL CONSIDERATIONS

The 8-pin DIP (N) package and the 14-pin Surface Mount (M) package are molded plastic packages with solid copper lead frames. The copper lead frame conducts the majority of the heat from the die, through the leads, to the printed circuit board copper, which acts as the heat sink. For best thermal performance, wide copper traces should be used, and all ground and unused pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane. Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and even double-sided or multilayer boards provide better heat paths to the surrounding air. Unless the power levels are small, using a socket for the 8-pin package is not recommended because of the additional thermal resistance it introduces, and the resultant higher junction temperature.

Because of the 0.5A current rating of the LM2574, the total package power dissipation for this switcher is quite low, ranging from approximately 0.1W up to 0.75W under varying conditions. In a carefully engineered printed circuit board, both the N and the M package can easily dissipate up to 0.75W, even at ambient temperatures of 60°C, and still keep the maximum junction temperature below 125°C.

A curve displaying thermal resistance vs. pc board area for the two packages is shown in the Typical Performance Characteristics curves section of this data sheet.

These thermal resistance numbers are approximate, and there can be many factors that will affect the final thermal resistance. Some of these factors include board size, shape, thickness, position, location, and board temperature. Other factors are, the area of printed circuit copper, copper thickness, trace width, multi-layer, single- or double-sided, and the amount of solder on the board. The effectiveness of the pc board to dissipate heat also depends on the size, number and spacing of other components on the board. Furthermore, some of these components, such as the catch diode and inductor will generate some additional heat. Also, the thermal resistance decreases as the power level increases because of the increased air current activity at the higher power levels, and the lower surface to air resistance coefficient at higher temperatures.

The data sheet thermal resistance curves and the thermal model in ***Switchers Made Simple*** software (version 3.3) can estimate the maximum junction temperature based on operating conditions. In addition, the junction temperature can be estimated in actual circuit operation by using the following equation.

$$T_j = T_{cu} + (\theta_{j\text{-}cu} \times P_D)$$

With the switcher operating under worst case conditions and all other components on the board in the intended enclosure, measure the copper temperature (T_{cu}) near the IC. This can be done by temporarily soldering a small thermocouple to the pc board copper near the IC, or by holding a small thermocouple on the pc board copper using thermal grease for good thermal conduction.

The thermal resistance ($\theta_{j\text{-}cu}$) for the two packages is:

$\theta_{j\text{-}cu}$ = 42°C/W for the N-8 package
$\theta_{j\text{-}cu}$ = 52°C/W for the M-14 package

The power dissipation (P_D) for the IC could be measured, or it can be estimated by using the formula:

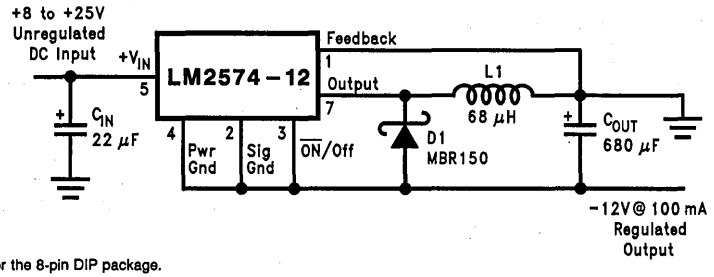
$$P_D = (V_{IN})(I_S) + \left(\frac{V_O}{V_{IN}}\right)(I_{LOAD})(V_{SAT})$$

Where I_S is obtained from the typical supply current curve (adjustable version use the supply current vs. duty cycle curve).

Additional Applications

INVERTING REGULATOR

Figure 11 shows a LM2574-12 in a buck-boost configuration to generate a negative 12V output from a positive input voltage. This circuit bootstraps the regulator's ground pin to the negative output voltage, then by grounding the feedback pin, the regulator senses the inverted output voltage and regulates it to −12V.



Note: Pin numbers are for the 8-pin DIP package.

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FIGURE 11. Inverting Buck-Boost Develops −12V

Additional Applications (Continued)

For an input voltage of 8V or more, the maximum available output current in this configuration is approximately 100 mA. At lighter loads, the minimum input voltage required drops to approximately 4.7V.

The switch currents in this buck-boost configuration are higher than in the standard buck-mode design, thus lowering the available output current. Also, the start-up input current of the buck-boost converter is higher than the standard buck-mode regulator, and this may overload an input power source with a current limit less than 0.6A. Using a delayed turn-on or an undervoltage lockout circuit (described in the next section) would allow the input voltage to rise to a high enough level before the switcher would be allowed to turn on.

Because of the structural differences between the buck and the buck-boost regulator topologies, the buck regulator design procedure section can not be used to to select the inductor or the output capacitor. The recommended range of inductor values for the buck-boost design is between 68 μH and 220 μH, and the output capacitor values must be larger than what is normally required for buck designs. Low input voltages or high output currents require a large value output capacitor (in the thousands of micro Farads).

The peak inductor current, which is the same as the peak switch current, can be calculated from the following formula:

$$I_p \approx \frac{I_{LOAD}(V_{IN} + |V_O|)}{V_{IN}} + \frac{V_{IN}|V_O|}{V_{IN}+|V_O|} \times \frac{1}{2L_1 f_{osc}}$$

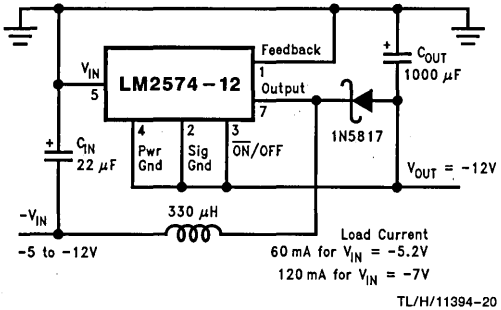
Where f_{osc} = 52 kHz. Under normal continuous inductor current operating conditions, the minimum V_{IN} represents the worst case. Select an inductor that is rated for the peak current anticipated.

Also, the maximum voltage appearing across the regulator is the absolute sum of the input and output voltage. For a −12V output, the maximum input voltage for the LM2574 is +28V, or +48V for the LM2574HV.

The ***Switchers Made Simple*** (version 3.3) design software can be used to determine the feasibility of regulator designs using different topologies, different input-output parameters, different components, etc.

NEGATIVE BOOST REGULATOR

Another variation on the buck-boost topology is the negative boost configuration. The circuit in *Figure 12* accepts an input voltage ranging from −5V to −12V and provides a regulated −12V output. Input voltages greater than −12V will cause the output to rise above −12V, but will not damage the regulator.



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Note: Pin numbers are for 8-pin DIP package.

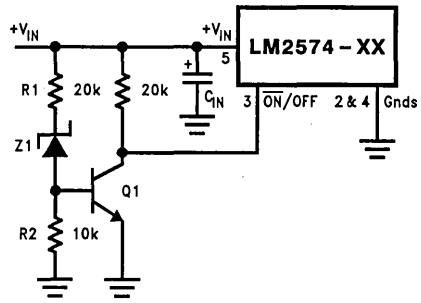
FIGURE 12. Negative Boost

Because of the boosting function of this type of regulator, the switch current is relatively high, especially at low input voltages. Output load current limitations are a result of the maximum current rating of the switch. Also, boost regulators can not provide current limiting load protection in the event of a shorted load, so some other means (such as a fuse) may be necessary.

UNDERVOLTAGE LOCKOUT

In some applications it is desirable to keep the regulator off until the input voltage reaches a certain threshold. An undervoltage lockout circuit which accomplishes this task is shown in *Figure 13*, while *Figure 14* shows the same circuit applied to a buck-boost configuration. These circuits keep the regulator off until the input voltage reaches a predetermined level.

$$V_{TH} \approx V_{Z1} + 2V_{BE}(Q1)$$



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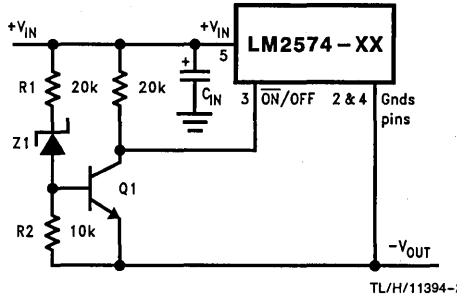
Note: Complete circuit not shown.

Note: Pin numbers are for 8-pin DIP package.

FIGURE 13. Undervoltage Lockout for Buck Circuit



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Note: Complete circuit not shown (see Figure 11).

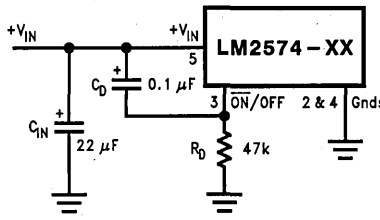
Note: Pin numbers are for 8-pin DIP package.

FIGURE 14. Undervoltage Lockout for Buck-Boost Circuit

Additional Applications (Continued)

DELAYED STARTUP

The $\overline{ON}$/OFF pin can be used to provide a delayed startup feature as shown in *Figure 15*. With an input voltage of 20V and for the part values shown, the circuit provides approximately 10 ms of delay time before the circuit begins switching. Increasing the RC time constant can provide longer delay times. But excessively large RC time constants can cause problems with input voltages that are high in 60 Hz or 120 Hz ripple, by coupling the ripple into the $\overline{ON}$/OFF pin.



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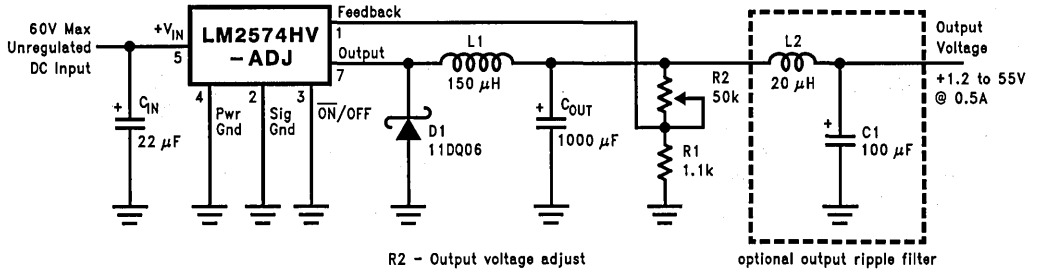
Note: Complete circuit not shown.

Note: Pin numbers are for 8-pin DIP package.

FIGURE 15. Delayed Startup

ADJUSTABLE OUTPUT, LOW-RIPPLE POWER SUPPLY

A 500 mA power supply that features an adjustable output voltage is shown in *Figure 16*. An additional L-C filter that reduces the output ripple by a factor of 10 or more is included in this circuit.



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Note: Pin numbers are for 8-pin DIP package.

FIGURE 16. 1.2V to 55V Adjustable 500 mA Power Supply with Low Output Ripple

Definition of Terms

BUCK REGULATOR

A switching regulator topology in which a higher voltage is converted to a lower voltage. Also known as a step-down switching regulator.

BUCK-BOOST REGULATOR

A switching regulator topology in which a positive voltage is converted to a negative voltage without a transformer.

DUTY CYCLE (D)

Ratio of the output switch's on-time to the oscillator period.

$$\textit{for buck regulator} \qquad D = \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}}$$

$$\textit{for buck-boost regulator} \qquad D = \frac{t_{ON}}{T} = \frac{|V_O|}{|V_O| + V_{IN}}$$

CATCH DIODE OR CURRENT STEERING DIODE

The diode which provides a return path for the load current when the LM2574 switch is OFF.

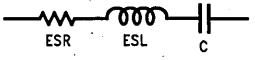
EFFICIENCY (η)

The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR)

The purely resistive component of a real capacitor's impedance (see *Figure 17*). It causes power loss resulting in capacitor heating, which directly affects the capacitor's operating lifetime. When used as a switching regulator output filter, higher ESR values result in higher output ripple voltages.



TL/H/11394–25

FIGURE 17. Simple Model of a Real Capacitor

Most standard aluminum electrolytic capacitors in the 100 µF–1000 µF range have 0.5Ω to 0.1Ω ESR. Higher-grade capacitors ("low-ESR", "high-frequency", or "low-inductance") in the 100 µF–1000 µF range generally have ESR of less than 0.15Ω.

EQUIVALENT SERIES INDUCTANCE (ESL)

The pure inductance component of a capacitor (see *Figure 17*). The amount of inductance is determined to a large extent on the capacitor's construction. In a buck regulator, this unwanted inductance causes voltage spikes to appear on the output.

Definition of Terms (Continued)

OUTPUT RIPPLE VOLTAGE

The AC component of the switching regulator's output voltage. It is usually dominated by the output capacitor's ESR multiplied by the inductor's ripple current (ΔI_{IND}). The peak-to-peak value of this sawtooth ripple current can be determined by reading the Inductor Ripple Current section of the Application hints.

CAPACITOR RIPPLE CURRENT

RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature.

STANDBY QUIESCENT CURRENT (I_{STBY})

Supply current required by the LM2574 when in the standby mode ($\overline{ON}$/OFF pin is driven to TTL-high voltage, thus turning the output switch OFF).

INDUCTOR RIPPLE CURRENT (ΔI_{IND})

The peak-to-peak value of the inductor current waveform, typically a sawtooth waveform when the regulator is operating in the continuous mode (vs. discontinuous mode).

CONTINUOUS/DISCONTINUOUS MODE OPERATION

Relates to the inductor current. In the continuous mode, the inductor current is always flowing and never drops to zero, vs. the discontinuous mode, where the inductor current drops to zero for a period of time in the normal switching cycle.

INDUCTOR SATURATION

The condition which exists when an inductor cannot hold any more magnetic flux. When an inductor saturates, the inductor appears less inductive and the resistive component dominates. Inductor current is then limited only by the DC resistance of the wire and the available source current.

OPERATING VOLT MICROSECOND CONSTANT ($E \bullet T_{op}$)

The product (in Volt•μs) of the voltage applied to the inductor and the time the voltage is applied. This $E \bullet T_{op}$ constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.

National Semiconductor

LM2594
SIMPLE SWITCHER® Power Converter 150 kHz 0.5A Step-Down Voltage Regulator

General Description

The LM2594 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version, and are packaged in a 8-lead DIP and a 8-lead surface mount package.

Requiring a minimum number of external components, these regulators are simple to use and feature internal frequency compensation†, a fixed-frequency oscillator, and improved line and load regulation specifications.

The LM2594 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2594 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 μA standby current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

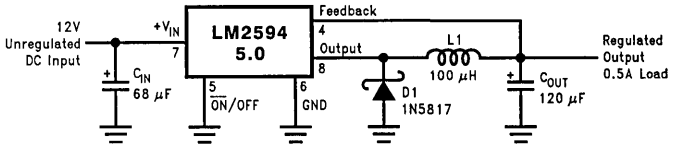
Features

- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V ±4% max over line and load conditions
- Available in 8-pin surface mount and DIP-8 package
- Guaranteed 0.5A output current
- Input voltage range up to 40V
- Requires only 4 external components
- 150 kHz fixed frequency internal oscillator
- TTL Shutdown capability
- Low power standby mode, I_Q typically 85 μA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative convertor

Typical Application (Fixed Output Voltage Versions)



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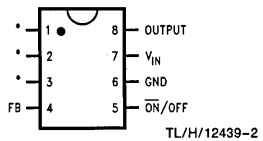
Connection Diagrams and Order Information

8-Lead DIP (N)



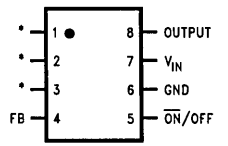
TL/H/12439-2

Top View

Order Number LM2594N-3.3, LM2594N-5.0, LM2594N-12 or LM2594N-ADJ
See NS Package Number N08E

*No internal connection, but should be soldered to pc board for best heat transfer.

8-Lead Surface Mount (M)



TL/H/12439-3

Top View

Order Number LM2594M-3.3, LM2594M-5.0, LM2594M-12 or LM2594M-ADJ
See NS Package Number M08A

†Patent Number 5,382,918.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage	45V
$\overline{ON}$/OFF Pin Input Voltage	$-0.3 \le V \le +25V$
Feedback Pin Voltage	$-0.3 \le V \le +25V$
Output Voltage to Ground (Steady State)	$-1V$
Power Dissipation	Internally limited
Storage Temperature Range	$-65°C$ to $+150°C$
ESD Susceptibility	
Human Body Model (Note 2)	2 kV
Lead Temperature	
M8 Package	
Vapor Phase (60 sec.)	$+215°C$
Infrared (15 sec.)	$+220°C$
N Package (Soldering, 10 sec.)	$+260°C$
Maximum Junction Temperature	$+150°C$

Operating Conditions

Temperature Range	$-40°C \le T_J +125°C$
Supply Voltage	4.5V to 40V

LM2594-3.3

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594-3.3		Units (Limits)
			Type (Note 3)	Limit (Note 4)	
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	$4.75V \le V_{IN} \le 40V$, $0.1A \le I_{LOAD} \le 0.5A$	3.3	3.168/**3.135** 3.432/**3.465**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	80		%

LM2594-5.0

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594-5.0		Units (Limits)
			Type (Note 3)	Limit (Note 4)	
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	$7V \le V_{IN} \le 40V$, $0.1A \le I_{LOAD} \le 0.5A$	5.0	4.800/**4.750** 5.200/**5.250**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	82		%

LM2594-12

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594-12		Units (Limits)
			Type (Note 3)	Limit (Note 4)	
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 2*					
V_{OUT}	Output Voltage	$15V \le V_{IN} \le 40V$, $0.1A \le I_{LOAD} \le 0.5A$	12.0	11.52/**11.40** 12.48/**12.60**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	88		%

LM2594-ADJ

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**

Symbol	Parameter	Conditions	LM2594-ADJ		Units (Limits)
			Type (Note 3)	Limit (Note 4)	
SYSTEM PARAMETERS (Note 5) Test Circuit *Figure 2*					
V_{FB}	Feedback Voltage	4.5V ≤ V_{IN} ≤ 40V, 0.1A ≤ I_{LOAD} ≤ 0.5A V_{OUT} programmed for 3V. Circuit of *Figure 2*	1.230	 1.193/**1.180** 1.267/**1.280**	V V(min) V(max)
η	Efficiency	V_{IN} = 12V, I_{LOAD} = 0.5A	80		%

All Output Voltage Versions

Electrical Characteristics Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V for the 3.3V, 5V, and Adjustable version and V_{IN} = 24V for the 12V version. I_{LOAD} = 100 mA

Symbol	Parameter	Conditions	LM2594-XX		Units (Limits)
			Type (Note 3)	Limit (Note 4)	
DEVICE PARAMETERS					
I_b	Feedback Bias Current	Adjustable Version Only, VFB = 1.3V	10	50/**100**	nA
f_O	Oscillator Frequency	(Note 6)	150	 127/**110** 173/**173**	kHz kHz(min) kHz(max)
V_{SAT}	Saturation Voltage	I_{OUT} = 0.5A (Notes 7 and 8)	0.9	 1.1/**1.2**	V V(max)
DC	Max Duty Cycle (ON) Min Duty Cycle (OFF)	(Note 8) (Note 9)	100 0		%
I_{CL}	Current Limit	Peak Current, (Notes 7 and 8)	0.8	 0.65/**0.58** 1.3/**1.4**	A A(min) A(max)
I_L	Output Leakage Current	(Notes 7, 9, and 10) Output = 0V Output = −1V	 2	50 15	μA(max) mA mA(max)
I_Q	Quiescent Current	(Note 9)	5	 10	mA mA(max)
I_{STBY}	Standby Quiescent Current	ON/OFF pin = 5V (OFF) (Note 10)	85	 200/**250**	μA μA(max)
θ_{JA}	Thermal Resistance	N Package, Junction to Ambient (Note 11) M Package, Junction to Ambient (Note 11)	95 150		°C/W
ON/OFF CONTROL Test Circuit *Figure 2*					
V_{IH} V_{IL}	$\overline{ON}$/OFF Pin Logic Input Threshold Voltage	 Low (Regulator ON) High (Regulator OFF)	1.3	 **0.6** **2.0**	V V(max) V(min)
I_H	$\overline{ON}$/OFF Pin Input Current	V_{LOGIC} = 2.5V (Regulator OFF)	5	 15	μA μA(max)
I_L		V_{LOGIC} = 0.5V (Regulator ON)	0.02	 5	μA μA(max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.

Note 3: Typical numbers are at 25°C and represent the most likely norm.

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 5: External components such as the catch diode, inductor, input and output capacitors, and voltage programming resistors can affect switching regulator system performance. When the LM2594 is used as shown in the *Figure 2* test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.

Note 6: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.

Note 7: No diode, inductor or capacitor connected to output pin.

Note 8: Feedback pin removed from output and connected to 0V to force the output transistor switch ON.

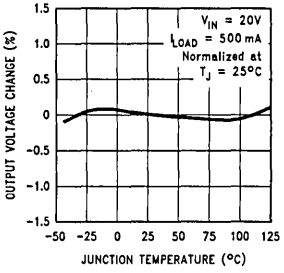
Note 9: Feedback pin removed from output and connected to 12V for the 3.3V, 5V, and the ADJ. version, and 15V for the 12V version, to force the output transistor switch OFF.

Note 10: V_{IN} = 40V.

Note 11: Junction to ambient thermal resistance with approximately 1 square inch of printed circuit board copper surrounding the leads. Additional copper area will lower thermal resistance further. See application hints in this data sheet and the thermal model in ***Switchers Made Simple*** software.

Typical Performance Characteristics (Circuit of *Figure 2*)

Normalized Output Voltage



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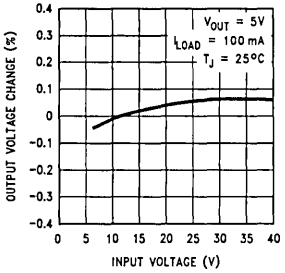
Line Regulation



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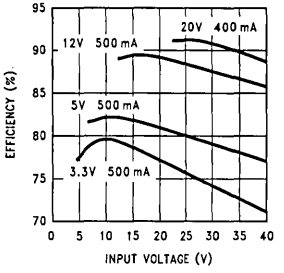
Efficiency



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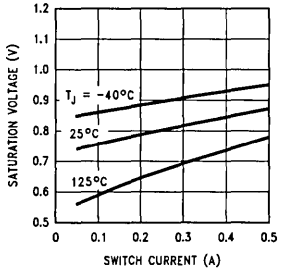
Switch Saturation Voltage



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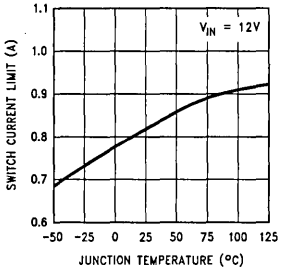
Switch Current Limit



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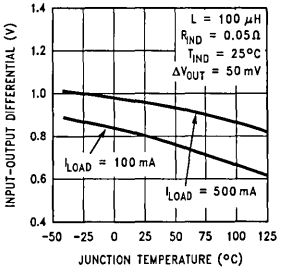
Dropout Voltage



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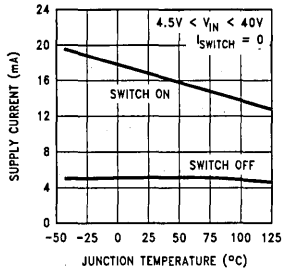
Typical Performance Characteristics (Circuit of *Figure 2*) (Continued)

Quiescent Current



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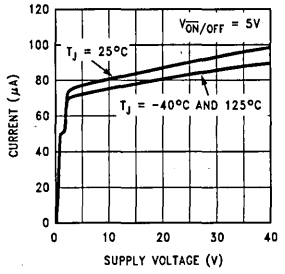
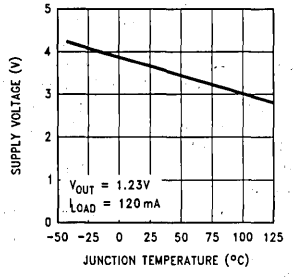
Standby Quiescent Current



TL/H/12439–11

Minimum Operating Supply Voltage



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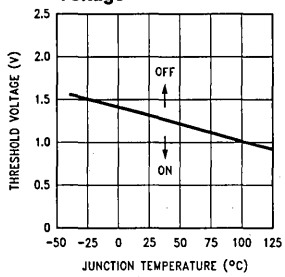
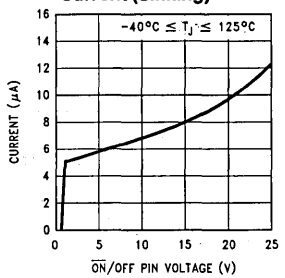
$\overline{ON}$/OFF Threshold Voltage



TL/H/12439–13

$\overline{ON}$/OFF Pin Current (Sinking)



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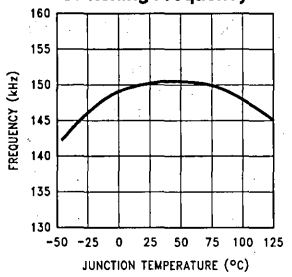
Switching Frequency



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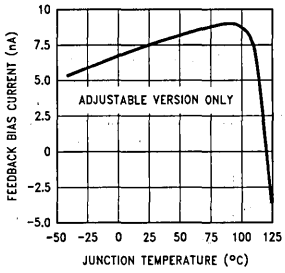
Feedback Pin Bias Current



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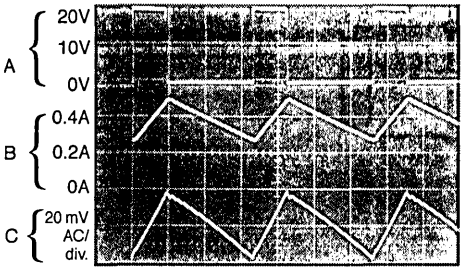
Typical Performance Characteristics (Circuit of *Figure 2*)

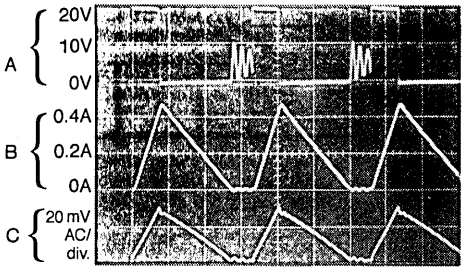
Continuous Mode Switching Waveforms
V_{IN} = 20V, V_{OUT} = 5V, I_{LOAD} = 400 mA
L = 100 μH, C_{OUT} = 120 μF, C_{OUT} ESR = 140 mΩ



TL/H/12439–17

A: Output Pin Voltage, 10V/div.
B: Inductor Current 0.2A/div.
C: Output Ripple Voltage, 20 mV/div.
Horizontal Time Base: 2 μs/div.

Discontinuous Mode Switching Waveforms
V_{IN} = 20V, V_{OUT} = 5V, I_{LOAD} = 200 mA
L = 33 μH, C_{OUT} = 220 μF, C_{OUT} ESR = 60 mΩ



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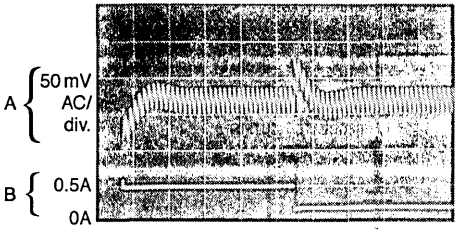
A: Output Pin Voltage, 10V/div.
B: Inductor Current 0.2A/div.
C: Output Ripple Voltage, 20 mV/div.
Horizontal Time Base: 2 μs/div.

Load Transient Response for Continuous Mode
V_{IN} = 20V, V_{OUT} = 5V, I_{LOAD} = 200 mA to 500 mA
L = 100 μH, C_{OUT} = 120 μF, C_{OUT} ESR = 140 mΩ



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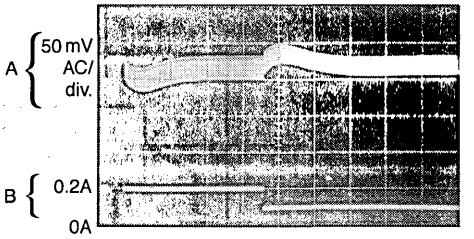
A: Output Voltage, 50 mV/div. (AC)
B: 200 mA to 500 mA Load Pulse
Horizontal Time Base: 50 μs/div.

Load Transient Response for Discontinuous Mode
V_{IN} = 20V, V_{OUT} = 5V, I_{LOAD} = 100 mA to 200 mA
L = 33 μH, C_{OUT} = 220 μF, C_{OUT} ESR = 60 mΩ



TL/H/12439–20

A: Output Voltage, 50 mV/div. (AC)
B: 100 mA to 200 mA Load Pulse
Horizontal Time Base: 200 μs/div.

Block Diagram

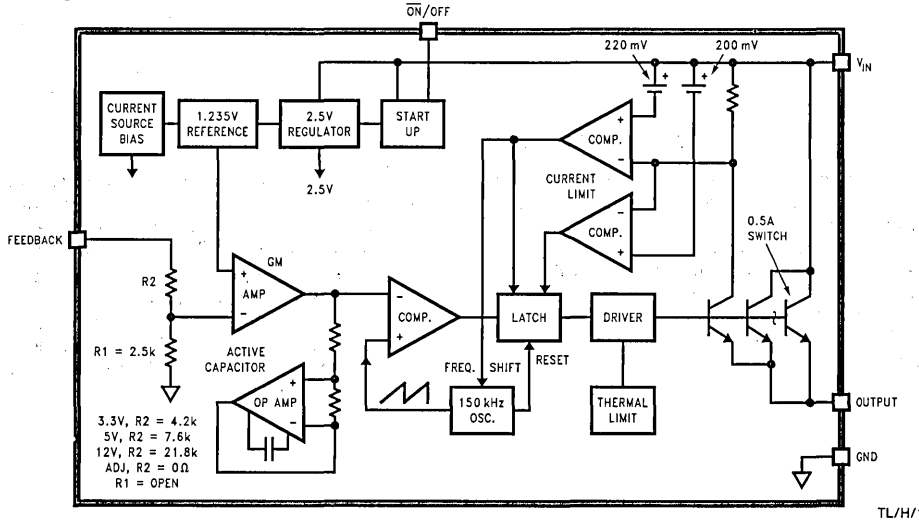


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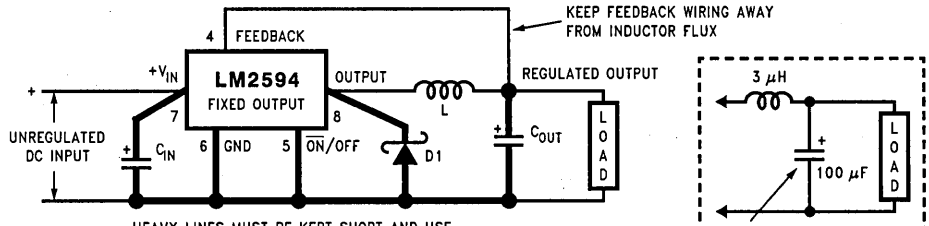
FIGURE 1

Test Circuit and Layout Guidelines

Fixed Output Voltage Versions



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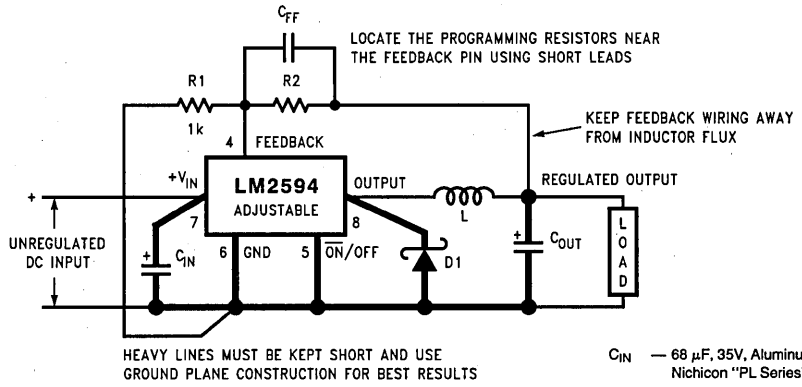
C_{IN} — 68 µF, 35V, Aluminum Electrolytic
Nichicon "PL Series"

C_{OUT} — 120 µF, 25V Aluminum Electrolytic,
Nichicon "PL Series"

D1 — 1A, 40V Schottky Rectifier, 1N5819

L1 — 100 µH, L20

Adjustable Output Voltage Versions



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$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \quad \text{where } V_{REF} = 1.23V$$

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Select R_1 to be approximately 1 kΩ, use a 1% resistor for best stability.

C_{IN} — 68 µF, 35V, Aluminum Electrolytic
Nichicon "PL Series"

C_{OUT} — 120 µF, 25V Aluminum Electrolytic,
Nichicon "PL Series"

D1 — 1A, 40V Schottky Rectifier, 1N5819

L1 — 100 µH, L20

R_1 — 1 kΩ, 1%

C_{FF} — See Application Information Section

FIGURE 2. Standard Test Circuits and Layout Guides

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by **heavy lines should be wide printed circuit traces and should be kept as short as possible.** For best results, external components should be located as close to the switcher IC as possible using ground plane construction or single point grounding.

If **open core inductors are used,** special care must be taken as to the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and C_{OUT} wiring can cause problems.

When using the adjustable version, special care must be taken as to the location of the feedback resistors and the associated wiring. Physically locate both resistors near the IC, and route the wiring away from the inductor, especially an open core type of inductor. (See application section for more information.)

LM2594 Series Buck Regulator Design Procedure (Fixed Output)

PROCEDURE (Fixed Output Voltage Version)

Given:

V_{OUT} = Regulated Output Voltage (3.3V, 5V or 12V)

V_{IN}(max) = Maximum DC Input Voltage

I_{LOAD}(max) = Maximum Load Current

1. Inductor Selection (L1)

A. Select the correct inductor value selection guide from *Figures 5, 6,* or *7.* (Output voltages of 3.3V, 5V, or 12V respectively.) For all other voltages, see the design procedure for the adjustable version.

B. From the inductor value selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code (LXX).

C. Select an appropriate inductor from the four manufacturer's part numbers listed in *Figure 9.*

2. Output Capacitor Selection (C_{OUT})

A. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between 82 μF and 220 μF and low ESR solid tantalum capacitors between 15 μF and 100 μF provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than 220 μF.

For additional information, see section on output capacitors in application information section.

B. To simplify the capacitor selection procedure, refer to the quick design component selection table shown in *Figure 3.* This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions.

C. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements for low output ripple voltage.

D. For computer aided design software, see ***Switchers Made Simple***® version 4.1 or later.

3. Catch Diode Selection (D1)

A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2594. The most stressful condition for this diode is an overload or shorted output condition.

B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

C. This diode must be fast (short reverse recovery time) and must be located close to the LM2594 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or High-

Procedure continued on next page.

EXAMPLE (Fixed Output Voltage Version)

Given:

V_{OUT} = 5V

V_{IN}(max) = 12V

I_{LOAD}(max) = 0.4A

1. Inductor Selection (L1)

A. Use the inductor selection guide for the 5V version shown in *Figure 6.*

B. From the inductor value selection guide shown in *Figure 6,* the inductance region intersected by the 12V horizontal line and the 0.4A vertical line is 100 μH, and the inductor code is L20.

C. The inductance value required is 100 μH. From the table in *Figure 9,* go to the L20 line and choose an inductor part number from any of the four manufacturers shown. (In most instance, both through hole and surface mount inductors are available.)

2. Output Capacitor Selection (C_{OUT})

A. See section on output capacitors in application information section.

B. From the quick design component selection table shown in *Figure 3,* locate the 5V output voltage section. In the load current column, choose the load current line that is closest to the current needed in your application, for this example, use the 0.5A line. In the maximum input voltage column, select the line that covers the input voltage needed in your application, in this example, use the 15V line. Continuing on this line are recommended inductors and capacitors that will provide the best overall performance.

The capacitor list contains both through hole electrolytic and surface mount tantalum capacitors from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturer's series that are listed in the table be used.

In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers needed.

120 μF 25V Panasonic HFQ Series

120 μF 25V Nichicon PL Series

C. For a 5V output, a capacitor voltage rating at least 7.5V or more is needed. But, in this example, even a low ESR, switching grade, 120 μF 10V aluminum electrolytic capacitor would exhibit approximately 400 mΩ of ESR (see the curve in *Figure 14* for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to 1% of the output voltage, or less, a capacitor with a higher voltage rating (lower ESR) should be selected. A 16V or 25V capacitor will reduce the ripple voltage by approximately half.

3. Catch Diode Selection (D1)

A. Refer to the table shown in *Figure 12.* In this example, a 1A, 20V, 1N5817 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output.

Example continued on next page.

LM2594 Series Buck Regulator Design Procedure (Fixed Output) (Continued)

PROCEDURE (Fixed Output Voltage Version)

Efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.

4. Input Capacitor (C_{IN})

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least ½ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in *Figure 13* shows typical RMS current ratings for several different aluminum electrolytic capacitor values.

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.

If solid tantalum input capacitors are used, it is recommended that they be surge current tested by the manufacturer.

Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the V_{IN} pin.

For additional information, see section on input capacitors in Application Information section.

EXAMPLE (Fixed Output Voltage Version)

4. Input Capacitor (C_{IN})

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12V, an aluminum electrolytic capacitor with a voltage rating greater than 18V ($1.5 \times V_{IN}$) would be needed. The next higher capacitor voltage rating is 25V.

The RMS current rating requirement for the input capacitor in a buck regulator is approximately ½ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed. The curves shown in *Figure 13* can be used to select an appropriate input capacitor. From the curves, locate the 25V line and note which capacitor values have RMS current ratings greater than 200 mA. Either a 47 µF or 68 µF, 25V capacitor could be used.

For a through hole design, a 68 µF/25V electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.

For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

Conditions			Inductor		Output Capacitor			
					Through Hole		Surface Mount	
Output Voltage (V)	Load Current (A)	Max Input Voltage (V)	Inductance (µH)	Inductor (#)	Panasonic HFQ Series (µF/V)	Nichicon PL Series (µF/V)	AVX TPS Series (µF/V)	Sprague 595D Series (µF/V)
3.3	0.5	5	33	L14	220/16	220/16	100/16	100/6.3
		7	47	L13	120/25	120/25	100/16	100/6.3
		10	68	L21	120/25	120/25	100/16	100/6.3
		40	100	L20	120/35	120/35	100/16	100/6.3
	0.2	6	68	L4	120/25	120/25	100/16	100/6.3
		10	150	L10	120/16	120/16	100/16	100/6.3
		40	220	L9	120/16	120/16	100/16	100/6.3
5	0.5	8	47	L13	180/16	180/16	100/16	33/25
		10	68	L21	180/16	180/16	100/16	33/25
		15	100	L20	120/25	120/25	100/16	33/25
		40	150	L19	120/25	120/25	100/16	33/25
	0.2	9	150	L10	82/16	82/16	100/16	33/25
		20	220	L9	120/16	120/16	100/16	33/25
		40	330	L8	120/16	120/16	100/16	33/25
12	0.5	15	68	L21	82/25	82/25	100/16	15/25
		18	150	L19	82/25	82/25	100/16	15/25
		30	220	L27	82/25	82/25	100/16	15/25
		40	330	L26	82/25	82/25	100/16	15/25
	0.2	15	100	L11	82/25	82/25	100/16	15/25
		20	220	L9	82/25	82/25	100/16	15/25
		40	330	L17	82/25	82/25	100/16	15/25

FIGURE 3. LM2594 Fixed Voltage Quick Design Component Selection Table

LM2594 Series Buck Regulator Design Procedure (Adjustable Output)

PROCEDURE (Adjustable Output Voltage Version)

Given:

V_{OUT} = Regulated Output Voltage

$V_{IN}(max)$ = Maximum Input Voltage

$I_{LOAD}(max)$ = Maximum Load Current

F = Switching Frequency *(Fixed at a nominal 150 kHz).*

1. **Programming Output Voltage** (Selecting R_1 and R_2, as shown in *Figure 2*)

   Use the following formula to select the appropriate resistor values.

   $$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \quad \text{where } V_{REF} = 1.23V$$

   Select a value for R_1 between 240Ω and 1.5 kΩ. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use 1% metal film resistors.)

   $$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

2. **Inductor Selection (L1)**

   A. Calculate the inductor Volt microsecond constant E • T (V • μs), from the following formula:

   $$E \bullet T = (V_{IN} - V_{OUT} - V_{SAT}) \bullet \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} + V_D} \bullet \frac{1000}{150\ kHz}\ (V \bullet \mu s)$$

   where V_{SAT} = internal switch saturation voltage = 0.9V

   and V_D = diode forward voltage drop = 0.5V

   B. Use the E • T value from the previous formula and match it with the E • T number on the vertical axis of the Inductor Value Selection Guide shown in *Figure 8.*

   C. on the horizontal axis, select the maximum load current.

   D. Identify the inductance region intersected by the E • T value and the Maximum Load Current value. Each region is identified by an inductance value and an inductor code (LXX).

   E. Select an appropriate inductor from the four manufacturer's part numbers listed in *Figure 9.*

3. **Output Capacitor Selection (C_{OUT})**

   A. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between 82 μF and 220 μF provide the best results. This capacitor should be located close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than 220 μF. **For additional information, see section on output capacitors in application information section.**

   B. To simplify the capacitor selection procedure, refer to the quick design table shown in *Figure 4.* This table contains different output voltages, and lists various output capacitors that will provide the best design solutions.

   C. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

Procedure continued on next page.

EXAMPLE (Adjustable Output Voltage Version)

Given:

V_{OUT} = 20V

$V_{IN}(max)$ = 28V

$I_{LOAD}(max)$ = 0.5A

F = Switching Frequency *(Fixed at a nominal 150 kHz).*

1. **Programming Output Voltage** (Selecting R_1 and R_2, as shown in *Figure 2*)

   Select R_1 to be 1 kΩ, 1%. Solve for R_2.

   $$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{20V}{1.23V} - 1\right)$$

   R_2 = 1k (16.26 − 1) = 15.26k, closest 1% value is 15.4 kΩ.

   R_2 = 15.4 kΩ.

2. **Inductor Selection (L1)**

   A. Calculate the inductor Volt • microsecond constant (E • T),

   $$E \bullet T = (28 - 20 - 0.9) \bullet \frac{20 + 0.5}{28 - 0.9 + 0.5} \bullet \frac{1000}{150}\ (V \bullet \mu s)$$

   $$E \bullet T = (7.1) \bullet \frac{20.5}{27.6} \bullet 6.67\ (V \bullet \mu s) = 35.2\ (V \bullet \mu s)$$

   B. E • T = 35.2 (V • μs)

   C. $I_{LOAD}(max)$ = 0.5A

   D. From the inductor value selection guide shown in *Figure 8,* the inductance region intersected by the 35 (V • μs) horizontal line and the 0.5A vertical line is 150 μH, and the inductor code is L19.

   E. From the table in *Figure 9,* locate line L19, and select an inductor part number from the list of manufacturers part numbers.

3. **Output Capacitor Selection (C_{OUT})**

   A. See section on C_{OUT} in Application Information section.

   B. From the quick design table shown in *Figure 4,* locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24V line. Under the output capacitor section, select a capacitor from the list of through hole electrolytic or surface mount tantalum types from four different capacitor manufacturers. It is recommended that both the manufacturers and the manufacturers series that are listed in the table be used.

   In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available.

   82 μF 50V Panasonic HFQ Series

   120 μF 50V Nichicon PL Series

Example continued on next page.

LM2594 Series Buck Regulator Design Procedure (Adjustable Output)

PROCEDURE (Adjustable Output Voltage Version)

4. Feedforward Capacitor (C_{FF}) (See *Figure 2*)

For output voltages greater than approximately 10V, an additional capacitor is required. The compensation capacitor is typically between 50 pF and 10 nF, and is wired in parallel with the output voltage setting resistor, R_2. It provides additional stability for high output voltages, low input-output voltages, and/or very low ESR output capacitors, such as solid tantalum capacitors.

$$C_{FF} = \frac{1}{31 \times 10^3 \times R_2}$$

This capacitor type can be ceramic, plastic, silver mica, etc. (Because of the unstable characteristics of ceramic capacitors made with Z5U material, they are not recommended.)

5. Catch Diode Selection (D1)

A. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2594. The most stressful condition for this diode is an overload or shorted output condition.

B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

C. This diode must be fast (short reverse recovery time) and must be located close to the LM2594 using short leads and short printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and should be the first choice, especially in low output voltage applications. Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turn-off characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.

6. Input Capacitor (C_{IN})

A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least ½ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. The curve shown in *Figure 13* shows typical RMS current ratings for several different aluminum electrolytic capacitor values.

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 1.5 times the maximum input voltage.

If solid tantalum input capacitors are used, it is recommended that they be surge current tested by the manufacturer.

Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the V_{IN} pin.

For additional information, see section on input capacitors in application information section.

EXAMPLE (Adjustable Output Voltage Version)

C. For a 20V output, a capacitor rating of at least 30V or more is needed. In this example, either a 35V or 50V capacitor would work. A 50V rating was chosen because it has a lower ESR which provides a lower output ripple voltage.

Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100 kHz ESR) closely match the types listed in the table. Refer to the capacitor manufacturers data sheet for this information.

4. Feedforward Capacitor (C_{FF})

The table shown in *Figure 4* contains feed forward capacitor values for various output voltages. In this example, a 1 nF capacitor is needed.

5. Catch Diode Selection (D1)

A. Refer to the table shown in *Figure 12*. Schottky diodes provide the best performance, and in this example a 1A, 40V, 1N5819 Schottky diode would be a good choice. The 1A diode rating is more than adequate and will not be overstressed even for a shorted output.

6. Input Capacitor (C_{IN})

The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 28V, an aluminum electrolytic aluminum electrolytic capacitor with a voltage rating greater than 42V ($1.5 \times V_{IN}$) would be needed. Since the the next higher capacitor voltage rating is 50V, a 50V capacitor should be used. The capacitor voltage rating of ($1.5 \times V_{IN}$) is a conservative guideline, and can be modified somewhat if desired.

The RMS current rating requirement for the input capacitor of a buck regulator is approximately ½ the DC load current. In this example, with a 400 mA load, a capacitor with a RMS current rating of at least 200 mA is needed.

The curves shown in *Figure 13* can be used to select an appropriate input capacitor. From the curves, locate the 50V line and note which capacitor values have RMS current ratings greater than 200 mA. A 47 µF/50V low ESR electrolytic capacitor capacitor is needed.

For a through hole design, a 47 µF/50V electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers capacitors can be used provided the RMS ripple current ratings are adequate.

For surface mount designs, solid tantalum capacitors are recommended. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

To further simplify the buck regulator design procedure, National Semiconductor is making available computer design software to be used with the Simple Switcher line of switching regulators. ***Switchers Made Simple*** *(version 4.1 or later) is available on a 3½" diskette for IBM compatible computers.*

LM2594 Series Buck Regulator Design Procedure (Adjustable Output)

(Continued)

Output Voltage (V)	Through Hole Output Capacitor			Surface Mount Output Capacitor		
	Panasonic HFQ Series (μF/V)	Nichicon PL Series (μF/V)	Feedforward Capacitor	AVX TPS Series (μF/V)	Sprague 595D Series (μF/V)	Feedforward Capacitor
1.2	220/25	220/25	0	220/10	220/10	0
4	180/25	180/25	4.7 nF	100/10	120/10	4.7 nF
6	82/25	82/25	4.7 nF	100/10	120/10	4.7 nF
9	82/25	82/25	3.3 nF	100/16	100/16	3.3 nF
12	82/25	82/25	2.2 nF	100/16	100/16	2.2 nF
15	82/25	82/25	1.5 nF	68/20	100/20	1.5 nF
24	82/50	120/50	1 nF	10/35	15/35	220 pF
28	82/50	120/50	820 pF	10/35	15/35	220 pF

FIGURE 4. Output Capacitor and Feedforward Capacitor Selection Table

LM2594 Series Buck Regulator Design Procedure

INDUCTOR VALUE SELECTION GUIDES (For Continuous Mode Operation)

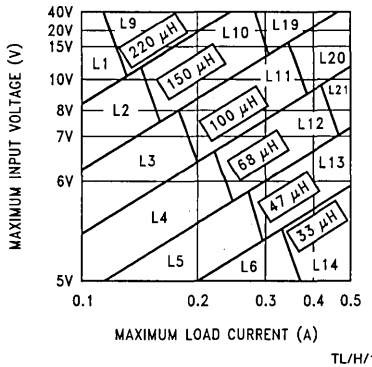

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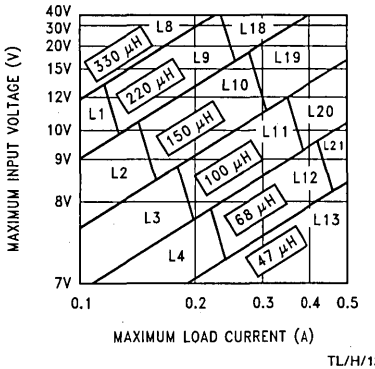
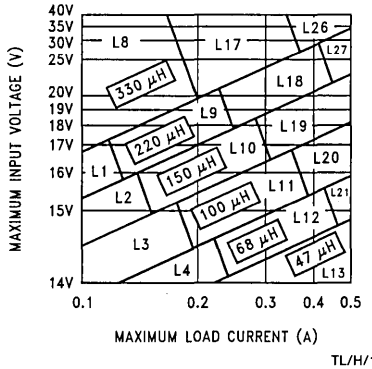
FIGURE 5. LM2594-3.3



TL/H/12439-25

FIGURE 6. LM2594-5.0



TL/H/12439-26

FIGURE 7. LM2594-12

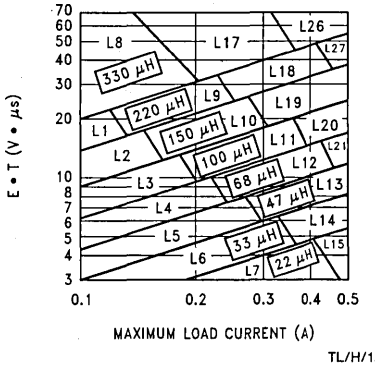


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FIGURE 8. LM2594-ADJ

LM2594 Series Buck Regulator Design Procedure (Continued)

	Inductance (μH)	Current (A)	Schott		Renco		Pulse Engineering		Coilcraft
			Through Hole	Surface Mount	Through Hole	Surface Mount	Through Hole	Surface Mount	Surface Mount
L1	220	0.18	67143910	67144280	RL-5470-3	RL1500-220	PE-53801	PE-53801-S	DO1608-224
L2	150	0.21	67143920	67144290	RL-5470-4	RL1500-150	PE-53802	PE-53802-S	DO1608-154
L3	100	0.26	67143930	67144300	RL-5470-5	RL1500-100	PE-53803	PE-53803-S	DO1608-104
L4	68	0.32	67143940	67144310	RL-1284-68	RL1500-68	PE-53804	PE-53804-S	DO1608-68
L5	47	0.37	67148310	67148420	RL-1284-47	RL1500-47	PE-53805	PE-53805-S	DO1608-473
L6	33	0.44	67148320	67148430	RL-1284-33	RL1500-33	PE-53806	PE-53806-S	DO1608-333
L7	22	0.60	67148330	67148440	RL-1284-22	RL1500-22	PE-53807	PE-53807-S	DO1608-223
L8	330	0.26	67143950	67144320	RL-5470-2	RL1500-330	PE-53808	PE-53808-S	DO3308-334
L9	220	0.32	67143960	67144330	RL-5470-3	RL1500-220	PE-53809	PE-53809-S	DO3308-224
L10	150	0.39	67143970	67144340	RL-5470-4	RL1500-150	PE-53810	PE-53810-S	DO3308-154
L11	100	0.48	67143980	67144350	RL-5470-5	RL1500-100	PE-53811	PE-53811-S	DO3308-104
L12	68	0.58	67143990	67144360	RL-5470-6	RL1500-68	PE-53812	PE-53812-S	DO1608-683
L13	47	0.70	67144000	67144380	RL-5470-7	RL1500-47	PE-53813	PE-53813-S	DO3308-473
L14	33	0.83	67148340	67148450	RL-1284-33	RL1500-33	PE-53814	PE-53814-S	DO1608-333
L15	22	0.99	67148350	67148460	RL-1284-22	RL1500-22	PE-53815	PE-53815-S	DO1608-223
L16	15	1.24	67148360	67148470	RL-1284-15	RL1500-15	PE-53816	PE-53816-S	DO1608-153
L17	330	0.42	67144030	67144410	RL-5471-1	RL1500-330	PE-53817	PE-53817-S	DO3316-334
L18	220	0.55	67144040	67144420	RL-5471-2	RL1500-220	PE-53818	PE-53818-S	DO3316-224
L19	150	0.66	67144050	67144430	RL-5471-3	RL1500-150	PE-53819	PE-53819-S	DO3316-154
L20	100	0.82	67144060	67144440	RL-5471-4	RL1500-100	PE-53820	PE-53820-S	DO3316-104
L21	68	0.99	67144070	67144450	RL-5471-5	RL1500-68	PE-53821	PE-53821-S	DDO3316-683
L26	330	0.80	67144100	67144480	RL-5471-1	—	PE-53826	PE-53826-S	—
L27	220	1.00	67144110	67144490	RL-5471-2	—	PE-53827	PE-53827-S	—

FIGURE 9. Inductor Manufacturers Part Numbers

Coilcraft Inc.	Phone	(800) 322-2645
	FAX	(708) 639-1469
Coilcraft Inc., Europe	Phone	+11 1236 730 595
	FAX	+44 1236 730 627
Pulse Engineering Inc.	Phone	(619) 674-8100
	FAX	(619) 674-8262
Pulse Engineering Inc., Europe	Phone	+353 93 24 107
	FAX	+353 93 24 459
Renco Electronics Inc.	Phone	(800) 645-5828
	FAX	(516) 586-5562
Schott Corp.	Phone	(612) 475-1173
	FAX	(612) 475-1786

FIGURE 10. Inductor Manufacturers Phone Numbers

Nichicon Corp.	Phone	(708) 843-7500
	FAX	(708) 843-2798
Panasonic	Phone	(714) 373-7857
	FAX	(714) 373-7102
AVX Corp.	Phone	(803) 448-9411
	FAX	(803) 448-1943
Sprague/Vishay	Phone	(207) 324-7223
	FAX	(207) 324-4140

FIGURE 11. Capacitor Manufacturers Phone Numbers

LM2594 Series Buck Regulator Design Procedure (Continued)

VR	1A Diodes			
	Surface Mount		Through Hole	
	Schottky	Ultra Fast Recovery	Schottky	Ultra Fast Recovery
20V		All of these diodes are rated to at least 50V.	1N5817	All of these diodes are rated to at least 50V.
			SR102	
30V	MBRS130		1N5818	
			SR103	
			11DQ03	
40V	MBRS140	MURS120	1N5819	MUR120
	10BQ040	10BF10	SR104	HER101
	10MQ040		11DQ04	11DF1
50V or more	MBRS160		SR105	
	10BQ050		MBR150	
	10MQ060		11DQ05	

FIGURE 12. Diode Selection Table

Application Information

PIN FUNCTIONS

$+V_{IN}$—This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents needed by the regulator.

Ground—Circuit ground.

Output—Internal switch. The voltage at this pin switches between $(+V_{IN} - V_{SAT})$ and approximately $-0.5V$, with a duty cycle of V_{OUT}/V_{IN}. To minimize coupling to sensitive circuitry, the PC board copper area connected to this pin should be kept to a minimum.

Feedback—Senses the regulated output voltage to complete the feedback loop.

$\overline{ON}$/OFF—Allows the switching regulator circuit to be shut down using logic level signals thus dropping the total input supply current to approximately 80 μA. Pulling this pin below a threshold voltage of approximately 1.3V turns the regulator on, and pulling this pin above 1.3V (up to a maximum of 25V) shuts the regulator down. If this shutdown feature is not needed, the $\overline{ON}$/OFF pin can be wired to the ground pin or it can be left open, in either case the regulator will be in the ON condition.

EXTERNAL COMPONENTS

C_{IN}—A low ESR aluminum or tantalum bypass capacitor is needed between the input pin and ground pin. It must be located near the regulator using short leads. This capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on.

The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor should be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.

The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately 10°C above an ambient temperature of 105°C. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. Capacitors that are physically large and have a large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.

Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of 40°C, a general guideline would be to select a capacitor with a ripple current rating of approximately 50% of the DC load current. For ambient temperatures up to 70°C, a current rating of 75% of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is needed to satisfy the RMS current requirements.

A graph shown in *Figure 13* shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon "PL" series of low ESR, high reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.

"Standard" electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.

Because of their small size and excellent performance, surface mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turn on when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a 100% surge current testing on their products to minimize this potential problem. If high turn on currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

Application Information (Continued)

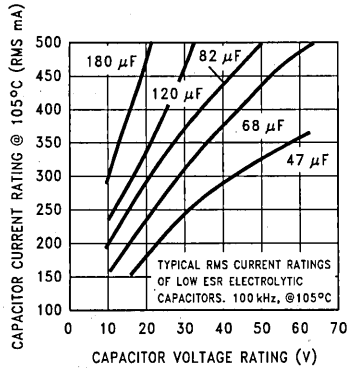

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FIGURE 13. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

OUTPUT CAPACITOR

C_{OUT}—An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low ESR Electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are; the 100 kHz Equivalent Series Resistance (ESR), the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.

The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is needed. This value is determined by the maximum allowable output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.

If very low output ripple voltage (less than 15 mV) is required, refer to the section on Output Voltage Ripple and Transients for a post ripple filter.

An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, Higher voltage electrolytic capacitors have lower ESR values (see *Figure 14*). Often, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See the quick design component selection tables in *Figures 3* and *4* for typical capacitor values, voltage ratings, and manufacturers capacitor types.

Electrolytic capacitors are not recommended for temperatures below −25°C. The ESR rises dramatically at cold temperatures and typically rises 3X @ −25°C and as much as 10X at −40°C. See curve shown in *Figure 15.*

Solid tantalum capacitors have a much better ESR spec for cold temperatures and are recommended for temperatures below −25°C.

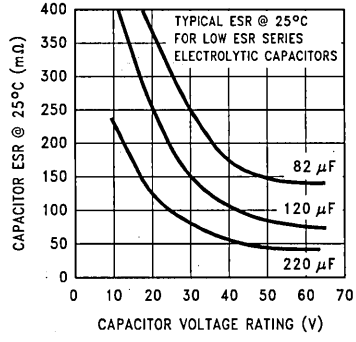

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FIGURE 14. Capacitor ESR vs Capacitor Voltage Rating (Typical Low ESR Electrolytic Capacitor)

CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be located close to the LM2594 using short leads and short printed circuit traces.

Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications (5V and lower). Ultra-fast recovery, or High-Efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series are much too slow and should not be used.

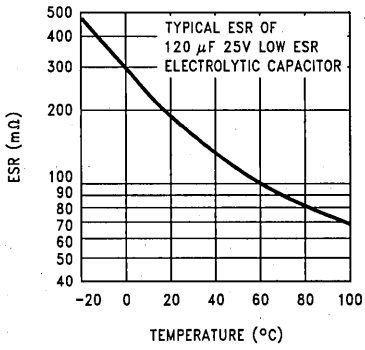

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FIGURE 15. Capacitor ESR Change vs Temperature

INDUCTOR SELECTION

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.

The LM2594 (or any of the Simple Switcher family) can be used for both continuous or discontinuous modes of operation.

Application Information (Continued)

In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak switch, inductor and diode currents, and can have lower output ripple voltage. But it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see *Figures 5* through *8*). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected. (See *Figure 16*.)

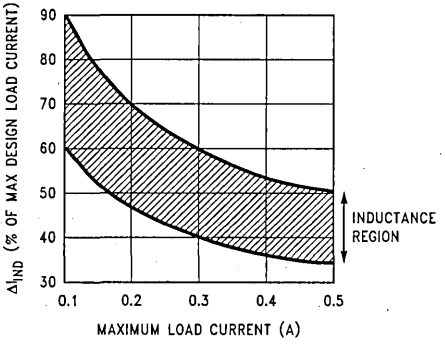

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FIGURE 16. (ΔI_{IND}) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.

When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.

Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, etc., as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wrapped on a ferrite bobbin. This type of construction makes for a inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe. Also see section on Open Core Inductors.

The inductors listed in the selection chart include ferrite E-core construction for Schott, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor and/or the LM2594. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

The inductor manufacturers data sheets include current and energy limits to avoid inductor saturation.

DISCONTINUOUS MODE OPERATION

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications and/or high input voltages, a discontinuous mode design may be a better choice. It would use an inductor that would be physically smaller, and would need only one half to one third the inductance value needed for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents (200 mA and below), the maximum switch current will still be less than the switch current limit.

Discontinuous operation can have voltage waveforms that are considerable different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present. (See photo titled; Discontinuous Mode Switching Waveforms) This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch or the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.

Different inductor types and/or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing. The computer aided design software ***Switchers Made Simple*** (version 4.1) will provide all component values for continuous and discontinuous modes of operation.

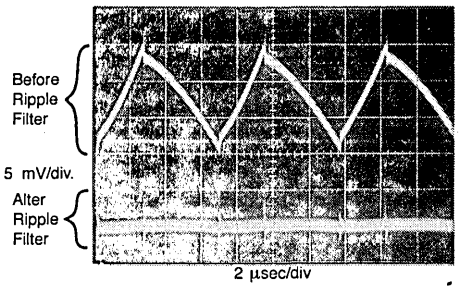

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FIGURE 17. Post Ripple Filter Waveform

Application Information (Continued)

OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately 0.5% to 3% of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low, however, caution must be exercised when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. If very low output ripple voltage is needed (less than 15 mV), a post ripple filter is recommended. (See *Figure 2.*) The inductance required is typically between 1 μH and 5 μH, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. The photo shown in *Figure 17* shows a typical output ripple voltage, with and without a post ripple filter.

When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferable at the output capacitor. This provides a very short scope ground thus eliminating the problems associated with the 3 inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.

The voltage spikes are caused by the fast switching action of the output switch and the diode, and the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-to-peak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.

If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will smoothly change from a continuous to a discontinuous mode of operation. Most switcher designs (irregardless how large the inductor value is) will be forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.

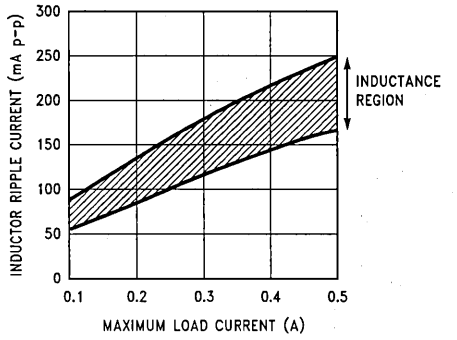

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FIGURE 18. Peak-to-Peak Inductor Ripple Current vs Load Current

In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current (ΔI_{IND}) can be useful for determining a number of other circuit parameters. Parameters such as, peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage and output capacitor ESR can all be calculated from the peak-to-peak ΔI_{IND}. When the inductor nomographs shown in *Figures 5* through *8* are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. The curve shown in *Figure 18* shows the range of (ΔI_{IND}) that can be expected for different load currents. The curve also shows how the peak-to-peak inductor ripple current (ΔI_{IND}) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage (see Inductor Selection Guides).

These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value

Consider the following example:

V_{OUT} = 5V, maximum load current of 300 mA

V_{IN} = 15V, nominal, varying between 11V and 20V.

The selection guide in *Figure 6* shows that the vertical line for a 0.3A load current, and the horizontal line for the 15V input voltage intersect approximately midway between the upper and lower borders of the 150 μH inductance region. A 150 μH inductor will allow a peak-to-peak inductor current (ΔI_{IND}) to flow that will be a percentage of the maximum load current. Referring to *Figure 18,* follow the 0.3A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current (ΔI_{IND}) on the left hand axis (approximately 150 mA p-p).

As the input voltage increases to 20V, it approaches the upper border of the inductance region, and the inductor ripple current increases. Referring to the curve in *Figure 18,* it can be seen that for a load current of 0.3A, the peak-to-peak inductor ripple current (ΔI_{IND}) is 150 mA with 15V in, and can range from 175 mA at the upper border (20V in) to 120 mA at the lower border (11V in).

Application Information (Continued)

Once the ΔI_{IND} value is known, the following formulas can be used to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current

$$= \left(I_{LOAD} + \frac{\Delta I_{IND}}{2}\right) = \left(0.3A + \frac{0.150}{2}\right) = 0.375A$$

2. Minimum load current before the circuit becomes discontinuous

$$= \frac{\Delta I_{IND}}{2} = \frac{0.150}{2} = 0.075A$$

3. Output Ripple Voltage $= (\Delta I_{IND}) \times (\text{ESR of } C_{OUT})$
$= 0.150A \times 0.240\Omega = 36 \text{ mV p-p}$

or

4. ESR of $C_{OUT} = \dfrac{\text{Output Ripple Voltage } (\Delta V_{OUT})}{\Delta I_{IND}}$

$$= \frac{0.036V}{0.150A} = 0.240\Omega$$

OPEN CORE INDUCTORS

Another possible source of increased output ripple voltage or unstable operation is from an open core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PC board copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor, determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PC board copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open core inductor which can cause stability problems or high output ripple voltage problems.

If unstable operation is seen, and an open core inductor is used, it's possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a toroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.

Sometimes, locating a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out), but if it is off center one direction or the other, then problems could arise. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.

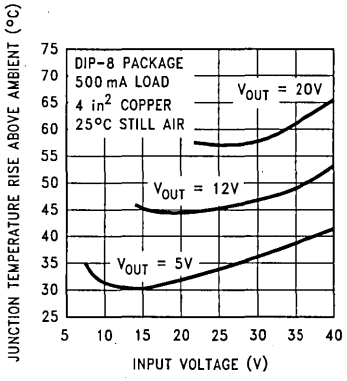
This discussion on open core inductors is not to frighten the user, but to alert the user on what kind of problems to watch out for when using them. Open core bobbin or "stick" inductors are an inexpensive, simple way of making a compact efficient inductor, and they are used by the millions in many different applications.

THERMAL CONSIDERATIONS

The LM2594 is available in two packages, an 8-pin through hole DIP (N) and an 8-pin surface mount SO-8 (M). Both packages are molded plastic with a copper lead frame. When the package is soldered to the PC board, the copper and the board are the heat sink for the LM2594 and the other heat producing components.

For best thermal performance, wide copper traces should be used and all ground and unused pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane (one exception to this is the output (switch) pin, which should not have large areas of copper). Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and even double-sided or multilayer boards provide a better heat path to the surrounding air. Unless power levels are small, sockets are not recommended because of the added thermal resistance it adds and the resultant higher junction temperatures.

Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect the junction temperature. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are, trace width, printed circuit copper area, copper thickness, single- or double-sided, multilayer board, and the amount of solder on the board. The effectiveness of the PC board to dissipate heat also depends on the size, quantity and spacing of other components on the board. Furthermore, some of these components such as the catch diode will add heat to the PC board and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.



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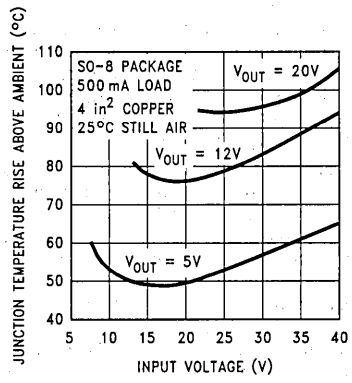
Circuit Data for Temperature Rise Curve (DIP-8)	
Capacitors	Through hole electrolytic
Inductor	Through hole, Schott, 100 μH
Diode	Through hole, 1A 40V, Schottky
PC board	4 square inches single sided 2 oz. copper (0.0028")

FIGURE 19. Junction Temperature Rise, DIP-8

Application Information (Continued)



TL/H/12439–34

Circuit Data for Temperature Rise Curve (Surface Mount)	
Capacitors	Surface mount tantalum, molded "D" size
Inductor	Surface mount, Coilcraft DO33, 100 μH
Diode	Surface mount, 1A 40V, Schottky
PC board	4 square inches single sided 2 oz. copper (0.0028")

FIGURE 20. Junction Temperature Rise, SO-8

The curves shown in *Figures 19* and *20* show the LM2594 junction temperature rise above ambient temperature with a 500 mA load for various input and output voltages. This data was taken with the circuit operating as a buck switcher with all components mounted on a PC board to simulate the junction temperature under actual operating conditions. This curve is typical, and can be used for a quick check on the maximum junction temperature for various conditions, but keep in mind that there are many factors that can affect the junction temperature.

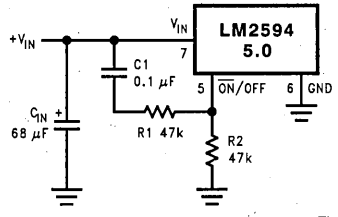


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FIGURE 21. Delayed Startup

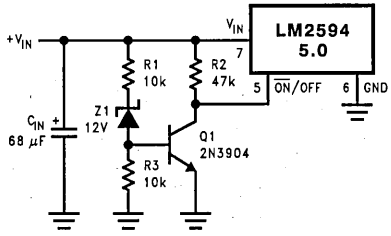

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FIGURE 22. Undervoltage Lockout for Buck Regulator

DELAYED STARTUP

The circuit in *Figure 21* uses the the $\overline{ON}$/OFF pin to provide a time delay between the time the input voltage is applied and the time the output voltage comes up (only the circuitry pertaining to the delayed start up is shown). As the input voltage rises, the charging of capacitor C1 pulls the $\overline{ON}$/OFF pin high, keeping the regulator off. Once the input voltage reaches its final value and the capacitor stops charging, and resistor R_2 pulls the $\overline{ON}$/OFF pin low, thus allowing the circuit to start switching. Resistor R_1 is included to limit the maximum voltage applied to the $\overline{ON}$/OFF pin (maximum of 25V), reduces power supply noise sensitivity, and also limits the capacitor, C1, discharge current. When high input ripple voltage exists, avoid long delay time, because this ripple can be coupled into the $\overline{ON}$/OFF pin and cause problems.

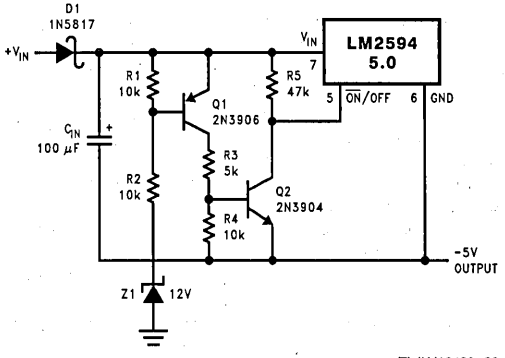
This delayed startup feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the regulator starts operating. Buck regulators require less input current at higher input voltages.

UNDERVOLTAGE LOCKOUT

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. An undervoltage lockout feature applied to a buck regulator is shown in *Figure 22,* while *Figures 23* and *24* applies the same feature to an inverting circuit. The circuit in *Figure 23* features a constant threshold voltage for turn on and turn off (zener voltage plus approximately one volt). If hysteresis is needed, the circuit in *Figure 24* has a turn ON voltage which is different than the turn OFF voltage. The amount of hysteresis is approximately equal to the value of the output voltage. If zener voltages greater than 25V are used, an additional 47 kΩ resistor is needed from the $\overline{ON}$/OFF pin to the ground pin to stay within the 25V maximum limit of the $\overline{ON}$/OFF pin.

INVERTING REGULATOR

The circuit in *Figure 25* converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the regulators ground pin to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.



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This circuit has an ON/OFF threshold of approximately 13V.

FIGURE 23. Undervoltage Lockout for Inverting Regulator

Application Information (Continued)

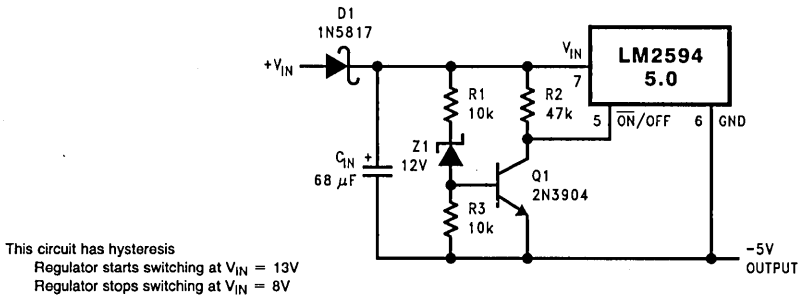


FIGURE 24. Undervoltage Lockout with Hysteresis for Inverting Regulator

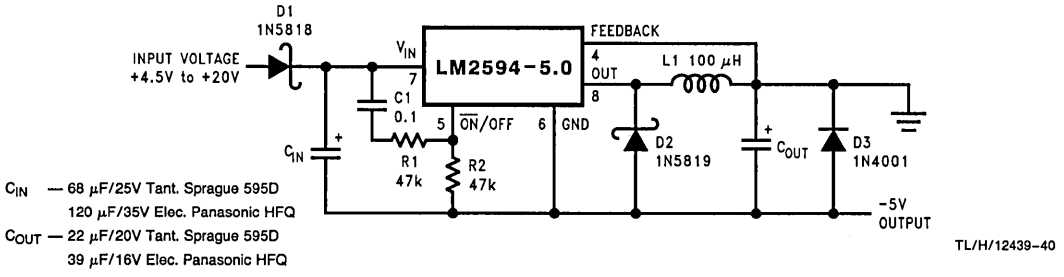


FIGURE 25. Inverting −5V Regulator with Delayed Startup

This example uses the LM2594-5 to generate a −5V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Since this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. The curve shown in *Figure 26* provides a guide as to the amount of output load current possible for the different input and output voltage conditions.

The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40V. For example, when converting +20V to −12V, the regulator would see 32V between the input pin and ground pin. The LM2594 has a maximum input voltage spec of 40V.

Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the C_{IN} capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closley resemble a buck configuration thus providing good closed loop stability. A Schottky diode is recommended for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.

Without diode D3, when the input voltage is first applied, the charging current of C_{IN} can pull the output positive by several volts for a short period of time. Adding D3 prevents the output from going positive by more than a diode voltage.

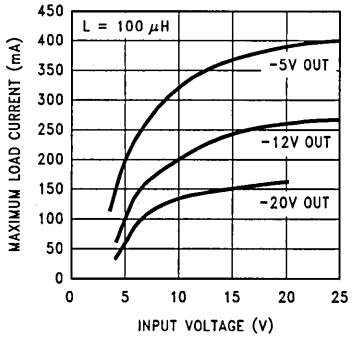


FIGURE 26. Inverting Regulator Typical Load Current

Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a 100 µH, 1A inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in *Figure 25* will provide good results in the majority of inverting designs.

This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2594 current limit (approx 0.8A) are needed for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or

Application Information (Continued)

sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high startup currents required by the inverting topology, the delayed startup feature (C1, R_1 and R_2) shown in *Figure 25* is recommended. By delaying the regulator startup, the input capacitor is allowed to charge up to a higher voltage before the switcher begins operating. A portion of the high input current needed for startup is now supplied by the input capacitor (C_{IN}). For severe start up conditions, the input capacitor can be made much larger than normal.

INVERTING REGULATOR SHUTDOWN METHODS

To use the $\overline{ON}$/OFF pin in a standard buck configuration is simple, pull it below 1.3V (@25°C, referenced to ground) to turn regulator ON, pull it above 1.3V to shut the regulator OFF. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now setting at the negative output voltage level. Two different shutdown methods for inverting regulators are shown in *Figures 27* and *28*.

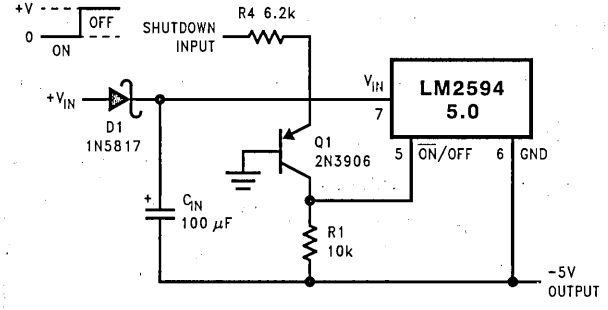


FIGURE 27. Inverting Regulator Ground Referenced Shutdown

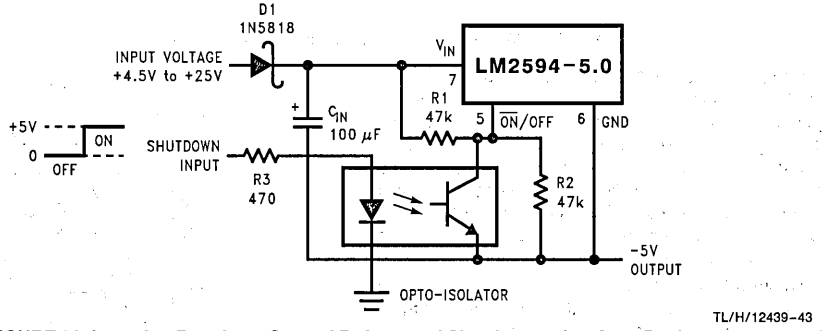
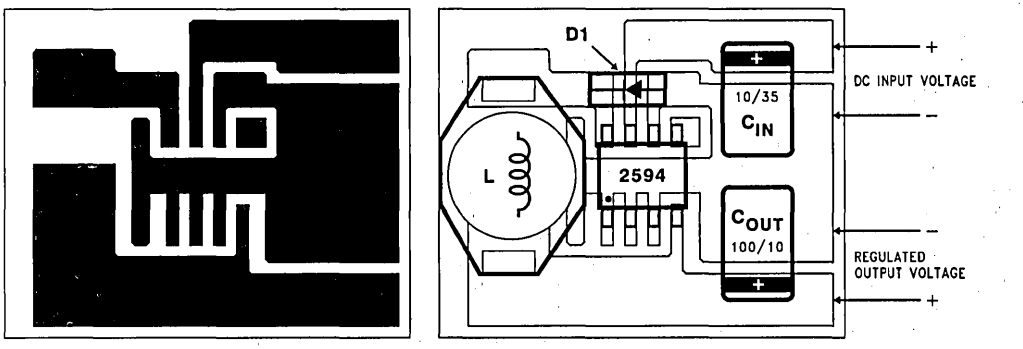


FIGURE 28. Inverting Regulator Ground Referenced Shutdown using Opto Device

Application Information (Continued)

TYPICAL SURFACE MOUNT PC BOARD LAYOUT, FIXED OUTPUT (2X SIZE)



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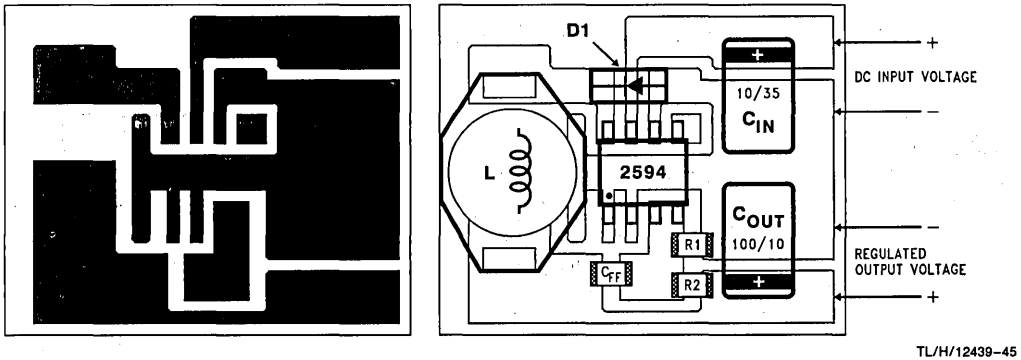
C_{IN} — 10 μF, 35V, Solid Tantalum
AVX, "TPS series"

C_{OUT} — 100 μF, 10V Solid Tantalum
AVX, "TPS series"

D1 — 1A, 40V Schottky Rectifier,
surface mount

L1 — 100 μH, L20, Coilcraft DO33

TYPICAL SURFACE MOUNT PC BOARD LAYOUT, ADJUSTABLE OUTPUT (2X SIZE)



TL/H/12439–45

C_{IN} — 10 μF, 35V, Solid Tantalum
AVX, "TPS series"

C_{OUT} — 100 μF, 10V Solid Tantalum
AVX, "TPS series"

D1 — 1A, 40V Schottky Rectifier, surface
mount

L1 — 100 μH, L20, Coilcraft DO33

R1 — 1 kΩ, 1%

R_2 — Use formula in Design Procedure

C_{FF} — See *Figure 4.*

FIGURE 29. PC Board Layout

National Semiconductor

LM3420-4.2, -8.4, -12.6, -16.8 Lithium-Ion Battery Charge Controller

General Description

The LM3420 series of controllers are monolithic integrated circuits designed for charging and end-of-charge control for Lithium-Ion rechargeable batteries. The LM3420 is available in four fixed voltage versions for one through four cell charger applications (4.2V, 8.4V, 12.6V and 16.8V respectively).

Included in a very small package is an (internally compensated) op amp, a bandgap reference, an NPN output transistor, and voltage setting resistors. The amplifier's inverting input is externally accessible for loop frequency compensation. The output is an open-emitter NPN transistor capable of driving up to 15 mA of output current into external circuitry.

A trimmed precision bandgap reference utilizes temperature drift curvature correction for excellent voltage stability over the operating temperature range. Available with an initial tolerance of 0.5% for the A grade version, and 1% for the standard version, the LM3420 allows for precision end-of-charge control for Lithium-Ion rechargeable batteries.

The LM3420 is available in a sub-miniature 5-lead SOT23-5 surface mount package thus allowing very compact designs.

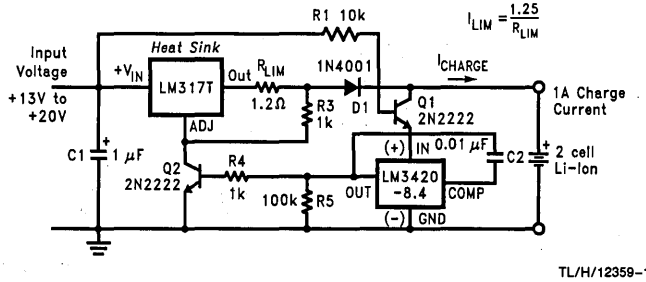
Features

- Voltage options for charging 1, 2, 3 or 4 cells
- Tiny SOT23-5 package
- Precision (0.5%) end-of-charge control
- Drive capability for external power stage
- Low quiescent current, 85 μA (typ.)

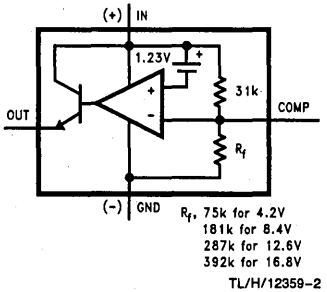
Applications

- Lithium-Ion battery charging
- Suitable for linear and switching regulator charger designs

Typical Application and Functional Diagram



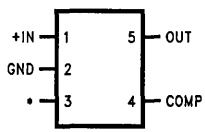
Typical Constant Current/Constant Voltage Li-Ion Battery Charger



LM3420 Functional Diagram

Connection Diagrams and Order Information

5-Lead Small Outline Package (M5)



Top View

Actual Size

TL/H/12359-4

*No internal connection, but should be soldered to PC board for best heat transfer.

For Ordering Information
See *Figure 1* in this Data Sheet
See NS Package Number MA05A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage V(IN)	20V
Output Current	20 mA
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
Vapor Phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Power Dissipation (T_A = 25°C) (Note 2)	300 mW
ESD Susceptibility (Note 3)	
Human Body Model	1500V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for methods on soldering surface-mount devices.

Operating Ratings (Notes 1 and 2)

Ambient Temperature Range	$-40°C \le T_A \le +85°C$
Junction Temperature Range	$-40°C \le T_J \le +125°C$
Output Current	15 mA

LM3420-4.2 Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V(IN) = V_{REG}, V_{OUT} = 1.5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM3420A-4.2 Limit (Note 5)	LM3420-4.2 Limit (Note 5)	Units (Limits)
V_{REG}	Regulation Voltage	I_{OUT} = 1 mA	4.2	4.221/**4.242** 4.179/**4.158**	4.242/**4.284** 4.158/**4.116**	V V(max) V(min)
	Regulation Voltage Tolerance	I_{OUT} = 1 mA		±0.5/±**1**	±1/±**2**	%(max)
I_q	Quiescent Current	I_{OUT} = 1 mA	85	110/**115**	125/**150**	μA μA(max)
G_m	Transconductance $\Delta I_{OUT}/\Delta V_{REG}$	20 μA ≤ I_{OUT} ≤ 1 mA V_{OUT} = 2V	3.3	1.3/**0.75**	1.0/**0.50**	mA/mV mA/mV(min)
		1 mA ≤ I_{OUT} ≤ 15 mA V_{OUT} = 2V	6.0	3.0/**1.5**	2.5/**1.4**	mA/mV mA/mV(min)
A_V	Voltage Gain $\Delta V_{OUT}/\Delta V_{REG}$	1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 200Ω (Note 6)	1000	550/**250**	450/**200**	V/V V/V(min)
		1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 2 kΩ	3500	1500/**900**	1000/**700**	V/V V/V(min)
V_{SAT}	Output Saturation (Note 7)	V(IN) = V_{REG} +100 mV I_{OUT} = 15 mA	1.0	1.2/**1.3**	1.2/**1.3**	V V(max)
I_L	Output Leakage Current	V(IN) = V_{REG} −100 mV V_{OUT} = 0V	0.1	0.5/**1.0**	0.5/**1.0**	μA μA(max)
R_f	Internal Feedback Resistor (Note 8)		75	94 56	94 56	kΩ kΩ(max) kΩ(min)
E_n	Output Noise Voltage	I_{OUT} = 1 mA, 10 Hz ≤ f ≤ 10 kHz	70			μV_{RMS}

LM3420-8.4
Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V(IN) = V_{REG}, V_{OUT} = 1.5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM3420A-8.4 Limit (Note 5)	LM3420-8.4 Limit (Note 5)	Units (Limits)
V_{REG}	Regulation Voltage	I_{OUT} = 1 mA	8.4	8.442/**8.484** 8.358/**8.316**	8.484/**8.568** 8.316/**8.232**	V V(max) V(min)
	Regulation Voltage Tolerance	I_{OUT} = 1 mA		±0.5/±**1**	±1/±**2**	%(max)
I_q	Quiescent Current	I_{OUT} = 1 mA	85	110/**115**	125/**150**	μA μA(max)
G_m	Transconductance $\Delta I_{OUT}/\Delta V_{REG}$	20 μA ≤ I_{OUT} ≤ 1 mA V_{OUT} = 6V	3.3	1.3/**0.75**	1.0/**0.50**	mA/mV mA/mV(min)
		1 mA ≤ I_{OUT} ≤ 15 mA V_{OUT} = 6V	6.0	3.0/**1.5**	2.5/**1.4**	mA/mV mA/mV(min)
A_V	Voltage Gain $\Delta V_{OUT}/\Delta V_{REG}$	1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 470Ω (Note 6)	1000	550/**250**	450/**200**	V/V V/V(min)
		1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 5 kΩ	3500	1500/**900**	1000/**700**	V/V V/V(min)
V_{SAT}	Output Saturation (Note 7)	V(IN) = V_{REG} + 100 mV I_{OUT} = 15 mA	1.0	1.2/**1.3**	1.2/**1.3**	V V(max)
I_L	Output Leakage Current	V(IN) = V_{REG} − 100 mV V_{OUT} = 0V	0.1	0.5/**1.0**	0.5/**1.0**	μA μA(max)
R_f	Internal Feedback Resistor (Note 8)		181	227 135	227 135	kΩ kΩ(max) kΩ(min)
E_n	Output Noise Voltage	I_{OUT} = 1 mA, 10 Hz ≤ f ≤ 10 kHz	140			μV_{RMS}

LM3420-12.6
Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V(IN) = V_{REG}, V_{OUT} = 1.5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM3420A-12.6 Limit (Note 5)	LM3420-12.6 Limit (Note 5)	Units (Limits)
V_{REG}	Regulation Voltage	I_{OUT} = 1 mA	12.6	12.663/**12.726** 12.537/**12.474**	12.726/**12.852** 12.474/**12.348**	V V(max) V(min)
	Regulation Voltage Tolerance	I_{OUT} = 1 mA		±0.5/±**1**	±1/±**2**	%(max)
I_q	Quiescent Current	I_{OUT} = 1 mA	85	110/**115**	125/**150**	μA μA(max)
G_m	Transconductance $\Delta I_{OUT}/\Delta V_{REG}$	20 μA ≤ I_{OUT} ≤ 1 mA V_{OUT} = 10V	3.3	1.3/**0.75**	1.0/**0.5**	mA/mV mA/mV(min)
		1 mA ≤ I_{OUT} ≤ 15 mA V_{OUT} = 10V	6.0	3.0/**1.5**	2.5/**1.4**	mA/mV mA/mV(min)
A_V	Voltage Gain $\Delta V_{OUT}/\Delta V_{REG}$	1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 750Ω (Note 6)	1000	550/**250**	450/**200**	V/V V/V(min)
		1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (**−1.3**) R_L = 10 kΩ	3500	1500/**900**	1000/**700**	V/V V/V(min)
V_{SAT}	Output Saturation (Note 7)	V(IN) = V_{REG} + 100 mV I_{OUT} = 15 mA	1.0	1.2/**1.3**	1.2/**1.3**	V V(max)
I_L	Output Leakage Current	V(IN) = V_{REG} − 100 mV V_{OUT} = 0V	0.1	0.5/**1.0**	0.5/**1.0**	μA μA(max)
R_f	Internal Feedback Resistor (Note 8)		287	359 215	359 215	kΩ kΩ(max) kΩ(min)
E_n	Output Noise Voltage	I_{OUT} = 1 mA, 10 Hz ≤ f ≤ 10 kHz	210			μV_{RMS}

LM3420-16.8
Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, V(IN) = V_{REG}, V_{OUT} = 1.5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM3420A-16.8 Limit (Note 5)	LM3420-16.8 Limit (Note 5)	Units (Limits)
V_{REG}	Regulation Voltage	I_{OUT} = 1 mA	16.8	16.884/**16.968** 16.716/**16.632**	16.968/**17.136** 16.632/**16.464**	V V(max) V(min)
	Regulation Voltage Tolerance	I_{OUT} = 1 mA		±0.5/±**1**	±1/±**2**	%(max)
I_q	Quiescent Current	I_{OUT} = 1 mA	85	110/**115**	125/**150**	μA μA(max)
G_m	Transconductance $\Delta I_{OUT}/\Delta V_{REG}$	20 μA ≤ I_{OUT} ≤ 1 mA V_{OUT} = 15V	3.3	0.8/**0.4**	0.7/**0.35**	mA/mV mA/mV(min)
		1 mA ≤ I_{OUT} ≤ 15 mA V_{OUT} = 15V	6.0	2.9/**0.9**	2.5/**0.75**	mA/mV mA/mV(min)
A_V	Voltage Gain $\Delta V_{OUT}/\Delta V_{REG}$	1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (−**1.3**) R_L = 1 kΩ (Note 6)	1000	550/**250**	450/**200**	V/V V/V(min)
		1V ≤ V_{OUT} ≤ V_{REG} − 1.2V (−**1.3**) R_L = 15 kΩ	3500	1200/**750**	1000/**650**	V/V V/V(min)
V_{SAT}	Output Saturation (Note 7)	V(IN) = V_{REG} + 100 mV I_{OUT} = 15 mA	1.0	1.2/**1.3**	1.2/**1.3**	V V(max)
I_L	Output Leakage Current	V(IN) = V_{REG} − 100 mV V_{OUT} = 0V	0.1	0.5/**1.0**	0.5/**1.0**	μA μA(max)
R_f	Internal Feedback Resistor (Note 8)		392	490 294	490 294	kΩ kΩ(max) kΩ(min)
E_n	Output Noise Voltage	I_{OUT} = 1 mA, 10 Hz ≤ f ≤ 10 kHz	280			μV_{RMS}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The typical thermal resistance (θ_{JA}) when soldered to a printed circuit board is approximately 306°C/W for the M5 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

Note 5: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Averaging Outgoing Quality Level (AOQL).

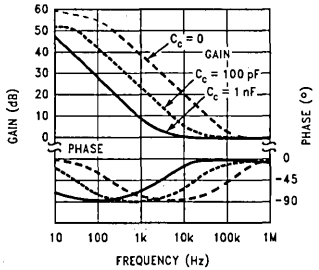
Note 6: Actual test is done using equivalent current sink instead of a resistor load.

Note 7: V_{SAT} = V(IN) − V_{OUT}, when the voltage at the IN pin is forced 100 mV above the nominal regulating voltage (V_{REG}).

Note 8: See Applications and Curves sections for information on this resistor.

Typical Performance Characteristics

4.2V Bode Plot



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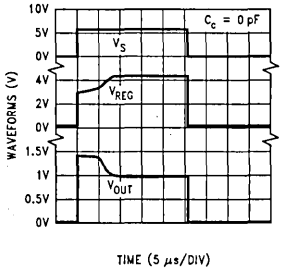
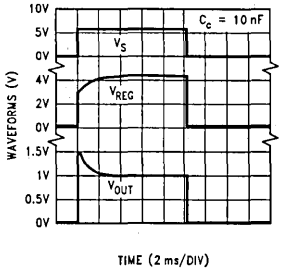
Response Time for 4.2V Version



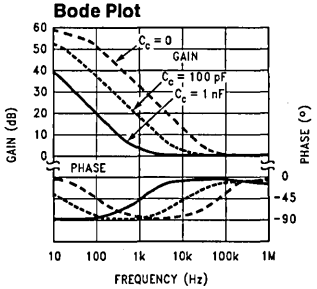
TL/H/12359-18

Response Time for 4.2V Version



TL/H/12359-19

8.4V Bode Plot



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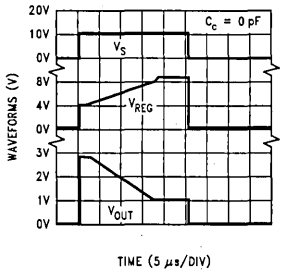
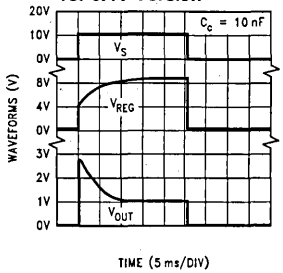
Response Time for 8.4V Version



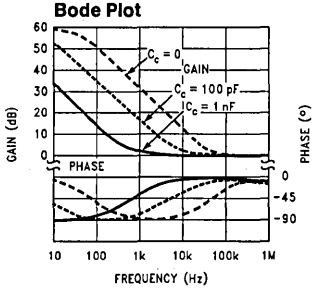
TL/H/12359-21

Response Time for 8.4V Version



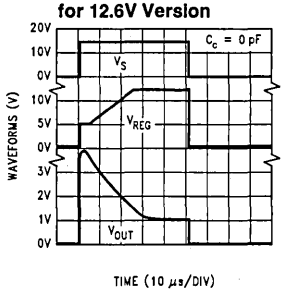
TL/H/12359-22

12.6V Bode Plot



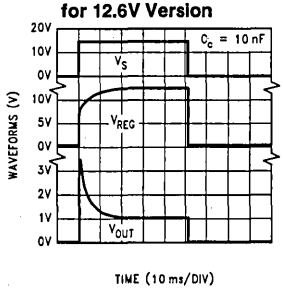
TL/H/12359-23

Response Time for 12.6V Version



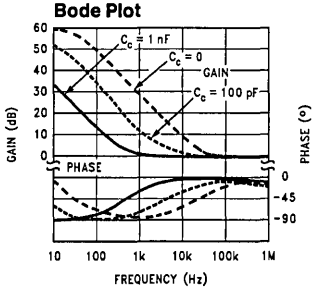
TL/H/12359-24

Response Time for 12.6V Version



TL/H/12359-25

16.8V Bode Plot



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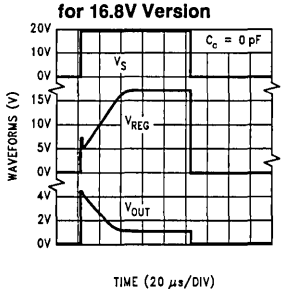
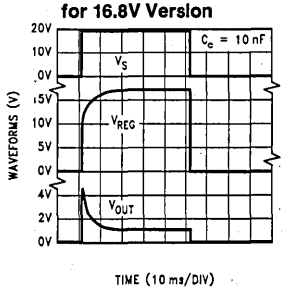
Response Time for 16.8V Version



TL/H/12359-27

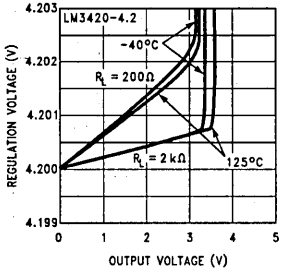
Response Time for 16.8V Version



TL/H/12359-28

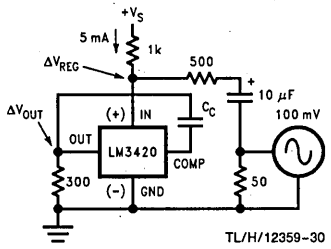
Typical Performance Characteristics (Continued)

Regulation Voltage vs Output Voltage and Load Resistance



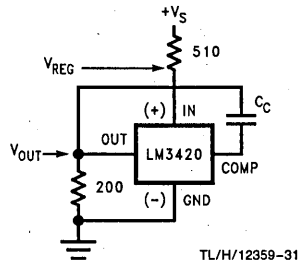
TL/H/12359-29

Circuit Used for Bode Plots



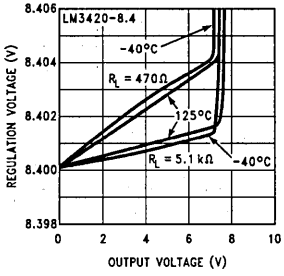
TL/H/12359-30

Circuit Used for Response Time



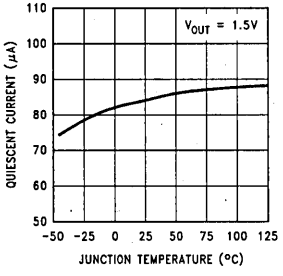
TL/H/12359-31

Regulation Voltage vs Output Voltage and Load Resistance



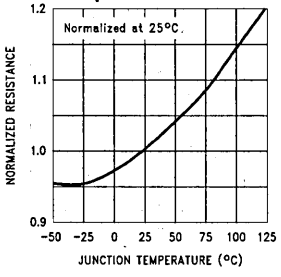
TL/H/12359-32

Quiescent Current



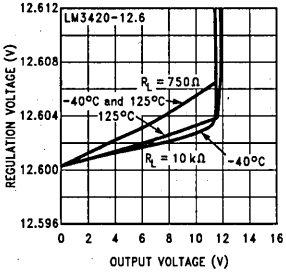
TL/H/12359-33

Internal Feedback Resistor (Rf) Tempco



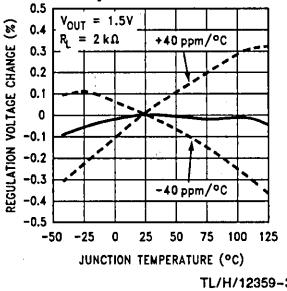
TL/H/12359-34

Regulation Voltage vs Output Voltage and Load Resistance



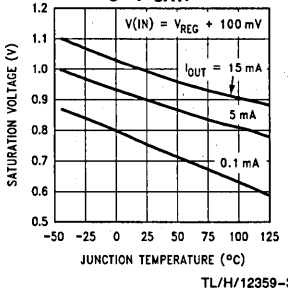
TL/H/12359-35

Normalized Temperature Drift



TL/H/12359-36

Output Saturation Voltage (V_{SAT})



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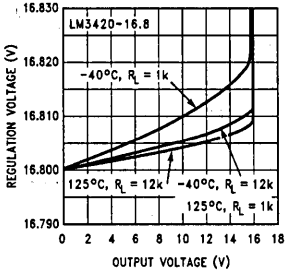
Regulation Voltage vs Output Voltage and Load Resistance



TL/H/12359-38

Five Lead Surface Mount Package Information

The small SOT23-5 package allows only 4 alphanumeric characters to identify the product. The table below contains the field information marked on the package.

Voltage	Grade	Order Information	Package Marking	Supplied as
4.2V	A (Prime)	LM3420AM5-4.2	D02A	250 unit increments on tape and reel
4.2V	A (Prime)	LM3420AM5X-4.2	D02A	3k unit increments on tape and reel
4.2V	B (Standard)	LM3420M5-4.2	D02B	250 unit increments on tape and reel
4.2V	B (Standard)	LM3420M5X-4.2	D02B	3k unit increments on tape and reel
8.4V	A (Prime)	LM3420AM5-8.4	D03A	250 unit increments on tape and reel
8.4V	A (Prime)	LM3420AM5X-8.4	D03A	3k unit increments on tape and reel
8.4V	B (Standard)	LM3420M5-8.4	D03B	250 unit increments on tape and reel
8.4V	B (Standard)	LM3420M5X-8.4	D03B	3k unit increments on tape and reel
12.6V	A (Prime)	LM3420AM5-12.6	D04A	250 unit increments on tape and reel
12.6V	A (Prime)	LM3420AM5X-12.6	D04A	3k unit increments on tape and reel
12.6V	B (Standard)	LM3420M5-12.6	D04B	250 unit increments on tape and reel
12.6V	B (Standard)	LM3420M5X-12.6	D04B	3k unit increments on tape and reel
16.8V	A (Prime)	LM3420AM5-16.8	D05A	250 unit increments on tape and reel
16.8V	A (Prime)	LM3420AM5X-16.8	D05A	3k unit increments on tape and reel
16.8V	B (Standard)	LM3420M5-16.8	D05B	250 unit increments on tape and reel
16.8V	B (Standard)	LM3420M5X-16.8	D05B	3k unit increments on tape and reel

FIGURE 1. SOT23-5 Marking

The first letter "D" identifies the part as a Driver, the next two numbers indicate the voltage, "02" for a 4.2V part, "03" for a 8.4V part, "04" for a 12.6V part, and "05" for a 16.8V part. The fourth letter indicates the grade, "B" for standard grade, "A" for the prime grade.

The SOT23-5 surface mount package is only available on tape in quantity increments of 250 on tape and reel (indicated by the letters "M5" in the part number), or in quantity increments of 3000 on tape and reel (indicated by the letters "M5X" in the part number).

Product Description

The LM3420 is a shunt regulator specifically designed to be the reference and control section in an overall feedback loop of a Lithium-Ion battery charger. The regulated output voltage is sensed between the IN pin and GROUND pin of the LM3420. If the voltage at the IN pin is less than the LM3420 regulating voltage (V_{REG}), the OUT pin sources no current. As the voltage at the IN pin approaches the V_{REG} voltage, the OUT pin begins sourcing current. This current is then used to drive a feedback device, (opto-coupler) or a power device, (linear regulator, switching regulator, etc.) which servos the output voltage to be the same value as V_{REG}.

In some applications, (even under normal operating conditions) the voltage on the IN pin can be forced above the V_{REG} voltage. In these instances, the maximum voltage applied to the IN pin should not exceed 20V. In addition, an external resistor may be required on the OUT pin to limit the maximum current to 20 mA.

Compensation

The inverting input of the error amplifier is brought out to allow overall closed-loop compensation. In many of the applications circuits shown here, compensation is provided by a single capacitor (C_C) connected from the compensation pin to the out pin of the LM3420. The capacitor values shown in the schematics are adequate under most conditions, but they can be increased or decreased depending on the desired loop response. Applying a load pulse to the output of a regulator circuit and observing the resultant output voltage response is an easy method of determining the stability of the control loop.

Analyzing more complex feedback loops requires additional information.

The formula for AC gain at a frequency (f) is as follows;

$$\text{Gain (f)} = 1 + \frac{Z_f(f)}{R_f}$$

$$\text{where } Z_f(f) = \frac{1}{j \bullet 2\pi \bullet f \bullet C_C}$$

where $R_f \approx 75\ k\Omega$ for the 4.2V part, $R_f \approx 181\ k\Omega$ for the 8.4V part, $R_f \approx 287\ k\Omega$ for the 12.6V part, and $R_f \approx 392\ k\Omega$ for the 16.8V part.

The resistor (R_f) in the formula is an internal resistor located on the die. Since this resistor value will affect the phase margin, the worst case maximum and minimum values are important when analyzing closed loop stability. The minimum and maximum room temperature values of this resistor are specified in the Electrical Characteristics section of this data sheet, and a curve showing the temperature coefficient is shown in the curves section. Minimum values of R_f result in lower phase margins.

Test Circuit

The test circuit shown in *Figure 2* can be used to measure and verify various LM3420 parameters. Test conditions are set by forcing the appropriate voltage at the V_{OUT} Set test point and selecting the appropriate R_L or I_{OUT} as specified in the Electrical Characteristics section. Use a DVM at the "measure" test points to read the data.

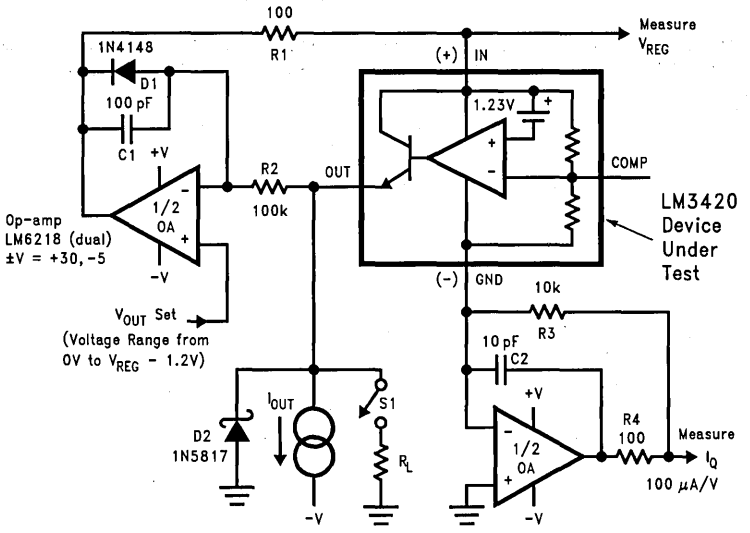


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FIGURE 2. LM3420 Test Circuit

V_{REG} External Voltage Trim

The regulation voltage (V_{REG}) of the LM3420 can be externally trimmed by adding a single resistor from the COMP. pin to the +IN pin or from the COMP. pin to the GND pin, depending on the desired trim direction. Trim adjustments up to ±10% of V_{REG} can be realized, with only a small increase in the temperature coefficient. (See temperature coefficient curve shown below)

Normalized Temperature Drift with Output Externally Trimmed

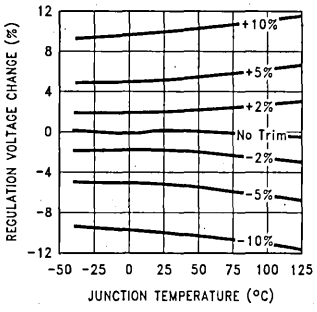

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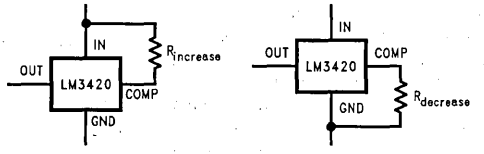
FIGURE 3



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Increasing V_{REG} **Decreasing V_{REG}**

FIGURE 4

Formulas for selecting trim resistor values are shown below.

For LM3420-4.2

$$R_{increase} = \frac{22 \times 10^5}{\%\ increase},$$

$$R_{decrease} = \frac{53 \times 10^5}{\%\ decrease} - 75 \times 10^3$$

For LM3420-8.4

$$R_{increase} = \frac{26 \times 10^5}{\%\ increase},$$

$$R_{decrease} = \frac{154 \times 10^5}{\%\ decrease} - 181 \times 10^3$$

For LM3420-12.6

$$R_{increase} = \frac{28 \times 10^5}{\%\ increase},$$

$$R_{decrease} = \frac{259 \times 10^5}{\%\ decrease} - 287 \times 10^3$$

For LM3420-16.8

$$R_{increase} = \frac{29 \times 10^5}{\%\ increase},$$

$$R_{decrease} = \frac{364 \times 10^5}{\%\ decrease} - 392 \times 10^3$$

Application Information

The LM3420 regulator/driver provides the reference and feedback drive functions for a Lithium-Ion battery charger. It can be used in many different charger configurations using both linear and switching topologies to provide the precision needed for charging Lithium-Ion batteries safely and efficiently. Output voltage tolerances better than 0.5% are possible without using trim pots or precision resistors. The circuits shown are designed for 2 cell operation, but they can readily be changed for either 1, 3 or 4 cell charging applications.

One item to keep in mind when designing with the LM3420 is that there are parasitic diodes present. In some designs, under special electrical conditions, unwanted currents may flow. Parasitic diodes exist from OUT to IN, as well as from GROUND to IN. In both instances the diode arrow is pointed toward the IN pin.

Application Circuits

The circuit shown in *Figure 5* performs constant-current, constant-voltage charging of two Li-Ion cells. At the beginning of the charge cycle, when the battery voltage is less than 8.4V, the LM3420 sources no current from the OUT pin, keeping Q2 off, thus allowing the LM317 Adjustable voltage regulator to operate as a constant-current source. (The LM317 is rated for currents up to 1.5A, and the LM350 and LM338 can be used for higher currents.) The LM317 forces a constant 1.25V across R_{LIM}, thus generating a constant current of

$$I_{LIM} = \frac{1.25V}{R_{LIM}}$$

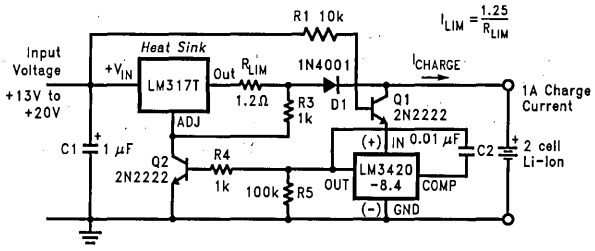

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FIGURE 5. Constant Current/Constant Voltage LI-Ion Battery Charger

Application Circuits (Continued)

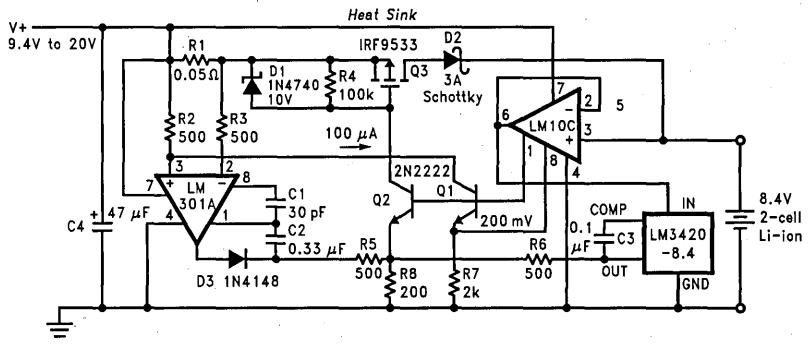

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FIGURE 6. Low Drop-Out Constant Current/Constant Voltage 2-Cell Charger

Transistor Q1 provides a disconnect between the battery and the LM3420 when the input voltage is removed. This prevents the 85 μA quiescent current of the LM3420 from eventually discharging the battery. In this application Q1 is used as a low offset saturated switch, with the majority of the base drive current flowing through the collector and crossing over to the emitter as the battery becomes fully charged. It provides a very low collector to emitter saturation voltage (approximately 5 mV). Diode D1 is also used to prevent the battery current from flowing through the LM317 regulator from the output to the input when the DC input voltage is removed.

As the battery charges, its voltage begins to rise, and is sensed at the IN pin of the LM3420. Once the battery voltage reaches 8.4V, the LM3420 begins to regulate and starts sourcing current to the base of Q2. Transistor Q2 begins controlling the ADJ. pin of the LM317 which begins to regulate the voltage across the battery and the constant voltage portion of the charging cycle starts. Once the charger is in the constant voltage mode, the charger maintains a regulated 8.4V across the battery and the charging current is dependent on the state of charge of the battery. As the cells approach a fully charged condition, the charge current falls to a very low value.

Figure 6 shows a Li-Ion battery charger that features a drop-out voltage of less than one volt. This charger is a constant-current, constant-voltage charger (it operates in constant-current mode at the beginning of the charge cycle and switches over to a constant-voltage mode near the end of the charging cycle). The circuit consists of two basic feedback loops. The first loop controls the constant charge current delivered to the battery, and the second determines the final voltage across the battery.

With a discharged battery connected to the charger, (battery voltage is less than 8.4V) the circuit begins the charge cycle with a constant charge current. The value of this current is set by using the reference section of the LM10C to force 200 mV across R7 thus causing approximately 100 μA of emitter current to flow through Q1, and approximately 1 mA of emitter current to flow through Q2. The collector current of Q1 is also approximately 100 μA, and this current flows through R2 developing 50 mV across it. This 50 mV is used as a reference to develop the constant charge current through the current sense resistor R1.

The constant current feedback loop operates as follows. Initially, the emitter and collector current of Q2 are both approximately 1 mA, thus providing gate drive to the MOSFET Q3, turning it on. The output of the LM301A op-amp is low. As Q3's current reaches 1A, the voltage across R1 approaches 50 mV, thus canceling the 50 mV drop across R2, and causing the op-amp's output to start going positive, and begin sourcing current into R8. As more current is forced into R8 from the op-amp, the collector current of Q2 is reduced by the same amount, which decreases the gate drive to Q3, to maintain a constant 50 mV across the 0.05Ω current sensing resistor, thus maintaining a constant 1A of charge current.

The current limit loop is stabilized by compensating the LM301A with C1 (the standard frequency compensation used with this op-amp) and C2, which is additional compensation needed when D3 is forward biased. This helps speed up the response time during the reverse bias of D3. When the LM301A output is low, diode D3 reverse biases and prevents the op-amp from pulling more current through the emitter of Q2. This is important when the battery voltage reaches 8.4V, and the 1A charge current is no longer needed. Resistor R5 isolates the LM301A feedback node at the emitter of Q2.

The battery voltage is sensed and buffered by the op-amp section of the LM10C, connected as a voltage follower driving the LM3420. When the battery voltage reaches 8.4V, the LM3420 will begin regulating by sourcing current into R8, which controls the collector current of Q2, which in turn reduces the gate voltage of Q3 and becomes a constant voltage regulator for charging the battery. Resistor R6 isolates the LM3420 from the common feedback node at the emitter of Q2. If R5 and R6 are omitted, oscillations could occur during the transition from the constant-current to the constant-voltage mode. D2 and the PNP transistor input stage of the LM10C will disconnect the battery from the charger circuit when the input supply voltage is removed to prevent the battery from discharging.

Application Circuits (Continued)

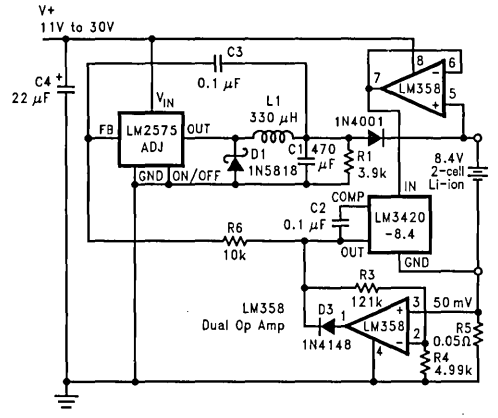

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FIGURE 7. High Efficiency Switching Regulator Constant Current/Constant Voltage 2-Cell Charger

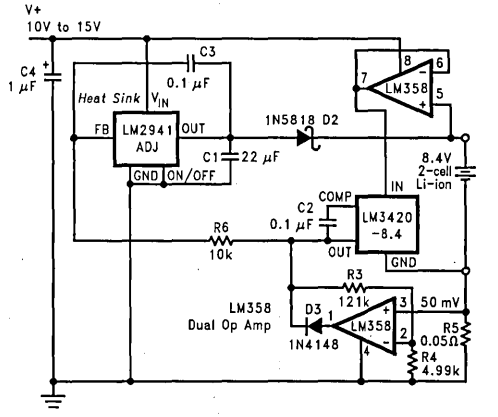

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FIGURE 8. Low Dropout Constant Current/Constant Voltage Li-Ion Battery Charger

A switching regulator, constant-current, constant-voltage two-cell Li-Ion battery charging circuit is shown in *Figure 7.* This circuit provides much better efficiency, especially over a wide input voltage range than the linear topologies. For a 1A charger an LM2575-ADJ. switching regulator IC is used in a standard buck topology. For other currents, or other packages, other members of the SIMPLE SWITCHER® buck regulator family may be used.

Circuit operation is as follows. With a discharged battery connected to the charger, the circuit operates as a constant current source. The constant-current portion of the charger is formed by the loop consisting of one half of the LM358 op amp along with gain setting resistors R3 and R4, current sensing resistor R5, and the feedback reference voltage of 1.23V. Initially the LM358's output is low causing the output of the LM2575-ADJ. to rise thus causing some charging current to flow into the battery. When the current reaches 1A, it is sensed by resistor R5 (50 mΩ), and produces 50 mV. This 50 mV is amplified by the op-amps gain of 25 to produce 1.23V, which is applied to the feedback pin of the LM2575-ADJ. to satisfy the feedback loop.

Once the battery voltage reaches 8.4V, the LM3420 takes over and begins to control the feedback pin of the LM2575-ADJ. The LM3420 now regulates the voltage across the battery, and the charger becomes a constant-voltage charger. Loop compensation network R6 and C3 ensure stable operation of the charger circuit under both constant-current and constant-voltage conditions. If the input supply voltage is removed, diode D2 and the PNP input stage of the LM358 become reversed biased and disconnects the battery to ensure that the battery is not discharged. Diode D3 reverse biases to prevent the op-amp from sinking current when the charger changes to constant voltage mode.

The minimum supply voltage for this charger is approximately 11V, and the maximum is around 30V (limited by the 32V maximum operating voltage of the LM358). If another op-amp is substituted for the LM358, make sure that the input common-mode range of the op-amp extends down to ground so that it can accurately sense 50 mV. R1 is included to provide a minimum load for the switching regulator to assure that switch leakage current will not cause the output to rise when the battery is removed.

The circuit in *Figure 8* is very similar to *Figure 7,* except the switching regulator has been replaced with a low dropout linear regulator, allowing the input voltage to be as low as 10V. The constant current and constant voltage control loops are the same as the previous circuit. Diode D2 has been changed to a Schottky diode to provide a reduction in the overall dropout voltage of this circuit, but Schottky diodes typically have higher leakage currents than a standard silicon diode. This leakage current could discharge the battery if the input voltage is removed for an extended period of time.

Another variation of a constant current/constant voltage switch mode charger is shown in *Figure 9.* The basic feedback loops for current and voltage are similar to the previous circuits. This circuit has the current sensing resistor, for the constant current part of the feedback loop, on the positive side of the battery, thus allowing a common ground between the input supply and the battery. Also, the LMC7101 op-amp is available in a very small SOT23-5 package thus allowing a very compact pc board design. Diode D4 prevents the battery from discharging through the charger circuitry if the input voltage is removed, although the quiescent current of the LM3420 will still be present (approximately 85 µA).

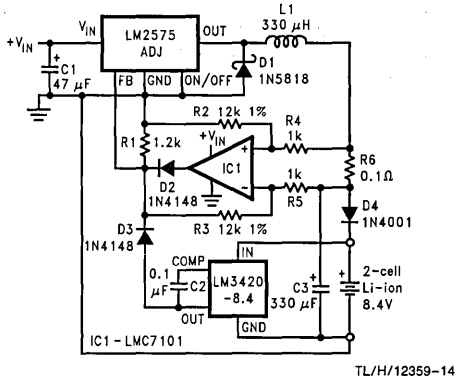

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FIGURE 9. High Efficiency Switching Charger with High Side Current Sensing

Application Circuits (Continued)

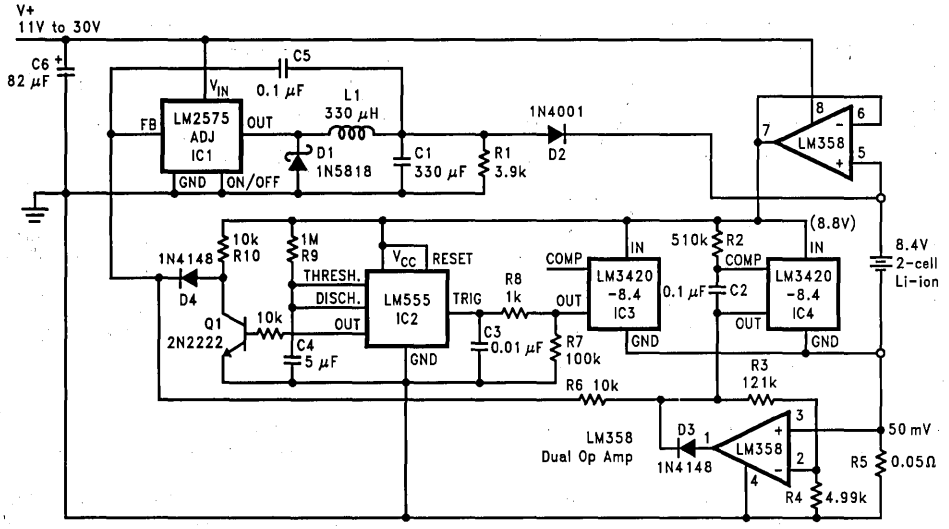

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FIGURE 10. (Fast) Pulsed Constant Current 2-Cell Charger

A rapid charge Lithium-Ion battery charging circuit is shown in *Figure 10.* This configuration uses a switching regulator to deliver the charging current in a series of constant current pulses. At the beginning of the charge cycle (constant-current mode), this circuit performs identically to the previous LM2575 charger by charging the battery at a constant current of 1A. As the battery voltage reaches 8.4V, this charger changes from a constant continuous current of 1A to a 5 second pulsed 1A. This allows the total battery charge time to be reduced considerably. This is different from the other charging circuits that switch from a constant current charge to a constant voltage charge once the battery voltage reaches 8.4V. After charging the battery with 1A for 5 seconds, the charge stops, and the battery voltage begins to drop. When it drops below 8.4V, the LM555 timer again starts the timing cycle and charges the battery with 1A for another 5 seconds. This cycling continues with a constant 5 second charge time, and a variable off time. In this manner, the battery will be charged with 1A for 5 seconds, followed by an off period (determined by the battery's state of charge), setting up a periodic 1A charge current. The off time is determined by how long it takes the battery voltage to decrease back down to 8.4V. When the battery first reaches 8.4V, the off time will be very short (1 ms or less), but when the battery approaches full charge, the off time will begin increasing to tens of seconds, then minutes, and eventually hours.

The constant-current loop for this charger and the method used for programming the 1A constant current is identical to the previous LM2575-ADJ. charger. In this circuit, a second LM3420-8.4 has its V_{REG} increased by approximately 400 mV (via R2), and is used to limit the output voltage of the charger to 8.8V in the event of a bad battery connection, or the battery is removed or possibly damaged.

The LM555 timer is connected as a one-shot, and is used to provide the 5 second charging pulses. As long as the battery voltage is less than the 8.4V, the output of IC3 will be held low, and the LM555 one-shot will never fire (the output of the LM555 will be held high) and the one-shot will have no effect on the charger. Once the battery voltage exceeds the 8.4V regulation voltage of IC3, the trigger pin of the LM555 is pulled high, enabling the one shot to begin timing. The charge current will now be pulsed into the battery at a 5 second rate, with the off time determined by the battery's state of charge. The LM555 output will go high for 5 seconds (pulling down the collector of Q1) which allows the 1A constant-current loop to control the circuit.

Application Circuits (Continued)

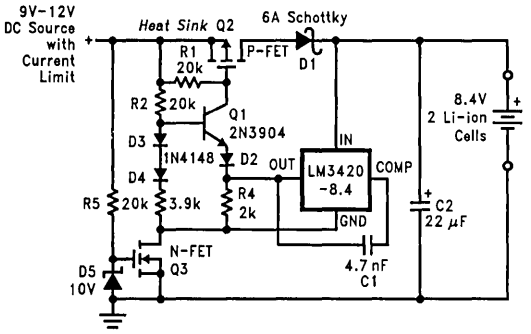

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FIGURE 11. MOSFET Low Dropout Charger

Figure 11 shows a low dropout constant voltage charger using a MOSFET as the pass element, but this circuit does not include current limiting. This circuit uses Q3 and a Schottky diode to isolate the battery from the charging circuitry when the input voltage is removed, to prevent the battery from discharging. Q2 should be a high current (0.2Ω) FET, while Q3 can be a low current (2Ω) device.

Note: Although the application circuits shown here have been built and tested, they should be thoroughly evaluated with the same type of battery the charger will eventually be used with.

Different battery manufacturers may use a slightly different battery chemistry which may require different charging characteristics. Always consult the battery manufacturer for information on charging specifications and battery details, and always observe the manufacturers precautions when using their batteries. Avoid overcharging or shorting Lithium-Ion batteries.

Section 8

Complete Cordless Phone Solution

Section 8 Contents

National Semiconductor

PRELIMINARY

NCL354
Cordless Telephone IC

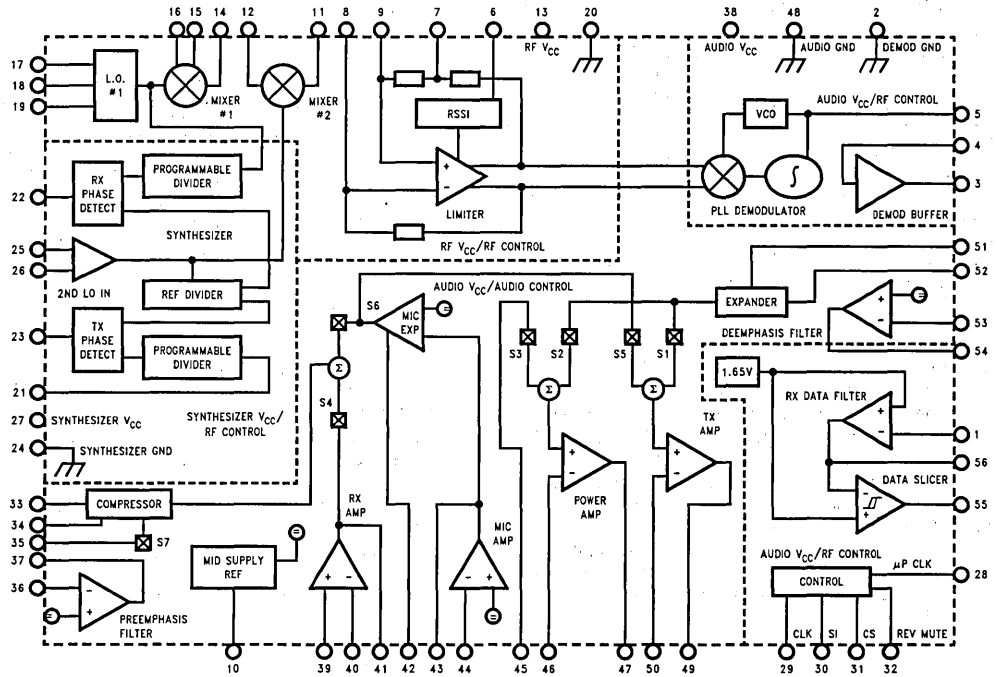
General Description

The NCL354 combines a high performance, dual conversion superheterodyne VHF radio receiver with the audio processing functions required to build a full featured narrow band FM cordless telephone system. Superior RF sensitivity, combined with advanced audio channel signal pre-emphasis/de-emphasis and compression/expansion processing, creates a high performance communications system with excellent noise characteristics and wide dynamic range. The built-in receive signal strength indicator (RSSI) allows for easy identification of channels which are not suitable for use or monitoring of the signal strength on the selected channel. A built-in phase locked loop (PLL) discriminator provides for low distortion demodulation of signals which have a wide dynamic range while eliminating the need for external adjustments. A microphone expander circuit reduces the transmitted background noise during silent periods, and enhanced power supply management techniques extend battery life. The audio portion includes digitally selected analog switches which allow the designer to easily incorporate speaker-phone and intercom features.

Features

- Low supply voltage 3V–5V
- Dual conversion receiver 46 MHz/49 MHz
- Companded audio channel 60 dB
- Microphone expander
- PLL discriminator
- Receive signal strength indicator for channel selection
- Highly selective filter for data reception
- Speaker phone and intercom capabilities
- Universal transmit and receive frequency synthesizers
- Battery saving features:
  - I_{CC} = 50 μA in standby state
  - I_{CC} = 5.5 mA in sniff mode
  - I_{CC} = 13 mA in communication mode
- Available in 56-pin TSSOP package

NCL354 Block Diagram



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1.0 Pin Names and Functions

Function	Name	Note	Pin #
RF Power	VCCRF		13
RF Ground	RFGND		20
Audio Power	VCCAUD		38
Audio Ground	AUDGND		48
Synthesizer Power	VCCSYNTH		27
Synthesizer GND	SYNTHGND		24
Demodulator Buffer Out	DMDOUT		3
Demodulator Buffer In	DMDIN		4
Demodulator Loop Filter	DMDFILT		5
Demodulator Ground	DMDGND		2
Expander Input	EXPIN		52
Expand Filter Cap	EXPCAP	C_{ext} = 2.2 µF	51
Deemphasis In	DEEMIN		53
Deemphasis Out	DEEMOUT		54
Data Filter In	DFIN		1
Data Filter Out	DFOUT		56
Data Slicer Out	RXDATA		55
Chip Select	CS	Active Hi, CMOS Levs	31
Serial In	SI	CMOS Levs	30
Serial Clock	CLKIN	CMOS Levs	29
Clock Out	CLKOUT	CMOS Levs	28
Receive Mute	RCVMUT	CMOS Levs	32
Hyb TX Amp +Out	HYTXOTP		49
Hyb TX Amp −In	HYTXIN		50
Auxilliary Amp Out	PAOUT		47
Auxilliary Amp −In	PAIN		46
Mic Amp −In	MICIN		44
Mic Amp Out	MICOUT		43

Function	Name	Note	Pin #
Speakerphone RX	SPKPHRX		45
Hybrid RX Amp Out	HYRXOUT		41
Hybrid RX Amp −In	HYRXINN		40
Hybrid RX Amp +In	HYRXINP		39
Mic Expander Filter Cap	MEXPCAP	C_{ext} = 0.4 µF	42
Int. Reference Bypass	IREFBYP	C_{ext} = 0.1 µF	10
Preemphasis −In	PREEMIN		36
Preemphasis Out	PREEMOT		37
Compressor Output	COMPOUT		33
Compressor Filter Cap	COMPCAP	C_{ext} = 2.2 µF	34
Compressor Error Cap	CPERCAP	C_{ext} = 1 µF	35
LO1	LO1A		17
LO1	LO1B		19
Varactor	VARAC		18
Mixer1 RF In1	MX1RFIN1		16
Mixer1 RF In2	MX1RFIN2		15
Mixer1 Out	MX1OUT		14
Mixer2 RF In	MX2RFIN		12
Mixer2 Out	MX2OUT		11
Limiter +In	LIMINP		9
Limiter −In	LIMINN		8
Limiter Bypass	LIMBYP		7
RSSI	RSSI		6
LO2 IN	LO2IN		25
LO2 OUT	LO2OUT	CMOS Levs	26
Receive Loop Phase Det	RXPD		22
Transmit Loop Phase Det	TXPD		23
Transmit RF In	TXRFIN		21
TOTAL			56

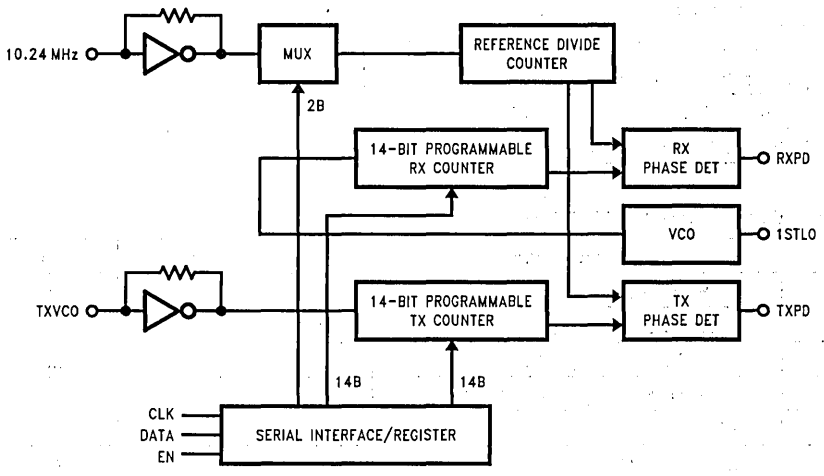
Frequency Synthesizer

The frequency synthesizer architecture (shown in *Figure 1*) uses two phase-locked loops to generate transmit and receive mix frequencies for most country channels; including US (25ch), China, Spain, France, Korea, New Zealand, U.K., Netherlands, and Australia. The frequencies are programmed through the microprocessor serial interface and a on board ROM. The 2nd LO and reference divider provides the reference frequencies for both transmit and receive loops. This synthesizer contains separate 14-bit dividers and phase detectors for each loop. In addition, the varactor for the 1st LO is on chip with two pins for connection to an external tank circuit.

Power Management

To maximize battery life, the NCL354 handset has 2 power down modes of operation. In Standby mode, all power is turned off except for the data registers so that logic control states are preserved. Power down is done in a manner that preserves the charge in all external capacitors. This minimizes the cycle time needed to restore operation, and eliminates the current needed to recharge the capacitors. Standby current is < 50 µA. In Sniff mode only those circuits needed to detect an incoming ring signal are turned on. This includes the RF section, Receive Synthesizer, and Data detector. In this mode, supply current is < 5.5 mA.

1.0 Pin Names and Functions (Continued)



TL/W/12474-2

FIGURE 1. Block Diagram of Serial Interface and Frequency Synthesizer

2.0 Receiver System Characteristics (1st and 2nd IF Mixers, Limiter, RSSI, and PLL)

T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_O = 50 MHz, Δ f_O = ±1.0 kHz, C Message Weight, fmod = 1.0 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
P_{SIN}	RF Input for 12 dB SINAD	Measured @ Deemphasis Out Matched Input, w/C-message Weighting RF $V_{CC} \geq$ 3.0 V_{DC}		−110		dBm
THD	Total Harmonic Distortion			0.1	1.5	%
BW_{DEMOD}	Demodulation Bandwidth		20			kHz
	Ultimate Quieting	Measured @ Deemphasis Out w/C-message Weighting fmod = 1 kHz fdev = 1 kHz		35		dB
	AM to PM Conversion	Measured @ Deemphasis Out RF = −60 dBm, AM = 30% fmod = 1 kHz		−30	−20	dB

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3.0 Electrical Specifications

3.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristic	Maximum	Units
RF V_{CC}	RF Supply Voltage	5.5	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage	5.5	V_{DC}
T_J	Junction Temperature	150	°C
T_{STJ}	Storage Temperature	−50 to +150	°C

3.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Min	Typ	Max	Units
RF V_{CC}	RF Supply Voltage	3.0		5.0	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage (Base)	3.0		5.0	V_{DC}
AUDIO V_{CC}	Audio Supply Voltage (Handset)	3.0		5.0	V_{DC}
T_A	Ambient Operating Temperature Range	−30	+25	+80	°C
F_{RF}	RF Input Frequency		49	80	MHz
F_{if1}	Maximum 1st IF		10.7	23	MHz
F_{if2}	Maximum 2nd IF		0.455	3	MHz

3.3 RECEIVER CHARACTERISTICS (1st and 2nd IF Mixers, Limiter, RSSI, and PLL)
T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_O = 50 MHz, Δf_O = ±1.0 kHz, C Message Weight, f_{mod} = 1.0 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
I_{CC}	Drain Current	No Input Signal, RF V_{CC} Enabled		4.2		mAdc
I_{CC}	Drain Current	No Input Signal, RF V_{CC} Disabled		20	100	μAdc

3.3.1 1st Mixer Characteristics T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_{rf} = 50 MHz, f_{lo} = 40 MHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
G_{MC1}	1st Mixer Conversion Voltage Gain	Loaded by 330Ω f_{rf} = 50 MHz f_{lo} = 40 MHz	11	15		dB
Z_{out1st}	1st Mixer Output Impedance	f_O = 10 MHz		330		Ω
Z_{in1st}	1st Mixer RF Input Impedance	f_{rf} = 50 MHz		2k		kΩ
V_{n1stm}	1st Mixer Input Noise Voltage	Referenced to 1st Mixer Input as an Amplifier		14		$nV/\sqrt{Hz}$
	1st Mixer LO Output Feedthrough	Measured @ 1st Mixer Output		28		dB
	1st Mixer LO Input Feedthrough	Measured @ 1st Mixer Input		28		dB
I_{P3m1}	1st Mixer 3rd Order Intercept	Referenced to 1st Mixer Input		30		mVrms
	1st Mixer 1dB Compression Point	Referenced to 1st Mixer Input		10		mVrms

3.0 Electrical Specifications (Continued)

3.3.2 2nd Mixer Characteristics T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_{rf} = 10.695 MHz, f_{lo} = 10.24 MHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
ZinRF2nd	2nd Mixer RF Input Impedance	f_{rf} = 10.695 MHz		330		Ω
Zout2nd	2nd Mixer Output Impedance	f_O = 455 kHz		1.5		kΩ
GMC2	2nd Mixer Conversion Voltage Gain	Loaded by 1.5 kΩ f_{rf} = 10.695 MHz f_{lo} = 10.24 MHz	10	15		dB
ZinLO2nd	2nd Mixer LO Input Impedance	f_{lo} = 10.24 MHz	20k			Ω
Vn2ndM	2nd Mixer Noise Voltage	Referenced to 2nd Mixer Input as an Amplifier		9		$nV/\sqrt{Hz}$
	2nd Mixer LO Output Feedthrough	Measured @ 2nd Mixer Output		40		dB
	2nd Mixer LO Input Feedthrough	Measured @ 2nd Mixer Input		40		dB
IP3m2	2nd Mixer 3rd Order Intercept	Referenced to 2nd Mixer Input		30		mVrms
	2nd Mixer 1 dB Compression Point	Referenced to 2nd Mixer Input		10		mVrms

3.3.3 Limiter Characteristics T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_O = 455 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
	Limiter Voltage Gain			90		dB
	Limiter Input Noise Voltage	Referenced to Limiter Input		20		$nV/\sqrt{Hz}$
	Limiter Output Voltage Swing			400		mV_{PP}
BWlim	Limiter −3 dB Bandwidth			2		MHz
SENSlmt	Limiter Sensitivity	For 12 dB sinad @ DEOUT		25		μVrms

3.3.4 RSSI Characteristics T_A = 25°C, RF V_{CC} = 3.3 V_{DC}, f_O = 455 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
DRRSSI	RSSI Dynamic Range (Logarithmic Response)			60		dB
	RSSI Voltage Output	Limiter in = 10 μVrms Limiter in = 10 mVrms		0.2 1.2		V
	RSSI Attack Time				100	μs
	RSSI Decay Time				100	μs

3.3.5 PLL Demodulator Characteristics
T_A = 25°C, Audio V_{CC} = 3.3 V_{DC}, f_O = 455 kHz, Δf_O = ±1.0 kHz, C Message Weight, f_{mod} = 1.0 kHz

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
ko	VCO Gain			100		kHz/V
kd	Phase Detector Gain			0.20		μA/□
kv	PLL Open Loop Gain			360×10^3		1/s
f_c	VCO Center Frequency	Open Loop	398	455	512	kHz

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3.0 Electrical Specifications (Continued)

3.4 AUDIO CHARACTERISTICS T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
Audio V_{CC} Enabled	Drain Current	I_{CCA}		8		mAdc
Audio V_{CC} Disabled	Drain Current	I_{CCA}		20	100	μAdc
From Enable Transition	Audio Switch Time	$t_{S1 \ldots S7}$			0.5	ms
	Audio Switch Isolation	$I_{S1 \ldots S7}$	65			dB
	Audio Switch Loss	L_{SW}			0.5	dB

3.4.1 Compressor Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	$V_{IN} \leq V_{IMAX}$ @ 1 kHz		0.5	1.0	%
G_{CO}	0 dB Gain	V_{IN} = 90 mVrms	−1.5	0	1.5	dB
t_{Ca}	Attack Time	G_{CO}, COMPCAP = 2.2 μF		6		ms
t_{Cd}	Decay Time	G_{CO}, COMPCAP = 2.2 μF		22		ms
G_T	Gain Tracking Linearity	11 dB > G_C > −20 dB	−2		+2	dB
PBW	Power Bandwidth	Unity Gain	10			kHz
DR_{IN}	Input Dynamic Range		−40		+22	dB
DR_{OUT}	Output Dynamic Range		−20		+11	dB
Vimax	Maximum Input Voltage Swing	f_O = 1 kHz		V_{CC} − 0.4	V_{CC} − 0.2	V_{PP}
Vomax	Maximum Output Voltage Swing	f_O = 1 kHz	V_{CC} − 2.0	V_{CC} − 1.6		V_{PP}
f_{lo}	Low Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB, CPERCAP = 1.0 μF $V_{IN} = G_{C0}$			180	Hz
f_{hi}	High Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB	4			kHz

3.4.2 Expander Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	$V_O \leq$ Vomax @ 1 kHz		0.5	1.0	%
G_{EO}	0 dB Gain	V_{IN} = 90 mVrms	−7.5	−6	−4.5	dB
t_{Ea}	Attack Time	G_{EO}, EXPCAP = 2.2 μF		19		ms
t_{Ed}	Decay Time	G_{EO}, EXPCAP = 2.2 μF		22		ms
G_T	Gain Tracking Linearity	11 dB > G_E > −20 dB	−2		+2	dB
PBW	Power Bandwidth	Unity Gain	10			kHz
DR_{IN}	Input Dynamic Range		−20		+11	dB
DR_{OUT}	Output Dynamic Range		−46		+16	dB
Vimax	Maximum Input Voltage Swing	f_O = 1 kHz		V_{CC} − 0.4	V_{CC} − 1.6	V_{PP}
Vomax	Maximum Output Voltage Swing	f_O = 1 kHz	V_{CC} − 2.0			V_{PP}
f_{lo}	Low Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB			180	Hz
f_{hi}	High Frequency Roll-Off	$G_{C(F)} = G_C$(1 kHz) − 3 dB $V_{IN} = G_{C0}$	4			kHz

3.0 Electrical Specifications (Continued)

3.4.3 Deemphasis Filter Op Amp Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain		2 × R_L			V/V
GBW	Gain-Bandwidth Product			200		kHz
Vinmax	Maximum Input Voltage Swing	A_{CL} = 10 dB			V_{CC} − 1.6	V_{PP}
Voutmax	Maximum Output Voltage Swing	A_{CL} = 10 dB	V_{CC} − 2.0			V_{PP}
I_B	Input Bias Current				200	nA
Requiv	Equivalent External DC Resistance for Minimal Input Offset to Expander			13.2		kΩ

3.4.4 TX Amplifier Characteristics T_A = 25°C

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
T_D	Total Distortion	f_O = 4 kHz		0.5	1.0	%
Handset Application, Inductive Earpiece, Audio V_{CC} = 3.6 V_{DC}						
Vinmax	Maximum Input Voltage Swing (1st Amp)	f_O = 4 kHz			V_{CC} − 1.6	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	f_O = 4 kHz	V_{CC} − 2.0			V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	f_O = 4 kHz			V_{CC} − 1.6	
Vomax	Maximum Output Voltage Swing (2nd Amp)	f_O = 4 kHz	V_{CC} − 2.0			V_{PP}
Z_L	Differential Ended Output Load			270		Ω
Handset Application, Ceramic Earpiece, Audio V_{CC} = 3.6 V_{DC}						
Vinmax	Maximum Input Voltage Swing (1st Amp)	f_O = 4 kHz			V_{CC} − 1.6	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	f_O = 4 kHz	V_{CC} − 1.0	V_{CC} − 0.6		V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	f_O = 4 kHz			V_{CC} − 0.2	
Vomax	Maximum Output Voltage Swing (2nd Amp)	f_O = 4 kHz	V_{CC} − 1.0	V_{CC} − 0.6		V_{PP}
Z_L	Differential Ended Output Load			1000		Ω
Base Application, Audio V_{CC} = 5 V_{DC}						
Vinmax	Maximum Input Voltage Swing (1st Amp)	f_O = 4 kHz			1.9	V_{PP}
Vomax	Maximum Output Voltage Swing (1st Amp)	f_O = 4 kHz	3			V_{PP}
Vinmax	Maximum Input Voltage Swing (2nd Amp)	f_O = 4 kHz			V_{CC} − 1.6	
Vomax	Maximum Output Voltage Swing (2nd Amp)	f_O = 4 kHz	3			V_{PP}
Z_L	Single Ended Output Load			450		Ω

3.0 Electrical Specifications (Continued)

3.4.5 RX Amplifier Characteristics T_A = 25°C, Audio V_{CC} = 5 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
V_{IN} max	Maximum Input Voltage Swing (Differential)	f_O = 4 kHz		0.32	3.2	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	f_O = 4 kHz	3.2			V_{PP}
Z_L	Output Load			10k ‖ 70p		Ω ‖ F
TD	Total Distortion	f_O = 4 kHz		0.5	1.0	%
I_B	Input Bias Current				100	nA

3.4.6 Microphone Amplifier/Expander Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain		60			dB
GBW	Gain-Bandwidth Product			500		kHz
V_{IN} max	Maximum Input Voltage Swing	A_{CL} = 20 dB, f_O = 4 kHz			V_{CC} − 1.6	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	A_{CL} = 20 dB, f_O = 4 kHz	V_{CC} − 0.6	V_{CC} − 0.4		V_{PP}
A_{CLH}	Closed Loop Gain—High Output	$V_O > V_{SWH}$, f_O = 1 kHz		20		dB
A_{CLL}	Closed Loop Gain—Low Output	$V_O < V_{SWL}$, f_O = 1 kHz		14		dB
V_{SWL}	Low Gain Switching Output Voltage	90% of final gain		5		mVrms
V_{SWH}	High Gain Switching Output Voltage	90% of final gain		50		mVrms
t_{SPATCK}	Speech Response Attack Time	C_{EXT} = 0.4 μF, @ 100 mVrms 90% of final gain		25		ms
t_{SPDECY}	Speech Response Decay Time	C_{EXT} = 0.4 μF, @ V_{OUT} max 90% of final gain		85		ms
TD	Total Distortion	f_O = 200 Hz–4 kHz		0.5	1.0	%
f_{LOW}	Low Frequency Cut-off	Z_{CL} = Z_{CL0} − 3 dB		180		Hz
Z_S	Source Impedance			4.7		kΩ
	External Resistor Value for Defeat	Handset Base		75 200		kΩ
	Gain Switching Threshold			35		mVrms
I_B	Input Bias Current				100	nA

3.4.7 Preemphasis Filter Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			500		kHz
V_{IN} max	Maximum Input Voltage Swing	A_{CL} = 0 dB, f_O = 4 kHz			V_{CC} − 1.6	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	A_{CL} = 0 dB, f_O = 4 kHz	V_{CC} − 2.0			V_{PP}
Z_L	Output Load			10k ‖ 70p		Ω ‖ F
A_{CL}	Closed Loop Gain	f_O = 4 kHz		0		dB
f_P	Filter Pole Frequency (−3 dB)	Z_{CL} = Z_{CL0} − 3 dB		1.0		kHz
I_B	Input Bias Current				100	nA

3.0 Electrical Specifications (Continued)

3.4.8 Auxiliary Amplifier Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Units
A_{OL}	Open Loop Gain			80		dB
GBW	Gain-Bandwidth Product			200		kHz
V_{IN} max	Maximum Input Voltage Swing	f_O = 4 kHz			V_{CC} −1.6	V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	f_O = 4 kHz, V_{CC} = 5V	V_{CC} − 2.0	V_{CC} − 1.6		V_{PP}
V_{OUT} max	Maximum Output Voltage Swing	V_{CC} = 5V	3			V_{PP}
Z_L	Output Load	f_O = 4 kHz		10k		Ω
A_{CL}	Closed Loop Gain	f_O = DC		6		dB
TD	Total Distortion	f_O = 4 kHz		0.5	1.0	%

3.5 RX Data Slicer Characteristics T_A = 25°C, Audio V_{CC} = 3.6 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
V_{IN} max	Maximum Input Voltage Swing				V_{CC} − 1.6	V_{PP}
V_O low	Output Voltage Low (OC Out)		0		0.25 V_{CC}	V
V_O high	Output Voltage High (OC Out)		0.75 V_{CC}		5.0	V
V_{SWIT}	Switching Point		V_{REF} ± 450 mV	V_{REF} ± 500 mV	V_{REF} ± 600 mV	V
t_r/t_f	Rise and Fall Time	10%–90% 90%–10%			2	µs
	Output State When No Data			Last Valid Data		
I_{SINK}	Sink Current	V_{OL} = 0.45V	2			mA

3.6 Serial Interface DC and AC Characteristics T_A = 25°C, Audio V_{CC} = 3.0 V_{DC}–5.0 V_{DC}, V_{SS} = 0 V_{DC}

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
I_{IL}	Input Leakage	V_{IN} = 0V to V_{DD}	−1		1	µA
V_{IH}	Input High Voltage	I_{IN} = 20 µA	V_{CC} − 0.3		V_{CC}	V
V_{IL}	Input Low Voltage	I_{IN} = 20 µA	0		0.3	V
t_r/t_f	Rise and Fall Times	20%–80% and 80%–20%			200	ns
f_{SK}	CLK Clock Frequency		0	256	260	kHz
t_{SKH}	CLK High Time		1.2			µs
t_{SKL}	CLK Low Time		1.2			µs
t_{CSS}	CS Setup Time	Relative to CLK	12			µs
t_{LH}	Data Latch Hold Time	Relative to CS Inactive	5			µs
t_{SIS}	SI Setup Time	Relative to CLK	800			ns
t_{SIH}	SI Hold Time	Relative to CLK	800			ns

3.0 Electrical Specifications (Continued)

3.7 PLL Synthesizer DC Characteristics $T_A = 25°C$, $V_{CC} = 3.6$ DC

Symbol	Characteristic	Conditions	Pin	Min	Max	Units
V_{IL}	Input Voltage Low		Data, Clk, En		0.3	V
V_{IH}	Input Voltage High		Data, Clk, En	$V_{CC} - 0.3$		V
I_{IL}	Input Current Low		Data, Clk, En	−5		μA
I_{IH}	Input Current High		Data, Clk, En		5	μA
I_{PDSRC}	Phase Detect Source Current		Rx PD, Tx PD	−0.5		mA
I_{PDSNK}	Phase Detect Sink Current		Rx PD, Tx PD		0.5	mA
V_{OLPD}	Phase Detect Output Voltage Low	$I_{PDSNK} = 0.5$ mA	Rx PD, Tx PD		0.6	V
V_{OHPD}	Phase Detect Output Voltage High	$I_{PDSRC} = -0.5$ mA	Rx PD, Tx PD	3.0		V
	TRI-STATE® Leakage Current		Rx PD, Tx PD	−50	50	nA
	Input Capacitance		Data,Clk,En		8	pF
	Output Capacitance		Rx PD, Tx PD		8	pF
t_{SU}	Setup Time Data to CLK		Data, CLK	100		ns
t_{SU}	Setup Time En to CLK		En, CLK	200		ns
t_H	Hold Time		Data, CLK	90		ns
t_{REC}	Recovery Time		En, CLK	90		ns
t_W	Input Pulse Width		En, Clk	100		ns
	2nd LO Frequency				12	MHz
	Tx VCO Input Frequency	$V_{IN} = 200\ mV_{PP}$			80	MHz

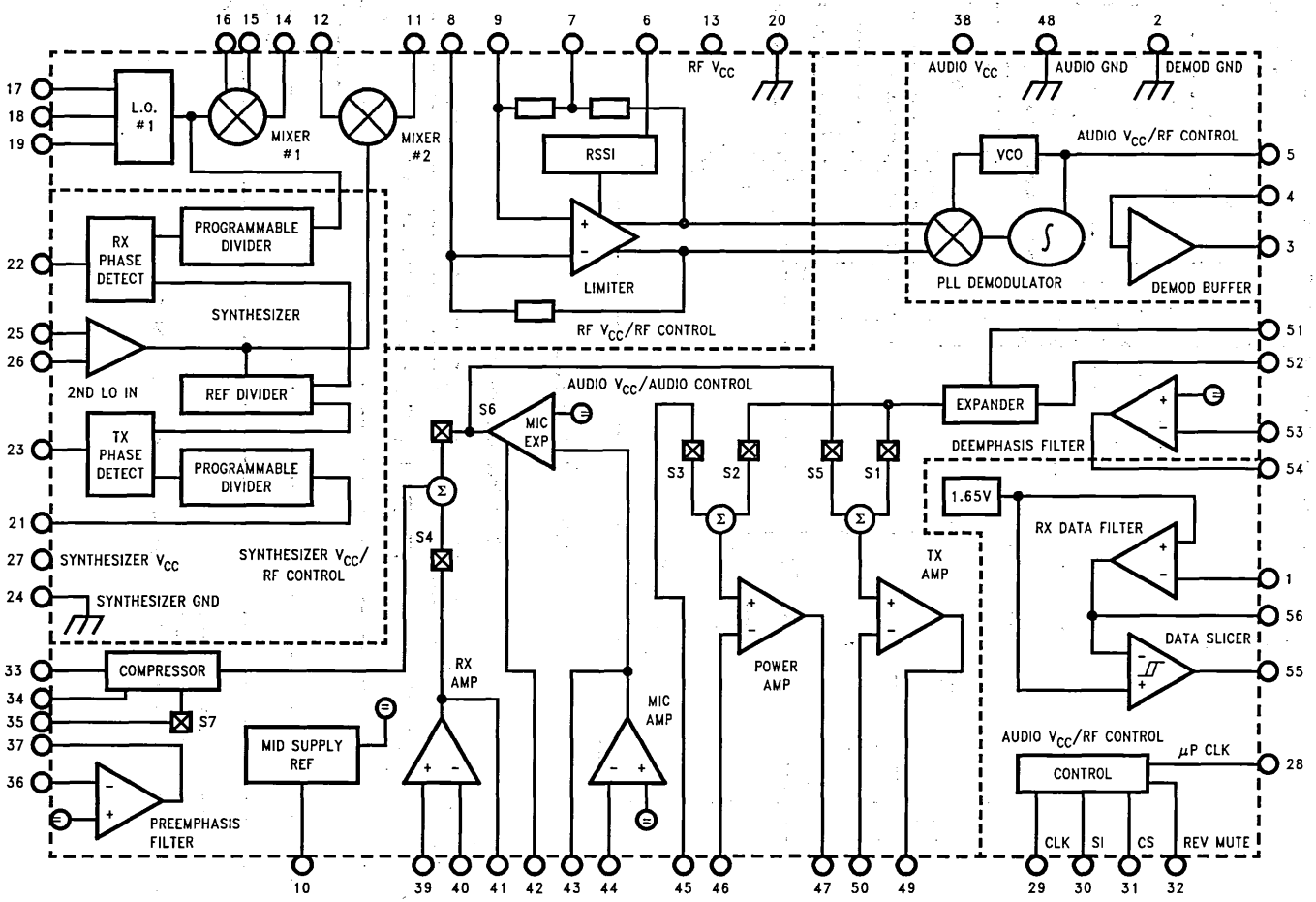

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FIGURE 3. NCL354 Block Diagram

4.0 NCL354 Serial Interface Timing

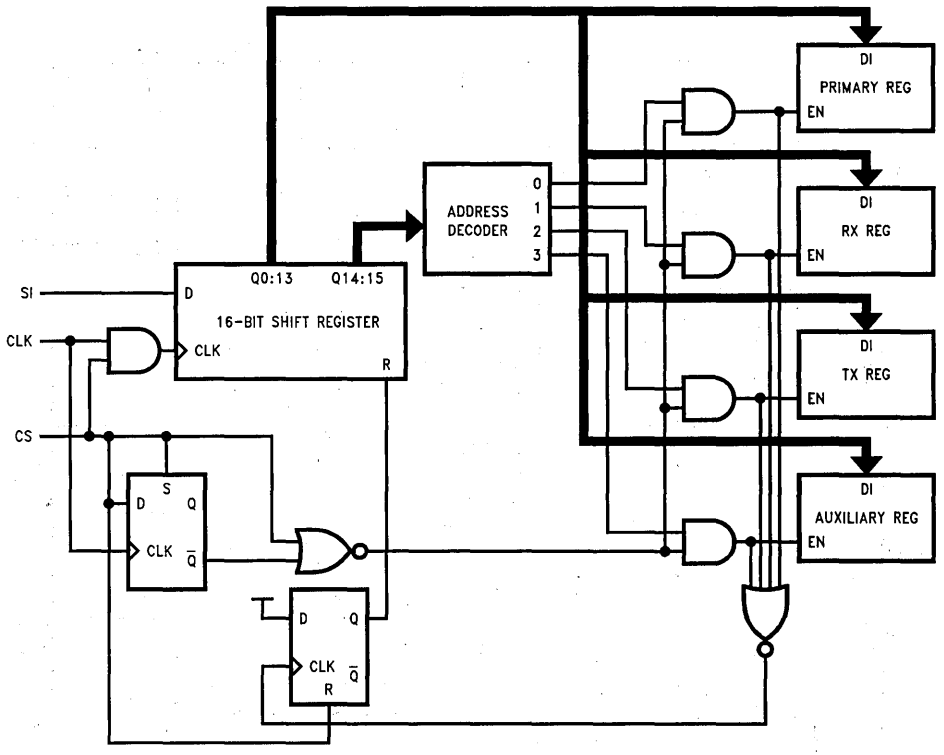

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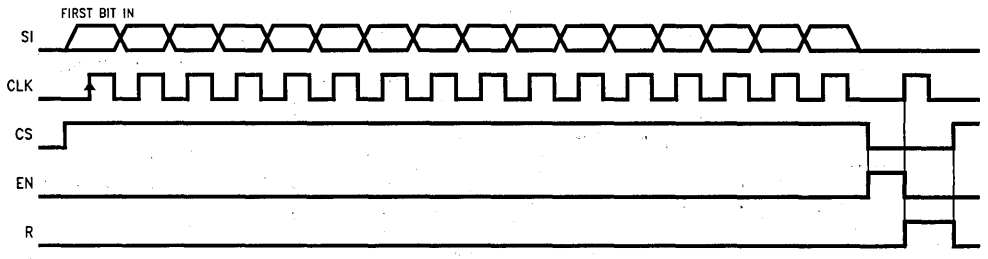
FIGURE 4. Serial Interface

Serial Interface Timing



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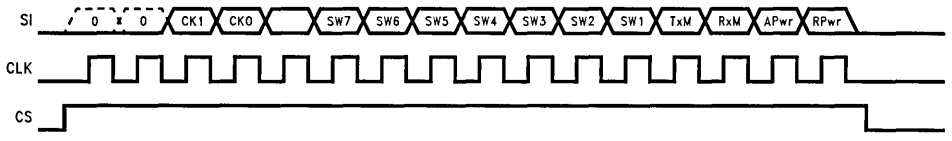
Note: "EN" is an internal signal that loads the registers.
"R" is an internal signal that resets the 16-bit shift register.
An extra clock pulse is required for resetting the shift register when < 16-bits are entered (SNFF mode).

4.0 NCL354 Serial Interface Timing (Continued)

Serial Interface Timing—Primary Control Register



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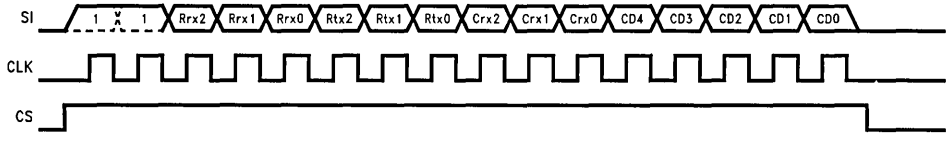
CK1–CK0 Clock Divider Select
SW7–SW1 Switch Select ("1" = switch closed)
TxM Transmit Mute
RxM Receive Mute
APwr Audio Power Switch

Serial Interface Timing—Auxiliary Control Register



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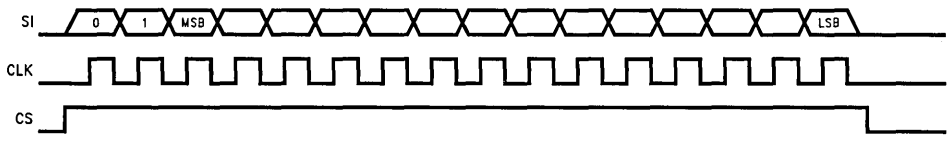
Rrx2–Rrx0 Receive Reference Frequency Select
Rtx2–Rtx0 Transmit Reference Frequency Select
Crx2–Crx0 Capacitor Select for Receive VCO
CD4–CD0 Carrier Detect Level
RPwr RF Power Switch

Serial Interface Timing—Receive Divider



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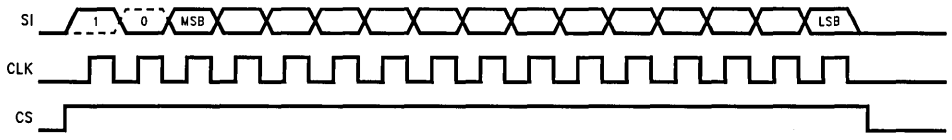
Serial Interface Timing—Transmit Divider



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Section 9

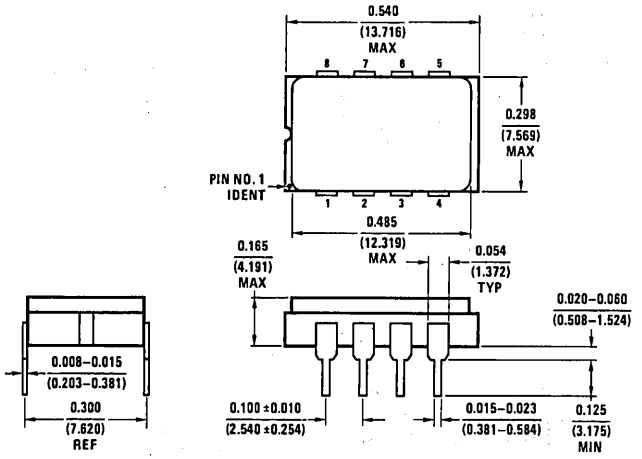
Physical Dimensions

Section 9 Contents

National Semiconductor

8 Lead Ceramic Sidebrazed Dual-in-Line Package
NS Package Number D08C

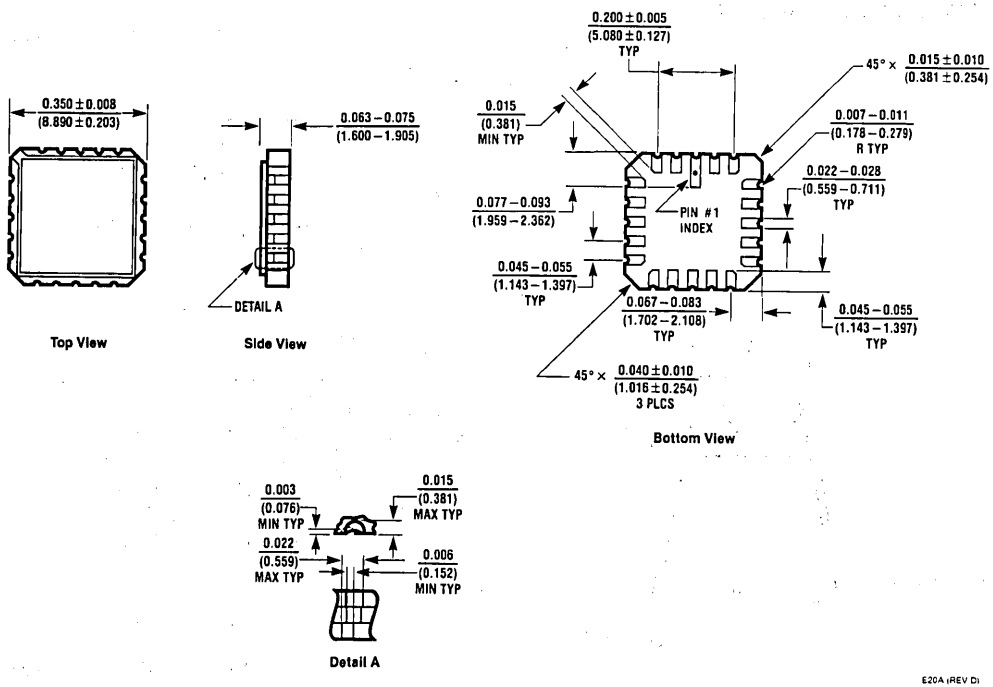
All dimensions are in inches (millimeters)



D08C (REV C)

20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A

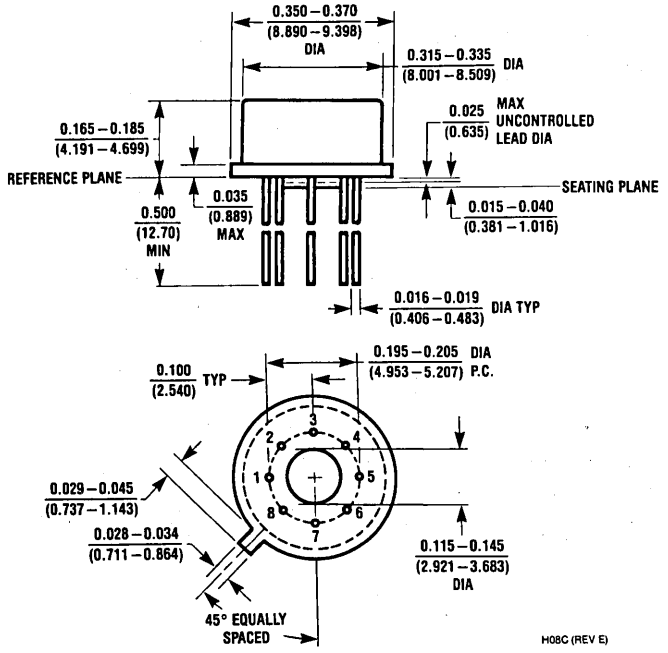
All dimensions are in inches (millimeters)



E20A (REV D)

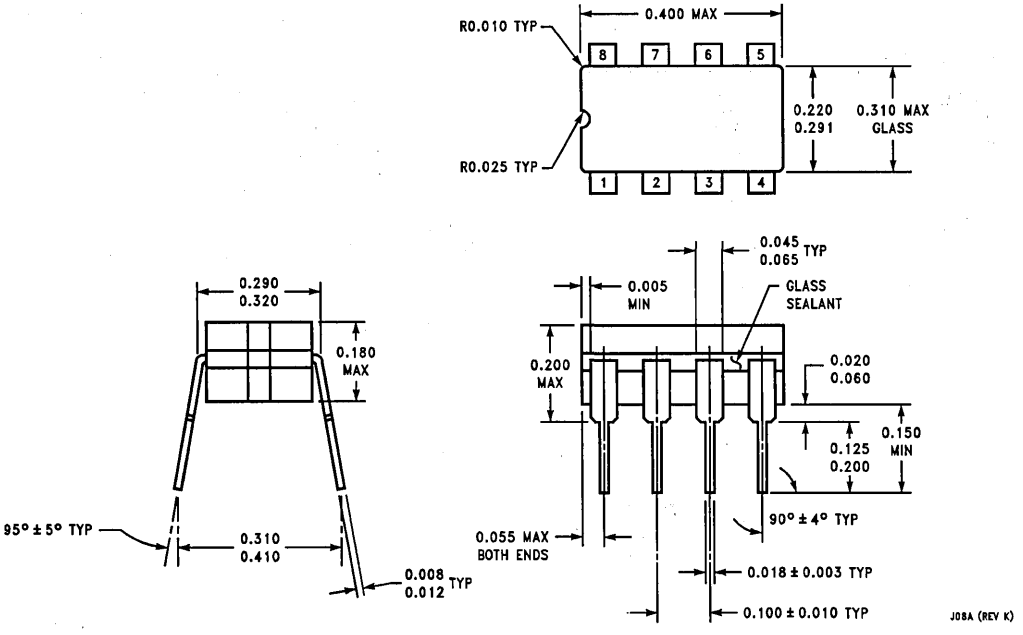
8 Lead (0.200″ Diameter P.C.) TO-5 Metal Can Package
NS Package Number H08C

All dimensions are in inches (millimeters)



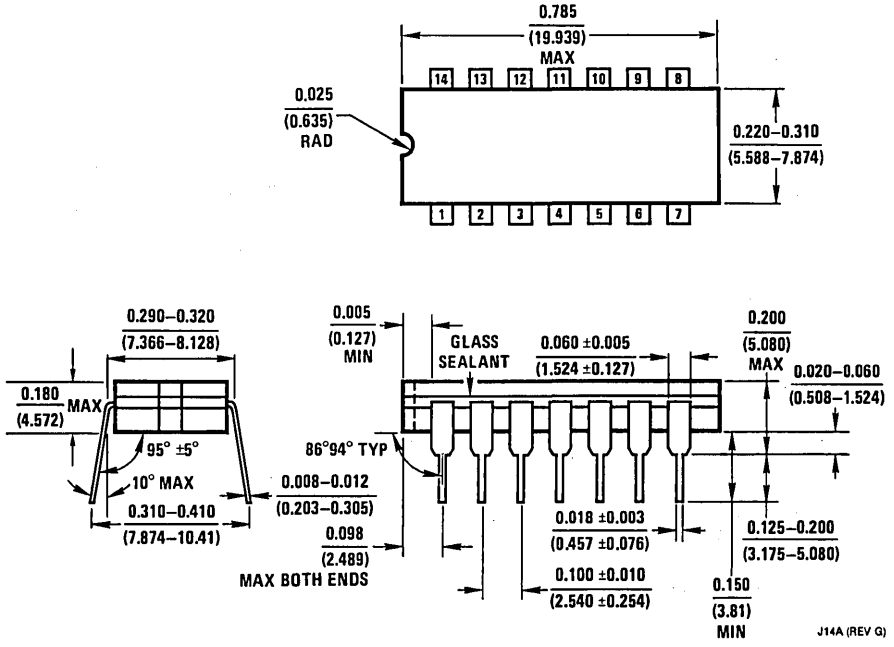
8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

All dimensions are in inches



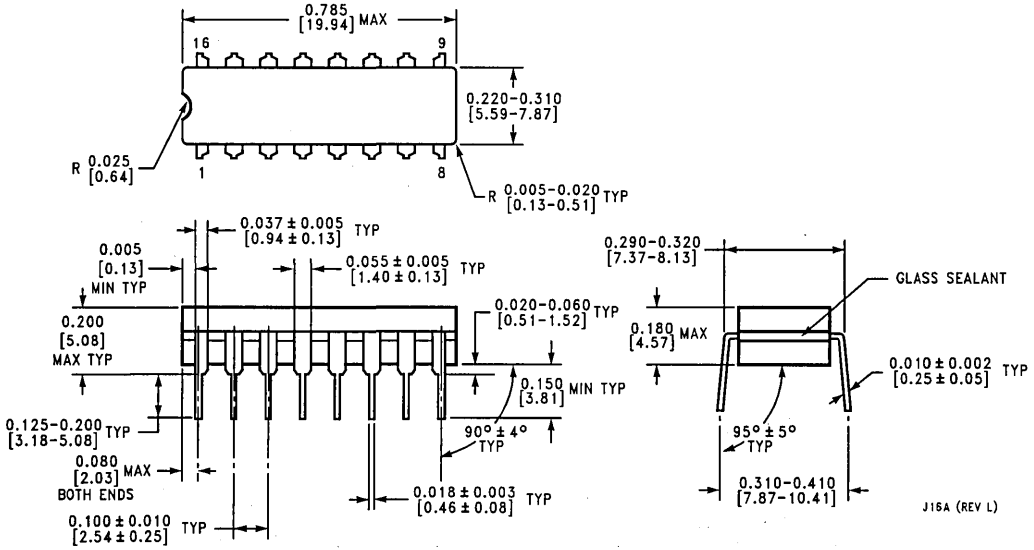
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A

All dimensions are in inches (millimeters)



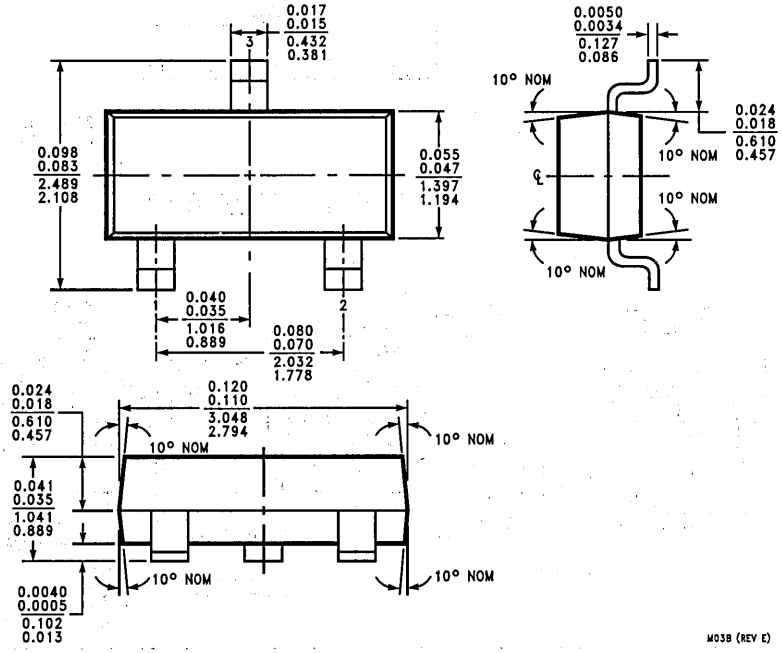
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A

All dimensions are in inches [millimeters]



3 Lead Molded SOT-23, Low Profile
NS Package Number M03B

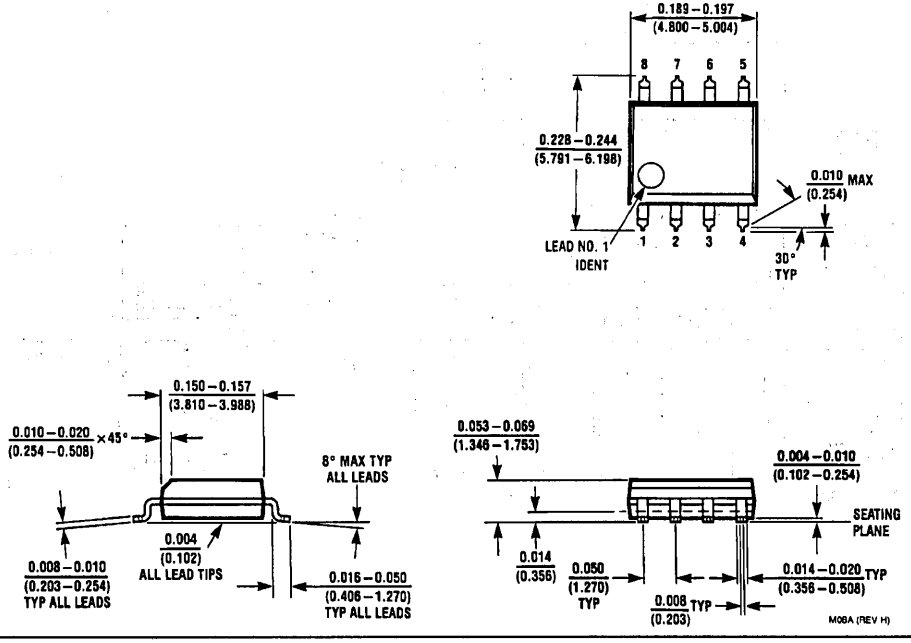
All dimensions are in inches / millimeters



M03B (REV E)

8 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

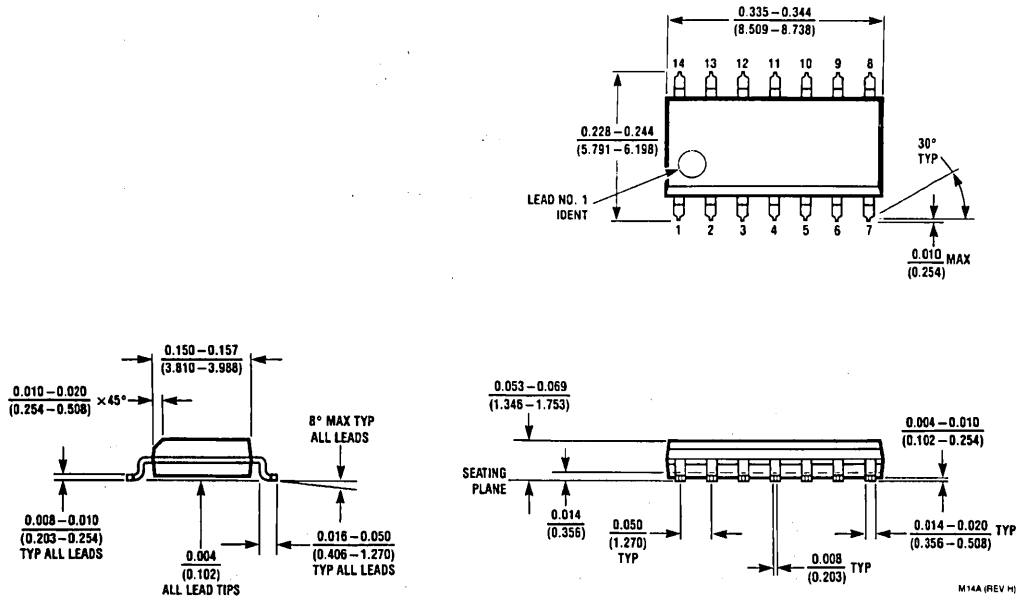
All dimensions are in inches (millimeters)



M08A (REV H)

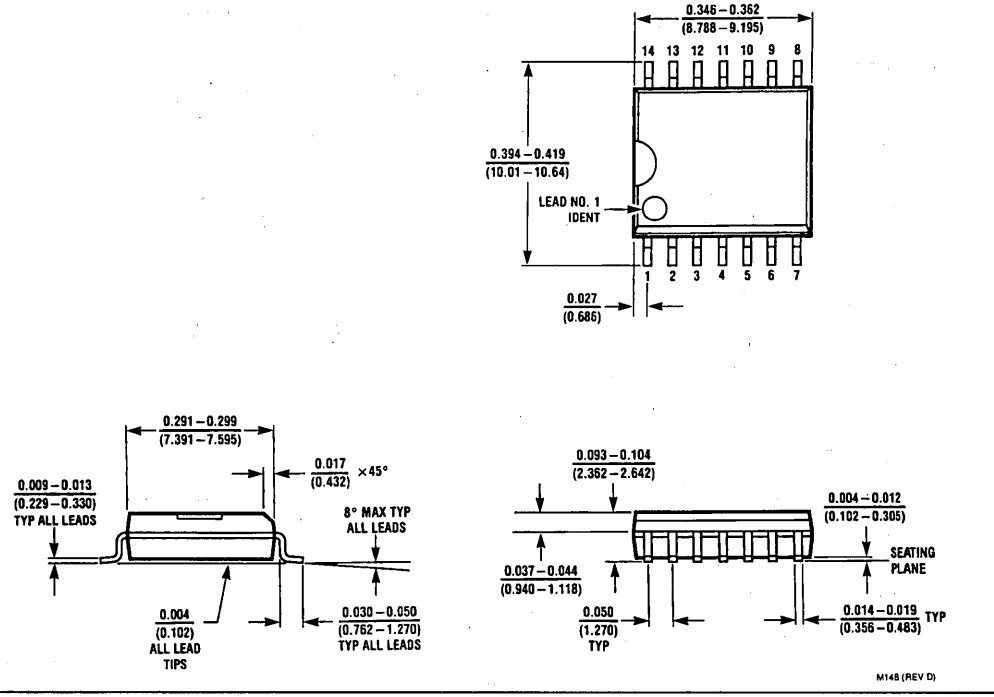
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



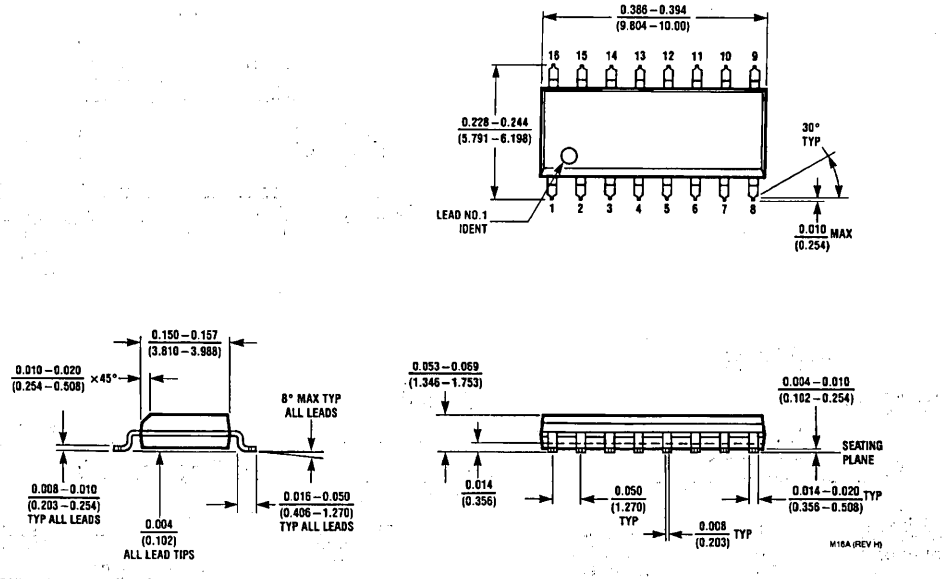
14 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14B

All dimensions are in inches (millimeters)



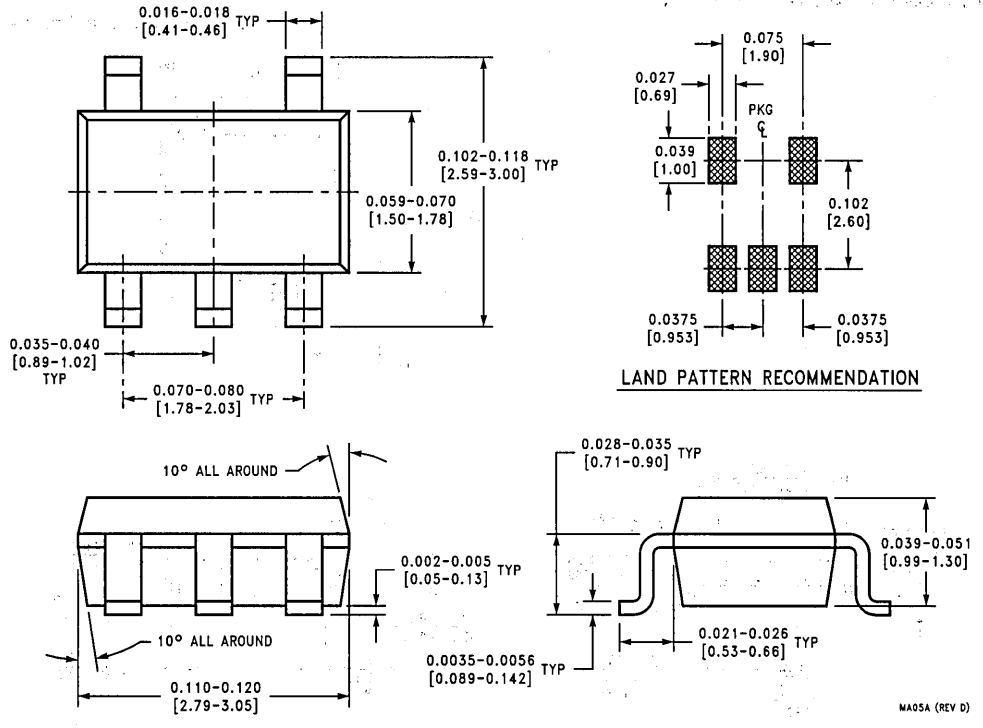
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)



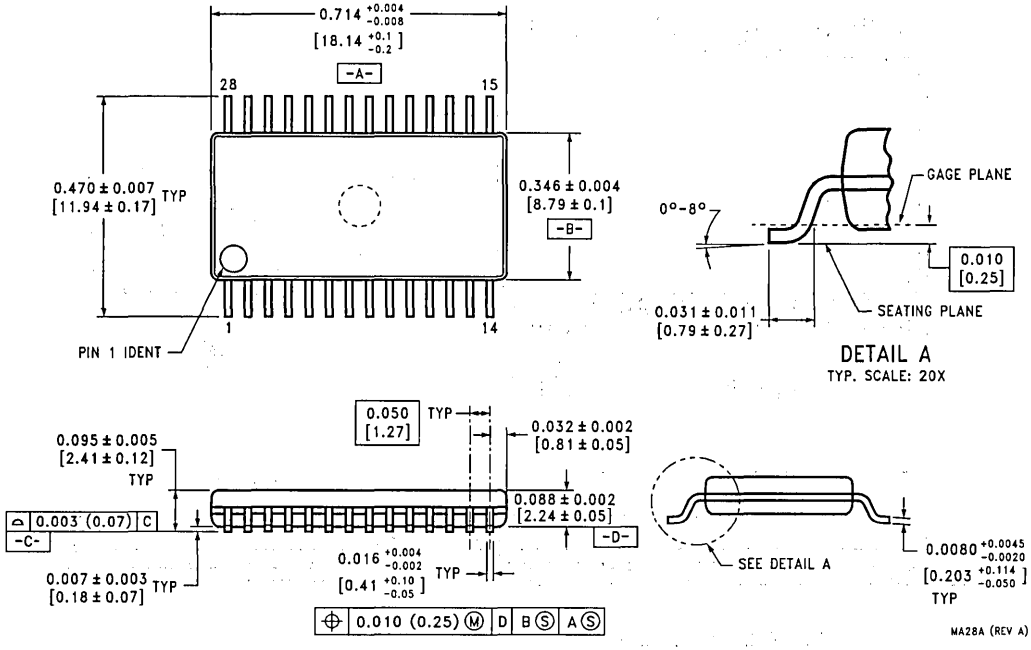
5 Lead Molded SOT-23-5
NS Package Number MA05A

All dimensions are in inches [millimeters]



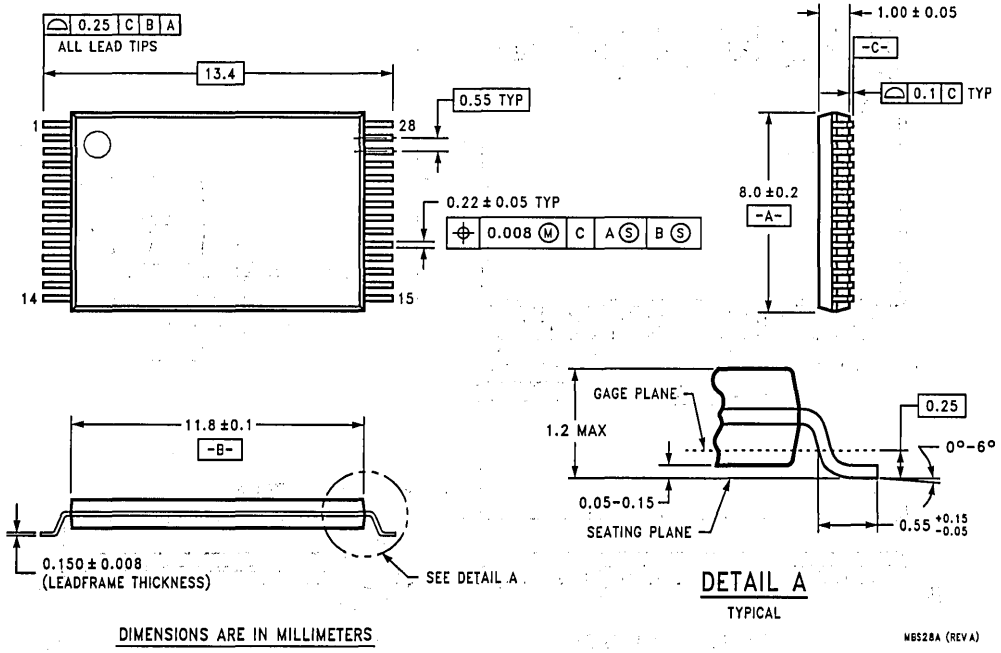
28 Lead (0.350" Wide) Molded Small Outline Package
NS Package Number MA28A

All dimensions are in inches [millimeters]



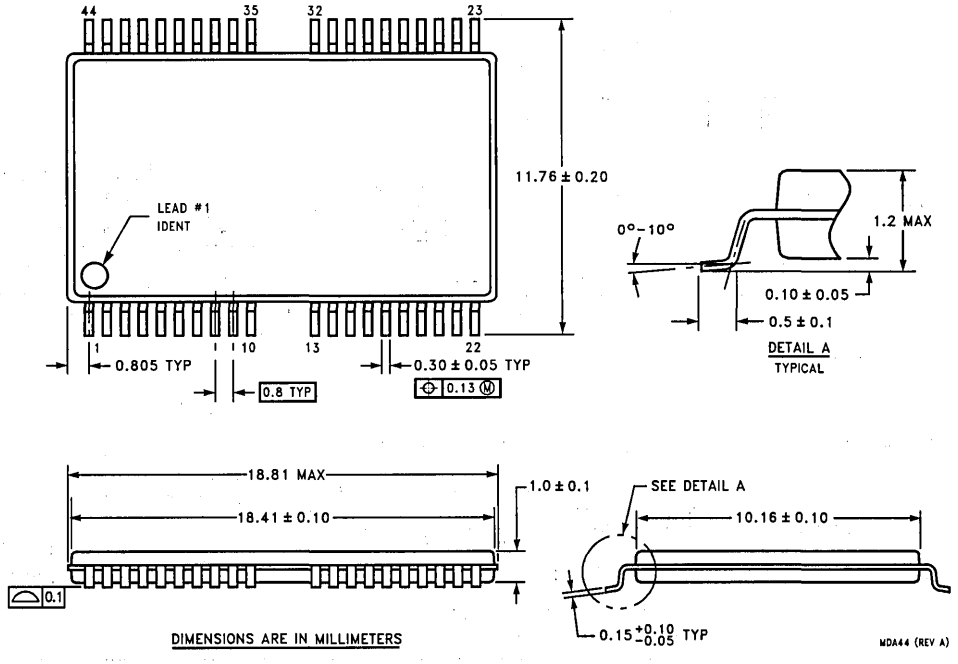
28 Lead Thin Small Outline Package, Type I
NS Package Number MBS28A

All dimensions are in millimeters



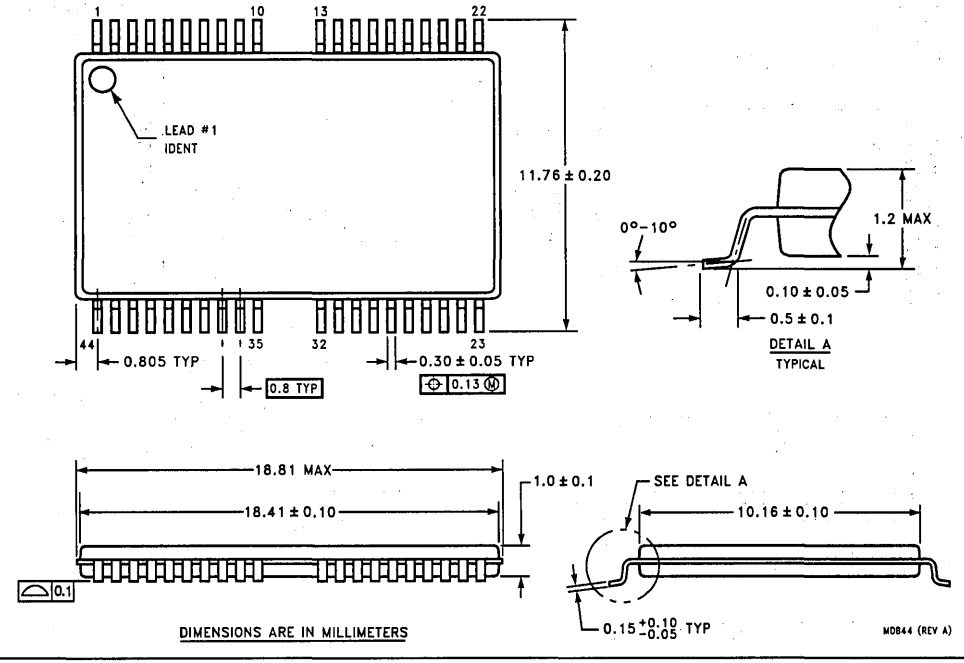
44 Lead Thin Small Outline Package, EIAJ, Type II
NS Package Number MDA44

All dimensions are in millimeters



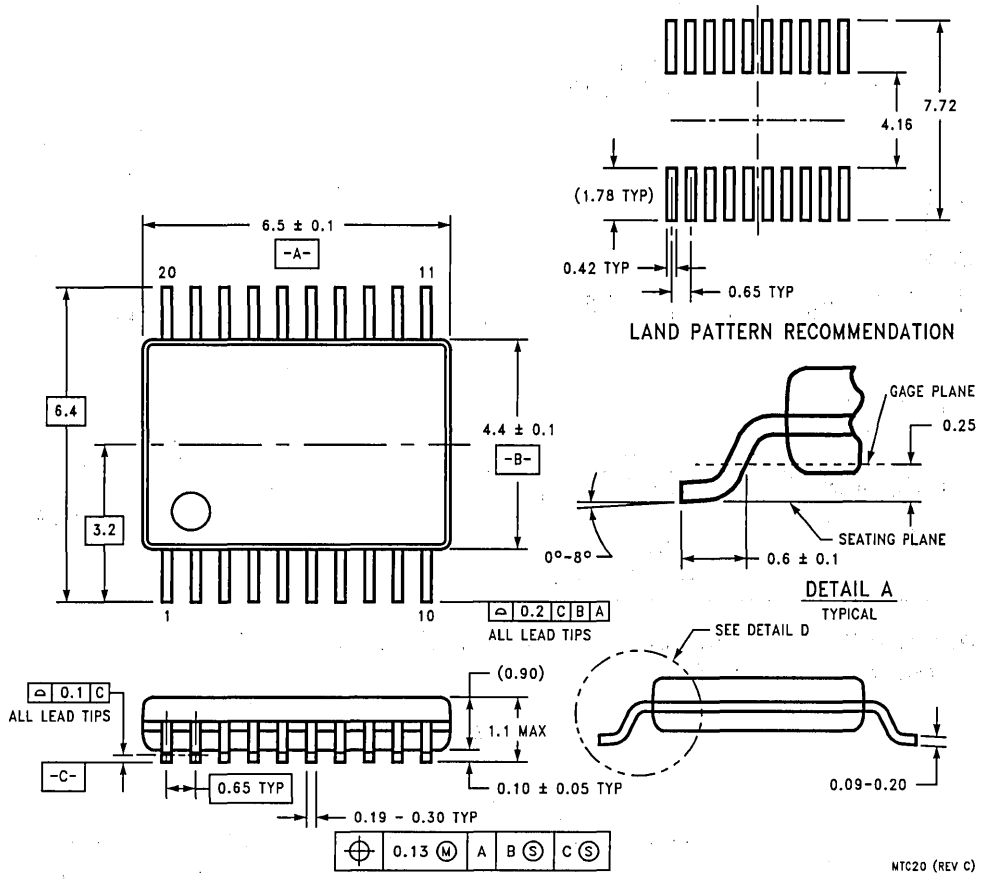
44 Lead Thin Small Outline Package, EIAJ, Type II
NS Package Number MDB44

All dimensions are in millimeters



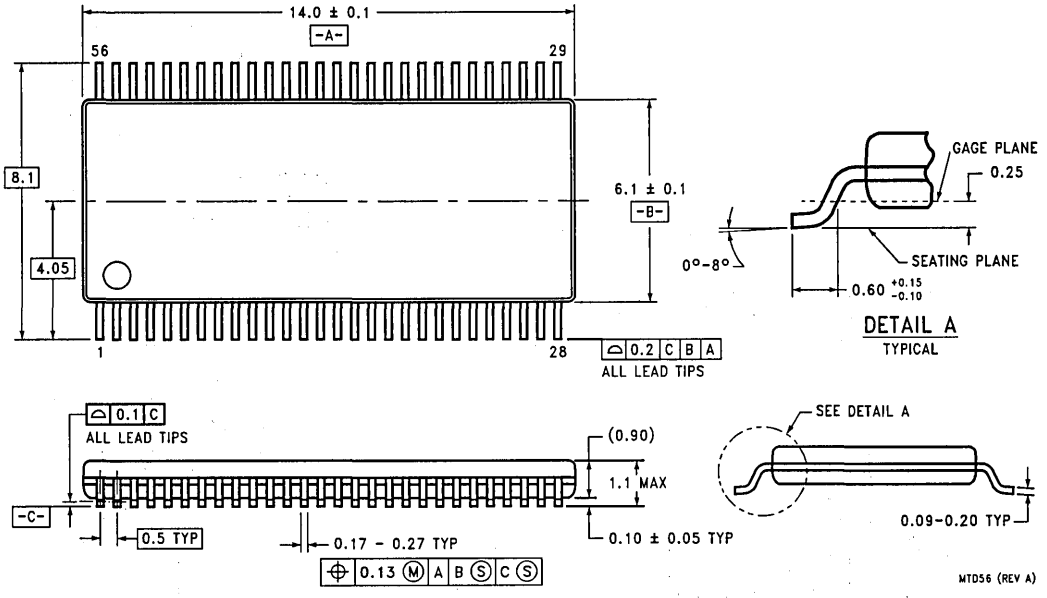
20 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20

All dimensions are in millimeters



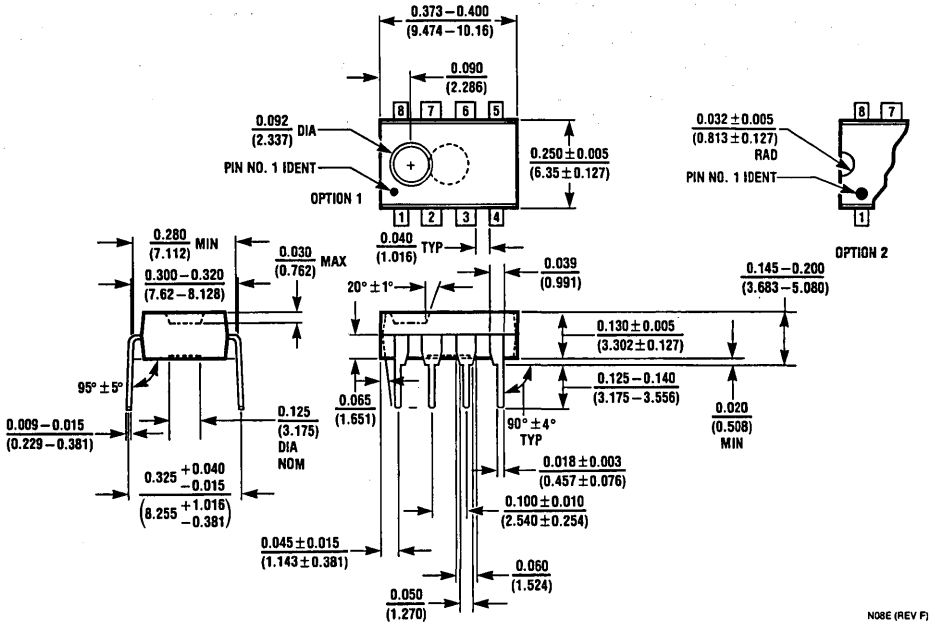
56 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56

All dimensions are in millimeters



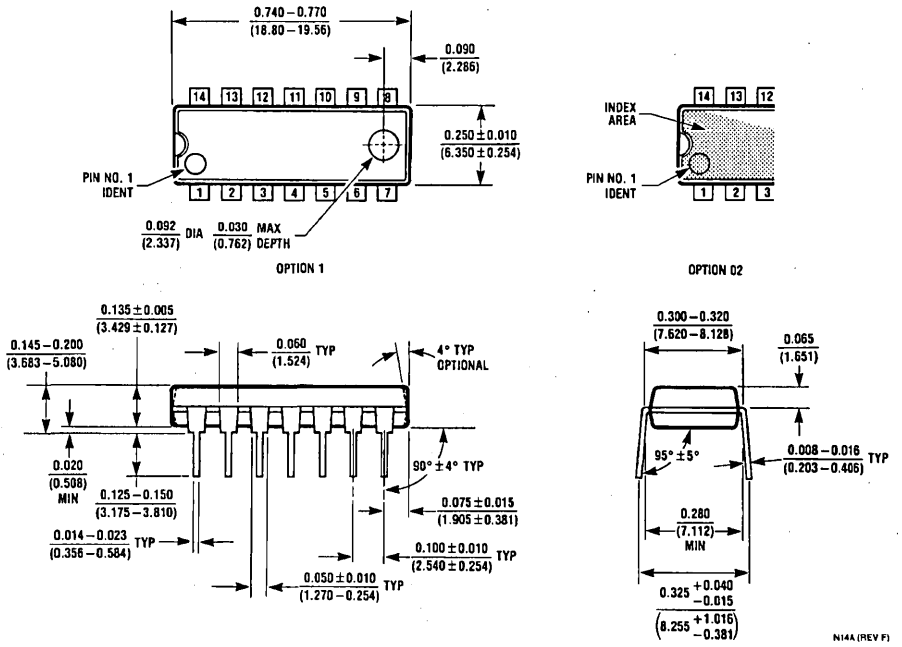
8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E

All dimensions are in inches (millimeters)



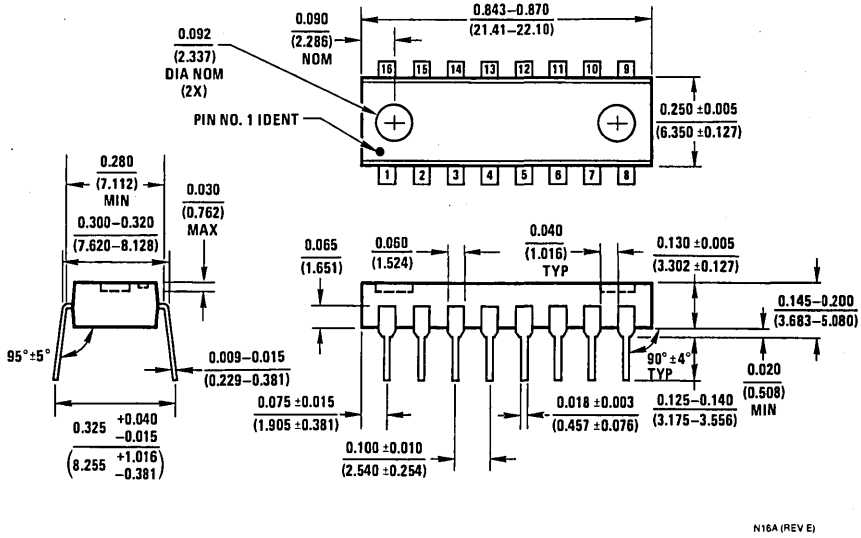
14 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N14A

All dimensions are in inches (millimeters)



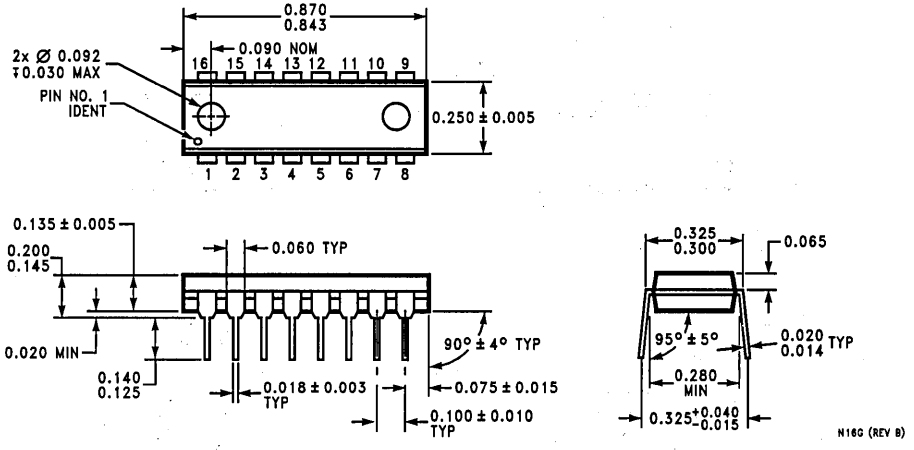
16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16A

All dimensions are in inches (millimeters)



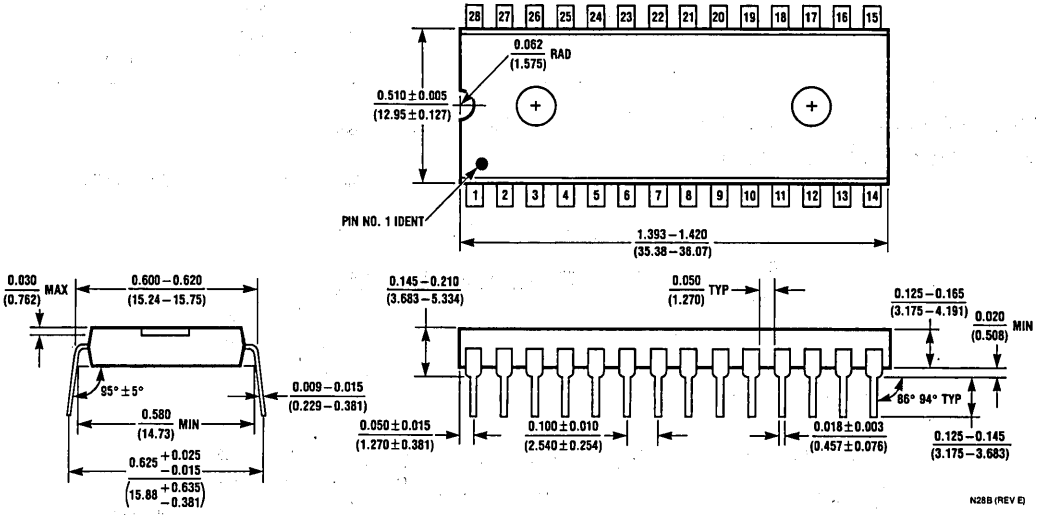
16 Lead (0.300" Wide) Molded Dual-in-Line Package, Thermally Enhanced
NS Package Number N16G

All dimensions are in inches



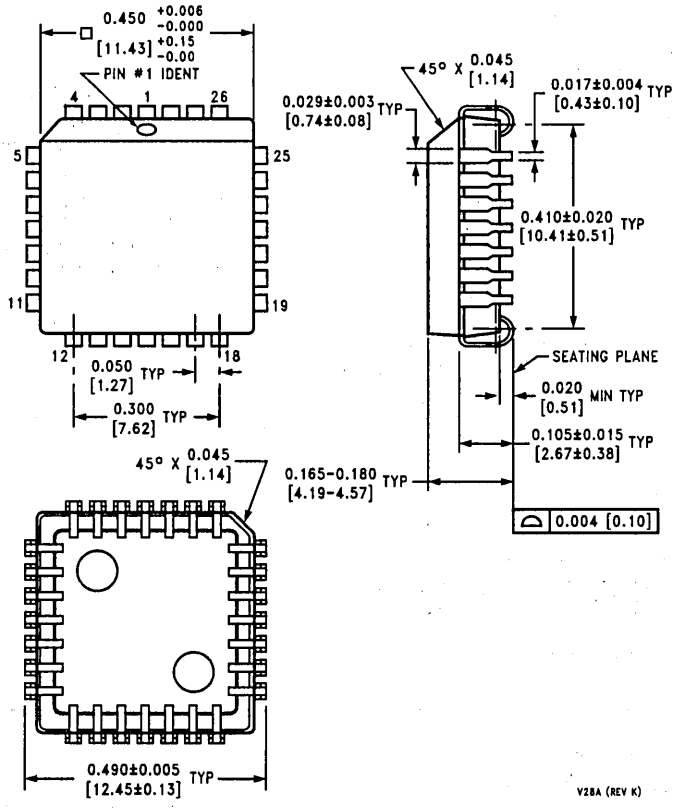
28 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N28B

All dimensions are in inches (millimeters)



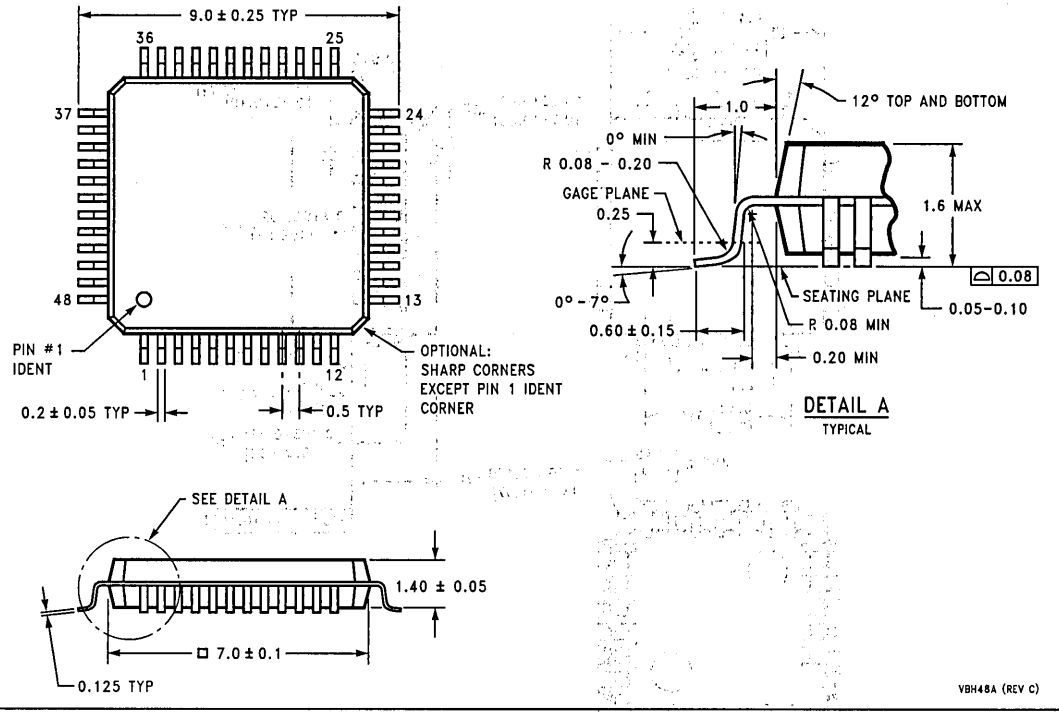
28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A

All dimensions are in inches [millimeters]



48 Lead (7mm x 7mm) Molded Plastic Quad Flat Package, JEDEC
NS Package Number VBH48A

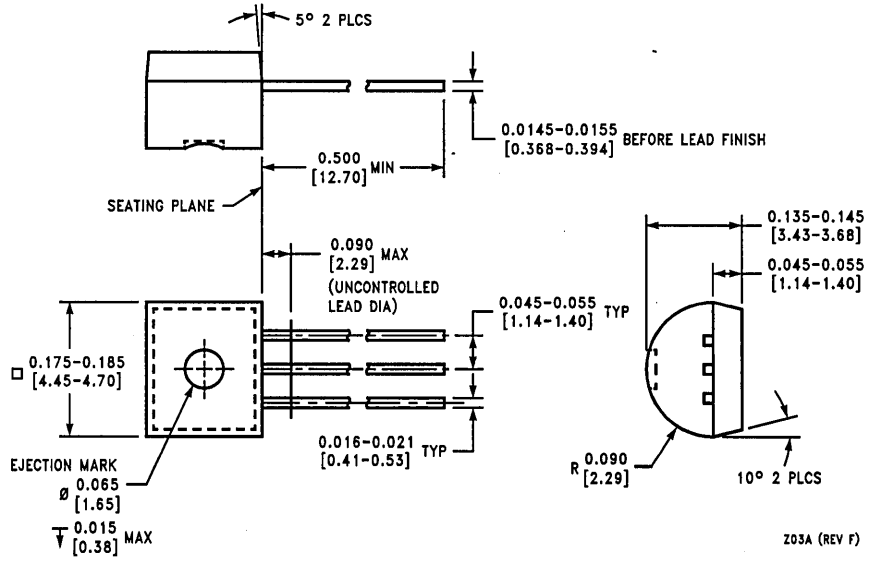
All dimensions are in millimeters



VBH48A (REV C)

3 Lead Molded TO-92
NS Package Number Z03A

All dimensions are in inches [millimeters]



Z03A (REV F)

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54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
SCAN18xxxA BiCMOS 5V Logic with Boundary Scan • 74LVT Low Voltage BiCMOS Logic
VME Extended TTL Technology for Backplanes

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Crystal Clock Oscillators

COP8™ DATABOOK—1994

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Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

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LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LOCAL AREA NETWORKS DATABOOK—1993 SECOND EDITION

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LOW VOLTAGE DATABOOK—1992

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MASS STORAGE HANDBOOK—1989

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Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

MEMORY DATABOOK—1994

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MEMORY APPLICATIONS HANDBOOK—1994

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Special Functions • Surface Mount

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POWER IC's DATABOOK—1995

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The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
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VHC/VHCT ADVANCED CMOS LOGIC DATABOOK—1993

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