National Semiconductor

400068

Mass Storage Handbook

A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

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Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Mass Storage
HANDBOOK

1989 Edition

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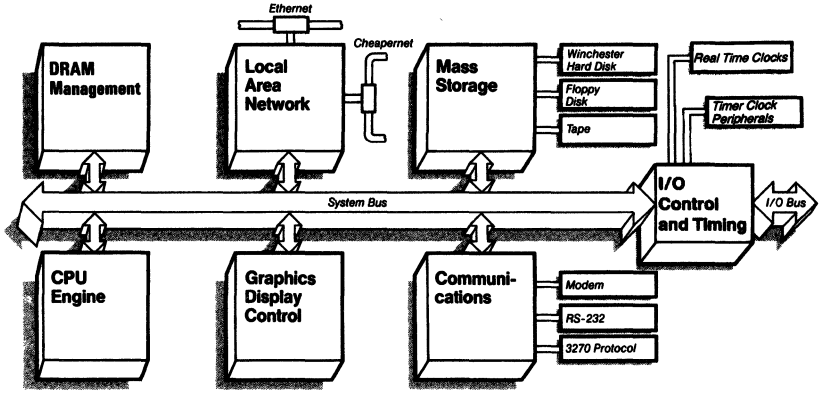
National Semiconductor

Introduction Advanced Peripherals



TL/XX/0058–1

National Semiconductor Advanced Peripherals products include complex VLSI peripheral circuits designed to serve a variety of applications. The Advanced Peripherals products are especially well suited for microcomputer and microprocessor systems such as graphics workstations, personal computers, and many others. National Semiconductor Advanced Peripherals devices are fully described in a series of databooks and handbooks.

Among the Advanced Peripherals books are the following titles:

MASS STORAGE

The National Semiconductor family of mass storage interface products offers the industry's highest performance and broadest range of products for Winchester hard disks and floppy disks. The Mass Storage Handbook includes complete product information and datasheets as well as a comprehensive design guide for disk controller systems.

DRAM MANAGEMENT

Today's large Dynamic Random Access Memory (DRAM) arrays require sophisticated high performance devices to provide timing access arbitration on board drive and control. National Semiconductor offers the broadest range of DRAM controllers with the highest "No-waitstate" performance available on the market. Controllers are available in Junction Isolated LS, Oxide Isolated ALS, and double metal CMOS for DRAMs from 64k bit through 4M bit devices, supporting memory arrays up to 64 Mbyte in size with only one LSI/VLSI device. For critical applications, National Semiconductor has developed several 16- and 32-bit Error Checking and Correction (ECC) devices to provide maximum data integrity. The Memory Support Handbook contains complete product information and several application notes detailing complete memory system design.

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Today's computer systems have created a huge demand for data communications and Local Area Networks (LANs). National Semiconductor provides a complete three-chip solution for an entire IEEE 802.3 standard for Ethernet/Cheapernet LANs. National Semiconductor offers a completely integrated solution for the IBM 370 class mainframes, System 3X and AS/400 systems for physical layer front end and processing of the IBM 3270/3299 "coaxial" and 5250 "twinaxial" protocols. To drive the communications lines, National Semiconductor has drivers and receivers designed to meet all the major standards such as RS-232, RS-422, and RS-485. Datasheets and applications information for all these products are in the LAN/DATA COMM Handbook.

GRAPHICS

Sophisticated human interface is a mark of the newest computer systems designs. Today's personal computer may have better graphics display capability than engineering workstations of a few years ago. National Semiconductor has developed a new family of Advanced Graphics products to provide extremely high performance, high resolution color graphics displays. The graphics chip set is designed to provide the highest level of performance with minimum demands and loading on the system CPU. The graphics system may be expanded to any number of color planes with virtually unlimited resolution. The Graphics Databook lays it all out and makes the display system design easy.

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National offers a family of Real Time Clocks (RTCs) and advanced Timer Clock Peripherals (TCPs). The RTC family provides a simple μP bus compatible interface to any system requiring accurate, reliable, on-going real time and calender functions. The TCP family offers the RTC, RAM and two 16-bit programmable timers with fast μP bus handshake controls for chip select, read and write. The Real Time Clock handbook includes complete product information and datasheets as well as applications information.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Rigid Disk Pulse Detectors

Section 1 Contents

National Semiconductor

DP8464B Disk Pulse Detector

General Description

The DP8464B Disk Pulse Detector utilizes analog and digital circuitry to detect amplitude peaks of the signal received from the read/write amplifier fitted with the heads of disk drives. The DP8464B produces a TTL compatible output which, on the positive leading edge, indicates a signal peak. Electrically, these peaks correspond to flux reversals on the magnetic medium. The signal from the read/write amplifier when reading a disk is therefore a series of pulses with alternating polarity. The Disk Pulse Detector accurately replicates the time position of these peaks.

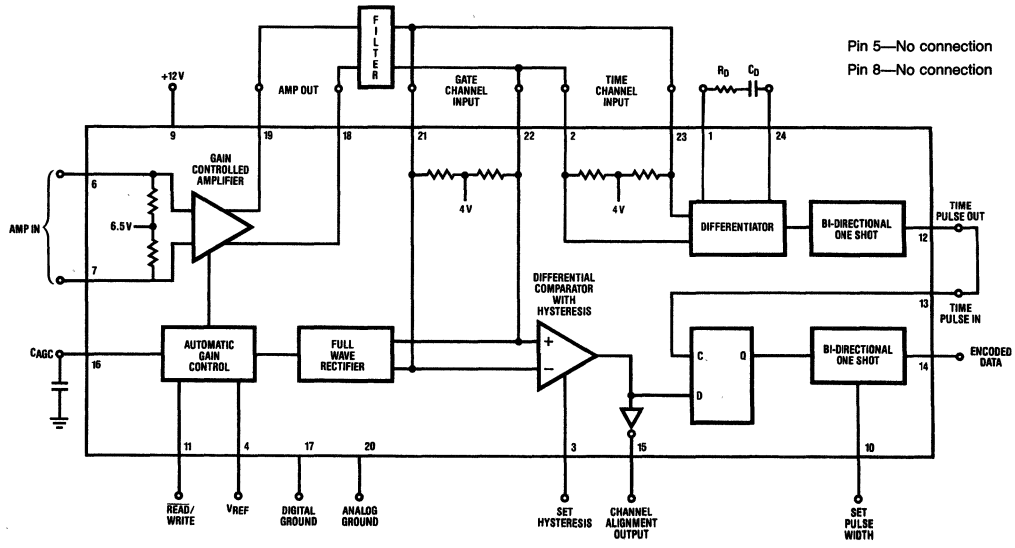
The DP8464B Disk Pulse Detector has three main sections: the Amplifier, the time channel and the gate channel. The Amplifier section consists of a wide bandwidth amplifier, a full wave rectifier and Automatic Gain Control (AGC). The time channel is made from the differentiator and its following bi-directional one shot, while the gate channel is made from the differential comparator with hysteresis, the D flip-flop and its following bi-directional one shot.

The Disk Pulse Detector is fabricated using an advanced oxide isolated Schottky process, and has been designed to function with data rates up to 15 Megabits/second. The DP8464B is available in either a 300 mil wide 24-pin dual-in-line package or a surface mount 28-pin plastic chip carrier package. Normally, it will be fitted in the disk drive, and its output may be directly connected to the DP8461 or the DP8465 Data Separator.

Features

- Wide input signal amplitude range—from 20 mVpp to 660 mVpp differential
- Data rates up to 15 Megabits/sec 2,7 code
- On-chip differential gain controlled amplifier, differentiator, comparator gating circuitry, and output pulse generator
- Input capacitively coupled directly from the disk head read/write amplifier
- Adjustable comparator hysteresis
- AGC and differentiator time constants set by external components
- TTL compatible digital Inputs and Outputs
- Encoded Data Output may connect directly to the DP8461 or DP8465 Data Separator
- Standard drive supply: 12V ± 10%
- Available in 300 mil wide 24-pin dual-in-line package, a surface mount 28-pin plastic chip carrier package, or a 40-pin TapePak® package

Block Diagram



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Note: All pin numbers in this data sheet refer to the 24-pin dual-in-line package.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Pins	Limit
Supply Voltage	9	14V
TTL Input Voltage	11,13	5.5V
TTL Output Voltage	12,14,15	5.5V
Input Voltage	3,4	5.5V
Minimum Input Voltage	3,4	−0.5V
Differential Input Voltage	6-7, 21-22, 2-23	3V or −3V
ESD Susceptibility (see Note 5)		

Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
Maximum Power Dissipation at 25°C	
Molded DIP Package (derate 15.6 mW/°C above 25°C)	1950 mW
Plastic Chip Carrier Package (derate 12.5 mW/°C above 25°C)	1560 mW

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	10.8	12.0	13.2	V
T_A	Ambient Temperature	0		70	°C

DC Electrical Characteristics

Over Recommended Operating Temperature and Supply Range V_{REF} = 0.5V, Set Hysteresis = 0.3V. $\overline{\text{Read}}$/Write = 0.3V unless otherwise noted. All Pin Numbers Refer to 24 Pin Dual-In-Line Package.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
AMPLIFIER							
$Z_{IN_{AI}}$	6,7	Amp In Impedance	T_A = 25°C (Note 1)	0.75	1.0	1.25	kΩ
A_{VMIN}	18,19	Min Voltage Gain	AC Output 4 Vpp Differential			6.0	V/V
A_{VMAX}	18,19	Max Voltage Gain	AC Output 4 Vpp Differential	200			V/V
$V_{C_{AGC}}$	16	Voltage on C_{AGC}	A_V = 6.0 A_V = 200	 2.8	4.5 3.7	5.5	V V
GATE CHANNEL							
$Z_{IN_{GCI}}$	21,22	Gate Channel Input Impedance	T_A = 25°C (Note 1)	1.75	2.5	3.25	kΩ
$I_{C_{AGC-}}$	16	Pin 16 Current which Charges C_{AGC}	$V_{PIN\ 16}$ = 3.9V $\lvert V_{PIN\ 21} - V_{PIN\ 22} \rvert$ = 1.3 V_{DC}	−1.5	−2.5	−3.5	mA
$I_{C_{AGC+}}$	16	Pin 16 Current which Discharges C_{AGC}	$V_{PIN\ 16}$ = 5V $\lvert V_{PIN\ 21} - V_{PIN\ 22} \rvert$ = 0.7 V_{DC}		1	5	μA
$I_{V_{REF}}$	4	V_{REF} Input Bias Current			−20	−100	μA
$V_{TH_{AGC}}$	22,21 4,16	AGC Threshold	(Note 2) $V_{PIN\ 16}$ = 4.2V	0.88	1.0	1.12	V
I_{SH}	3	Set Hysteresis Input Bias Current			−60	−100	μA
$V_{TH_{SH}}$	22,21 3,15	Set Hysteresis Threshold	(Note 3)	0.48	0.6	0.72	V
TIME CHANNEL							
$Z_{IN_{TC}}$	2,23	Time Channel Input Impedance	T_A = 25°C (Note 1)	3.5	5.0	6.5	kΩ
I_{C_d}	24	Current into Pin 1 and 24 that Discharges C_d		1.4	1.8	2.50	mA

DC Electrical Characteristics Over Recommended Operating Temperature and Supply Range V_{REF} = 0.5V, Set Hysteresis = 0.3V. $\overline{Read}$/Write = 0.3V unless otherwise noted. All pin numbers refer to the 24 pin dual-in-line package. (Continued)

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
WRITE MODE							
$Z_{IN_{AI}}$	6,7	Amp In Impedance in Write Mode	$V_{PIN\ 11}$ = 2.0V	50		250	Ω
$I_{C_{AGC-}}$	16	Pin 16 Current in Write Mode	$V_{PIN\ 11}$ = 2.0V $V_{PIN\ 16}$ = 3.9V $\lvert V_{PIN\ 21} - V_{PIN\ 22} \rvert$ = 1.3 V_{DC}		1	5	μA
DIGITAL PINS							
V_{IH}	11,13	High Level Input Voltage		2			V
V_{IL}	11,13	Low Level Input Voltage				0.8	V
V_I	11,13	Input Clamp Voltage	V_{CC} = Min I_I = −18 mA			−1.5	V
I_{IH}	11,13	High Level Input Current	V_{CC} = Max V_I = 2.7V			20	μA
I_I	11,13	Input Current at Maximum Input Voltage	V_{CC} = Max V_I = 5.5V			1	mA
I_{IL}	11,13	Low Level Input Current	V_{CC} = Max V_I = 0.5V			−200	μA
V_{OH}	12,14, 15	High Level Output Voltage	V_{CC} = Min I_{OH} = −40 μA (Note 4)	2.7			V
V_{OL}	12,14, 15	Low Level Output Voltage	V_{CC} = Min I_{OL} = 800 μA (Note 4)			0.5	V
I_{OS}	12,14, 15	Output Short Circuit Current	V_{CC} = Max V_O = OV			−100	mA
I_{CC}	9	Supply Current	V_{CC} = Max		54	75	mA

AC Electrical Characteristics

Over Recommended Operating Temperature and Supply Range unless otherwise noted

Symbol	Pins	Parameter	Conditions	Typ	Max	Units
DP8464B-2 t_{pp}	14	Pulse Pairing	(See Pulse Pairing Set Up)	±1.5	±3	ns
DP8464B-3 t_{pp}	14	Pulse Pairing	(See Pulse Pairing Set Up)	±2	±5	ns
DP8464B-1 t_{pp}	14	Pulse Pairing	(See Pulse Pairing Set Up) at 25°C V_{CC} = 12V only	±0.5	±1	ns

Note 1: The temperature coefficient of the input impedance is typically 0.05% per degree C.

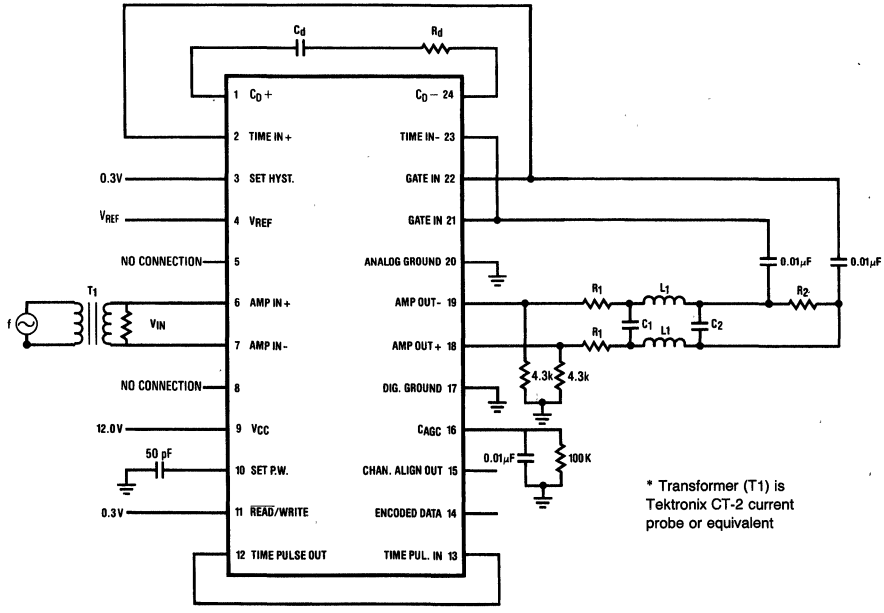
Note 2: The AGC Threshold is defined as the voltage across the Gate Channel Input (pins 21 and 22) when the voltage on C_{AGC} (pin 16) is 4.2V.

Note 3: The Set Hysteresis Threshold is defined as the minimum differential AC signal across the Gate Channel Input (pins 21 and 22) which causes the voltage on the Channel Alignment Output (pin 15) to change state.

Note 4: To prevent inductive coupling from the digital outputs to Amp In, the TTL outputs should not drive more than one ALS TTL load each.

Note 5: The following pins did not meet the 2000V ESD test with the human body model, 120 pF thru 1.5 kΩ: Pins 1, 2, 3, 10, 11, 12, 14, 21, 24.

Pulse Pairing Set Up



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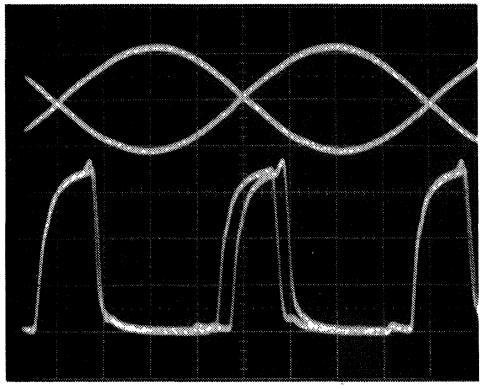
DP8464B

f = 2.5 MHz
V_{IN} = 40 mV_{pp} differential
V_{REF} = 0.50V
C_D = 50 pF
R_D = 430Ω

Filter

R1 = 240Ω R2 = 680Ω
C1 = 15 pF C2 = 100 pF
L1 = 4.7 μH

This is a 3 pole Bessel with the corner frequency at 7.5 MHz.



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Pulse Pairing Measurement

Connect a scope probe to pin 14 (Encoded Data Out) and trigger off its positive edge. Adjust the trigger holdoff so the scope first triggers off the pulse associated with the positive peak and then off the pulse associated with the negative peak (as shown in the scope photo below). Pulse pairing is displayed on the second pair of pulses on the display. If the second pulses are separated by 4 ns, then the pulse pairing for this part is ±2 ns.

Circuit Operation

The output from the read/write amplifier is AC coupled to the Amp Input of the DP8464B. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the Gate Channel Input four times the DC voltage on V_{REF}. Typically the signal on Amp Out will be set for 4 Vpp differential. Since the filter usually has a 6 dB loss, the signal on the Gate Channel Input will be 2 Vpp differential. The user should therefore set 0.5V on V_{REF} which can be done with a simple voltage divider from the +12V supply.

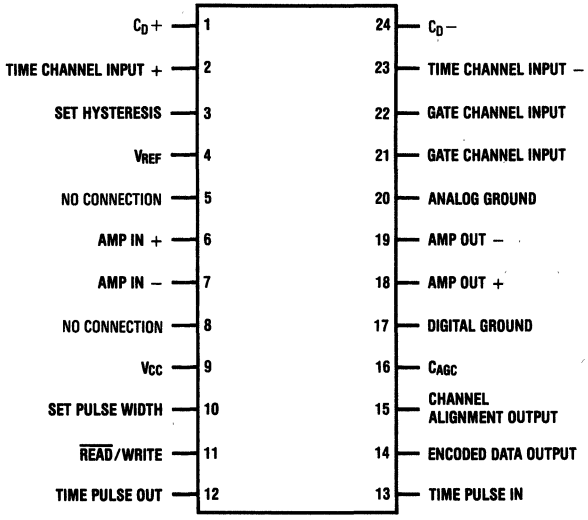
The peak detection is performed by feeding the output of the Amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering (the tendency to return to the baseline), the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised

Circuit Operation (Continued)

of a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level which will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bi-directional one shot. This pulse will clock the new data at the D input through to the output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flop is not changing since the logic level into the D input has not changed. The comparator circuitry is therefore a gating channel which prevents any noise near the baseline from contaminating the data. The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential AC signal across the Gate Channel Input must be larger than 0.6V before the output of the comparator will change states. In this case, the hysteresis is 30% of a 2V peak to peak differential signal at the gate channel input.

Connection Diagrams

Dual-In-Line (DIP) Package

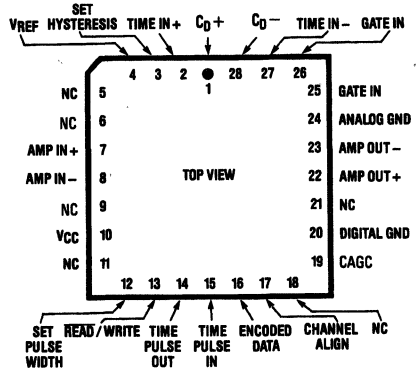


Top View

TL/F/5283–2

Order Number DP8464BN-3 or DP8464BN-2
See NS Package N24C

Plastic Chip Carrier (PCC) Package



TL/F/5283–30

Order Number DP8464BV-3, DP8464BV-2 or DP8464BV-1
See NS Package V28A

Pin Definitions

(All pin numbers refer to the 24 pin dual-in-line package)

Pin #	Name	Function
Power Supply		
9	V_{CC}	The supply is +12V ± 10%.
17	Digital Ground	Digital signals should be referenced to this pin.
20	Analog Ground	Analog signals should be referenced to this pin.
Analog Signals		
6	Amp In+	These are the differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
7	Amp In−	
18	Amp Out+	These are the differential outputs of the Amplifier. These outputs should be capacitively coupled to the gating channel filter (if required) and to the time channel filter.
19	Amp Out−	
22	Gate Channel Inputs	These are the differential inputs to the AGC block and the gating channel. These inputs must be capacitively coupled from the Amp Out.
21		
2	Time Channel Input+	These are the differential inputs to the differentiator in the time channel. In most applications, a filter between the Amp Out (pins 18 and 19) and these inputs is required to band limit the noise and to correct for any phase distortion introduced by the read circuitry. In all cases this input must be capacitively coupled to prevent disturbing the DC input level.
23	Time Channel Input−	
1	C_d+	The external differentiator network is connected between these two pins.
24	C_d−	
3	Set Hysteresis	The DC voltage on this pin sets the amount of hysteresis on the differential comparator. Typically this voltage can be established by a simple resistive divider from the positive supply.
4	V_{REF}	The AGC circuit adjusts the gain of the amplifier to make the differential peak to peak voltage on the Gate Channel Input equal to four times the DC voltage on this pin. This voltage can be established by a simple resistive divider from the positive supply.
5	No connection	
8	No connection	
16	C_{AGC}	The external capacitor for the AGC is connected between this pin and Analog Ground.

Pin #	Name	Function
Digital Signals		
10	Set Pulse Width	An external capacitor to control the pulse width of the Encoded Data Out is connected between this pin and Digital Ground.
11	$\overline{\text{Read}}$/Write	If this pin is low, the Pulse Detector is in the read mode and the chip is active. When this pin goes high, the pulse detector is forced into a standby mode. This is a standard TTL input.
12	Time Pulse Out	This is the TTL output from the bi-directional one shot following the differentiator. In most applications this can be connected directly to the Time Pulse In.
13	Time Pulse In	This is the TTL input to the clock of the D flip-flop. Usually this is connected directly to the Time Pulse Out pin.
15	Channel Alignment	This is the buffered output of the differential comparator with hysteresis. This is usually used in the initial system design and is not used in production.
14	Encoded Data Out	This is the standard TTL output whose leading edge, indicates the time position of the peaks.

Application Information

GENERAL DESCRIPTION

All pin numbers refer to 24 pin dual-in-line package.

The DP8464B Disk Pulse Detector utilizes analog and digital circuitry to detect amplitude peaks of the signal received from the Read/Write Amplifier. The analog signal from a disk is a series of pulses, the peaks of which correspond to 1's or flux reversals on the magnetic medium. The pulse detector must accurately determine the time position of these peaks. The peaks are indicated by the positive leading edge of a TTL compatible output pulse. This task is complicated by variable pulse amplitudes depending on the media type, head position, head type and read/write amplifier circuit gain. Additionally, as the bit density on the disk increases, the amplitude decreases and significant bit interaction occurs resulting in pulse distortion and shifting of the peaks.

The graph in *Figure 1* shows how the pulse amplitude varies with the number of flux reversals per inch (or recording density) for a given head disk system. The predominant disk applications are associated with the first two regions on this graph, Regions 1 and 2. Typical waveforms received by the pulse detector for these regions are shown next to the graph.

Application Information (Continued)

Region 1 is the high resolution area characterized by a large spread between flux reversals and a definite return to baseline (no signal) between these peaks. Pulses of this type are predominantly found in drives which use either thin film heads or plated media, or in drives which utilize run length limited codes (like the 2,7 code) which spread the distance between flux reversals.

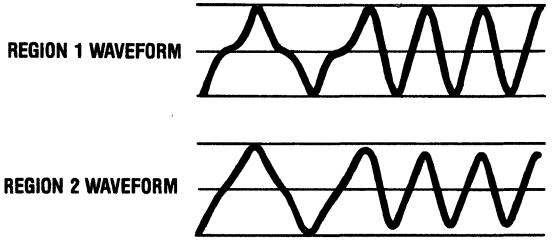
A Region 2 waveform will vary from a tendency to return to the baseline (called shouldering) to almost sinusoidal at the higher frequencies. These pulses come from drives which use limited frequency codes (such as MFM). The pulses may contain shouldering on the outer tracks of the disk and be nearly sinusoidal on the inner tracks since the flux density increases towards the inner track.

Detecting pulse peaks of waveforms of such variable characteristics requires a means of separating both noise and shouldering-caused errors from the true peaks. In the past, mild shoulder-caused errors were blocked by self-gating circuits (such as the "de-snaker"). These circuits fail when shouldering is extensive, hence the need for the DP8464B which includes a peak sensing circuit and an amplitude sensitive gating channel in parallel.

The main circuit blocks of the DP8464B are shown in *Figure 2*. The output from the read/write amplifier is fed directly to the Amp Input of the DP8464B. This is the input of a Gain Controlled Amplifier. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak-to-peak differential Gate Channel input voltage four times the DC voltage on V_{REF}.

The peak detection is performed by feeding the output of the Gain Controlled Amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering (the tendency to return to the baseline) as seen in Region 1 and the upper part of Region 2, the differentiator will also respond to noise near the baseline. To avoid this, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel comprises a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have valid data out, the input amplitude must first cross the hysteresis level. This will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bi-directional one shot. This pulse will clock in the new data on the D input, which will appear at the Q output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flop is not changing since the logic level into the D input has not yet changed. The comparator circuitry is therefore a gating channel to prevent any noise near the baseline from contaminating the data.

The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential Gate Channel Input must be larger than 0.6V (±0.3V) before the output of the comparator will change states. The Time Pulse Out, Encoded Data, and Channel Alignment Output are designed to drive 1 standard TTL gate.



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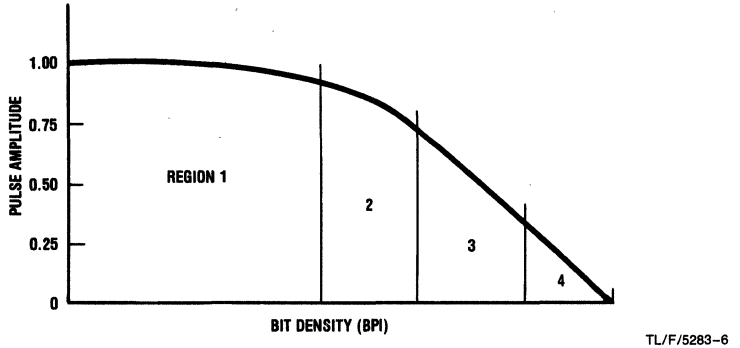

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FIGURE 1. Pulse Amplitude vs. Bit Density with Typical Waveforms

Block Diagram

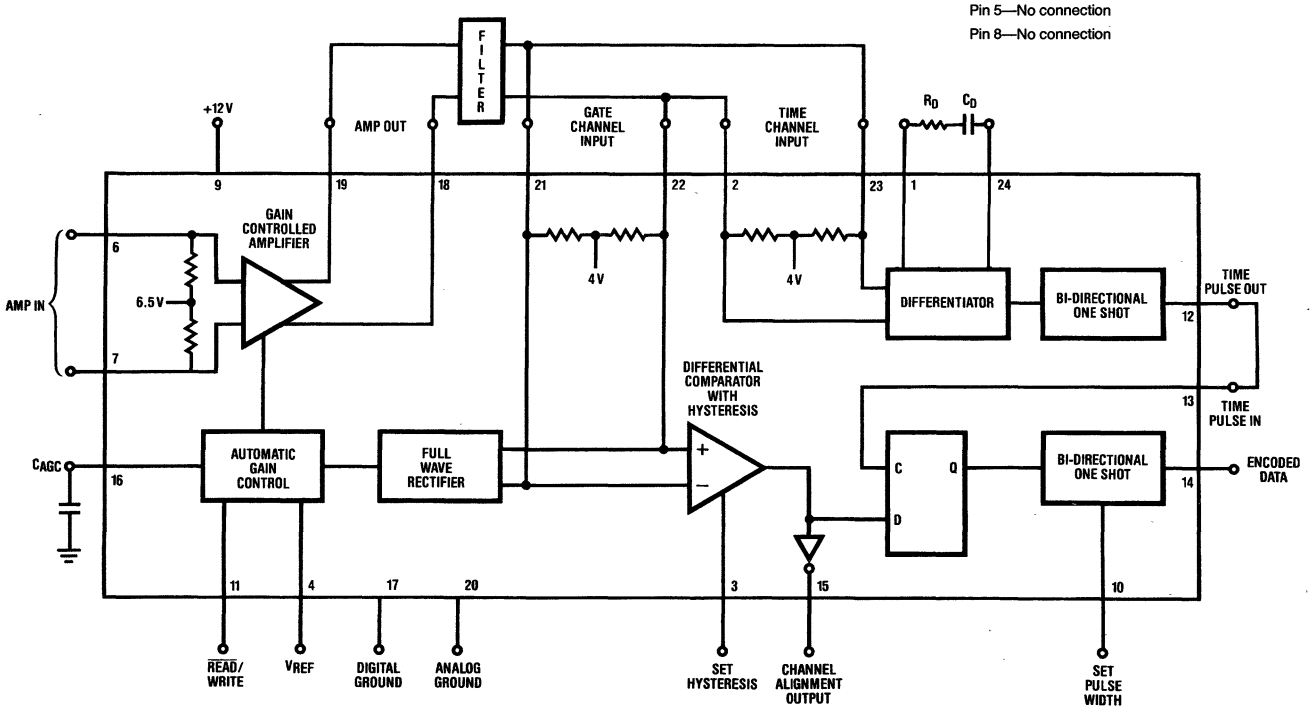

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FIGURE 2. DP8464B Block Diagram, Region 1 Connection

Application Information (Continued)

GAIN CONTROLLED AMPLIFIER

The purpose of the Gain Controlled Amplifier is to increase the differential input signal to a fixed amplitude while maintaining the exact shape of the input waveform. The Gain Controlled Amplifier is designed to accept input signals from 20 mVpp to 660 mVpp differential and amplify that signal to 4 Vpp differential. The gain is therefore from 6 to 200 and is controlled by the automatic gain control (AGC) loop. The amplifier output is actually capable of delivering typically 5 Vpp differential output but the parts are only tested and guaranteed to 4 Vpp.

The input to the Gain Controlled Amplifier is shown in *Figure 3*. The value of the input capacitors should be selected so that the pole formed by the coupling capacitor and the 1k bias resistor is a factor of 10 lower than the lowest signal frequency. These input bias resistors have a ±20% tolerance and a temperature coefficient of 0.05% per degree C. When the pulse detector is in the write mode, these bias resistors are automatically shunted by 425Ω resistors. This allows the input circuit to recover quickly from the large transients encountered during a write to read transition. The input impedance to the amplifier is therefore 1k during read operations and 300Ω during write operations.

The output of the Gain Controlled Amplifier is shown in *Figure 4*. The outputs are biased at (12V − (0.75 mA × 2.4k) − 0.75V) or 9.5V. Since each output will swing ±1V (4 Vpp differential), each output pin will swing from 8.5V to 10.5V. If the total differential load placed on the output is 1k, (see *Figure 5*) then the circuit must supply 2V/1k or 2 mA. Since the output is class A, external resistors to ground must be used to provide the sink current. In this case, in order to sink 2 mA at the lowest voltage, then (8.5V/2 mA) or an external 4.3k resistor from each output to ground is required. Note that the circuit has additional margin since the internal 2 mA current sources were not included in the calculation. Typically the output impedance of the Gain Controlled Amplifier is 17Ω, and the −3 dB bandwidth is greater than 20 MHz.

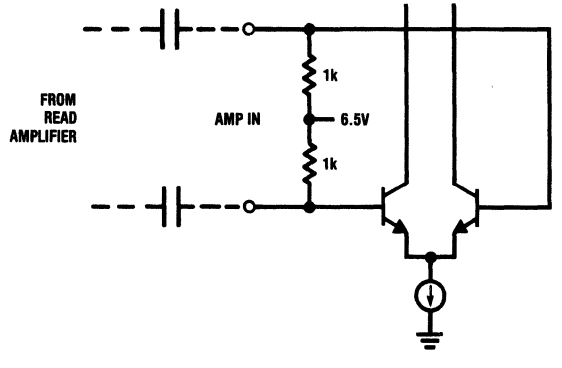

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FIGURE 3. Input to Gain Controlled Amplifier

Application Information (Continued)

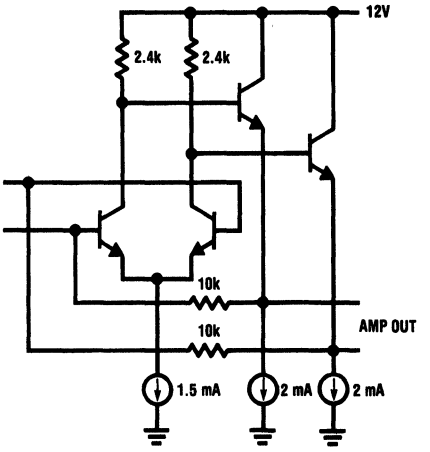

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FIGURE 4. Output of Gain Controlled Amplifier

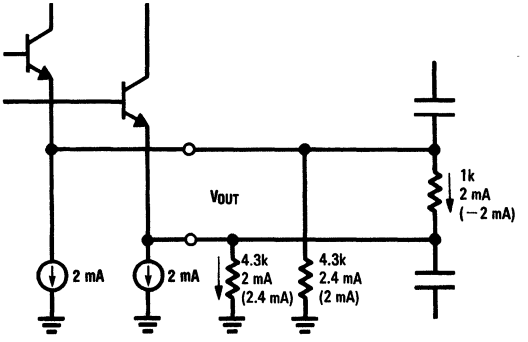

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FIGURE 5. Output Stage with 1k Differential Load

Application Information (Continued)

AUTOMATIC GAIN CONTROL (AGC)

The Automatic Gain Control holds the signal level at the Gate Channel Input at a constant level by controlling the gain of the Gain Controlled Amplifier. This is necessary because the amplitude of the input signal will vary with track location, variations in the magnetic film, and differences in the actual recording amplitude. The Gain Controlled Amplifier is designed for a maximum 4 Vpp differential output. To prevent the Gain Controlled Amplifier from saturating, the V_{REF} level must be set so the maximum amplifier output voltage is 4 Vpp. The AGC will force the differential peak-to-peak signal on the Gate Channel Input to be four times the voltage applied to the V_{REF} pin. Normally some kind of filter is connected between the Gain Controlled Amplifier's output and the Gate Channel Input. Typically this filter has a 6 dB insertion loss in its pass band. Since the AGC holds the amplitude at the Gate Channel Input constant, this 6 dB loss through the Gate Channel filter will cause the Gain Controlled Amplifier's output to be 6 dB larger than the Gate Channel Input.

The AGC loop starts out in the high gain mode. When the input signal is larger than expected, the AGC loop will quickly reduce the amplifier gain so the peak-to-peak differential voltage on the Gate Channel Input remains four times the voltage on V_{REF}. If the input amplitude suddenly drops, the AGC loop will slowly increase the amplifier gain until the differential peak-to-peak Gate Channel Input voltage again reaches four times V_{REF}. The AGC loop requires several peaks to react to an increased input signal. In order to recover the exact peak timing during this transition, the V_{OUT} level must be set somewhat lower than the maximum of 4 Vpp. For instance, if the V_{REF} is 0.5V, and if the loss in the gate channel filter is 6 dB, then the Amp Output is 4 Vpp. If the Amp Input suddenly increases 30%, the amplifier may saturate and the timing for a few peaks may be disturbed until the AGC reduces the amplifier gain. If the peak detection is critical during this time, the system may fail. The proper operation, for this example, is to set the V_{REF} at 0.35V so the amplifier will not saturate if the input suddenly increases 30%.

A simplified circuit of the AGC block is shown in *Figure 6.* When the full wave rectified signal from the Gate Channel Input is greater than V_{REF}, the voltage on the collector of transistor T1 will increase and charge up the external capacitor C_{AGC} through T2. The typical available charging current is 2.5 mA. Conversely, if this input is less than V_{REF}, transistor T2 will be off, so the capacitor C_{AGC} will be discharged by the base current going into the Darlington T3 and T4. This discharge current is approximately 1 μA. The voltage across C_{AGC} controls the gain of the Gain Controlled Amplifier. This voltage will vary from typically 3.4V at the highest gain to 4.5V at the lowest gain.

When the AGC circuit has not received an input signal for a long time, the base current of the Darlington will discharge the external C_{AGC} to 3.4V. The amplifier will now be at its highest gain. When a large signal comes in, the external C_{AGC} will be charged up with the 2.4 mA from T2 thereby reducing the gain of the amplifier. The formula, $I = C \times (dV/dt)$ can be used to calculate the time required for the amplifier to go from a gain of 200 to a gain of 6. For instance, if $C_{AGC} = 0.01\ \mu f$, the charging current I is 2.4 mA, and the dV required for the amplifier to go through its gain range is 1.1V, then

$$dt = (0.01\ \mu F \times 1.1V)/(2.4\ mA) \text{ or } 4.6\ \mu s.$$

In reality, the gain does not change this quickly since the C_{AGC} would only be charging during a portion of the input waveform.

By using the same argument, the time required to increase the amplifier gain after the input has been suddenly reduced can be calculated. This time, the discharging current is only 1 μa so

$$dt = (0.01\ \mu F \times 1.1V)/1\ \mu A) \text{ or } 11\ ms.$$

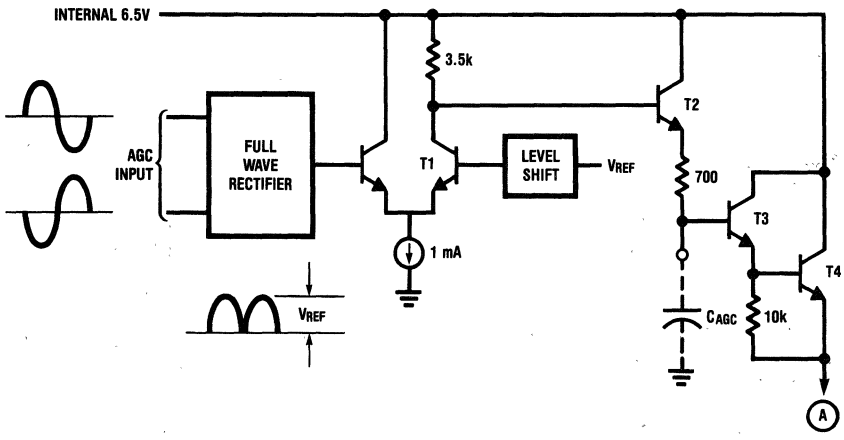

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FIGURE 6. Simplified AGC Circuit

Application Information (Continued)

This time can be decreased by placing an external resistor across the C_{AGC}. For instance, if a 100k resistor is placed in parallel with C_{AGC}, then the discharge current is 40 μA. The time required to increase the amplifier gain is now 40 times faster or 275 μs. If this external resistor is made even smaller, say 10k, then the discharge time will go to 27.5 μs. Now however, there is another problem introduced. The response time of the AGC is so fast that it distorts the signal at the output of the Gain Controlled Amplifier. Distortion of the signal at the Amplifier Output can affect the time position of the peaks of this signal. Be sure to check this distortion over the range of input levels you expect to encounter, when choosing the external R and C values for the AGC.

If the value of the bleed resistor across the C_{AGC} is decreased (in order to equalize the AGC attack and decay times) the value of C_{AGC} must be increased in order to maintain an AGC response that does not distort the signal. There is a second order effect on the amplitude that results from this attack and decay time equalization. Referring to *Figure 2*, notice that the AGC is driven from a full wave rectified version of the Gate Channel Input signal. When the AGC is operated normally (ie. fast attack and slow decay) the voltage that appears across C_{AGC} is the peak detected value of this full wave rectified waveform. However, if you equalize the AGC attack and decay times the voltage across C_{AGC} is the RMS voltage (0.707 times the peak) of the full wave rectified waveform. Thus, the voltage across C_{AGC} is less and the amplitude out of the Gain Controlled Amplifier will consequently be 1.4 times larger.

It is possible to externally drive the C_{AGC} pin to control the gain of the amplifier. It must be noted that the gain of the amplifier is not always exactly 200 when the voltage on C_{AGC} is 3.4V. The transfer curve between the gain of the amplifier and the voltage on C_{AGC} is only approximate. This transfer curve will vary between parts and with temperature. Care should be taken to prevent the voltage on the C_{AGC} pin from going below ground or above 5.5V. *Figure 7* shows a typical curve of the Gain Controlled Amplifier Gain vs. the voltage across C_{AGC} (Vpin 16.)

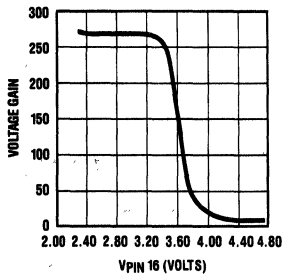

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FIGURE 7. Gain Controlled Amplifier Gain vs. Vpin 16

It is possible to change the time constant of the AGC circuit by switching in different external components at the desired times. For instance, as shown in *Figure 8*, an external open collector TTL gate and resistor can be added in parallel with C_{AGC} to decrease the AGC response time. Similarly, an external capacitor could be switched in to increase the response time. Since in the absence of an external resistor the discharge time of C_{AGC} is much longer than the attack time there may be some applications where it is desirable to switch in a parallel resistor to quickly discharge C_{AGC} then switch it out to force a quick attack. Because of the quick attack time, the AGC obtains the proper level quicker than it would had C_{AGC} simply been allowed to discharge to the new level.

There are some applications where it is desirable to hold the AGC level for a period of time. This can be done by raising the $\overline{\text{READ}}$/WRITE pin. This will shut off the input circuitry, and it will take time (about 2.5 μs) for the circuit to recover when going back into the read mode. *Figure 9* shows a method to hold the AGC level while remaining in the read mode (which could be used in embedded servo applications). If the voltage on V_{REF} is raised to 3V, then the amplifier output voltage cannot get large enough to turn on the circuitry to charge up C_{AGC}. For this to work properly, there can not be a large discharge current path (resistor in parallel with C_{AGC}) across C_{AGC}. The AGC block can be bypassed altogether by connecting V_{REF} to 3V. In this way, the user can use his own AGC circuit to drive the C_{AGC} pin directly.

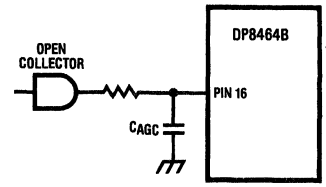

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FIGURE 8. Circuit to Decrease AGC Response Time

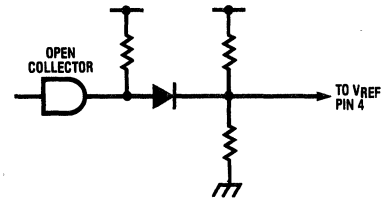

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FIGURE 9. Circuit for AGC Hold

$\overline{\text{READ}}$/WRITE

In the normal read mode, the signal from the read/write head amplifier is in the range of 20 mVpp to 660 mVpp. However, when data is being written to the disk, the signal coming into the analog input of the pulse detector will be on the order of 600 mV. Such a large signal will disturb the AGC level and would probably saturate the amplifier. In addition, if a different read/write amplifier is selected, there will be a transient introduced because the offset of the preamplifiers are not matched. A $\overline{\text{READ}}$/WRITE input pin has been provided to minimize these effects to the pulse detector. This is a standard TTL input.

When the $\overline{\text{READ}}$/WRITE pin is low, the pulse detector is in the read mode. When the $\overline{\text{READ}}$/WRITE pin is taken high, three things happen. First, the 1k resistors across the AMP IN pins are shunted by 300Ω resistors, as described previously in the Gain Controlled Amplifier section. Next, the amplifier is squelched so there is no signal on the Amp Output.

Application Information (Continued)

Finally, the previous AGC level is held. This AGC hold function is accomplished by not allowing any current to charge up the external C_{AGC}. The voltage across this capacitor will slowly reduce due to the bias current into the Darlington (see *Figure 6*) or through any resistor placed in parallel with C_{AGC}. Therefore, as described in the Automatic Gain Control section, the gain of the amplifier will slowly increase. All of these three events happen simultaneously.

When the $\overline{\text{READ}}$/WRITE input is returned low, the pulse detector will go back to the read mode in a specific sequence. First of all, the input impedance at the Amp In is returned to 1k. Then, after approximately 1 μs, the Gain Controlled Amplifier is taken out of the squelch mode, and finally approximately 1 μs after that, the AGC circuit is turned back on. This return to the read mode is designed to minimize analog transients in order to provide stable operation after 2.5 μs. It is very important that the analog input be stable before the chip is returned to the read mode. It is recommended that other than when writing, the Pulse Detector be in the read mode at all times in order to prevent the 2.5 μs delay from slowing up the system. The $\overline{\text{READ}}$/WRITE pin may be connected to the Write Gate output of a controller (such as the DP8466 Disk Data Controller).

TIME CHANNEL FILTER

The peak detection is performed by feeding the output of the Gain Controlled Amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. The differentiator can also respond to noise near the baseline, in which case the comparator gating channel will inhibit the output. The purpose of the external filter is to bandwidth limit the incoming signal for noise considerations. Care must be used in the design of this filter to ensure the delay is not a function of frequency. For this reason, a high order Bessel filter with its constant group delay characteristics can be used in this application. Often, this filter must be specifically designed to correct errors introduced by the non-ideal phase characteristics of the input read head. The typcial −3 dB point for this filter is around 1.5 times the highest recorded frequency. The design of this filter is complex and will not be discussed here. However, the following discussion does give a feel for some of the considerations involved in the filter design. The reader is referred to reference #3 listed at the end of the Applications Notes for further filter design information.

Figure 10 shows a typical Region 1 waveform where there is no bit interaction. This waveform is primarily the sum of the fundamental frequency and its 3rd harmonic (higher odd harmonics are present when there is more shouldering).

If the filter is to preserve this wave shape (this would be the case if no read/write head phase compensation were necessary) then the phase relationship between the fundamental frequency and its harmonics must not be altered. *Figure 11* shows the output when the 3rd harmonic has the proper magnitude, but the phase relationship is not maintained. The result is that the output waveform is not the same shape as the input (in a severe case it may be almost unrecognizable) and the time position of the peaks has been altered.

One electrical parameter which describes how well a filter will preserve a wave shape is called group delay. Group delay is defined as the change in phase divided by the change in frequency. If the group delay is constant over the

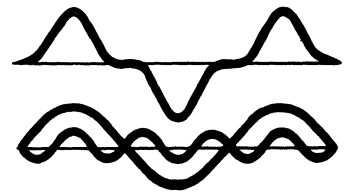

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FIGURE 10. Typical Region 1 Waveform

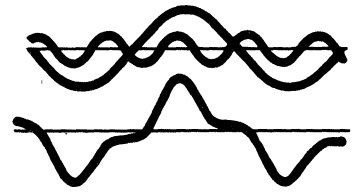

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FIGURE 11. Region 1 Waveform with the Incorrect Phase Relationship

frequencies of interest, then the wave shape will be maintained. An MFM coded signal will contain three basic frequency components for the various digital patterns of data. For instance, a 10 Megabit/sec MFM signal will consist of analog frequencies of 2.5 MHz, 3.33 MHz and 5 MHz. On the outer track the bit density is the lowest and the 5 and 3.33 MHz signals will look sinusoidal while the 2.5 MHz signal will have a tendency to return to the baseline. This returning to the baseline is called shouldering and is illustrated in *Figure 10*. Since this shouldering is rich in 3rd harmonic—the 2.5 MHz signal will have a strong 7.5 MHz component. The 10 Megabit/sec MFM signal will therefore have 2.5 MHz, 3.33 MHz, 5 MHz, and 7.5 MHz components which must be filtered with constant group delay in order to reproduce the original waveform. For example, if the phase shift through the filter at 2.5 MHz is 33.3°, then at 3.33 MHz the phase shift must be 44.3°, at 5 MHz—66.6°, and at 7.5 MHz—99.9°. The group delay $\frac{d\theta}{dt}$ for this case is 13.32°/MHz. This can be better interpreted as a time delay. 33.3° of a 2.5 MHz signal is equivalent to (33.3/360) × (1/2.5 MHz) or 37 ns. Similarly, 66.6° on a 5 MHz signal is (66.6/360) × (1/5 MHz) = 37 ns.

The third order Bessel Filter as shown in the 10 Mbit/sec. pulse pairing measurement board on the data sheet is designed for a constant group delay and a −3 dB point of 7.5 MHz. At this frequency the delay through the filter is 35 ns. The Gain Controlled Amplifier of the DP8464B is designed for a group delay of a 7.8 ns ±0.5 ns for frequencies up to 7.5 MHz. The 7.8 ns delay in the Gain Controlled Amplifier and the 37 ns delay in the Bessel Filter do not introduce any timing error, only a delay of 44.3 ns from the Amp Input to the output of the filter.

DIFFERENTIATOR

A simplified circuit of the first stage of the differentiator is shown in *Figure 12*. The voltages at V3 and V4 are simply two diodes down from V1 and V2. Therefore the voltage

Application Information (Continued)

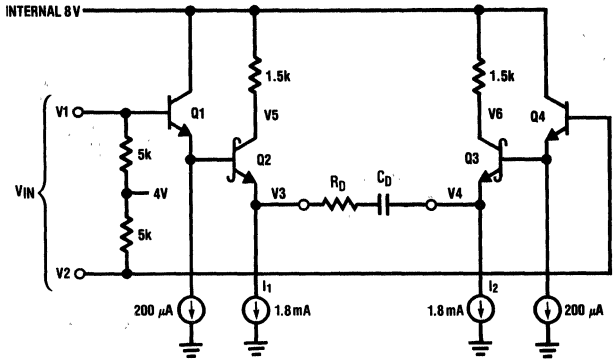

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FIGURE 12. Simplified Differentiator First Stage

across the external differentiator network (C_d in series with R_d) is the differential input voltage V1 − V2. When R_d is zero, the current through C_d is $I = C \times (dV/dt)$ or $C_d \times (dV_{IN}/dt)$. The Q2 collector current is the sum of the 1.8 mA current source plus the current through C_d or

$$1.8\ mA + C_d \times (dV_{IN}/dt).$$

Similarly, the Q3 collector current is

$$1.8\ mA - C_d \times (dV_{IN}/dt).$$

Therefore, the differentiator output voltage, V5 − V6, is

$$1.5k \times 2 \times C_d \times (dV_{IN}/dt).$$

The input is at a peak when V5 − V6 = 0V.

The differentiator network (C_d and R_d) should be selected so the maximum current into the differentiator network is not greater than the minimum current of I1 and I2 over temperature. In the electrical specifications, the minimum current is specified for 1.4 mA (I_{Cd} Current into Pin 1 and 24 that discharges C_d). For example, the highest analog frequency in a 10 Megabit/sec, MFM signal is 5 MHz. Since the AGC loop has forced the input to the differentiator to 2 V_{PP} (which includes the 6 dB loss of the filter), then the voltage across the capacitor (assuming R_d is 0) is:

$$V_{IN} = 1 \times \sin(2 \times \pi \times 5E6 \times t)$$

and

$$dV_{IN}/dt = 1 \times 2 \times \pi \times 5E6 \times \cos(2 \times \pi \times 5E6 \times t)$$

and the maximum slope is

$$(dV_{IN}/dt)max = 1 \times 2 \times \pi \times 5E6 = 314E5\ V/sec.$$

For this example, C_d can now be calculated. Since $I = C \times (dV/dt)$, then for I = 1.4 mA, dV/dt = 314E5, then the maximum C_d must equal 45 pF. From this example, a following simple design equation for the value of C_d can be derived.

$$C_d = 445/(V_{IN} \times f_{max})$$

where

C_d is the maximum external differentiator capacitor in pF

V_{IN} is the peak to peak differential Time Channel input voltage

f_{max} is the maximum analog frequency in MHz

Note that this is the maximum value for the capacitor when the series resistor R_d is zero. The value of the capacitor can be increased if a series resistor is used, but the maximum current through the differentiator network must not exceed 1.4 mA. If too large a value for C_d is used, the delay through the differentiator will become dependent on frequency. This will not show up in a single frequency test such as a test for pulse pairing.

For the MFM code, the maximum analog frequency is ½ the data rate. For the ½(2,7) code, the maximum analog frequency is ⅓ the data rate. The above sinusoidal analysis is valid as long as the highest frequency on the outer track is nearly sinusoidal. If, however, there is significant shouldering of this signal then the value of C_d should be reduced accordingly.

The following table summarizes the value of C_d to use for a 2 V_{pp} differential signal to the time channel input.

Data Rate	Code	Maximum Frequency	C_d
5 mbits/sec	MFM	2.5 MHz	90 pF
5 mbits/sec	2,7	1.6 MHz	140 pF
10 mbits/sec	MFM	5.0 MHz	45 pF
10 mbits/sec	2,7	3.3 MHz	67 pF

As noted above, the value of the capacitor can be increased if a series resistor is used, but the maximum current through the differentiator network must not exceed 1.4 mA. For example, the components used in the Pulse Pairing Setup (see AC Electrical Specifications) are for a typical 10 Mbits/sec MFM drive. The combination of the C_d of 50 pF and the R_d of 430Ω gives a combined impedance of 768Ω at the highest frequency of 5 MHz. This gives a maximum current of 1.3 mA—well below the 1.4 mA limit.

A resistor is placed in series with C_d in order to bandlimit the differentiator response. This resistor also has an effect on the phase linearity of the differentiator. An ideal differentiator produces an output that is 90 degree phase shifted from the input regardless of the input frequency. The presence of the series resistor produces an output phase shift that is less than 90 degrees and changes with the input frequency. This resistor can be used to correct for frequency related phase problems encountered elsewhere in the read path.

Application Information (Continued)

To properly decode the information on the disk, the read channel must determine if there is a peak (or a "1") during a period of time called a detection window. The detection window for MFM and the (2,7) code is

$$1/(2 \times \text{data bit rate}).$$

This detection window must accommodate errors in many parts of the system including filters, data separator, and peak shift variations in the data pattern. The pulse pairing of the DP8464B should be included in the error budget calculation.

Unequal delays through the bi-directional one shots will contribute to pulse pairing. To minimize this effect, pin 2 should be connected to 22 and pin 23 should be connected to 21. If connected this way, the delays tend to cancel. For the PCC Package, Pin 26 to Pin 2, and Pin 25 to Pin 27.

DIFFERENTIAL COMPARATOR WITH HYSTERESIS

The actual peak detection is done in the time channel with the differentiator. Unfortunately, the differentiator not only responds to signal peaks but also responds to noise at the baseline. In order to prevent this noise from generating false data, the signal at the output of the Gain Controlled Amplifier is also passed through a gating channel which prevents any output change before the input signal has crossed an established level. This gating channel comprises a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is set externally via the Set Hysteresis pin. The amount of hysteresis is twice the voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential input signal must be larger than 0.6V($\pm$0.3V) before the output of the comparator will change states. The 0.6V hysteresis represents 30% of a typical 2V differential input signal level to the gating channel. The hysteresis level is usually set between 15% to 40% of the differential input signal.

The operation of the gating channel is shown in *Figure 13*. At the top is a typical Region 1 waveform which exhibits shouldering on the lowest frequency and is almost sinusoidal on the highest frequency. In this example, this waveform is fed to both the timing and the gating channel. The hysteresis level (of about 25%) has been drawn on this waveform. The second waveform is the output of the differentiator and its bi-directional one shot. This is the waveform on the Time Pulse Out pin. While there is a positive edge pulse at each peak, there is also noise at the shoulders. In this example, the Time Pulse Out is connected directly to the Time Pulse In without any external delay. This output is therefore the clock for the D flip-flop.

The third waveform in *Figure 13* is the output of the Comparator with Hysteresis which goes to the D input of the flip-flop. The true peaks are the first positive edges of the Time Pulse Out which occur after the output of the comparator has changed states. The D flip-flop will "clock" in these valid peaks to the output bi-directional one shot. Therefore, the noise pulses (due to the differentiator responding to noise at the baseline) just "clock" in the old data through the flip-flop and the output does not change.

The Q output of the flip-flop drives the output bidirectional one-shot which generates the positive edges corresponding to the peaks. The width of the data pulses can be controlled by an external capacitor from the Set Pulse Width pin to ground. This pulse width can be adjusted from 20 ns to ½ the period of the highest frequency. Typical values for this capacitor are 20 pF for a 25 ns pulse width to 100 pF for a 100 ns pulse.

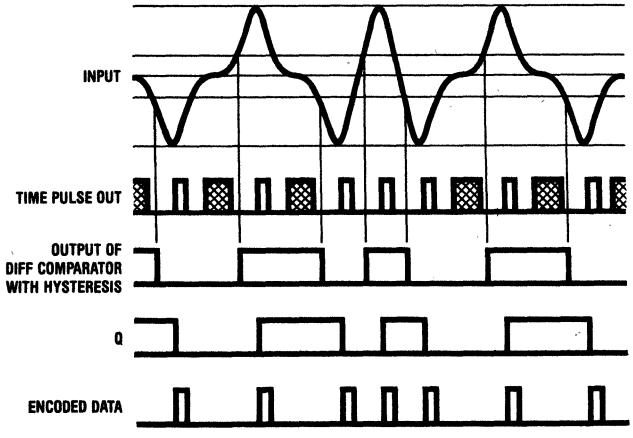

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FIGURE 13. Time and Gate Channel Operation for Region 1 Signals

Application Information (Continued)

PULSE DETECTOR OPERATION IN REGIONS 1 AND 2

Figure 14 shows the input waveform for the lowest frequency followed by the highest frequency for an MFM code. In MFM the highest frequency is twice the lowest frequency. The outer track has the least flux changes per inch (FCI) and is illustrated in the waveforms at the top. There is so much room between the pulses that the signal returns to the baseline for the lowest frequency while there is shouldering at the highest frequency. As you go towards the inner track, the pulses become more crowded and bit interaction occurs. At the third curve down (N × 1.7 FCI), there is shouldering at the lowest frequency while the highest frequency is almost sinusoidal. At higher bit densities, the lowest frequency looks sinusoidal, while the highest frequency is decreasing in amplitude. In *Figure 14*, the first three waveforms are examples of Region 1 operation (very little change in amplitude with frequency). The last two waveforms are examples of Region 2 operation.

In a disk system, the bit density changes about a factor of 1.7 between the inner and the outer track. For instance, if the input waveform for the F-2F signal on the inner track of a system looks similar to waveform #4 in *Figure 14* (N × 2.2 FCI), then the outer track will have a bit density that is approximately N × 2.2/1.7 or N × 1.3 FCI. This is shown in the second waveform. Tracks half the way in will have a bit density of the average between the inner and outer tracks, in this case N × 1.7 FCI which is illustrated in the third waveform. Note that the analog waveforms change considerably with track location. Self-gating circuits ("desnakers") can be used in MFM systems which operate in these last three curves (from N × 1.7 FCI to N × 2.9 FCI). If the FCI becomes much less, the shouldering on the lowest frequency will let in too much noise. If the FCI is increased, the peak resolution gets very poor. Now we can compare these waveforms to longer run length limited codes.

Figure 15 shows the analog waveform for the lowest frequency followed by the highest frequency for a 2,7 code. In the 2,7 code, the frequency range is from F to 2.66 × F. Unlike the MFM code, there is no region where the self-gating "desnaker" will work on both the inner and outer tracks.

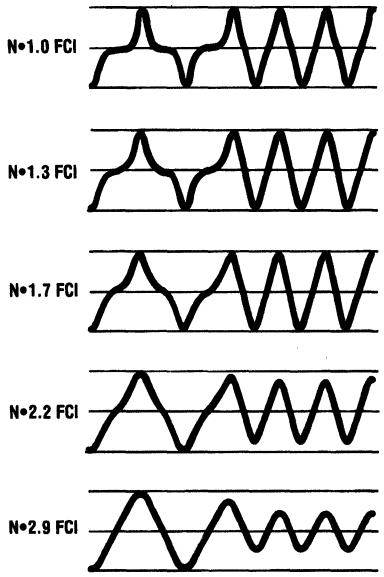

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FIGURE 14. MFM F-2F Pulse Waveforms for Various Flux Changes per Inch

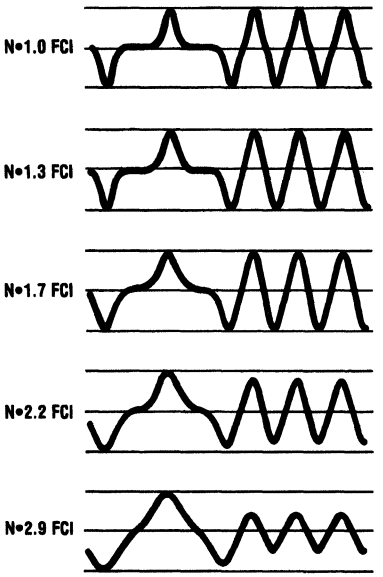

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FIGURE 15. F-2.66 × F Pulse Waveforms for Various Flux Changes per Inch

Application Information (Continued)

The simplest operation is for systems operating entirely in Region 1, that is, no amplitude reduction between the highest and the lowest frequency at the inner track. The inner track is specified because the pulse interaction is most severe on the inner track. For Region 1 operation, only the Time Channel filter is required, so the Gate Channel Input is connected to the Time Channel Input. Since no external time delay is required to align the time and gate channels, the Time Pulse Out is connected directly to the Time Pulse In. The Region 1 connection is shown in *Figure 2*. The internal timing for this operation is shown in *Figure 13*.

If there is significant amplitude reduction at the highest frequency, the peak detection becomes more complex. If the worst case waveform is like the fourth waveform on *Figure 14*, then the Region 1 connection might still work satisfactorily. However, if the input begins to approach the fifth waveform, this system configuration will completely fail. One problem is that the AGC will respond to the frequency dependent amplitude modulation and distort the waveform.

Figure 16 illustrates this problem which is encountered in systems operating in Region 2. If the input digital pattern suddenly shifts from a high frequency to a low frequency, the bit density may shift from the 70% level on the BPI curve of *Figure 1* to a point at 90% on the BPI curve. As shown, the AGC loop is correcting for this frequency-induced change in amplitude by quickly decreasing the amplifier gain. The situation gets worse if the input digital pattern shifts back to a high frequency. The AGC loop now cannot quickly increase the amplifier gain, so the output waveform will very slowly increase. The AGC response to frequency related amplitude change is not desirable since the AGC is now distorting the input waveform. This can be prevented by inserting a lead network between the Gain Controlled Amplifier's output and the AGC input, as shown in *Figure 17*. This will increase the amplitude of the higher frequency into the AGC, thereby preventing the AGC from changing gain.

Another problem encountered in Region 2 operation is that the amplitude of the highest frequency may be so low that it may not trip the hysteresis level. If this happens, these peaks would not be gated on to the output. This problem can also be corrected by placing a separate filter to the gating channel which will make the amplitude of the highest frequency equal the amplitude of the lowest frequency. This is illustrated in the following example.

Consider a disk system which uses the 2,7 code and has an input at the inner track which looks like the fifth waveform in *Figure 15*. Since the flux density on the outer track is 1/1.7 times the flux density of the inner track, the outer track waveform will look like the third waveform. One filter cannot perfectly compensate both these extremes, so we design to compensate a waveform between these two. The track which is ⅔ of the way in towards the inner track is a good compromise. The filter in this example is a single zero placed such that the lowest frequency followed by the highest frequency have the same amplitude on the track ⅔ of the way in. *Figure 18* shows the operation of the inner track of this example. While the gating channel filter has made the amplitudes of the two frequencies nearly the same, the time relationship to the Time Channel Input has not been preserved. The proper operation is to have the positive edge of the signal at the Time Pulse In pin, which corresponds to a peak, be the first positive edge after the output of the comparator has changed states. This can be accomplished either of two ways. One way is to insert an external delay between the Time Pulse Out and the Time Pulse In as shown in *Figure 18*. The required delay can be determined by comparing the Time Pulse Out to the Channel Alignment Output with both external filters in the circuit. Another way is to design the Time Channel Filter with more group delay. This will probably require additional poles.

Figure 19 shows the outer track operation of our example. Notice how the system has taken care of the shoulder-induced-noise on the Time Pulse Out. The external delay has shifted the Time Pulse In so the noise is not clocking in new data to the flip-flop. It is important to select this delay such that the positive edge corresponding to a signal peak is always the first positive edge after the output of the comparator has changed states.

While the gating filter has equalized the amplitudes between the highest and the lowest frequency, the amplitude between the inner and the outer track has not been held constant. This can be seen by comparing the Gate Channel Input between *Figure 18* and *Figure 19*. In order to avoid saturating the Gain Controlled Amplifier, the voltage on the V_{REF} pin must be set so that the voltage out of the Gain Controlled Amplifier is 4 Vpp or less for all tracks. The low frequency signal on the inner track contains far more fundamental frequency than the low frequency signal on the outer track. Consequently, the low frequency inner track signal will experience more attenuation than the low frequency outer track signal in passing through the gating channel filter which, for this example, has been optimized to pass higher frequencies. The AGC tends to hold the input to the gating channel constant for a fixed V_{REF} level. Therefore the largest output from the Gain Controlled Amplifier is for the low frequency inner track signal. The voltage on V_{REF} should be adjusted so that the differential output swing of the Gain Controlled Amplifier is 4 Vpp maximum for this signal. This means that the output voltage on the outer track will be less than 4 Vpp.

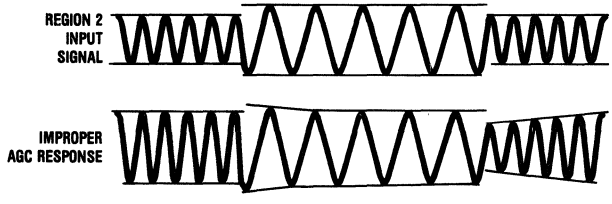

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FIGURE 16. Improper AGC Response to Region 2 Signal

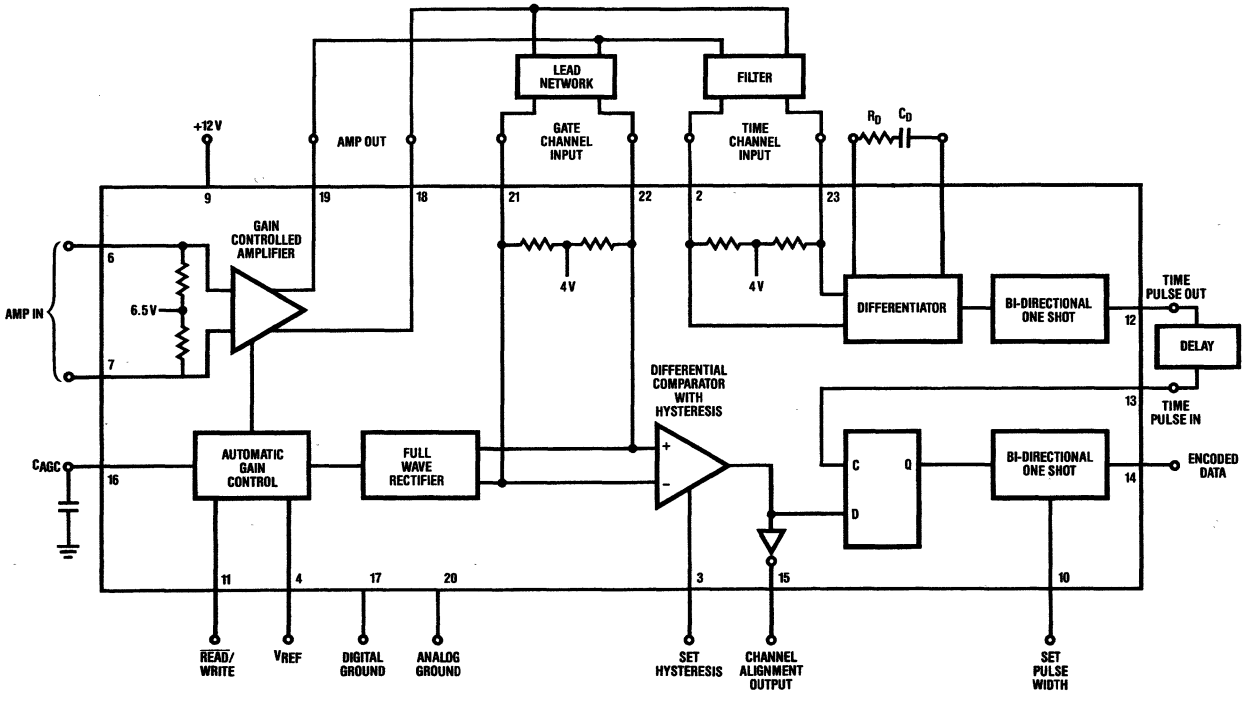

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FIGURE 17. Circuit Connection for Region 2 Operation

Application Information (Continued)

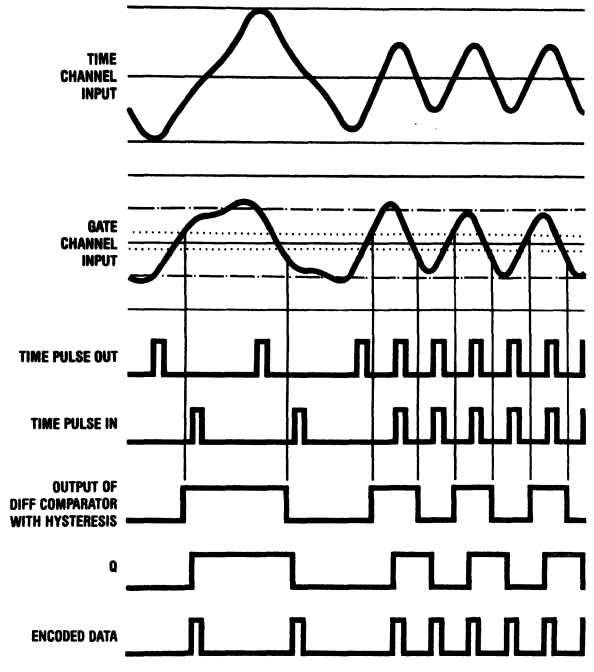

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FIGURE 18. Region 2 Inner Track Operation

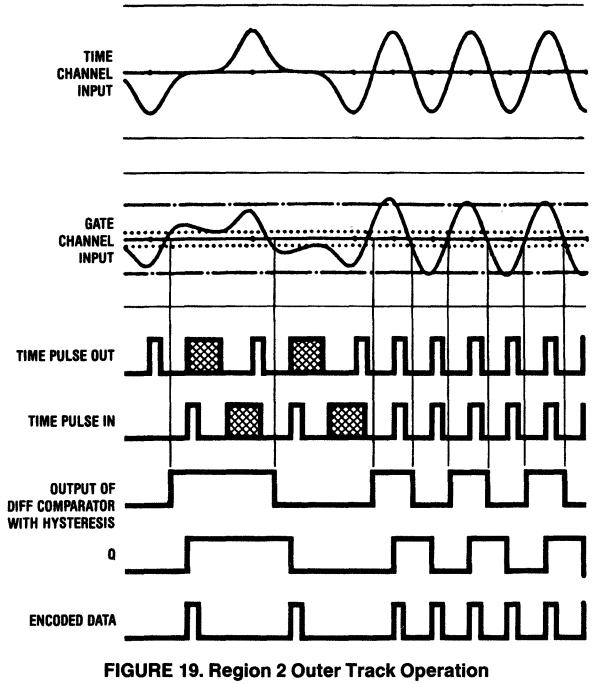

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FIGURE 19. Region 2 Outer Track Operation

Application Information (Continued)

Another troublesome input pattern which should be investigated is a high frequency triplet surrounded by the lowest frequency as shown in *Figure 20*. Since the center bit of the triplet does not rise very much above the baseline, there is the possibility it will not trip the hysteresis level. This pattern should be checked to ensure the gating channel filter raises this center bit enough for the proper operation of the gating channel. The operation of the triplet in the previous example is shown in *Figure 21*.

LAYOUT CONSIDERATIONS

Figure 22 is a top view of the component layout for the DP8464B application board whose schematic is shown in *Figure 23*. Care must be exercised in the board layout in order to isolate all digital signals from analog signals. The layout shown in *Figure 22* is a good example of what is required in this regard. In particular the Amp. In pins (pins 6 and 7) and the C_{DIFF} pins (pins 1 and 24) must be isolated from all digital signals. An analog ground plane will greatly aid in this isolation as will separate digital and analog grounds. The V_{CC} (pin 9) should have a 0.1 μf bypass capacitor to analog ground located close to the DP8464B. The component list is provided as an example. These components will need to be optimized for a specific read channel.

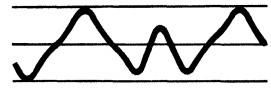

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FIGURE 20. (2,7) Triplet

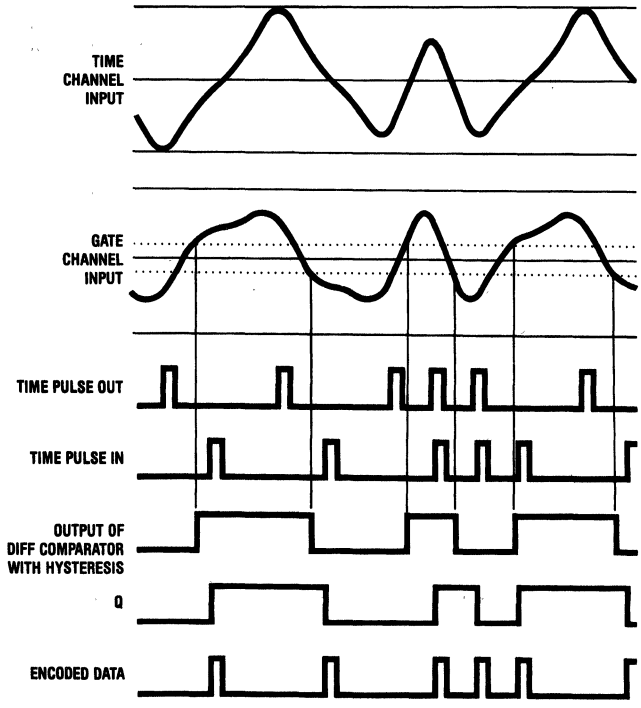

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FIGURE 21. Region 2 Triplet Operation

Application Information (Continued)

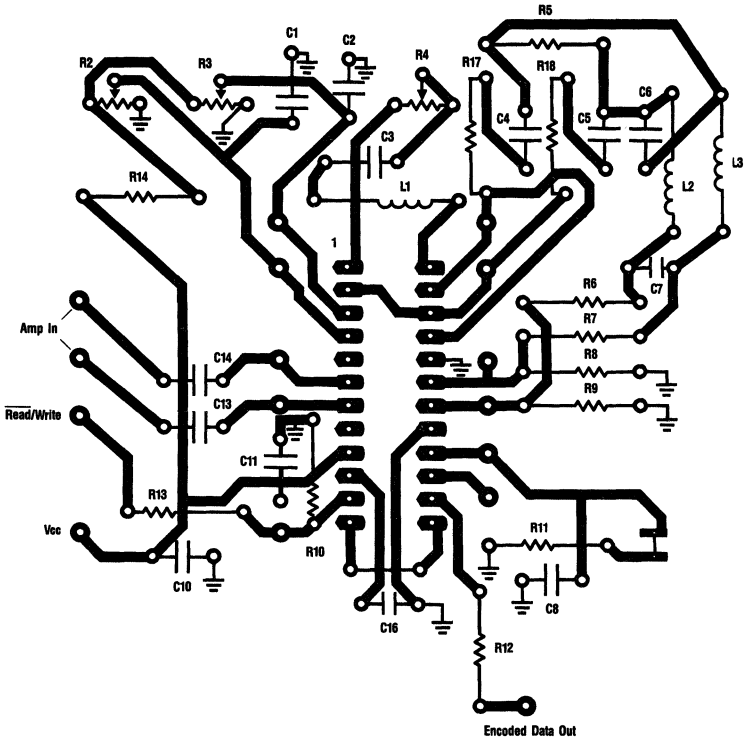

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FIGURE 22. DP8464B Component Layout—Top View

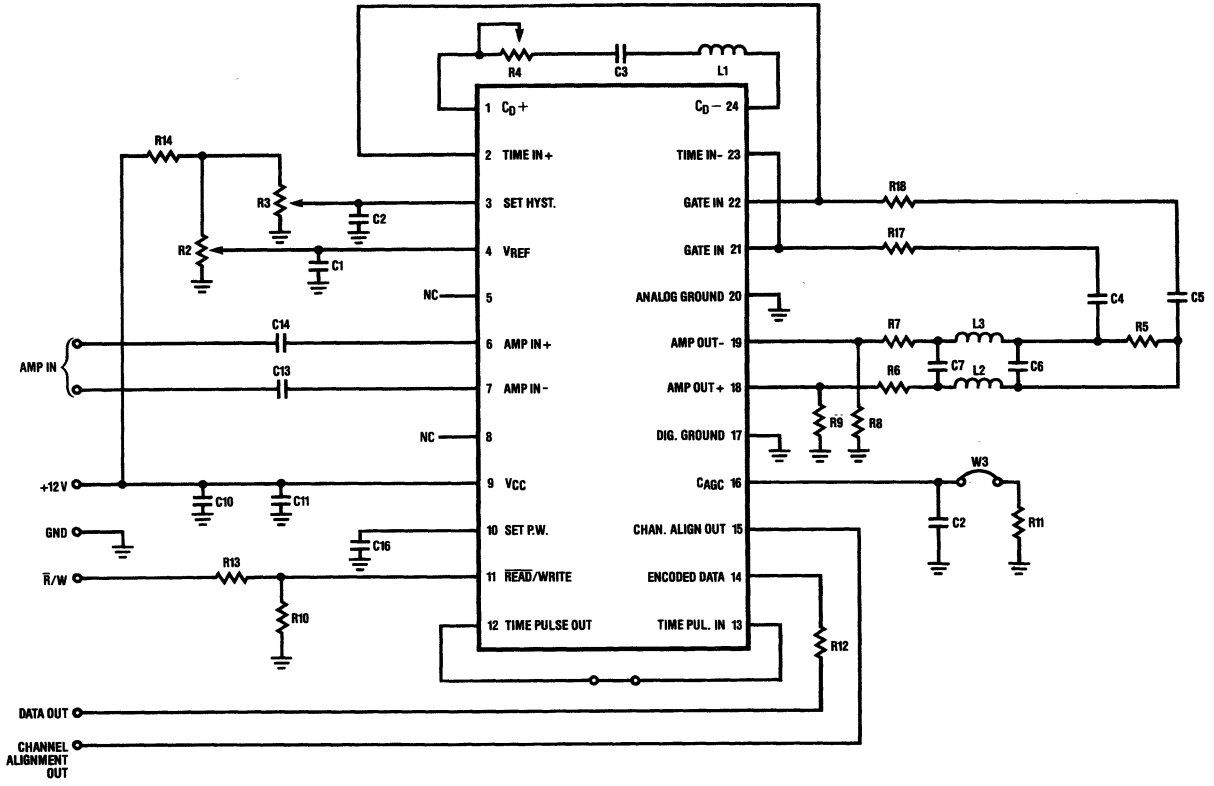

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FIGURE 23. DP8464B Application Board Schematic

Application Information (Continued)

PARTS LIST FOR DP8464B BOARD

Component Name	Note #	Function	Value	Value for 5 Mbits/sec	Value for 10 Mbits/sec
R2	3	Adjustment for V_{REF} (AGC amplitude)	1k pot		
R3	3	Adjustment for Set Hyst. (threshold)	1k pot		
R4	2	Adjustment for differentiator network Q	5k pot		
R5	1	Low pass filter resistor	560Ω		
R6	1	Low pass filter resistor	240Ω		
R7	1	Low pass filter resistor	240Ω		
R8		Amp Out emitter bias resistor	4.3k		
R9		Amp Out emitter bias resistor	4.3k		
R10		Pull down resistor for Read/Write Pin	5.1k		
R11		Resistor in parallel with C_{AGC}	100k		
R12		Encoded Data Out damping resistor	51Ω		
R13		Read/Write damping resistor	51Ω		
R14		Divider network for Set Hyst. and V_{REF}	2.4k		
R17	6	Series resistor for Time Channel Input	Not required on DP8464B		
R18	6	Series resistor for Time Channel Input	Not required on DP8464B		
C1		V_{REF} cap	0.1 μF		
C2		Set Hyst. cap	0.1 μF		
C3	2	Differentiator cap		100 pF	50 pF
C4		Time and Gate Channel In coupling cap	0.01 μF		
C5		Time and Gate Channel In coupling cap	0.01 μF		
C6	1	Low pass filter cap		200 pF	100 pF
C7	1	Low pass filter cap		30 pF	15 pF
C8	4	C_{AGC} cap	0.01 μF		
C10		V_{CC} cap	1.0 μF		
C11		V_{CC} cap	0.1 μF		
C13	5	Amp In coupling cap	2200 pF		
C14	5	Amp In coupling cap	2200 pF		
C16		Set Pulse Width cap		100 pF	50 pF
L1	2	Differentiator inductor		3.6 μH	1.6 μH
L2	1	Low pass filter inductor		10 μH	4.7 μH
L3	1	Low pass filter inductor		10 μH	4.7 μH

BREADBOARD OPERATION NOTES

1. The low pass filter is a 3 pole Bessel with the corner frequency at 3.75 MHz for the 5Mbits/sec board (7.5 MHz for the 10 Mbits/sec board).
2. The differentiator is a simple RLC filter with the break frequency at 8.5 MHz for the 5 Mbits/sec board (17 MHz for the 10 Mbits/sec board). The resistor can be adjusted to correct for phase distortion in the channel.
3. The V_{REF} should be set at 0.5V. Since the low pass filter has a 6 dB loss, the signal on AMP OUT is 4 Vpp differential while the amplitude into the gate channel is 2 Vpp differential. The Set Hyst. should be nominally set at 0.3V.
4. The AGC attack time (the response to an increased input amplitude) is about 2 μs. To increase this time, increase the value of C8 (the AGC capacitor). The AGC decay time (the response to a decrease in amplitude) is about 10 ms. To increase this time, increase the value of R11. Care must be taken to not allow the response of the AGC loop to become too fast, otherwise loop instability may occur.
5. The input pole is set at 72 kHz (1k input impedance and a 2200 pF input coupling capacitor).
6. Pulse pairing (described in the differentiator section of this data sheet) can be caused by unequal delays through the Bi-directional one shots. To minimize this effect, pin 2 should be connected to pin 22, and pin 23 should be connected to pin 21. If connected this way, the delays tend to cancel.

REFERENCES

1. I. H. Graham, "Data Detection Methods vs. Head Resolution in Digital Recording," IEEE Transactions on Magnetics Vol. MAG-14, No. 4 (July 1978)
2. I. H. Graham, "Digital Magnetic Recording Circuits," to be published.
3. Anatol I., Zverev, Handbook of Filter Synthesis, John Wiley & Sons publisher, 1967.

Connection Diagrams (Continued)

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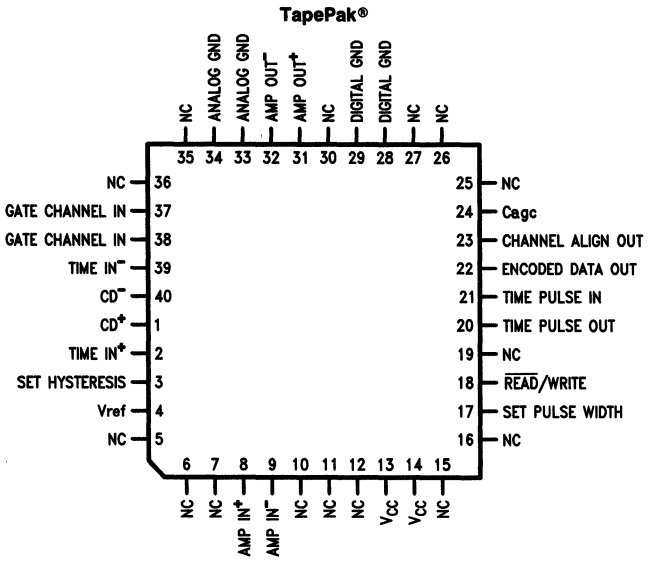

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Top View
Order Number DP8464BTP-3 or DP8464BTP-2
See NS Package Number TP40A

National Semiconductor

PRELIMINARY

DP8468B
Disk Pulse Detector + Embedded Servo Detector

General Description

The DP8468B Disk Pulse Detector + Servo utilizes analog and digital circuitry to detect amplitude peaks of the signal received from the read/write amplifier fitted with the heads of disk drives. The DP8468B produces a TTL compatible output which, on the positive leading edge, indicates a signal peak. Electrically, these peaks correspond to flux reversals on the magnetic medium. The signal from the read/write amplifier when reading a disk is therefore a series of pulses with alternating polarity. The Disk Pulse Detector accurately replicates the time position of these peaks.

The DP8468B also incorporates two gated detectors which detect embedded servo information, used for head positioning. It is primarily intended for detecting a burst type servo pattern as shown in *Figure 16*. However, with external sync detection circuitry it will detect a tri-bit type servo pattern also shown in *Figure 16*. The DP8468B provides two buffered low impedance voltage outputs which represent the peak detected level of each servo burst. These voltages are suitable for digitizing by an analog to digital converter, as would typically be done in a system that utilizes stepper motors for head positioning. The DP8468B also provides a low impedance output that represents the difference voltage, centered about an external reference voltage, between the two servo channels. This voltage is useful in servo systems using a linear voice coil for head positioning.

The Disk Pulse Detector + Servo is fabricated using an advanced oxide isolated Schottky process, and has been designed to function with data rates up to 15 Megabits/second. The DP8468B is available in a surface mount 28-pin plastic chip carrier package. Normally, it will be fitted in the disk drive, and its output may be directly connected to any of National's Data Separators or Synchronizers.

Features

- Wide input signal amplitude range—from 20 mVpp to 660 mVpp differential
- Data rates up to 15 Megabits/sec ½(2,7) code
- On-chip differential gain controlled amplifier, differentiator, comparator gating circuitry, and output pulse generator
- Input capacitively coupled directly from the disk head read/write amplifier
- Adjustable comparator hysteresis
- Dynamic hysteresis tracks signal amplitude
- AGC and differentiator time constants set by external components
- TTL compatible digital Inputs and Outputs
- Encoded Data Output may connect directly to any of National's Data Separators or Synchronizers
- Standard drive supply: 12V ±10%, 5V ±5%
- Built in embedded servo detector
- On chip buffers provide low impedance servo output voltages
- User adjustable servo time constants
- Differentiator and time pulse outputs available as pins on special engineering parts
- Available in a surface mount 28-pin plastic chip carrier package or 40-pin TapePak® package

Block Diagram

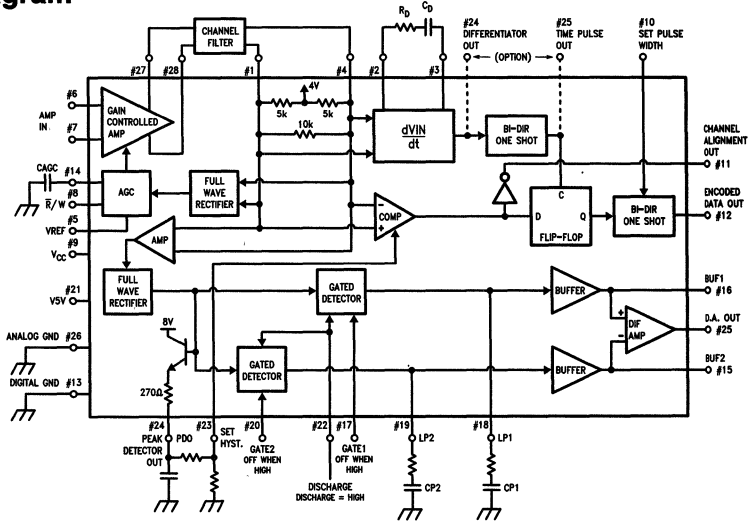

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FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Pins	Limit
Supply Voltage	9	14V
TTL Input Voltage	8, 17, 20, 22	5.5V
TTL Output Voltage	12, 11	5.5V
Input Voltage	23, 5	5.5V
Minimum Input Voltage	23, 5	−0.5V
Differential Input Voltage	6–7, 4–1,	3V or −3V

ESD susceptibility rating is to be determined.

	Limit
Storage Temperature	−65°C to 150°C
Lead Temp. (Soldering, 10 seconds)	300°C
Maximum Power Dissipation at 25°C Plastic Chip Carrier Package (derate 12.5 mW/°C above 25°C)	1560 mW

Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, (V_{CC})	10.8	12.0	13.2	V
Logic Supply, (V5V)	4.75	5	5.25	V
Ambient Temperature, (T_A)	0		70	°C

DC Electrical Characteristics

Over Recommended Operating Temperature and Supply Range V_{REF} = 0.5V, Set Hysteresis = 0.3V. $\overline{Read}$/Write = 0.3V, $V_{PIN\ 17}$ = $V_{PIN\ 20}$ = 2V, $V_{PIN\ 22}$ = 0.3V, unless otherwise noted.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
AMPLIFIER							
$Z_{IN_{AI}}$	6, 7	Amp In Impedance	T_A = 25°C (Note 1)	1.4	2.0	2.6	kΩ
A_{VMIN}	28, 27	Min Voltage Gain	AC Output 4 Vpp Differential			7.0	V/V
A_{VMAX}	28, 27	Max Voltage Gain	AC Output 4 Vpp Differential	200			V/V
$V_{C_{AGC}}$	14	Voltage on C_{AGC}	A_V = 7.0 A_V = 200	• 2.8	4.5 3.7	5.5	V V
CHANNEL							
$Z_{IN_{CI}}$	4, 1	Channel Input Impedance	T_A = 25°C (Note 1)		2.5		kΩ
$I_{C_{AGC}-}$	14	Pin 14 Current which Charges C_{AGC}	$V_{PIN\ 14}$ = 3.9V $\lvert V_{PIN\ 4} - V_{PIN\ 1}\rvert$ = 1.3V	−2.5	−4.2	−6	mA
$I_{C_{AGC}+}$	14	Pin 14 Current which Discharges C_{AGC}	$V_{PIN\ 14}$ = 5V $\lvert V_{PIN\ 4} - V_{PIN\ 1}\rvert$ = 0.7V		0.1	1	μA
$I_{V_{REF}}$	5	V_{REF} Input Bias Current			−20	−100	μA
$V_{TH_{AGC}}$	4, 1 5, 14	AGC Threshold	(Note 2), $V_{PIN\ 14}$ = 4.2V	0.915	1.04	1.165	V
I_{SH}	23	Set Hysteresis Input Bias Current			−40	−70	μA
$V_{TH_{SH}}$	4, 1 23, 11	Set Hysteresis Threshold	(Note 3)	0.48	0.6	0.72	V
I_{C_d}	2, 3	Current into Pin 2 and 3 that Discharges C_d		1.4	1.8		mA
WRITE MODE							
$Z_{IN_{AI}}$	6, 7	Amp In Impedance in Write Mode	$V_{PIN\ 8}$ = 2.0V		100	200	Ω
$I_{C_{AGC}-}$	14	Pin 14 Current in Write Mode	$V_{PIN\ 8}$ = 2.0V $V_{PIN\ 14}$ = 3.9V $\lvert V_{PIN\ 4} - V_{PIN\ 1}\rvert$ = 2.6V		0.1	1.0	μA

DC Electrical Characteristics Over Recommended Operating Temperature and Supply Range V_{REF} = 0.5V, Set Hysteresis = 0.3V. $\overline{Read}$/Write = 0.3V, $V_{PIN\ 17}$ = $V_{PIN\ 22}$ = 0.3V, unless otherwise noted. (Continued)

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL PINS							
V_{IH}	8, 17, 20, 22	High Level Input Voltage		2			V
V_{IL}	8, 17, 20, 22	Low Level Input Voltage				0.8	V
V_I	8, 17, 20, 22	Input Clamp Voltage	V_{5V} = Min, I_I = −18 mA			−1.5	V
I_{IH}	8, 17, 20, 22	High Level Input Current	V_{5V} = Max, V_I = 2.7V			20	μA
I_I	8, 17, 20, 22	Input Current at Maximum Input Voltage	V_{5V} = Max, V_I = 5.5V			1	mA
I_{IL}	8, 17, 20, 22	Low Level Input Current	V_{5V} = Max, V_I = 0.5V			−200	μA
V_{OH}	12	High Level Output Voltage	V_{5V} = Min, I_{OH} = −40 μA (Note 4)	2.7			V
V_{OL}	12	Low Level Output Voltage	V_{5V} = Min, I_{OL} = 800 μA (Note 4)			0.5	V
I_{LH}	11	High Level Output Leakage Current	$V_{Pin\ 11}$ = 5.5V Measure Current into Pin 11			10	μA
V_{OL}	11	Low Level Output Voltage	$I_{PIN\ 11}$ = 5 mA			0.5	V
I_{OS}	12	Output Short Circuit Current	V_{5V} = Max, V_O = 0V			−100	mA
SERVO CHANNEL							
Z_{DIS}	18, 19	Discharge Impedence	$V_{PIN\ 22}$ = 2V Force 3V on Pins 18 or 19.	1.0	1.5	2.3	kΩ
V_{BOQ}	15, 16	Buffer Quiescent Output Level	$V_{PIN\ 17, 20, 22}$ = 0.3V V_{CI} = 0V, $V_{PIN\ 21}$ = 5V Pull 0 mA from Pins 15 and 16.	1.1	1.2	1.3	V
Av_Q	15, 16	Quiescent Output Level Gain to Pin 21	$V_{PIN\ 17, 20, 22}$ = 0.3V V_{CI} = 0V, $V_{PIN\ 21}$ = 4.5V Pull 0 mA from Pin 15 and 16. $Av_Q = \frac{V_{BOQ} - V_{PIN\ 15\ or\ 16}}{5V - 4.5V}$		0.226		V/V
V_{PDOQ}	24	Peak Detector Quiescent Output Level	$V_{PIN\ 21}$ = 5V, V_{CI} = 0V, Pull 200 μA from Pin 24	0.14	0.36	0.64	V
I_L	18, 19	Gated Off Leakage Current	$V_{PIN\ 22}$ = 0.3V $V_{PIN\ 20}$ = $V_{PIN\ 17}$ = 2V Force 6.6V on Pin 18 or Pin 19	−1	0.2	1	μA
$V_{OS_{BO}}$	16, 15	Buffer Output Offset Voltage For V_{CI} = $1V_{pk\text{-}pk}$	$V_{PIN\ 17, 20, 22}$ = 0.3V $V_{PIN\ 1}$ = 4.25V $V_{PIN\ 4}$ = 3.75V Pull 0 mA from Pin 15 and 16. $V_{OS_{BO}}$ = $V_{PIN\ 16}$ − $V_{PIN\ 15}$		±1	±15	mV
$V_{OS_{SYS}}$	25, 21	System Output Offset Voltage For V_{CI} = $1V_{pk\text{-}pk}$	$V_{PIN\ 17, 20, 22}$ = 0.3V, $V_{PIN\ 21}$ = 5V V_{PIN1} = 4.25V, V_{PIN4} = 3.75V Pull 0 mA from Pin 25 $V_{OS_{SYS}}$ = $V_{PIN\ 25}$ − $V_{PIN\ 21}$		±5	±20	mV
$Av_{DA}\|_{2V}$	25, 21	Difference Amplifier Gain, 2V Differential Input	$V_{PIN\ 17, 20}$ = 2V, $V_{PIN\ 21}$ = 5V $V_{PIN\ 22}$ = 0.3V $V_{PIN\ 19}$ = 5.4V, $V_{PIN\ 18}$ = 3.4V $Av_{DA} = \frac{V_{PIN\ 21} - V_{PIN\ 25}}{V_{PIN\ 19} - V_{PIN\ 18}}$	0.42	0.49	0.57	V/V
$Av_{DA}\|_{1V}$	25, 21	Difference Amplifier Gain, 1V Differential Input	$V_{PIN\ 17, 20}$ = 4V, $V_{PIN\ 21}$ = 5V $V_{PIN\ 22}$ = 0.3V $V_{PIN\ 19}$ = 4.9V, $V_{PIN\ 18}$ = 3.9V $Av_{DA} = \frac{V_{PIN\ 21} - V_{PIN\ 25}}{V_{PIN\ 19} - V_{PIN\ 18}}$	0.43	0.5	0.57	V/V

DC Electrical Characteristics Over Recommended Operating Temperature and Supply Range V_{REF} = 0.5V, Set Hysteresis = 0.3V. $\overline{Read}$/Write = 0.3V, $V_{PIN\ 17}$ = $V_{PIN\ 22}$ = 0.3V, unless otherwise noted. (Continued)

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
SERVO CHANNEL (Continued)							
GL_{DA}	25	Difference Amplifier Gain Linearity	$GL_{DA} = \left\| \frac{Av_{da}\|_{2V}}{Av_{da}\|_{1V}} - 1 \right\| \times 100$ $V_{PIN\ 21}$ = 5V		0.5	2.5	%
Z_{PDO} Source	24	Peak Detector Out Output Impedence	$V_{PIN\ 17, 20, 22}$ = 0.3V, V_{CI} = 1V Measure $V_{PIN\ 24}$ with 200 µA and 3 mA Pulled out of the Pin. $Z_{PDO\ Source} = \frac{\lvert change\ in\ V_{PIN\ 24} \rvert}{3\ mA - 0.2\ mA}$	150	200	250	Ω
$Av_{gd}\|_{2V}$	15, 16	Gated Detector Gain For V_{CI} = $2V_{pk\text{-}pk}$	$V_{PIN\ 22, 20, 17}$ = 0.3V V_{PIN1} = 4.5V, V_{PIN4} = 3.5V $Av_{gd} = \frac{V_{PIN\ 15\ or\ 16} - V_{BOQ}}{V_{CI}}$	1.45	1.8	2.25	V/V
$Av_{gd}\|_{1V}$	15, 16	Gated Detector Gain For V_{CI} = $1V_{pk\text{-}pk}$	$V_{PIN\ 22, 20, 17}$ = 0.3V V_{PIN1} = 4.25V, V_{PIN4} = 3.75V $Av_{gd} = \frac{V_{PIN\ 15\ or\ 16} - V_{BOQ}}{V_{CI}}$	1.6	2	2.4	V/V
$AV_{PDO}\|_{2V}$	24	Peak Detector Output Voltage Gain For V_{CI} = $2V_{pk\text{-}pk}$	V_{PIN1} = 4.5V, V_{PIN4} = 3.5V $Av_{PDO} = \frac{V_{PIN\ 24\ pk\text{-}pk}}{V_{CI}}$	1.45	1.9	2.25	V/V
$AV_{PDO}\|_{1V}$	24	Peak Detector Output Voltage Gain For V_{CI} = $1V_{pk\text{-}pk}$	V_{PIN1} = 4.25V, V_{PIN4} = 3.75V $Av_{PDO} = \frac{V_{PIN\ 24AC}}{V_{CI}}$	1.6	2.0	2.4	V/V
GL_{gd}	15, 16	Gated Detector Gain Linearity	$GI_{gd} = \frac{\frac{\lvert V_{PIN\ 16} - V_{PIN\ 15} \rvert_{eighth}}{\lvert V_{PIN\ 16} - V_{PIN\ 15} \rvert_{quarter}} - 0.5}{0.5} \times 100$ $\lvert V_{PIN\ 16} - V_{PIN\ 15} \rvert_{eighth}$ = (Note 5) $\lvert V_{PIN\ 16} - V_{PIN\ 15} \rvert_{quarter}$ = (Note 6)		±0.5	±2.5	%
I_{CC}	9	V_{CC} Supply Current	V_{CC} = Max	25	46	65	mA
I_{5V}	21	5V Supply Current	V_{5V} = Max	3	7	11	mA

AC Electrical Characteristics Over Recommended Operating Temperature and Supply Range Refer to AC Test Setup. f = 2.5 MHz unless otherwise indicated.

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
t_{charge}	15, 16	Gated Detector Charge Time	V_{CI} = 2V pk-pk, $V_{PIN\ 22}$ = 0.3V, S1 & S2 = Closed. With LP1 and LP2 discharged, measure the time from Pin 17 or 20 going from 2V to 0.3V, to V_{bo_1} or V_{bo_2} respectively, reaching 90% of their final value.		11		µs
$t_{discharge}$	15, 16	Gated Detector Discharge Time	V_{CI} = 2V, pk–pk,S1 & S2 = Closed. With LP1 charged, measure the time from Pin 22 going from 0.3V to 2V, to the voltage at V_{bo_1} or V_{bo_2} reaching 90% of their final value.		56		µs
t_{ON}	18, 19	Gated Detector Turn On Time	V_{CI} = 1V DC, $V_{PIN\ 22}$ = 0.3V, S1 & S2 = Open. With LP1 discharged, measure the time from Pin 17 going from 2V to 0.3V, to the voltage on Pin 18 increasing 0.1V Do a similar measurement with LP2, Pin 20 and Pin 19.		8		ns

AC Electrical Characteristics Over Recommended Operating Temperature and Supply Range Refer to AC Test Setup. f = 2.5 MHz unless otherwise indicated. (Continued)

Symbol	Pins	Parameter	Conditions	Min	Typ	Max	Units
t_{OFF}	18, 19	Gated Detector Turn Off Time	V_{CI} = 1V DC, $V_{PIN\ 22}$ = 2V, S1 & S2 = Open. Measure the time from Pin 17 going from 0.3V to 2V, to the voltage on Pin 18 decreasing by 0.1V. Do a similar measurement with Pins 20 and 19.		10		ns
DP8468B-2 t_{PP}	12	Pulse Pairing (Note 7)	f = 2.5 MHz and f = 3.33 MHz V_{AI} = 60 mVpp differential.			±3	ns
DP8468B-3 t_{PP}	12	Pulse Pairing (Note 7)	f = 2.5 MHz and f = 3.33 MHz V_{AI} = 60 mVpp differential.			±5	ns

Note 1: The temperature coefficient of the input impedance is typically 0.05% per degree C.

Note 2: The AGC Threshold is defined as the voltage across the Channel Input (pins 4 and 1) when the voltage on C_{AGC} (pin 14) is 4.2V.

Note 3: The Set Hysteresis Threshold is defined as the minimum differential AC signal across the Channel Input (pins 4 and 1) which causes the voltage on the Channel Alignment Output (pin 11) to change state.

Note 4: To prevent inductive coupling from the digital outputs to Amp In, the TTL outputs should not drive more than one ALS TTL load each. Pin 11 is an open collector output which is tested with an external 1k pullup resistor to the 5V supply.

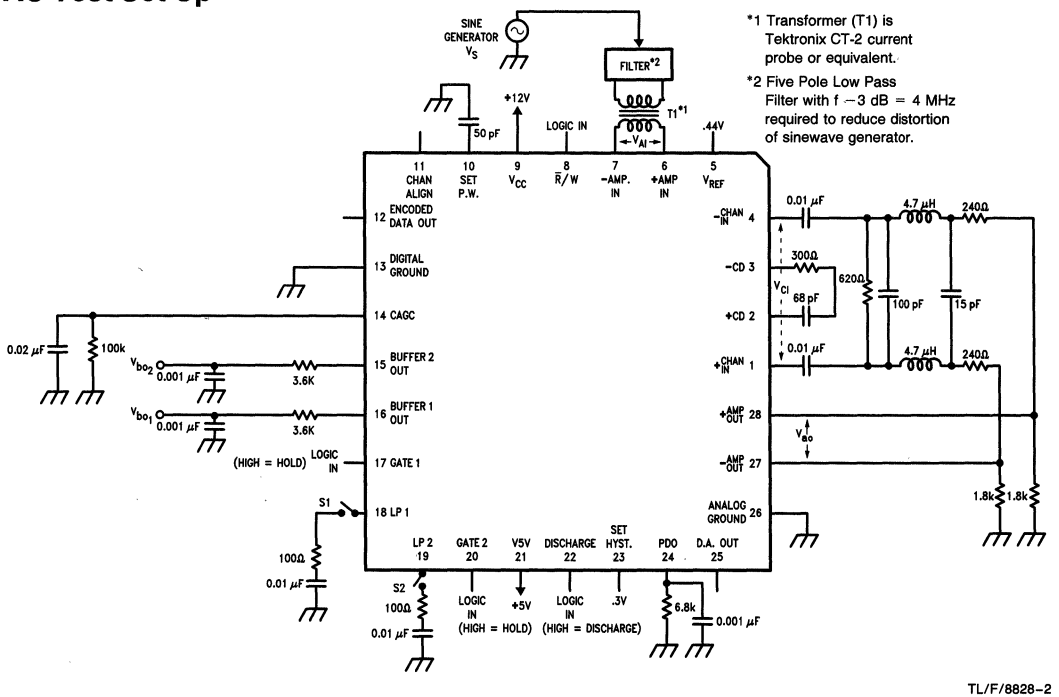
Note 5: $|V_{PIN\ 16} - V_{PIN\ 15}|_{eighth}$ = The difference in the buffer output voltages with the channel input level set to simulate the read head mispositioned by one eighth of a track, This is done by setting V_{CI} = 1.25V and measuring $V_{PIN\ 15}$ then set V_{CI} = 0.75V and measure $V_{PIN\ 16}$. The absolute value of the difference between Pins 15 and 16 is the quantity of interest. The part is also tested with Pin 16 measured at a V_{CI} = 1.25V and Pin 15 measured with V_{CI} = 0.75V.

$V_{PIN\ 17} = V_{PIN\ 18} = 0.3V$

Note 6: $|V_{PIN\ 16} - V_{PIN\ 15}|_{quarter}$ = The difference in the buffer output voltages with the channel input level set to simulate the read head mispositioned by one quarter of a track, This is done by setting V_{CI} = 1.5V and measuring $V_{PIN\ 15}$ then set V_{CI} = 0.5V and measure $V_{PIN\ 16}$. The absolute value of the difference between Pins 15 and 16 is the quantity of interest. The part is also tested with Pin 16 measured at a V_{CI} = 1.5V and Pin 15 measured with V_{CI} = 0.5V.
$V_{PIN\ 17} = V_{PIN\ 18} = 0.3V$

Note 7: For this Preliminary specification only, pulse pairing is measured and guaranteed at 25°C and 2.5 MHz.

AC Test Set Up



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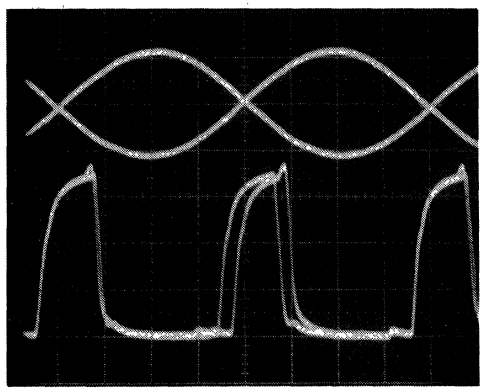
AC Test Set Up (Continued)

The channel filter is a 3 pole Bessel with the corner frequency at 7.5 MHz which is similar to filters used in 10 Mbits/sec 2,7 drives.



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Pulse Pairing Measurement

Connect a scope probe to pin 12 (Encoded Data Out) and trigger off its positive edge. Adjust the trigger holdoff so the scope first triggers off the pulse associated with the positive peak and then off the pulse associated with the negative peak (as shown in the scope photo below). Pulse pairing is displayed on the second pair of pulses on the display. If the second pulses are separated by 2 ns, then the pulse pairing for this part is ±1 ns.

Chip Operation

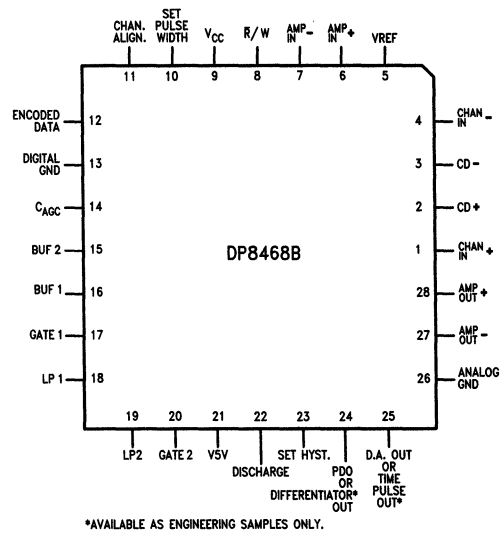
The output from the read/write amplifier is AC coupled to the Amp Input of the DP8468B. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the Gate Channel Input four times the DC voltage on V_{REF}. Typically the signal on Amp Out will be set for 4 Vpp differential. Since the filter usually has a 6 dB loss, the signal on the Gate Channel Input will be 2 Vpp differential. The user should therefore set 0.5V on V_{REF} which can be done with a simple voltage divider from the +12V supply.

The peak detection is performed by feeding the output of the Amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering (the tendency to return to the baseline), the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised of a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level which will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bi-directional one shot. This pulse will clock the new data at the D input through to the output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flop is not changing since the logic level into the D input has not changed. The comparator circuitry is therefore a gating channel which prevents any noise near the baseline from contaminating the data. The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential AC signal across the Gate Channel Input must be larger than 0.6V before the output of the comparator will change states. In this case, the hysteresis is 30% of a 2V peak to peak differential signal at the gate channel input.

The signal at the Channel Input pins #1 and #4 is amplified and fed to a full wave rectifier. This full wave rectified signal is then presented to the inputs of two separately gated detectors which, when gated on, will generate a DC voltage level proportionate to the peak level of the full wave rectified signal. When recovering embedded servo information each channel is independently gated, thereby detecting a signal whose amplitude represents the relative positioning of the read head. The difference of the DC voltages from the gated detectors is the head positioning information. The DC voltages appear across external RC networks connected to pins 18 and 19. The output buffers level shift these DC voltages which then appear at the low impedance output pins 15 and 16. The voltages at these pins are differenced and appear at the low impedance output pin 25 centered about the external reference voltage applied to pin 21.

Connection Diagram

Plastic Chip Carrier (PCC) Package



*AVAILABLE AS ENGINEERING SAMPLES ONLY.

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Plastic Chip Carrier (V)
Order Number DP8468BV-3 or DP8468BV-2
See NS Package Number V28A

Pin Definitions

Pin #	Name	Function
POWER SUPPLY		
9	V_{CC}	The supply is +12V ±10%.
21	V5V	Supplies internal chip logic and provides a reference voltage for the zero level of the difference amplifier output on pin 25. Supply tolerance is 5V ±5%.

Pin Definitions (Continued)

Pin #	Name	Function
POWER SUPPLY (Continued)		
26	Analog Ground	Analog signals should be referenced to this pin.
13	Digital Ground	Digital signals should be referenced to this pin.
ANALOG SIGNALS		
6 7	Amp. in+ Amp. in−	These are the differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
28 27	Amp. out+ Amp. out−	These are the differential outputs of the Amplifier. These outputs should be capacitively coupled to the channel filter.
4 1	Channel Inputs	These are the differential inputs to the time, gating and servo channels. These inputs must be capacitively coupled to the channel filter at the amp. outputs.
2 3	C_d+ C_d−	The external differentiator network is connected between these two pins.
23	Set Hysteresis	The DC voltage on this pin sets the amount of hysteresis on the differential comparator.
24	PDO	This is a Peak Detector Output signal that is used in conjunction with the set hysteresis pin 23 to provide a dynamic hysteresis function.
5	V_{REF}	The AGC circuit adjusts the gain of the gain controlled amplifier to make the differential peak to peak voltage at the Channel Inputs equal to four times the DC voltage on this pin.
14	C_{AGC}	The external capacitor for the AGC is connected between this pin and Analog Ground.
18 19	LP1 LP2	The peak detected servo signal voltage appears across the RC networks connected from these pins to analog ground.
16 15	Buffer Out 1 Buffer Out 2	These low impedance pins, output the DC level at pins 18 and 19 respectively, level shifted down by two diode drops.
25	D.A. Out	This low impedance pin outputs the difference in voltage between pins 16 and 15 about a zero level set by the voltage on pin 21.
DIGITAL SIGNALS		
10	Set Pulse Width	An external capacitor to control the pulse width of the Encoded Data Out is connected between this pin and Digital Ground.
8	$\overline{\text{READ}}$/ WRITE	If this pin is low, the Pulse Detector is in the read mode and the chip is active. When this pin goes high, the pulse detector is forced into a stand-by mode. This is a standard TTL input.

Pin #	Name	Function
DIGITAL SIGNALS (Continued)		
11	Channel Alignment Output	This is the buffered, open collector, output of the differential comparator with hysteresis.
12	Encoded Data Out	This is the standard TTL output whose leading edge indicates the time position of the peaks.
17 20	Gate 1 Gate 2	These inputs accept TTL levels. When a low level is present the embedded servo signal is allowed to charge the RC network at pins 18 and 19 respectively. A high level will force a hold condition of the DC voltage across the RC network and will also disable the servo channel.
22	Discharge	This input accepts a TTL level. A high level connects a 1.5k internal resistor to ground on pins 18 and 19.

SPECIAL ENGINEERING PIN OUT AVAILABLE

On an engineering basis only, the Differentiator Output and the output of the time channel bi-directional one shot (referred to from now on as 'Time Pulse Output') will be brought out as pins. The Differentiator and Time Pulse Output pins will not be available on production parts. They are only available by special request on an engineering basis.

In order to bring out these pins it is necessary to eliminate two other pins. The pin trade off and operation details are as follows:

1. The Differentiator Output replaces the Peak Detector Output (PDO), pin 24. The Differentiator Output is buffered by an emitter follower which has a 3k resistor in series with the emitter connected to the output pin. This is shown in *Figure 12*. An external resistor to ground must be connected to this pin in order to bias the output emitter follower. The combination of the 3 kΩ output resistor and the external resistor pull down, form a voltage divider that attenuates the level of the differentiator output signal. Please note that the differentiator signal will only be linear near the differentiator output zero crossing because the signal peaks at the differentiator output are clamped by the Schottky diodes across the collectors of Q2 and Q3 as shown in *Figure 12*.
2. The Time Pulse Output replaces the Difference Amplifier Output (D.A. Out), pin 25. This pin is a standard TTL output capable of driving one ALS load.

DIFFERENCES BETWEEN THE DP8468B AND THE DP8464B

The DP8468B is a DP8464B type pulse detector in combination with two gated detectors which are used to detect embedded servo information in a Winchester disk drive. In order to fit into a 28-pin PCC package and provide the additional embedded servo detection functions, some of the pins on the DP8464B were eliminated. Other changes were made to reduce power dissipation. A summary of the differences between the two parts is given here for the benefit of those who are familiar with the DP8464B.

1. The Time Channel Inputs are now internally connected to the Gate Channel Inputs.

Pin Definitions (Continued)

2. The Time Pulse Out pin is now internally connected to the Time Pulse In pin, and not normally brought out as an output.
3. The Channel Alignment Output is now open collector and requires an external pull up resistor for use.
4. The internal logic is powered from an external 5V supply connected to pin 21.
5. The output impedance that drives C_{AGC}, pin 14, has been reduced from 700Ω to 350Ω. This allows you to double the external capacitance on this pin and still achieve the same attack time as with the DP8464B. The large capacitor allows for longer AGC hold times, which is useful during the embedded servo sectors.
6. The internal leakage current from pin 14 to ground has been reduced by a factor of 5.
7. The combined differential input impedance of the Gate Channel and the Time Channel has been increased from 1.67 kΩ to 2.5 kΩ.
8. The internal current sources on the Amp. Output pins have been eliminated. The current in the output emitter followers is now entirely set by the external pull down resistors on pins 27 and 28.
9. In addition to the embedded servo circuitry, a Dynamic Hysteresis function has been added. The hysteresis level can be set as before or the set hysteresis pin can be connected through an external RC network to the PDO output, pin 24, to implement the Dynamic Hysteresis function.
10. The gain controlled amplifier input impedance in read mode has been increased to 2 kΩ.

Application Information

GENERAL DESCRIPTION OF PULSE DETECTION

The DP8468B Disk Pulse Detector utilizes analog and digital circuitry to detect amplitude peaks of the signal received from the Read/Write Amplifier. The analog signal from a disk is a series of pulses, the peaks of which correspond to 1's or flux reversals on the magnetic media. The pulse detector must accurately determine the time position of these peaks. The peaks are indicated by the positive leading edge of a TTL compatible output pulse. This task is complicated by variable pulse amplitudes depending on the media type, head position, head type and read/write amplifier circuit gain. Additionally, as the bit density on the disk increases, the amplitude decreases and significant bit interaction occurs resulting in pulse distortion and shifting of the peaks.

The graph in *Figure 2* shows how the pulse amplitude varies with the number of flux reversals per inch (or recording density) for a given head disk system. The predominant disk applications are associated with the first two regions on this graph, Regions 1 and 2. Typical waveforms received by the pulse detector for these regions are shown next to the graph.

Region 1 is the high resolution area characterized by a large spread between flux reversals and a definite return to baseline (no signal) between these peaks. Pulses of this type are predominantly found in drives which use either thin film heads or plated media, or in drives which utilize run length limited codes (like the 2,7 code) which spread the distance between flux reversals.

A Region 2 waveform will vary from a tendency to return to the baseline (called shouldering) to almost sinusoidal at the higher frequencies. These pulses come from drives which use limited frequency codes (such as MFM). The pulses may contain shouldering on the outer tracks of the disk and be nearly sinusoidal on the inner tracks since the flux density increases towards the inner track.

Detecting pulse peaks of waveforms of such variable characteristics requires a means of separating both noise and shouldering-caused errors from the true peaks. In the past, mild shoulder-caused errors were blocked by self-gating circuits (such as the "de-snaker"). These circuits fail when shouldering is extensive, hence the need for the DP8468B which includes a peak sensing circuit and an amplitude sensitive gating channel in parallel.

The main circuit blocks of the DP8468B are shown in *Figure 1*. The output from the read/write amplifier is fed directly to the Amp Input of the DP8468B. This is the input of a Gain Controlled Amplifier. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak-to-peak differential Channel input voltage four times the DC voltage on V_{REF}.

The peak detection is performed by feeding the output of the Gain Controlled Amplifier through an external filter to

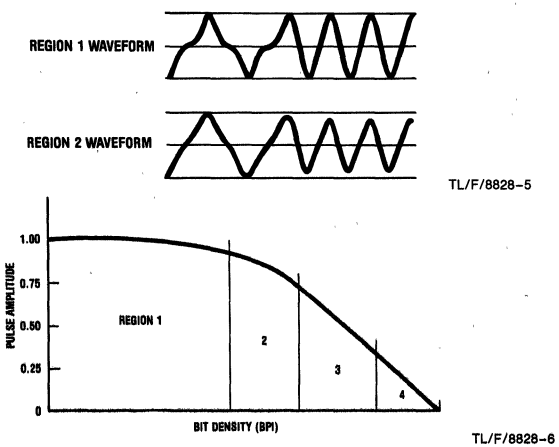

FIGURE 2. Pulse Amplitude vs. Bit Density with Typical Waveforms

Application Information (Continued)

the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering (the tendency to return to the baseline) as seen in Region 1 and the upper part of Region 2, the differentiator will also respond to noise near the baseline. To avoid this, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel comprises a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have valid data out, the input amplitude must first cross the hysteresis level. This will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bi-directional one shot. This pulse will clock in the new data on the D input, which will appear at the Q output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flop is not changing since the logic level into the D input has not yet changed. The comparator circuitry is therefore a gating channel to prevent any noise near the baseline from contaminating the data.

The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential Channel Input must be larger than 0.6V (±0.3V) before the output of the comparator will change states. The Encoded Data Output is designed to drive 1 standard TTL gate. The Channel Alignment output is an open collector which requires a pull up resistor, if you want to monitor this point, otherwise this pin can be left floating.

GAIN CONTROLLED AMPLIFIER

The purpose of the Gain Controlled Amplifier is to increase the differential input signal to a fixed amplitude while maintaining the exact shape of the input waveform. The Gain Controlled Amplifier is designed to accept input signals from 20 mVpp to 660 mVpp differential and amplify that signal to 4 Vpp differential. The gain is therefore from 6 to 200 and is controlled by the automatic gain control (AGC) loop. The amplifier output is actually capable of delivering typically 5 Vpp differential output but the parts are only tested and guaranteed to 4 Vpp.

The input to the Gain Controlled Amplifier is shown in *Figure 3*. The value of the input capacitors should be selected so that the pole formed by the coupling capacitor and the 2k bias resistor is a factor of 10 lower than the lowest signal frequency. These input bias resistors have a ±20% tolerance and a temperature coefficient of 0.05% per degree C. When the pulse detector is in the write mode, these bias resistors are automatically shunted by 70Ω resistors. This allows the input circuit to recover quickly from the large transients encountered during a write to read transition. The input impedance to the amplifier is therefore 2k during read operations and 68Ω during write operations.

The output of the Gain Controlled Amplifier is shown in *Figure 4*. The outputs are biased at (12V − (0.75 mA × 2.4k) − 0.75V) or 9.5V. Since each output will swing ±1V (4 Vpp differential), each output pin will swing from 8.5V to 10.5V. If the total differential load placed on the output is 1k, (see *Figure 5*) then the circuit must supply 2V/1k or 2 mA. Since the output is class A, external resistors to ground must be

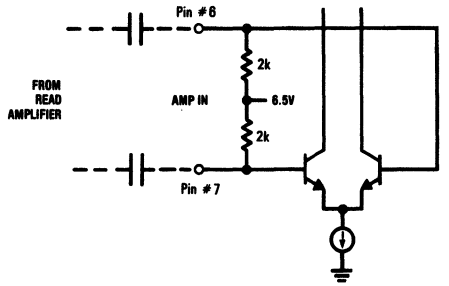

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FIGURE 3. Input to Gain Controlled Amplifier

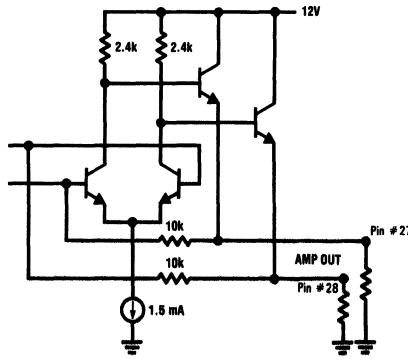

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FIGURE 4. Output of Gain Controlled Amplifier

Application Information (Continued)

used to provide the sink current. In this case, in order to sink 2 mA at the lowest voltage and provide a 2 mA safety margin, then (8.5V/4 mA) or an external 2k resistor from each output to ground is required. The additional 2 mA margin insures that the output emitter followers never turn off. Typically the output impedance of the Gain Controlled Amplifier is 17Ω, and the −3 dB bandwidth is greater than 20 MHz.

AUTOMATIC GAIN CONTROL (AGC)

The Automatic Gain Control holds the signal level at the Channel Input at a constant level by controlling the gain of the Gain Controlled Amplifier. This is necessary because the amplitude of the input signal will vary with track location, variations in the magnetic film, and differences in the actual recording amplitude. The Gain Controlled Amplifier is designed for a maximum 4 Vpp differential output. To prevent the Gain Controlled Amplifier from saturating, the V_{REF} level must be set so the maximum amplifier output voltage is 4 Vpp. The AGC will force the differential peak-to-peak signal on the Channel Input to be four times the voltage applied to the V_{REF} pin. Normally some kind of filter is connected between the Gain Controlled Amplifier's output and the Channel Input. Typically this filter has a 6 dB insertion loss in its pass band. Since the AGC holds the amplitude at the Channel Input constant, this 6 dB loss through the Channel filter will cause the Gain Controlled Amplifier's output to be 6 dB larger than the Channel Input.

The AGC loop starts out in the high gain mode. When the input signal is larger than expected, the AGC loop will quickly reduce the amplifier gain so the peak-to-peak differential voltage on the Channel Input remains four times the voltage on V_{REF}. If the input amplitude suddenly drops, the AGC loop will slowly increase the amplifier gain until the differential peak-to-peak Channel Input voltage again reaches four times V_{REF}. The AGC loop requires several peaks to react to an increased input signal. In order to recover the exact peak timing during this transition, the V_{OUT} level must be set somewhat lower than the maximum of 4 Vpp. For instance, if the V_{REF} is 0.5V, and if the loss in the channel filter is 6 dB, then the Amp Output is 4 Vpp. If the Amp Input suddenly increases 30%, the amplifier may saturate and the timing for a few peaks may be disturbed until the AGC reduces the amplifier gain. If the peak detection is critical during this time, the system may fail. The proper operation, for this example, is to set the V_{REF} at 0.35V so the amplifier will not saturate if the input suddenly increases 30%.

A simplified circuit of the AGC block is shown in *Figure 6*. When the full wave rectified signal from the Channel Input is greater than V_{REF}, the voltage on the collector of transistor T1 will increase and charge up the external capacitor C_{AGC} through T2. The typical available charging current is 2.5 mA. Conversely, if this input is less than V_{REF}, transistor T2 will be off, so the capacitor C_{AGC} will be discharged by the base current going into the Darlington T3 and T4. This discharge

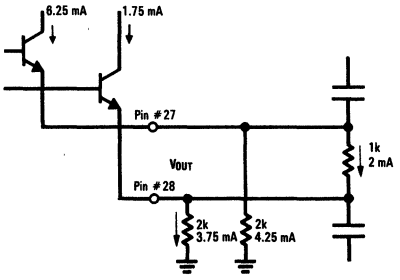

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FIGURE 5. Output Stage with 1k Differential Load

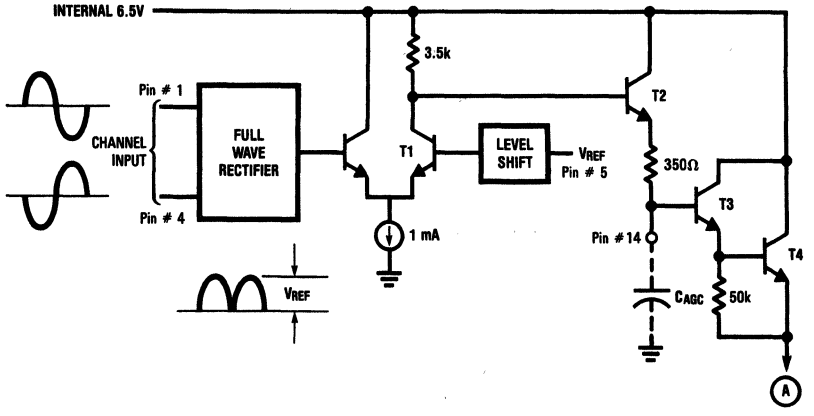

FIGURE 6. Simplified AGC Circuit

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Application Information (Continued)

current is approximately 1 μA. The voltage across C_{AGC} controls the gain of the Gain Controlled Amplifier. This voltage will vary from typically 3.4V at the highest gain to 4.5V at the lowest gain.

When the AGC circuit has not received an input signal for a long time, the base current of the Darlington will discharge the external C_{AGC} to 3.4V. The amplifier will now be at its highest gain. When a large signal comes in, the external C_{AGC} will be charged up with 5 mA from T2 thereby reducing the gain of the amplifier. The formula, $I = C \times (dV/dt)$ can be used to calculate the time required for the amplifier to go from a gain of 200 to a gain of 6. For instance, if C_{AGC} = 0.01 μF, the charging current I is 5 mA, and the dV required for the amplifier to go through its gain range is 1.1V, then

$$dt = (0.01\ \mu F \times 1.1V)/(5\ mA) \text{ or } 2.3\ \mu s.$$

In reality, the gain does not change this quickly since the C_{AGC} would only be charging during a portion of the input waveform.

By using the same argument, the time required to increase the amplifier gain after the input has been suddenly reduced can be calculated. This time, the discharging current is only 1 μA so

$$dt = (0.01\ \mu F \times 1.1V)/1\ \mu A) \text{ or } 11\ ms.$$

This time can be decreased by placing an external resistor across the C_{AGC}. For instance, if a 100k resistor is placed in parallel with C_{AGC}, then the discharge current is 40 μA. The time required to increase the amplifier gain is now 40 times faster or 275 μs. If this external resistor is made even smaller, say 10k, then the discharge time will go to 27.5 μs. Now however, there is another problem introduced. The response time of the AGC is so fast that it distorts the signal at the output of the Gain Controlled Amplifier. Distortion of the signal at the Amplifier Output can affect the time position of the peaks of this signal. Be sure to check this distortion over the range of input levels you expect to encounter, when choosing the external R and C values for the AGC.

If the value of the bleed resistor across the C_{AGC} is decreased (in order to equalize the AGC attack and decay times) the value of C_{AGC} must be increased in order to maintain an AGC response that does not distort the signal. There is a second order effect on the amplitude that results from this attack and decay time equalization. Referring to *Figure 1*, notice that the AGC is driven from a full wave rectified version of the Channel Input signal. When the AGC is operated normally (ie. fast attack and slow decay) the voltage that appears across C_{AGC} is the peak detected value of this full wave rectified waveform. However, if you equalize the AGC attack and decay times the voltage across C_{AGC} is the RMS voltage (0.707 times the peak) of the full wave rectified waveform. Thus, the voltage across C_{AGC} is less and the amplitude out of the Gain Controlled Amplifier will consequently be 1.4 times larger.

It is possible to externally drive the C_{AGC} pin to control the gain of the amplifier. When properly filtered, the peak detector output, Pin 24, can be used in this regard. It must be noted that the gain of the amplifier is not always exactly 200 when the voltage on C_{AGC} is 3.4V. The transfer curve between the gain of the amplifier and the voltage on C_{AGC} is only approximate. This transfer curve will vary between parts and with temperature. Care should be taken to prevent the voltage on the C_{AGC} pin from going below ground or above 5.5V. *Figure 7* shows a typical curve of the Gain Controlled Amplifier Gain vs. the voltage across C_{AGC} (Vpin 14.)

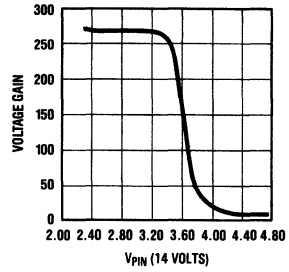

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FIGURE 7. Gain Controlled Amplifier Gain vs. Vpin 14

It is possible to change the time constant of the AGC circuit by switching in different external components at the desired times. For instance, as shown in *Figure 8*, an external open collector TTL gate and resistor can be added in parallel with C_{AGC} to decrease the AGC response time. Similarly, an external capacitor could be switched in to increase the response time. Since in the absence of an external resistor the discharge time of C_{AGC} is much longer than the attack time there may be some applications where it is desirable to switch in a parallel resistor to quickly discharge C_{AGC} then switch it out to force a quick attack. Because of the quick attack time, the AGC obtains the proper level quicker than it would had C_{AGC} simply been allowed to discharge to the new level.

There are some applications where it is desirable to hold the AGC level for a period of time. This can be done by raising the $\overline{\text{READ}}$/WRITE pin. This will shut off the input circuitry, and it will take time (about 2.5 μs) for the circuit to recover when going back into the read mode.

The AGC must be disabled during the servo sector. This is necessary in order to insure that the AGC does not respond to the servo signal and adjust the signal amplitude to the AGC threshold. The method of raising the $\overline{\text{READ}}$/WRITE pin voltage high will not work in this instance as the servo circuitry uses the input amplifier.

Figure 9 shows a method to hold the AGC level while remaining in the read mode (which could be used in embedded servo applications). If the voltage on V_{REF} is raised above 2V, then the amplifier output voltage cannot get large enough to turn on the circuitry to charge up C_{AGC}. For this to work properly, there cannot be a large discharge current path (resistor in parallel with C_{AGC}) across C_{AGC}. The scheme, as shown in *Figure 9*, removes the parallel resistor when the gate output is high.

The AGC block can be bypassed altogether by connecting V_{REF} to 3V. In this way, the user can use his own AGC circuit to drive the C_{AGC} pin directly.

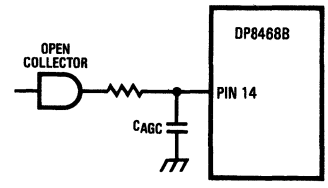

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FIGURE 8. Circuit to Decrease AGC Response Time

Application Information (Continued)

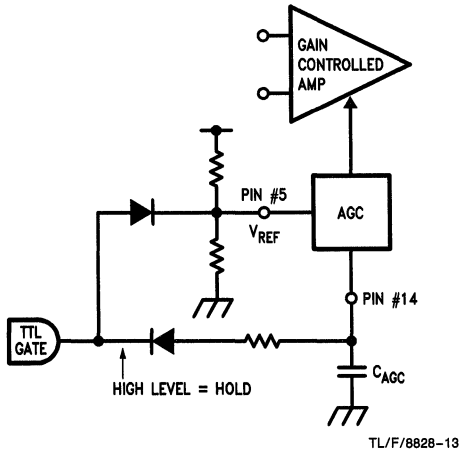

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FIGURE 9. AGC Hold Circuit

READ/WRITE

In the normal read mode, the signal from the read/write head amplifier is in the range of 20 mVpp to 660 mVpp. However, when data is being written to the disk, the signal coming into the analog input of the pulse detector will be on the order of 600 mV. Such a large signal will disturb the AGC level and would probably saturate the amplifier. In addition, if a different read/write amplifier is selected, there will be a transient introduced because the offset of the preamplifiers are not matched. A READ/WRITE input pin has been provided to minimize these effects to the pulse detector. This is a standard TTL input.

When the READ/WRITE pin is low, the pulse detector is in the read mode. When the READ/WRITE pin is taken high, three things happen. First, the 1k resistors across the AMP IN pins are shunted by 70Ω resistors, as described previously in the Gain Controlled Amplifier section. Next, the amplifier is squelched so there is no signal on the Amp Output.

Finally, the previous AGC level is held. This AGC hold function is accomplished by not allowing any current to charge up the external C_{AGC}. The voltage across this capacitor will slowly reduce due to the bias current into the Darlington (see *Figure 6*) or through any resistor placed in parallel with C_{AGC}. Therefore, as described in the Automatic Gain Control section, the gain of the amplifier will slowly increase. All of these three events happen simultaneously.

When the READ/WRITE input is returned low, the pulse detector will go back to the read mode in a specific sequence. First of all, the input impedance at the Amp In is returned to 1k. Then, after approximately 1 μs, the Gain Controlled Amplifier is taken out of the squelch mode, and finally approximately 1 μs after that, the AGC circuit is turned back on. This return to the read mode is designed to minimize analog transients in order to provide stable operation after 2.5 μs. It is very important that the analog input be stable before the chip is returned to the read mode. It is recommended that other than when writing, the Pulse Detector be in the read mode at all times in order to prevent the 2.5 μs delay from slowing up the system. The READ/WRITE pin may be connected to the Write Gate output of a controller (such as the DP8466 Disk Data Controller).

CHANNEL FILTER

The peak detection is performed by feeding the output of the Gain Controlled Amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. The differentiator can also respond to noise near the baseline, in which case the comparator gating channel will inhibit the output. The purpose of the external filter is to bandwidth limit the incoming signal for noise considerations. Care must be used in the design of this filter to ensure the delay is not a function of frequency. For this reason, a high order Bessel filter with its constant group delay characteristics can be used in this application. Often, this filter must be specifically designed to correct errors introduced by the non-ideal phase characteristics of the input read head. The typcial −3 dB point for this filter is around 1.5 times the highest recorded frequency. The design of this filter is complex and will not be discussed here. However, the following discussion does give a feel for some of the considerations involved in the filter design. The reader is referred to reference #3 listed at the end of the Applications Notes for further filter design information.

Figure 10 shows a typical Region 1 waveform where there is no bit interaction. This waveform is primarily the sum of the fundamental frequency and its 3rd harmonic (higher odd harmonics are present when there is more shouldering).

If the filter is to preserve this wave shape (this would be the case if no read/write head phase compensation were necessary) then the phase relationship between the fundamental frequency and its harmonics must not be altered. *Figure 11* shows the output when the 3rd harmonic has the proper magnitude, but the phase relationship is not maintained. The result is that the output waveform is not the same shape as the input (in a severe case it may be almost unrecognizable) and the time position of the peaks has been altered.

One electrical parameter which describes how well a filter will preserve a wave shape is called group delay. Group delay is defined as the change in phase divided by the change in frequency. If the group delay is constant over the frequencies of interest, then the wave shape will be maintained. An MFM coded signal will contain three basic frequency components for the various digital patterns of data. For instance, a 10 Megabit/sec MFM signal will consist of analog frequencies of 2.5 MHz, 3.33 MHz and 5 MHz. On the outer track the bit density is the lowest and the 5 and 3.33 MHz signals will look sinusoidal while the 2.5 MHz signal will have a tendency to return to the baseline. This returning to the baseline is called shouldering and is illustrated in *Figure 10*. Since this shouldering is rich in 3rd harmonic—the 2.5 MHz signal will have a strong 7.5 MHz component. The 10 Megabit/sec MFM signal will therefore have 2.5 MHz, 3.33 MHz, 5 MHz, and 7.5 MHz components which must be filtered with constant group delay in order to reproduce the original waveform. For example, if the phase shift through the filter at 2.5 MHz is 33.3°, then at 3.33 MHz the phase shift must be 44.3°, at 5 MHz—66.6°, and at 7.5 MHz—99.9°. The group delay $\frac{d\theta}{dt}$ for this case is 13.32°/MHz. This can be better interpreted as a time delay. 33.3° of a 2.5 MHz signal is equivalent to (33.3/360) × (1/2.5 MHz) or 37 ns. Similarly, 66.6° on a 5 MHz signal is (66.6/360) × (1/5 MHz) = 37 ns.

Application Information (Continued)

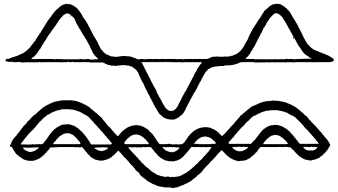

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FIGURE 10. Typical Region 1 Waveform

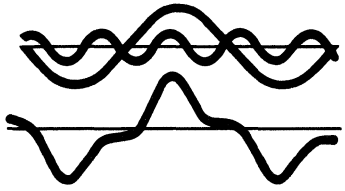

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FIGURE 11. Region 1 Waveform with the Incorrect Phase Relationship

The third order Bessel Filter as shown in the 10 Mbit/sec. pulse pairing measurement board on the data sheet is designed for a constant group delay and a −3 dB point of 7.5 MHz. At this frequency the delay through the filter is 35 ns. The Gain Controlled Amplifier of the DP8468 is designed for a group delay of a 7.8 ns for frequencies up to 7.5 MHz. The 7.8 ns delay in the Gain Controlled Amplifier and the 37 ns delay in the Bessel Filter do not introduce any timing error, only a delay of 44.3 ns from the Amp Input to the output of the filter.

DIFFERENTIATOR

A simplified circuit of the first stage of the differentiator is shown in *Figure 12*. The voltages at V3 and V4 are simply two diodes down from V1 and V2. Therefore the voltage across the external differentiator network (C_d in series with R_d) is the differential input voltage V1 − V2. When R_d is zero, the current through C_d is $I = C \times (dV/dt)$ or $C_d \times (dV_{IN}/dt)$. The Q2 collector current is the sum of the 1.8 mA current source plus the current through C_d or

$$1.8\ mA + C_d \times (dV_{IN}/dt).$$

Similarly, the Q3 collector current is

$$1.8\ mA - C_d \times (dV_{IN}/dt).$$

Therefore, the differentiator output voltage, V5 − V6, is

$$1.5k \times 2 \times C_d \times (dV_{IN}/dt).$$

The input is at a peak when V5 − V6 = 0V.

The differentiator network (C_d and R_d) should be selected so the maximum current into the differentiator network is not greater than the minimum current of I1 and I2 over temperature. In the electrical specifications, the minimum current is specified for 1.4 mA (I_{Cd} Current into Pin 1 and 24 that discharges C_d). For example, the highest analog frequency in a 10 Megabit/sec, MFM signal is 5 MHz. Since the AGC loop has forced the input to the differentiator to 2 V_{PP} (which includes the 6 dB loss of the filter), then the voltage across the capacitor (assuming R_d is 0) is:

$$V_{IN} = 1 \times \sin(2 \times \pi \times 5E6 \times t)$$

and

$$dV_{IN}/dt = 1 \times 2 \times \pi \times 5E6 \times \cos(2 \times \pi \times 5E6 \times t)$$

and the maximum slope is

$$(dV_{IN}/dt)max = 1 \times 2 \times \pi \times 5E6 = 314E5\ V/sec.$$

For this example, C_d can now be calculated. Since $I = C \times (dV/dt)$, then for I = 1.4 mA, dV/dt = 314E5, then the maximum C_d must equal 45 pF. From this example, a following simple design equation for the value of C_d can be derived.

$$C_d = 445/(V_{IN} \times f_{max})$$

where

C_d is the maximum external differentiator capacitor in pF

V_{IN} is the peak to peak differential Channel input voltage

f_{max} is the maximum analog frequency in MHz

Note that this is the maximum value for the capacitor when the series resistor R_d is zero. The value of the capacitor can

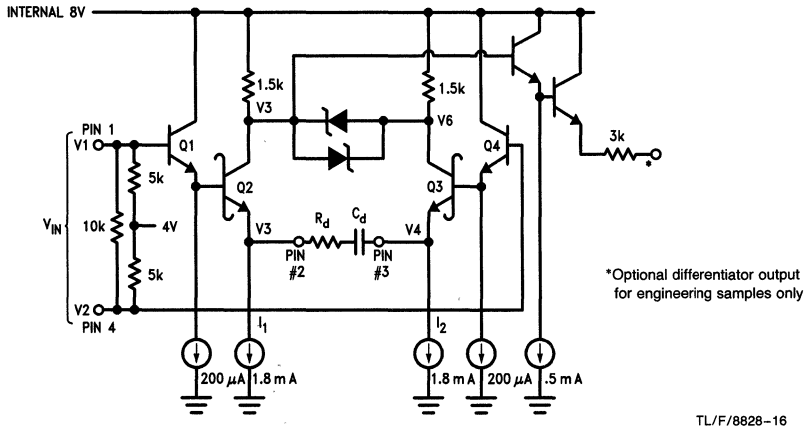

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FIGURE 12. Simplified Differentiator First Stage

Application Information (Continued)

be increased if a series resistor is used, but the maximum current through the differentiator network must not exceed 1.4 mA. If too large a value for C_d is used, the delay through the differentiator will become dependent on frequency. This will not show up in a single frequency test such as a test for pulse pairing.

For the MFM code, the maximum analog frequency is ½ the data rate. For the ½(2,7) code, the maximum analog frequency is ⅓ the data rate. The above sinusoidal analysis is valid as long as the highest frequency on the outer track is nearly sinusoidal. If, however, there is significant shouldering of this signal then the value of C_d should be reduced accordingly.

The following table summarizes the value of C_d to use for a 2 V_{pp} differential signal to the channel input.

Data Rate	Code	Maximum Frequency	C_d
5 mbits/sec	MFM	2.5 MHz	90 pF
5 mbits/sec	2,7	1.6 MHz	140 pF
10 mbits/sec	MFM	5.0 MHz	45 pF
10 mbits/sec	2,7	3.3 MHz	67 pF

As noted above, the value of the capacitor can be increased if a series resistor is used, but the maximum current through the differentiator network must not exceed 1.4 mA.

A resistor is placed in series with C_d in order to bandlimit the differentiator response. This resistor also has an effect on the phase linearity of the differentiator. An ideal differentiator produces an output that is 90 degree phase shifted from the input regardless of the input frequency. The presence of the series resistor produces an output phase shift that is less than 90 degrees and changes with the input frequency. This resistor can be used to correct for frequency related phase problems encountered elsewhere in the read path.

To properly decode the information on the disk, the read channel must determine if there is a peak (or a "1") during a period of time called a detection window. The detection window for MFM and the (2,7) code is

$$1/(2 \times \text{data bit rate}).$$

This detection window must accommodate errors in many parts of the system including filters, data separator, and peak shift variations in the data pattern. The pulse pairing of the DP8468 should be included in the error budget calculation.

DIFFERENTIAL COMPARATOR WITH HYSTERESIS

The actual peak detection is done in the time channel with the differentiator. Unfortunately, the differentiator not only responds to signal peaks but also responds to noise at the baseline. In order to prevent this noise from generating false data, the signal at the output of the Gain Controlled Amplifier is also passed through a gating channel which prevents any output change before the input signal has crossed an established level. This gating channel comprises a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is set externally via the Set Hysteresis pin. The amount of hysteresis is twice the voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential input signal must be larger than 0.6V($\pm$0.3V) before the output of the comparator will change states. The 0.6V hysteresis represents 30% of a typical 2V differential input signal level to the gating channel. The hysteresis level is usually set between 15% to 40% of the differential input signal.

The operation of the gating channel is shown in *Figure 13*. At the top is a typical Region 1 waveform which exhibits shouldering on the lowest frequency and is almost sinusoidal on the highest frequency. In this example, this waveform is fed to both the timing and the gating channel. The hysteresis level (of about 25%) has been drawn on this waveform. The second waveform is the output of the differentiator and its bi-directional one shot. While there is a positive edge pulse at each peak, there is also noise at the shoulders. This waveform is the clock for the D flip-flop.

The third waveform in *Figure 13* is the output of the Comparator with Hysteresis which goes to the D input of the flip-flop. The true peaks are the first positive edges of the differentiator's bi-directional one shot output which occur after the output of the comparator has changed states. The D flip-flop will "clock" in these valid peaks to the output bi-directional one shot. Therefore, the noise pulses (due to the

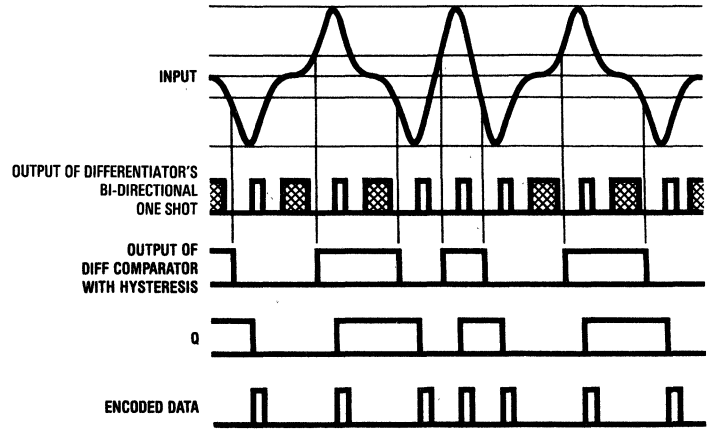

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FIGURE 13. Pulse Detector Operation for Region 1 Signals

Application Information (Continued)

differentiator responding to noise at the baseline) just "clock" in the old data through the flip-flop and the output does not change.

The Q output of the flip-flop drives the output bidirectional one-shot which generates the positive edges corresponding to the peaks. The width of the data pulses can be controlled by an external capacitor from the Set Pulse Width pin to ground. This pulse width can be adjusted from 20 ns to ½ the period of the highest frequency. Typical values for this capacitor are 20 pF for a 25 ns pulse width to 100 pF for a 100 ns pulse.

DYNAMIC HYSTERESIS

A dynamically changing hysteresis level (as a function of signal level at the Channel Input pins) can easily be implemented with the DP8468B. An amplified full wave rectified peak detecting output, pin 24, is made available for this function. A resistor capacitor network is connected from pin 24 to pin 23 as shown in *Figure 14*. The RC time constant determines the rate at which the hysteresis level can dynamically change as a function of the signal level out of the Gain Controlled Amplifier.

This time constant can be made to be much faster than the response time of the AGC of the Gain Controlled Amplifier. In this manner the hysteresis level can maintain a nearly constant percentage of the peak amplitude of the signal at the Channel Input Pins.

The charge time of the pin 24 capacitor, C_{PDO}, is set by the pin 24 output resistor. R_O, (approx. 270Ω) and the capacitor value. The discharge time is longer since the external bleed resistor, R_B, across the pin 24 capacitor is much larger than R_O. The charge time can be made longer by adding an external resistor in series with pin 24.

Figure 15 shows a plot of the hysteresis level obtained as a function of the peak to peak differential channel input level, pins 1 and 4, for the circuit shown in *Figure 14*. Note that V_{HYST} does not go to zero when there is no signal at the Channel Input. This is because pin 24 has a DC quiescent output level of approximately .8V. Consequently, a 50% reduction in the Channel Input level results in a 36% reduction in the hysteresis level in the linear region of *Figure 15*.

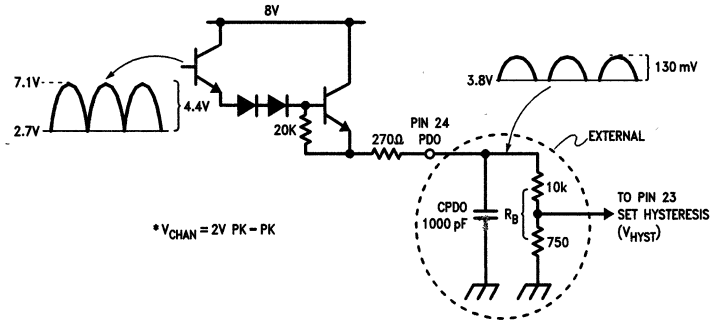

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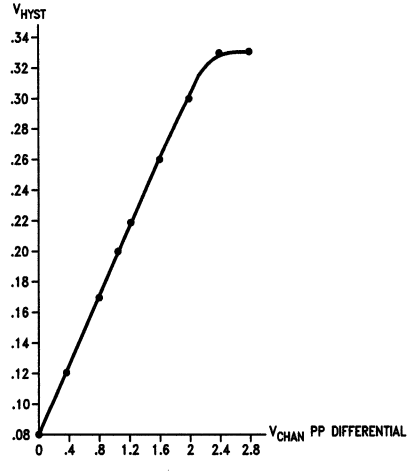
FIGURE 14. Dynamic Hysteresis Circuitry



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Note: The circuit in *Figure 14* was used to generate this curve.

FIGURE 15. Dynamic Hysteresis Operation

Application Information (Continued)

EMBEDDED SERVO DETECTION SCHEMES

Figure 16 shows the two types of embedded servo patterns the DP8468B is capable of detecting. By far the simplest pattern to detect and to write onto the disk, is the Burst Pattern. Two servo bursts are written on alternate half tracks on the disk surface. These bursts are each generally 10 μs to 30 μs in duration.

When the read head is exactly centered between the two half tracks, the amplitude of each servo burst will be equal and one half the level that would be detected had the read head been exactly centered over the servo burst. If, for example, the read head is not centered but closer to the A burst, then the detected amplitude of the A burst will be proportionately larger than the detected amplitude of the B burst. If the A and B signals are gated into separate peak detectors then the levels of the A and B burst signals are detected. Comparing the relative levels of the resulting DC voltage yields a correction term for repositioning the read/write head.

The two burst scheme is particularly easy to write on the disk surface because the A and B patterns do not overlap. Consequently, an inexpensive servo writer can be used to lay down the servo pattern. The disadvantage of this two burst approach is that because of the physical separation of the A and B burst, an error term is introduced in the relative amplitudes when this pattern is used to detect the head position during a fast seek. For example if the head is moving across the A track in the direction of the B track, then by the time the A burst is detected the head will have moved closer to the B burst, resulting in an error term. This error term may or may not be important depending on the application.

This error term during a fast seek can be eliminated with the 'Interlaced Tri-Bit Pattern', also shown in *Figure 16*. This pattern uses accurately positioned A and B pulses written on alternate half tracks. When the read head is exactly centered between the two half tracks the recovered A and B amplitudes will be exactly equal. If, for example, the read head is positioned closer to the A half track, then the A pulse will be proportionately larger than the B pulse. Because the A and B pulses are so close together in time, a third negative going Sync pulse is required to synchronize

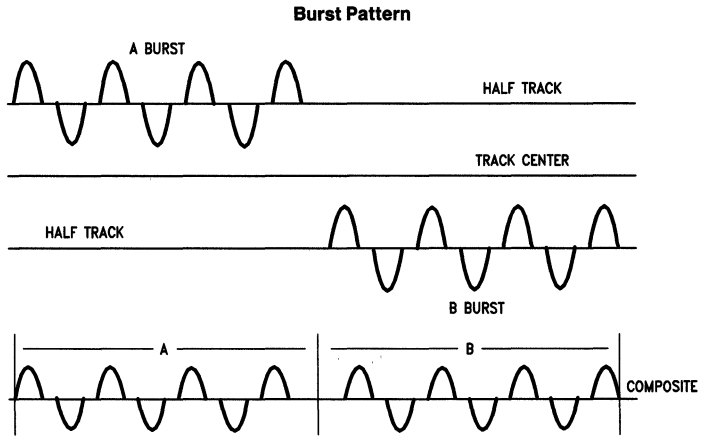

FIGURE 16. Servo Patterns

Application Information (Continued)

the gating of the A and B signals. Without the Sync pulse, there would be no way to gate the A and B pulses into the separate servo channels.

Because of the close proximity of the A and B pulses, the seek error term is eliminated. The price that is paid for this is high, however. Writing this servo pattern on the disk surface requires an expensive and very accurate servo writer. Also, external Sync detection circuitry must be added to the DP8468B. The Channel Alignment Output can be used for this purpose. Once the Sync pulse is detected then gating signals must be generated to control the Gated Detectors on the DP8468B.

GATED SERVO DETECTORS

Figure 17 is a simplified schematic of one of the gated detectors. The gated detectors require TTL gating signals which overlap the duration of the servo burst pattern. The gated detectors are basically peak detectors, but by adding a resistor in series with the peak detector capacitors, Cp1 and Cp2, filtering of the servo signal is accomplished. However, the RC time constant of this series combination should be shorter than the length of the servo burst. This allows the capacitor to fully charge up to the peak of the servo burst. Consequently, the longer the servo burst is, the longer RC time constant can be used and the less sensitive will be the Peak Detectors to noise spikes.

A separate TTL input is provided to implement the discharge of the peak detector capacitors. This discharge drains the capacitors of the charge they acquired during the previous servo sector. When discharge (pin 22) is high, approximately 1 kΩ is connected through two diodes and 1 schottky diode from the peak detector pins, 18 and 19, to ground. The discharge time will then depend on the RC time constant of the sum of the external resistor + 1 kΩ times the external capacitor.

The gated detectors are placed in a hold mode (i.e., gated off) when the gating pins 17 and 20 are high and pin 22 is low. In this mode a small leakage current (less than 1 μA) will slowly discharge the peak detector capacitors.

When centered on track, the channel input signal level from the servo burst should equal 1V peak to peak differential. Thus when on track, the servo burst is half the amplitude of the channel input signal in the data field. The channel filter should not be designed to increase the amplitude of the servo signal. The DP8468B has a built in amplifier that will boost the signal level. This amplifier saturates when the channel input signal exceeds 2V peak to peak differential. All that happens if this amplifier saturates is that the recovered DC level at the buffer outputs will not linearly track the amplitude of the channel input signal.

The output of the gated detectors drive two high input impedance unity gain buffers which provide a level shifted low impedance output voltage representation of the voltage across the peak detector capacitors. A simplified schematic of one of the buffers is shown in *Figure 18*. Though the output buffers do some level shifting, they do not level shift all the way down to a ground reference. In fact the minimum output voltage from the output buffers is approximately 1.2V for Vpin21 = 5V.

This minimum output voltage is designed to be a constant percentage of the 5V input level at pin 21 independent of temperature. This minimum output level is important when calculating an error correction term using the expression (A − B)/(A + B) where A and B represent the amplitudes of the servo burst signals. Since the A and B voltages at the buffer outputs do not go to zero, an additional term, C, must be accounted for. The modified expression then becomes:

$$\text{error} = (A - B)/(A + B - 2C)$$

where C = minimum output level of each buffer.

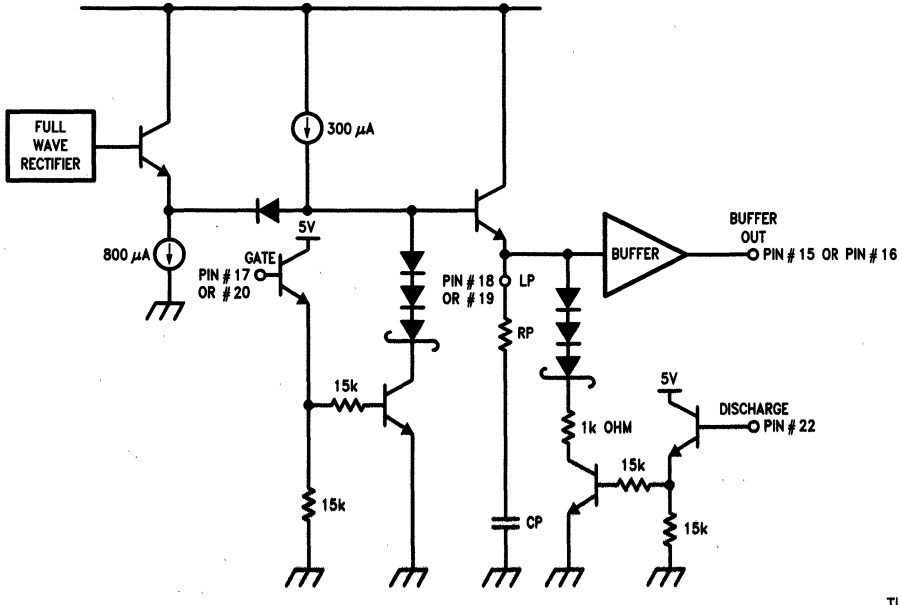

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FIGURE 17. Gated Detector

Application Information (Continued)

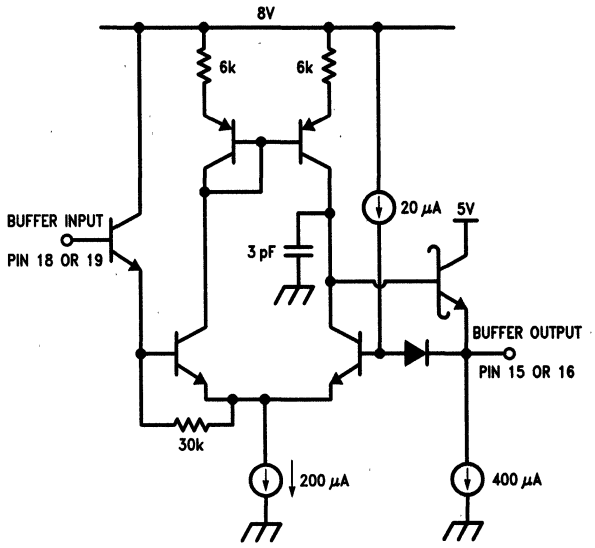

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FIGURE 18. Buffer

If C is not accounted for, a gain error will result. As mentioned above, C is designed to be a constant percentage of the voltage applied to pin 21, independent of temperature. Thus,

$$C = K * Vpin\ 21$$

where K = a constant (approx. = 0.22).

Therefore, C will represent a constant number of bits in a system that digitizes the buffer outputs and uses the voltage applied to Vpin21 as an ADC (analog to digital converter) reference.

BUFFER OUTPUTS USED WITH ADC

The output voltage levels from the buffer have been specifically designed to allow them to be directly connected to a muxed A to D converter. Some muxed ADC's allow for a reduced span by tying one of the inputs to a level that will represent all 0's when converted. This can be accomplished with the above scheme by tying the ADC input to a resistor voltage divider from pin 21 to ground with the ratio of the resistors given by:

$$[R1/(R1 + R2)] = K$$

With this technique, the full resolution of the ADC can be utilized. The span of the voltage at the buffer outputs between minimum and maximum detected signals is approximately 3.5V. Because of this large voltage span at the buffer outputs, it may not be necessary to use the above reduced span technique. The 3.5V span allows for better than 7 bits of ADC resolution when digitizing with an 8-bit ADC between 0V and the ADC reference (which should be tied to pin 21).

The output buffers have been designed so that their output levels never exceed the voltage on pin 21. Thus the user need not be concerned that the buffer outputs will exceed the maximum allowed input voltage to the ADC.

The buffers are capable of sourcing up to 3 mA of current and can sink about 300 μA. This sink current can be increased by adding an external pull down resistor from the buffer outputs to ground.

DIFFERENCE AMPLIFIER USE WITH AN ADC

Though muxed ADCs are very common today and often available as part of a microprocessor, there may be some users who do not have muxed inputs. The DP8468B can still be used in these applications by using the difference amplifier output.

A simplified schematic of the difference amplifier is shown in *Figure 19*. When the voltage at the buffer outputs are equal (i.e., on track center) the voltage at the difference amplifier output will equal the voltage on pin 21. The DC transfer function for the difference amplifier output is given below and plotted in *Figure 20:*

$$V_{OUT} = (1/2)\,[A - B] + Vpin\ 21$$

Using the above equation the maximum and minimum voltage for V_{OUT} can be calculated. They are:

V_{OUT} max. = (1/2) ([(2 * 1.75) + 1.2] − 1.2) + 5 = 6.75V

V_{OUT} min. = (1/2) (1.2 − [(2 * 1.75] + 1.2)] + 5 = 3.25V

Since most ADCs can only digitize voltages below 5V, the difference amplifier's output must some how be level shifted down. The easiest way to accomplish this is to use a resistor voltage divider from the difference amplifier output to ground. In this case a divider ratio of 5/6.75 is required to insure that the center of the divider never goes above 5V. For a symetric span about the on channel voltage (on channel voltage = (5/6.75)*5V = 3.704V) the total output span will now be 2.592V. This is a large enough span to still allow for greater than 7 bits of accuracy from an 8-bit ADC.

The above technique is only valid if the AGC has been allowed to settle to a known and constant level prior to the servo sector. Also the AGC must be put into a hold mode during the servo sector. If the AGC is allowed to adjust the signal levels to a known and constant level prior to the servo sector then the (A + B − 2C) denominator term is a constant independent of the track. Consequently, this term can be neglected from the gain error calculation and only the one difference output need be digitized.

Application Information (Continued)

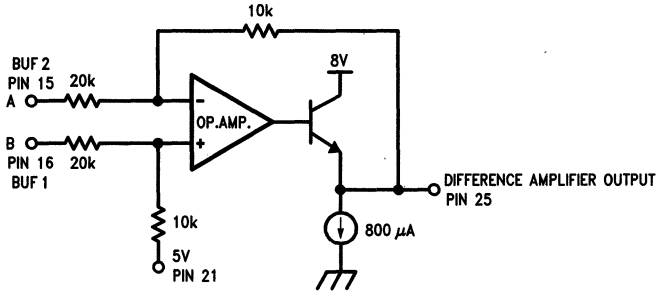

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FIGURE 19. Difference Amplifier

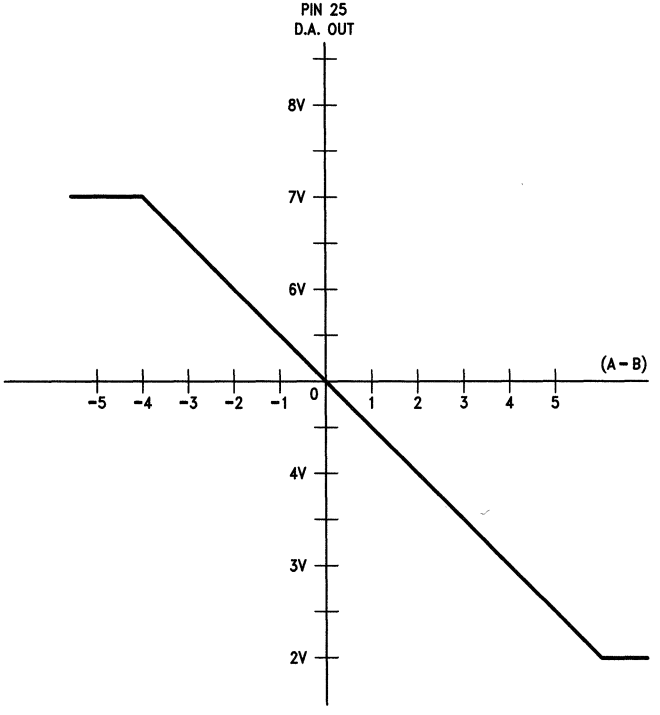

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FIGURE 20. Difference Amplifier DC Transfer Curve

Application Information (Continued)

The output stage of the difference amplifier is capable of sourcing about 3 mA of current and can sink about 500 μA. The sink current can be increased by adding an external resistor from the DA output, pin 25, to ground.

DIFFERENCE AMPLIFIER OUTPUT USED IN A LINEAR FEEDBACK SYSTEM

The difference amplifier provides an accurate difference between the two servo detector voltages. However, this difference is only an accurate representation of the positioning error after both servo channels have been updated. Consequently, the difference output is meaningless during the servo sector and only accurate after the servo sector. A linear system that is providing positioning feedback based on the output from the difference amplifier, will probably require an external sample and hold at the difference amplifier output in order to prevent a false correction during the servo sector. A sample would then be taken after the servo sector when both detectors are gated off.

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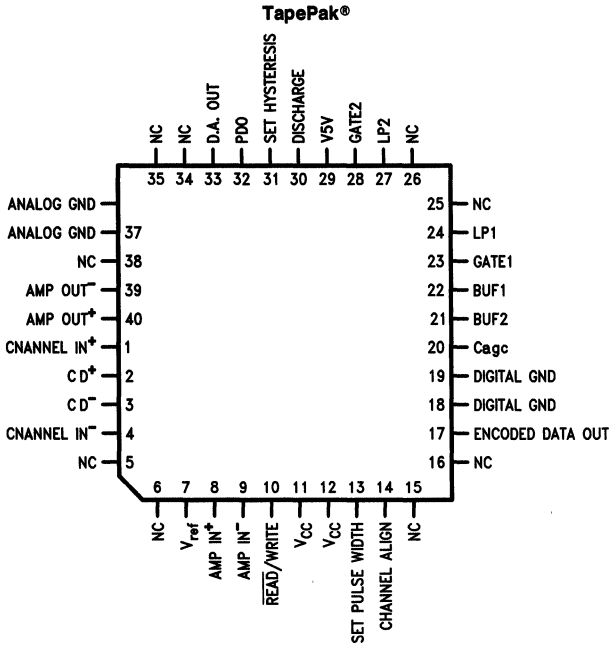
3. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley & Sons publisher, 1967.



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Top View
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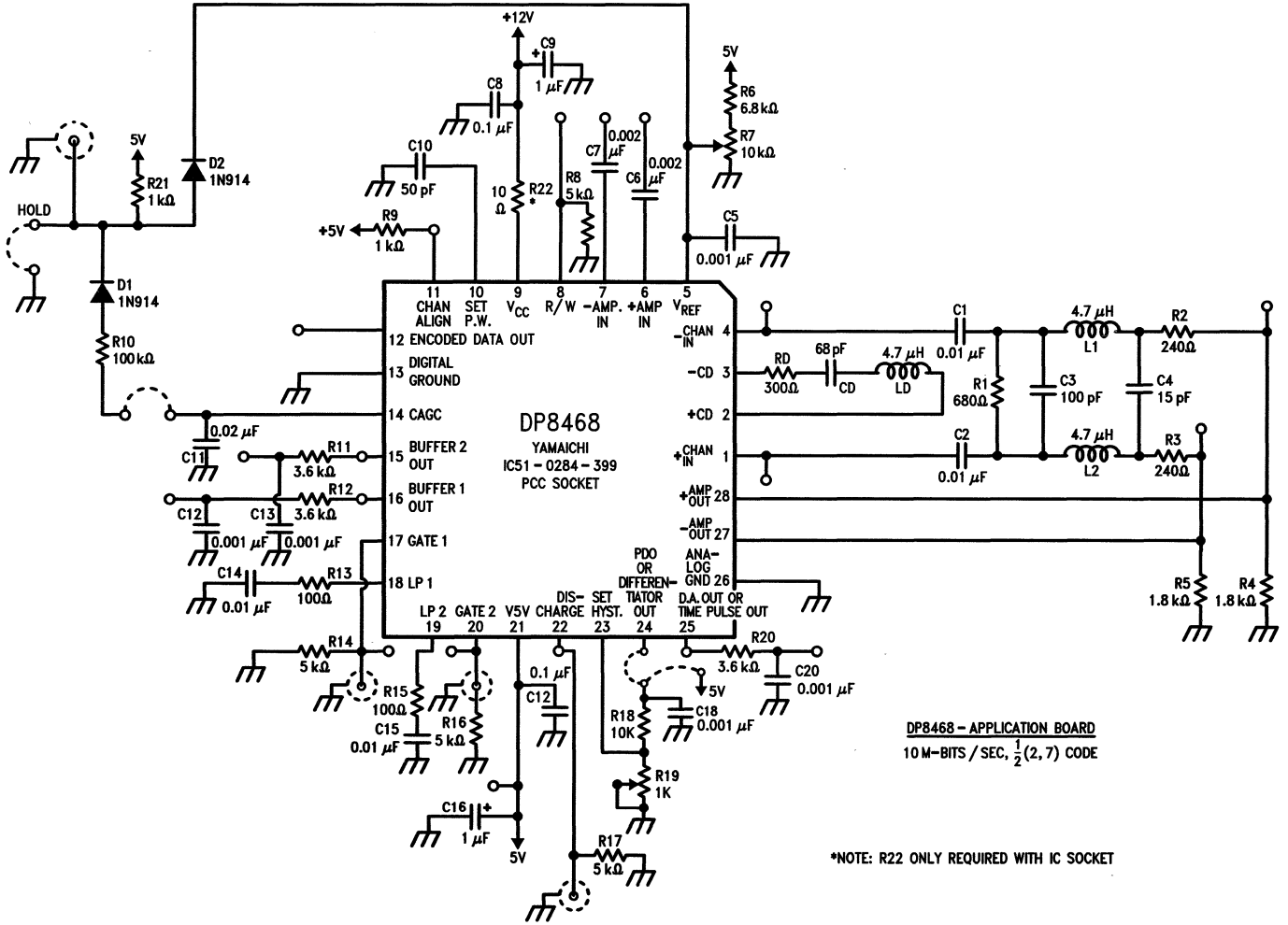
See NS Package Number TP40A



DP8468 – APPLICATION BOARD
10 M-BITS / SEC, $\frac{1}{2}$ (2, 7) CODE

*NOTE: R22 ONLY REQUIRED WITH IC SOCKET

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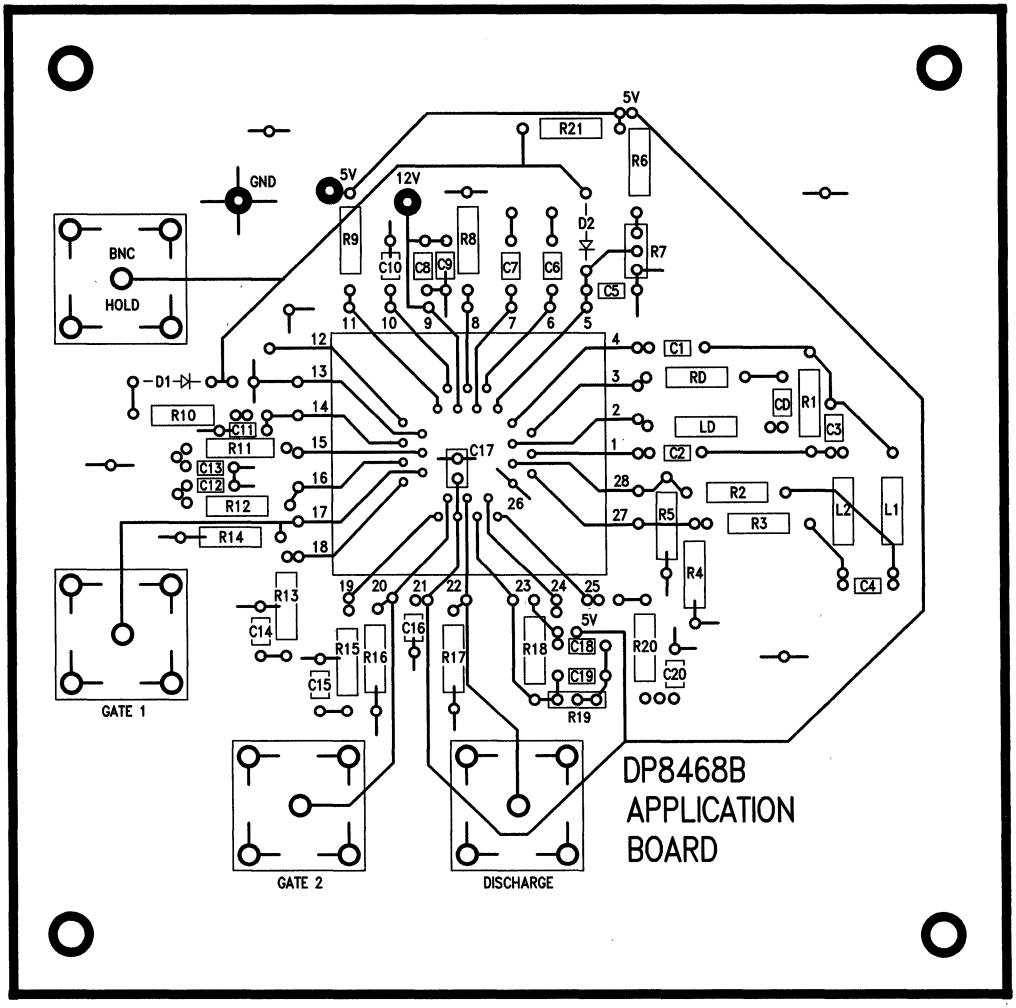
Component Side



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