1989

General Purpose Linear Devices Databook

National Semiconductor

National Semiconductor

400026

General Purpose Linear Devices

Databook

- *Continuous Voltage Regulators*
- *Switching Voltage Regulators*
- *Operational Amplifiers*
- *Buffers*
- *Voltage Comparators*
- *Instrumentation Amplifiers*
- *Surface Mount*

For information on additional linear devices, please see the Data Acquisition Linear Devices and Special Purpose Linear Devices Databooks

General Purpose Linear Devices Databook

1989 Edition

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

AbuseableTM
AnadigTM
ANS-R-TRANTM
APPSTM
ASPECTTM
Auto-Chem DeflasherTM
BCPTM
BI-FETTM
BI-FET IITM
BI-LINETM
BIPLANTM
BLCTM
BLXTM
Brite-LiteTM
BTLTM
CheckTrackTM
CIMTM
CIMBUSTM
CLASICTM
Clock✓ChekTM
COMBOTM
COMBO ITM
COMBO IITM
COPSTM microcontrollers
Datachecker®
DENSPAKTM
DIBTM
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DISCERNTM
DISTILLTM
DNR®
DPVMTM
ELSTARTM
Embedded System Processor™
E-Z-LINKTM
FACTTM
FAIRCADTM
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FAST®
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GNXTM
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HandiScanTM
HEX 3000TM
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I3L®
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Integral ISETM
IntelisplayTM
ISETM
ISE/06TM
ISE/08TM
ISE/16TM
ISE32TM
ISOPLANARTM
ISOPLANAR-ZTM
KeyScanTM
LMCMOSTM
M2CMOSTM
MacrobusTM
MacrocomponentTM
MAXI-ROM®
Meat✓ChekTM
MenuMasterTM
Microbus™ data bus
MICRO-DACTM
μtalkerTM
MicrotalkerTM
MICROWIRETM
MICROWIRE/PLUSTM
MOLETM
MSTTM
Naked-8TM
National®
National Semiconductor®
National Semiconductor Corp.®
NAX 800TM
Nitride PlusTM
Nitride Plus OxideTM
NMLTM
NOBUSTM
NSC800TM
NSCISETM
NSX-16TM
NS-XC-16TM
NTERCOMTM
NURAMTM
OXISSTM
P2CMOSTM
PC MasterTM
Perfect WatchTM
Pharma✓ChekTM
PLANTM
PLANARTM
Plus-2TM
PolycraftTM
POSilinkTM
POSitalkerTM
Power + ControlTM
POWERplanarTM
QUAD3000TM
QUIKLOOKTM
RATTM
RTX16TM
SABRTM
Script✓ChekTM
SCXTM
SERIES/800TM
Series 900TM
Series 3000TM
Series 32000®
Shelf✓ChekTM
SofChekTM
SPIRETM
STARTM
StarlinkTM
STARPLEXTM
Super-BlockTM
SuperChipTM
SuperScriptTM
SYS32TM
TapePak®
TDSTM
TeleGateTM
The National Anthem®
Time✓ChekTM
TINATM
TLCTM
TrapezoidalTM
TRI-CODETM
TRI-POLYTM
TRI-SAFETM
TRI-STATE®
TURBOTRANSCEIVERTM
VIPTM
VR32TM
WATCHDOGTM
XMOSTM
XPUTM
Z STARTM
883B/RETSTM
883S/RETSTM

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Linear Products
Introduction

National Semiconductor Corporation first established itself as the Linear Leader in 1967 with the introduction of the FIRST MONOLITHIC VOLTAGE REGULATOR . . . LM100. In the 20 years since, many of our products were firsts in performance and function. Today, this catalog spans the traditional areas of Op Amps, Voltage Regulators, Voltage References and Temperature Sensors, to Data Acquisition, Communication, Automotive, and Power Plus Control. National Semiconductor intends to remain a leader in the traditional product areas while forging ahead into VLSI solutions for analog problems and analog systems.

You can rely on National LINEAR to develop the most comprehensive product offering for use in the commercial, computer, automotive, telecommunication, industrial or military business segments. More than 1,000 basic LINEAR products (5400 options) allow design engineers to find the optimum Linear IC solution from National Semiconductor.

The Linear product line is presented in 3 Databooks. All sections are referenced and cross-indexed to provide quick and easy access. The technical information and basic product specifications are presented in data sheet format, including maximum ratings, electrical characteristics, performance curves and package information.

Additional application information is available as specific application notes or completely compiled in the LINEAR APPLICATIONS HANDBOOK. A product cross reference to the specific application note has been provided. This handbook and the 3-volume set of Linear Data Books represent a complete base of information to the National LINEAR product line.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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*Devices Not Covered In Last Publication

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Section 3 Operational Amplifiers (Continued)

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*Devices Not Covered In Last Publication

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Available Hybrid Products

Device Number	Databook
ADC1210/ADC1211	Data Acquisition Linear Devices
AF100	Data Acquisition Linear Devices
AF150	Data Acquisition Linear Devices
AF151	Data Acquisition Linear Devices
AH0014/AH0015/AH0019	Data Acquisition Linear Devices
DH0006	Individual Datasheet
DH0008	Individual Datasheet
DH0011	Individual Datasheet
DH0034	Individual Datasheet
DH0035	Individual Datasheet
DH3467	Individual Datasheet
DH3725	Individual Datasheet
LH0002	General Purpose Linear Devices
LH0003	General Purpose Linear Devices
LH0004	General Purpose Linear Devices
LH0020	General Purpose Linear Devices
LH0021/LH0041	General Purpose Linear Devices
LH0022/LH0042/LH0052	General Purpose Linear Devices
LH0023/LH0043	Data Acquisition Linear Devices
LH0024	General Purpose Linear Devices
LH0032	General Purpose Linear Devices
LH0033/LH0063	General Purpose Linear Devices
LH0036	General Purpose Linear Devices
LH0038	General Purpose Linear Devices
LH0044	General Purpose Linear Devices
LH0045	General Purpose Linear Devices
LH0053	Data Acquisition Linear Devices
LH0061	General Purpose Linear Devices
LH0062	General Purpose Linear Devices
LH0070/LH0071	Data Acquisition Linear Devices
LH0075	General Purpose Linear Devices
LH0076	General Purpose Linear Devices
LH0082	General Purpose Linear Devices
LH0084	General Purpose Linear Devices
LH0086	General Purpose Linear Devices
LH0091	Special Purpose Linear Devices
LH0094	Special Purpose Linear Devices
LH0101	General Purpose Linear Devices

Device Number	Databook
LH1605	General Purpose Linear Devices
LH2101	General Purpose Linear Devices
LH2108/LH2308	General Purpose Linear Devices
LH2110/LH2210/LH2310	General Purpose Linear Devices
LH2111/LH2211/LH2311	General Purpose Linear Devices
LH2422	Special Purpose Linear Devices
LH4001	General Purpose Linear Devices
LH4002	General Purpose Linear Devices
LH4003	General Purpose Linear Devices
LH4004	General Purpose Linear Devices
LH4006	General Purpose Linear Devices
LH4008	General Purpose Linear Devices
LH4009	General Purpose Linear Devices
LH4010	General Purpose Linear Devices
LH4011	General Purpose Linear Devices
LH4012	General Purpose Linear Devices
LH4033/LH4063	General Purpose Linear Devices
LH4101	General Purpose Linear Devices
LH4104	General Purpose Linear Devices
LH4105	General Purpose Linear Devices
LH4106	General Purpose Linear Devices
LH4117	General Purpose Linear Devices
LH4118	General Purpose Linear Devices
LH4124	General Purpose Linear Devices
LH4141	General Purpose Linear Devices
LH4161	General Purpose Linear Devices
LH4162	General Purpose Linear Devices
LH4200	General Purpose Linear Devices
LH4266	Special Purpose Linear Devices
LH4860	Data Acquisition Linear Devices
LH7001	General Purpose Linear Devices
LH7070/LH7071	Data Acquisition Linear Devices
HS7067	General Purpose Linear Devices
HS7107	General Purpose Linear Devices
MH0007	Individual Datasheet

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Additional Available Linear Devices

Additional Available Linear Devices (Continued)

Additional Available Linear Devices (Continued)

Device	Databook
LF398A Monolithic Sample and Hold Circuit	Data Acquisition Linear Devices
LF11201 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF11202 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF11331 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF11332 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF11333 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13006 Digital Gain Set	Data Acquisition Linear Devices
LF13007 Digital Gain Set	Data Acquisition Linear Devices
LF13201 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13202 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13331 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13332 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13333 Quad SPST JFET Analog Switch	Data Acquisition Linear Devices
LF13508 8-Channel Analog Multiplexer	Data Acquisition Linear Devices
LF13509 4-Channel Analog Multiplexer	Data Acquisition Linear Devices
LH0023 Sample and Hold Circuit	Data Acquisition Linear Devices
LH0043 Sample and Hold Circuit	Data Acquisition Linear Devices
LH0053 High Speed Sample and Hold Amplifier	Data Acquisition Linear Devices
LH0070 Series BCD Buffered Reference	Data Acquisition Linear Devices
LH0071 Series Precision Buffered Reference	Data Acquisition Linear Devices
LH0091 True RMS to DC Converter	Special Purpose Linear Devices
LH0094 Multifunction Converter	Special Purpose Linear Devices
LH2422 CRT Video Driver Amplifier	Special Purpose Linear Devices
LH4266 SPDT RF Switch	Special Purpose Linear Devices
LH4860 Super Fast 12-Bit Track-Hold Amplifier	Data Acquisition Linear Devices
LH7070 Series Precision BCD Buffered Reference	Data Acquisition Linear Devices
LH7071 Series Precision Binary Buffered Reference	Data Acquisition Linear Devices
LM34 Precision Fahrenheit Temperature Sensor	Data Acquisition Linear Devices
LM35 Precision Centigrade Temperature Sensor	Data Acquisition Linear Devices
LM113 Reference Diode	Data Acquisition Linear Devices
LM122 Precision Timer	Special Purpose Linear Devices
LM129 Precision Reference	Data Acquisition Linear Devices
LM131 Precision Voltage-to-Frequency Converter	Data Acquisition Linear Devices
LM134 3-Terminal Adjustable Current Source	Data Acquisition Linear Devices
LM135 Precision Temperature Sensor	Data Acquisition Linear Devices
LM136-2.5V Reference Diode	Data Acquisition Linear Devices
LM136-5.0V Reference Diode	Data Acquisition Linear Devices
LM168 Precision Voltage Reference	Data Acquisition Linear Devices
LM169 Precision Voltage Reference	Data Acquisition Linear Devices
LM185 Adjustable Micropower Voltage Reference	Data Acquisition Linear Devices
LM185-1.2 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM185-2.5 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM194 SuperMatch Pair	Special Purpose Linear Devices
LM195 Ultra Reliable Power Transistor	Special Purpose Linear Devices
LM199 Precision Reference	Data Acquisition Linear Devices
LM231 Precision Voltage-to-Frequency Converter	Data Acquisition Linear Devices
LM234 3-Terminal Adjustable Current Source	Data Acquisition Linear Devices
LM235 Precision Temperature Sensor	Data Acquisition Linear Devices
LM236-2.5V Reference Diode	Data Acquisition Linear Devices
LM236-5.0V Reference Diode	Data Acquisition Linear Devices
LM268 Precision Voltage Reference	Data Acquisition Linear Devices
LM285 Adjustable Micropower Voltage Reference	Data Acquisition Linear Devices

Additional Available Linear Devices (Continued)

Device	Databook
LM285-1.2 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM285-2.5 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM295 Ultra Reliable Power Transistor	Special Purpose Linear Devices
LM299 Precision Reference	Data Acquisition Linear Devices
LM313 Reference Diode	Data Acquisition Linear Devices
LM322 Precision Timer	Special Purpose Linear Devices
LM329 Precision Reference	Data Acquisition Linear Devices
LM331 Precision Voltage-to-Frequency Converter	Data Acquisition Linear Devices
LM334 3-Terminal Adjustable Current Source	Data Acquisition Linear Devices
LM335 Precision Temperature Sensor	Data Acquisition Linear Devices
LM336-2.5V Reference Diode	Data Acquisition Linear Devices
LM336-5.0V Reference Diode	Data Acquisition Linear Devices
LM368 Precision Voltage Reference	Data Acquisition Linear Devices
LM368-2.5 Precision Voltage Reference	Data Acquisition Linear Devices
LM369 Precision Voltage Reference	Data Acquisition Linear Devices
LM380 Audio Power Amplifier	Special Purpose Linear Devices
LM381 Low Noise Dual Preamplifier	Special Purpose Linear Devices
LM382 Low Noise Dual Preamplifier	Special Purpose Linear Devices
LM383 7 Watt Audio Power Amplifier	Special Purpose Linear Devices
LM384 5 Watt Audio Power Amplifier	Special Purpose Linear Devices
LM385 Adjustable Micropower Voltage Reference	Data Acquisition Linear Devices
LM385-1.2 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM385-2.5 Micropower Voltage Reference Diode	Data Acquisition Linear Devices
LM386 Low Voltage Audio Power Amplifier	Special Purpose Linear Devices
LM387 Low Noise Dual Preamplifier	Special Purpose Linear Devices
LM388 1.5-Watt Audio Power Amplifier	Special Purpose Linear Devices
LM389 Low Voltage Audio Power Amplifier with NPN Transistor Array	Special Purpose Linear Devices
LM390 1 Watt Battery Operated Audio Power Amplifier	Special Purpose Linear Devices
LM391 Audio Power Driver	Special Purpose Linear Devices
LM394 SuperMatch Pair	Special Purpose Linear Devices
LM395 Ultra Reliable Power Transistor	Special Purpose Linear Devices
LM399 Precision Reference	Data Acquisition Linear Devices
LM555 Timer	Special Purpose Linear Devices
LM555C Timer	Special Purpose Linear Devices
LM556 Dual Timer	Special Purpose Linear Devices
LM556C Dual Timer	Special Purpose Linear Devices
LM565 Phase Locked Loop	Special Purpose Linear Devices
LM565C Phase Locked Loop	Special Purpose Linear Devices
LM566C Voltage Controlled Oscillator	Special Purpose Linear Devices
LM567 Tone Decoder	Special Purpose Linear Devices
LM567C Tone Decoder	Special Purpose Linear Devices
LM592 Differential Video Amplifier	Special Purpose Linear Devices
LM621 Brushless Motor Commutator	Special Purpose Linear Devices
LM628 Precision Motion Controller	Special Purpose Linear Devices
LM629 Precision Motion Controller	Special Purpose Linear Devices
LM733 Differential Video Amplifier	Special Purpose Linear Devices
LM733C Differential Video Amplifier	Special Purpose Linear Devices
LM831 Low Voltage Audio Power Amplifier	Special Purpose Linear Devices
LM832 Dynamic Noise Reduction System DNR	Special Purpose Linear Devices
LM903 Fluid Level Detector	Special Purpose Linear Devices
LM1035 Dual DC Operated Tone/Volume/Balance Circuit	Special Purpose Linear Devices
LM1036 Dual DC Operated Tone/Volume/Balance Circuit	Special Purpose Linear Devices

Additional Available Linear Devices (Continued)

Additional Available Linear Devices (Continued)

Device	Databook
LM2002 8 Watt Audio Power Amplifier	Special Purpose Linear Devices
LM2005 20 Watt Automotive Power Amplifier	Special Purpose Linear Devices
LM2065 Advanced FM IF System	Special Purpose Linear Devices
LM2877 Dual 4 Watt Power Audio Amplifier	Special Purpose Linear Devices
LM2878 Dual 5 Watt Power Audio Amplifier	Special Purpose Linear Devices
LM2879 Dual 8 Watt Audio Amplifier	Special Purpose Linear Devices
LM2889 TV Video Modulator	Special Purpose Linear Devices
LM2893 Carrier Current Transceiver	Special Purpose Linear Devices
LM2896 Dual Power Audio Amplifier	Special Purpose Linear Devices
LM2905 Precision Timer	Special Purpose Linear Devices
LM2907 Frequency to Voltage Converter	Special Purpose Linear Devices
LM2917 Frequency to Voltage Converter	Special Purpose Linear Devices
LM3045 Transistor Array	Special Purpose Linear Devices
LM3046 Transistor Array	Special Purpose Linear Devices
LM3086 Transistor Array	Special Purpose Linear Devices
LM3089 FM Receiver IF System	Special Purpose Linear Devices
LM3146 High Voltage Transistor Array	Special Purpose Linear Devices
LM3189 FM IF System	Special Purpose Linear Devices
LM3361A Low Voltage/Power Narrow Band FM IF System	Special Purpose Linear Devices
LM3820 AM Radio System	Special Purpose Linear Devices
LM3905 Precision Timer	Special Purpose Linear Devices
LM3909 LED Flasher/Oscillator	Special Purpose Linear Devices
LM3911 Temperature Controller	Data Acquisition Linear Devices
LM3914 Dot/Bar Display Driver	Special Purpose Linear Devices
LM3915 Dot/Bar Display Driver	Special Purpose Linear Devices
LM3916 Dot/Bar Display Driver	Special Purpose Linear Devices
LM3999 Precision Reference	Data Acquisition Linear Devices
LM4500A High Fidelity FM Stereo Demodulator with Blend	Special Purpose Linear Devices
LM18293 Four Channel Push Pull Driver	Special Purpose Linear Devices
LMC555 CMOS Timer	Special Purpose Linear Devices
LMC567 Low Power Tone Decoder	Special Purpose Linear Devices
LMC568 Low Power Phase-Locked Loop	Special Purpose Linear Devices
LMC835 Digital Controlled Graphic Equalizer	Special Purpose Linear Devices
LMF90 4th-Order LMCMOS™ Programmable Elliptic Notch Filter	Data Acquisition Linear Devices
LMF100 High Performance Dual Switched Capacitor Filter	Data Acquisition Linear Devices
LMF120 Mask Programmable Switched Capacitor Filter	Data Acquisition Linear Devices
LP395 Ultra Reliable Power Transistor	Special Purpose Linear Devices
MF4 4th Order Switched Capacitor Butterworth Lowpass Filter	Data Acquisition Linear Devices
MF5 Universal Monolithic Switched Capacitor Filter	Data Acquisition Linear Devices
MF6 6th Order Switched Capacitor Butterworth Lowpass Filter	Data Acquisition Linear Devices
MF8 4th Order Switched Capacitor Bandpass Filter	Data Acquisition Linear Devices
MF10 Universal Monolithic Dual Switched Capacitor Filter	Data Acquisition Linear Devices
MM54C905 12-Bit Successive Approximation Register	Data Acquisition Linear Devices
MM54HC4016 Quad Analog Switch	Data Acquisition Linear Devices
MM54HC4051 8-Channel Analog Multiplexer	Data Acquisition Linear Devices
MM54HC4052 Dual 4-Channel Analog Multiplexer	Data Acquisition Linear Devices
MM54HC4053 Triple 2-Channel Analog Multiplexer	Data Acquisition Linear Devices
MM54HC4066 Quad Analog Switch	Data Acquisition Linear Devices
MM54HC4316 Quad Analog Switch with Level Translator	Data Acquisition Linear Devices
MM74C905 12-Bit Successive Approximation Register	Data Acquisition Linear Devices
MM74HC4016 Quad Analog Switch	Data Acquisition Linear Devices
MM74HC4051 8-Channel Analog Multiplexer	Data Acquisition Linear Devices

Additional Available Linear Devices (Continued)

Device	Databook
MM74HC4052 Dual 4-Channel Analog Multiplexer	Data Acquisition Linear Devices
MM74HC4053 Triple 2-Channel Analog Multiplexer	Data Acquisition Linear Devices
MM74HC4066 Quad Analog Switch	Data Acquisition Linear Devices
MM74HC4316 Quad Analog Switch with Level Translator	Data Acquisition Linear Devices
μA9708 6-Channel 8-Bit μP Compatible A/D Converter	Data Acquisition Linear Devices

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CROSS REFERENCE BY PART NUMBER

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers are listed in this section and reference the nearest National Semiconductor Corp. direct replacement or recommended replacement with either an improved or functional replacement. The following notations are appended to assist you in finding the best option.

No reference note ..... "DIRECT REPLACEMENT"

Note (1) ..... "IMPROVED REPLACEMENT" Pin-for-Pin replacement with "SUPERIOR" Electrical Specifications.

Note (2) ..... "FUNCTIONAL REPLACEMENT" Similar device. Consult datasheet to determine the suitability for specific application.

Note (3) ..... "SIMILAR DEVICE" with superior performance. Consult datasheet to determine suitability of the replacement for specific application.

ANALOG DEVICES	NATIONAL	
AD0042	LH0042	(2)
AD101A	LM101A	(1)
AD201A	LM210A	(1)
AD301A	LM301A	(1)
AD3542	LH0042	(2)
AD5035	LH0042	(2)
AD506	LH0022	(2)
AD509	LH0003	(2)
AD521	LH0036	(2)
AD521	LM363	(2)
AD524	LH0038	(2)
AD537	LM331	(2)
AD562	DAC1266	(3)
AD563	DAC1265	(3)
AD565A	DAC1265	
AD566A	DAC1266	
AD567	DAC1230	(2)
AD573	ADC1005	(2)
AD581	LH0070	(1)
AD581	LM581	
AD582	LF398	(2)
AD583	LF198	(3)
AD588	LM369	(2)
AD589M	LM385	(1)
AD589U	LM185	(1)
AD590	LM134	(2)
AD590	LM135	(2)
AD590	LM34	(3)
AD590	LM35	(3)
AD611J	LF411C	(1)
AD611K	LF411AC	(1)
AD614	LH0086	(2)
AD624	LH0038	(2)
AD650	LM331	(2)
AD651	LM331	(2)
AD654	LM331	(2)
AD673	ADC0841	(2)
AD741	LM741	
AD7502	LF13509	(2)
AD7516	CD4066B	(2)
AD7523	DAC0830	(2)
AD7523	DAC0831	(2)
AD7523	DAC0832	(2)
AD7524	DAC0830	(2)
AD7524	DAC0831	(2)
AD7524	DAC0832	(2)
AD7533	DAC1020	
AD7533	DAC1021	
AD7533	DAC1022	
AD7541	DAC1218	(1)
AD7541	DAC1219	(1)
AD7541A	DAC1218	(2)
AD7541A	DAC1219	(2)
AD7542	DAC1208	(2)
AD7542	DAC1209	(2)
AD7542	DAC1210	(2)
AD7545	DAC1208	(2)
AD7545	DAC1209	(2)
AD7545	DAC1210	(2)
AD7548	DAC1230	(2)
AD7548	DAC1231	(2)
AD7548	DAC1232	(2)
AD7552	ADC1220	(2)
AD7552	ADC1225	(2)
AD7571	ADC1005	(2)
AD7571	ADC1025	(2)
AD7575	ADC0820	(2)
AD7576	ADC0820	(2)
AD7578	ADC1205	(2)
AD7578	ADC1225	(2)
AD7820	ADC0820	
ADDAC-08	DAC0800	
ADDAC-08	DAC0801	
ADDAC-08	DAC0802	
ADDAC80	DAC1280+	(1)
ADDAC85	DAC2180+	(1)
ADLH0032	LH0032	(2)
ADLH0033	LH0033	(2)
ADOP07	LM607	(1)

APEX	NATIONAL	
PA01	LH0101	(2)
PA01	LM12	(2)
PA07	LM12	(2)
PA010	LH0101	(2)
PA010	LM12	(2)
PA011	LM12	(2)
PA51	LM12	(2)
PA73	LM12	(2)

BURR-BROWN	NATIONAL	
3507	LM6361	(2)
3533	LH0033	(2)
3542	LH0042	(2)
3550	LM6361	(2)
3551	LM6361	(2)
3553	LH0063	(2)
3554	LH0032	(2)
3571	LM675	(2)
3572	LH0021	(2)
3573	LM675	(2)
3626	LH0036	(2)
3629	LH0038	(2)
3606A6	LH0084	(2)
3606A6	LH0086	(2)
HOS-100	LH0033	(2)
INA102	LH0038	(2)
SHC298A	LF398A	(1)
SHC80	LF398	(2)
SHC85	LF398	(2)

CTS	NATIONAL	
CTS0002	LH002	
CTS0004	LH0004	
CTS0021	LH0021	
CTS0024	LH0024	
CTS0032	LH0032	
CTS0033	LH0033	
CTS0041	LH0041	
CTS0042	LH0042	
CTS2101A	LH2101A	
CTS2111	LH2111	

ELANTEC	NATIONAL	
EHA2500	LM6161	(2)
EHA2502	LM6161	(2)
EHA2505	LM6361	(2)
EHA2510	LM6161	(2)
EHA2512	LM6161	(2)
EHA2515	LM6361	(2)
EHA2520	LM6164	(2)
EHA2522	LM6164	(2)
EHA2525	LM6364	(2)
EHA2600	LM6161	(2)
EHA2602	LM6161	(2)
EHA2605	LM6361	(2)
EHA2620	LM6164	(2)
EHA2622	LM6164	(2)
EHA2625	LM6364	(2)
EL2006	LM6161	(2)
EL2006C	LM6261	(2)
ELH0002	LH0002	(1)
ELH0021	LH0021	(1)
ELH0032	LH0032	(1)
ELH0033	LH0033	(1)
ELH0041	LH0041	(1)
ELH0101	LH0101	(1)

EXAR	NATIONAL	
XR-1001	MF4C-100	(1)
XR-1002	MF4C-50	(1)
XR084	LF347	(1)
XR084M	LF147	(1)
XR1458	LM1458	(1)
XR146	LF146	(1)
XR246	LF246	(1)
XR346	LF346	(1)

HARRIS (Incl. GE/RCA/ INTERSIL)	NATIONAL	
AD7520	DAC1021	
AD7520	DAC1022	
AD7521	DAC1220	
AD7521	DAC1221	
AD7521	DAC1222	
AD7530	DAC1020	(3)
AD7530	DAC1021	(3)
AD7530	DAC1022	(3)
AD7531	DAC1220	
AD7531	DAC1221	
AD7531	DAC1222	
AD7533	DAC1020	
AD7533	DAC1021	
AD7533	DAC1022	
AD7541	DAC1218	
AD7541	DAC1219	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
CA081	LF411M	(2)
CA081A	LF411C	(2)
CA081B	LF411C	(2)
CA081C	TL081C	(2)
CA082	LF412M	(2)
CA082A	LF412C	(2)
CA082B	LF412C	(2)
CA082C	TL082C	(2)
CA084	LF147	(2)
CA084B	LF347B	(2)
CA084C	LF347	(2)
CA124	LM124	(1)
CA139	LM139	(1)
CA139A	LM139A	(1)
CA1458	LM1458	(1)
CA1558	LM1558	(1)
CA158	LM158	(1)
CA158A	LM158A	(1)
CA224	LM224	(1)
CA239	LM239	(1)
CA239A	LM239A	(1)
CA258	LM258	(1)
CA258A	LM258A	(1)
CA301A	LM301A	(1)
CA307	LM307	(1)
CA3105	LM675	(2)
CA311	LM311	(1)
CA324	LM324	(1)
CA3290	LM393	(2)
CA339	LM339	(1)
CA339A	LM339A	(1)
CA3401	LM3401	(1)
CA358	LM358	(1)
CA358A	LM358A	(1)
CA741	LM741	(1)
CA747	LM747	(1)
CA748	LM748	(1)
DG201	LF11201	
DG211	LF13201	
DG212	LF13202	
HA-OP07	LM607	(1)
HA2400	LM604AM	(2)
HA2404	LM604AM	(2)
HA2405	LM604C	(2)
HA2406	LM604C	(2)
HA2500	LM6161	(2)
HA2502	LM6161	(2)
HA2505	LM6361	(2)
HA2510	LM6161	(2)
HA2512	LM6161	(2)
HA2515	LM6361	(2)
HA2520	LH0003	(1)
HA2520	LM6164	(2)
HA2522	LH0003	(1)
HA2522	LM6164	(2)
HA2525	LH0003	(1)
HA2525	LH6364	(2)
HA2530	LH0024	(2)
HA2535	LH0024	(2)
HA2540	LH0032	(2)
HA2541-2	LM6161	(2)
HA2541-5	LM6361	(2)
HA2542	LH0032	(2)
HA2542-2	LM6164	(2)
HA2542-5	LM6164	(2)
HA2600	LM6161	(2)
HA2602	LM6161	(2)
HA2605	LM6361	(2)
HA2620	LM6164	(2)
HA2622	LM6164	(2)
HA2625	LM6364	(2)
HA2640	LH0004	(1)
HA5033	LH0033	(1)
HA5162	LH0062	(2)
HA5180	LH0052	(1)
HF-10	MF10	
HI-201	LF13201	
HI-300	AH5020	(2)
ICH8530	LH0101	(2)
ICL7114	ADC1205	(2)
ICL7114	ADC1225	(2)
ICL7660	LMC7660	(1)
ICL8069	LM313	
ICL8069	LM385-1.2	
IH5009	AH5009	
IH5010	AH5010	
IH5011	AH5011	
IH5012	AH5012	
IH6108	LF13508	
IH6208	LF13509	
LM741	LM741	
μA748	LM748	

HEWLETT-PACKARD	NATIONAL	
HCTL-100	LM628	(3)

HITACHI	NATIONAL	
HA13421A	LM18293	(3)
HA17082	LF353	(1)
HA17082A	LF412	(1)
HA17084	LF347	(1)
HA17084A	LF347B	(1)
HA17094	LM2904	(1)
HA17301	LM3301	(1)
HA17324	LM324	(1)
HA17339	LM339	(1)
HA17358	LM358	(1)
HA17393	LM393	(1)
HA17458	LM1458	(1)
HA17741	LM741	(1)
HA17747	LM747	(1)
HA17901	LM2901	(1)
HA17902	LM2902	(1)
HA17903	LM2903	(1)

LINEAR TECHNOLOGY	NATIONAL	
AD581	LH0070	
AD581	LM581	
LM1009M	LM136-2.5	
LM129	LM129	
LM134	LM134	
LM185	LM185	
LM199	LM199	
LM234	LM234	
LM329	LM329	
LM334	LM334	
LM385	LM385	
LM399	LM399	
LT1001	LM607A	(1)
LT1004C	LM385	
LT1004M	LM185	
LT1009C	LM336-2.5	
LT1019C	LM368	(2)
LT1019M	LM168	(2)
LT1020	LP2951	(3)
LT1021C	LM369	(1)
LT1021M	LM169	(1)
LT1029C	LM336-5.0	
LT1029M	LM136-5.0	
LT1031	LH0070	
LT117A	LM117A	

LT123A	LM123A	
LT138A	LM138A	
LT150A	LM150A	
LT317A	LM317A	
LT323A	LM323A	
LT338A	LM338A	
LT350A	LM350A	
REF-01	LM168	(1)
REF-01	LM368	(1)
SG1524	LM1524D	(1)
SG1525A	LM1525A	(2)
SG1527A	LM1527A	(2)
SG3524	LM3524D	(1)
SG3525A	LM3525A	(2)
SG3527A	LM3527A	(2)

LSI COMPUTER	NATIONAL	
LS7261	LM621	(3)
LS7263	LM621	(3)

MICRA	NATIONAL	
MC0002	LH0002	
MC0003	LH0003	
MC0004	LH0004	
MC0032	LH0032	
MC0033	LH0033	
MC0041	LH0041	
MC0063	LH0063	

MICRO POWER	NATIONAL	
MP108	LM108	
MP108A	LM108A	
MP155	LF155	
MP155A	LF155A	
MP156	LF156	
MP156A	LF156A	
MP157	LF157	
MP157A	LF157A	
MP208	LM208	
MP208A	LM208A	
MP2108A	LH2108A	
MP308	LM308	
MP308A	LM308A	
MP355A	LF355A	
MP356A	LF356A	
MP357A	LF357A	
MP5010G	LM185	
MP5010G	LM385	
MP5010H	LM185	
MP5010H	LM385	
MP5010L	LM185	
MP5010L	LM385	
MPOP07	LM607	(1)

MOTOROLA	NATIONAL	
AD562A	DAC1266	(2)
AD563A	DAC1265	(2)
DAC-08	DAC0800	
DAC-08	DAC0801	
DAC-08	DAC0802	
LM109H	LM109H	
LM109K	LM109K STEEL	
LM117K	LM117K STEEL	
LM123K	LM123K STEEL	
LM137K	LM137K STEEL	
LM150K	LM150K STEEL	
LM2931	LM2931	
LM309K	LM309K STEEL	
LM317K	LM317K STEEL	
LM323K	LM323K STEEL	
LM337K	LM337K STEEL	
LM350K	LM350K STEEL	
MC1408	DAC0806	
MC1408	DAC0807	
MC1408	DAC0808	
MC1414	LM1414	
LM1436	LM343	(1)
MC14442	ADC0829	(2)
MC14444	ADC0830	(2)
MC145040	ADC0811	(2)
MC145041	ADC0811	
MC1458	LM1458	
MC1496	LM1496	
MC1508	DAC0808	
MC1514	LM1514	
MC1536	LM143	(1)
MC1558	LM1558	
MC1596	LM1596	
MC1709	LM709	
MC1710	LM710	
MC1723	LM723	
MC1723C	LM723C	
MC1741	LM741	
MC1747	LM747	
MC1748	LM748	
MC3301	LM3301	
MC3302	LM3302	
MC3361	LM3361A	(1)
MC34001	LF351	(1)
MC34001A	LF411C	(1)
MC34001B	LF411C	(1)
MC34002	LF353	(1)
MC34002A	LF412A	(1)
MC34002B	LF412C	(1)
MC34004	LF147	(1)
MC34004	LF347	(1)
MC34004B	LF147	(1)
MC34004B	LF347B	(1)
MC3401	LM3401	(1)
MC3410	DAC1020	
MC3412	DAC1265	(2)
MC35001	LF411M	(1)
MC35001A	LF411M	(1)
MC35001B	LF411M	(1)
MC35002	LF412M	(1)
MC35002A	LF412AM	(1)
MC35002B	LF412M	(1)
MC3510	DAC1020	(2)
MC4741	LM348	
MC78LXXACG	LM78LXXACH	
MC78LXXACP	LM78LXXACZ	
MC78LXXCG	LM78LXXCH	
MC78LXXCP	LM78LXXSACZ	
MC78MXXCT	LM341P-XX	
MC78MXXCT	LM342P-XX	
MC78MXXCT	LM78MXXCT	
MC78XXACT	LM340AT-XX	
MC78XXCK	LM78XXCK	
MC78XXCT	LM78XXCT	
MC79LXXACG	LM320H-XX	
MC79LXXACP	LM320LZ-XX	
MC79LXXCP	LM79LXXCZ	
MC79LXXCP	LM79LXXCZ	
MC79MXXAKC	LM320MP-XX	
MC79XXACT	LM320T-XX	
MC79XXAKC	LM320K-XX	
MC79XXCK	LM320K-XX	
MC79XXCK	LM79XXCK	
MC79XXCT	LM79XXCT	

PRECISION MONOLITHIC INC.	NATIONAL	
ADC-910	ADC1005	(2)
ADC-910	ADC1025	(2)
AMP-01	LH0038	(2)
BUF-03	LH0033	(1)
DAC-02	DAC1020	(2)
DAC-02	DAC1021	(2)
DAC-02	DAC1022	(2)
DAC-03	DAC1020	(2)
DAC-03	DAC1021	(2)
DAC-03	DAC1022	(2)
DAC-05	DAC1020	(2)
DAC-05	DAC1021	(2)
DAC-05	DAC1022	(2)
DAC-08	DAC0800	
DAC-08	DAC0801	
DAC-08	DAC0802	
DAC-100	DAC1020	(2)
DAC-100	DAC1021	(2)
DAC-100	DAC1022	(2)
DAC-1408	DAC0806	(2)
DAC-1408	DAC0807	(2)
DAC-1408	DAC0808	(2)
DAC-312	DAC1266	
DAC-8012	DAC1208	(2)
DAC-8012	DAC1209	
DAC-8012	DAC1210	
DAC-888	DAC-0830	(2)
DAC-888	DAC0831	(2)
DAC-888	DAC0832	(2)
MUX-08E	LF13508	
MUX-24E	LF13509	
OP-05	LM607	(2)
OP-07	LM607	(1)
OP-15	LF411	(1)
OP-215	LF412	(1)
OP-77	LM607	(1)
PM-108	LM108	
PM-108A	LM108A	
PM-139	LM139	
PM-139A	LM139A	
PM-155	LF155	
PM-155A	LF155A	
PM-156	LF156	
PM-156A	LF156A	
PM-157	LF157	
PM-157A	LF157A	
PM-208	LM208	
PM-208A	LM208A	
PM-2108A	LH2108A	
PM-308	LM308	
PM-308A	LM308A	
PM-339A	LM339A	
PM-355	LF355	
PM-355A	LF355A	
PM-356	LF356	
PM-357	LF357	
PM-357A	LF357A	
PM-725	LM725	
PM-741	LM741	
PM-747	LM747	
PM-7533	DAC1020	
PM-7533	DAC1021	
PM-7533	DAC1022	
PM-7541	DAC1218	
PM-7541	DAC1219	
PM356A	LF356A	
PM420	LM124	(1)

REF-01CJ	LM368-1.0	(1)
REF-02	LM368-5.0	(3)
REF-43	LM368-2.5	(1)
REF-01	LM369	(1)
SW-06B	LF11333	
SW-06F	LF13333	
SW-06G	LF13333	
SW-201B	LF11201	
SW-201F	LF13201	
SW-201G	LF13201	
SW-202B	LF11202	
SW-202F	LF13202	
SW-202G	LF13202	

RAYTHEON	**NATIONAL**	
LP365	LP365	
RC1458	LM1458	
RC1558	LM1558	
RC714	LM607	(1)
RC741	LM741	
RC747	LM747	
REF-01	LM369	(1)
REF-01T	LM368	(1)
REF-02	LM368-5.0	(3)
REF-03	LM368-5.0	(1)

SAMSUNG	**NATIONAL**
KA3524	LM3524D
KA431	LM431
KA78S40	LM78S40
LM741	LM741
MC78LXX	LM78LXX
MC78MXX	LM78MXX
MC78XX	LM78XX
MC79MXX	LM79MXX
MC79XX	LM79XX

SGS-THOMSON	**NATIONAL**	
L123CB	LM723CN	(1)
L293	LM18293	
L4940	LM2940T-5.0	(2)
L4941	LM2940T-5.0	(2)
L4960	LM2579	(2)
L4962	LM2579	(2)
L78MXXCV	LM341P-XX	(2)
L78S05CV	LM323K-5.0	(1)
L78XXACV	LM340AT-XX	
L78XXCT	LM78XXCK	
L78XXCV	LM78XXCT	
L790XXACV	LM320T-XX	
L79XXCT	LM79XXCK	
L79XXCV	LM79XXCT	
LF198	LF198A	(1)
LF298	LF298	
LF398	LF398A	(1)
LM105H	LM105H	(1)
LM109K	LM109K STEEL	(1)
LM117H	LM117H	(1)
LM117K	LF117K	(1)
LM117K	LF117K STEEL	(1)
LM123K	LF123K STEEL	(1)
LM134	LM134	
LM135	LM135	
LM137H	LM137H	(1)
LM137K	LM137K STEEL	(1)
LM138K	LM138K STEEL	(1)
LM234	LM234	
LM235	LM235	
LM2930A	LM2930T-5.0	(1)
LM2931A	LM2931AT-5.0	
LM2935	LM2935	
LM305H	LM305H	(1)
LM309H	LM309H	(1)
LM309K	LM309K STEEL	(1)
LM317H	LM317H	(1)
LM317K	LM317K	(1)
LM317K	LM317K STEEL	(1)
LM317T	LM317T	(1)
LM323K	LM323K STEEL	(1)
LM334	LM334	
LM335	LM335	
LM335A	LM335A	
LM337H	LM337H	(1)
LM337K	LM337K STEEL	(1)
LM338K	LM338K STEEL	(1)
LM748	LM748	
LM7805MK	LM140K-5.0	(1)
SG1524	LM1524D	(1)
SG1525A	LM1525A	(1)
SG1527A	LM1527A	(1)
SG2524	LM2524D	(1)
SG3524	LM3524D	(1)
SG3525A	LM3525A	(1)
SG3527A	LM3527A	(1)
TBC0136	LM336	
TCA3089	LM3089	
TDA2310	LM381	
μA741	LM741	
μA748	LM748	
μA7805CK	LM7805KC	(1)
μA7812CK	LM7812KC	(1)
μA7812MK	LM140K-12	(1)
μA7815CK	LM7815KC	(1)
μA7815MK	LM140K-15	(1)
μA7905CK	LM7905KC	(1)
μA7905MK	LM120K-5.0	(1)
μA7912CK	LM7912KC	(1)
μA7912MK	LM120K-12	(1)
μA7915CK	LM7915KC	(1)
μA7915MK	LM120K-15	(1)

SIEMENS	**NATIONAL**	
TCA365	LH0101	(1)

SIGNETICS	**NATIONAL**	
78LXXACS	LM78LXXACZ	(1)
78LXXADB	LM78XXACH	(1)
78LXXCDB	LM78LXXCH	(1)
78LXXCS	LM78LXXACZ	(1)
78XXCU	LM78XXCT	(1)
78XXDA	LM78XXCK	(1)
79XXCU	LM79XXCT	(1)
79XXDA	LM79XXCK	(1)
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
DAC-08	DAC0800	
DAC-08	DAC0801	
DAC-08	DAC0802	
LF198	LF198	
LF298	LF298	
LF398	LF398	
LM109DB	LM109H	(1)
LM309DA	LM309K	(1)
LM309DB	LM309H	(1)
LM340XXDA	LM340KXX	
LM340XXLL	LM340T-XX	
MC1408	DAC0806	
MC1408	DAC0807	
MC1408	DAC0808	
MC1496N	LM1496N	
MC1508	DAC0808	
MC1596K	LM1596H	
NE4558	LM833	(2)
NE4558D	LM833CM	(2)
NE4558N	LM833CN	(2)
NE5034	ADC0841	(2)
NE5118	DAC0830	(2)
NE529	LM361	(1)
NE532	LM358	(1)
NE5410	DAC1020	(2)
NE5532	LM833	
NE5532N	LM833CN	(2)
NE5532P	LM833CN	(2)
NE555N	LM555CN	
SA532	LM2904	(1)
SA534	LM2902	(1)
SE5118	DAC0830	(2)
SE529	LM161	(1)
SE532	LM158	(1)
SE5410	DAC1020	(2)
SE567	LM567	(2)
μA723CF	LM723CJ	(1)
μA723CL	LM723CH	(1)
μA723CN	LM723CN	(1)
μA723F	LM723J	(1)
μA723L	LM723H	(1)
μA741	LM741	
μA747	LM747	

SILICON GENERAL	**NATIONAL**	
SG101	LM101A	
SG101A	LM101A	
SG104	LM104	
SG105	LM105	
SG107	LM107	
SG109	LM109	
SG117	LM117	
SG1173	LM675	(2)
SG117A	LM117A	
SG117MV	LM117HV	
SG120-XX	LM120-XX	
SG123	LM123	
SG123A	LM123A	
SG124	LM124	
SG137	LM137	
SG138	LM138	
SG138A	LM138A	
SG140-XX	LM140-XX	
SG1436	LM343	(1)
SG150	LM150	
SG150A	LM150A	
SG1524	LM1524D	(1)
SG1524B	LM1524D	
SG1525A	LM1525A	(1)
SG1527A	LM1527A	(1)
SG1536	LM143	(1)
SG201	LM201A	
SG201A	LM201A	
SG204	LM204	
SG205	LM205	
SG207	LM207	
SG224	LM224	
SG2524	LM2524D	(1)
SG2524B	LM2524D	
SG301A	LM301A	
SG304	LM304	
SG305	LM305	
SG307	LM307	
SG309	LM309	
SG317	LM317	

SG3173	LM675	(2)
SG317A	LM317A	
SG317MV	LM317HV	
SG320-XX	LM320-XX	
SG323	LM323	
SG323A	LM323A	
SG324	LM324	
SG337	LM337	
SG338	LM338	
SG338A	LM338A	
SG340-XX	LM340-XX	
SG350	LM350	
SG350A	LM350A	
SG3524	LM3524D	(1)
SG3524B	LM3524D	
SG3525A	LM3525A	(1)
SG3527A	LM3527A	(1)
SG723	LM723	
SG723C	LM723C	
SG741	LM741	
SG78XX	LM140-XX	
SG78XXA	LM140A-XX	(2)
SG78XXAC	LM340A-XX	(2)
SG78XXC	LM78XXC	
SG79XX	LM120-XX	
SG79XXA	LM120-XX	(2)
SG79XXAC	LM320-XX	(2)
SG79XXC	LM79XXC	

SILICONIX	**NATIONAL**	
DG201	LF13201	
DG202	LF13202	
DG211	LF13201	
DG212	LF13202	
DG508	LF13508	
DG509	LF13509	

SPRAGUE	**NATIONAL**	
SG3525A	LM3525A	
SG3527A	LM3527A	
UDN2993B	LM18293	(3)

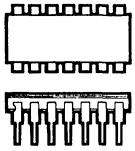
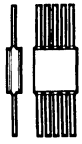
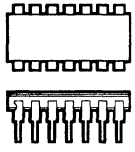
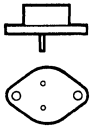
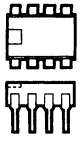
TELEDYNE	**NATIONAL**
TP0032	LH0032
TP0033	LH0033

TEXAS INSTRUMENTS	**NATIONAL**	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
ADC0808	ADC0808	
ADC0809	ADC0809	
ADC0831	ADC0831	
ADC0832	ADC0832	
ADC0834	ADC0834	
ADC0838	ADC0838	
LM317KC	LM317T	(1)
RC4558	LM833	
RC4588D	LM833CM	
RV4558D	LM833CM	
TL071	LF351	(1)
TL071A	LF411	(1)
TL071B	LF411	(1)
TL072	LF353	(1)
TL072A	LF412	(1)
TL072B	LF412	(1)
TL074	LF347	(1)
TL074A	LF347B	(1)
TL081	TL081	(1)
TL081A	LF411	(1)
TL081B	LF411	(1)
TL082	TL082	(1)
TL082A	LF412	(1)
TL082B	LF412	(1)
TL084	LF347	(1)
TL084A	LF347B	(1)
TL087	LF411A	(1)
TL088	LF411A	(1)
TL288	LF412A	(1)
TL487N	LM3915N	(2)
TL489N	LM3914N	(2)
TL490N	LM3914N	(2)
TL491N	LM3914N	(2)
TL520	ADC0848	(2)
TL521	ADC0848	(2)
TL522	ADC0848	(2)
TL530	ADC0830B	
TL531	ADC0830C	
TL532	ADC0829B	
TLC532A	ADC0829B	(2)
TL533	ADC0829C	
TLC533A	ADC0829C	(2)
TLC274AC	LMC660AI	(2)
TLC274AI	LMC660AI	(2)
TLC274AM	LMC660AM	(2)
TLC274BC	LMC660AI	(2)
TLC274BI	LMC660AI	(2)
TLC274BM	LMC660AM	(2)
TLC274C	LMC660C	(2)
TLC2741	LMC660AI	(2)
TLC274M	LMC660AM	(2)
TLC540	ADC0811	(2)
TLC541	ADC0811	
TLC549	ADC0831	(2)
TLO61	LF441	(1)
TLO61A	LF441	(1)
TLO61B	LF441A	(1)
TLO62	LF442	(1)
TLO62A	LF442A	(1)
TLO62B	LF442	(1)
TLO64	LF444	(1)
TLO64A	LF444A	(1)
μA709	LM709	
μA723CJ	LM723CJ	
μA723CN	LM723CN	
μA723MJ	LM723J	
μA733CN	LM733CN	
μA741	LM741	
μA747	LM747	
μA78LXXACL	LM78LXXACZ	
μA78MXXCKD	LM78MXXCP	
μA78XXCKC	LM78XXCT	
μA79MXXCKD	LM79MXXCP	
μA79XXCKC	LM79XXCT	

TOSHIBA	**NATIONAL**	
TA7504	LM741	
TA75339	LM2901	(1)
TA75358	LM2904	(1)
TA75393	LM2903	(1)
TA75902	LM2902	(1)

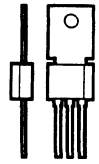
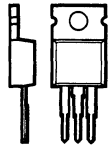
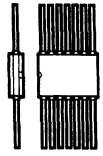
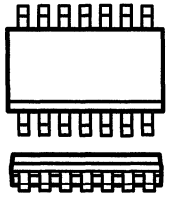
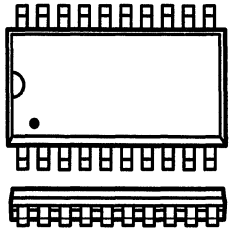
UNITRODE	**NATIONAL**	
L293	LM18293	
UC117	LM117	
UC137	LM137	
UC150	LM150	
UC1524	LM1524D	(1)
UC1524A	LM1524D	(2)
UC1525A	LM1525A	
UC1527A	LM1527A	
UC2524	LM2524D	(1)
UC2524A	LM2524D	(2)
UC317	LM317	
UC337	LM337	
UC350	LM350	
UC3524	LM3524D	(1)
UC3524A	LM3524D	(2)
UC3525A	LM3525A	
UC3527A	LM3527A	
UC494	LM494	(2)
UC78XXACK	LM340AK-XX	(2)
UC78XXAK	LM140AK-XX	(2)
UC78XXCK	LM340K-XX	
UC78XXCK	LM78XXCK	
UC78XXK	LM140K-XX	
UC79XXACK	LM320K-XX	(2)
UC79XXAK	LM120K-XX	(2)
UC79XXCK	LM79XXCK	
UC79XXK	LM120K-XX	(1)

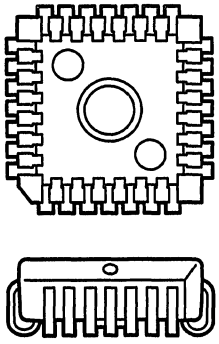
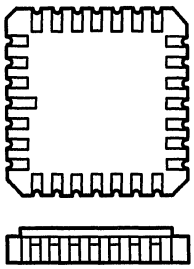
Industry Package Cross-Reference Guide

	NSC	NSC μA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
 4/16 Lead Glass/Metal DIP	D	D	I	L		D	C	D	D
 Glass/Metal Flat Pack	F	F	Q	F	F, S	K	F		Q
 TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	S*, V1**		A	H
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J		G	D	J, J8
 TO-3 (Steel)	K			KS					K
TO-3 (Aluminum)	KC	K	DA	K	K				
 8-, 14- and 16-Lead Plastic DIP	N	T, P	V, A, B	P	P, N	E	P	C	N, N8

*With dual-in-line formed leads

**With radically formed leads

		NSC	NSC μA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
	TO-202 (D-40, Durawatt)	P					KD			
	TO-220 3- & 5-Lead	T	U	U		KC		T	H	T
	TO-220 11-, 15- & 23-Lead	T								
	Low Temperature Glass Hermetic Flat Pack	W	F		F	W				
	TO-92 (Plastic)	Z	W	S	P	LP			H	Z
	SO (Narrow Body)	M	S	D	D	D	M	MP	G	S
	SO (Wide Body)	WM				DW				

	NSC	NSC μA	Signetics	Motorola	TI	RCA	Hitachi	NEC	LTC
 PCC	V	Q	A	FN	FN	Q	CP	L	
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	BJ	CG	K	

Section 1

Continuous Voltage Regulators

Section 1 Contents

Section 1 Contents (Continued)

National Semiconductor

Voltage Regulators Definition of Terms

Current-Limit Sense Voltage: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

Input Voltage Range: The range of dc input voltages over which the regulator will operate within specifications.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Output-Input Voltage Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Output Noise Voltage: The RMS ac voltage at the output with constant load and no inut ripple, measured over a specified frequency range.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current: That par of input current to the regulator that is not delivered to the load.

Ripply Rejection: The line regulation for ac inupt signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

Standby Current Drain: That part of the operating current of the regulator which does not contribute to the load current. (See Quiescent Current)

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Thermal Regulation: Percentage change in output voltage for a given change in power dissipation over a specified time period.

National Semiconductor

Continuous Voltage Regulators Selection Guide

Voltage Regulators

Adjustable Positive Voltage Regulators

Amps	Device	Output Voltage	Package
10.0	LM196K	1.25V–15V	TO-3
	LM396K	1.25V–15V	TO-3
5.0	†LM138K	1.2V–32V	TO-3
	LM338K, T	1.2V–32V	TO-3, TO-220
3.0	†LM150K	1.2V–33V	TO-3
	LM350K, T, AT	1.2V–33V	TO-3, TO-220
1.5	†LM117K	1.2V–37V	TO-3
	†LM117HVK	1.2V–57V	TO-3
	LM317K, T, AK, AT	1.2V–37V	TO-3, TO-220
	LM317HVK	1.2V–57V	TO-3
1.0	LM2941T,CT	5V–20V	TO-220
	LM78GCT*	5V–30V	TO-220 (4 Pin)
0.5	†LM117H	1.2V–37V	TO-39
	†LM117HVH	1.2V–57V	TO-39
	LM317H	1.2V–57V	TO-39
	LM317HVH	1.2V–37V	TO-39
	LM317MP	1.2V–37V	TO-202
	LM78MGCT*	5V–30V	TO-220 (4-Pin)
0.2	†LH0075G, CG	0–27V	TO-8
0.1	LM317LZ, M	1.2V–37V	TO-92, SO-8
	LM2931CT	3.0V–24V	TO-220, 5-LEAD
	†LP2951CN, J, H, M	1.24V–29V	DIP, CERDIP, HEADER, SO-8

*These products were formerly manufactured by Fairchild Semiconductor Corporation. The prefixes have been changed from μA to LM and may be found with the former prefix as well as the latter.

†Military qualified device. More more information, consult the Military/Aerospace Selection Guide.

Voltage Regulators (Continued)

Adjustable Negative Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	LM133K	−1.2V – −32V	TO-3
	LM333K, T	−1.2V – −32V	TO-3, TO-220
1.5	†LM137K	−1.2V – −37V	TO-3
	†LM137HVK	−1.2V – −47V	TO-3
	LM337K, T	−1.2V – −37V	TO-3, TO-220
	LM337HVK	−1.2V – −47V	TO-3
1.0	LM79GCT*	−2.2V– −30V	TO-220 (4-Pin)
0.5	†LM137H	−1.2V – −37V	TO-39
	†LM137HVH	−1.2V – −47V	TO-39
	LM337H	−1.2V – −37V	TO-39
	LM337HVH	−1.2V – −47V	TO-39
	LM337MP	−1.2V – −37V	TO-202
	LM79MGCT*	−2.2V– −30V	TO-224 (4 Pin)
0.2	†LH0076G, CG	0–27V	TO-8
0.1	LM337LZ, M	−1.2V – −37V	TO-92, SO-8

Adjustable Positive/Negative Voltage Regulator

Amps	Device	Output Voltage	Package
±0.1	LH7001	±1.2V to ±37V	DIP, TO-5

Fixed Positive Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	†LM123K	5V	TO-3
	LM323K, AK	5V	TO-3
1.0	†LM109K	5V	TO-3
	†LM140AK	5V, 12V, 15V	TO-3
	†LM140K	5V, 12V, 15V	TO-3
	†LM2940T	5V, 8V, 10V, 12V	TO-220
	LM2940CT	5V, 12V, 15V	TO-220
	LM309K	5V	TO-3
	LM340AK, T	5V, 12V, 15V	TO-3, TO-220
	LM340K, T	5V, 12V, 15V	TO-3, TO-220
	LM78xxCK, T**	5V, 6V, 8V, 12V, 15V, 18V, 24V	TO-3, TO-220
0.5	LM2984CT	5V, 12V, 15V	TO-220, TO-202
	LM341T, P	5V, 12V, 15V	TO-220, TO-202
	LM78MxxCT, H**	5V, 6V, 8V, 12V, 15V, 24V	TO-220, TO-39
0.2	†LM109H	5V	TO-39
	LM309H	5V	TO-39
	LM342P	5V, 12V, 15V	TO-202
0.15	LM2930T	5V, 8V	TO-220
0.1	†LM140LAH	5V, 12V, 15V	TO-39
	LM2931Z, T	5V	TO-92, TO-220
	LM340LZ, H	5V, 12V, 15V	TO-92, TO-39
	LM78LxxACZ, H, M**	5V, 6.2V, 8.2V, 9V, 12V, 15V	TO-92, TO-39, SO-8
	LP2950CZ	5V	TO-92
0.05	LM2936Z	5V	TO-92

*The LM320 has better electrical characteristics than the LM79xx.

LM100 Series +55°C to +150°C

LM300 Series 0°C to +125°C

**These products were formerly manufactured by Fairchild Semiconductor Corporation. The prefixes have been changed from μA to LM and may be found with the former prefix as well as the latter.

†Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

Voltage Regulators (Continued)

Fixed Negative Voltage Regulators

Amps	Device	Output Voltage	Package
3.0	†LM145K	−5V, −5.2V	TO-3
	LM345K	−5V, −5.2V	TO-3
1.5	†LM120K	−5V, −12V, −15V	TO-3
	LM320K, T	−5V, −12V, −15V	TO-3, TO-220
	LM79xxCT, K**	−5V, −8V, −12V, −15V	TO-220, TO-3
0.5	LM320MP	−5V, −12V, −15V	TO-220
	LM79MxxCT, H**	−5V, −8V, −12V, −15V	TO-220, TO-39
0.2	†LM120H	−5V, −12V, −15V	TO-39
	LM320H	−5V, −12V, −15V	TO-39
0.1	LM320LZ	−5V, −12V, −15V	TO-92
	LM79LxxACZ, M	−5V, −12V, −15V	TO-92, SO-8

Low Dropout Regulators

Amps	Device	Output Voltage	Package
0.050	LM2936Z	5V	TO-92
0.100	LM2931T, Z	5V, ADJ	TO-220, TO-92
	LP2950CZ	5V	TO-92
	LP2951N, J, H	ADJ	DIP, CERDIP, HEADER
0.150	LM2930T	5V, 8V	TO-220
0.500	LM2984CT	TRIPLE 5V + WATCHDOG	TO-220, 11-LEAD
0.750	LM2925T	5V WITH DELAYED RESET	TO-220, 5-LEAD
	LM2935T	DUAL 5V	TO-220, 5-LEAD
1.0	†LM2940T	5V, 8V, 10V, 12V	TO-220
	LM2940CT	5V, 12V, 15V	TO-220
	LM2941T	Adjustable (5V to 20V)	TO-220
	LM2941CT	Adjustable (5V to 20V)	TO-220

Shunt Regulators

Amps	Device	Output Voltage	Package
0.15	LM431ACZ, M	2.5V–36V	TO-92, SO-8

Building Block Regulators

Device	Title	Package
†LM104/204/304	Negative Regulator	TO-39
†LM105/205/305	Voltage Regulator (Positive)	TO-39
LM376	Voltage Regulator (Positive)	8-Pin Plastic DIP
†LM723	Voltage Regulator	14-Pin DIP, TO-39

**These products were formerly manufactured by Fairchild Semiconductor Corporation. The prefixes have been changed from μA to LM and may be found with the former prefix as well as the latter.

†Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

National Semiconductor

LH0075 Positive Precision Programmable Regulator

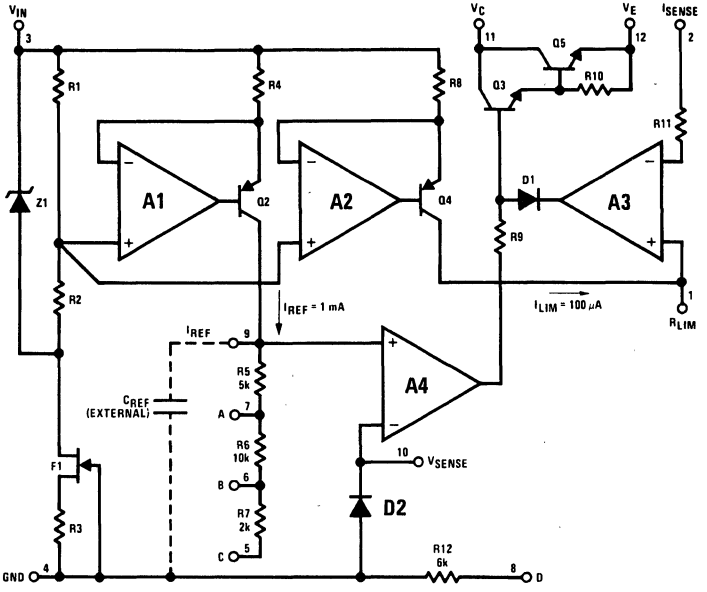
General Description

The LH0075 is a precision programmable regulator for positive voltages. Regulated output voltages from 0 to 27V may be obtained using one external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (5V, 6V, 10V, 12V and 15V). The output current limit is adjustable from 0 to 200 mA using two external resistors. These features provide an inventory of precision regulated values in one package.

Features

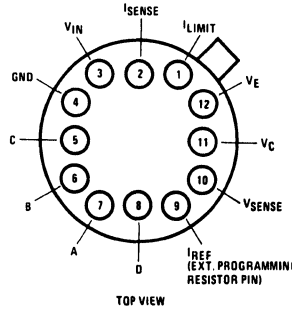
- Output adjustable to 0V
- Line regulation typically 0.008%/V
- Load regulation typically 0.075%
- Remote voltage sensing
- Ripple rejection of 80 dB
- Adjustable precision current limit
- Output currents to 200 mA
- Popular voltages available without external resistors

Schematic Diagram



Connection Diagram

TO-8 Metal Can Package

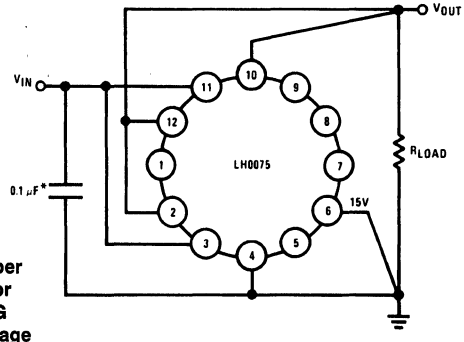


Case is electrically isolated

Order Number LH0075G or LH0075CG
See NS Package Number H12B

Typical Applications

Precision 15V Reference Supply without Current Limit



TL/H/5549–1

*Needed if device is far from filter capacitors

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

Input Voltage	32V
Output Voltage	27V
Output Current	200 mA
Power Dissipation	See Curve

Operating Temperature Range	
LH0075	−55°C to +125°C
LH0075C	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics Conditions for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0075			LH0075C			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_A = 25°C$		0.008	0.02		0.008	0.04	%/V
Load Regulation	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA $V_{OUT} \leq 5.0V$ $V_{OUT} \geq 5.0V$		 2.5 0.055	 7.5 0.15		 2.5 0.055	 15 0.3	 mV %
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = 15V$	0.998	1.000	1.002	0.995	1.00	1.005	mA
Load Regulation	1 mA < I_{LOAD} < 200 mA $V_{OUT} \leq 5.0V$ $V_{OUT} \geq 5.0V$		 4.0 0.075	 15 0.3		 4.0 0.075	 25 0.5	 mV %
Reference Current Drift ($\Delta I_{REF}/\Delta$Temp.)	$V_{IN} = 15V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		27	0		27	V
Minimum Input Voltage		10			10			V
Input-Output Differential Voltage	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA		3.0	3.2		3.0	3.5	V
Quiescent Supply Current	$V_{IN} = 15V$		6.0	8.0		6.5	10	mA
Ripple Rejection	$V_{OUT} = 5.0V$, f = 120 Hz $C_{REF} = 2.2$ μF		65 80			65 80		dB dB
Output Voltage Tolerance	$T_A = 25°C$ (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta$Temp.)	(Note 3)		0.003			0.003		%/°C

Note 1: Minimum load current is established by I_{LIM}, the current from Q4 (see schematic). I_{LIM} goes directly to the output if the current limit feature is used.

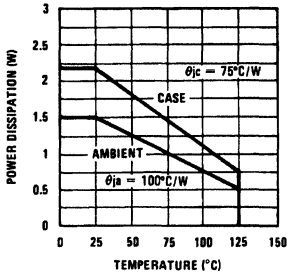
Note 2: For $V_{IN} = 15V$ and V_{OUT} obtained by using R5, R6, R7, and R12 individually.

Note 3: Total change over specified temperature range.

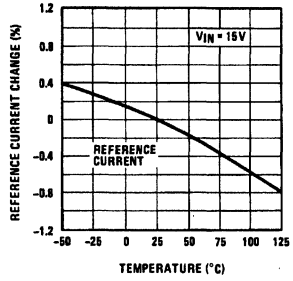
Note 4: Refer to RETS075G drawing for military specifications on the LN0075.

Typical Performance Characteristics

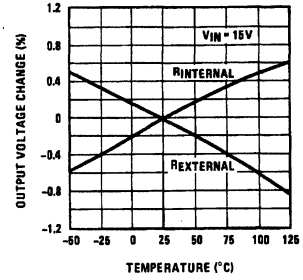
Maximum Power Dissipation



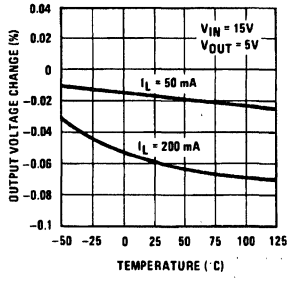
Reference Current Change with Temperature (Normalized)



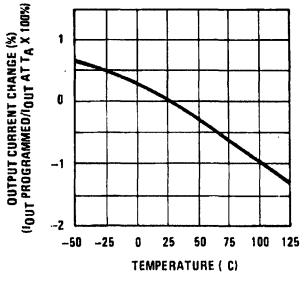
Temperature Stability



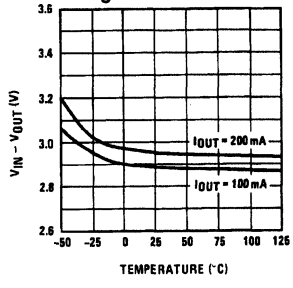
Output Voltage Change with Temperature (Normalized)



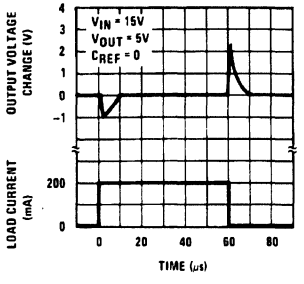
Current Limit



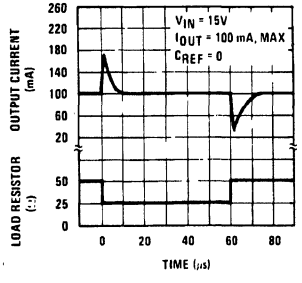
Input-Output Differential Voltage



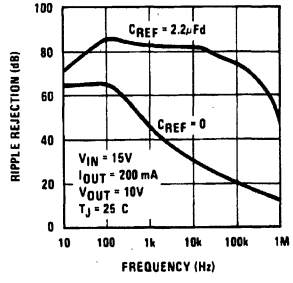
Load Transient Response (Voltage Mode)



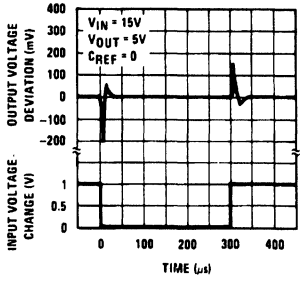
Load Transient Response (Current Mode)



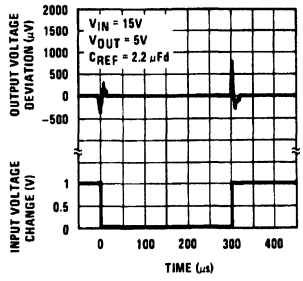
Ripple Rejection



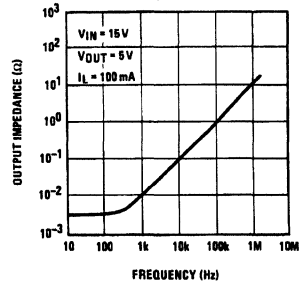
Line Transient Response



Line Transient Response



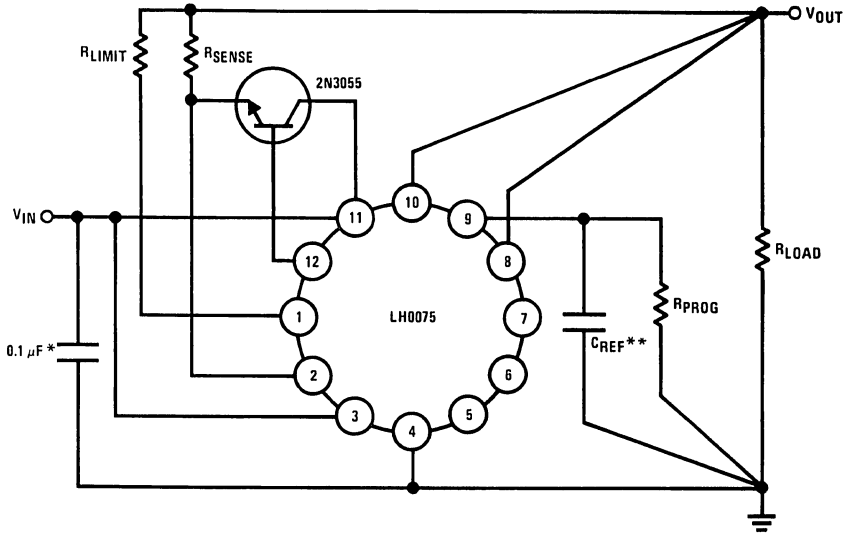
Output Impedance



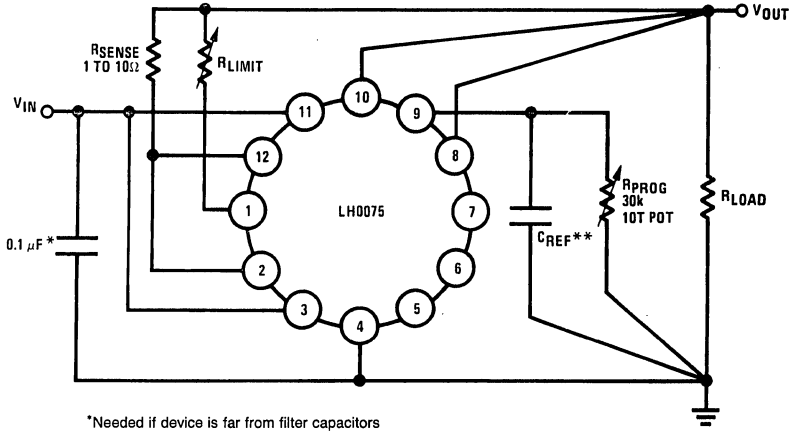
TL/H/5549–2

Typical Applications (Continued)

2A Regulator with Current Limit



Variable Voltage Reference with Current Limit



*Needed if device is far from filter capacitors
**Optional—improves transient response

TL/H/5549–3

$$R_{PROG} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}} \qquad I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\ \mu A$$

$$I_{OUT} \leq 200\ \text{mA}$$

Applications Information

The LH0075 does not require capacitors for stable operation, but an input bypass is recommended if device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for almost all applications.

Applications Information (Continued)

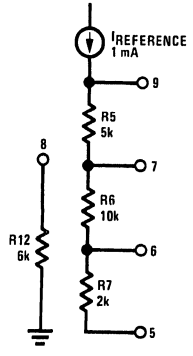
DESCRIPTION OF OPTIONS

Ripple Rejection Compensation. (Increases Ripple Rejection Typically to 80 dB)

The ripple rejection may be improved by connecting an external capacitor between pin 9 and ground. (The typical performance curves show the rejection with a capacitance of 2.2 μFd.)

Internal Voltage Programming

The LM0075 provides various precision output voltages simply by using one or more of the internal resistors. A particular voltage may be obtained by external connections as shown in Table I.



R5, R6, R7 and R12 are precision-trimmed to 0.1%.

TL/H/5549–4

FIGURE 1

External Voltage Programming

An external resistance can be connected between pin 9 and ground to obtain any voltage from 0 to 27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{Desired}}{1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −65 ppm/°C. Choosing a resistive material with a temperature coefficient of 65 ppm/°C will compensate the negative temperature coefficient, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is Nichrome, which has a typical temperature coefficient of 80 ppm/°C.

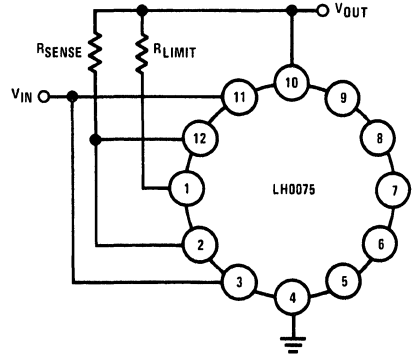
Since a current source is used as a reference, this makes remote voltage programming possible.

Current Limit Programming

The maximum current output of the device may be limited by adding two external resistors as shown below. The resistor values are easily calculated with the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1\right] \times 100\mu A$$

where $R_{SENSE} = 1$ to 10Ω



TL/H/5549–5

FIGURE 2. Current Limit Programmng

This programmable current limit feature can be extended to make the LH0075 a programmable constant current source. This can be done by leaving pin 9 open and setting R_{LIMIT} and R_{SENSE} as desired.

For applications where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it goes directly to the output of the LH0075. If the total current drawn from the output is less than the minimum, the output will rise.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} must be placed as close to the output of the LH0075 as possible, but R_{LIMIT} can be a fixed resistor or potentiometer located remotely from the device.

TABLE I. Connection Scheme for Internal Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9
5			Gnd		
6				●	●
8	●	●	●		●
10		Gnd	●		●
12	Gnd		●		●
15	●	Gnd		●	
18			●		●

National Semiconductor

LH0076 Negative Precision Programmable Regulator

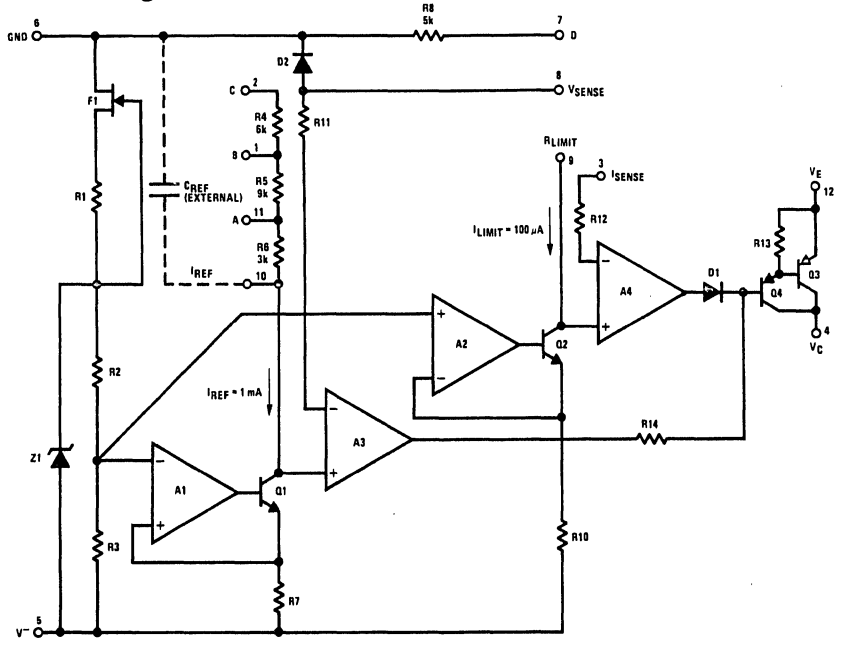
General Description

The LH0076 is a precision programmable regulator for negative voltages. Regulated output voltages from 0 to −27V may be obtained by using 1 external resistor. Also available without any external components are several fixed regulated voltages with accuracies to 0.1% (−3V, −5V, −6V, −8V, −9V, −12V, −15V and −18V). The output current limit is adjustable from 0 to 200 mA using 2 external resistors. These features provide an inventory of precision regulated values in 1 package.

Features

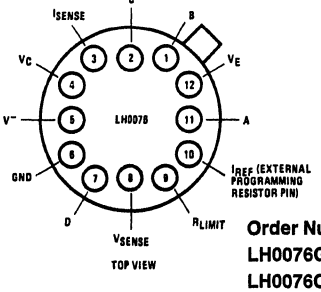
- Line regulation typically 0.005%/V
- Load regulation typically 0.02%
- Remote voltage sensing
- Ripple rejection–70 dB
- Output Adjustable to 0V
- Adjustable precision current limit
- Output current to 200 mA

Schematic Diagram



Connection Diagram

Metal Can Package

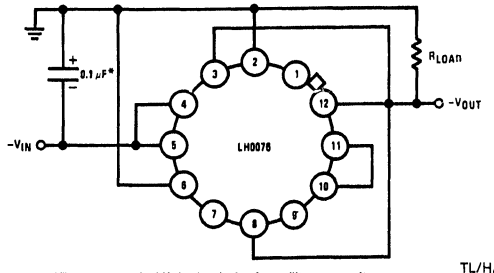


Case is electrically isolated

Order Number
LH0076G
LH0076CG
See NS Package H12B

Typical Applications

Precision −15V Reference Supply without Current Limit



*Recommended if device is far from filter capacitors

TL/H/5548–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Input Voltage	−32V
Output Voltage	−27V
Output Current	200 mA
Power Dissipation	See Curve
Operating Temperature Range	
LH0076	−55°C to +125°C
LH0076C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	300°C

Electrical Characteristics Conditions are for $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted

Parameter	Conditions	LH0076			LH0076C			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_A = 25°C$		0.005	0.02		0.005	0.04	%/V
Load Regulation	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA							
	$V_{OUT} \geq -5.0V$			7.5			15	mV
	$V_{OUT} \leq -5.0V$		0.02	0.15		0.02	0.3	%
Reference Current (I_{REF})	$T_A = 25°C$, $V_{IN} = -15V$	0.998	1.000	1.002	0.995	1.000	1.005	mA
Reference Current Drift ($\Delta I_{REF}/\Delta$Temp.)	$V_{IN} = -15V$		−0.0065			−0.0065		%/°C
Minimum Load Current (I_{LIM})	(Note 1)	98	100	102	95	100	105	μA
Output Voltage Range		0		−27	0		−27	V
Minimum Input Voltage		−10			−10			V
Input-Output Differential Voltage	$T_A = 25°C$, 1 mA < I_{LOAD} < 200 mA		2.7	3.2		2.7	3.5	V
Quiescent Supply Current	$V_{IN} = -15V$		11	15		11	15	mA
Ripple Rejection	$V_{OUT} = 5.0V$, f = 120 Hz		70			70		dB
Output Voltage Tolerance	$T_A = 25°C$, (Note 2)		±0.1	±0.5		±0.1	±1.0	%
Output Voltage Change with Temperature ($\Delta V_{OUT}/\Delta$Temp.)	(Note 3)		0.003			0.003		%/°C

Note 1: Minimum load current is established by I_{LIM}, the current to Q2 (see schematic.) I_{LIM} draws directly from the output if the current limit feature is used.

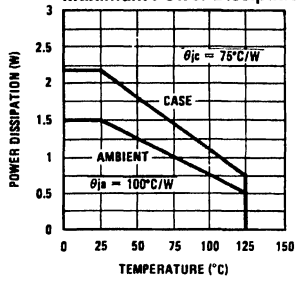
Note 2: For $V_{IN} = 15V$ and V_{OUT} obtained by using R4, R5, R6, and R8 individually.

Note 3: Total change over specified temperature range.

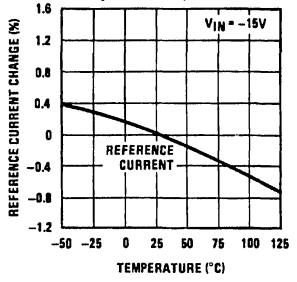
Note 4: Refer to RETS0076G for military specifications on the LH0076.

Typical Performance Characteristics

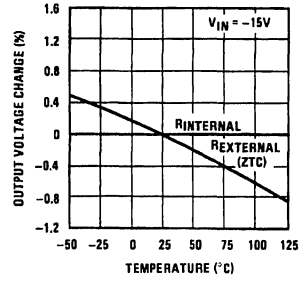
Maximum Power Dissipation



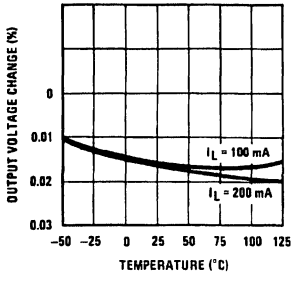
Reference Current Change with Temperature (Normalized)



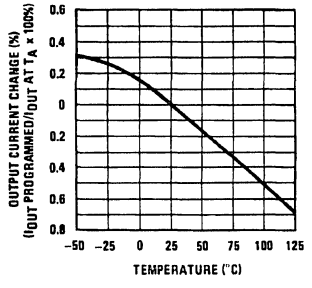
Temperature Stability



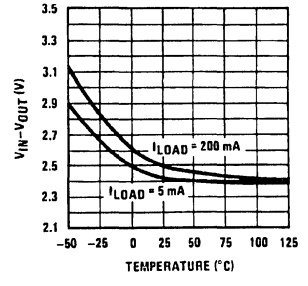
Output Voltage Change with Temperature (Normalized)



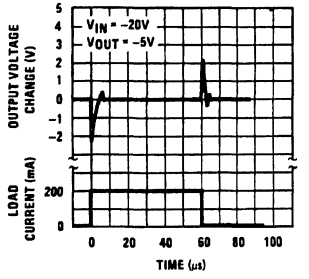
Current Limit



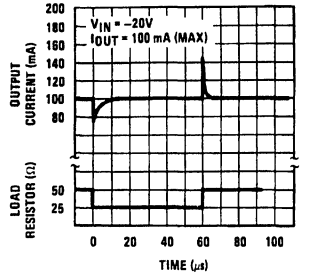
Input-Output Differential Voltage



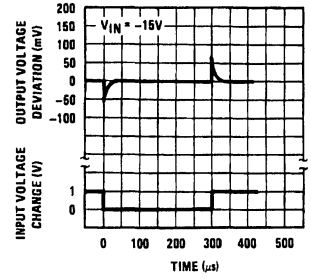
Load Transient Response (Voltage Mode)



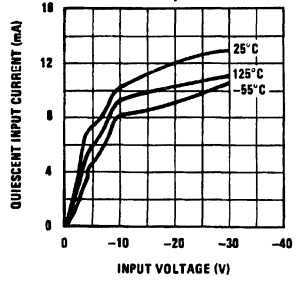
Load Transient Response (Current Mode)



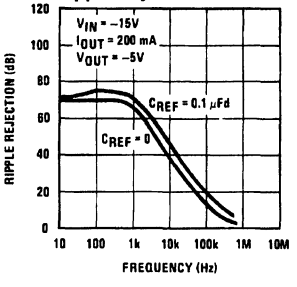
Line Transient Response



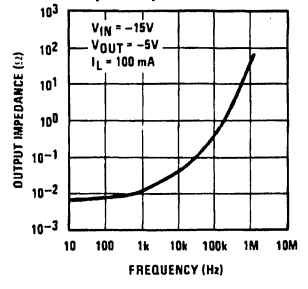
Quiescent Input Current



Ripple Rejection



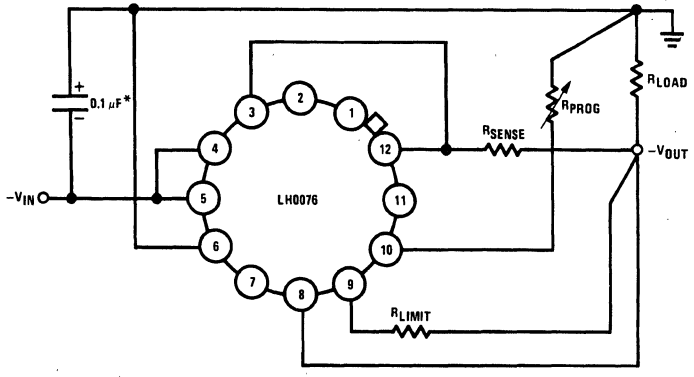
Output Impedance



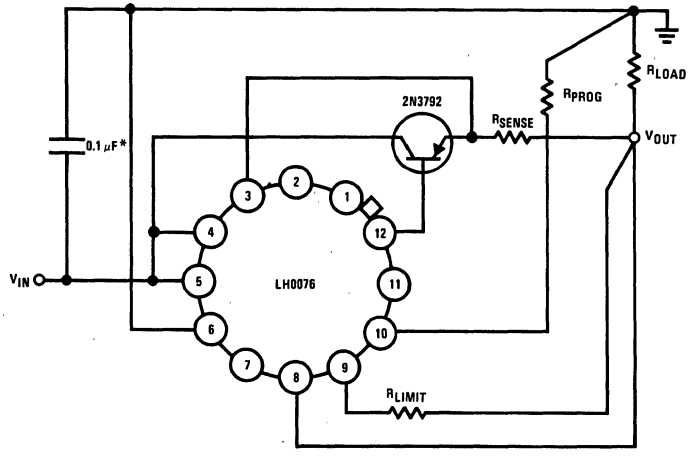
TL/H/5548–3

Typical Applications (Continued)

Variable Voltage Reference with Current Limit



2-Amp Regulator with Current Limit



TL/H/5548–4

*Recommended if device is far from filter capacitors

Application Information

The LH0076 does not require external capacitors for stable operation. However, an input bypass is recommended if the device is far from filter capacitors. A 0.1 μF for input bypassing should be adequate for most applications.

DESCRIPTION OF OPTIONS

External Voltage Programming

An external resistance can be connected between pin 10 and ground to obtain any voltage from 0 to −27V using the following equation:

$$R_{EXT} = \frac{V_{OUT}\ \text{desired}}{-1\ \text{mA}}$$

The reference current (I_{REF}) has a typical temperature coefficient of −60 ppm/°C. Choosing a resistive material with a temperature coefficient of 60 ppm/°C will compensate the negative tempco of the reference current, resulting in an output voltage with minimal change over the operating temperature range. Example of a good resistive material is nichrome, which has a typical tempco of 80 ppm/°C. Nichrome is the resistive material used in the LH0076, resulting in output voltage drift of 20 ppm/°C typically.

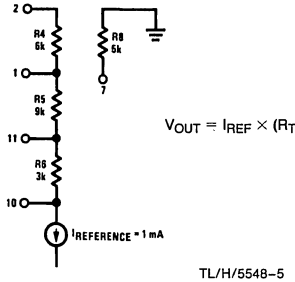
Application Information (Continued)

Because a current source is used as a reference, remote voltage programming is possible.

Internal Voltage Programming

The LH0076 provides various precision output voltages simply by using 1 or more of the internal programming resistors. These voltages may be obtained by using the connections as shown in Table 1.

R_{TOTAL} is the total resistance between pin 10 and ground



$V_{OUT} = I_{REF} \times (R_{TOTAL})$

TL/H/5548–5

R4, R5, R6 and R8 are precision trimmed to 0.1%

FIGURE 1

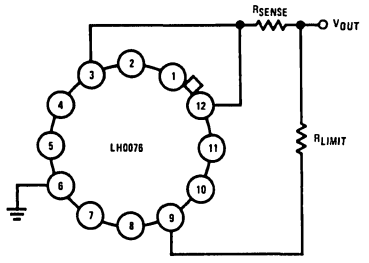
Current Limit Programming

The maximum current output of the device may be limited by adding 2 external resistors as shown in *Figure 2.* The resistor values are calculated using the following equation:

$$I_{OUT(MAX)} = \left[\frac{R_{LIMIT}}{R_{SENSE}} + 1 \right] \times 100\mu A$$

where $R_{SENSE} = 1$ to 10Ω

This programming current limit feature can be extended to make the LH0076 a programmable current sink. This can be done by leaving pin 10 open and setting R_{LIMIT} and R_{SENSE} as desired. (See *Figure 3).*

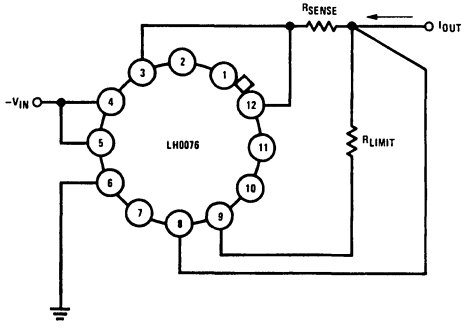


TL/H/5548–6

FIGURE 2. Current Limit Programming

For application where the current limit is used, a minimum load current of 100 μA is established at the output. This arises from the fact that the constant current used in setting maximum output current is 100 μA, and it comes directly from the output of the LH0076. If the total current is less than this minimum current, the output will drop.

As in the remote voltage adjustment application, remote current sensing can be applied similarly. R_{SENSE} should be placed as close to the output of the LH0076 as possible, but R_{LIMIT} can be a resistor or potentiometer located remotely from the device.



TL/H/5548–7

FIGURE 3. Precision Current Sink

TABLE 1. Connection Scheme for Internally Available Output Voltages

OUTPUT VOLTAGE (V)	PIN 1	PIN 2	PIN 7	PIN 10	PIN 11
−3					GND
−5			●	●	
−6	○	Gnd	○	○	
−8			●	●	●
−9	Gnd			●	●
−12	Gnd				
−15		Gnd		●	●
−18		Gnd			

National Semiconductor

PRELIMINARY

LH7001
Positive/Negative Adjustable Regulator

General Description

The LH7001 combines a positive and a negative adjustable regulator in one package. Both can supply 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors on each side to set the output voltage.

In addition to high performance both sides of the LH7001 offer full overload protection. Included are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

The LH7001 is intended for voltage and current regulation in systems where both polarities are required. This is, e.g., the case with supplies for op-amps and buffers, where the LH7001 can also be used to protect from overloads.

Normally, for stable operation, no external capacitor is needed on the positive side. The negative side requires only a single 1 μF solid tantalum capacitor. On both sides, larger output capacitors can be added to improve transient response. In case the device is further than 6 inches from the input filter capacitors, input bypass capacitors are needed. The adjustment terminals can be bypassed to achieve very high ripple rejection.

The positive and the negative regulator are electrically separated and can therefore be used independent from each other. Since each regulator is "floating" and sees only the input to output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

The LH7001 is available in a standard molded 8 pin DIP as LH7001CN with a temperature range of $-40°C$ to $+125°C$, and in an 8 pin TO-5 package as LH7001H with a temperature range from $-55°C$ to $+150°C$.

Features

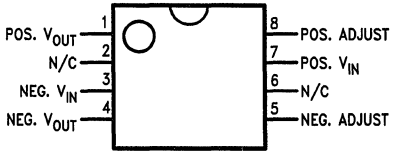
- Dual output down to $\pm 1.2V$
- Guaranteed ± 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.5%
- Current limit constant with temperature
- Standard 8 pin DIP and 8 pin TO-5 packages
- 80 dB ripple rejection
- Output is short circuit protected

Applications

- Dual precision voltage regulator
- Dual precision current limiter
- Voltage and current protection for op-amps
- Dual tracking regulator

Connection Diagrams

Plastic Package
(Dual-In-Line, 8 Pin)

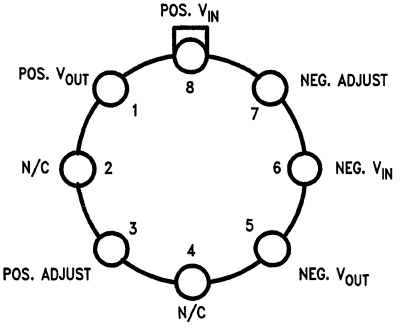


TL/K/10127–1

Top View

Order Number LH7001CN
See NS Package Number N08E

Metal Can Package
(TO-5, 8 Pin)



TL/K/10127–2

Top View

Order Number LH7001H
See NS Package Number H08D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature	
LH7001CN	−40°C to +125°C
LH7001H	−55°C to +150°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering)	
LH7001CN	4 sec. to 260°C
LH7001H	10 sec. to 300°C
ESD Rating	TBD

Electrical Characteristics (Note 1) (unless otherwise noted, these specifications apply: $-55°C < T_j < +150°C$ for the LH7001 and $-40°C \le T_j < +125°C$ for the LH7001C, $|V_{IN} - V_{OUT}| = 5V$ and $I_{OUT} = 40$ mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 600 mW for LH7001H and up to 900 mW for LH7001CN, I_{MAX} is 100 mA. Specifications apply for both positive and negative current limiter.

Parameter	Conditions		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max. Unless Otherwise Noted)
Line Regulation	$3V < \|V_{IN} - V_{OUT}\| < 40V$ (Note 4)	$T_j = 25°C$	0.01 **0.02**	0.04 **0.07**		%/V
Load Regulation	$5\text{ mA} < I_{OUT} < I_{MAX}$ (Note 4), $P \le 625$ mW	$T_j = 25°C$	0.5	0.8 **1.5**		%
Adjustment Pin Current			**50**	**100**		μA
Adjustment Pin Current Change	$5\text{ mA} < I_L < 100$ mA $3V < \|V_{IN} - V_{OUT}\| < 40V$, $P \le 625$ mW		**4**	**10**		μA
Reference Voltage	$3V < \|V_{IN} - V_{OUT}\| < 40V$, (Note 4) $5\text{ mA} < I_{OUT} < 100$mA		**1.25**	**1.3** **1.2**		V(Min)
Current Limit	$3V < \|V_{IN} - V_{OUT}\| < 13V$		**200**	**300** **100**		mA mA (Min)
	$\|V_{IN} - V_{OUT}\| < 40V$		**50**	**120** **25**		mA mA (Min)
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.04	0.2		%/W
Minimum Load Current	$\|V_{IN} - V_{OUT}\| < 40V$		**3.5**	**5**		mA
	$3 < \|V_{IN} - V_{OUT}\| < 15V$		**1.5**	**3.5**		mA
RMS Output Noise, % of V_{OUT}	$T_j = 25°C$, 10 Hz < f < 10 kHz		0.003			%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz $C_{ADJ} = 0$ μF $C_{ADJ} = 10$ μF		 65 80			dB
Long Term Stability	$T_j = 125°C$, 1000 Hrs.		0.3			%
Thermal Resistance Junction to Ambient (No Heat Sink)	H Package (TO-5)		**180**			°C/W
	N Package (DIP)		**110**			°C/W
Thermal Resistance Junction to Case	H Package (TO-5)		75			°C/W

Note 1: Boldface limits are guaranteed over full temperature range. Operating junction temperature range of LH7001CN is −25°C to +125°C, and LH7001H is −55°C to +150°C.

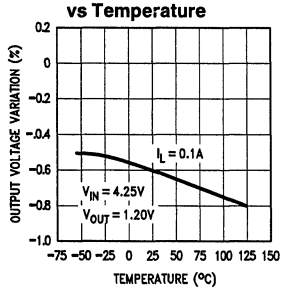
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculated outgoing quality level.

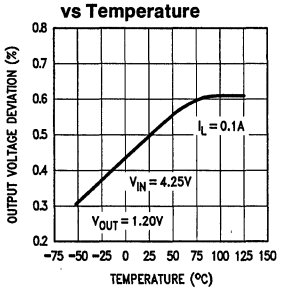
Note 4: This parameter is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Typical Performance Characteristics

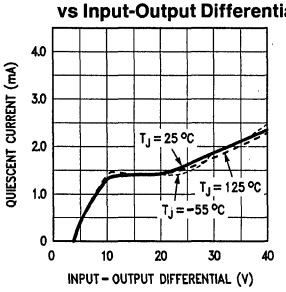
Positive Regulator Load Regulation vs Temperature



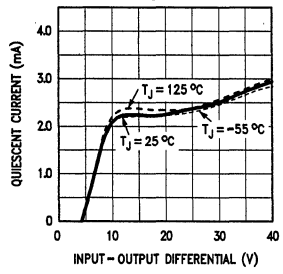
Negative Regulator Load Regulation vs Temperature



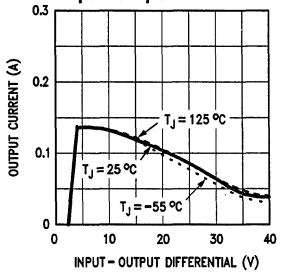
Positive Regulator Min. Operating Current vs Input-Output Differential



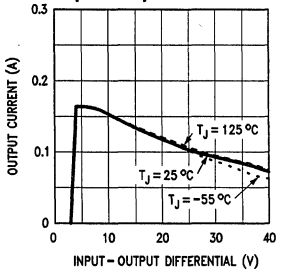
Neg. Regulator Min. Operating Current vs Input-Output Differential



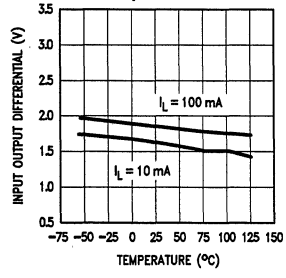
Pos. Regulator Output Current Limit vs Input-Output Differential



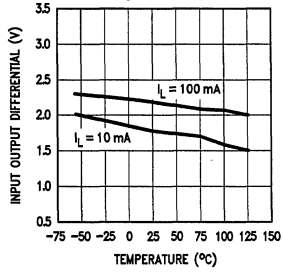
Neg. Regulator Output Current Limit vs Input-Output Differential



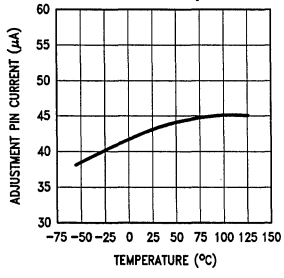
Pos. Regulator Dropout Voltage vs Temperature



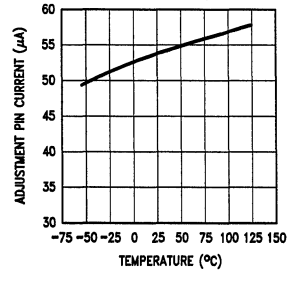
Negative Regulator Dropout Voltage vs Temperature



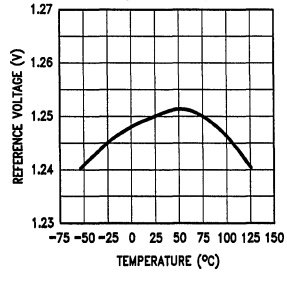
Positive Regualtor Adjustment Pin Current vs Temperature



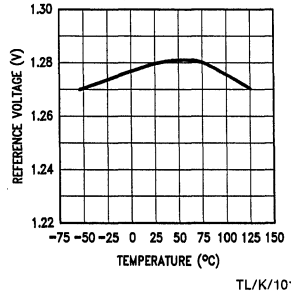
Negative Regulator Adjustment Pin Current vs Temperature



Positive Regulator Reference Voltage Stability vs Temperature



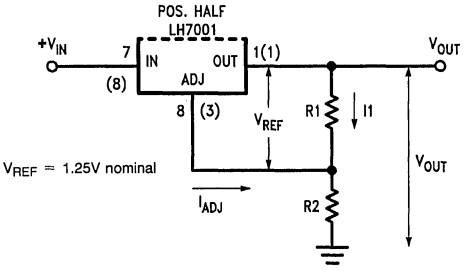
Negative Regulator Reference Voltage Stability vs Temperature



TL/K/10127–3

Application Hints

In operation, the positive regulator develops a nominal 1.25V reference voltage, V_{REF}, between the output and the adjust terminal *(Figure 1)*. The negative regulator develops −1.25V. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of $V_{OUT} = V_{REF}(1 + R2/R1) + I_{ADJ}(R2)$



TL/K/10127–4

Pinout shown for DIP (TO-5 in parenthesis)

FIGURE 1. Positive Voltage Regulator

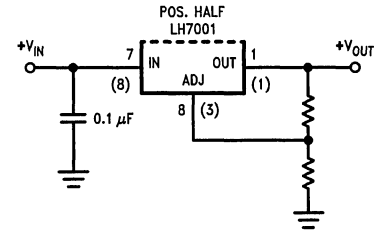
Since the current from the adjustment terminal represents an error term, the LH7001 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output voltage will rise. I_{ADJ} is typically 50 μA (see graph in Typical Performance Characteristics).

Stability

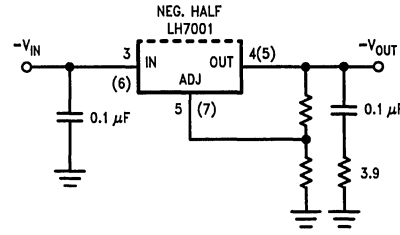
An input bypass capacitor is recommended for both the positive and the negative regulator in case the regulator is more than 6 inches away from the usual large filter capacitor. A 0.1 μF disk or 1 μF tantalum on the inputs is suitable bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possibility of problems.

The positive regulator is stable with no output capacitors. However, like any feedback circuit, certain values of external capacitance can cause excessive ringing. For the positive regulator these values are between 500 pF and 5000 pF. Additional capacitance on the output will correct the problem.

To stabilize the negative side, a lossy capacitor of more than 0.1 μF is needed from the negative output to ground. A 1 μF tantalum or 3.9Ω in series with a 0.1 μF ceramic will meet the requirement *(Figure 2)*. However, in some applications, like on the supply voltage for an op-amp, a high grade bypass capacitor is needed. In this case a lossy ceramic bead in series with the negative output, followed by 0.1 μF to ground, is recommended *(Figure 3)*. The bead needs to be optimized for frequencies around 1 MHz, a Fair-Rite 2673000101 works well.



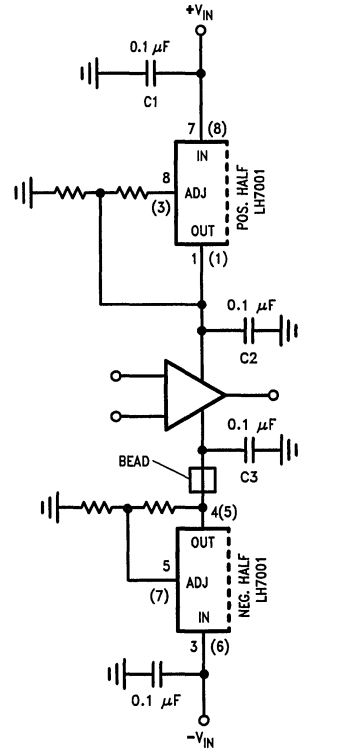
TL/K/10127–5



TL/K/10127–6

Pinout shown for DIP (TO-5 in parenthesis)

FIGURE 2. Choice of Capacitors for Stable Operation



TL/K/10127–7

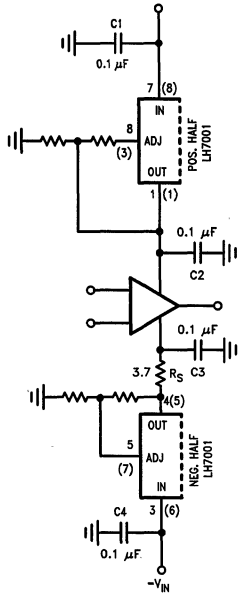
The negative regulator is stabilized with ferrite bead and C3.

Pinout shown for DIP (TO-5 in parenthesis)

FIGURE 3. LH7001 Supplying an Op-Amp

Stability (Continued)

A resistor value of 3.9Ω in series with the output followed by a 0.1 μF to ground is another way to suppress oscillations of the negative regulator, but this is only acceptable where the load regulation is not critical *(Figure 4)*.

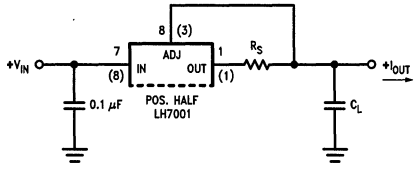


TL/K/10127–8

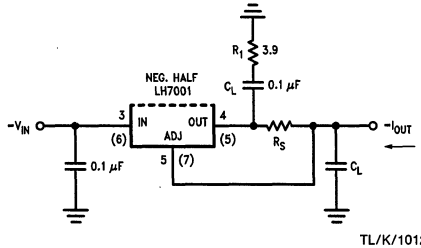
The negative regulator is stablized by R_S, C3.

FIGURE 4. LH7001 Supplying an Op-Amp*

In the current limit mode the negative regulator has a series sense resistor which separates the device from the load and its bypass capacitor. A 0.1 μF ceramic capacitor in series with 3.9Ω from the output to ground will suppress oscillations *(Figure 5)*.



TL/K/10127–9



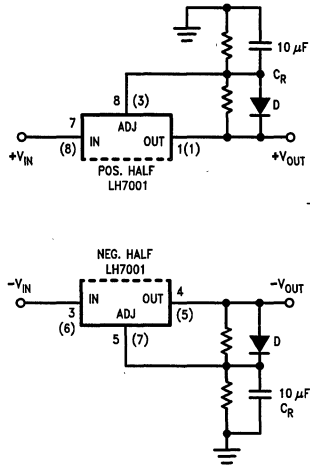
TL/K/10127–10

R1, C1 Stabilize the negative side. $I_{OUT} = \pm 1.25\ V/R_S$.

FIGURE 5. LH7001 as Dual Current Limiter*

Improved Ripple Rejection

The adjustment terminals on both the positive and the negative regulator can be bypassed to ground to improve ripple rejection and noise. These bypass capacitors prevent ripple and noise from being amplified. With 10 μF bypass capacitors 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciable increase the ripple rejection at frequencies above 120 Hz. If bypass capacitors are used, it is sometimes necessary to include protection diodes (see next section) to prevent the capacitors from discharging through internal low current paths and damaging the device *(Figure 6)*.



TL/K/10127–11

TL/K/10127–12

FIGURE 6. LH7001 with Improved Ripple Rejection*

Protection Diodes

When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage the device.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. *Figure 7* shows how to protect the device with discharge diodes.

*Pinout shown for DIP (TO-5 in parenthesis)

Protection Diodes

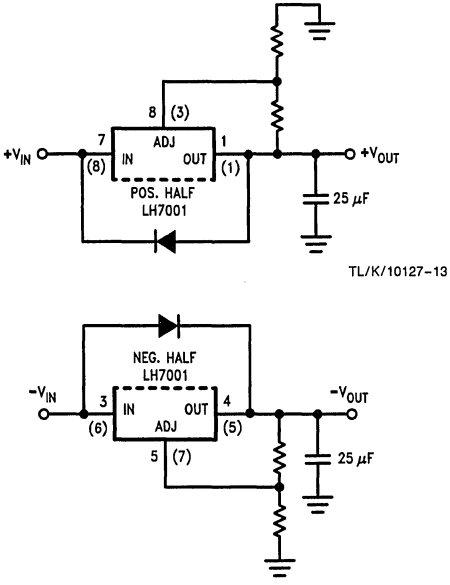


FIGURE 7. LH7001 with Large Capacitive Loads*

The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LH7001 the discharge path is through a large junction that is able to sustain a 2A surge without being degraded. For output capacitors of 10 µF or less, the LH7001's ballast resistors and output structure limit the peak current to a low enough level so that there is no need to use protection diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when either the input or output is shorted. When shorts might occur and the capacitance is in excess of 10 µF discharge diodes are recommended *(Figure 6)*.

Capacitors

In general, the best type of capacitor to use are solid tantalum. These capacitors have low impedance even at high frequencies. Depending on capacitor construction, it takes about 25 µF in aluminum electrolytic to equal 1 µF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 5 MHz. For this reason, a 0.01 µF disk may work better than a 0.1 µF disk as a bypass.

Load Regulation

The LH7001 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 50 mΩ resistance between the regulator and load will have a load regulation due to line resistance of 50 mΩ x I_L. If the set resistor is connected near the load the effective line resistance will be 50 mΩ (1 + R2/R1) or, in this case, 11.5 times worse.

Figure 8 shows the effect of resistance between the regulator and the connection of the set resistor.

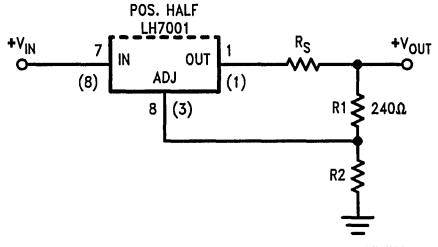


FIGURE 8. Positive Regulator with Line Resistance in Output Lead*

It is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the output pin. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

The setting resistor is normally chosen to be 240Ω. The reference voltage of 1.25V causes a current of 5.2 mA to flow, which is much larger than the maximally 100 µA flowing through the adjustment pin. This makes the regulation very stable. However, if a smaller set current is desired, the setting resistor can be increased at the expense of voltage accuracy, e.g. to 2 kΩ.

Thermal Regulation

When power is dissipated in an IC, temperature gradient occurs across the chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LH7002 specification is 0.2 %/W, maximum.

*Pinout shown for DIP (TO-5 in parenthesis)

Current Limiting and Thermal Protection

Both the positive and the negative regulator protect themselves as well as the loads. They do this by limiting the current and by a thermal shutdown feature that cuts in should the temperature in the regulator get too high.

The current limiting is relatively constant over temperature. The limit is constant up to about 15V input-to-output differential, then drops (see the graphs in the Typical Performance Characteristics).

The thermal shutdown will cut the current off as soon as the thermal sensor reaches typically 162°C. Thus the cut-off depends on the power dissipated in the LH7001 and the thermal resistance:

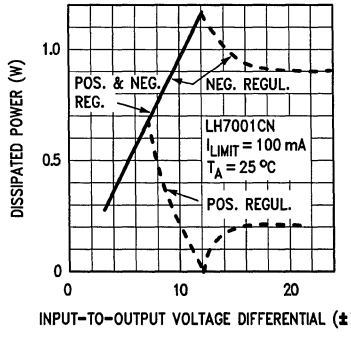
$$I_{MAX} = T_{MAX}/R_{TH}\,(V_{IN} - V_{OUT})$$

There are also two time constants involved. One is the time constant of the chip; it is typically 100 ms. The other one is the time constant of the package; it is typically 20 sec (the exact value depends on the type of cooling, heatsink, etc.). This means that for a short time the device can absorb more power than in a steady state condition.

The thermal protection on each side is independent of the other. When the protection cuts in, the output current becomes pulse width modulated. In this way the dissipation in the device is limited. The repetition time can range from several tens to several hundreds of milliseconds, with the faster times for the higher overstress. Normally, under symmetrical electric conditions, the positive side will go into thermal protection before the negative side.

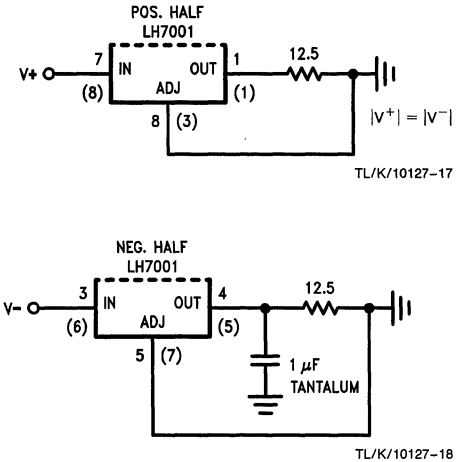
Figure 9 shows the dissipation of the positive and the negative regulator for the DIP package. The conditions are symmetrical as shown in *Figure 10*. The current through the regulators is held at a constant ±100 mA. With increasing voltage the dissipation in the device increases, and the positive regulator starts to turn off in a pulsed fashion. When the power is increased further, the positive regulator is OFF and the negative regulator goes into pulsed thermal shutdown. *Figure 11* shows the same graph for the TO-5 package.

It needs to be mentioned that the LH7001CN in the DIP package will be protected from catastrophic failure, but if operated in thermal shutdown frequently or for long durations the thermal shutdown temperature of nominally 162°C, will reduce the lifetime of the plastic package.



TL/K/10127–16

FIGURE 9. Dissipated Power of Positive and Negative Regulator vs In-to-Out Voltage Differential in a Typical LH7001CN (DIP Package)

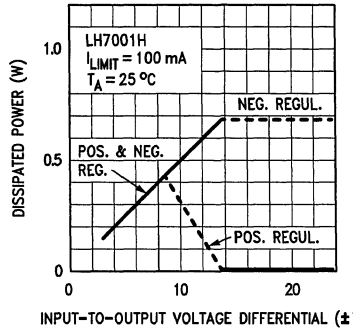


TL/K/10127–17

TL/K/10127–18

*Pinout shown for DIP (TO-5 in parenthesis)

FIGURE 10. Circuit Used to Determine Dissipation Characteristics*

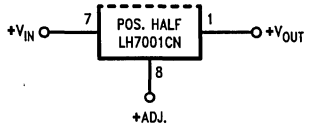


TL/K/10127–19

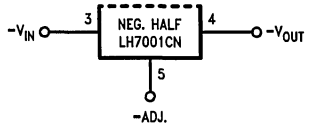
FIGURE 11. Dissipated Power of Positive and Negative Regulator vs In-to-Out Voltage Differential in a Typical LH7001H (TO-5 Package)

Schematic Diagrams

LH7001CN (DIP)

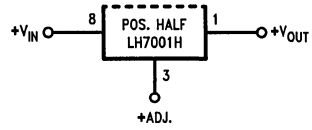


TL/K/10127–20

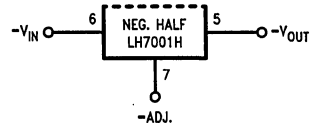


TL/K/10127–21

LH7001H (TO-5)



TL/K/10127–22

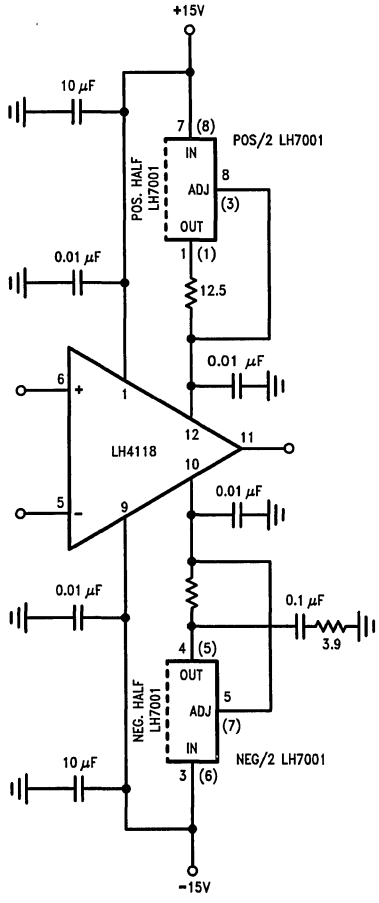


TL/K/10127–23

For detailed schematic diagrams see LM317L and LM337L datasheets.

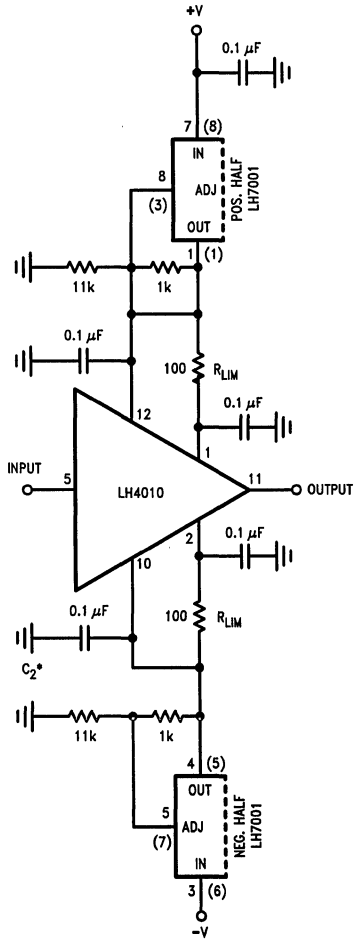
Typical Applications

Dual Current Limiter*



TL/K/10127–24

Dual Voltage Regulator*

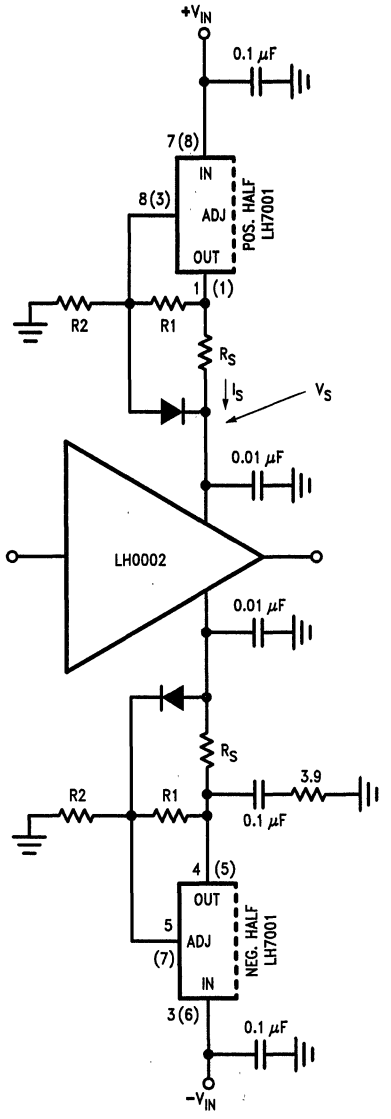


TL/K/10127–25

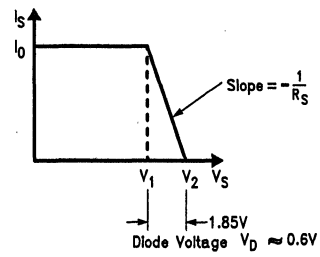
*Pinout shown for DIP (TO-5 in parenthesis)

Typical Applications (Continued)

Dual Current and Voltage Protection*



TL/K/10127-26



TL/K/10127-27

$$R_S = \frac{1.25V + V_D}{I_O}$$

$R_1 = 1\ k\Omega$ (Chosen)

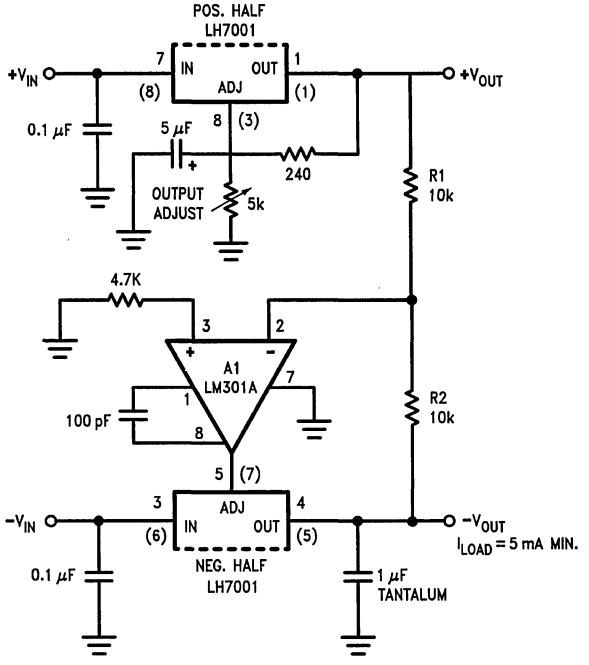
$$R_2 = R_1\left(\frac{V_2}{1.25} - 1\right)$$

$V_1 = V_2 - I_O R_S$

*Pinout shown for DIP (TO-5 in parenthesis)

Typical Applications (Continued)

Tracking Regulator*



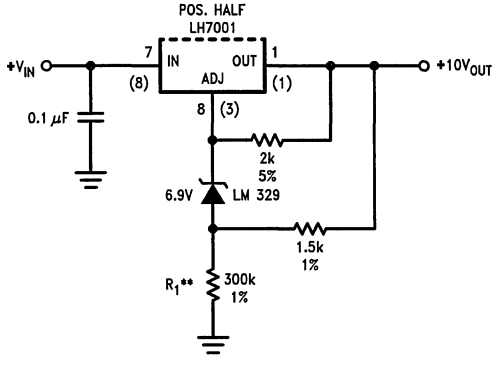
TL/K/10127–28

A_1 = LM301A, LM307 or LF13741 Only

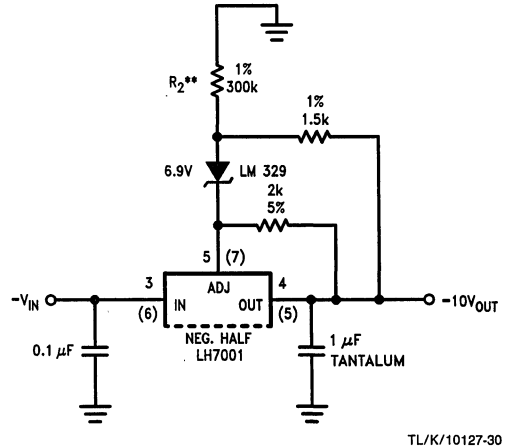
R_1, R_2 = Matched resistors with good TC tracking

*Pinout shown for DIP (TO-5 in parenthesis)

±10V High Stability Regulator*



TL/K/10127–29



TL/K/10127-30

*Pinout shown for DIP (TO-5 in parenthesis).

**To trim the output voltages R_1 and R_2 can be replaced by a series combination of 240Ω and a 100Ω potentiometer.

National Semiconductor

LM104/LM204/LM304 Negative Regulator

General Description

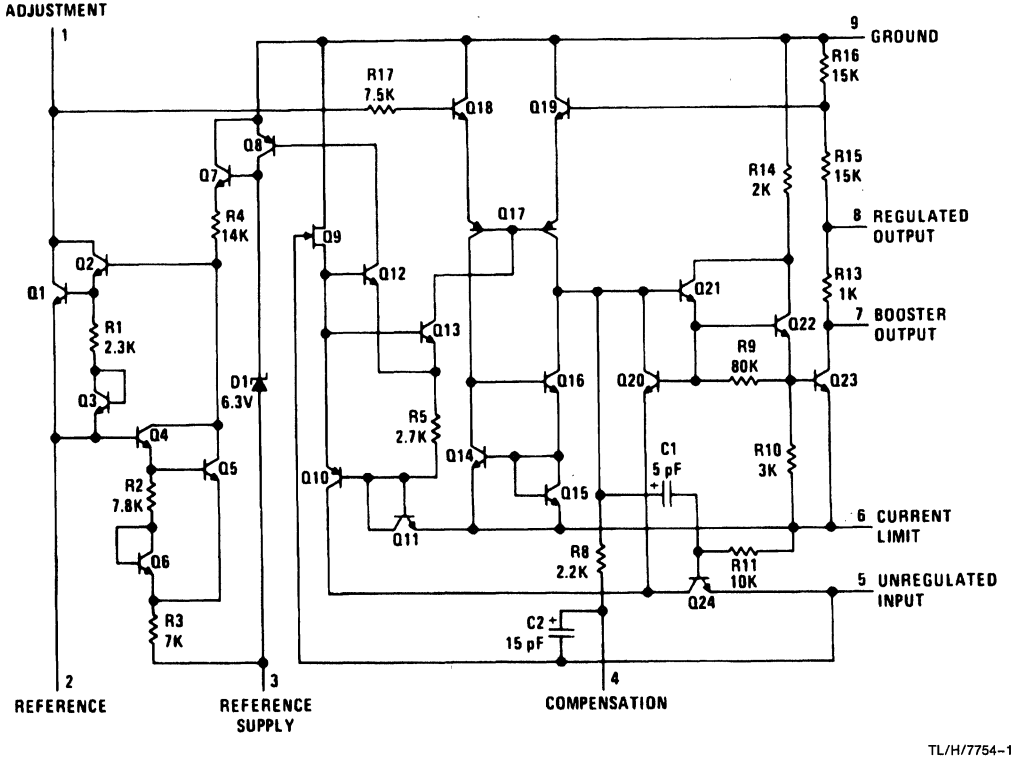
The LM104 series are precision voltage regulators which can be programmed by a single external resistor to supply any voltage from 40V down to zero while operating from a single unregulated supply. They can also provide 0.01-percent regulation in circuits using a separate, floating bias supply, where the output voltage is limited only by the breakdown of external pass transistors. Although designed primarily as linear, series regulators, the circuits can be used as switching regulators, current regulators or in a number of other control applications. Typical performance characteristics are:

- Subsurface zener reference
- 1 mV regulation no load to full load
- 0.01%/V line regulation
- 0.2 mV/V ripple rejection
- 0.3% temperature stability over military temperature range

The LM104 series is the complement of the LM105 positive regulator, intended for systems requiring regulated negative voltages which have a common ground with the unregulated supply. By themselves, they can deliver output currents to 25 mA, but external transistors can be added to get any desired current. The output voltage is set by external resistors, and either constant or foldback current limiting is made available.

The LM104 is specified for operation over the −55°C to +125°C military temperature range. The LM204 is specified for operation over the −25°C to +85°C temperature range. The LM304 is specified for operation from 0°C to +70°C.

Schematic Diagram



TL/H/7754–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 6)

	LM104/LM204	LM304
Input Voltage	50V	40V
Input-Output Voltage Differential	50V	40V
Power Dissipation (Note 1)	500 mW	500 mW
Operating Temperature Range		
LM104	−55°C to +125°C	
LM204	−25°C to +85°C	
LM304		0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C for plastic	300°C for hermetic

Electrical Characteristics

Parameter	Conditions	LM104/LM204			LM304			Units
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range		−50		−8	−40		−8	V
Output Voltage Range		−40		−0.015	−30		−0.035	V
Output-Input Voltage Differential (Note 3)	I_O = 20 mA I_O = 5 mA	2.0 0.5		50 50	2.0 0.5		40 40	V V
Load Regulation (Note 4)	$O \le I_O \le 20$ mA $R_{SC} = 15\Omega$		1	5		1	5	mV
Line Regulation (Note 5)	$V_{OUT} \le -5V$ $\Delta V_{IN} = 0.1\ V_{IN}$		0.056	0.1		0.056	0.1	%
Ripple Rejection	C_{19} = 10 μF, f = 120 Hz $V_{IN} < -15V$ $-7V \ge V_{IN} \ge -15V$		0.2 0.5	0,.5 1.0		0.2 0.5	0.5 1.0	mV/V mV/V
Output Voltage Scale Factor	$R_{2\text{-}3}$ = 2.4k	1.8	2.0	2.2	1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \le -1V$		0.3	1.0		0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz $V_O \le -5V$, $C_{1\text{-}9} = 0$ $C_{1\text{-}9}$ = 10 μF		0.007 15			0.007 15		% μV
Standby Current Drain	I_L = 5 mA, V_O = 0 $V_O = -30V$ $V_O = -40V$		1.7 3.6	2.5 5.0		1.7 3.6 	2.5 5.0 	mA mA mA
Long Term Stability	$V_O \le -1V$		0.01	1.0		0.01	1.0	%

Note 1: The maximum junction temperature of the LM104 is 150°C, while that of the LM204 is 125°C and LM304 is 100°C. For operating at elevated temperatures, devices in the H10C package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: These specifications apply for junction temperatures between −55°C and 150°C (between −25°C and 100°C for the LM204 and 0°C to +85°C for the LM304) and for input and output voltages within the ranges given, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 3: When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1V.

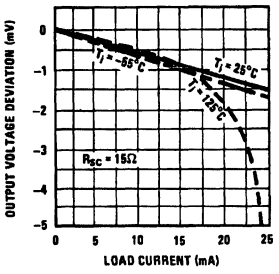
Note 4: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

Note 5: With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0V and − 5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.

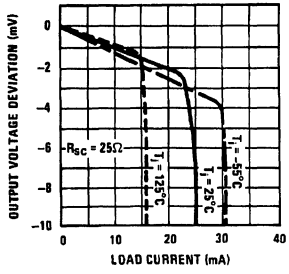
Note 6: Refer to RETS104X drawing for military specifications for the LM104.

Typical Performance Characteristics

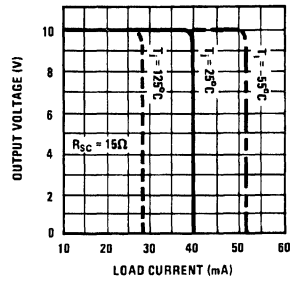
Load Regulation



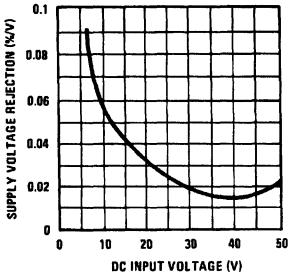
Load Regulation



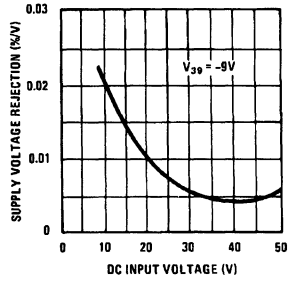
Current Limiting



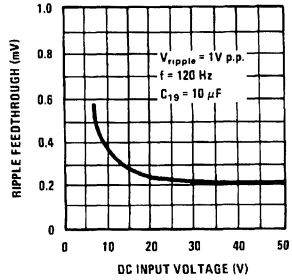
Supply Voltage Rejection



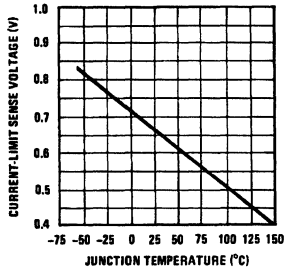
Supply Voltage Rejection With Preregulated Reference Supply



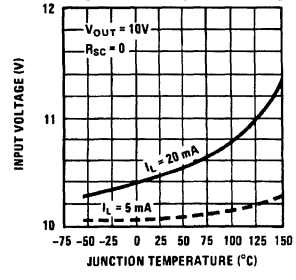
Ripple Rejection



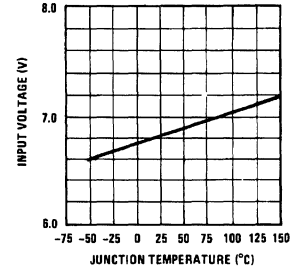
Current Limit Sense Voltage



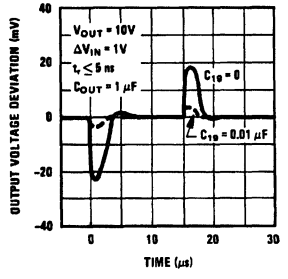
Regulator Dropout Voltage



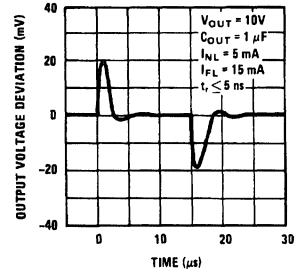
Minimum Input Voltage



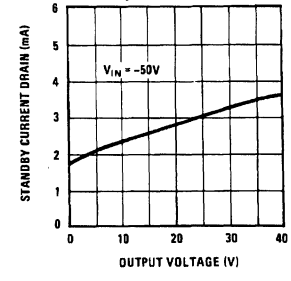
Line Transient Response



Load Transient Response



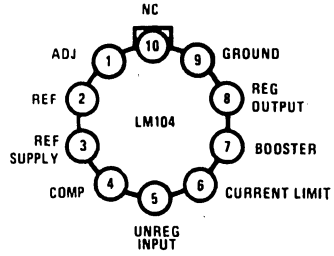
Standby Current Drain



TL/H/7754–7

Connection Diagram

Metal Can Package



TL/H/7754–2

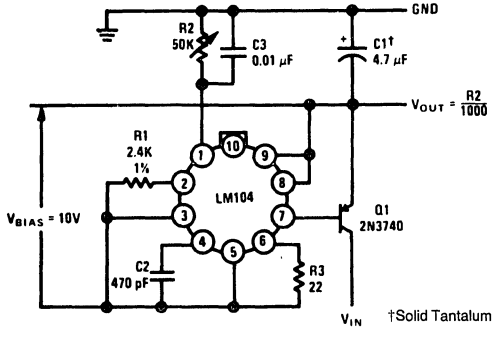
Note: Pin 5 connected to case.

Top View

Order Number LM104H, LM204H or LM304H
See NS Package H10C

Typical Applications

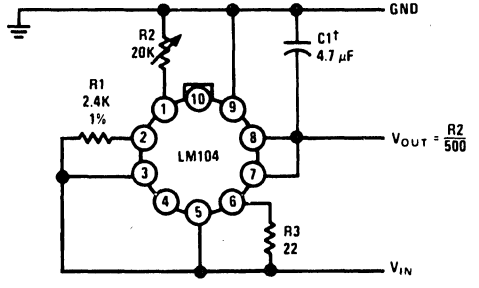
Operating with Separate Bias Supply



†Solid Tantalum

TL/H/7754–3

Basic Regulator Circuit

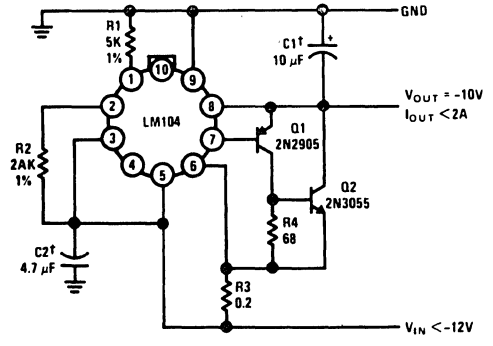


†Solid Tantalum

Trim R1 for exact scale factor.

TL/H/7754–5

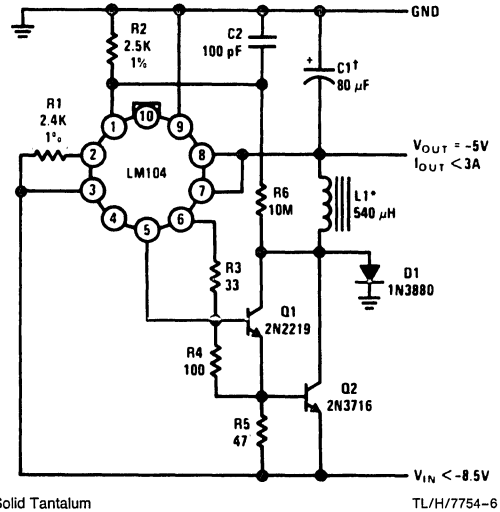
High Current Regulator



†Solid Tantalum

TL/H/7754–4

Switching Regulator



†Solid Tantalum

TL/H/7754–6

*60 turns #20 on Arnold Engineering A930157-2 Molybdenum Permalloy Core.

National Semiconductor

LM105/LM205/LM305/LM305A, LM376 Voltage Regulators

General Description

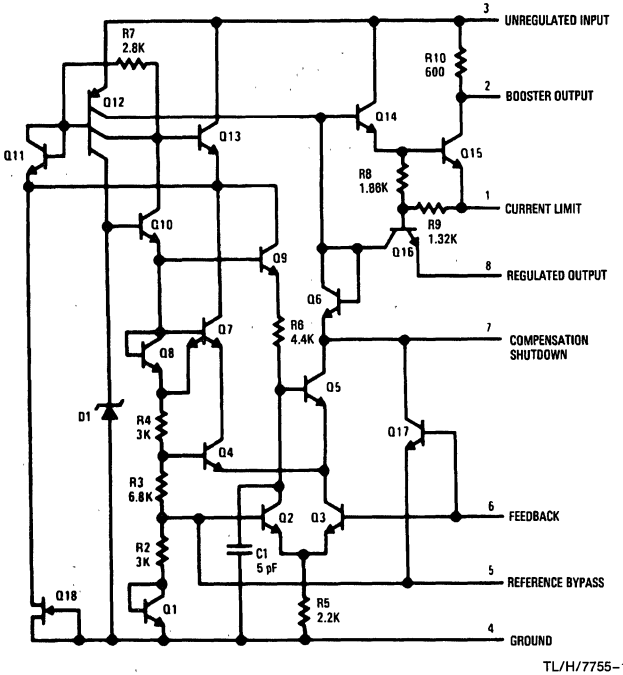
The LM105 series are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection on 0.01%V
- 45 mA output current without external pass transistor (LM305A)

Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in either an 8-lead, TO-5 header or a 1/4" x 1/4" metal flat package.

The LM105 is specified for operation for $-55°C \leq T_A \leq +125°C$, the LM205 is specified for $-25°C \leq T_A \leq +85°C$, and the LM305/LM305A, LM376 is specified for $0°C \leq T_A \leq +70°C$.

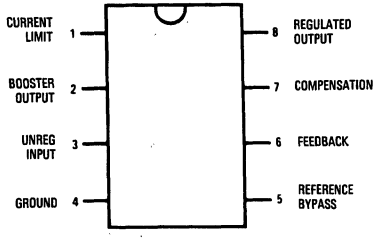
Schematic and Connection Diagrams



TL/H/7755–1

Pin connections shown are for metal can.

Dual-In-Line Package

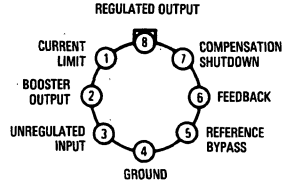


TL/H/7755–2

Top View

Order Number LM376N
See NS Package Number N08E

Metal Can Package



TL/H/7755–3

Top View

Order Number LM105H,
LM205H, LM305H or LM305AH
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

	LM105	LM205	LM305	LM305A	LM376
Input Voltage	50V	50V	40V	50V	40V
Input-Output Differential	40V	40V	40V	40V	40V
Power Dissipation (Note 1)	800 mW	800 mW	800 mW	800 mW	400 mW
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	−0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	260°C

Electrical Characteristics (Note 2)

Parameter	Conditions	LM105			LM205			LM305			LM305A			LM376			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Voltage Range		8.5		50	8.5		50	8.5		40	8.5		50	9.0		40	V
Output Voltage Range		4.5		40	4.5		40	4.5		30	4.5		40	5.0		37	V
Input-Output Voltage Differential		3.0		30	3.0		30	3.0		30	3.0		30	3.0		30	V
Load Regulation (Note 3)	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05		0.02	0.05		0.02	0.05							%
	$R_{SC} = 10\Omega$, $T_A = T_{A(MAX)}$		0.03	0.1		0.03	0.1		0.03	0.1							%
	$R_{SC} = 10\Omega$, $T_A = T_{A(MIN)}$		0.03	0.1		0.03	0.1		0.03	0.1							%
		$0 \le I_O \le 12$ mA			$0 \le I_O \le 12$ mA			$0 \le I_O \le 12$ mA									
	$R_{SC} = 0\Omega$, $T_A = 25°C$											0.02	0.2			0.2	%
	$R_{SC} = 0\Omega$, $T_A = 70°C$											0.03	0.4			0.5	%
	$R_{SC} = 0\Omega$, $T_A = 0°C$											0.03	0.4			0.5	%
											$0 \le I_O \le 45$ mA			$0 \le I_O \le 25$ mA			
Line Regulation	$T_A = 25°C$															0.03	%/V
	$0°C \le T_A \le +70°C$															0.1	%/V
	$V_{IN} - V_{OUT} \le 5V$, $T_A = 25°C$		0.025	0.06		0.025	0.06		0.025	0.06		0.025	0.06				%/V
	$V_{IN} - V_{OUT} \ge 5V$, $T_A = 25°C$		0.015	0.03		0.015	0.03		0.015	0.03		0.015	0.03				%/V
Temperature Stability	$T_{A(MIN)} \le T_A \le T_{A(MAX)}$		0.3	1.0		0.3	1.0		0.3	1.0		0.3	1.0				%

Electrical Characteristics (Note 2) (Continued)

Parameter	Conditions	LM105			LM205			LM305			LM305A			LM376			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Feedback Sense Voltage		1.63	1.7	1.81	1.63	1.7	1.81	1.63	1.7	1.81	1.55	1.7	1.85	1.60	1.72	1.80	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz																
	C_{REF} = 0		0.005			0.005			0.005			0.005					%
	C_{REF} = 0.1 μF		0.002			0.002			0.002			0.002					%
Standby Current Drain	V_{IN} = 30V, T_A = 25°C															2.5	mA
	V_{IN} = 40V								0.8	2.0							mA
	V_{IN} = 50V		0.8	2.0		0.8	2.0					0.8	2.0				mA
Current Limit Sense Voltage	T_A = 25°C, R_{SC} = 10Ω, V_{OUT} = 0V, (Note 4)	225	300	375	225	300	375	225	300	375	225	300	375		300		mV
Long Term Stability			0.1			0.1			0.1			0.1					%
Ripple Rejection	C_{REF} = 10 μF, f = 120 Hz		0.003			0.003			0.003			0.003					%/V
θ_{JA}	Epoxy Dual-In-Line Package														140		°C/W
θ_{JA}	TO-5 Board Mount in Still Air		230			230			230			230					°C/W
θ_{JA}	TO-5 Board Mount in 400 LF/Min Air Flow		92			92			92			92					°C/W
θ_{JC}	TO-5		25			25			25			25					°C/W

Note 1: The maximum junction temperature of the LM105 and LM305A is 150°C, the LM205 and LM376 is 100°C, and the LM305 is 85°C. For operation at elevated temperatures, devices in the H08C package must be derated based on a thermal resistance of 168°C/W junction to ambient, or 25°C/W junction to case. For the epoxy dual-in-line package, derating is based on a thermal resistance of 138°C/W junction to ambient. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power average over a five second interval for the LM105 and LM205, and averaged over a two second interval for the LM305.

Note 2: Unless otherwise specified, these specifications apply for temperatures within the operating temperature range, for input and output voltages within the range given, and for a divider impedance seen by the feedback terminal of 2 kΩ. Load and line regulation specifications are for a constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

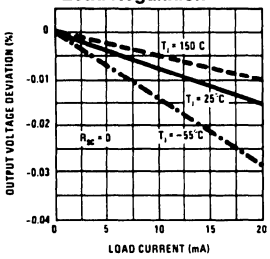
Note 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

Note 4: With no external pass transistor.

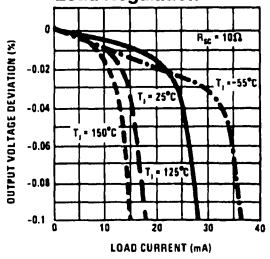
Note 5: Refer to RETS105X Drawing for military specifications for the LM105.

Typical Performance Characteristics LM105/LM205/LM305/LM305A

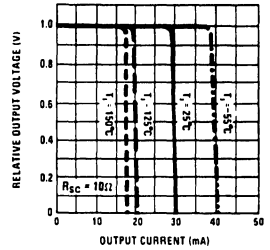
Load Regulation



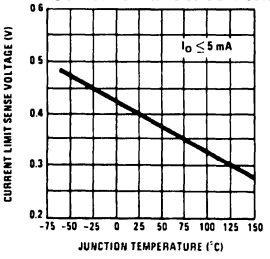
Load Regulation



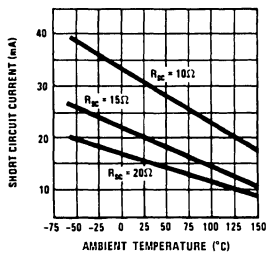
Current Limiting Characteristics



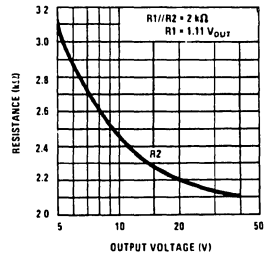
Current Limit Sense Voltage



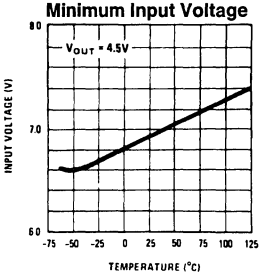
Short Circuit Current



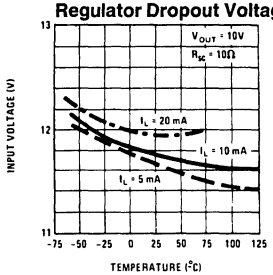
Optimum Divider Resistance Values



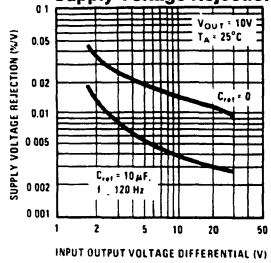
Minimum Input Voltage



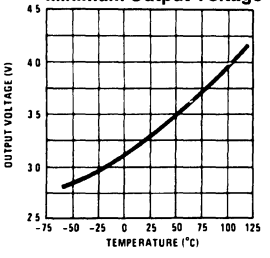
Regulator Dropout Voltage



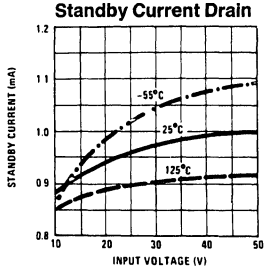
Supply Voltage Rejection



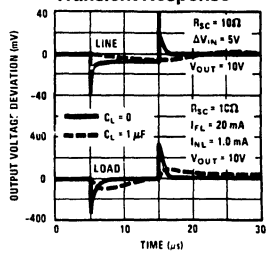
Minimum Output Voltage



Standby Current Drain



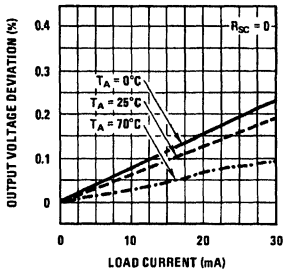
Transient Response



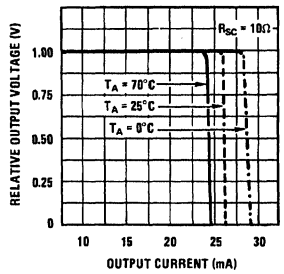
TL/H/7755–6

Typical Performance Characteristics LM376

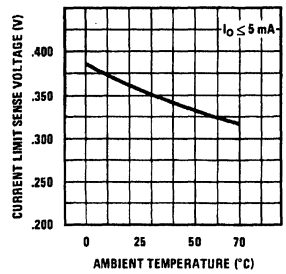
Load Regulation



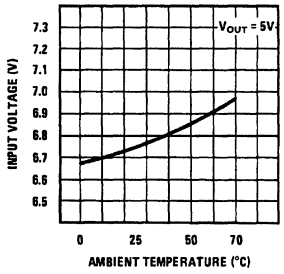
Current Limiting Characteristics



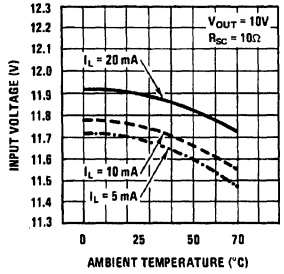
Current Limiting Sense Voltage



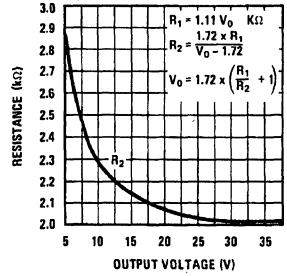
Minimum Input Voltage



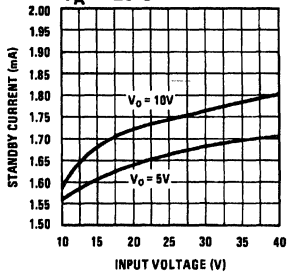
Regulator Dropout Voltage



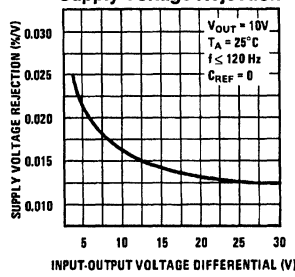
Optimum Divider Resistance



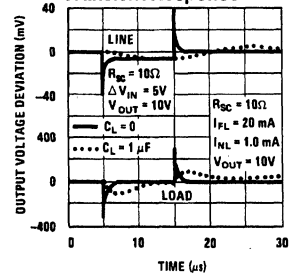
Standby Current Drain
T_A = 25°C



Supply Voltage Rejection



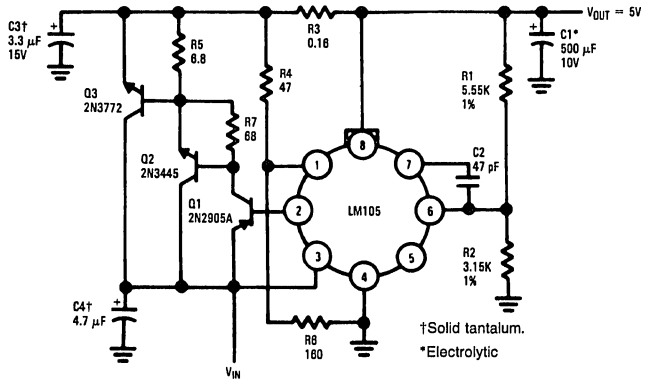
Transient Response



TL/H/7755–7

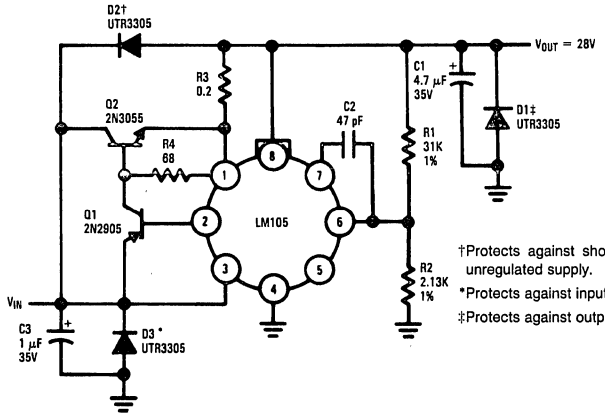
Typical Applications

10A Regulator with Foldback Current Limiting



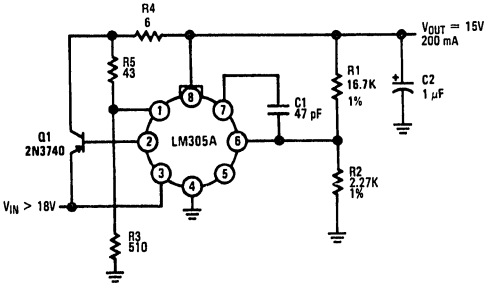
TL/H/7755–4

1.0A Regulator with Protective Diodes



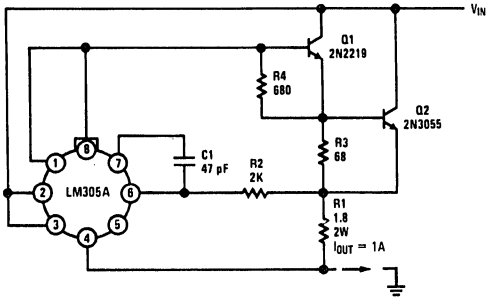
TL/H/7755–5

Linear Regulator with Foldback Current Limiting



TL/H/7755–8

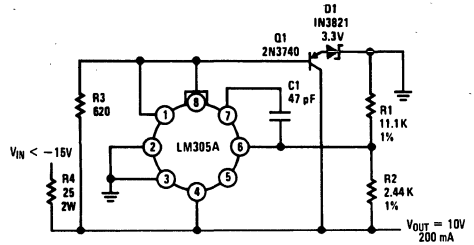
Current Regulator



TL/H/7755–9

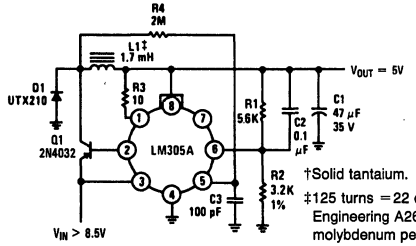
Typical Applications (Continued)

Shunt Regulator



TL/H/7755–10

Switching Regulator

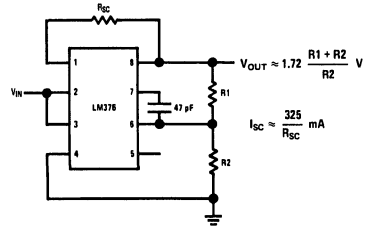


†Solid tantalum.

‡125 turns = 22 on Arnold Engineering A262123-2 molybdenum permally core.

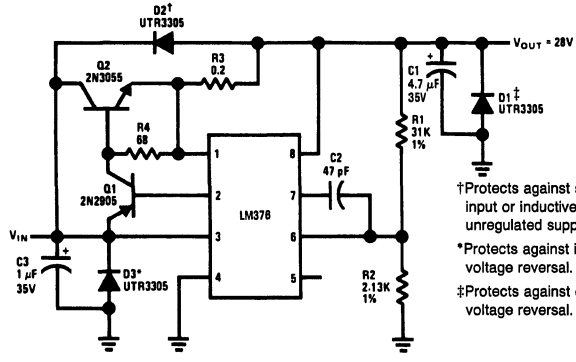
TL/H/7755–11

Basic Positive Regulator with Current Limiting



TL/H/7755–12

1.0A Regulator with Protective Diodes



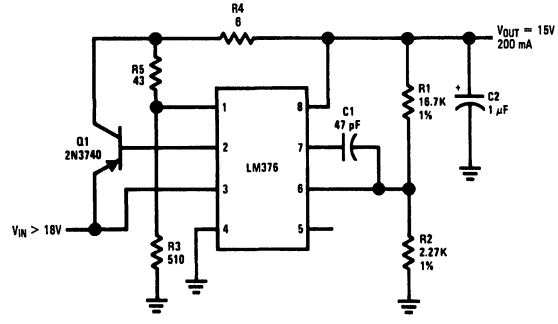
†Protects against shorted input or inductive loads on unregulated supply.

*Protects against input voltage reversal.

‡Protects against output voltage reversal.

TL/H/7755–13

Linear Regulator with Foldback Current Limiting



TL/H/7755–14

National Semiconductor

LM109/LM309 5-Volt Regulator

General Description

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

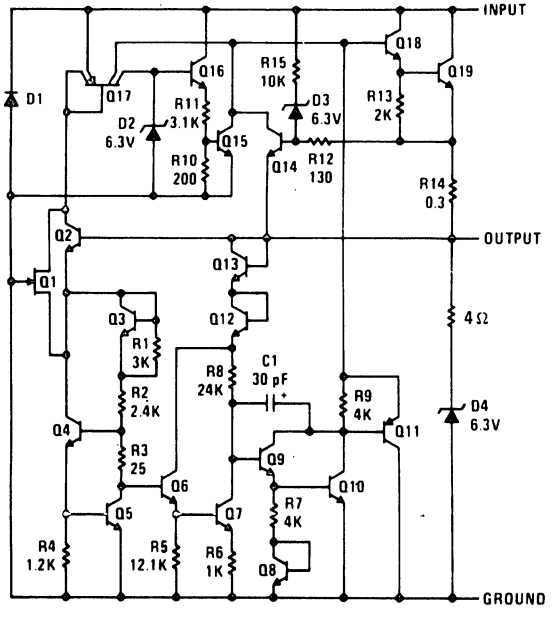
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Features

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

Schematic Diagram



TL/H/7138–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 3)

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	−55°C to +150°C
LM309	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM109			LM309			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$ $7.10V \le V_{IN} \le 25V$		4.0	50		4.0	50	mV
Load Regulation	$T_j = 25°C$							
TO-5 Package	$5\ mA \le I_{OUT} \le 0.5A$		15	50		15	50	mV
TO-3 Package	$5\ mA \le I_{OUT} \le 1.5A$		15	100		15	100	mV
Output Voltage	$7.40V \le V_{IN} \le 25V$, $5\ mA \le I_{OUT} \le I_{MAX}$, $P < P_{MAX}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7.40V \le V_{IN} \le 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$7.40V \le V_{IN} \le 25V$			0.5			0.5	mA
	$5\ mA \le I_{OUT} \le I_{MAX}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$ $10\ Hz \le f \le 100\ kHz$		40			40		μV
Long Term Stability			10			20		mV
Ripple Rejection	$T_j = 25°C$	50			50			dB
Thermal Resistance, Junction to Case	(Note 2)							
TO-5 Package			15			15		°C/W
TO-3 Package			2.5			2.5		°C/W

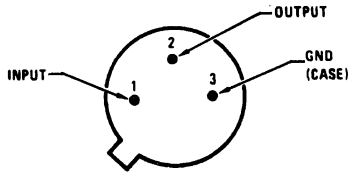
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM109 and $0°C \le T_j \le +125°C$ for the LM309; $V_{IN} = 10V$; and $I_{OUT} = 0.1A$ for the TO-39 package or $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-39 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$.

Note 2: Without a heat sink, the thermal resistance of the TO-39 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

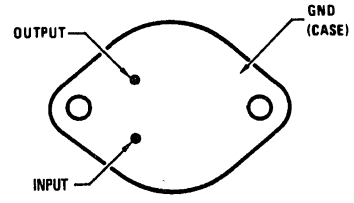
Note 3: Refer to RETS109H drawing for LM109H or RETS109K drawing for LM109K military specifications.

Connection Diagrams

Metal Can Packages



Order Number LM109H or LM309H
See NS Package Number H03A



TL/H/7138–3

Order Number LM109K STEEL or LM309K STEEL
See NS Package Number K02A

For Aluminum Package
Order Number LM309K
See NS Package Number KC02A

Application Hints

a. Bypass the input of the LM109 to ground with ≥ 0.2 μF ceramic or solid tantalum capacitor if main filter capacitor is more than 4 inches away.

b. Use steel package instead of aluminum if more than 5,000 thermal cycles are expected. (ΔT ≥ 50°C)

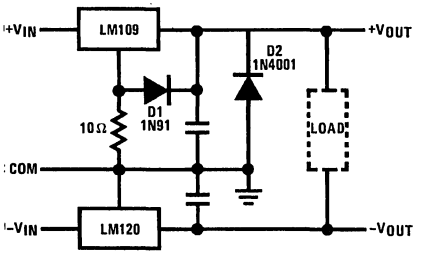
c. Avoid insertion of regulator into "live" socket if input voltage is greater than 10V. The output will rise to within 2V of the unregulated input if the ground pin does not make contact, possibly damaging the load. The LM109 may also be damaged if a large output capacitor is charged up, then discharged through the internal clamp zener when the ground pin makes contact.

d. The output clamp zener is designed to absorb transients only. It will not clamp the output effectively if a failure occurs in the internal power transistor structure. Zener dynamic impedance is ≈ 4Ω. Continuous RMS current into the zener should not exceed 0.5A.

e. Paralleling of LM109s for higher output current is not recommended. Current sharing will be almost nonexistent, leading to a current limit mode operation for devices with the highest initial output voltage. The current limit devices may also heat up to the thermal shutdown point (≈ 175°C). Long term reliability cannot be guaranteed under these conditions.

f. Preventing latchoff for loads connected to negative voltage:

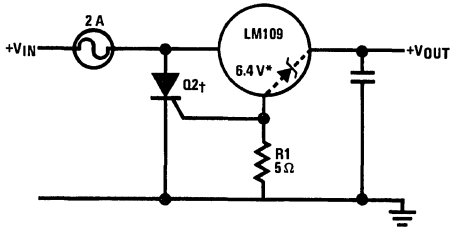
If the output of the LM109 is pulled negative by a high current supply so that the output pin is more than 0.5V negative with respect to the ground pin, the LM109 can latch off. This can be prevented by clamping the ground pin to the output pin with a germanium or Schottky diode as shown. A silicon diode (1N4001) at the output is also needed to keep the positive output from being pulled too far negative. The 10Ω resistor will raise $+V_{OUT}$ by ≈ 0.05V.



TL/H/7138–7

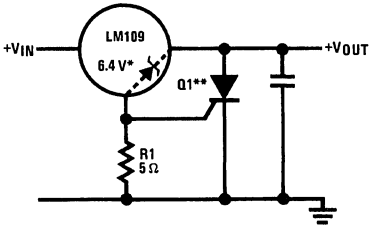
Crowbar Overvoltage Protection

Input Crowbar



TL/H/7138–8

Output Crowbar



TL/H/7138–9

*Zener is internal to LM109.

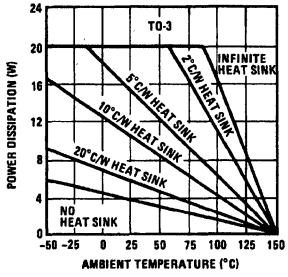
**Q1 must be able to withstand 7A continuous current if fusing is not used at regulator input. LM109 bond wires will fuse at currents above 7A.

†Q2 is selected for surge capability. Consideration must be given to filter capacitor size, transformer impedance, and fuse blowing time.

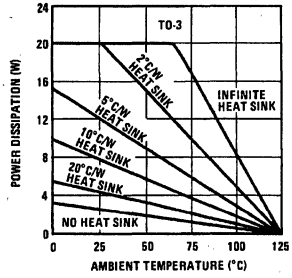
††Trip point is ≈ 7.5V.

Typical Performance Characteristics

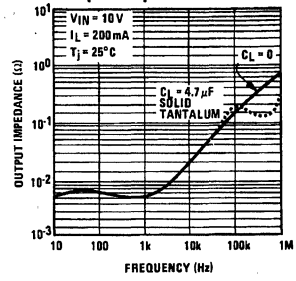
Maximum Average Power Dissipation (LM109K)



Maximum Average Power Dissipation (LM309K)

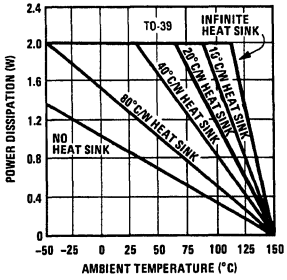


Output Impedance

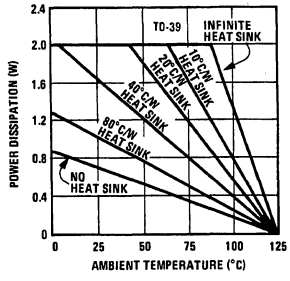


TL/H/7138–10

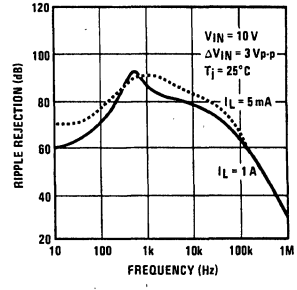
Maximum Average Power Dissipation (LM109H)



Maximum Average Power Dissipation (LM309H)

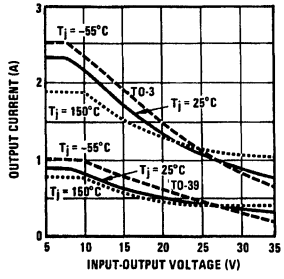


Ripple Rejection

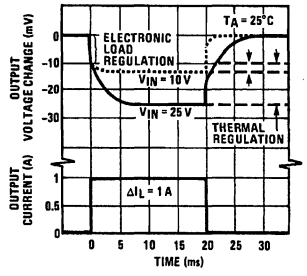


TL/H/7138–11

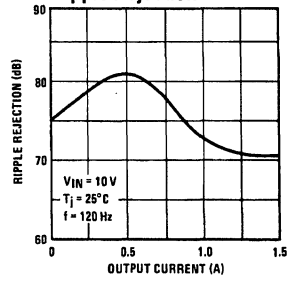
Current Limit Characteristics (Note 1)



Thermally Induced Output Voltage Variation



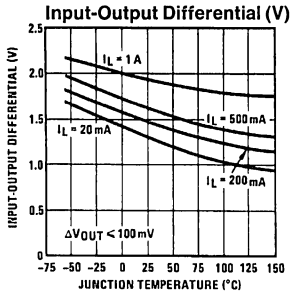
Ripple Rejection

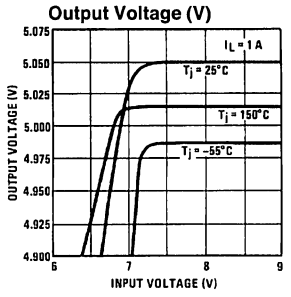


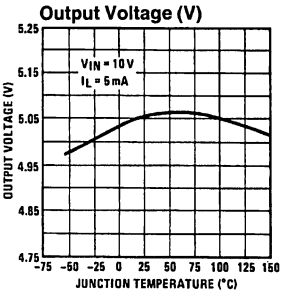
TL/H/7138–12

Note 1: Current limiting foldback characteristics are determined by input output differential, not by output voltage.

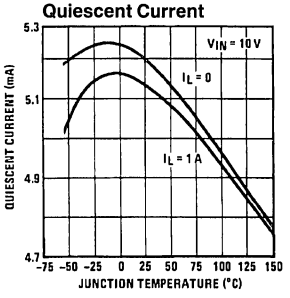
Typical Performance Characteristics (Continued)

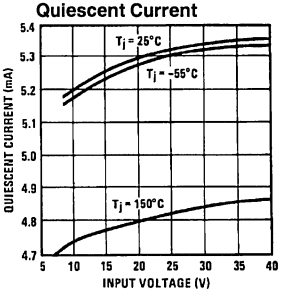


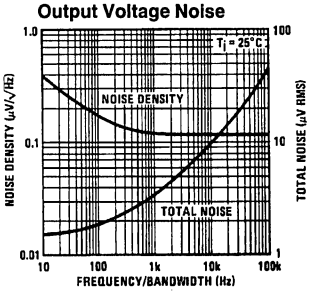




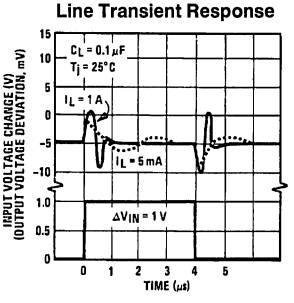
TL/H/7138–13

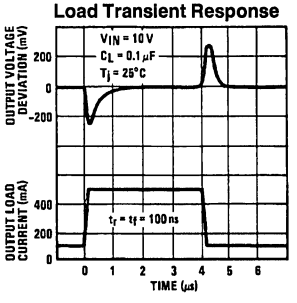






TL/H/7138–14

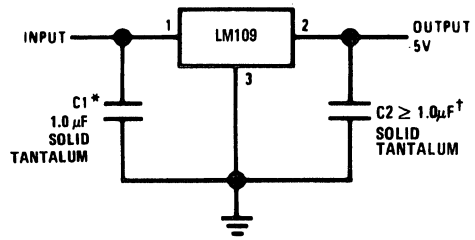




TL/H/7138–15

Typical Applications

Fixed 5V Regulator



TL/H/7138–2

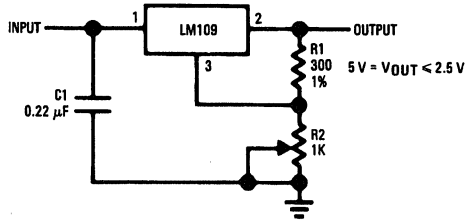
*Required if regulator is located more than 4" from power supply filter capacitor.

†Although no output capacitor is needed for stability, it does improve transient response.

C2 should be used whenever long wires are used to connect to the load, or when transient response is critical.

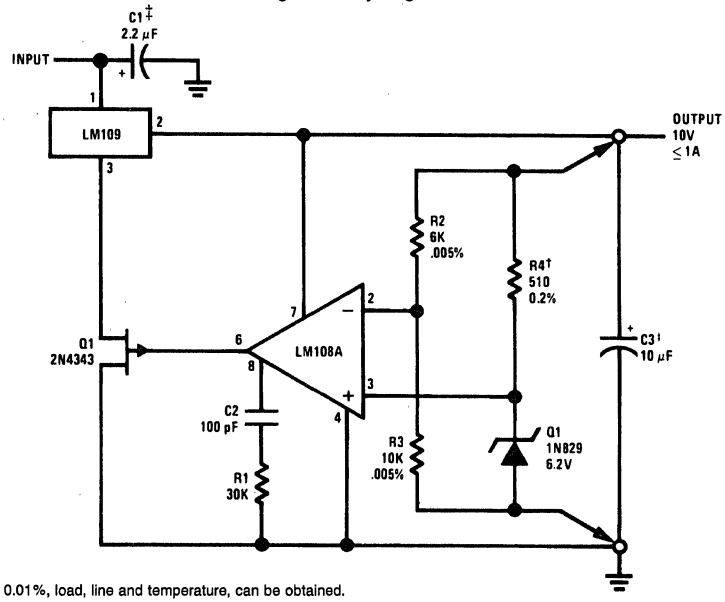
Note: Pin 3 electrically connected to case.

Adjustable Output Regulator



TL/H/7138–4

High Stability Regulator*



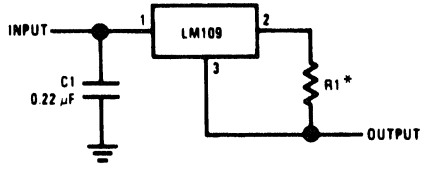
*Regulation better than 0.01%, load, line and temperature, can be obtained.

†Determines zener current. May be adjusted to minimize thermal drift.

‡Solid tantalum.

TL/H/7138–5

Current Regulator



TL/H/7138–6

*Determines output current. If wirewound resistor is used, bypass with 0.1 μF.

National Semiconductor

LM117A/LM117/LM317A/LM317 3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117 series devices with a "K" suffix are packaged in standard TO-3 transistor packages, while those with an "H" suffix are in a solid Kovar-base TO-39 transistor package. The LM117A and LM117 are rated for operation from −55°C to +150°C, the LM317A from −40°C to +125°C, and the LM317 from 0°C to +125°C. The LM317AT and the LM317T are available in a TO-220 plastic package and the LM317MP in a TO-202 plastic package.

For applications requiring greater output current, see LM150 series (3A) and LM138 series (5A) data sheets. For the negative complement, see LM137 series data sheet.

LM117 Series Packages and Power Capability

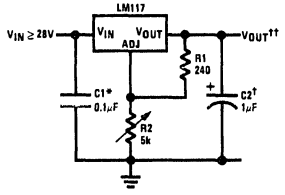
Part Number Suffix	Package	Rated Power Dissipation	Design Load Current
K	TO-3	20W	1.5A
H	TO-39	2W	0.5A
T	TO-220	20W	1.5A
MP	TO-202	2W	0.5A

Features

- Guaranteed 1% output voltage tolerance (LM117A, LM317A)
- Guaranteed max. 0.01%/V line regulation (LM117A, LM317A)
- Guaranteed max. 0.3% load regulation (LM117A, LM117)
- Guaranteed 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- 100% electrical burn-in
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–25V Adjustable Regulator



TL/H/9063–1

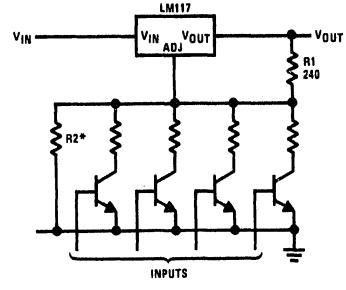
Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

Digitally Selected Outputs



TL/H/9063–2

*Sets maximum V_{OUT}

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance (Note 5)	3 kV

Operating Temperature Range

LM117A/LM117	$-55°C \le T_J \le +150°C$
LM317A	$-40°C \le T_J \le +125°C$
LM317	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 3)

Parameter	Conditions	LM117A			LM117			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage		1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10 mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$ (Note 4)		0.005	0.01		0.01	0.02	%/V
			0.01	**0.02**		**0.02**	**0.05**	%/V
Load Regulation	$10 mA \le I_{OUT} \le I_{MAX}$ (Note 4)		0.1	0.3		0.1	0.3	%
			0.3	**1**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.03	0.07		0.03	0.07	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le I_{MAX}$ $3V \le (V_{IN} - V_{OUT}) \le 40V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$(V_{IN} - V_{OUT}) \le 15V$							
	K Package	**1.5**	**2.2**	**3.4**	**1.5**	**2.2**	**3.4**	A
	H Package	**0.5**	**0.8**	**1.8**	**0.5**	**0.8**	**1.8**	A
	$(V_{IN} - V_{OUT}) = 40V$							
	K Package	0.3	0.4		0.3	0.4		A
	H Package	0.15	0.2		0.15	0.2		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**80**		**66**	**80**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3		2.3	3	°C/W
	H Package		12	15		12	15	°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35			35		°C/W
	H Package		140			140		°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 3)

Parameter	Conditions	LM317A			LM317			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage		1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V, 10 mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V (Note 4)		0.005	0.01		0.01	0.04	%/V
			0.01	**0.02**		**0.02**	**0.07**	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ I_{MAX} (Note 4)		0.1	0.5		0.1	0.5	%
			0.3	**1**		**0.3**	**1.5**	%
Thermal Regulation	20 ms Pulse		0.04	0.07		0.04	0.07	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ I_{MAX} 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	T_{MIN} ≤ T_J ≤ T_{MAX}		**1**			**1**		%
Minimum Load Current	($V_{IN} - V_{OUT}$) = 40V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	($V_{IN} - V_{OUT}$) ≤ 15V							
	K and T Package	**1.5**	**2.2**	**3.4**	**1.5**	**2.2**	**3.4**	A
	H Package	**0.5**	**0.8**	**1.8**	**0.5**	**0.8**	**1.8**	A
	P Package				**0.5**	**0.8**	**1.8**	A
	($V_{IN} - V_{OUT}$) = 40V							
	K and T Package	0.15	0.4		0.15	0.4		A
	H Package	0.075	0.2		0.075	0.2		A
	P Package				0.075	0.2		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**80**		**66**	**80**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3		2.3	3	°C/W
	H Package		12	15		12	15	°C/W
	T Package		4	5		4		°C/W
	P Package					7		°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35			35		°C/W
	H Package		140			140		°C/W
	T Package		50			50		°C/W
	P Package					80		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS117AH drawing for the LM117AH, the RETS117H drawing for the LM117H, the RETS117AK drawing for the LM117AK, or the RETS117K for the LM117K military specifications.

Note 3: Although power dissipation is internally limited, these specifications are applicable for maximum power dissipations of 2W for the TO-39 and TO-202, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39 and TO-202 packages. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

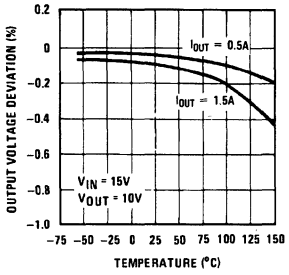
Note 4: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

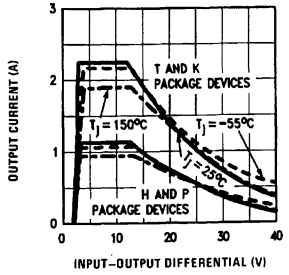
Typical Performance Characteristics

Output Capacitor = 0 μF unless otherwise noted

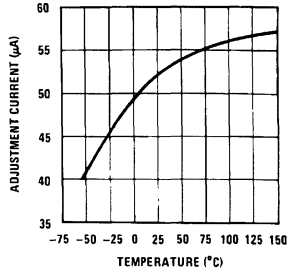
Load Regulation



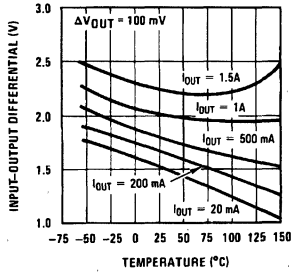
Current Limit



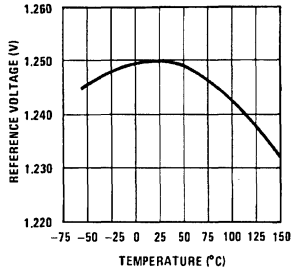
Adjustment Current



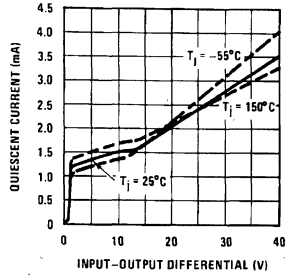
Dropout Voltage



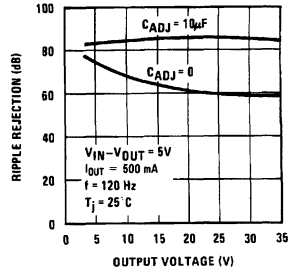
Temperature Stability



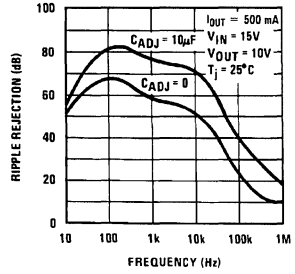
Minimum Operating Current



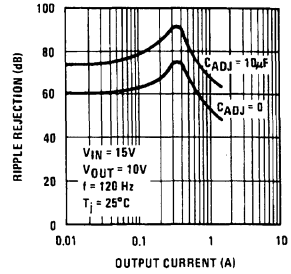
Ripple Rejection



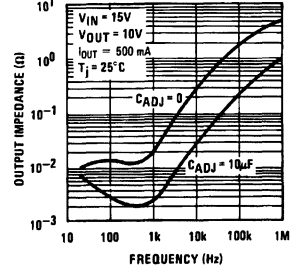
Ripple Rejection



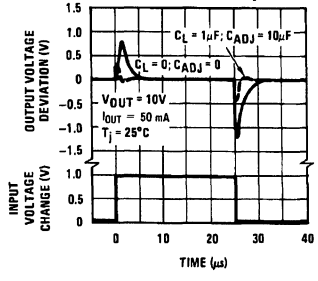
Ripple Rejection



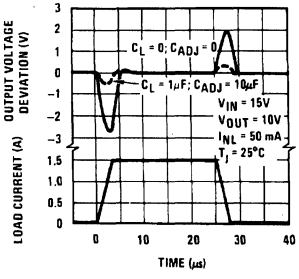
Output Impedance



Line Transient Response



Load Transient Response

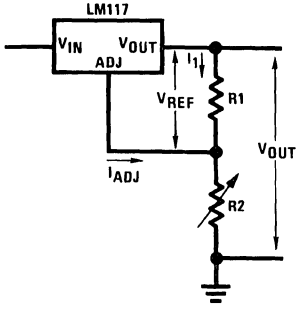


TL/H/9063–4

Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9063–5

FIGURE 1

Since the 100 μA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

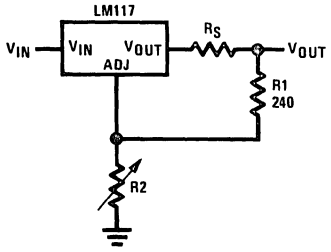
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 μF will merely improve the loop stability and output impedance.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9063–6

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

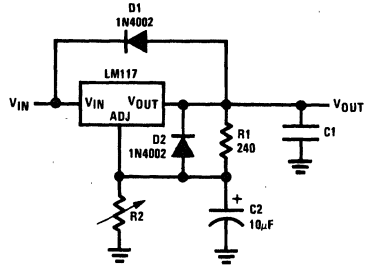
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

Application Hints (Continued)

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



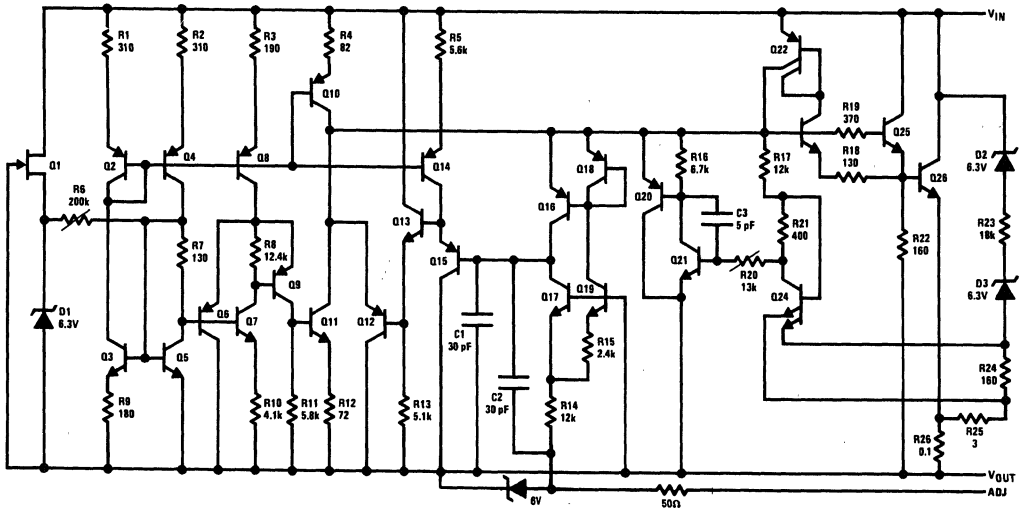
$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1
D2 protects against C2

TL/H/9063–7

FIGURE 3. Regulator with Protection Diodes

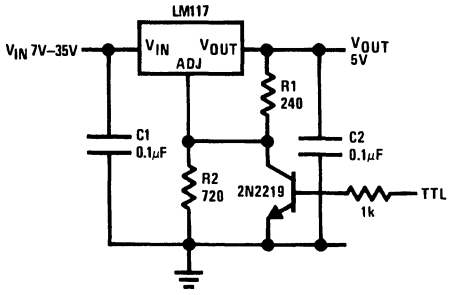
Schematic Diagram



TL/H/9063–8

Typical Applications (Continued)

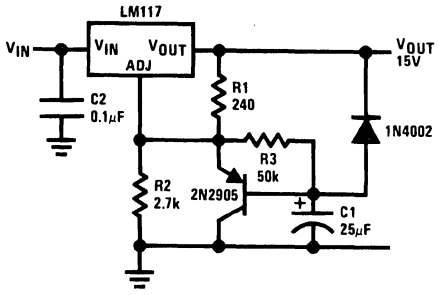
5V Logic Regulator with Electronic Shutdown*



*Min. output ≈ 1.2V

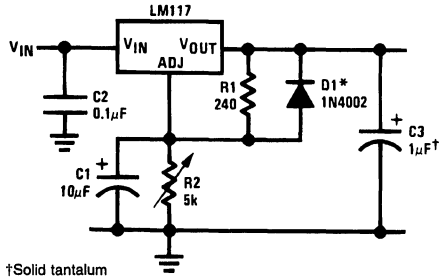
TL/H/9063-3

Slow Turn-On 15V Regulator



TL/H/9063-9

Adjustable Regulator with Improved Ripple Rejection

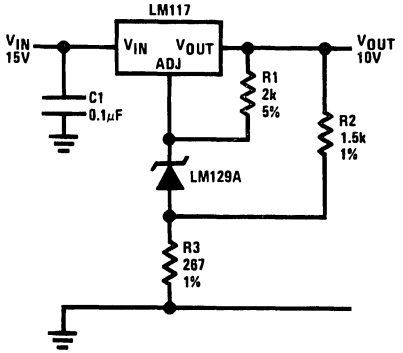


†Solid tantalum

*Discharges C1 if output is shorted to ground

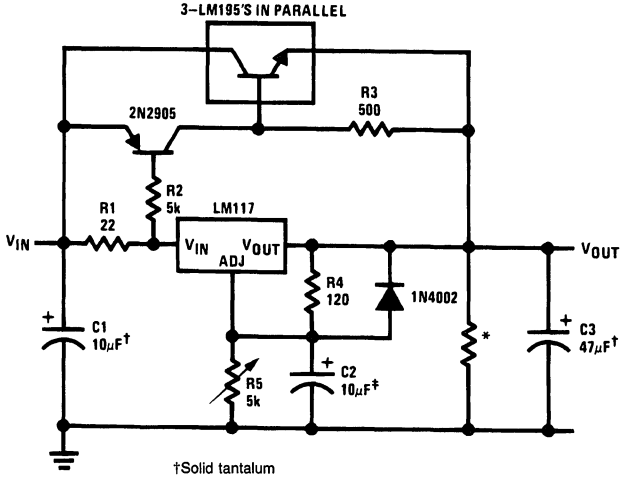
TL/H/9063-10

High Stability 10V Regulator



TL/H/9063-11

High Current Adjustable Regulator



†Solid tantalum

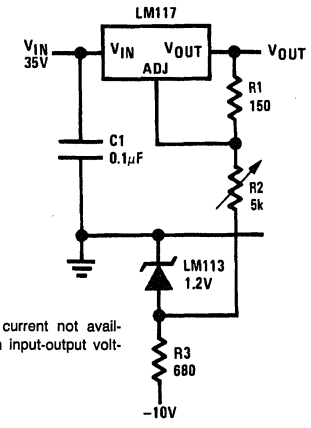
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

TL/H/9063-12

Typical Applications (Continued)

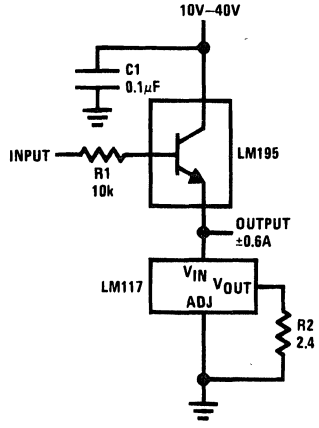
0 to 30V Regulator



Full output current not available at high input-output voltages

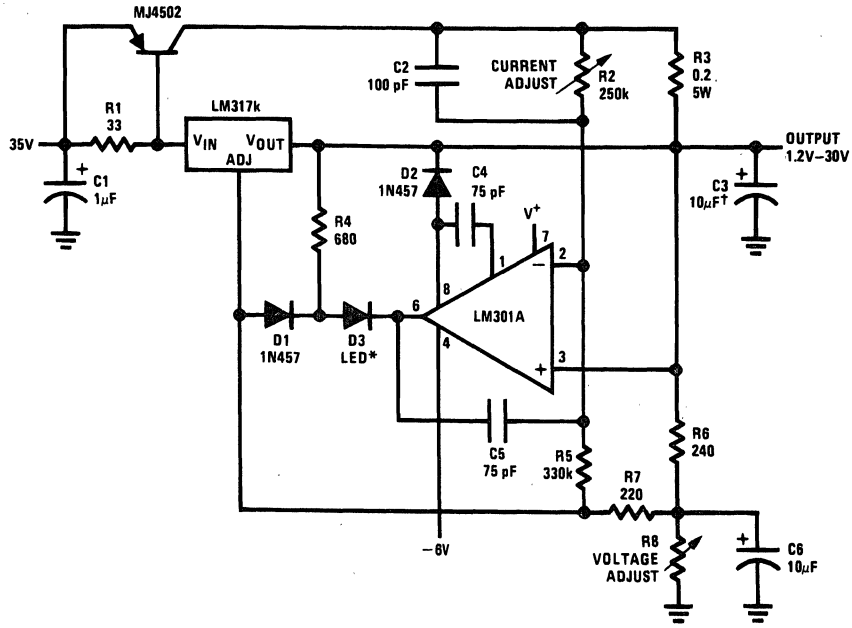
TL/H/9063–13

Power Follower



TL/H/9063–14

5A Constant Voltage/Constant Current Regulator



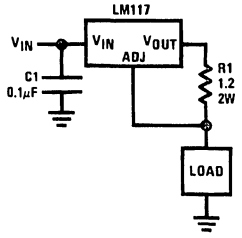
†Solid tantalum

*Lights in constant current mode

TL/H/9063–15

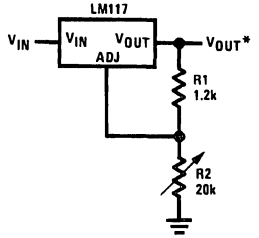
Typical Applications (Continued)

1A Current Regulator



TL/H/9063–16

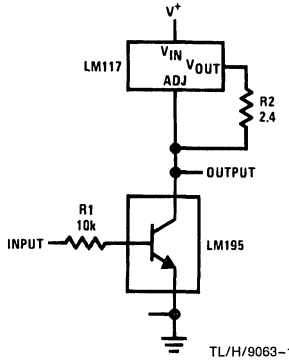
1.2V–20V Regulator with Minimum Program Current



TL/H/9063–17

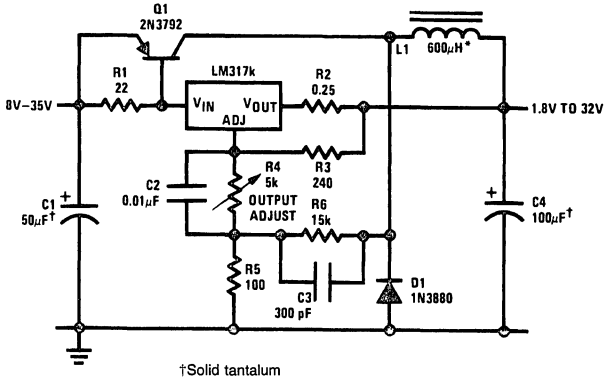
*Minimum load current ≈ 4 mA

High Gain Amplifier



TL/H/9063–18

Low Cost 3A Switching Regulator

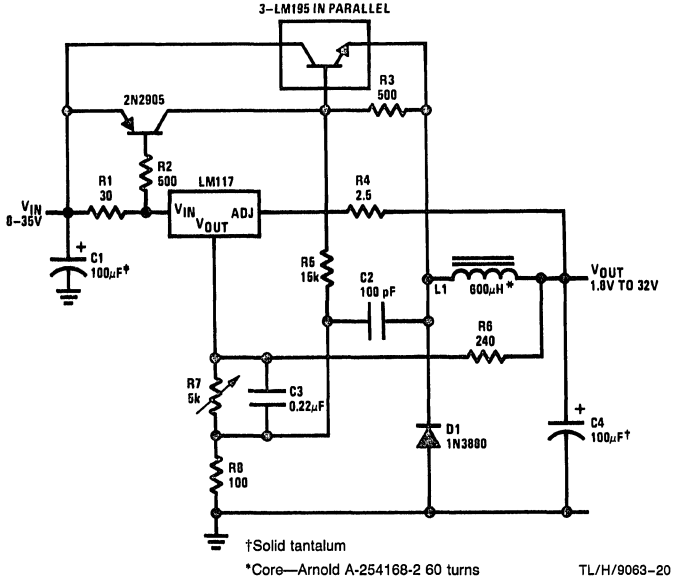


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063–19

4A Switching Regulator with Overload Protection

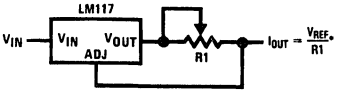


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9063–20

Precision Current Limiter

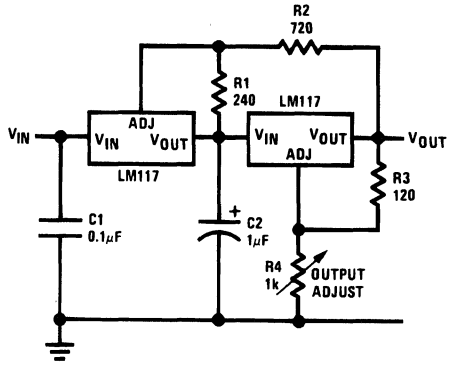


*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9063–21

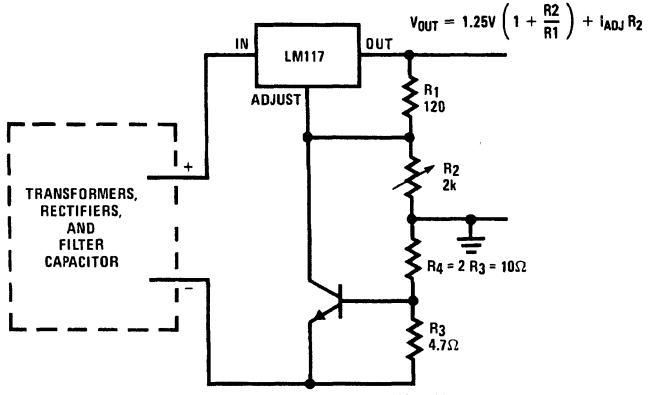
Typical Applications (Continued)

Tracking Preregulator



TL/H/9063–22

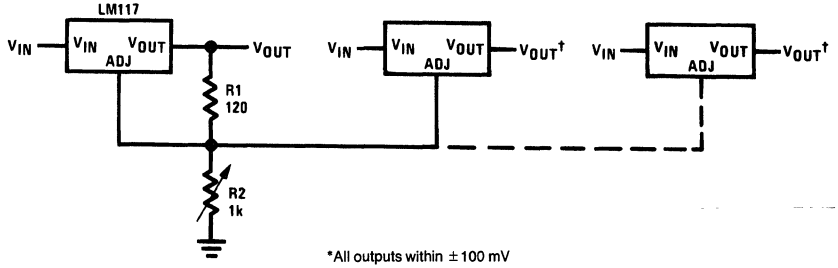
Current Limited Voltage Regulator



TL/H/9063–23

– Short circuit current is approximately $\frac{600\ mV}{R3}$, or 120 mA
(Compared to LM117's higher current limit)
– At 50 mA output only ¾ volt of drop occurs in R_3 and R_4

Adjusting Multiple On-Card Regulators with Single Control*

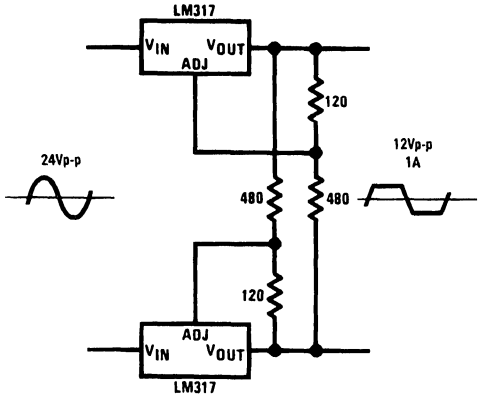


*All outputs within ±100 mV
†Minimum load—10 mA

TL/H/9063–24

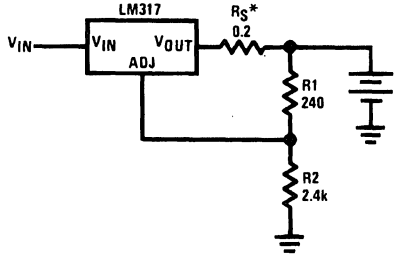
Typical Applications (Continued)

AC Voltage Regulator



TL/H/9063–25

12V Battery Charger

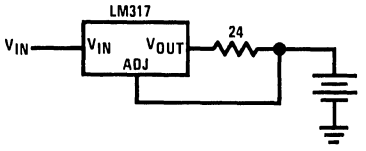


TL/H/9063–26

*R_S—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

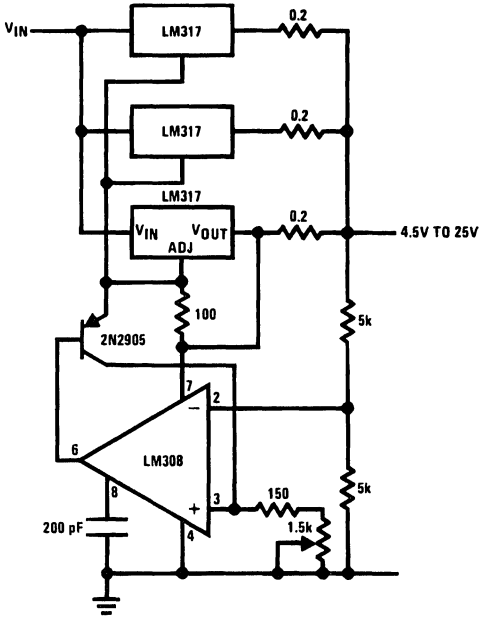
Use of R_S allows low charging rates with fully charged battery.

50 mA Constant Current Battery Charger



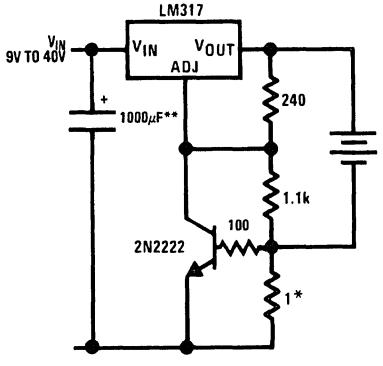
TL/H/9063–27

Adjustable 4A Regulator



TL/H/9063–28

Current Limited 6V Charger



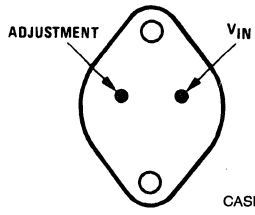
TL/H/9063–29

*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

Connection Diagrams (See Physical Dimension section for further information)

(TO-3)
Metal Can Package



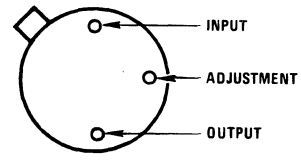
TL/H/9063–30

Bottom View

Steel Packages
Order Number LM117AK STEEL, LM117K STEEL, LM317AK STEEL or LM317K STEEL
See NS Package Number K02A

Aluminum Packages
Order Number LM317AKC or LM317KC
See NS Package Number KC02A

(TO-39)
Metal Can Package

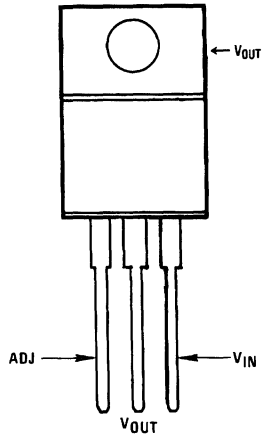


TL/H/9063–31

Bottom View

Order Number LM117AH, LM117H, LM317AH or LM317H
See NS Package Number H03A

(TO-220)
Plastic Package

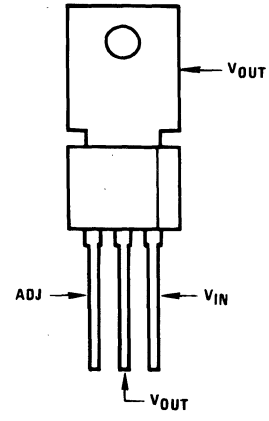


TL/H/9063–32

Front View

Order Number LM317AT or LM317T
See NS Package Number T03B

(TO-202)
Plastic Package



TL/H/9063–33

Front View

Order Number LM317MP
See NS Package Number P03A

National Semiconductor

LM117HV/LM317HV 3-Terminal Adjustable Regulator

General Description

The LM117HV/LM317HV are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 57V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117HV is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117HV series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117HV is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e. do not short the output to ground.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117HV can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

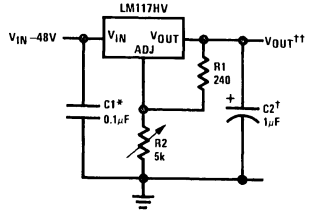
The LM117HVK STEEL, and LM317HVK STEEL are packaged in standard TO-3 transistor packages while the LM117HVH, and LM317HVH are packaged in a solid Kovar base TO-39 transistor package. The LM117HV is rated for operation from −55°C to +150°C, and the LM317HV from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–45V Adjustable Regulator



TL/H/9062-1

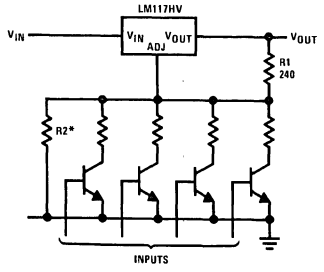
Full output current not available at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R_2$$

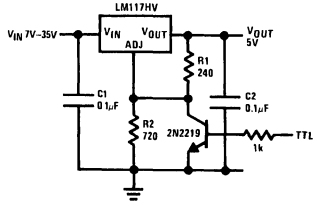
Digitally Selected Outputs



TL/H/9062-2

*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



TL/H/9062-3

*Min. output ≈ 1.2V

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 3)

Power Dissipation	Internally limited
Input—Output Voltage Differential	+60V, −0.3V
Operating Junction Temperature Range	
LM117HV	−55°C to +150°C
LM317HV	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Preconditioning Burn-In in Thermal Limit	100% All Devices
ESD Tolerance (Note 4)	2000V

Electrical Characteristics (Note 1)

Parameter	Conditions	LM117HV			LM317HV			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	T_J = 25°C, 3V ≤ V_{IN} − V_{OUT} ≤ 60V (Note 2) I_L = 10 mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	T_J = 25°C, 10 mA ≤ I_{OUT} ≤ I_{MAX}		0.1	0.3		0.1	0.5	%
Thermal Regulation	T_J = 25°C, 20 ms Pulse		0.03	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	10 mA ≤ I_L ≤ I_{MAX} 3.0 V ≤ (V_{IN} − V_{OUT}) ≤ 60V		0.2	5		0.2	5	μA
Reference Voltage	3.0 V ≤ (V_{IN} − V_{OUT}) ≤ 60V, (Note 3) 10 mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	3.0V ≤ (V_{IN} − V_{OUT}) ≤ 60V, I_L = 10 mA, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ I_{MAX} (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	T_{MIN} ≤ T_J ≤ T_{MAX}		1			1		%
Minimum Load Current	(V_{IN} − V_{OUT}) = 60V		3.5	7		3.5	12	mA
Current Limit	(V_{IN} − V_{OUT}) ≤ 15V							
	K Package	1.5	2.2	3.5	1.5	2.2	3.7	A
	H Package	0.5	0.8	1.8	0.5	0.8	1.9	A
	(V_{IN} − V_{OUT}) ≤ 60V							
	K Package		0.1			0.1		A
	H Package		0.03			0.03		A
RMS Output Noise, % of V_{OUT}	T_J = 25°C, 10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz		65			65		dB
	C_{ADJ} = 10 μF	66	80		66	80		dB
Long-Term Stability	T_J = 125°C		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
Thermal Resistance, Junction to Ambient (no heat sink)	H Package		140			140		°C/W
	K Package		35			35		°C/W

Note 1: Unless otherwise specified, these specifications apply: −55°C ≤ T_J ≤ +150°C for the LM117HV, and 0°C ≤ T_J ≤ +125°C for the LM317HV; V_{IN} − V_{OUT} = 5V and I_{OUT} = 0.1A for the TO-39 package and I_{OUT} = 0.5A for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 and 0.5A for the TO-39 package.

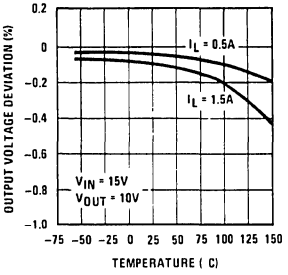
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Note 3: Refer to RETS117HVH for LM117HVH or RETS117HVK for LM117HVK military specificatioins.

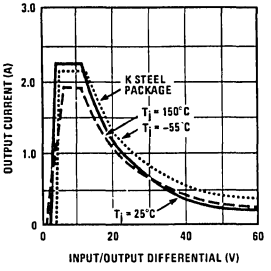
Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics (K Package)

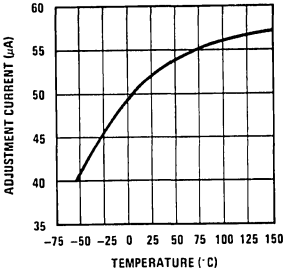
Load Regulation



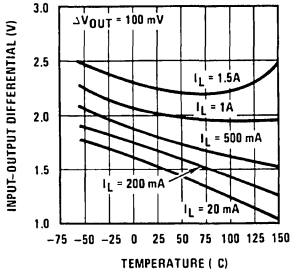
Current Limit



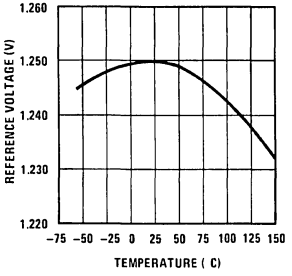
Adjustment Current



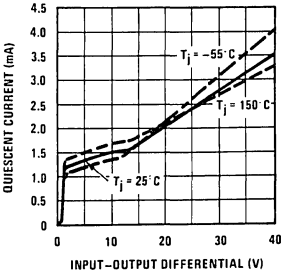
Dropout Voltage



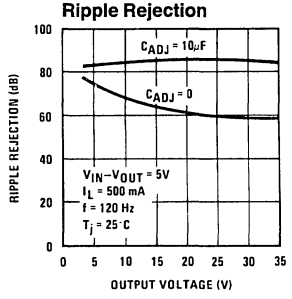
Temperature Stability



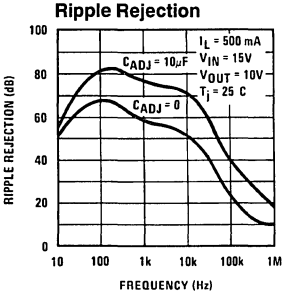
Minimum Operating Current



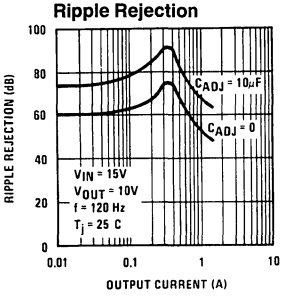
Ripple Rejection



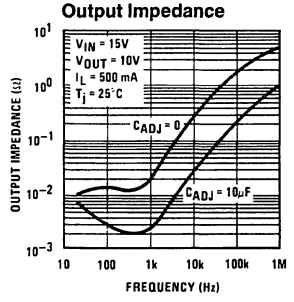
Ripple Rejection



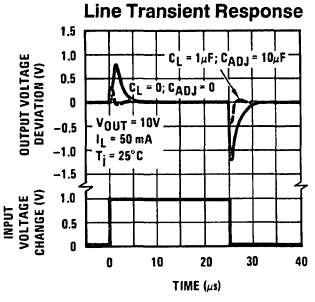
Ripple Rejection



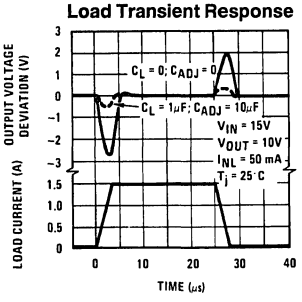
Output Impedance



Line Transient Response



Load Transient Response

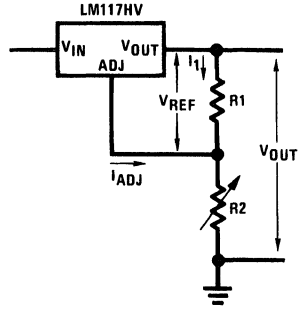


TL/H/9062–4

Application Hints

In operation, the LM117HV develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/9062–5

FIGURE 1

Since the 100 μA current from the adjustment terminal represents an error term, the LM117HV was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM117HV to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

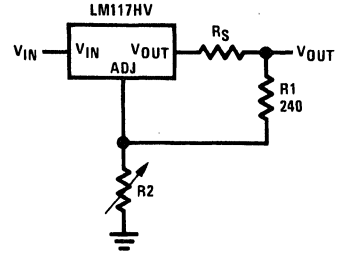
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM117HV is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of load capacitance larger than 10 μF will merely improve the loop stability and output impedance.

Load Regulation

The LM117HV is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9062–6

FIGURE 2. Regulator with Line Resistance in Output Lead

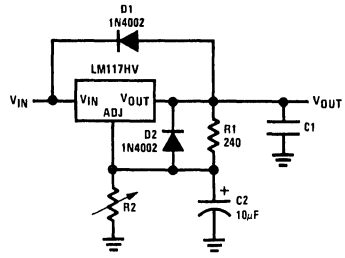
With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117HV, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117HV is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM117HV with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



TL/H/9062–7

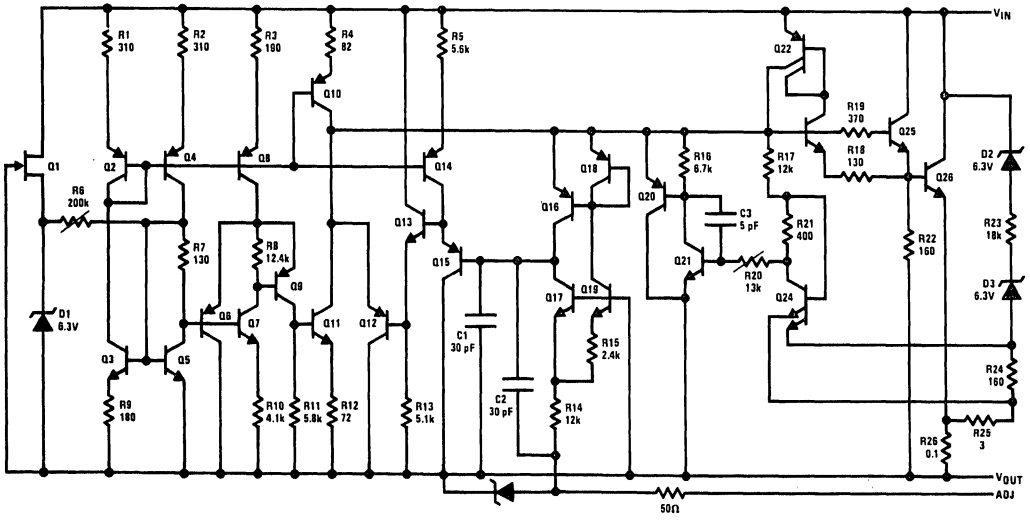
FIGURE 3. Regulator with Protection Diodes

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1

D2 protects against C2

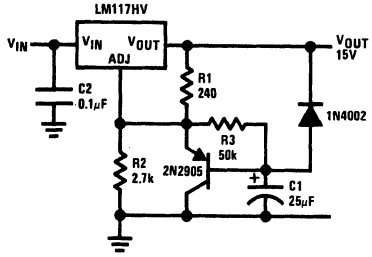
Schematic Diagram



TL/H/9062–8

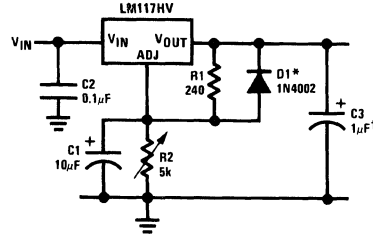
Typical Applications (Continued)

Slow Turn-On 15V Regulator



TL/H/9062–9

Adjustable Regulator with Improved Ripple Rejection

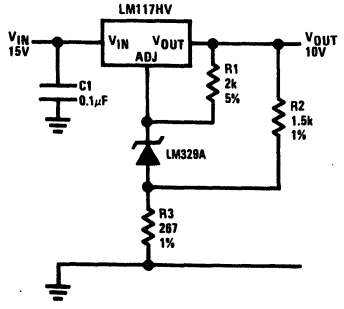


TL/H/9062–10

†Solid tantalum

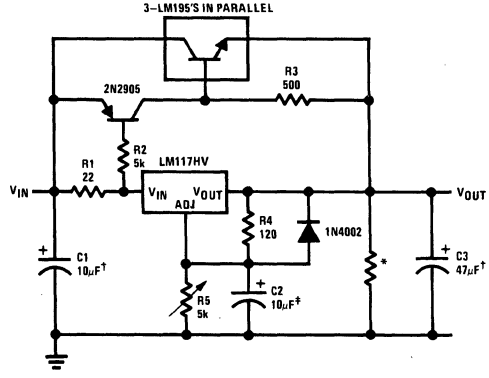
*Discharges C1 if output is shorted to ground

High Stability 10V Regulator



TL/H/9062–11

High Current Adjustable Regulator



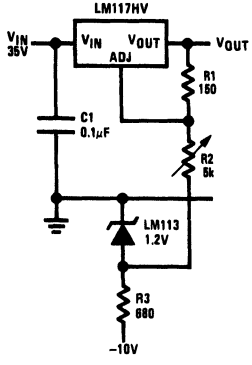
TL/H/9062–12

†Solid tantalum

*Minimum load current = 30 mA

‡Optional—improves ripple rejection

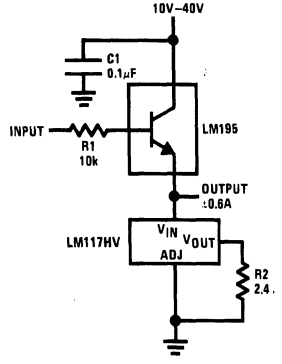
0 to 30V Regulator



TL/H/9062–13

Full output current not available at high input-output voltages

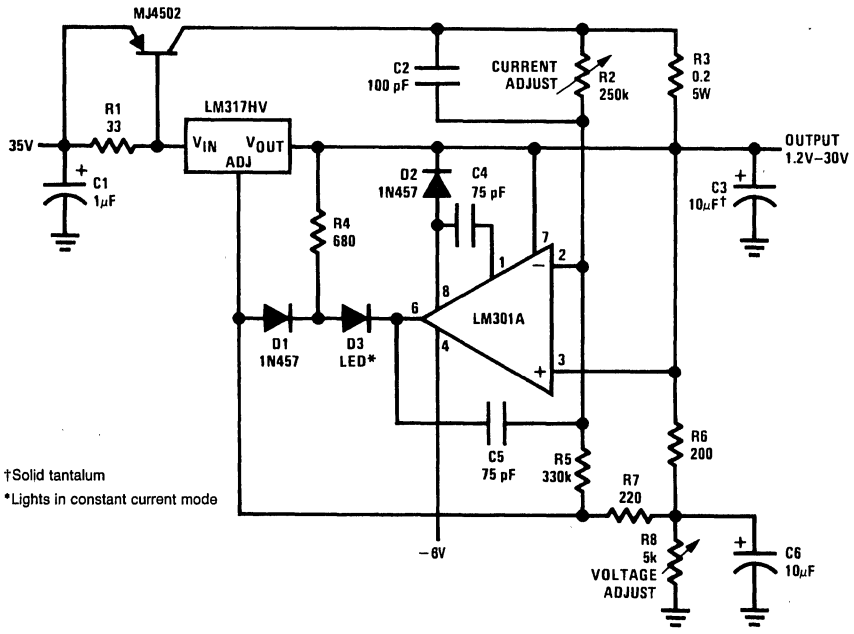
Power Follower



TL/H/9062–14

Typical Applications (Continued)

5A Constant Voltage/Constant Current Regulator

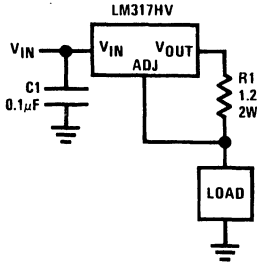


†Solid tantalum

*Lights in constant current mode

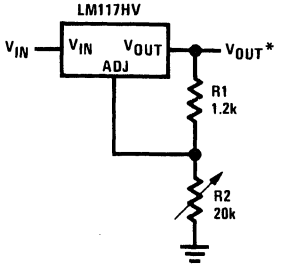
TL/H/9062–15

1A Current Regulator



TL/H/9062–16

1.2V–20V Regulator with Minimum Program Current

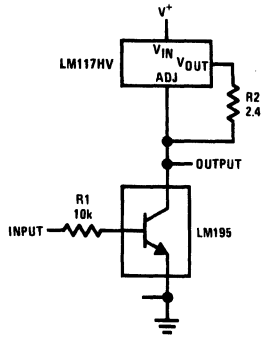


TL/H/9062–17

*Minimum load current ≈ 4 mA

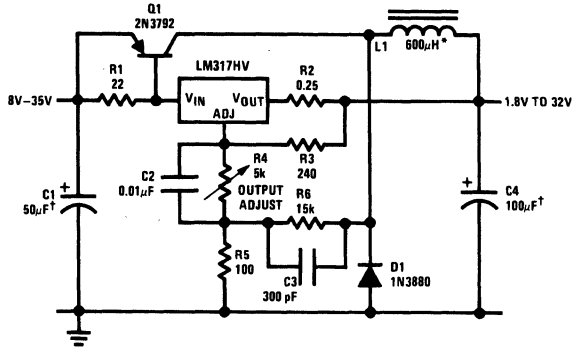
Typical Applications (Continued)

High Gain Amplifier



TL/H/9062–18

Low Cost 3A Switching Regulator

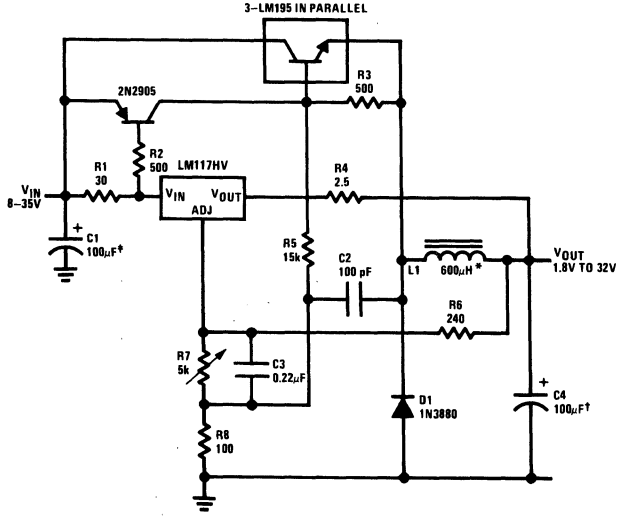


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–19

4A Switching Regulator with Overload Protection

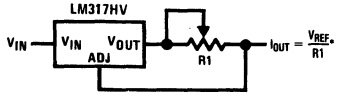


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

TL/H/9062–20

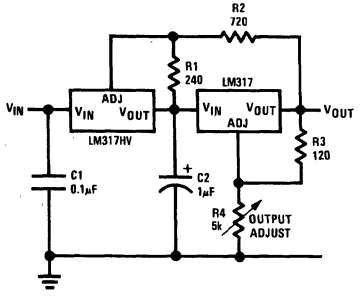
Precision Current Limiter



TL/H/9062–21

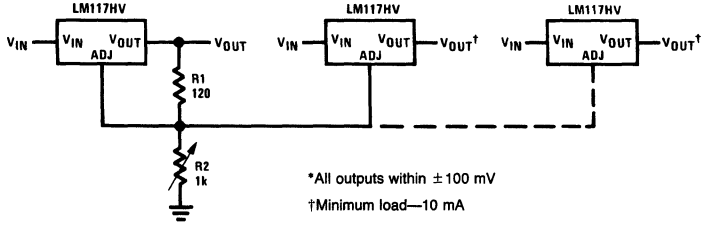
*0.8Ω ≤ R1 ≤ 120Ω

Tracking Preregulator



TL/H/9062–22

Adjustable Multiple On-Card Regulators with Single Control*



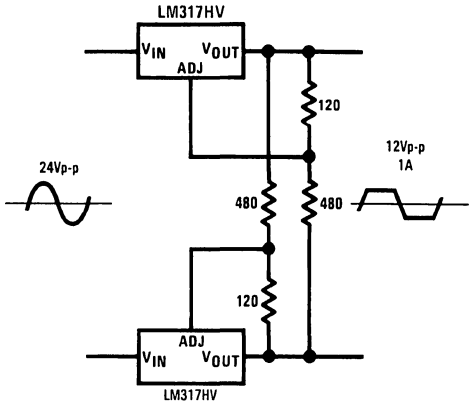
*All outputs within ±100 mV

†Minimum load—10 mA

TL/H/9062–23

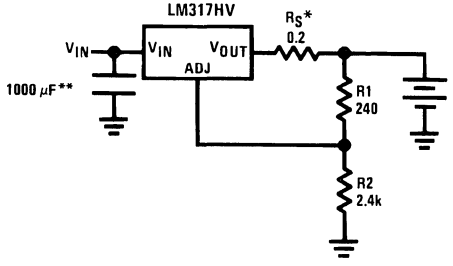
Typical Applications (Continued)

AC Voltage Regulator



TL/H/9062-24

12V Battery Charger



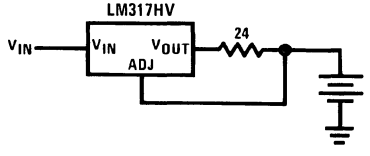
TL/H/9062-25

*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

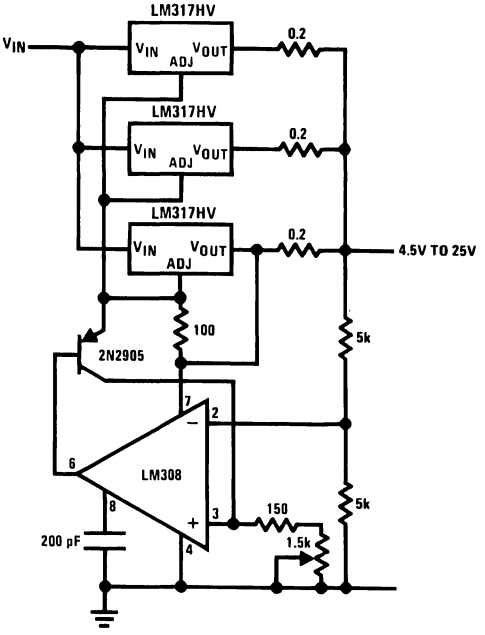
**The 1000 μF is recommended to filter out input transients

50 mA Constant Current Battery Charger



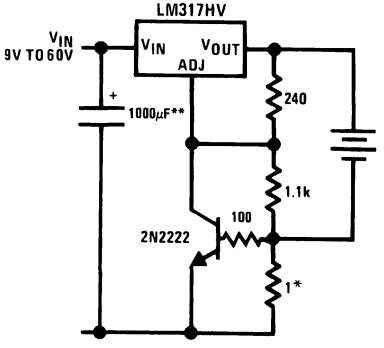
TL/H/9062-26

Adjustable 4A Regulator



TL/H/9062-27

Current Limited 6V Charger



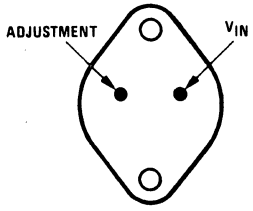
TL/H/9062-28

*Sets peak current (0.6A for 1Ω)

**The 1000 μF is recommended to filter out input transients

Connection Diagrams (See Physical Dimension section for further information)

(TO-3 Steel)
Metal Can Package

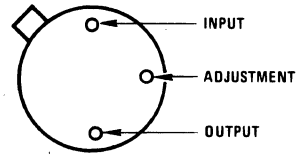


TL/H/9062–29

Case is Output
Bottom View

Order Number LM117HVK STEEL,
LM317HVK STEEL
See NS Package Number K02A

(TO-39)
Metal Can Package



TL/H/9062–30

Case is Output
Bottom View

Order Number LM117HVH,
or LM317HVH
See NS Package Number H03A

National Semiconductor

LM120/LM320
Series 3-Terminal Negative Regulators

General Description

The LM120 series are three-terminal negative regulators with a fixed output voltage of −5V, −12V, and −15V, and up to 1.5A load current capability. Where other voltages are required, the LM137 and LM137HV series provide an output voltage range of −1.2V to −47V.

The LM120 need only one external component—a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

Features

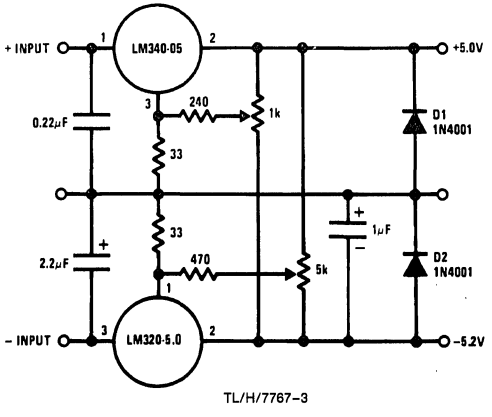
- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- Low temperature drift
- Easily adjustable to higher output voltage

LM120 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM120/LM320	TO-3 (K)	20W	1.5A
	TO-39 (H)	2W	0.5A
LM320	TO-220 (T)	15W	1.5A
LM320M	TO-202 (P)	7.5W	0.5A

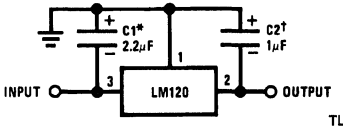
Typical Applications

Dual Trimmed Supply



TL/H/7767–3

Fixed Regulator



TL/H/7767–2

*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may substituted. Values given may be increased without limit.

For output capacitance in excess of 100 μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

−5 Volt Regulators (Note 3)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Power Dissipation	Internally Limited
Input Voltage	−25V
Input-Output Voltage Differential	25V
Junction Temperatures	See Note 1
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic	260°C

Electrical Characteristics

Order Numbers		Metal Can Package												Power Plastic Package						Units
		LM120K-5.0 (TO-3)			LM320K-5.0 (TO-3)			LM120H-5.0 (TO-39)			LM320H-5.0 (TO-39)			LM320T-5.0 (TO-220)			LM320MP-5.0 (TO-202)			
Design Output Current (I_D) Device Dissipation (P_D)		1.5A 20W			1.5A 20W			0.5A 2W			0.5A 2W			1.5A 15W			0.5A 7.5W			
Parameter	Conditions (Note 1)	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage	T_J = 25°C, V_{IN} = 10V, I_{LOAD} = 5 mA	−5.1	−5	−4.9	−5.2	−5	−4.8	−5.1	−5	−4.9	−5.2	−5	−4.8	−5.2	−5	−4.8	−5.2	−5	−4.8	V
Line Regulation	T_J = 25°C, I_{LOAD} = 5 mA, $V_{MIN} \le V_{IN} \le V_{MAX}$		10	25		10	40		10	25		10	40		10	40		10	40	mV
Input Voltage		−25		−7	−25		−7	−25		−7	−25		−7	−25		−7.5	−25		−7.5	V
Ripple Rejection	f = 120 Hz	54	64		54	64		54	64		54	64		54	64		54	64		dB
Load Regulation, (Note 2)	T_J = 25°C, V_{IN} = 10V, 5 mA $\le I_{LOAD} \le I_D$		50	75		60	100		30	50		30	50		50	100		40	100	mV
Output Voltage, (Note 1)	−7.5V $\le V_{IN} \le V_{MAX}$, 5 mA $\le I_{LOAD} \le I_D$, $P \le P_D$	−5.20		−4.80	−5.25		−4.75	−5.20		−4.80	−5.25		−4.75	−5.25		−4.75	−5.25	−5	−4.75	V
Quiescent Current	$V_{MIN} \le V_{IN} \le V_{MAX}$		1	2		1	2		1	2		1	2		1	2		1	2	mA
Quiescent Current Change	T_J = 25°C $V_{MIN} \le V_{IN} \le V_{MAX}$ 5 mA $\le I_{LOAD} \le I_D$		0.1 0.1	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.04	0.4 0.4		0.05 0.04	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.04	0.3 0.25	mA mA
Output Noise Voltage	T_A = 25°C, C_L = 1 μF, I_L = 5 mA, V_{IN} = 10V, 10 Hz ≤ f ≤ 100 kHz		150			150			150			150			150			150		μV
Long Term Stability			5	50		5	50		5	50		5	50		10			10		mV
Thermal Resistance Junction to Case Junction to Ambient				3 35			3 35			Note 4 Note 4			Note 4 Note 4		4 50			12 70		°C/W °C/W

Note 1: This specification applies over −55°C ≤ T_J ≤ +150°C for the LM120 and 0°C ≤ T_J ≤ +125°C for the LM320.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to P_D.

Note 3: For −5V 3 amp regulators, see LM145 data sheet.

Note 4: Thermal resistance of typically 85°C/W (in 400 linear feet air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

Note 5: Refer to RETS120-5H drawing for LM120H-5.0 or RETS120-5K drawing for LM120-5K military specifications.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input Voltage	−35V
Input-Output Voltage Differential	30V
Junction Temperatures	See Note 1
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Order Numbers		Metal Can Package												Power Plastic Package						Units
		LM120K-12 (TO-3)			LM320K-12 (TO-3)			LM120H-12 (TO-39)			LM320H-12 (TO-39)			LM320T-12 (TO-220)			LM320MP-12 (TO-202)			
Design Output Current (I_D) Device Dissipation (P_D)		1A 20W			1A 20W			0.2A 2W			0.2A 2W			1A 15W			0.5A 7.5W			
Parameter	Conditions (Note 1)	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage	T_J = 25°C, V_{IN} = 17V, I_{LOAD} = 5 mA	−12.3	−12	−11.7	−12.4	−12	−11.6	−12.3	−12	−11.7	−12.4	−12	−11.6	−12.4	−12	−11.6	−12.5	−12	−11.5	V
Line Regulation	T_J = 25°C, I_{LOAD} = 5 mA, $V_{MIN} \le V_{IN} \le V_{MAX}$		4	10		4	20		4	10		4	20		4	20		4	24	mV
Input Voltage		−32		−14	−32		−14	−32		−14	−32		−14	−32		−14.5	−32		−14.5	V
Ripple Rejection	f = 120 Hz	56	80		56	80		56	80		56	80		56	80		56	80		dB
Load Regulation, (Note 2)	T_J = 25°C, V_{IN} = 17V, 5 mA $\le I_{LOAD} \le I_D$		30	80		30	80		10	25		10	40		30	80		40	100	mV
Output Voltage, (Note 1)	14.5V $\le V_{IN} \le V_{MAX}$, 5 mA $\le I_{LOAD} \le I_D$, $P \le P_D$	−12.5		−11.5	−12.6		−11.4	−12.5		−11.5	−12.6		−11.4	−12.6		−11.4	−12.6		−11.4	V
Quiescent Current	$V_{MIN} \le V_{IN} \le V_{MAX}$		2	4		2	4		2	4		2	4		2	4		2	4	mA
Quiescent Current Change	T_J = 25°C $V_{MIN} \le V_{IN} \le V_{MAX}$ 5 mA $\le I_{LOAD} \le I_D$		0.1 0.1	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.03	0.4 0.4		0.05 0.03	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.04	0.3 0.25	mA mA
Output Noise Voltage	T_A = 25°C, C_L = 1 μF, I_L = 5 mA, V_{IN} = 17V, 10 Hz ≤ f ≤ 100 kHz		400			400			400			400			400			400		μV
Long Term Stability			12	120		12	120		12	120		12	120		24			24		mV
Thermal Resistance Junction to Case Junction to Ambient				 3 35			 3 35			 Note 3 Note 3			 Note 3 Note 3			 4 50			 12 70		 °C/W °C/W

Note 1: This specification applies over −55°C ≤ T_J ≤ +150°C for the LM120 and 0°C ≤ T_J ≤ +125°C for the LM320.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to P_D.

Note 3: Thermal resistance of typically 85°C/W (in 400 linear feet/min air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

Note 4: Refer to RETS120H-12 drawing for LM120H-12 or RETS120-12K drawing for LM120K-12 military specifications.

−15 Volt Regulators

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input Voltage	
LM120/LM320	−40V
LM320T/LM320MP	−35V
Input-Output Voltage Differential	30V
Junction Temperatures	See Note 1
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Order Numbers		Metal Can Package												Power Plastic Package						Units
		LM120K-15 (TO-3)			LM320K-15 (TO-3)			LM120H-15 (TO-39)			LM320H-15 (TO-39)			LM320T-15 (TO-220)			LM320MP-15 (TO-202)			
Design Output Current (I_D) Device Dissipation (P_D)		1A 20W			1A 20W			0.2A 2W			0.2A 2W			1A 15W			0.5A 7.5W			
Parameter	Conditions (Note 1)	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage	T_J = 25°C, V_{IN} = 20V, I_{LOAD} = 5 mA	−15.3	−15	−14.7	−15.4	−15	−14.6	−15.3	−15	−14.7	−15.4	−15	−14.6	−15.5	−15	−14.5	−15.6	−15	−14.4	V
Line Regulation	T_J = 25°C, I_{LOAD} = 5 mA, $V_{MIN} \le V_{IN} \le V_{MAX}$		5	10		5	20		5	10		5	20		5	20		5	30	mV
Input Voltage		−35		−17	−35		−17	−35		−17	−35		−17	−35		−17.5	−35		−17.5	V
Ripple Rejection	f = 120 Hz	56	80		56	80		56	80		56	80		56	80		56	80		dB
Load Regulation, (Note 2)	T_J = 25°C, V_{IN} = 20V, 5 mA ≤ I_{LOAD} ≤ I_D		30	80		30	80		10	25		10	40		30	80		40	100	mV
Output Voltage, (Note 1)	17.5V ≤ V_{IN} ≤ V_{MAX}, 5 mA ≤ I_{LOAD} ≤ I_D, P ≤ P_D	−15.5		−14.5	−15.6		−14.4	−15.5		−14.5	−15.6		−14.4	−15.7		−14.3	−15.7		−14.3	V
Quiescent Current	$V_{MIN} \le V_{IN} \le V_{MAX}$		2	4		2	4		2	4		2	4		2	4		2	4	mA
Quiescent Current Change	T_J = 25°C $V_{MIN} \le V_{IN} \le V_{MAX}$ 5 mA ≤ I_{LOAD} ≤ I_D		0.1 0.1	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.03	0.4 0.4		0.05 0.03	0.4 0.4		0.1 0.1	0.4 0.4		0.05 0.04	0.3 0.25	mA mA
Output Noise Voltage	T_A = 25°C, C_L = 1 μF, I_L = 5 mA, V_{IN} = 20V, 10 Hz ≤ f ≤ 100 kHz		400			400			400			400			400			400		μV
Long Term Stability			15	150		15	150		15	150		15	150		30			30		mV
Thermal Resistance Junction to Case Junction to Ambient				 3 35			 3 35			 Note 3 Note 3			 Note 3 Note 3			 4 50			 12 70		°C/W °C/W

Note 1: This specification applies over −55°C ≤ T_J ≤ +150°C for the LM120 and 0°C ≤ T_J ≤ +125°C for the LM320.

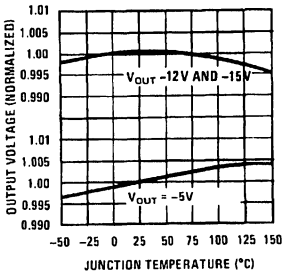
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, low duty cycle, pulse testing is used. The LM120/LM320 series does have low thermal feedback, improving line and load regulation. On all other tests, even though power dissipation is internally limited, electrical specifications apply only up to P_D.

Note 3: Thermal resistance of typically 85°C/W (in 400 linear feet/min air flow), 224°C/W (in static air) junction to ambient, of typically 21°C/W junction to case.

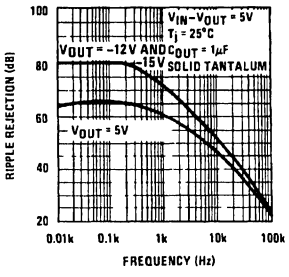
Note 4: Refer to RETS120-15H drawing for LM120H-15 or RETS120-15K drawing for LM120K-15 military specifications.

Typical Performance Characteristics

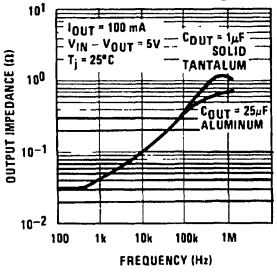
Output Voltage vs Temperature



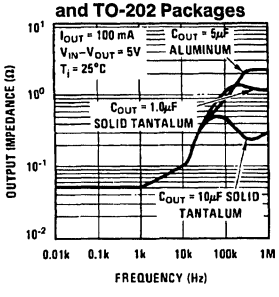
Ripple Rejection (All Types)



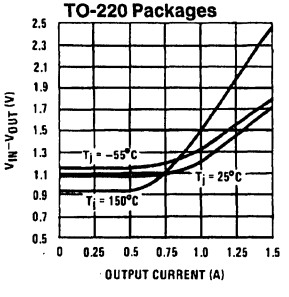
Output Impedance TO-3 and TO-220 Packages



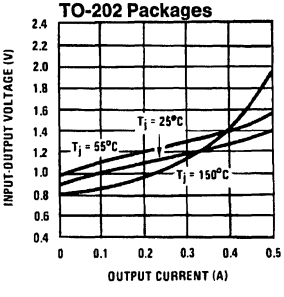
Output Impedance TO-5 and TO-202 Packages



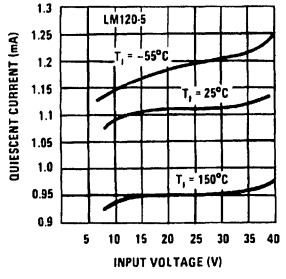
Minimum Input-Output Differential TO-3 and TO-220 Packages



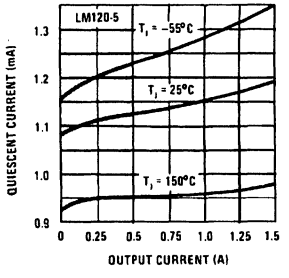
Minimum Input-Output Differential TO-5 and TO-202 Packages



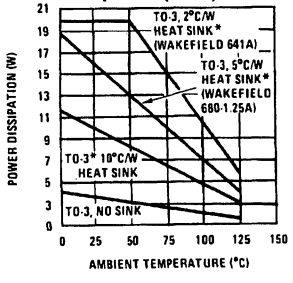
Quiescent Current vs Input Voltage



Quiescent Current vs Load Current



Maximum Average Power Dissipation (TO-3)

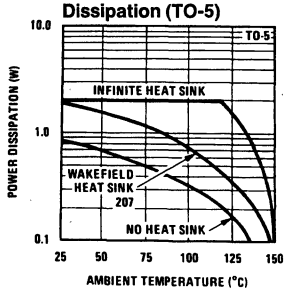


TL/H/7767–4

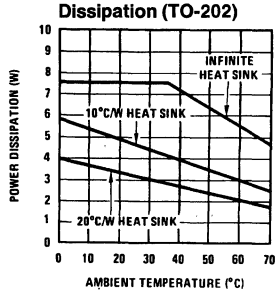
*These curves for LM120.
Derate 25°C further for LM320.

Typical Performance Characteristics (Continued)

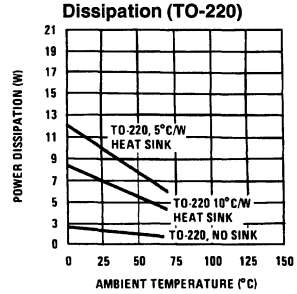
Maximum Average Power Dissipation (TO-5)



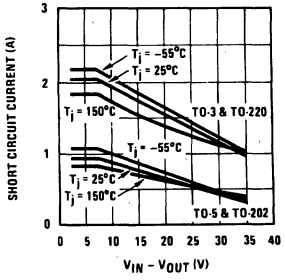
Maximum Average Power Dissipation (TO-202)



Maximum Average Power Dissipation (TO-220)



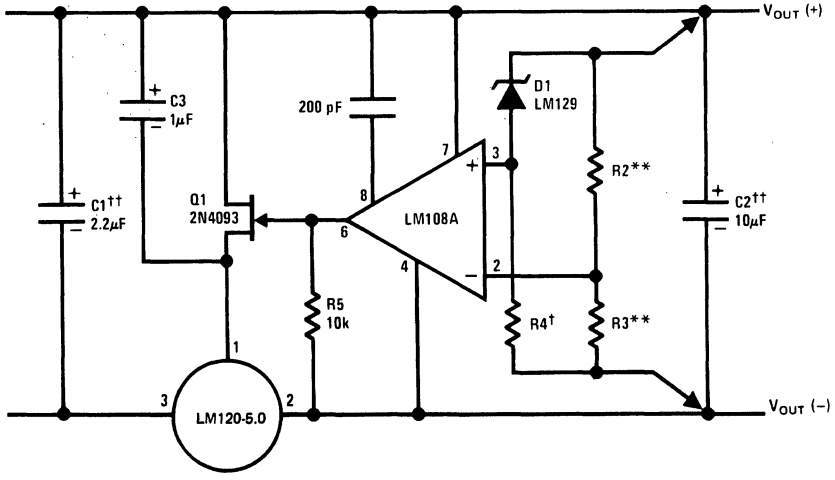
Short Circuit Current



TL/H/7767–5

Typical Applications (Continued)

High Stability 1 Amp Regulator



TL/H/7767–6

Lead and line regulation — 0.01% temperature stability — 0.2%

†Determines Zener current.

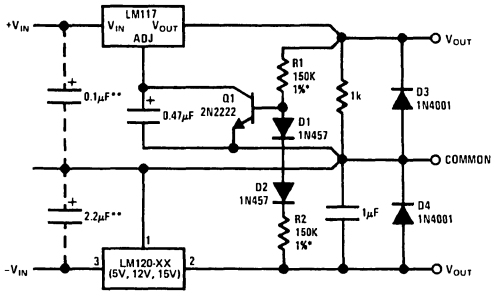
††Solid tantalum.

An LM120-12 or LM120-15 may be used to permit higher input voltages, but the regulated output voltage must be at least −15V when using the LM120-12 and −18V for the LM120-15.

**Select resistors to set output voltage. 2 ppm/°C tracking suggested.

Typical Applications (Continued)

Wide Range Tracking Regulator



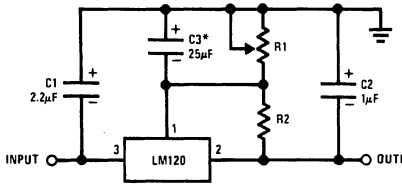
TL/H/7767–7

*Resistor tolerance of R1 and R2 determine matching of (+) and (−) inputs.

**Necessary only if raw supply capacitors are more than 3″ from regulators

An LM3086N array may substitute for Q1, D1 and D2 for better stability and tracking. In the array diode transistors Q5 and Q4 (in parallel) make up D2; similarly, Q1 and Q2 become D1 and Q3 replaces the 2N2222.

Variable Output



TL/H/7767–9

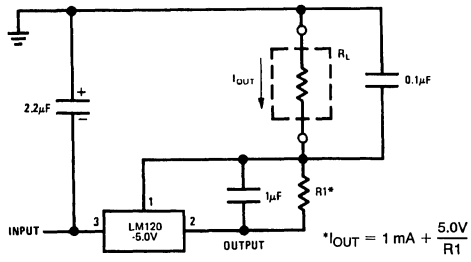
*Optional. Improves transient response and ripple rejection.

$$V_{OUT} = V_{SET}\frac{R1+R2}{R2}$$

SELECT R2 AS FOLLOWS:

LM120-5	**−300Ω**
LM120-12	**−750Ω**
LM120-15	**−1k**

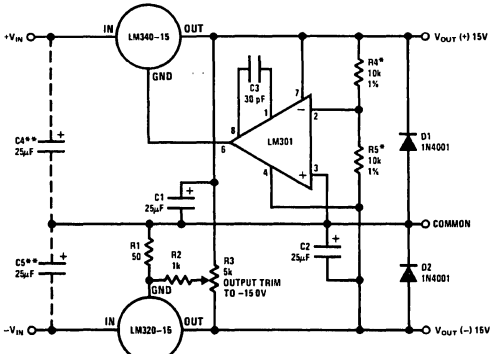
Current Source



$$*I_{OUT} = 1\ mA + \frac{5.0V}{R1}$$

TL/H/7767–8

±15V, 1 Amp Tracking Regulators



TL/H/7767–12

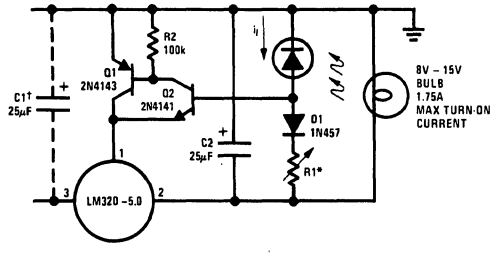
Performance (Typical)

Load Regulation at ΔI_L = 1A	10 mV	1 mV
Output Ripple, C_{IN} = 3000 μF, I_L = 1A	100 μVrms	100 μVrms
Temperature Stability	+50 mV	+50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150 μVrms	150 μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 2″ from regulators.

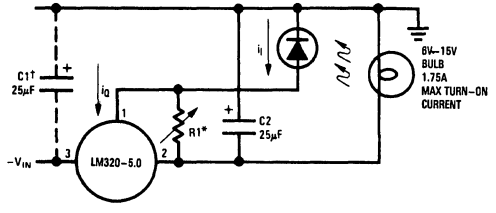
Light Controllers Using Silicon Photo Cells



TL/H/7767–10

*Lamp brightness increases until i_l = 5V/R1 (i_l can be set as low as 1 μA).

†Necessary only of raw supply filter capacitor is more than 2″ from LM320MP.

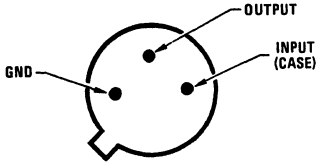


TL/H/7767–11

*Lamp brightness increases until $i_l = i_Q$ (1 mA) + 5V/R1.

†Necessary only if raw supply filter capacitor is more than 2″ from LM320.

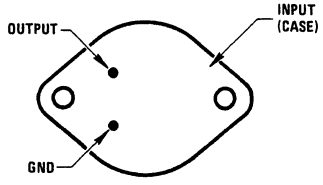
Connection Diagrams



TL/H/7767–13

Bottom View

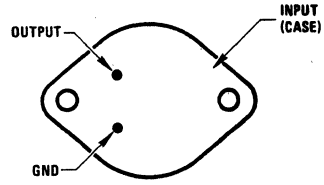
Metal Can Package TO-39 (H)
Order Number LM120H-5.0, LM120H-12, LM120H-15, LM320H-5.0, LM320H-12 or LM320H-15
See NS Package Number H03A



TL/H/7767–14

Bottom View

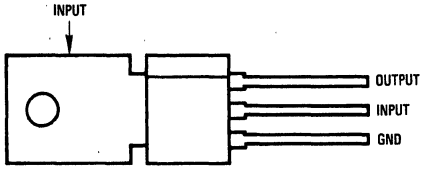
Steel Metal Can Package TO-3 (K)
Order Number LM120K-5.0, LM120K-12, LM120K-15, LM320K-5.0, LM320K-12 or LM320K-15
See NS Package Number K02A



TL/H/7767–15

Bottom View

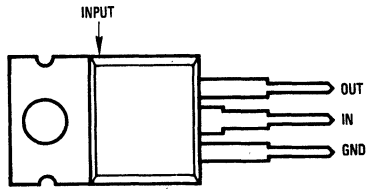
Aluminum Metal Can Package TO-3 (KC)
Order Number LM320KC-5.0, LM320KC-12 or LM320KC-15
See NS Package Number KC02A



TL/H/7767–16

Front View

Power Package TO-202 (P)
Order Number LM320MP-5.0, LM320MP-12 or LM320MP-15
See NS Package Number P03A

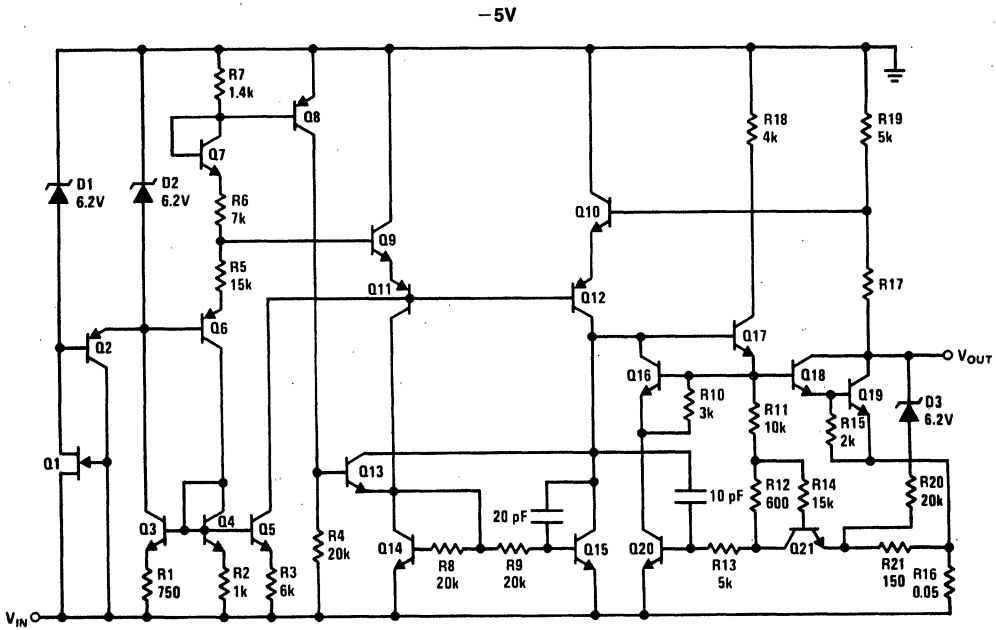


TL/H/7767–17

Front View

Power Package TO-220 (T)
Order Number LM320T-5.0, LM320T-12 or LM320T-15
See NS Package Number T03B

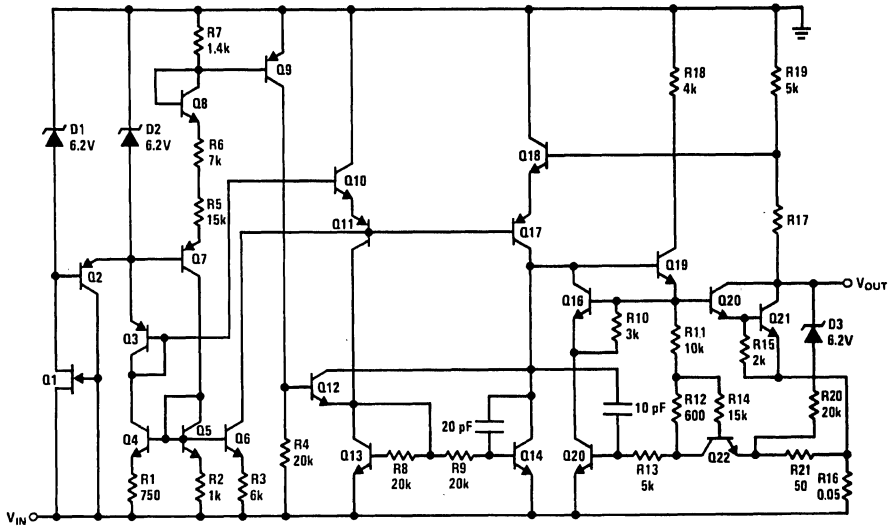
Schematic Diagrams



TL/H/7767–18

Schematic Diagrams (Continued)

−12V and −15V



TL/H/7767–19

National Semiconductor

LM123A/LM123/LM323A/LM323 3-Amp, 5-Volt Positive Regulator

General Description

The LM123 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The LM123A and LM323A offer improved precision over the standard LM123 and LM323. Parameters with tightened specifications include output voltage tolerance, line regulation, and load regulation.

The 3 amp regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1 amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1 μF solid tantalum capacitor should be used on the input. A 0.1 μF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature, and power dissipation ensure that the LM123 will perform satisfactorily as a system element.

For applications requiring other voltages, see LM150 series adjustable regulator data sheet.

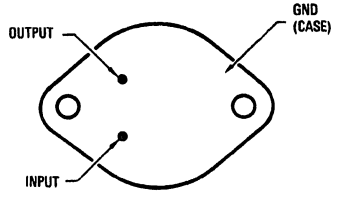
Operation is guaranteed over the junction temperature range −55°C to +150°C for LM123A/LM123, −40°C to +125°C for LM323A, and 0°C to +125°C for LM323. A hermetic TO-3 package is used for high reliability and low thermal resistance.

Features

- Guaranteed 1% initial accuracy (A version)
- 3 amp output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5V minimum input voltage
- 30W power dissipation
- 100% electrical burn-in

Connection Diagram

Metal Can Package

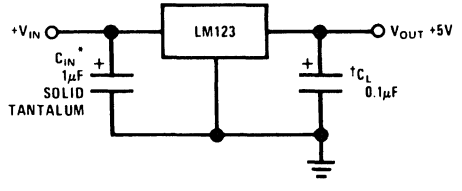


TL/H/7771–2

Order Number LM123AK STEEL, LM123K STEEL, LM323AK STEEL or LM323K STEEL
See NS Package Number K02A

Typical Applications

Basic 3 Amp Regulator



TL/H/7771–3

*Required if LM123 is more than 4" from filter capacitor.

†Regulator is stable with no load capacitor into resistive loads.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Input Voltage	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM123A, LM123	−55°C to +150°C
LM323A	−40°C to +125°C
LM323	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Tolerance (Note 5)	2000V

Preconditioning

Burn-In in Thermal Limit **100% All Devices**

LM123A/LM123 Electrical Characteristics (Note 1)

Parameter	Conditions	LM123A			LM123			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	$T_j = 25°C$ $V_{IN} = 7.5V$, $I_{OUT} = 0A$	4.95	5	5.05	4.7	5	5.3	V
	$7.5V \le V_{IN} \le 15V$ $0A \le I_{OUT} \le 3A$, $P \le 30W$	4.85		5.15	4.6		5.4	V
Line Regulation (Note 3)	$T_j = 25°C$ $7.5V \le V_{IN} \le 15V$		5	10		5	25	mV
Load Regulation (Note 3)	$T_j = 25°C$, $V_{IN} = 7.5V$, $0A \le I_{OUT} \le 3A$		25	50		25	100	mV
Quiescent Current	$7.5V \le V_{IN} \le 15V$, $0A \le I_{OUT} \le 3A$		12	20		12	20	mA
Output Noise Voltage	$T_j = 25°C$ $10\ Hz \le f \le 100\ kHz$		40			40		μVrms
Short Circuit Current Limit	$T_j = 25°C$ $V_{IN} = 15V$ $V_{IN} = 7.5V$		 3 4	 4.5 6		 3 4	 4.5 5	 A A
Long Term Stability				35			35	mW
Thermal Resistance Junction to Case (Note 2)			2			2		°C/W

LM323A/LM323 Electrical Characteristics (Note 1)

Parameter	Conditions	LM323A			LM323			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	$T_j = 25°C$ $V_{IN} = 7.5V$, $I_{OUT} = 0A$	4.95	5	5.05	4.8	5	5.2	V
	$7.5V \le V_{IN} \le 15V$ $0A \le I_{OUT} \le 3A$, $P \le 30W$	4.85		5.15	4.75		5.25	V
Line Regulation (Note 3)	$T_j = 25°C$ $7.5V \le V_{IN} \le 15V$		5	10		5	25	mV
Load Regulation (Note 3)	$T_j = 25°C$, $V_{IN} = 7.5V$, $0A \le I_{OUT} \le 3A$		25	50		25	100	mV
Quiescent Current	$7.5V \le V_{IN} \le 15V$, $0A \le I_{OUT} \le 3A$		12	20		12	20	mA
Output Noise Voltage	$T_j = 25°C$ $10\ Hz \le f \le 100\ kHz$		40			40		μVrms
Short Circuit Current Limit	$T_j = 25°C$ $V_{IN} = 15V$ $V_{IN} = 7.5V$		 3 4	 4.5 6		 3 4	 4.5 5	 A A
Long Term Stability				35			35	mW
Thermal Resistance Junction to Case (Note 2)			2			2		°C/W

Note 1: Unless otherwise noted, specifications apply for $-55°C \le T_j \le +150°C$ for the LM123A and LM123, $-40°C \le T_j \le +125°C$ for the LM323A, and $0°C \le T_j \le +125°C$ for the LM323. Although power dissipation is internally limited, specifications apply only for $P \le 30W$.

Note 2: Without a heat sink, the thermal resistance of the TO-3 package is about 35°C/W. With a heat sink, the effective thermal resistance can only approach the specified values of 2°C/W, depending on the efficiency of the heat sink.

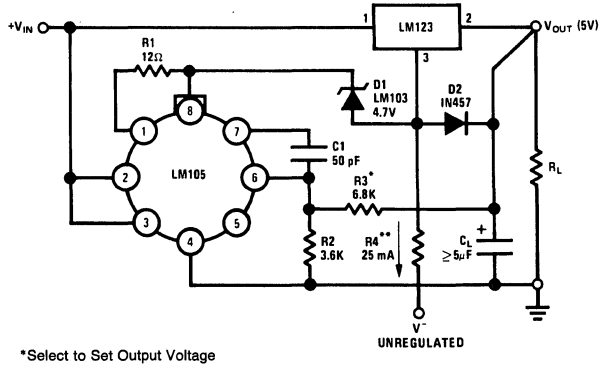
Note 3: Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%.

Note 4: Refer to RETS123K drawing for LM123K, and to RETS123AK for LM123AK military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Typical Applications (Continued)

Adjustable Output 5V–10V 0.1% Regulation



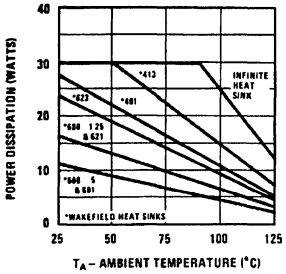
*Select to Set Output Voltage

**Select to Draw 25 mA from V−

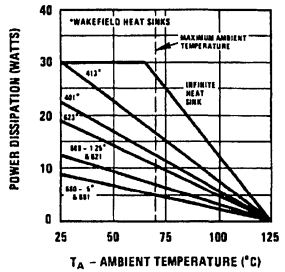
TL/H/7771–4

Typical Performance Characteristics

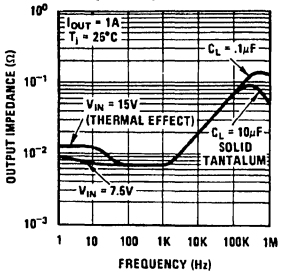
Maximum Average Power Dissipation for LM123A, LM123



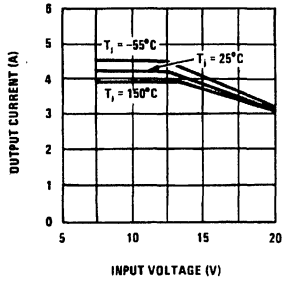
Maximum Average Power Dissipation for LM323A, LM323



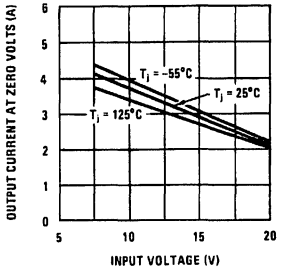
Output Impedance



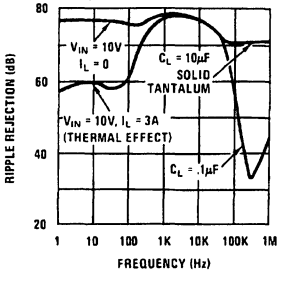
Peak Available Output Current



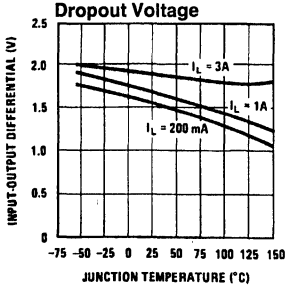
Short Circuit Current



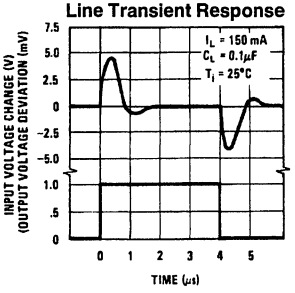
Ripple Rejection



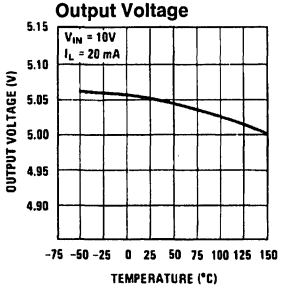
Dropout Voltage



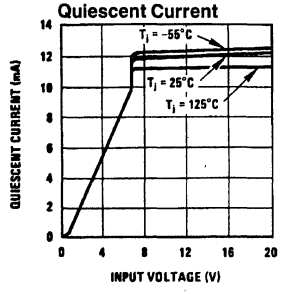
Line Transient Response



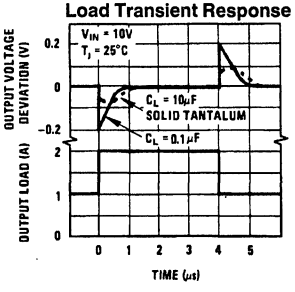
Output Voltage



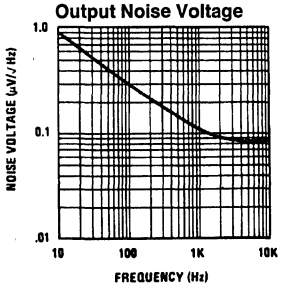
Quiescent Current



Load Transient Response



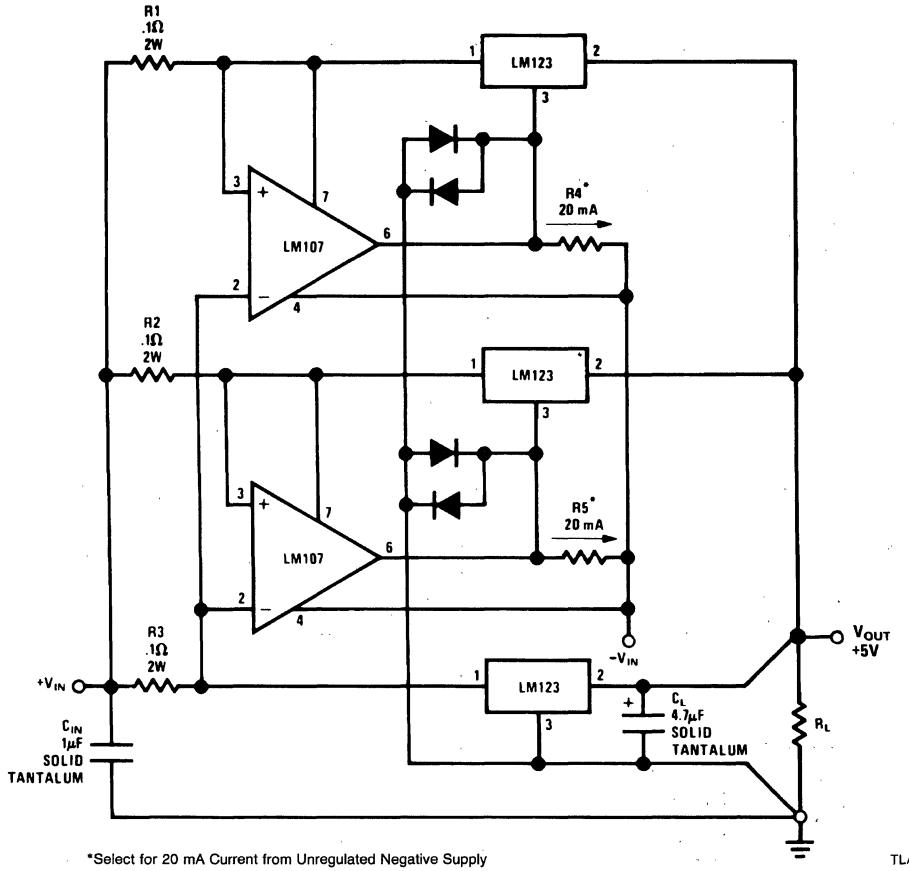
Output Noise Voltage



TL/H/7771–5

Typical Applications (Continued)

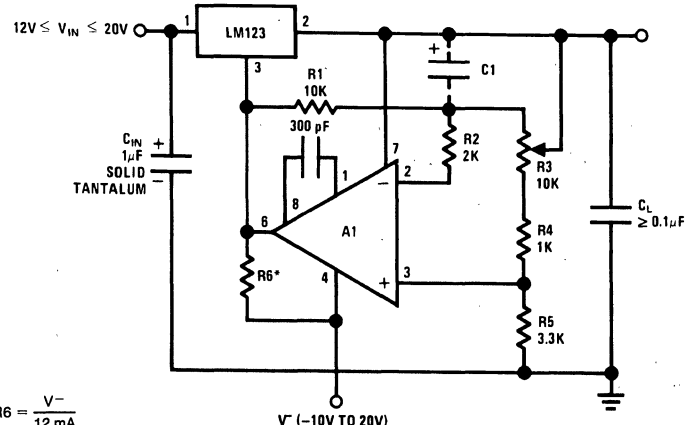
10 Amp Regulator with Complete Overload Protection



*Select for 20 mA Current from Unregulated Negative Supply

TL/H/7771–6

Adjustable Regulator 0V–10V @ 3A



$*R6 = \frac{V^-}{12\ mA}$

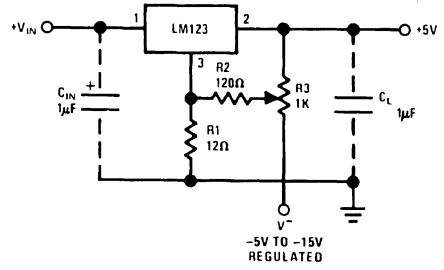
A_1—LM101A

C_1—2 μF Optional—Improves Ripple Rejection, Noise, and Transient Response

TL/H/7771–7

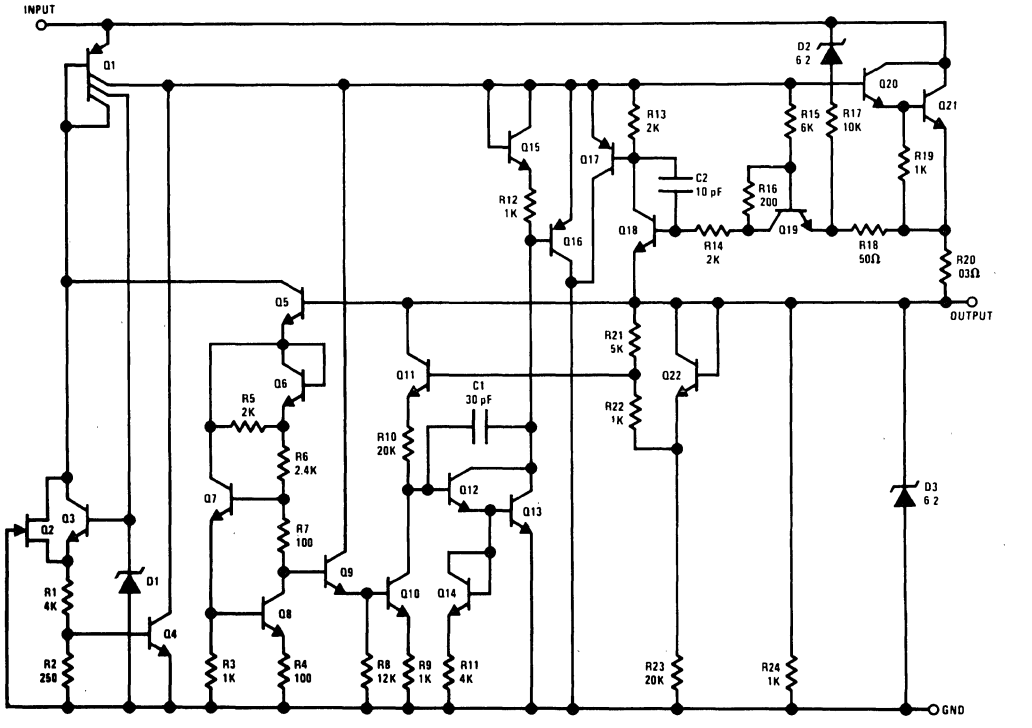
Typical Applications (Continued)

Trimming Output to 5V



TL/H/7771–8

Schematic Diagram



TL/H/7771–1

National Semiconductor

LM125/LM325/LM325A, LM126/LM326 Voltage Regulators

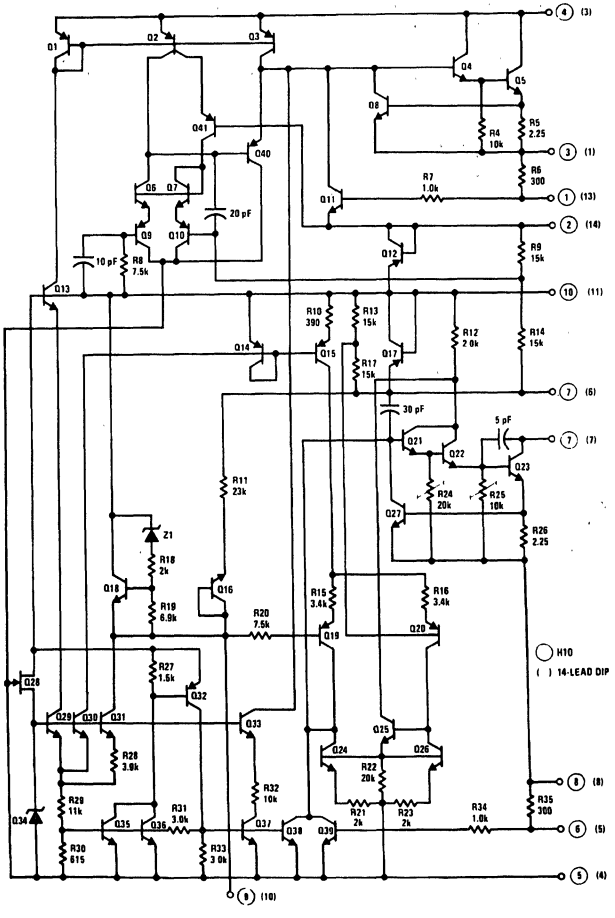
General Description

These are dual polarity tracking regulators designed to provide balanced positive and negative output voltages at current up to 100 mA, the devices are set for ±15V and ±12V outputs respectively. Input voltages up to ±30V can be used and there is provision for adjustable current limiting. These devices are available in two package types to accommodate various power requirements and temperature ranges.

Features

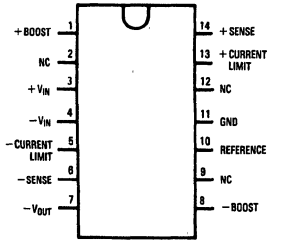
- ±15V and ±12V tracking outputs
- Output current to 100 mA
- Output voltage balanced to within 1% (LM125, LM126, LM325A)
- Line and load regulation of 0.06%
- Internal thermal overload protection
- Standby current drain of 3 mA
- Externally adjustable current limit
- Internal current limit

Schematic and Connection Diagrams



TL/H/7776–1

Dual-In-Line Package

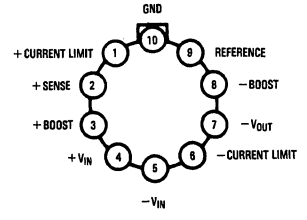


TL/H/7776–2

Top View

Order Number LM325AN, LM325N or LM326N
See NS Package Number N14A

Metal Can Package



Case connected to $-V_{IN}$ TL/H/7776–3

Top View

Order Number LM125H, LM325H, LM126H or LM326H
See NS Package Number H10C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Input Voltage	±30V
Forced V_O+ (Min) (Note 1)	−0.5V
Forced V_O- (Max) (Note 1)	+0.5V
Power Dissipation (Note 2)	P_{MAX}
Output Short-Circuit Duration (Note 3)	Continuous

Operating Conditions

Operating Free Temperature Range	
LM125	−55°C to +125°C
LM325, LM325A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics LM125/LM325/LM325A (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	T_j = 25°C				
LM125/LM325A		14.8	15	15.2	V
LM325		14.5	15	15.5	V
Input-Output Differential		2.0			V
Line Regulation	V_{IN} = 18V to 30V, I_L = 20 mA, T_j = 25°C		2.0	10	mV
Line Regulation Over Temperature Range	V_{IN} = 18V to 30V, I_L = 20 mA,		2.0	20	mV
Load Regulation	I_L = 0 to 50 mA, V_{IN} = ±30V,				
V_O+	T_j = 25°C		3.0	10	mV
V_O-			5.0	10	mV
Load Regulation Over Temperature Range	I_L = 0 to 50 mA, V_{IN} = ±30V				
V_O+			4.0	20	mV
V_O-			7.0	20	mV
Output Voltage Balance	T_j = 25°C				
LM125, LM325A				±150	mV
LM325				±300	mV
Output Voltage Over Temperature Range	P ≤ P_{MAX}, 0 ≤ I_O ≤ 50 mA,				
LM125, LM325A	18V ≤ $\|V_{IN}\|$ ≤ 30	14.65		15.35	V
LM325		14.27		15.73	V
Temperature Stability of V_O			±0.3		%
Short Circuit Current Limit	T_j = 25°C		260		mA
Output Noise Voltage	T_j = 25°C, BW = 100 − 10 kHz		150		μVrms
Positive Standby Current	T_j = 25°C		1.75	3.0	mA
Negative Standby Current	T_j = 25°C		3.1	5.0	mA
Long Term Stability			0.2		%/kHr
Thermal Resistance Junction to Case (Note 4)					
LM125H, LM325H			20		°C/W
Junction to Ambient	(Still Air)		215		°C/W
Junction to Ambient	(400 Lf/min Air Flow)		82		°C/W
Junction to Ambient	(Still Air)				
LM325AN, LM325N			90		°C/W

Note 1: That voltage to which the output may be forced without damage to the device.

Note 2: Unless otherwise specified these specifications apply for T_j = 55°C to +150°C on LM125, T_j = 0°C to +125°C on LM325A, T_j = 0°C to +125°C on LM325, V_{IN} = ±20V, I_L = 0 mA, I_{MAX} = 100 mA, P_{MAX} = 2.0W for the H10 Package. I_{MAX} = 100 mA. I_{MAX} = 100 mA, P_{MAX} = 1.0W for the DIP N Package.

Note 3: If the junction temperature exceeds 150°C, the output short circuit duration is 60 seconds.

Note 4: Without a heat sink, the thermal resistance junction to ambient of the H10 Package is about 155°C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.

Note 5: Refer to RETS125X drawing for military specification of LM125.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Input Voltage	±30V
Forced V_O^+ (Min) (Note 1)	−0.5V
Forced V_O^- (Max) (Note 1)	+0.5V
Power Dissipation (Note 2)	Internally Limited
Output Short-Circuit Duration (Note 3)	Continuous

Operating Conditions

Operating Free Temperature Range	
LM126	−55°C to +125°C
LM326	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics LM126/LM326 (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	T_j = 25°C				
LM126/LM326		11.8	12	12.2	V
		11.5		12.5	V
Input-Output Differential		2.0			V
Line Regulation	V_{IN} = 15V to 30V I_L = 20 mA, T_j = 25°C		2.0	10	mV
Line Regulation Over Temperature Range	V_{IN} = 15V to 30V, I_L = 20 mA		2.0	20	mV
Load Regulation	I_L = 0 to 50 mA, V_{IN} = ±30V,				
V_O^+	T_j = 25°C		3.0	10	mV
V_O^-			5.0	10	mV
Load Regulation Over Temperature Range	I_L = 0 to 50 mA, V_{IN} = ±30V				
V_O^+			4.0	20	mV
V_O^-			7.0	20	mV
Output Voltage Balance	T_j = 25°C				
LM126, LM326				±125	mV
				±250	mV
Output Voltage Over Temperature Range	$P \leq P_{MAX}$, $0 \leq I_O \leq 50$ mA,				
LM126	$15V \leq \lvert V_{IN} \rvert \leq 30$	11.68		12.32	V
LM326		11.32		12.68	V
Temperature Stability of V_O			±0.3		%
Short Circuit Current Limit	T_j = 25°C		260		mA
Output Noise Voltage	T_j = 25°C, BW = 100 − 10 kHz		100		μVrms
Positive Standby Current	T_j = 25°C, I_L = 0		1.75	3.0	mA
Negative Standby Current	T_j = 25°C, I_L = 0		3.1	5.0	mA
Long Term Stability			0.2		%/kHr
Thermal Resistance Junction to Case (Note 4)					
LM126H, LM326H			20		°C/W
Junction to Ambient	(Still Air)		155		°C/W
Junction to Ambient	(400 Lf/min Air Flow)		62		°C/W
Junction to Ambient LM326N			150		°C/W

Note 1: That voltage to which the output may be forced without damage to the device.

Note 2: Unless otherwise specified these specifications apply for T_j = 55°C to +150°C on LM126, T_j = 0°C to +125°C on LM326, V_{IN} = ±20V, I_L = 0 mA, I_{MAX} = 100 mA, P_{MAX} = 2.0W for the H10 Package. I_{MAX} = 100 mA. I_{MAX} = 100 mA, P_{MAX} = 1.0W for the DIP N Package.

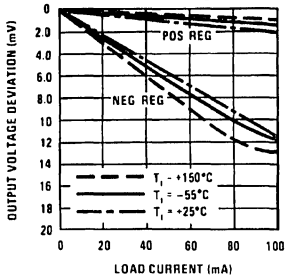
Note 3: If the junction temperature exceeds 150°C, the output short circuit duration is 60 seconds.

Note 4: Without a heat sink, the thermal resistance junction to ambient of the H10 Package is about 155°C/W. With a heat sink, the effective thermal resistance can only approach the junction to case values specified, depending on the efficiency of the sink.

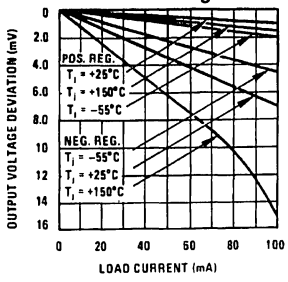
Note 5: Refer to RETS126X drawing for military specification of LM126.

Typical Performance Characteristics

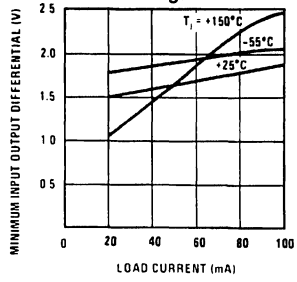
LM125 Load Regulation



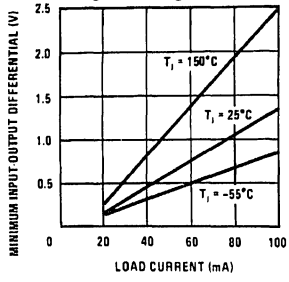
LM126 Load Regulation



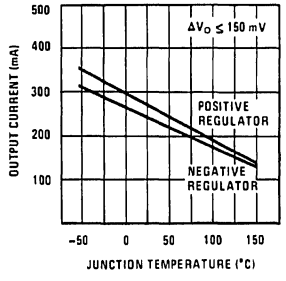
LM125/126 Regulator Dropout Voltage for Positive Regulator



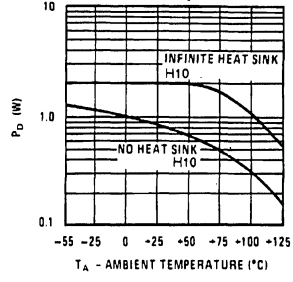
LM125/126 Regulator Dropout Voltage for Negative Regulator



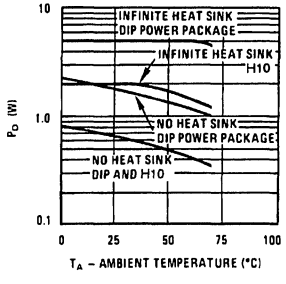
LM125/126 Peak Output Current vs Junction Temperature



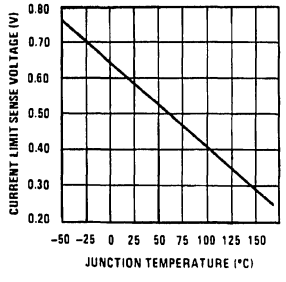
LM125/126 Maximum Average Power Dissipation vs Ambient Temperature



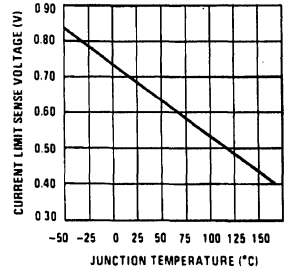
LM325/326 Maximum Average Power Dissipation vs Ambient Temperature



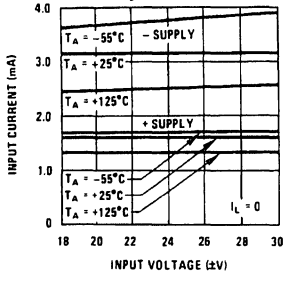
LM125/126 Current Limit Sense Voltage vs Temperature for Negative Regulator



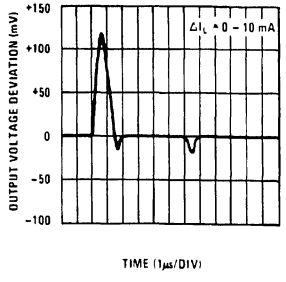
LM125/126 Current Limit Sense Voltage vs Temperature for Positive Regulator



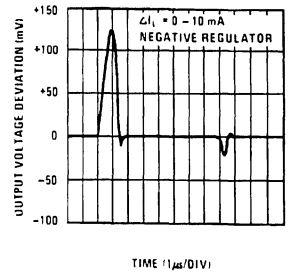
LM125/126 Standby Current Drain



LM125 Load Transient Response for Negative Regulator



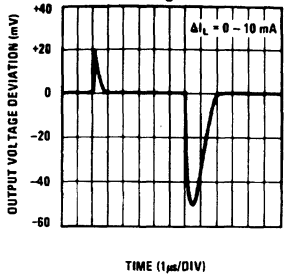
LM126 Load Transient Response



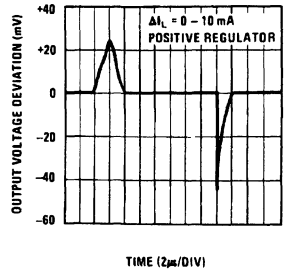
TL/H/7776–4

Typical Performance Characteristics (Continued)

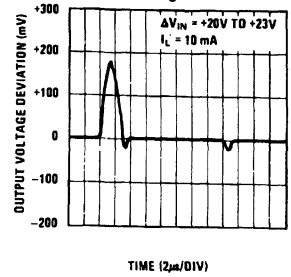
LM125
Load Transient Response
for Positive Regulator



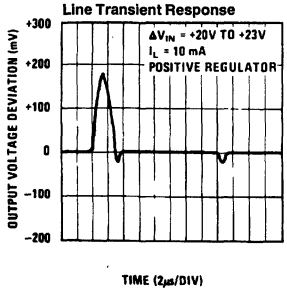
LM126
Load Transient Response



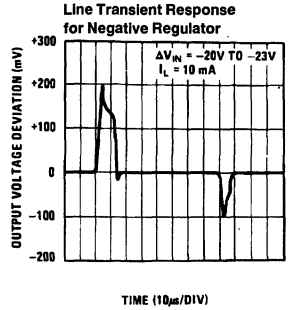
LM125
Line Transient Response
for Positive Regulator



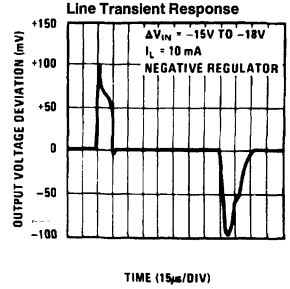
LM126
Line Transient Response



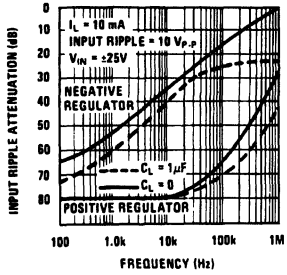
LM125
Line Transient Response
for Negative Regulator



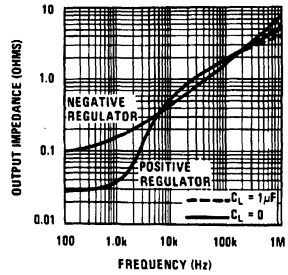
LM126
Line Transient Response



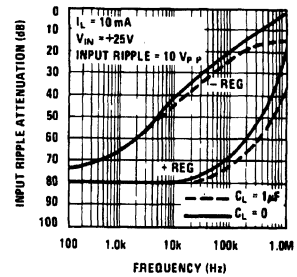
LM125
Ripple Rejection



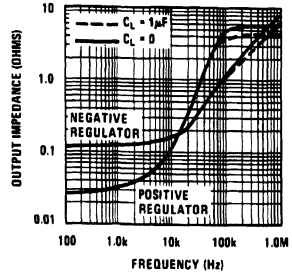
LM125
Output Impedance
vs Frequency



LM126
Ripple Rejection



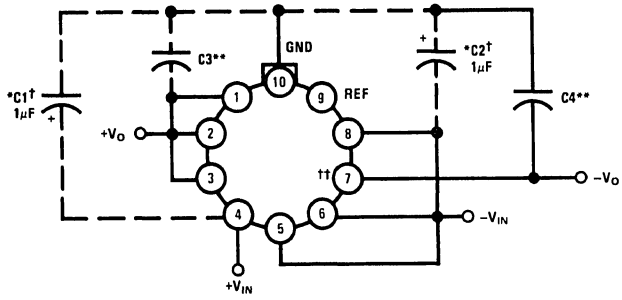
LM126
Output Impedance
vs Frequency



TL/H/7776–5

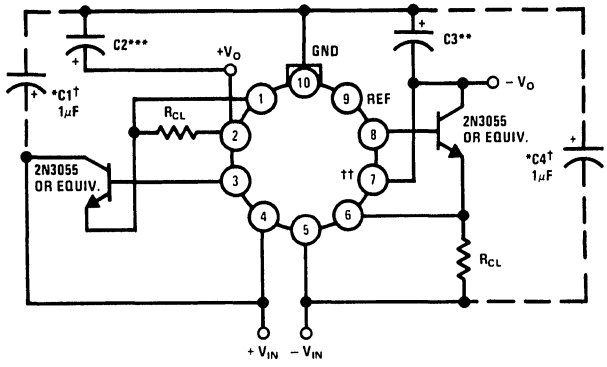
Typical Applications

Basic Regulator†††



TL/H/7776-6

2.0 Amp Boosted Regulator With Current Limit



TL/H/7776-7

Note: Metal can (H) packages shown.

$$I_{CL} = \frac{\text{Current Limit Sense Voltage (See Curve)}}{R_{CL}}$$

†Solid tantalum

††Short pins 6 and 7 on dip

†††R_{CL} can be added to the basic regulator between pins 6 and 5, 1 and 2 to reduce current limit.

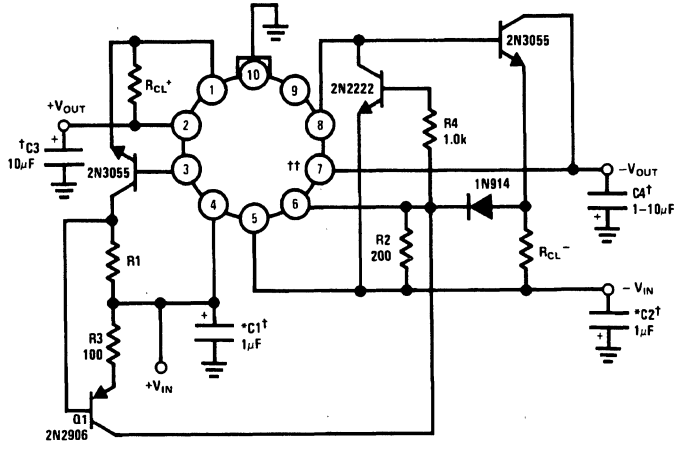
*Required if regulator is located an appreciable distance from power supply filter.

**Although no capacitor is needed for stability, it does help transient response. (If needed use 1 μF electrolytic).

***Although no capacitor is needed for stability, it does help transient response. (If needed use 10 μF electrolytic).

Typical Applications (Continued)

Positive Current Dependent Simultaneous Current Limiting



TL/H/7776–8

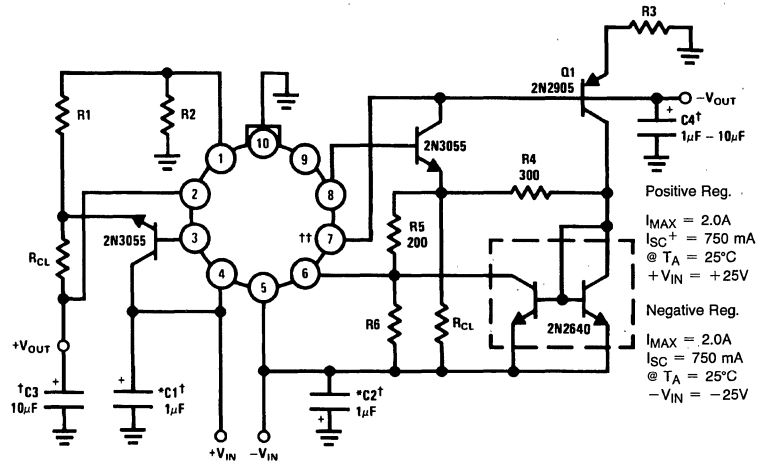
$$I_{CL}^+ = \frac{\frac{V_{SENSE\ NEG}}{2} + V_{BEQ1}}{R1}$$

$$I_{CL}^+ = \frac{V_{SENSE\ NEG} + V_{DIODE}}{R_{CL}^-}$$

$$R_{CL}^+ = \frac{V_{SENSE}^+}{1.1\ I_{CL}^+}$$

I_{CL}^+ Controls Both Sides of the Regulator.

Boosted Regulator With Foldback Current Limit



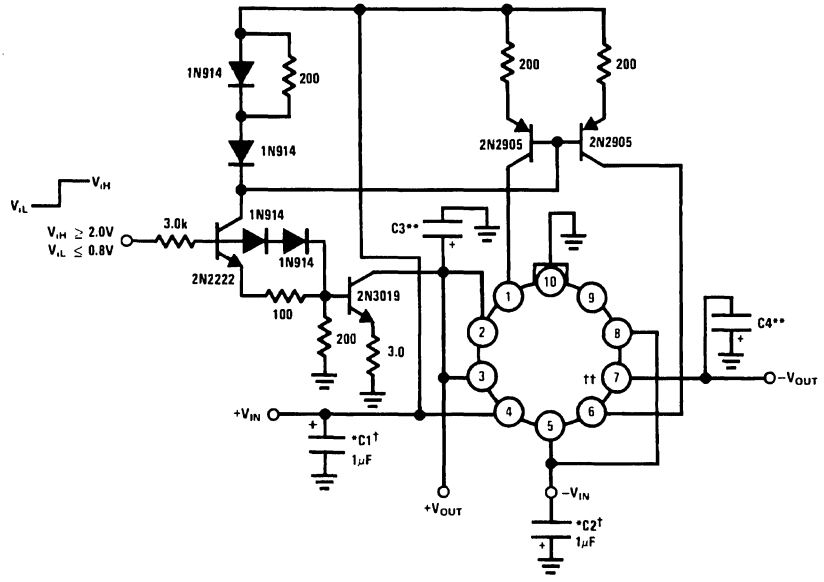
TL/H/7776–9

Resistor Values

	125	126
R1	18	20
R2	310	180
R3	2.4k	1.35k
R6	300	290
R_{CL}	0.7	0.9

Typical Applications (Continued)

Electric Shutdown



TL/H/7776–10

†Solid tantalum

††Short pins 6 and 7 on dip

*Required if regulator is located an appreciable distance from power supply filter.

**Although no capacitor is needed for stability, it does help transient response. (If needed use 1 μF electrolytic).

National Semiconductor

LM133/LM333 3-Ampere Adjustable Negative Regulators

General Description

The LM133/LM333 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −3.0A over an output voltage range of −1.2V to −32V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM133 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

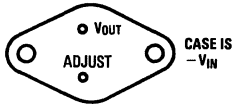
The LM133/LM333 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM133/LM333 are ideal complements to the LM150/LM350 adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −32V
- 3.0A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output is short circuit protected

Connection Diagrams

TO-3
Metal Can Package

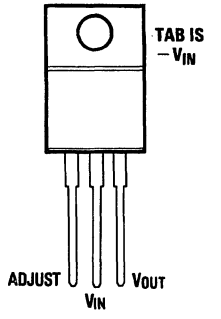


TL/H/9065–1

Bottom View

Steel TO-3 Metal Can Package (K STEEL)
Order Number LM133K STEEL or LM333K STEEL
See NS Package Number K02A

TO-220
Plastic Package



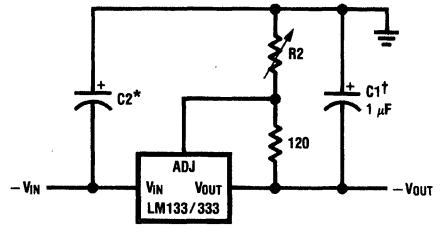
TL/H/9065–2

Bottom View

3-Lead TO-220 Plastic Package (T)
Order Number LM333T
See NS Package Number T03B

Typical Applications

Adjustable Negative Voltage Regulator



TL/H/9065–3

Full output current not available at high input-output voltages.

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power supply filter capacitor.

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	35V
Operating Junction Temperature Range	T_{MIN} to T_{MAX}
LM133	−55°C to +150°C
LM333	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package	300°C
TO-220 Package	260°C

Preconditioning

Burn-In In Thermal Limit	100% All Devices

Electrical Characteristics LM133 (Note 1) (Note 5)

Parameter	Conditions	Typical	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Max Unless Noted)
Reference Voltage	T_J = 25°C, I_L = 10 mA	−1.250	−1.238 −1.262		V(MIN) V(MAX)
	$T_{MIN} \le T_J \le T_{MAX}$, 3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 35V, 10 mA ≤ I_L ≤ 3A, P ≤ P_{MAX}				
	LM133	**−1.250**	**−1.225**		V(MIN)
	LM133		**−1.275**		V(MAX)
Line Regulation	T_J = 25°C, 3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 35V, I_{OUT} = 50 mA (Note 2)	0.01	0.02		% /V
	LM133	**0.02**	**0.05**		% /V
Load Regulation	T_J = 25°C, 10 mA ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX} (Notes 2 and 6)	0.2	0.5		%
	LM133	**0.4**	**1.0**		%
Thermal Regulation	T_J = 25°C, 10 ms Pulse	0.002	0.01		% /W
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$	0.4			%
Long Term Stability	T_J = 125°C, 1000 Hours	0.15		0.8	%
Adjust Pin Current	T_J = 25°C				
	LM133	65	90		μA
	LM133	**70**	**100**		μA
Adjust Pin Current Change	T_J = 25°C, 10 mA ≤ I_L ≤ 3A	2	5	**6**	μA
	T_J = 25°C, 3.0V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 35V	2	5	**6**	μA
Minimum Load Current	$\|V_{IN} - V_{OUT}\|$ ≤ 35V, T_J = 25°C				
	LM133	**2.5**	**5.0**		mA
	$\|V_{IN} - V_{OUT}\|$ ≤ 10V, T_J = 25°C				
	LM133	**1.2**	**2.5**		mA
Current Limit (Note 6)	3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 10V, T_J = 25°C				
	LM133	**3.9**	**3.0**		A(MIN)
	$\|V_{IN} - V_{OUT}\|$ = 20V, T_J = 25°C				
	LM133	**2.4**	**1.25**		A(MIN)
	$\|V_{IN} - V_{OUT}\|$ = 30V, T_J = 25°C				
	LM133	0.4	**0.3**		A(MIN)
Output Noise (% of V_{OUT})	10 Hz to 10 kHz, T_J = 25°C	0.003		0.010	% (rms)
Ripple Rejection	V_{OUT} = 10V, f = 120 Hz, T_J = 25°C				
	C_{ADJ} = 0 μF	60		55	dB
	C_{ADJ} = 10 μF	77		70	dB
Thermal Resistance	TO-3 Package (K STEEL)	1.2		1.8	°C/W
	TO-220 Package (T)	3		4	°C/W
Thermal Shutdown Temperature	LM133	163	150		°C(MIN)
	LM133			190	°C(MAX)

Electrical Characteristics LM133 (Note 1) (Note 5)

Parameter	Conditions	Typical	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Max Unless Noted)
Reference Voltage	T_J = 25°C, I_L = 10 mA	−1.250	−1.225 −1.275		V(MIN) V(MAX)
	$T_{MIN} \le T_J \le T_{MAX}$, 3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 35V, 10 mA ≤ I_L ≤ 3A, P ≤ P_{MAX}	**−1.250**		**−1.213** **−1.287**	V(MIN) V(MAX)
Line Regulation	T_J = 25°C, 3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 35V, I_{OUT} = 50 mA (Note 2)	0.001 **0.02**	0.004	 **0.07**	% /V % /V
Load Regulation	T_J = 25°C, 10 mA ≤ I_{OUT} ≤ 3A, P ≤ P_{MAX} (Notes 2 and 6)	0.2 **0.4**	1.0	 **1.5**	% %
Thermal Regulation	T_J = 25°C, 10 ms Pulse	0.002	0.02		% /W
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$	0.5			%
Long Term Stability	T_J = 125°C, 1000 Hours	0.2		0.8	%
Adjust Pin Current	T_J = 25°C	65 **70**	95	 **100**	μA μA
Adjust Pin Current Change	T_J = 25°C, 10 mA ≤ I_L ≤ 3A T_J = 25°C, 3.0V ≤ $\|V_{IN}\|$ ≤ 35V	2.5 2.5	7 7	**8** **8**	μA μA
Minimum Load Current	$\|V_{IN} - V_{OUT}\|$ ≤ 35V, T_J = 25°C $\|V_{IN} - V_{OUT}\|$ ≤ 10V, T_J = 25°C	**2.5** **1.5**	10 5.0	**10** **5.0**	mA mA
Current Limit (Note 6)	3V ≤ $\|V_{IN} - V_{OUT}\|$ ≤ 10V, T_J = 25°C $\|V_{IN} - V_{OUT}\|$ = 20V, T_J = 25°C $\|V_{IN} - V_{OUT}\|$ = 30V, T_J = 25°C	**3.9** **2.4** 0.4	2.0 1.0 0.20	**3.0** **1.0** **0.2**	A(MIN) A(MIN) A(MIN)
Output Noise (% of V_{OUT})	10 Hz to 10 kHz, T_J = 25°C	0.003		0.010	% (rms)
Ripple Rejection	V_{OUT} = 10V, f = 120 Hz, T_J = 25°C C_{ADJ} = 0 μF C_{ADJ} = 10 μF	 60 77		 50 66	 dB dB
Thermal Resistance Junction to Case	TO-3 Package (K STEEL) TO-220 Package (T)	1.2 3		1.8 4	°C/W °C/W
Thermal Shutdown Temperature		163		150 190	°C(MIN) °C(MAX)
Thermal Resistance Junction to Ambient (No Heatsink)	K Package T Package	35 50			°C/W °C/W

Note 1: Unless otherwise specified, these specifications apply: −55°C ≤ T_J ≤ +150°C for the LM133; and −40°C ≤ T_J + 125°C for the LM333; $|V_{IN} - V_{OUT}|$ = 5V; and I_{OUT} = 0.5A. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 30W.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8" below the base of the TO-3 package.

Note 3: Testing limits are guaranteed and 100% tested in production.

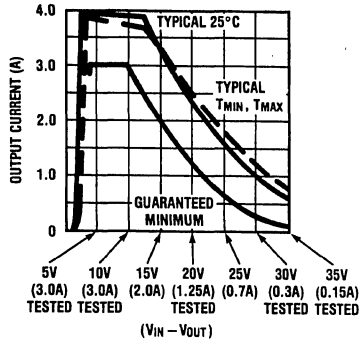
Note 4: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 5: Specifcations in **boldface** apply over the full rated temperature range.

Note 6: The output capability of the LM333 is guaranteed at 3A in the range of 3V ≤ $|V_{IN} - V_{OUT}|$ ≤ 10V. At voltages above 10V, the available output current decreases, but in the range 10V ≤ $|V_{IN} - V_{OUT}|$ ≤ 15V, the available current is 30W − $|V_{IN} - V_{OUT}|$. At voltages higher than 15V, refer to graphs for actual guaranteed output current available.

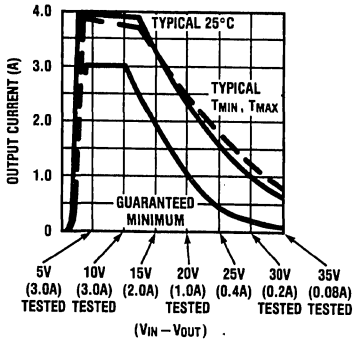
Guaranteed Performance Characteristics

LM133 Guaranteed Output Current



TL/H/9065–4

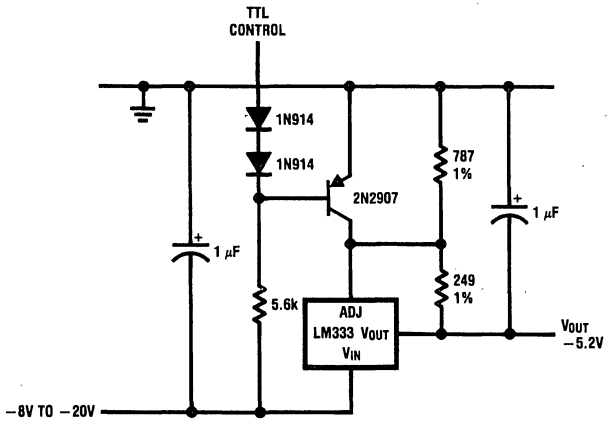
LM333 Guaranteed Output Current



TL/H/9065–5

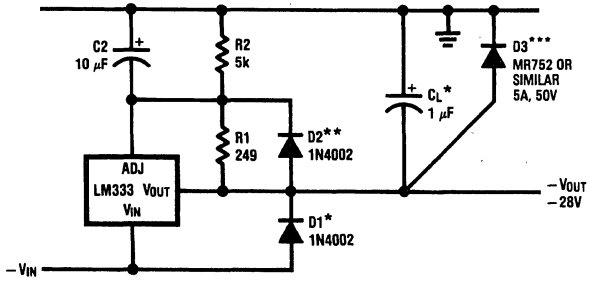
Typical Applications (Continued)

−5.2V Regulator with Electronic Shutdown*



TL/H/9065–6

Negative Regulator with Protection Diodes



TL/H/9065–7

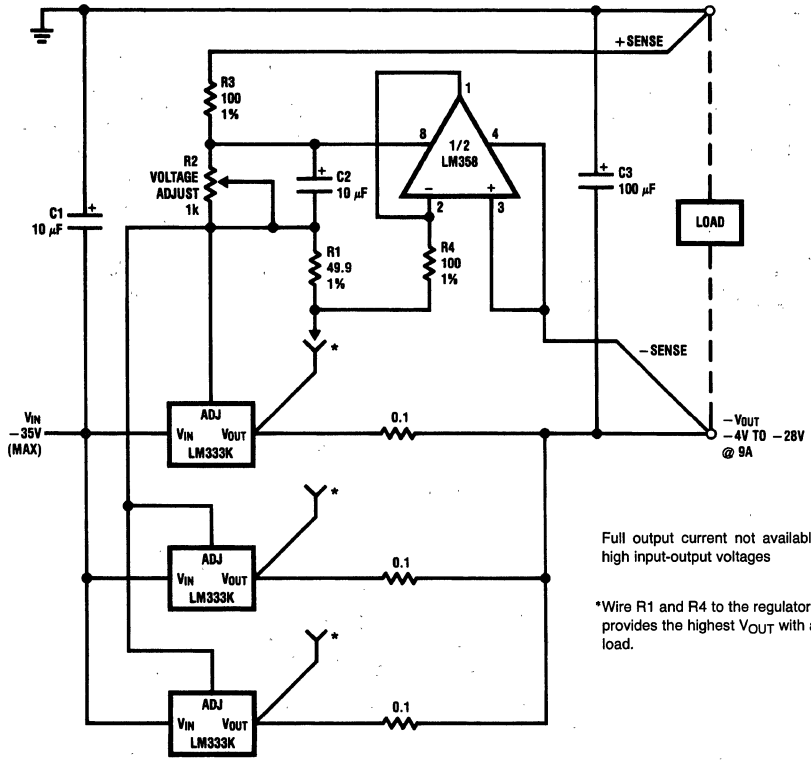
*When C_L is larger than 20 µF, D1 protects the LM133 in case the input supply is shorted.

**When C2 is larger than 10 µF and $-V_{OUT}$ is larger than −25V, D2 protect the LM133 in case the output is shorted.

***In case V_{OUT} is shorted to a positive supply, D3 protects the LM133 from overvoltage, and protects the load from reversed voltage.

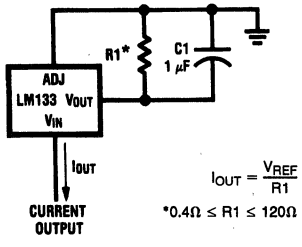
Typical Applications (Continued)

High-Performance 9-Ampere Adjustable Regulator



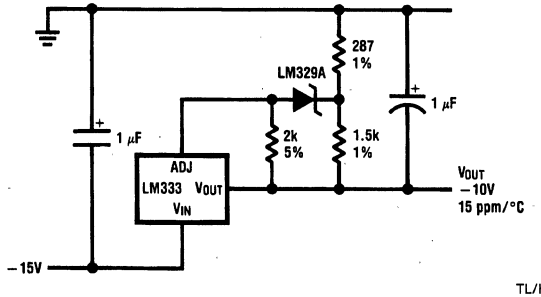
TL/H/9065–8

Current Regulator



TL/H/9065–9

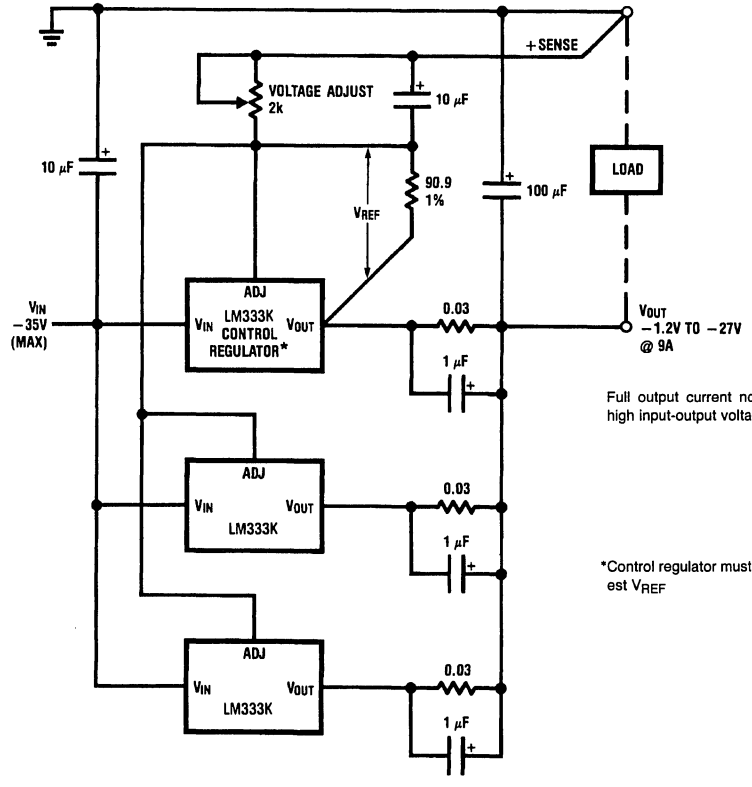
High Stability—10V Regulator



TL/H/9065–10

Typical Applications (Continued)

High-Current Adjustable Regulator

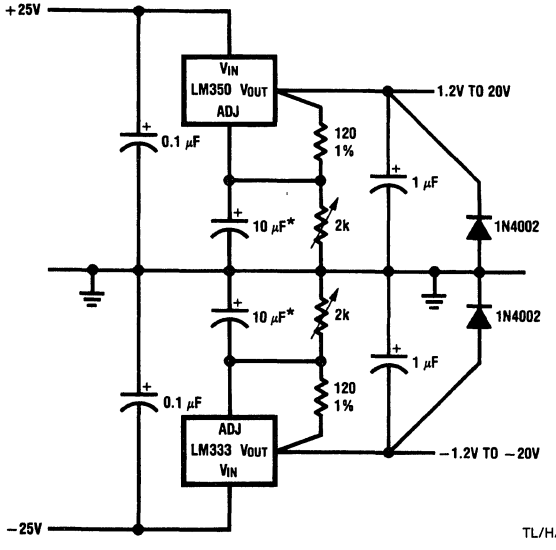


Full output current not available at high input-output voltages

*Control regulator must have the largest V_{REF}

TL/H/9065–11

Adjustable Lab Voltage Regulator

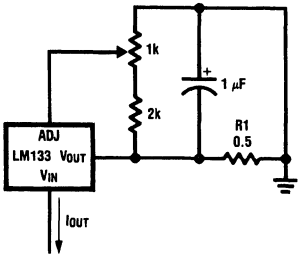


TL/H/9065–12

Full output current not available at high input-output voltages.

*The 10 μF capacitors are optional to improve ripple rejection.

Adjustable Current Regulator



TL/H/9065–13

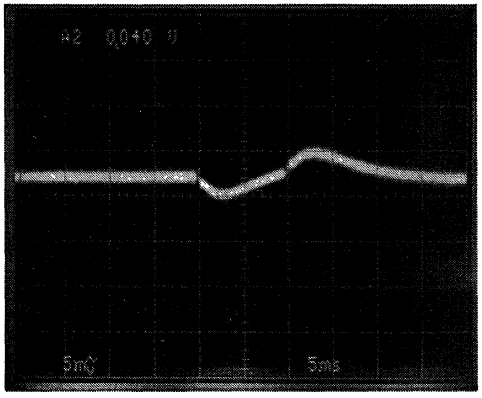
$$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\% \text{ adjustable}$$

Typical Applications (Continued)

THERMAL REGULATION

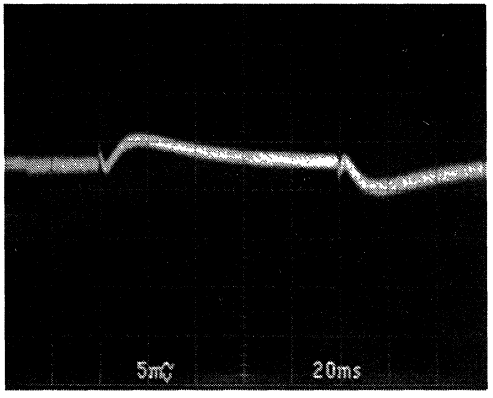
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since the power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per watt, within the first 10 rms after a step of power is applied. The LM133's specification is 0.01%/W, max.

In *Figure 1,* a typical LM133's output drifts only 2 mV (or 0.02% of $V_{OUT} = -10V$) when a 20W pulse is applied for 10 ms. This performance is thus well inside the specification limit of $0.01\%/W \times 20W = 0.2\%$ max. When the 20W pulse is ended, the thermal regulation again shows a 2 mV step as the LM133 chip cools off. Note that the load regulation error of about 1 mV (0.01%) is additional to the thermal regulation error. In *Figure 2*, when the 20W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



TL/H/9065–14

FIGURE 1



TL/H/9065–15

FIGURE 2

National Semiconductor

LM137/LM337
3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

Features

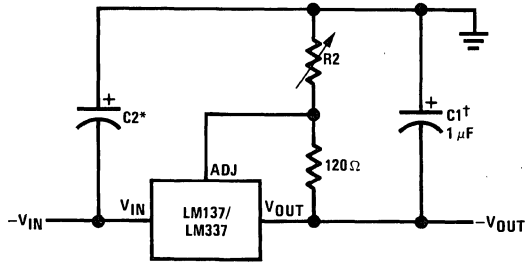
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output is short circuit protected

LM137 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM137/337	TO-3 (K) TO-39 (H)	20W 2W	1.5A 0.5A
LM337	TO-220 (T)	15W	1.5A
LM337M	TO-202 (P)	7.5W	0.5A

Typical Applications

Adjustable Negative Voltage Regulator



TL/H/9067–1

Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Rating	2k Volts

Preconditioning

Burn-In in Thermal Limit	**100% All Devices**

Electrical Characteristics (Note 1)

Parameter	Conditions	LM137			LM337			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_j = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2) $I_L = 10$ mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, 10 mA $\le I_{OUT} \le I_{MAX}$		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	10 mA $\le I_L \le I_{MAX}$ $3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $T_A = 25°C$		2	5		2	5	μA
Reference Voltage	$T_j = 25°C$ (Note 3) $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3) 10 mA $\le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	−1.225 −1.200	−1.250 −1.250	−1.275 −1.300	−1.213 −1.200	−1.250 −1.250	−1.287 −1.300	V V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	10 mA $\le I_{OUT} \le I_{MAX}$, (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$ $\lvert V_{IN} - V_{OUT} \rvert \le 10V$		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 15V$ K and T Package H and P Package $\lvert V_{IN} - V_{OUT} \rvert = 40V$, $T_j = 25°C$ K and T Package H and P Package	 1.5 0.5 0.24 0.15	 2.2 0.8 0.4 0.17	 3.5 1.8 	 1.5 0.5 0.15 0.10	 2.2 0.8 0.4 0.17	 3.7 1.9 	 A A A A
RMS Output Noise, % of V_{OUT}	$T_j = 25°C$, 10 Hz $\le f \le$ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz $C_{ADJ} = 10$ μF	 66	60 77		 66	60 77		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package K Package T Package P Package		12 2.3	15 3		12 2.3 4 7	15 3	°C/W °C/W °C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	H Package K Package T Package P Package		140 35			140 35 50 80		°C/W °C/W °C/W °C/W

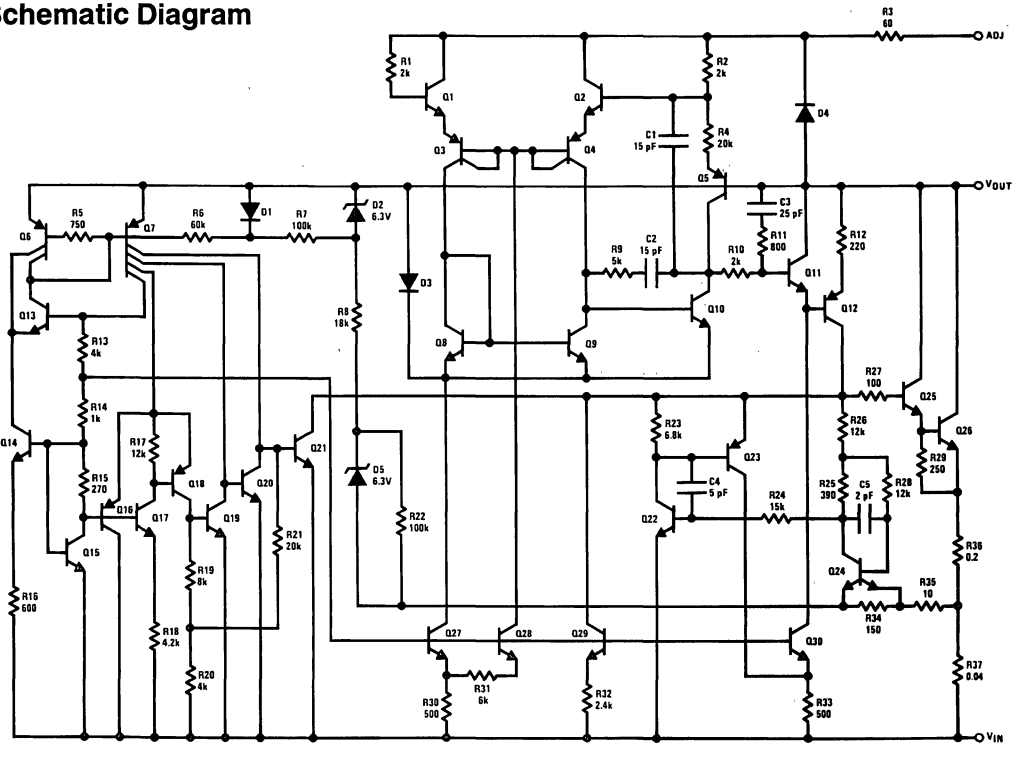
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and TO-202 packages and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages, and 0.5A for the TO-202 package and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8" below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

Note 4: Refer to RETS137H drawing for LM137H or RETS137K drawing for LM137K military specifications.

Schematic Diagram

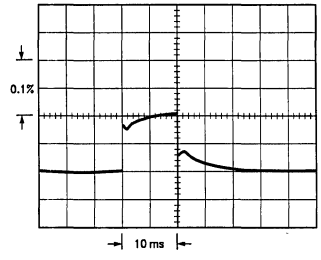


TL/H/9067–2

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

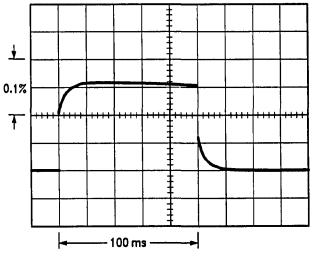
In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W × 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step at the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



TL/H/9067–3

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_{IL} = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

FIGURE 1



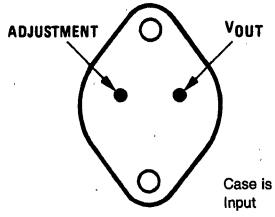
TL/H/9067–4

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

FIGURE 2

Connection Diagrams

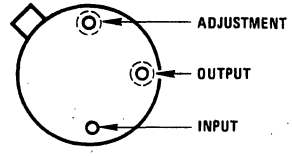
TO-3
Metal Can Package



TL/H/9067–5

Bottom View
Order Number LM137K STEEL or LM337K STEEL
See NS Package Number K02A

TO-39
Metal Can Package

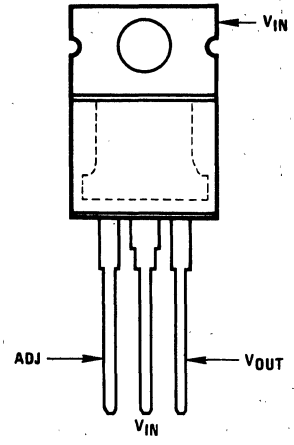


TL/H/9067–6

Bottom View

Order Number LM137H or LM337H
See NS Package Number H03B

TO-220
Plastic Package

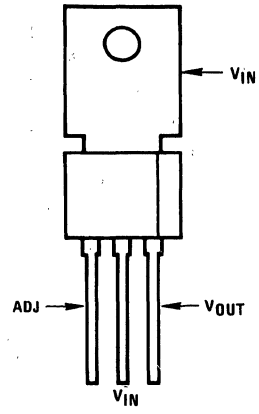


TL/H/9067–7

Front View

Order Number LM337T
See NS Package Number T03B

TO-202
Plastic Package



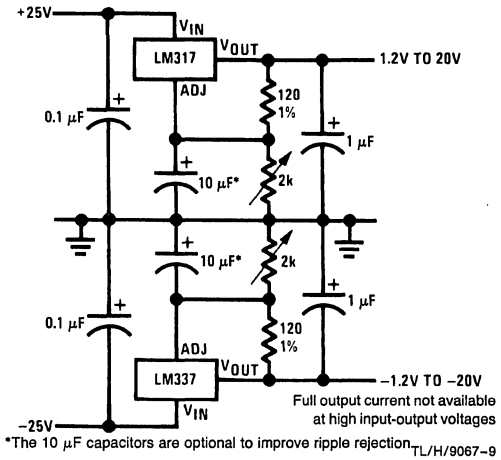
TL/H/9067–8

Front View

Order Number LM337MP
See NS Package Number P03A

Typical Applications (Continued)

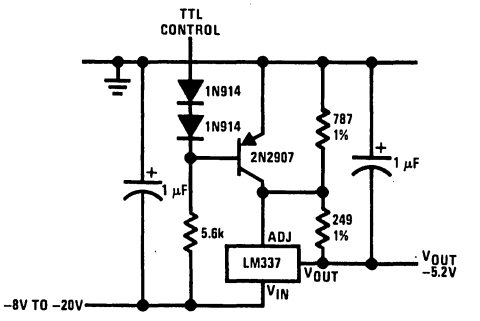
Adjustable Lab Voltage Regulator



*The 10 μF capacitors are optional to improve ripple rejection

TL/H/9067-9

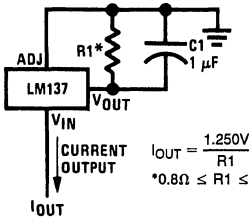
−5.2V Regulator with Electronic Shutdown*



TL/H/9067-10

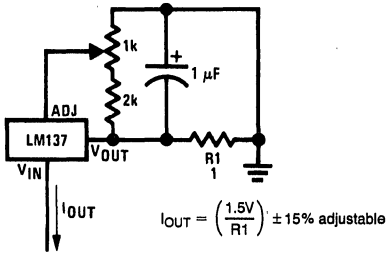
*Minimum output ≅ −1.3V when control input is low

Current Regulator



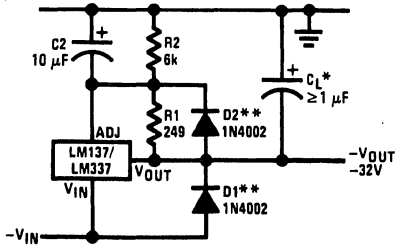
TL/H/9067-11

Adjustable Current Regulator



TL/H/9067-12

Negative Regulator with Protection Diodes

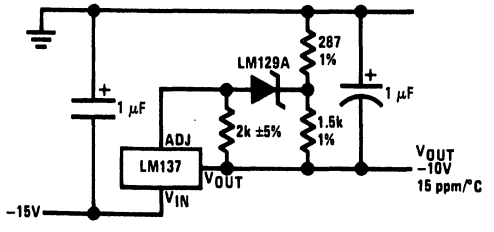


TL/H/9067-13

*When C_L is larger than 20 μF, D1 protects the LM137 in case the input supply is shorted

**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

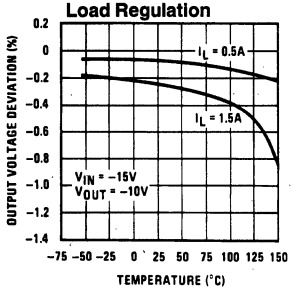
High Stability −10V Regulator



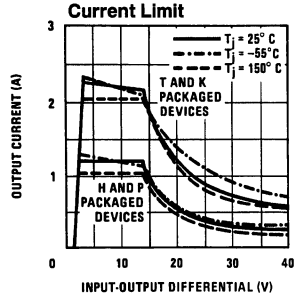
TL/H/9067-14

Typical Performance Characteristics (K Steel and T Packages)

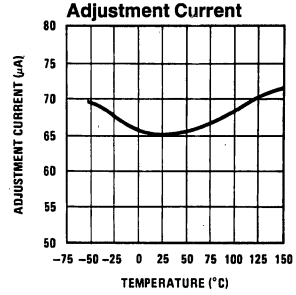
Load Regulation



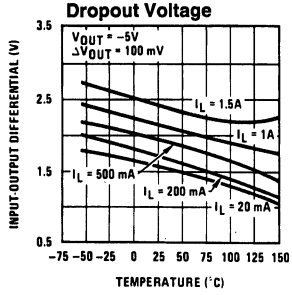
Current Limit



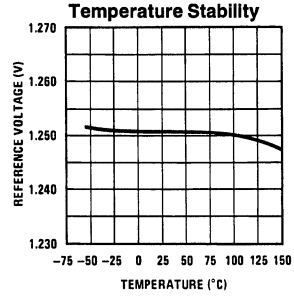
Adjustment Current



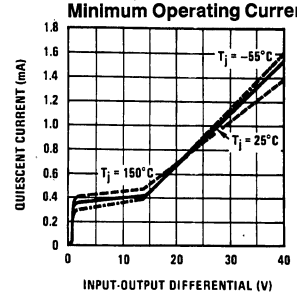
Dropout Voltage



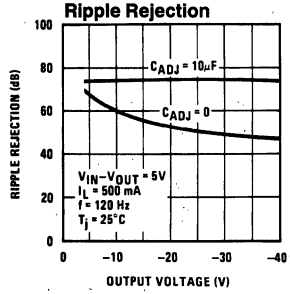
Temperature Stability



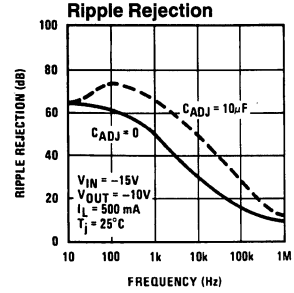
Minimum Operating Current



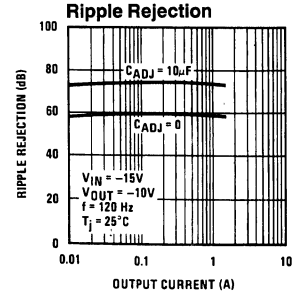
Ripple Rejection



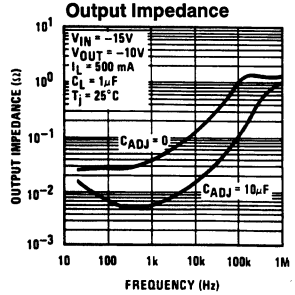
Ripple Rejection



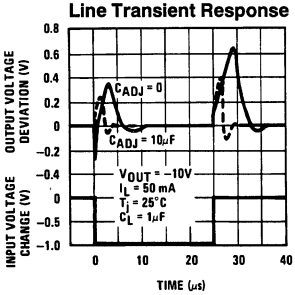
Ripple Rejection



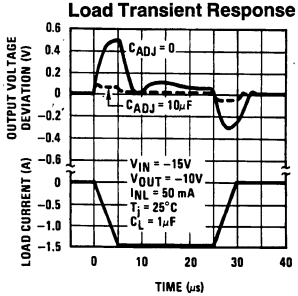
Output Impedance



Line Transient Response



Load Transient Response



TL/H/9067–15

National Semiconductor

LM137HV/LM337HV 3-Terminal Adjustable Negative Regulators (High Voltage)

General Description

The LM137HV/LM337HV are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −47V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137HV series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

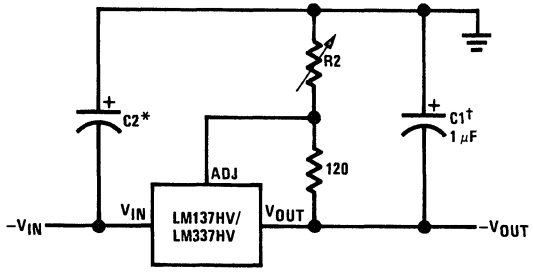
The LM137HV/LM337HV serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137HV/LM337HV are ideal complements to the LM117HV/LM317HV adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −47V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package
- Output short circuit protected

Typical Applications

Adjustable Negative Voltage Regulator



TL/H/9066–1

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left[-I_{Adj}(R_2)\right]$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Power Dissipation	Internally limited
Input—Output Voltage Differential	50V
Operating Junction Temperature Range	
LM137HV	−55°C to +150°C
LM337HV	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°

ESD rating is to be determined.

Preconditioning

Burn-In in Thermal Limit 100% All Devices

Electrical Characteristics (Note 1)

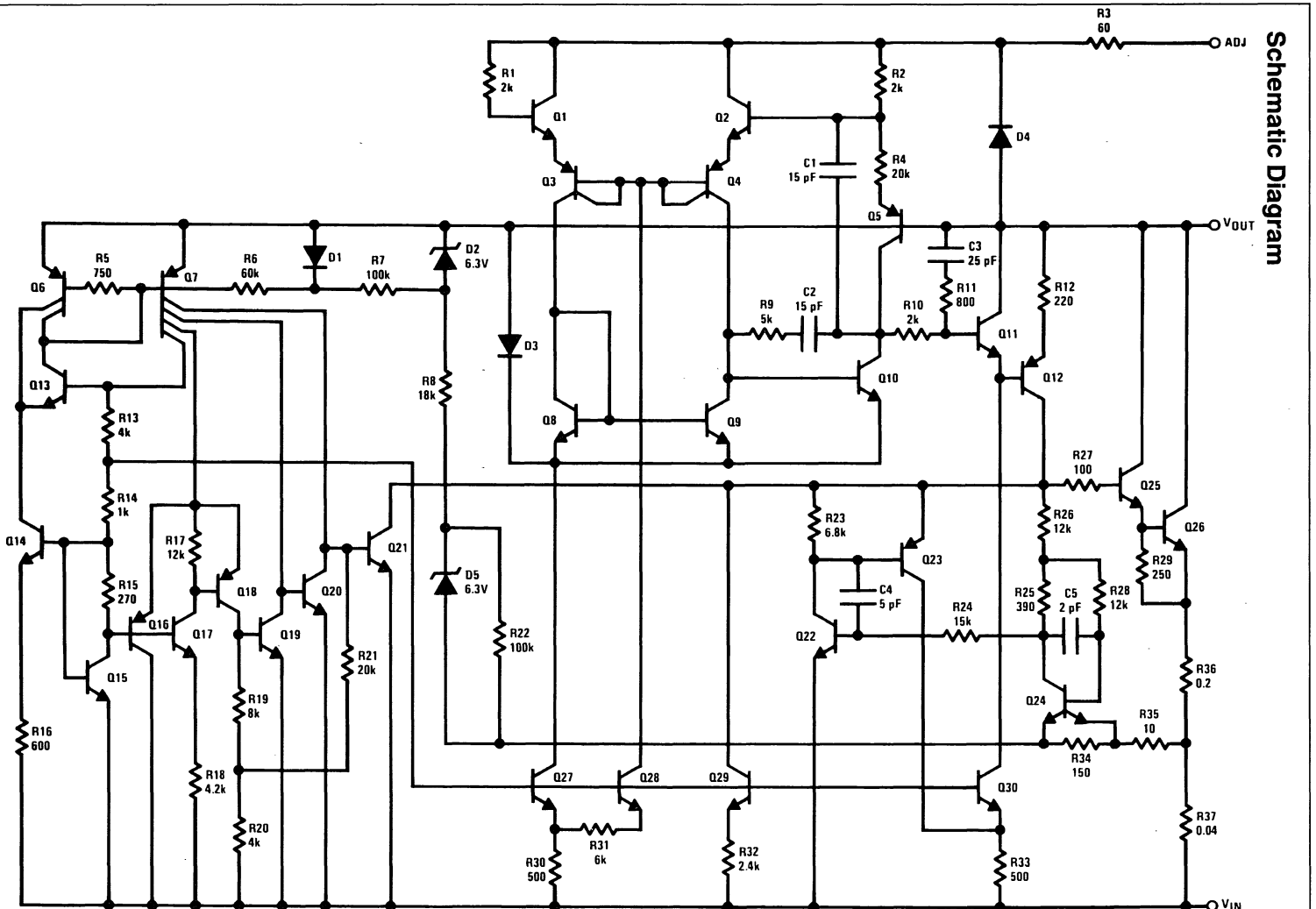
Parameter	Conditions	LM137HV			LM337HV			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_J = 25°C$, $3V \le \lvert V_{IN}-V_{OUT}\rvert \le 50V$, (Note 2) $I_L = 10$ mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_J = 25°C$, 10 mA $\le I_{OUT} \le I_{MAX}$		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_J = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	10 mA $\le I_L \le I_{MAX}$		2	5		2	5	μA
	$3.0V \le \lvert V_{IN}-V_{OUT}\rvert \le 50V$, $T_J = 25°$		4	6		3	6	μA
Reference Voltage	$T_J = 25°C$, (Note 3)	−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
	$3V \le \lvert V_{IN}-V_{OUT}\rvert \le 50V$, (Note 3)	−1.200	−1.250	−1.300	−1.200	−1.250	−1.300	V
	10 mA $\le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$							
Line Regulation	$3V \le \lvert V_{IN}-V_{OUT}\rvert \le 50V$, (Note 2) $I_L = 10$ mA		0.02	0.05		0.02	0.07	%/V
Load Regulation	10 mA $\le I_{OUT} \le I_{MAX}$, (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \le 50V$		2.5	5		2.5	10	mA
	$\lvert V_{IN}-V_{OUT}\rvert \le 10V$		1.2	3		1.5	6	mA
Current Limit	$\lvert V_{IN}-V_{OUT}\rvert \le 13V$							
	K Package	1.5	2.2	3.2	1.5	2.2	3.5	A
	H Package	0.5	0.8	1.6	0.5	0.8	1.8	A
	$\lvert V_{IN}-V_{OUT}\rvert = 50V$							
	K Package	0.2	0.4	0.8	0.1	0.4	0.8	A
	H Package	0.1	0.17	0.5	0.050	0.17	0.5	A
RMS Output Noise, % of V_{OUT}	$T_J = 25°C$, 10 Hz $\le f \le$ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10$ μF	66	77		66	77		dB
Long-Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
Thermal Resistance	H Package		140			140		°C/W
	K Package		35			35		°C/W

Note 1: Unless otherwise specified, these specifications apply: $-55°C \le T_j \le +150°C$ for the LM137HV, $0°C \le T_j \le +125°C$ for the LM337HV; $V_{IN}-V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 package and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulations. Load regulation is measured on the output pin at a point 1/8" below the base of the TO-3 and TO-39 packages.

Note 3: Refer to RETS237HVH drawing for LM137HVH or RETS137HVK for LM137HVK military specifications.

Schematic Diagram

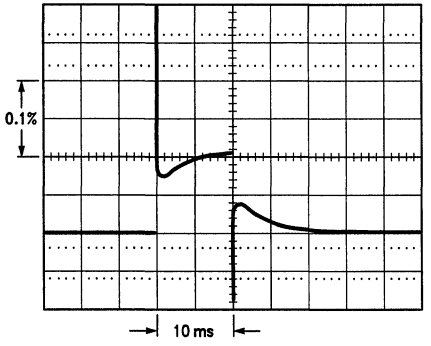


TL/H/9066–2

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137HV's specification is 0.02%/W, max.

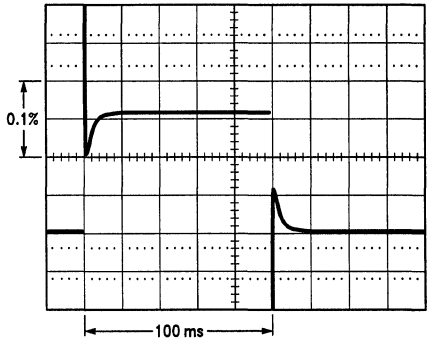
In *Figure 1,* a typical LM137HV's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137HV chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2,* when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



TL/H/9066-3

LM137HV, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

FIGURE 1



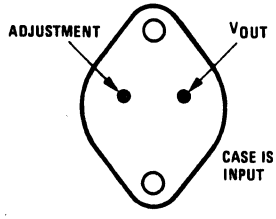
TL/H/9066-4

LM137HV, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

FIGURE 2

Connection Diagram (See Physical Dimensions section for further information)

TO-3
Metal Can Package

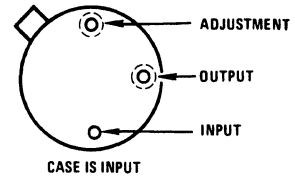


TL/H/9066-5

Bottom View

Order Number LM137HVK Steel or LM337HVK Steel
See NS Package Number K02A

TO-39
Metal Can Package



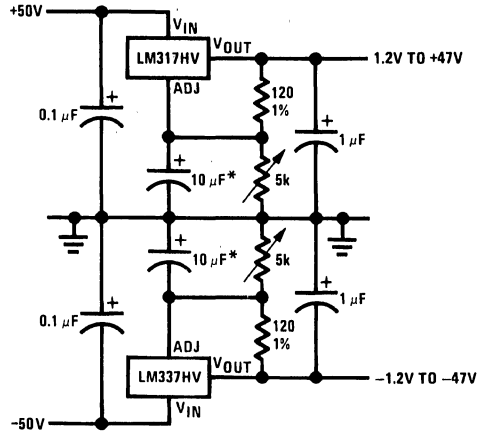
TL/H/9066-6

Bottom View

Order Number LM137HVH or LML337HVH
See NS Package Number H03B

Typical Applications (Continued)

Adjustable High Voltage Regulator

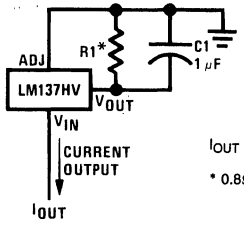


TL/H/9066-7

Full output current not available
at high input-output voltages

*The 10 μF capacitors are optional to improve ripple rejection

Current Regulator

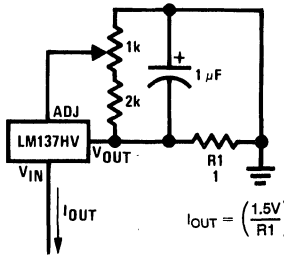


$I_{OUT} = \frac{V_{REF}}{R1}$

* 0.8Ω ≤ R1 ≤ 120Ω

TL/H/9066-8

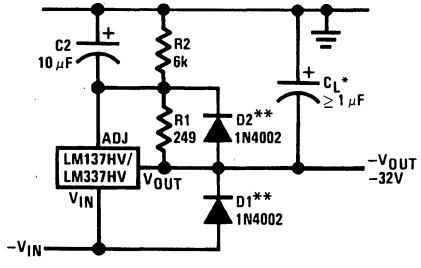
Adjustable Current Regulator



$I_{OUT} = \left(\frac{1.5V}{R1}\right)$ ±15% adjustable

TL/H/9066-9

Negative Regulator with Protection Diodes

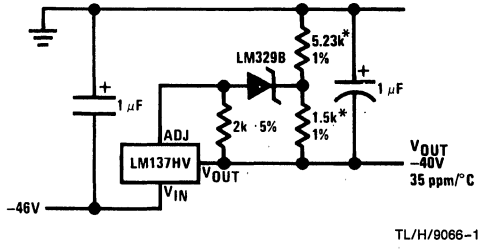


TL/H/9066-10

*When C_L is larger than 20 μF, D1 protects the LM137HV in case the input supply is shorted

**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137HV is case the output is shorted

High Stability −40V Regulator

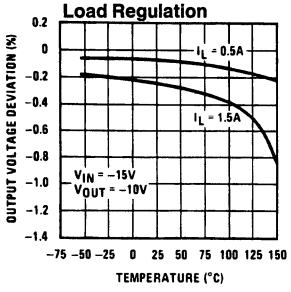


TL/H/9066-11

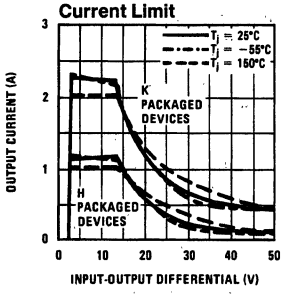
* Use resistors with good tracking TC < 25 ppm/°C

Typical Performance Characteristics (H and K-STEEL Package)

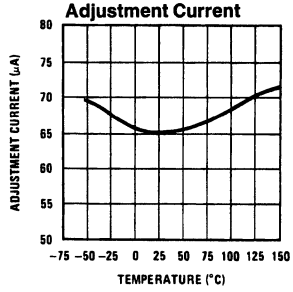
Load Regulation



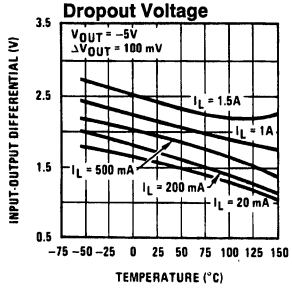
Current Limit



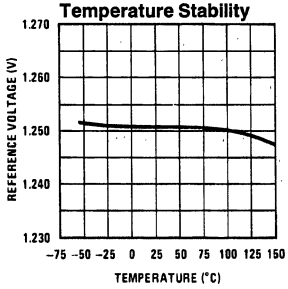
Adjustment Current



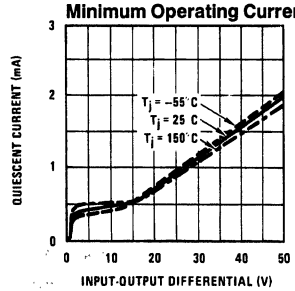
Dropout Voltage



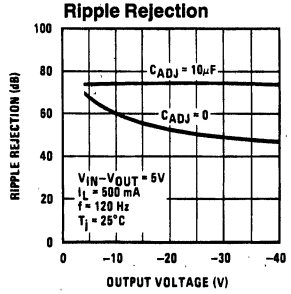
Temperature Stability



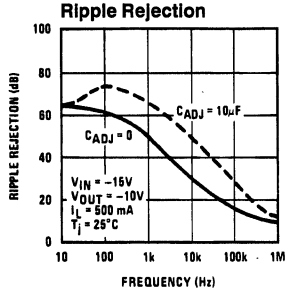
Minimum Operating Current



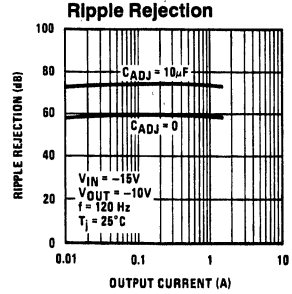
Ripple Rejection



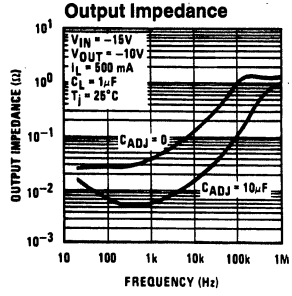
Ripple Rejection



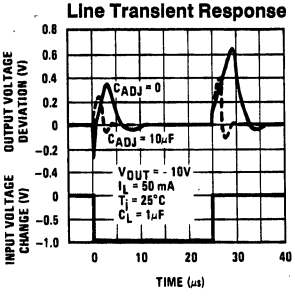
Ripple Rejection



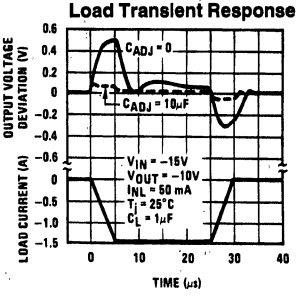
Output Impedance



Line Transient Response



Load Transient Response



TL/H/9066–12

National Semiconductor

LM138A/LM138, LM338A/LM338 5-Amp Adjustable Regulators

General Description

The LM138 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation—comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., do not short-circuit output to ground. The part numbers in the LM138 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM138A/LM138 are rated for $-55°C \leq T_J \leq +150°C$, while the LM338A is rated for $-40°C \leq T_J \leq +125°C$, and the LM338 is rated for $0°C \leq T_J \leq +125°C$.

Features

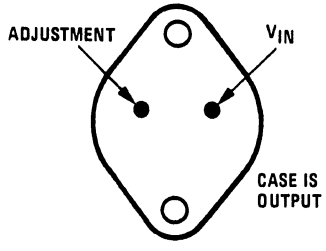
- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Guaranteed thermal regulation
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- Output is short-circuit protected
- Guaranteed 1% output voltage tolerance (LM138A, LM338A)
- Guaranteed max. 0.01%/V line regulation (LM138A, LM338A)
- Guaranteed max. 0.3% load regulation (LM138A, LM338A)

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

Connection Diagrams (See Physical Dimension section for further information)

(TO-3 STEEL)
Metal Can Package

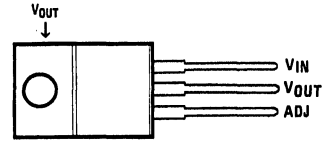


TL/H/9060–30

Bottom View

Order Number LM138AK STEEL/LM138K STEEL/ LM338AK STEEL/LM338K STEEL
See NS Package Number K02A

(TO-220)
Plastic Package



TL/H/9060–31

Front View

Order Number LM338AT/LM338T
See NS Package Number T03B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

Power Dissipation	Internally limited
Input/Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance	TBD

Operating Temperature Range

LM138A/LM138	$-55°C \le T_J \le +150°C$
LM338A	$-40°C \le T_J \le +125°C$
LM338	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V; and I_{OUT} = 10 mA. (Note 2)

Parameter	Conditions	LM138A			LM138			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 35V$, $10 mA \le I_{OUT} \le 5A$, $P \le 50W$	**1.225**	**1.250**	**1.270**	**1.19**	**1.24**	**1.29**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 35V$ (Note 3)		0.005	0.01		0.005	0.01	%/V
			0.02	**0.04**		**0.02**	**0.04**	%/V
Load Regulation	$10 mA \le I_{OUT}) \le 5V$ (Note 3)		0.1	0.3		0.1	0.3	%
			0.3	**0.6**		**0.3**	**0.6**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.01	%/W
Adjustment Pin Current			**45**	**100**		**45**	**100**	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le 5A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$V_{IN} - V_{OUT} \le 10V$							
	DC	**5**	**8**		**5**	**8**		A
	0.5 ms Peak	**7**	**12**		**7**	**12**		A
	$V_{IN} - V_{OUT}$ = 30V			1			1	A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**60**			**60**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**60**	**75**		**60**	**75**		dB
Long-Term Stability	T_J = 125°C, 1000 Hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package			1			1	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V; and I_{OUT} = 10 mA. (Note 2)

Parameter	Conditions	LM338A			LM338			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V, 10 mA ≤ I_{OUT} ≤ 5A, P ≤ 50W	**1.225**	**1.250**	**1.270**	**1.19**	**1.24**	**1.29**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V (Note 3)		0.005	0.01		0.005	0.03	%/V
			0.02	**0.04**		**0.02**	**0.06**	%/V
Load Regulation	10 mA ≤ I_{OUT}) ≤ 5V (Note 3)		0.1	0.3		0.1	0.5	%
			0.3	**0.6**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.002	0.02		0.002	0.02	%/W
Adjustment Pin Current			**45**	**100**		**45**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ 5A, 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	T_{MIN} ≤ T_J ≤ T_{MAX}		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	$V_{IN} - V_{OUT}$ ≤ 10V DC 0.5 ms Peak	**5** **7**	**8** **12**		**5** **7**	**8** **12**		A A
	$V_{IN} - V_{OUT}$ = 30V			1			1	A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**60**	**60** **75**		**60**	**60** **75**		dB dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance Junction to Case	K Package T Package			1 4			1 4	°C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package T Package		35 50			35 50		°C/W °C/W

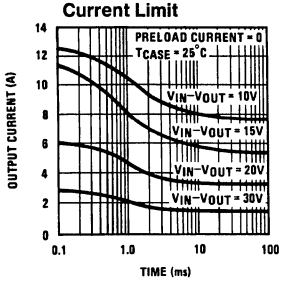
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

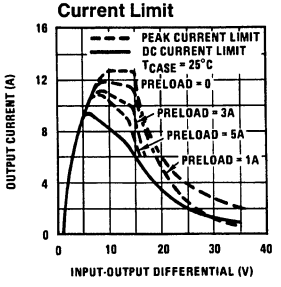
Note 2: These specifications are applicable for power dissipations up to 50W for the TO-3 (K) package and 25W for the TO-220 (T) package. Power dissipation is guaranteed at these values up to 15V input-output differential. Above 15V differential, power dissipation will be limited by internal protection circuitry. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

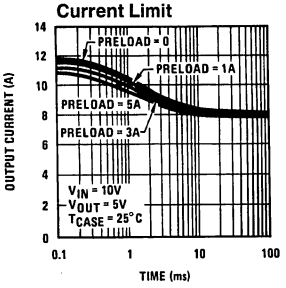
Note 3: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

Note 4: Refer to RETS138K drawing for military specifications of LM138K.

Typical Performance Characteristics







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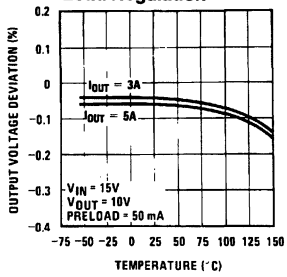
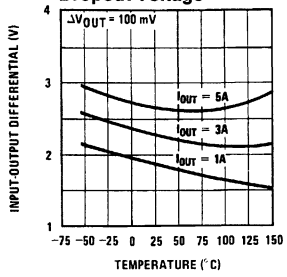
Typical Performance Characteristics (Continued)

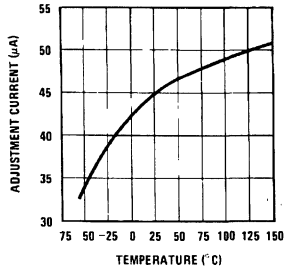
Load Regulation



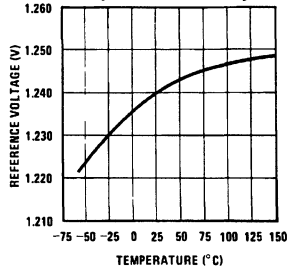
Dropout Voltage



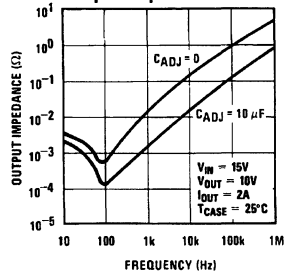
Adjustment Current



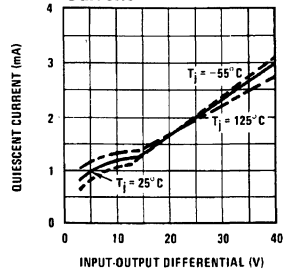
Temperature Stability



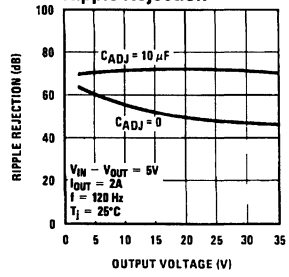
Output Impedance



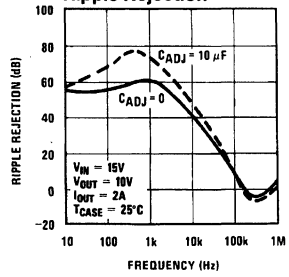
Minimum Operating Current



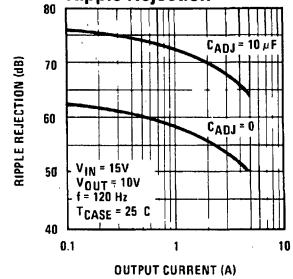
Ripple Rejection



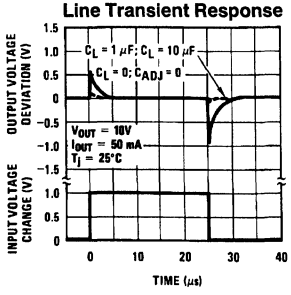
Ripple Rejection



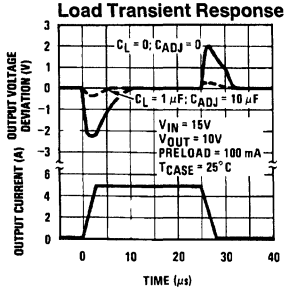
Ripple Rejection



Line Transient Response



Load Transient Response

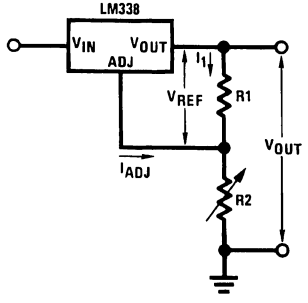


TL/H/9060–5

Application Hints

In operation, the LM138 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$



TL/H/9060–6

FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM138 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassiing when adjustment or output capacitors are used but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM138 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 75 dB ripple rejection is obtainable at any output level. Increases over 20 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

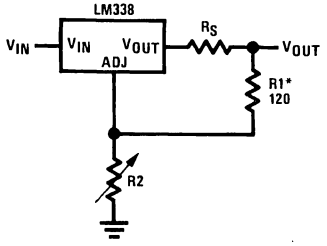
In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM138 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM138 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator (case) rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9060–7

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

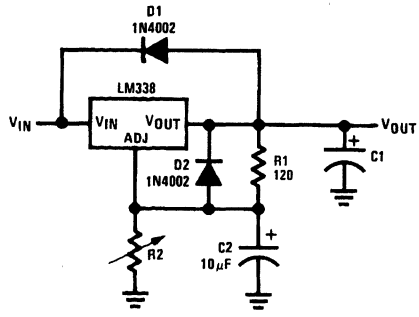
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 20 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM138 this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 100 μF or less at output of 15V or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM138 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM138 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Application Hints (Continued)



TL/H/9060–8

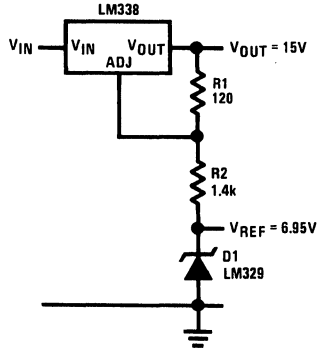
D1 protects against C1
D2 protects against C2

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

FIGURE 3. Regulator with Protection Diodes

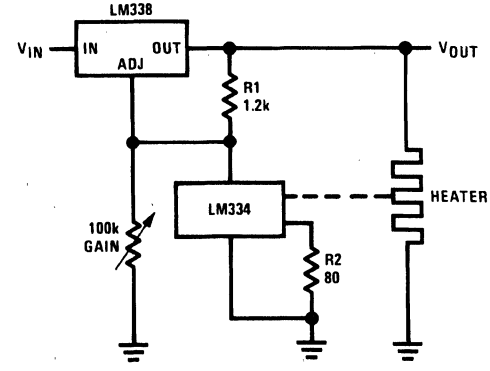
Typical Applications

Regulator and Voltage Reference



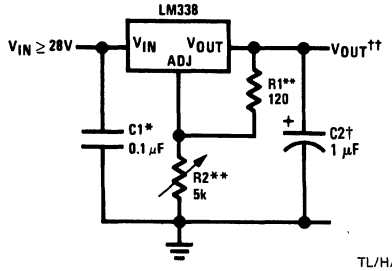
TL/H/9060–3

Temperature Controller



TL/H/9060–10

1.2V–25V Adjustable Regulator



TL/H/9060–1

Full output current not available
at high input-output voltages

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

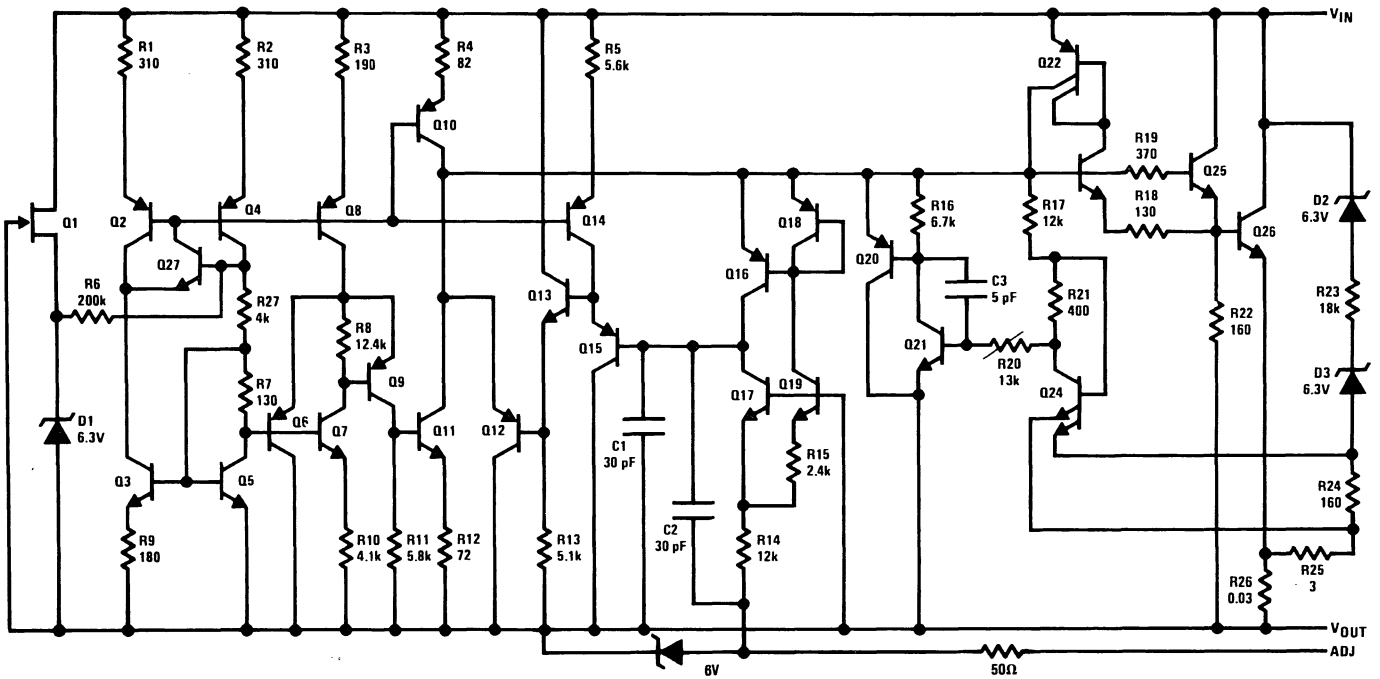
$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,(R_2)$$

**R1 = 240Ω for LM138. R1, R2 as an assembly can be ordered from Bourns:

MIL part no. 7105A-AT2-502

COMM part no. 7105A-AT7-502

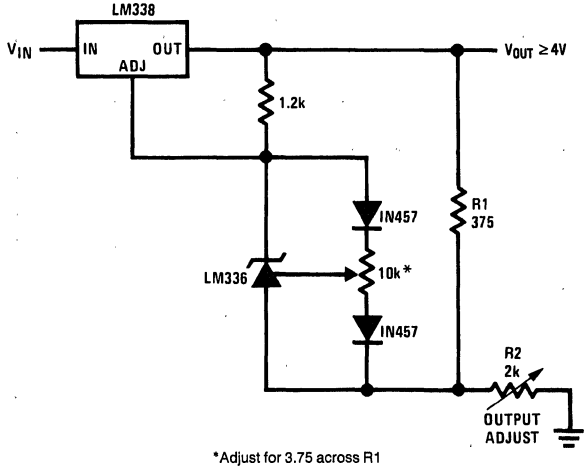
Schematic Diagram



TL/H/9060–9

Typical Applications (Continued)

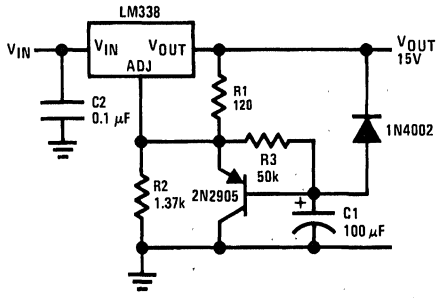
Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75 across R1

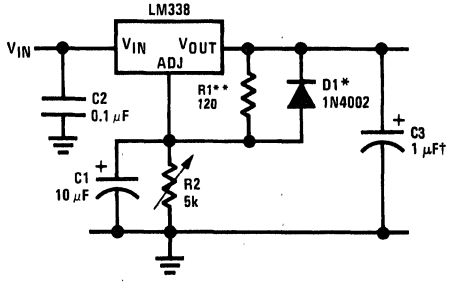
TL/H/9060–12

Slow Turn-On 15V Regulator



TL/H/9060–13

Adjustable Regulator with Improved Ripple Rejection



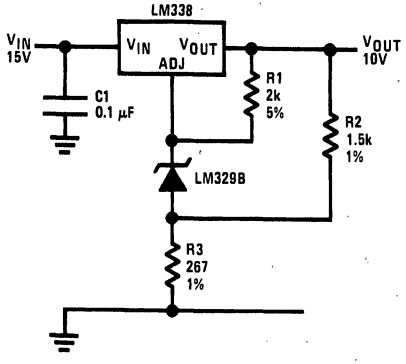
TL/H/9060–14

†Solid tantalum

*Discharges C1 if output is shorted to ground

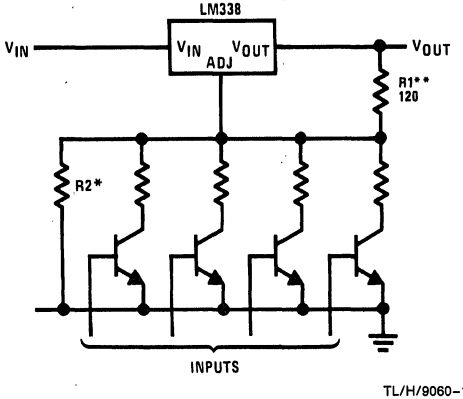
**R1 = 240Ω for LM138

High Stability 10V Regulator



TL/H/9060–15

Digitally Selected Outputs



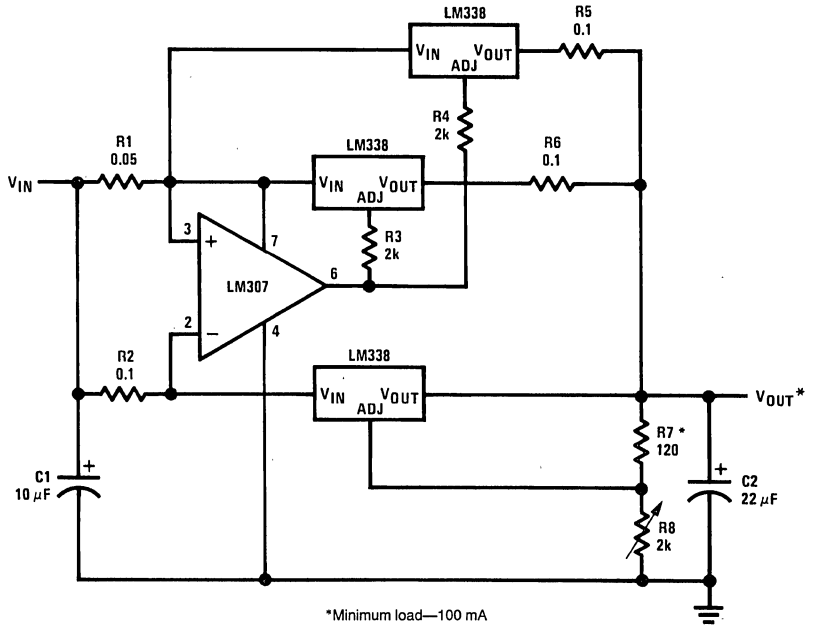
TL/H/9060–16

*Sets maximum V_{OUT}

**R1 = 240Ω for LM138

Typical Applications (Continued)

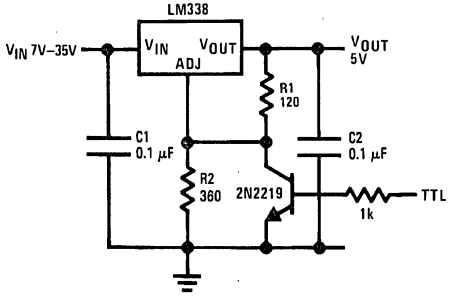
15A Regulator



*Minimum load—100 mA

TL/H/9060–17

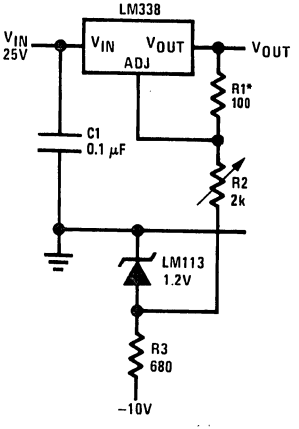
5V Logic Regulator with Electronic Shutdown**



**Minimum output ≈ 1.2V

TL/H/9060–18

0 to 22V Regulator

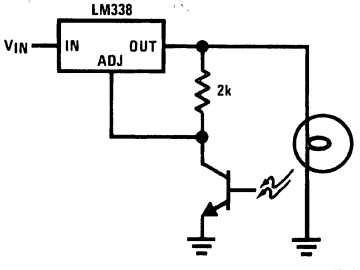


TL/H/9060–19

*R1 = 240Ω, R2 = 5k for LM138

Full output current not available at high input-output voltages

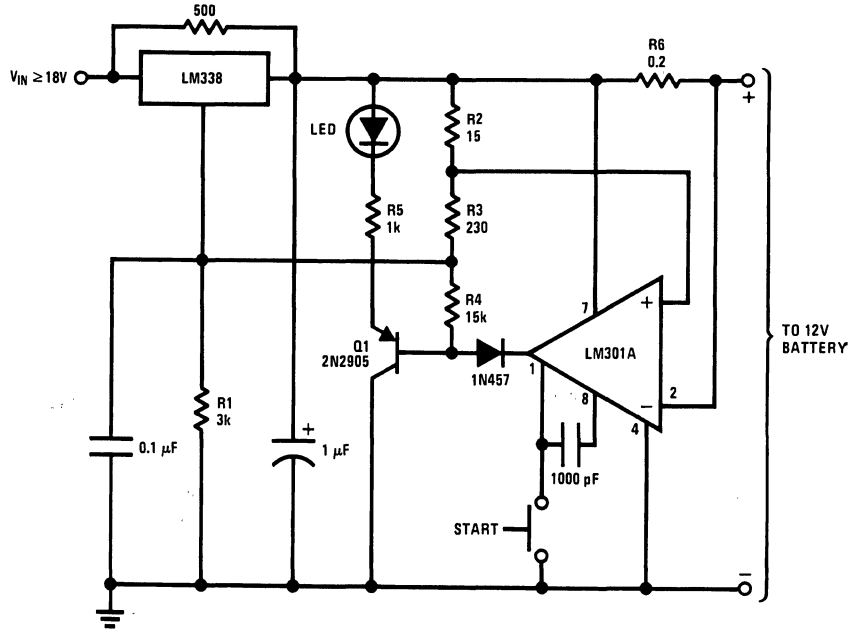
Light Controller



TL/H/9060–11

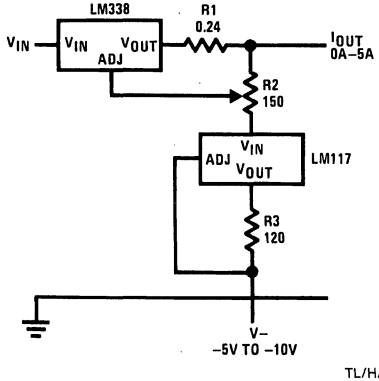
Typical Applications (Continued)

12V Battery Charger



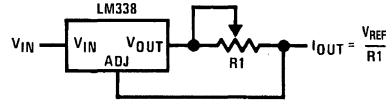
TL/H/9060–20

Adjustable Current Regulator



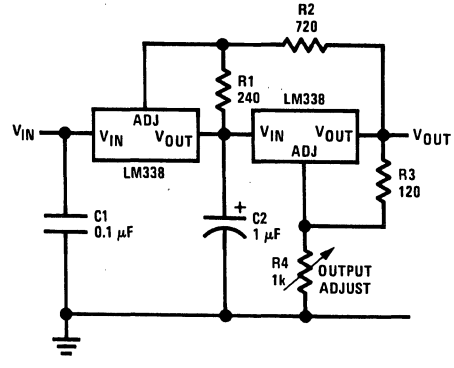
TL/H/9060–21

Precision Current Limiter



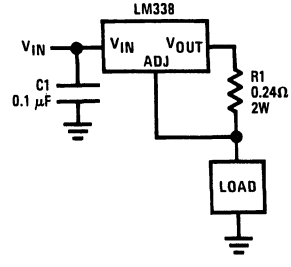
TL/H/9060–22

Tracking Preregulator



TL/H/9060–24

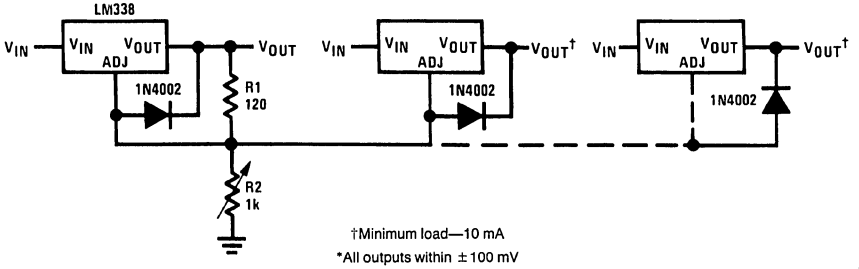
5A Current Regulator



TL/H/9060–23

Typical Applications (Continued)

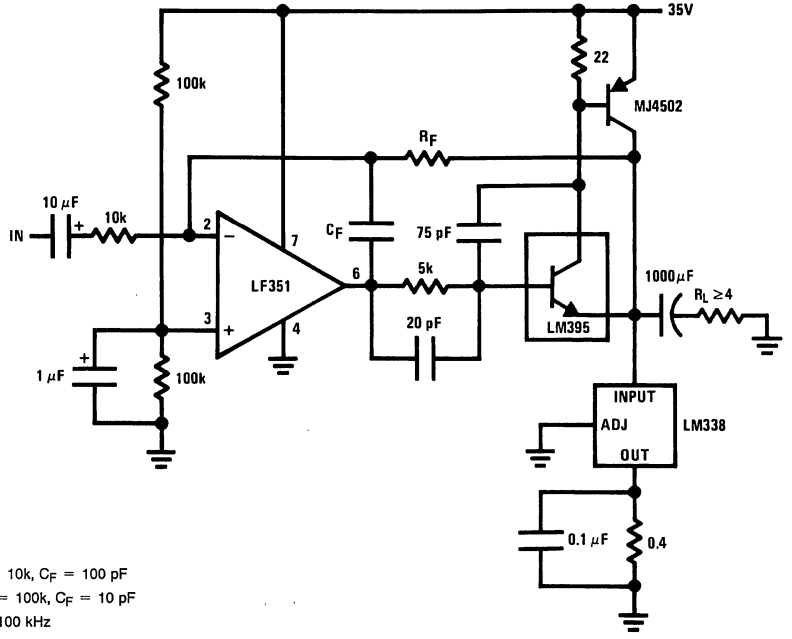
Adjusting Multiple On-Card Regulators with Single Control*



†Minimum load—10 mA
*All outputs within ±100 mV

TL/H/9060–25

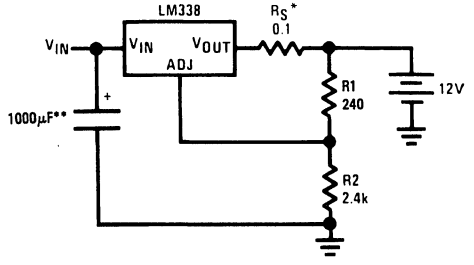
Power Amplifier



A_V = 1, R_F = 10k, C_F = 100 pF
A_V = 10, R_F = 100k, C_F = 10 pF
Bandwidth ≥ 100 kHz
Distortion ≤ 0.1%

TL/H/9060–27

Simple 12V Battery Charger



TL/H/9060–28

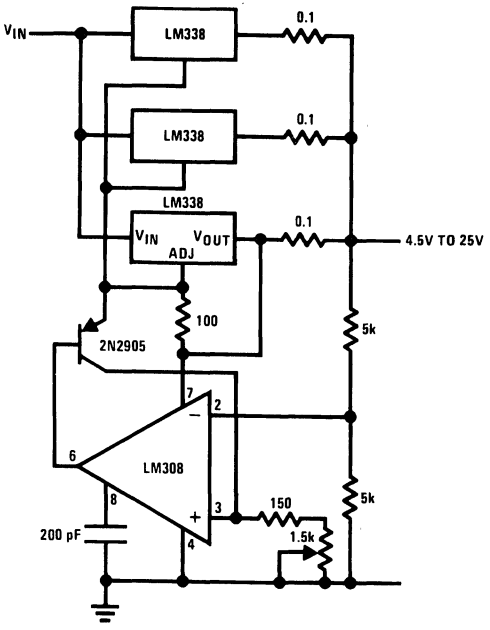
*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

**The 1000 μF is recommended to filter out input transients

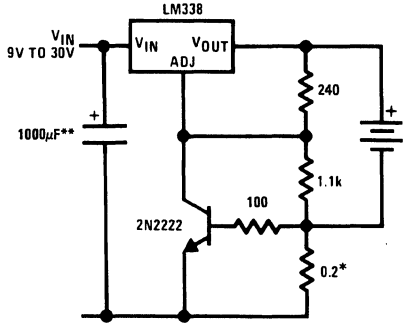
Typical Applications (Continued)

Adjustable 15A Regulator



TL/H/9060–26

Current Limited 6V Charger

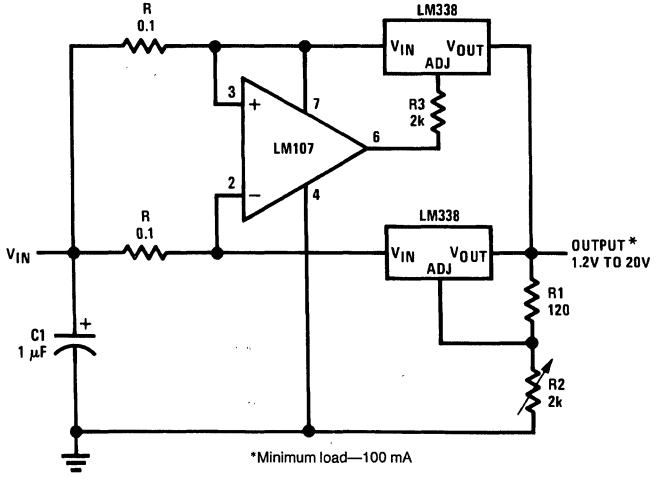


TL/H/9060–29

*Set max charge current to 3A

**The 1000 μF is recommended to filter out input transients.

10A Regulator



*Minimum load—100 mA

TL/H/9060–2

National Semiconductor

LM140A/LM140/LM340A/LM340 Series 3-Terminal Positive Regulators

General Description

The LM140A/LM140/LM340A/LM340 series of positive 3-terminal voltage regulators are designed to provide superior performance as compared to the previously available 78XX series regulator. Computer programs were used to optimize the electrical and thermal performance of the packaged IC which results in outstanding ripple rejection, superior line and load regulation in high power applications (over 15W).

With these advances in design, the LM340 is now guaranteed to have line and load regulation that is a factor of 2 better than previously available devices. Also, all parameters are guaranteed at 1A vs 0.5A output current. The LM140A/LM340A provide tighter output voltage tolerance, ±2% along with 0.01%/V line regulation and 0.3%/A load regulation.

Current limiting is included to limit peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over limiting die temperature.

Considerable effort was expended to make the LM140-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The entire LM140A/LM140/LM340A/LM340 series of regulators is available in the steel TO-3 power package. The LM340A/LM340 series is also available in the TO-220 plastic power package as well as an aluminum TO-3 package.

For output voltages other than 5V, 12V, and 15V, the LM117 and LM117HV series provide an output voltage range from +1.2V to +57V.

Features

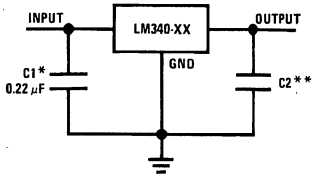
- Complete specifications at 1A load
- Output voltage tolerances of ±2% at T_j = 25°C and ±4% over the temperature range (LM140A/LM340A)
- Fixed output voltages available 5, 12, and 15V
- Line regulation of 0.01% of V_{OUT}/V of ΔV_{IN} at 1A load (LM140A/LM340A)
- Load regulation of 0.3% of V_{OUT}/A (LM140A/LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- 100% thermal limit burn-in
- Special circuitry allows start-up even if output is pulled to negative voltage (±supplies)

LM140 Series Package and Power Capability

Device	Package	Rated Power Dissipation	Design Output Current
LM140/ LM340	TO-3 (K)	20W	1.5A
LM340	TO-220 (T)	15W	1.5A

Typical Applications

Fixed Output Regulator

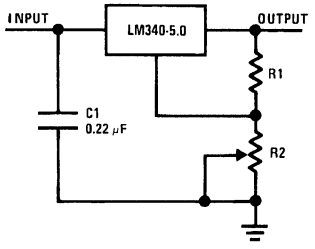


TL/H/7781–1

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 μF, ceramic disc).

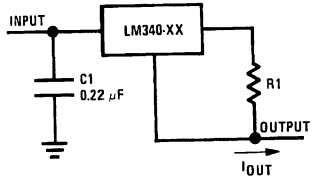
Adjustable Output Regulator



TL/H/7781–2

V_{OUT} = 5V + (5V/R1 + I_Q) R2 5V/R1 > 3 I_Q, load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM340-5).

Current Regulator



TL/H/7781–3

$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes.

1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Input Voltage (V_O = 5V, 12V, 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	
LM140A/LM140	−55°C to +125°C
LM340A/LM340	0°C to +70°C
Maximum Junction Temperature	
(TO-3 Package K, KC)	150°C
(TO-220 Package T)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K, KC	300°C
TO-220 Package T	230°C
ESD Tolerance (Note 4)	2000V

Electrical Characteristics LM140A/LM340A (Note 2)

I_{OUT} = 1A, −55°C ≤ T_j ≤ +150°C (LM140A), or 0°C ≤ T_j ≤ + 125°C (LM340A) unless otherwise specified

Symbol	Output Voltage		5V			12V			15V			Units
	Input Voltage (unless otherwise noted)		10V			19V			23V			
	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_j = 25°C	4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A	4.8		5.2	11.5		12.5	14.4		15.6	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA			10			18			22	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		T_j = 25°C		3	10		4	18		4	22	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
		T_j = 25°C			4			9			10	mV
		Over Temperature			12			30			30	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	T_j = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	25		12	32		12	35	mV
		250 mA ≤ I_O ≤ 750 mA			15			19			21	mV
		Over Temperature, 5 mA ≤ I_O ≤ 1A			25			60			75	mV
I_Q	Quiescent Current	T_j = 25°C			6			6			6	mA
		Over Temperature			6.5			6.5			6.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5	mA
		T_j = 25°C, I_O = 1A			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O = 500 mA			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(17.9 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	T_j = 25°C, f = 120 Hz, I_O = 1A	68	80		61	72		60	70		dB
		or f = 120 Hz, I_O = 500 mA,	68			61			60			dB
		Over Temperature,										
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	T_j = 25°C, I_O = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	T_j = 25°C		2.1			1.5			1.2		A
	Peak Output Current	T_j = 25°C		2.4			2.4			2.4		A
	Average TC of V_O	Min, T_j = 0°C, I_O = 5 mA		−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_j = 25°C	7.5			14.5			17.5			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 3: Refer to RETS140A-12K for LM140K-12, RETS140A-15K for LM140K-15, or RETS140A-05K for LM140K-5.0 military drawing specifications.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics LM140 (Note 2) $-55°C \le T_j \le +150°C$ unless otherwise specified

Symbol	Output Voltage / Input Voltage (unless otherwise noted) / Parameter	Conditions		5V / 10V Min	5V / 10V Typ	5V / 10V Max	12V / 19V Min	12V / 19V Typ	12V / 19V Max	15V / 23V Min	15V / 23V Typ	15V / 23V Max	Units
V_O	Output Voltage	$T_j = 25°C$, 5 mA $\le I_O \le$ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le$ 15W, 5 mA $\le I_O \le$ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \le V_{IN} \le V_{MAX}$		(8 ≤ V_{IN} ≤ 20)			(15.5 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	$T_j = 25°C$		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			$-55°C \le T_j \le +150°C$			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		$I_O \le$ 1A	$T_j = 25°C$			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			$-55°C \le T_j \le +150°C$			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	$T_j = 25°C$	5 mA $\le I_O \le$ 1.5A		10	50		12	120		12	150	mV
			250 mA $\le I_P \le$ 750 mA			25			60			75	mV
		$-55°C \le T_j \le +150°C$, 5 mA $\le I_O \le$ 1A				50			120			150	mV
I_Q	Quiescent Current	$I_O \le$ 1A	$T_j = 25°C$			6			6			6	mA
			$-55°C \le T_j \le +150°C$			7			7			7	mA
ΔI_Q	Quiescent Current Change	5 mA $\le I_O \le$ 1A				0.5			0.5			0.5	mA
		$T_j = 25°C$, $I_O \le$ 1A				0.8			0.8			0.8	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$		(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O = 500 mA, $-55°C \le T_j \le +150°C$				0.8			0.8			0.8	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$		(8 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(18.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	$I_O \le$ 1A, $T_j = 25°C$ or	68	80		61	72		60	70		dB
			$I_O \le$ 500 mA,	68			61			60			dB
			$-55°C \le T_j \le +150°C$										
		$V_{MIN} \le V_{IN} \le V_{MAX}$		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	$T_j = 25°C$, I_O = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	$T_j = 25°C$			2.1			1.5			1.2		A
	Peak Output Current	$T_j = 25°C$			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \le T_j \le +150°C$, I_O = 5 mA			−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O \le$ 1A			7.5			14.6			17.7		V

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

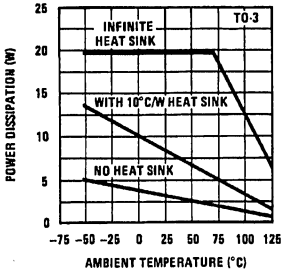
Electrical Characteristics LM340 (Note 2) $0°C \le T_j \le +125°C$ unless otherwise specified

Symbol	Output Voltage / Input Voltage (unless otherwise noted) / Parameter	Conditions	5V / 10V Min	5V / 10V Typ	5V / 10V Max	12V / 19V Min	12V / 19V Typ	12V / 19V Max	15V / 23V Min	15V / 23V Typ	15V / 23V Max	Units
V_O	Output Voltage	$T_j = 25°C$, $5\ mA \le I_O \le 1A$	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le 15W$, $5\ mA \le I_O \le 1A$	4.75	5.25		11.4		12.6	14.25		15.75	V
		$V_{MIN} \le V_{IN} \le V_{MAX}$	$(7.5 \le V_{IN} \le 20)$			$(14.5 \le V_{IN} \le 27)$			$(17.5 \le V_{IN} \le 30)$			V
ΔV_O	Line Regulation	$I_O = 500\ mA$, $T_j = 25°C$		3	50		4	120		4	150	mV
		ΔV_{IN}	$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$			V
		$0°C \le T_j \le +125°C$			50			120			150	mV
		ΔV_{IN}	$(8 \le V_{IN} \le 20)$			$(15 \le V_{IN} \le 27)$			$(18.5 \le V_{IN} \le 30)$			V
		$I_O \le 1A$, $T_j = 25°C$			50			120			150	mV
		ΔV_{IN}	$(7.5 \le V_{IN} \le 20)$			$(14.6 \le V_{IN} \le 27)$			$(17.7 \le V_{IN} \le 30)$			V
		$0°C \le T_j \le +125°C$			25			60			75	mV
		ΔV_{IN}	$(8 \le V_{IN} \le 12)$			$(16 \le V_{IN} \le 22)$			$(20 \le V_{IN} \le 26)$			V
ΔV_O	Load Regulation	$T_j = 25°C$, $5\ mA \le I_O \le 1.5A$		10	50		12	120		12	150	mV
		$250\ mA \le I_O \le 750\ mA$			25			60			75	mV
		$5\ mA \le I_O \le 1A$, $0°C \le T_j \le +125°C$			50			120			150	mV
I_Q	Quiescent Current	$I_O \le 1A$, $T_j = 25°C$			8			8			8	mA
		$0°C \le T_j \le +125°C$			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	$5\ mA \le I_O \le 1A$			0.5			0.5			0.5	mA
		$T_j = 25°C$, $I_O \le 1A$			1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$	$(7.5 \le V_{IN} \le 20)$			$(14.8 \le V_{IN} \le 27)$			$(17.9 \le V_{IN} \le 30)$			V
		$I_O = 500\ mA$, $0°C \le T_j \le +125°C$			1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$	$(7 \le V_{IN} \le 25)$			$(14.5 \le V_{IN} \le 30)$			$(17.5 \le V_{IN} \le 30)$			V
V_N	Output Noise Voltage	$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$		40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120\ Hz$, $I_O \le 1A$, $T_j = 25°C$	62	80		55	72		54	70		dB
		or $I_O \le 500\ mA$, $0°C \le T_j \le +125°C$	62			55			54			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$	$(8 \le V_{IN} \le 18)$			$(15 \le V_{IN} \le 25)$			$(18.5 \le V_{IN} \le 28.5)$			V
R_O	Dropout Voltage	$T_j = 25°C$, $I_O = 1A$		2.0			2.0			2.0		V
	Output Resistance	$f = 1\ kHz$		8			18			19		mΩ
	Short-Circuit Current	$T_j = 25°C$		2.1			1.5			1.2		A
	Peak Output Current	$T_j = 25°C$		2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \le T_j \le +125°C$, $I_O = 5\ mA$		−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O \le 1A$	7.5			14.6			17.7			V

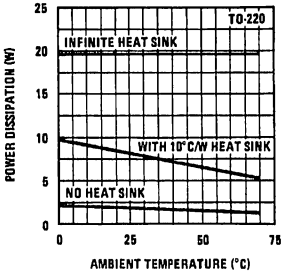
Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

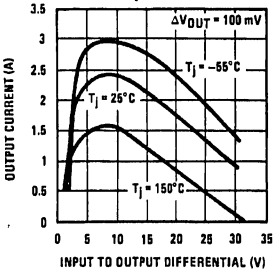
Maximum Average Power Dissipation



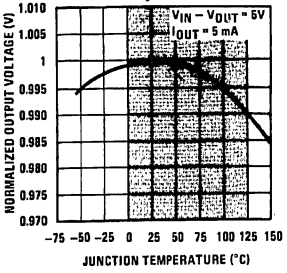
Maximum Average Power Dissipation



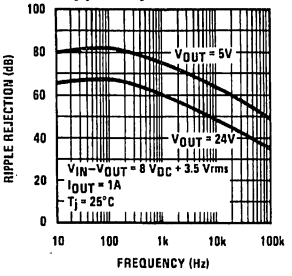
Peak Output Current



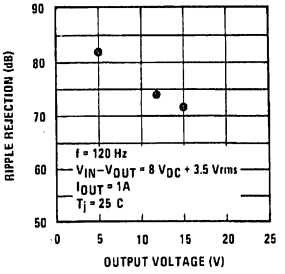
Output Voltage (Normalized to 1V at T_J = 25°C)



Ripple Rejection

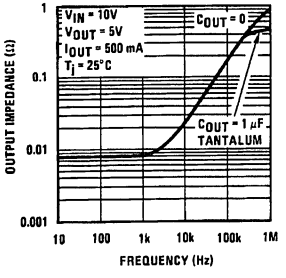


Ripple Rejection

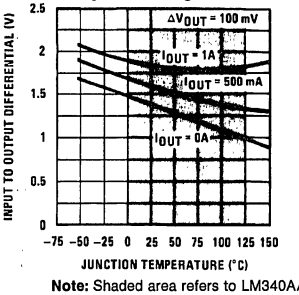


Note: Shaded area refers to LM340A/LM340.

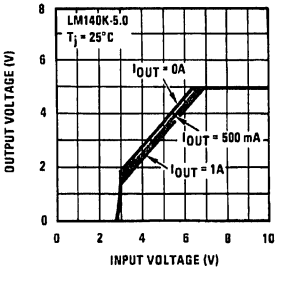
Output Impedance



Dropout Voltage

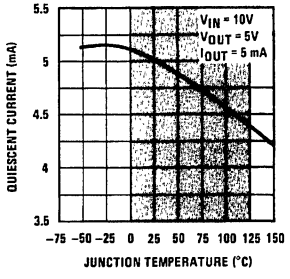


Dropout Characteristics

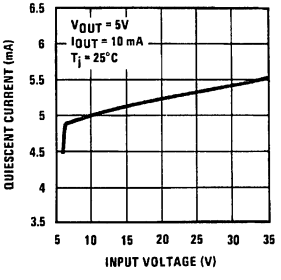


Note: Shaded area refers to LM340A/LM340.

Quiescent Current



Quiescent Current



Note: Shaded area refers to LM340A/LM340.

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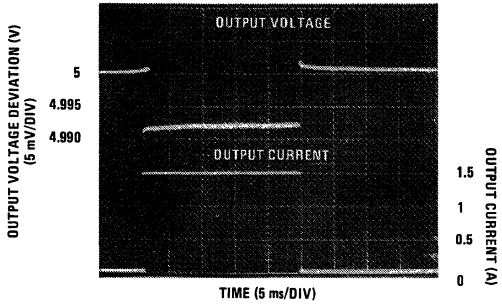
Typical Performance Characteristics (Continued)

Load Regulation
140AK-5.0, V_{IN} = 10V, T_A = 25°C



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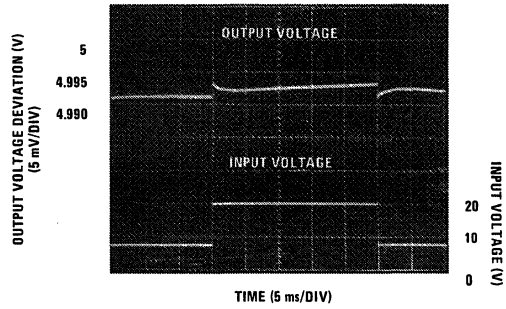
Line Regulation
140AK-5.0, I_{OUT} = 1A, T_A = 25°C



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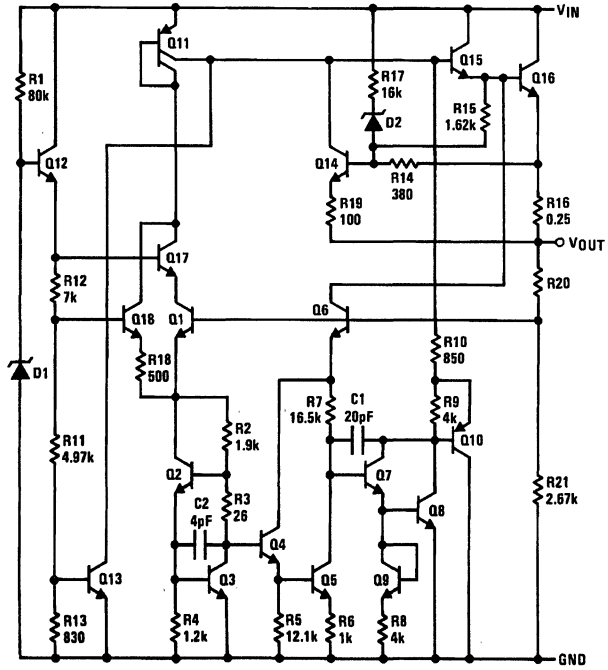
Equivalent Schematic



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Application Hints

The LM340 is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

Shorting the Regulator Input: When using large capacitors at the output of these regulators, a protection diode connected input to output *(Figure 1)* may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial V_{OUT} because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal and the regulator will be destroyed. The fast diode in *Figure 1* will shunt most of the capacitors discharge current around the regulator. Generally no protection diode is required for values of output capacitance $\leq 10\ \mu F$.

Raising the Output Voltage above the Input Voltage: Since the output of the LM340 does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the "Shorting the Regulator Input" section.

Regulator Floating Ground*(Figure 2)*: When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT}. If ground is reconnected with power "ON", damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, thermal limit ceases operating, or ground should be connected first if power must be left on.

Transient Voltages: If transients exceed the maximum rated input voltage of the 340, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

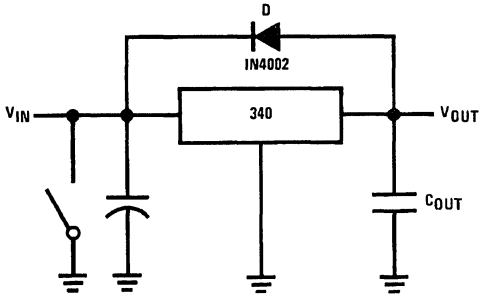

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FIGURE 1. Input Short

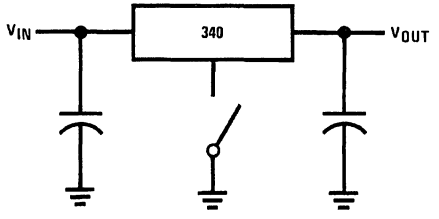

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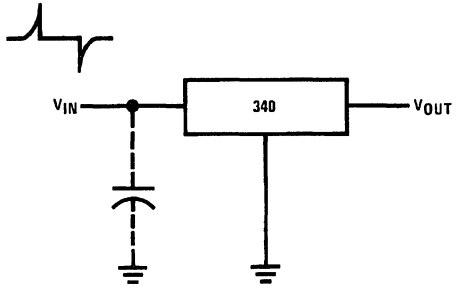
FIGURE 2. Regulator Floating Ground

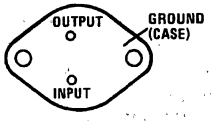


TL/H/7781–10

FIGURE 3. Transients

Connection Diagrams

TO-3 Metal Can Package (K and KC)



TL/H/7781–11

Bottom View

Steel Package Order Numbers:

LM140AK-5.0 LM140K-5.0 LM340AK-5.0 LM340K-5.0
LM140AK-12 LM140K-12 LM340AK-12 LM340K-12
LM140AK-15 LM140K-15 LM340AK-15 LM340K-15

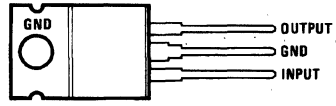
See Package Number K02A

Aluminum Package Order Numbers:

LM340KC-5.0
LM340KC-12
LM340KC-15

See Package Number KC02A

TO-220 Power Package (T)



TL/H/7781–12

Top View

Plastic Package Order Numbers:

LM340AT-5.0 LM340T-5.0
LM340AT-12 LM340T-12
LM340AT-15 LM340T-15

See Package Number T03B

National Semiconductor

LM140L/LM340L Series 3-Terminal Positive Regulators

General Description

The LM140L series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. The LM140LA is an improved version of the LM78LXX series with a tighter output voltage tolerance (specified over the full military temperature range), higher ripple rejection, better regulation and lower quiescent current. The LM140LA regulators have ±2% V_{OUT} specification, 0.04%/V line regulation, and 0.01%/mA load regulation. When used as a zener diode/resistor combination replacement, the LM140LA usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM140LA to be used in logic systems, instrumentation, Hi-Fi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The LM140LA/LM340LA are available in the low profile metal three lead TO-39 (H) and the LM340LA are also available in the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shut-down circuit takes over, preventing the IC from overheating.

For applications requiring other voltages, see LM117L Data Sheet.

Features

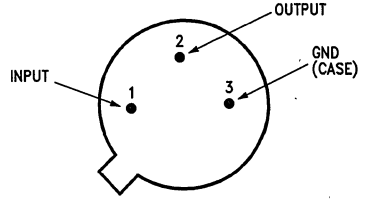
- Line regulation of 0.04%/V
- Load regulation of 0.01%/mA
- Output voltage tolerances of ±2% at T_j = 25°C and ±4% over the temperature range (LM140LA) ±3% over the temperature range (LM340LA)
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in metal TO-39 low profile package (LM140LA/LM340LA) and plastic TO-92 (LM340LA)

Output Voltage Options

LM140LA-5.0	5V	LM340LA-5.0	5V
LM140LA-12	12V	LM340LA-12	12V
LM140LA-15	15V	LM340LA-15	15V

Connection Diagrams

TO-39 Metal Can Package (H)

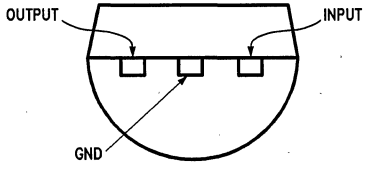


TL/H/7782–2

Bottom View

Order Number LM140LAH-5.0, LM140LAH-12, LM140LAH-15, LM340LAH-5.0, LM340LAH-12 or LM340LAH-15
See NS Package Number H03A

TO-92 Plastic Package (Z)



TL/H/7782–3

Bottom View

Order Number LM340LAZ-5.0, LM340LAZ-12 or LM340LAZ-15
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Input Voltage
5.0V, 12V, 15V Output Voltage Options 35V
Internal Power Dissipation (Note 1) Internally Limited

Operating Temperature Range
LM140LA −55°C to +125°C
LM340LA 0°C to +70°C
Maximum Junction Temperature +150°C
Storage Temperature Range
Metal Can (H package) −65°C to +150°C
Molded TO-92 −55°C to +150°C
Lead Temperature (Soldering, 10 sec.) +300°C
Plastic TO-92 +230°C

Electrical Characteristics (Note 2)

Test conditions unless otherwise specified. $T_A = -55°C$ to $+125°C$ (LM140LA), $T_A = 0°C$ to $+70°C$ (LM340LA), $I_O = 40$ mA, $C_{IN} = 0.33\ \mu F$, $C_O = 0.01\ \mu F$.

Output Voltage Option				5.0V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	$T_j = 25°C$		4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
	Output Voltage Over Temp. (Note 4)	LM140LA	$I_O = 1 - 100$ mA	4.8		5.2	11.5		12.5	14.4		15.6	V
				(7.2–20)			(14.5–27)			(17.6–30)			
		LM340LA	$I_O = 1 - 100$ mA or $I_O = 1 - 40$ mA and $V_{IN} = (\ )V$	4.85		5.15	11.65		12.35	14.55		15.45	
				(7–20)			(14.3–27)			(17.5–30)			
ΔV_O	Line Regulation	$T_j = 25°C$	$I_O = 40$ mA $V_{IN} = (\ )V$		18	30		30	65		37	70	mV
				(7–25)			(14.2–30)			(17.3–30)			
			$I_O = 100$ mA $V_{IN} = (\ )V$		18	30		30	65		37	70	
				(7.5–25)			(14.5–30)			(17.5–30)			
	Load Regulation	$T_j = 25°C$	$I_O = 1 - 40$ mA		5	20		10	40		12	50	
			$I_O = 1 - 100$ mA		20	40		30	80		35	100	
	Long Term Stability				12			24			30		mV 1000 hrs
I_O	Quiescent Current	$T_j = 25°C$			3	4.5		3	4.5		3.1	4.5	mA
		$T_j = 125°C$				4.2			4.2			4.2	
ΔI_Q	Quiescent Current Change	$T_j = 25°C$	ΔLoad $I_O = 1 - 40$ mA			0.1			0.1			0.1	mA
			ΔLine $V_{IN} = (\ )V$			0.5			0.5			0.5	
				(7.5–25)			(14.3–30)			(17.5–30)			
V_N	Output Noise Voltage	$T_j = 25°C$ (Note 3) $f = 10$ Hz–10 kHz			40			80			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	$f = 120$ Hz, $V_{IN} = (\ )V$		55	62		47	54		45	52		dB
				(7.5–18)			(14.5–25)			(17.5–28.5)			
	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O = 40$ mA		7			14.2			17.3			V

Note 1: Thermal resistance of H-package is typically 26°C/W θ_{jC}, 250°C/W θ_{jA} still air, and 94°C/W θ_{jA} 400 lf/min of air. For the Z-package is 60°C/W θ_{jC}, 232°C/W θ_{jA} still air, and 88°C/W θ_{jA} at 400 lf/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

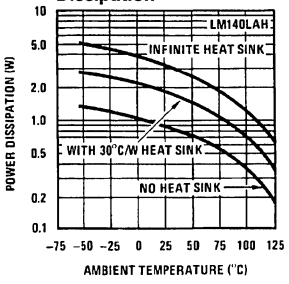
Note 3: It is recommended that a minimum load capacitor of 0.01 μF be used to limit the high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within 0.01% V_O/°C.

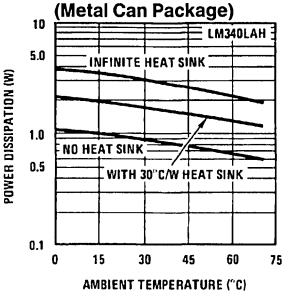
Note 5: Refer to RETS140-12H for LM140LAH-12, RETS140-15H for LM140LAH-15 or RETS140-15H for LM140LAH-5.0 military specification.

Typical Performance Characteristics

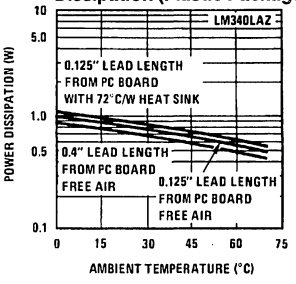
Maximum Average Power Dissipation



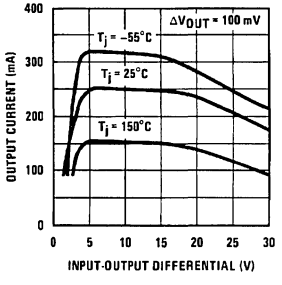
Maximum Average Power Dissipation (Metal Can Package)



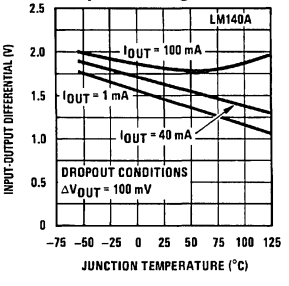
Maximum Average Power Dissipation (Plastic Package)



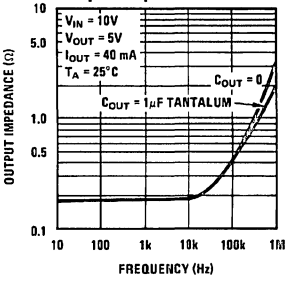
Peak Output Current



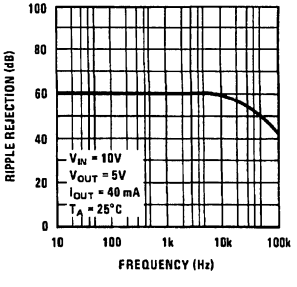
Dropout Voltage



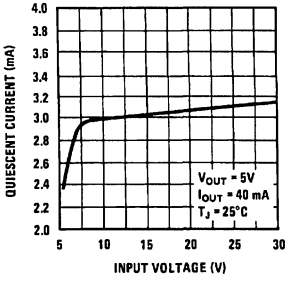
Output Impedance



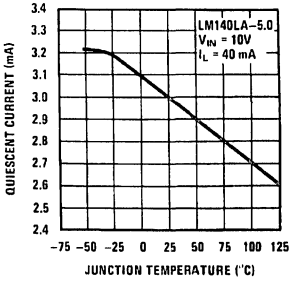
Ripple Rejection



Quiescent Current



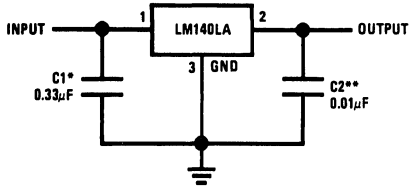
Quiescent Current



TL/H/7782–4

Typical Applications

Fixed Output Regulator

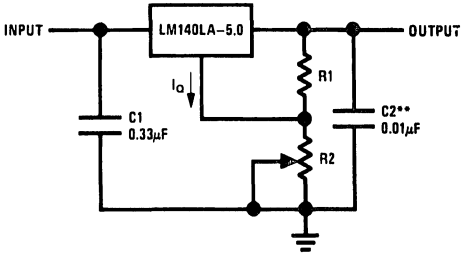


TL/H/7782–5

*Required if the regulator is located far from the power supply filter.

**See note 3 in the electrical characteristics table.

Adjustable Output Regulator

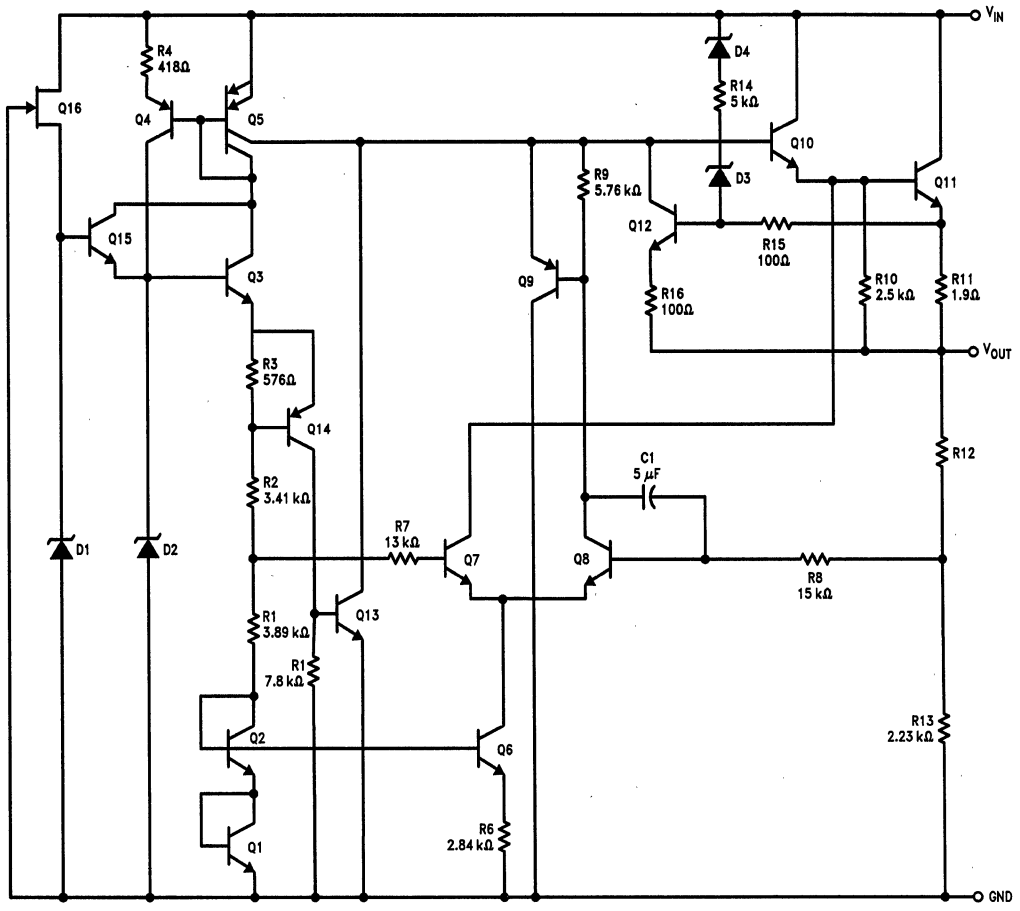


TL/H/7782–6

$V_{OUT} = 5V + (5V/R1 + I_Q) R2$

$5V/R1 = 3\ I_Q$ load regulation (L_r) $[(R1 + R2)/R1]$ (L_r of LM140LA-5.0)

Equivalent Circuit



TL/H/7782–1

National Semiconductor

LM145/LM345 Negative Three Amp Regulator

General Description

The LM145 is a three-terminal negative regulator with a fixed output voltage of −5V or −5.2V, and up to 3A load current capability. This device needs only one external component—a compensation capacitor at the output, making it easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM145 immune to overload conditions. The regulator has current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

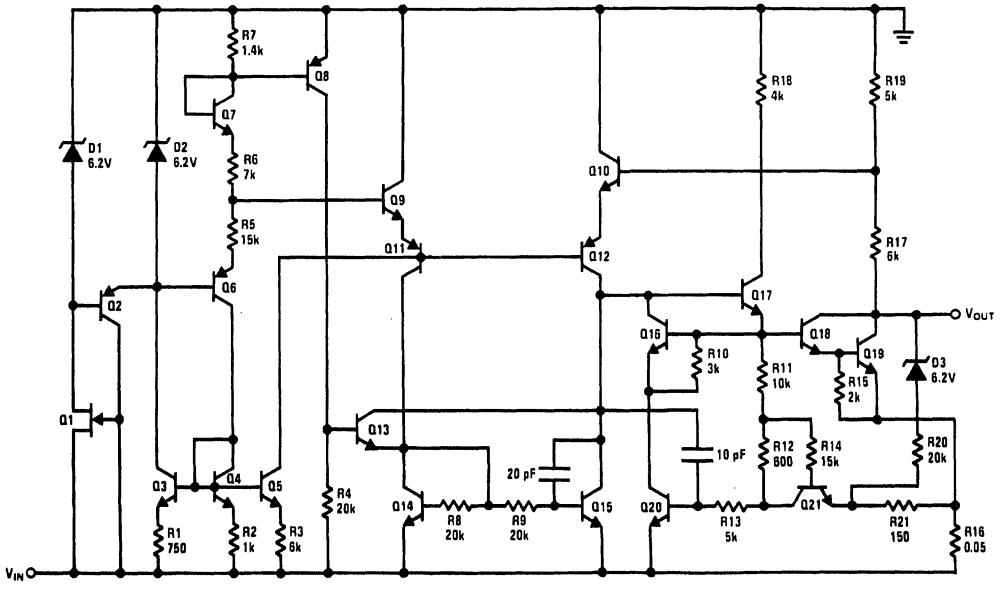
Although primarily intended for fixed output voltage applications, the LM145 may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the device allows this technique to be used with good regulation.

The LM145 comes in a hermetic TO-3 package rated at 25W. A reduced temperature range part LM345 is also available.

Features

- Output voltage accurate to better than ±2%
- Current limit constant with temperature
- Internal thermal shutdown protection
- Operates with input-output voltage differential of 2.8V at full rated load over full temperature range
- Regulation guaranteed with 25W power dissipation
- 3A output current guaranteed
- Only one external component needed
- 100% electrical burn-in

Schematic Diagram



TL/H/7785–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Input Voltage	20V
Input-Output Differential	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM145	−55°C to +150°C
LM345	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (−5V & −5.2V) (Note 1)

Parameter	Conditions	Limits						Units
		LM145			LM345			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage 5.0V 5.2V	T_j = 25°C, I_{OUT} = 5 mA, V_{IN} = −7.5	 −5.1 −5.3	 −5.0 −5.2	 −4.9 −5.1	 −5.2 −5.4	 −5.0 −5.2	 −4.8 −5.0	 V V
Line Regulation (Note 2)	T_j = 25°C −20V ≤ V_{IN} ≤ −7.5V		5	15		5	25	mV
Load Regulation (Note 2)	T_j = 25°C, V_{IN} = −7.5V 5 mA ≤ I_{OUT} ≤ 3A		30	75		30	100	mV
Output Voltage 5.0V 5.2V	−20V ≤ V_{IN} ≤ −7.8V 5 mA ≤ I_{OUT} ≤ 3A P ≤ 25W T_{MIN} ≤ T_j ≤ T_{MAX}	 −5.20 −5.40		 −4.80 −5.00	 −5.25 −5.45		 −4.75 −4.95	 V V
Quiescent Current	−20V ≤ V_{IN} ≤ −7.5V 5 mA ≤ I_{OUT} ≤ 3A		1.0	3.0		1.0	3.0	mA
Short Circuit Current	V_{IN} = −7.5V, T_j = +25°C V_{IN} = −20V, T_j = +25°C		4 2	5.5 3.5		4 2	5.5 3.5	A A
Output Noise Voltage	T_A = 25°C, C_L = 4.7 μF 10 Hz ≤ f ≤ 100 kHz		150			150		μV
Long Term Stability			5	50		5	50	mV
Thermal Resistance Junction to Case			2			2		°C/W

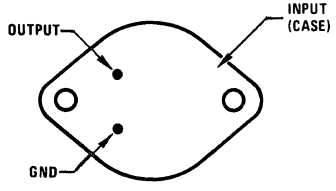
Note 1: Unless otherwise specified, these specifications apply: −55°C ≤ T_j ≤ +150°C for the LM145 and 0°C ≤ T_j ≤ +125°C for the LM345. V_{IN} = 7.5V and I_{OUT} = 5 mA. Although power dissipation is internally limited, electrical specifications apply only for power levels up to 25W. For calculations of junction temperature rise due to power dissipation, use a thermal resistance of 35°C/W for the TO-3 with no heat sink. With a heat sink, use 2°C/W for junction to case thermal resistance.

Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

Note 3: Refer to RETS145K-5.2V for LM145K-5.2V or RETS145K-5V for LM145K-5.0 military specifications.

Connection Diagram

Metal Can Package

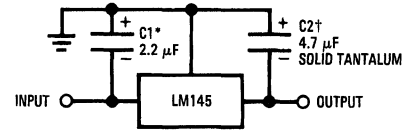


TL/H/7785–2

Bottom View
Order Number LM145K-5.0, LM345K-5.0, LM145K-5.2, or LM345K-5.2
See NS Package Number K02A

Typical Applications

Fixed Regulator



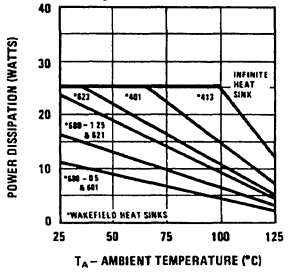
TL/H/7785–3

†Required for stability. For value given, capacitor must be solid tantalum. 50 μF aluminum electrolytic may be substituted. Values given may be increased without limit.

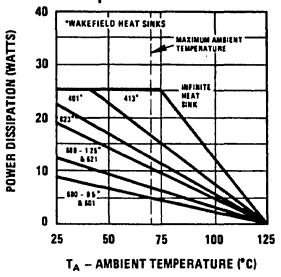
*Required if regulator is separated from filter capacitor. For value given, capacitor must be solid tantulum. 50 μF aluminum electrolytic may be substituted.

Typical Performance Characteristics

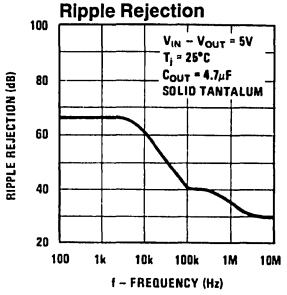
Maximum Average Power Dissipation for LM145



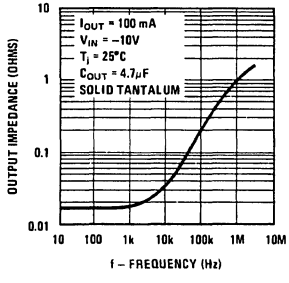
Maximum Average Power Dissipation for LM345



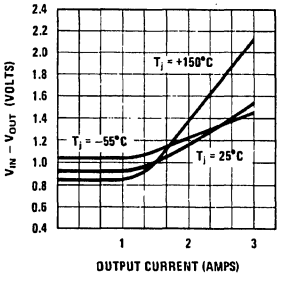
Ripple Rejection



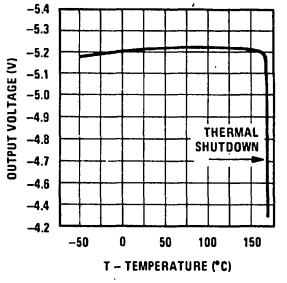
Output Impedance



Minimum Input-Output Voltage Differential

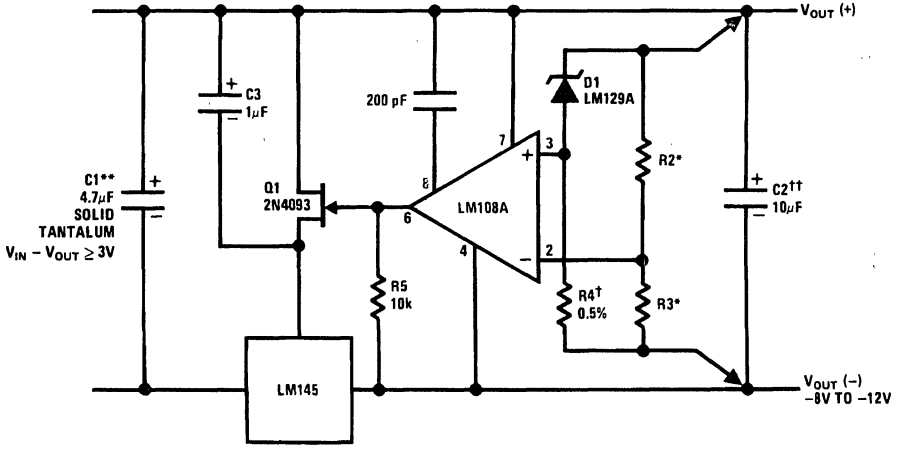


Output Voltage vs Temperature



TL/H/7785–4

Typical Applications (Continued)



TL/H/7785–5

*Select resistors to set output voltage. 1 ppm/C tracking suggested.

**C1 is not needed if power supply filter capacitor is within 3″ of regulator.

†Determines zener current. May be adjusted to minimize temperature drift.

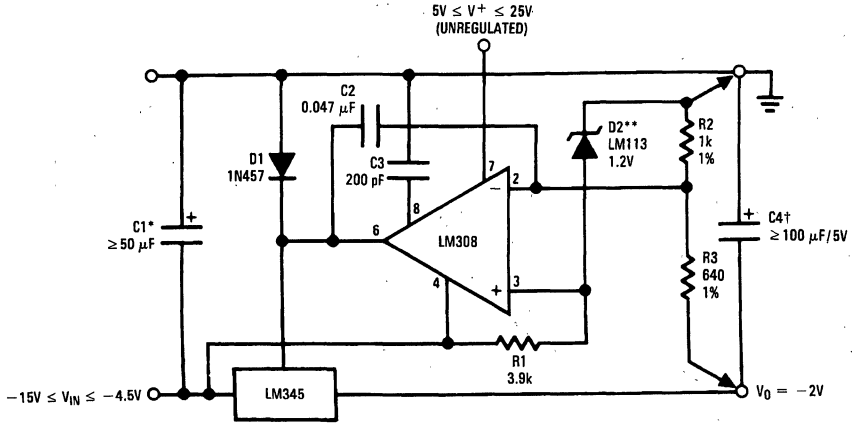
††Solid tantalum.

Load and line regulation < 0.01%

Temperature drift < 0.001%/C

Typical Applications (Continued)

High Stability Regulator



TL/H/7785–6

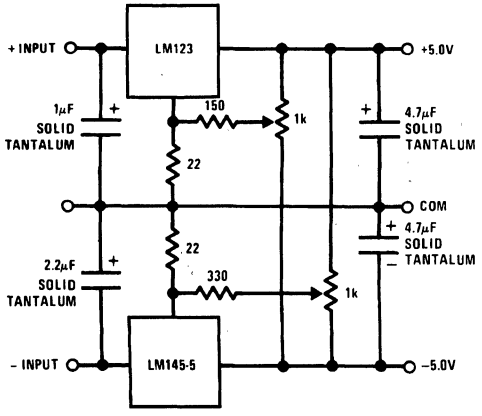
**C1 is not needed if power supply filter capacitor is within 3" of regulator.

†Keep C4 within 2" of LM345.

**D2 sets initial output voltage accuracy. The LM113 is available in −5, −2, and −1% tolerance.

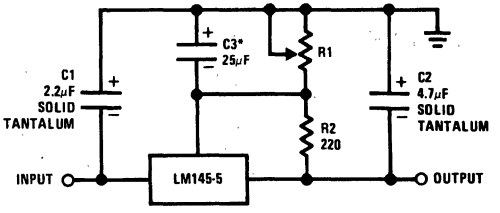
−2V ECL Termination Regulator

Dual 3 Amp Trimmed Supply



TL/H/7785–7

Variable Output (−5.0V to −15V)



TL/H/7785–8

*Optional. Improves transient response and ripple rejection.

$$V_{OUT} = -5V\left(\frac{R1 + R2}{R2}\right)$$

National Semiconductor

LM150A/LM150, LM350A/LM350 3-Amp Adjustable Regulators

General Description

The LM150 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

By connecting a fixed resistor between the adjustment pin and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The part numbers in the LM150 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM150A/LM150 are rated for $-55°C \leq T_J \leq +150°C$, while the LM350A is rated for $-40°C \leq T_J \leq +125°C$, and the LM350 is rated for $0°C \leq T_J \leq +125°C$.

Features

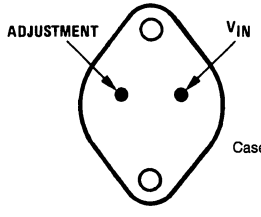
- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Guaranteed thermal regulation
- Output is short circuit protected
- Current limit constant with temperature
- 100% electrical burn-in in thermal limit
- 86 dB ripple rejection
- Guaranteed 1% output voltage tolerance (LM150A, LM350A)
- Guaranteed max. 0.01%/V line regulation (LM150A, LM350A)
- Guaranteed max. 0.3% load regulation (LM150A, LM350A)

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

Connection Diagrams

(TO-3 STEEL)
Metal Can Package

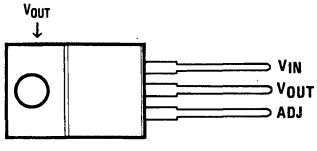


TL/H/9061-4

Bottom View

Order Number LM150AK STEEL, LM150K STEEL, LM350AK STEEL or LM350K STEEL
See NS Package Number K02A

(TO-220)
Plastic Package



TL/H/9061-5

Front View

Order Number LM350AT or LM350T
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+35V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Tolerance	TBD
Operating Temperature Range	
LM150A/LM150	$-55°C \le T_J \le +150°C$
LM350A	$-40°C \le T_J \le +125°C$
LM350	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics

Specifications with standard type face are for $T_J = 25°C$, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT} = 5V$, and $I_{OUT} = 10$ mA. (Note 2)

Parameter	Conditions	LM150A			LM150			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	$I_{OUT} = 10$ mA, $T_J = 25°C$	1.238	1.250	1.262				V
	$3V \le (V_{IN} - V_{OUT}) \le 35V$, $10 mA \le I_{OUT} \le 3A$, $P \le 30W$	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 35V$ (Note 3)		0.005	0.01		0.005	0.01	%/V
			0.02	**0.05**		**0.02**	**0.05**	%/V
Load Regulation	$10 mA \le I_{OUT} \le 3A$ (Note 3)		0.1	0.3		0.1	0.3	%
			0.3	**1**		**0.3**	**1**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.01	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le 3A$, $3V \le (V_{IN} - V_{OUT}) \le 35V$		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		**3.5**	**5**		**3.5**	**5**	mA
Current Limit	$V_{IN} - V_{OUT} \le 10V$	**3.0**	**4.5**		**3.0**	**4.5**		A
	$V_{IN} - V_{OUT} = 30V$	0.3	1		0.3	1		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.001		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 0$ μF		**65**			**65**		dB
	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 10$ μF	**66**	**86**		**66**	**86**		dB
Long-Term Stability	$T_J = 125°C$, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package		1.2	1.5		1.2	1.5	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W

Electrical Characteristics (Continued)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range.** Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA. (Note 2) (Continued)

Parameter	Conditions	LM350A			LM350			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA, T_J = 25°C	1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V, 10 mA ≤ I_{OUT} ≤ 3A, P ≤ 30W	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V (Note 3)		0.005	0.01		0.005	0.03	%/V
			0.02	**0.05**		**0.02**	**0.07**	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ 3A (Note 3)		0.1	0.3		0.1	0.5	%
			0.3	**1**		**0.3**	**1.5**	%
Thermal Regulation	20 ms Pulse		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			**50**	**100**		**50**	**100**	μA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ 3A, 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V		**0.2**	**5**		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**			**1**		%
Minimum Load Current	$V_{IN} - V_{OUT}$ = 35V		**3.5**	**10**		**3.5**	**10**	mA
Current Limit	$V_{IN} - V_{OUT}$ ≤ 10V	**3.0**	**4.5**		**3.0**	**4.5**		A
	$V_{IN} - V_{OUT}$ = 30V	0.3	1		0.25	1		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.001			0.001		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**			**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**86**		**66**	**86**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.25	1		0.25	1	%
Thermal Resistance, Junction to Case	K Package		1.2	1.5		1.2	1.5	°C/W
	T Package		3	4		3	4	°C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	K Package		35			35		°C/W
	T Package		50			50		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

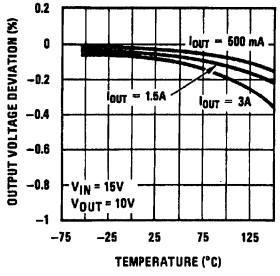
Note 2: These specifications are applicable for power dissipations up to 30W for the TO-3 (K) package and 25W for the TO-220 (T) package. Power dissipation is guaranteed at these values up to 15V input-output differential. Above 15V differential, power dissipation will be limited by internal protection circuitry. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 3: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

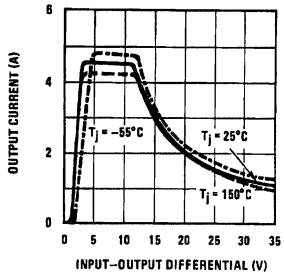
Note 4: Refer to RETS150K drawing for military specifications of the LM150K.

Typical Performance Characteristics

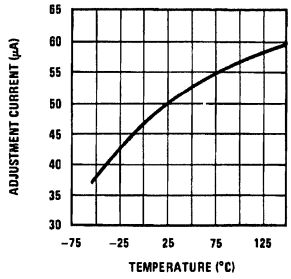
Load Regulation



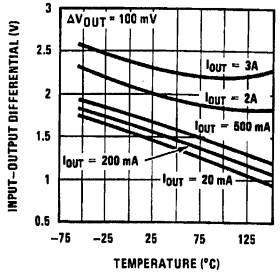
Current Limit



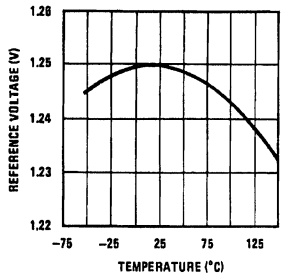
Adjustment Current



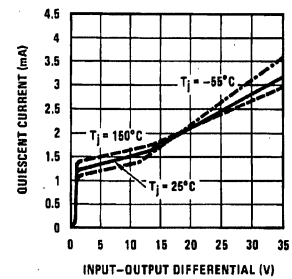
Dropout Voltage



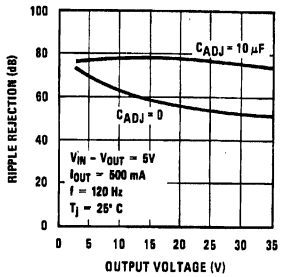
Temperature Stability



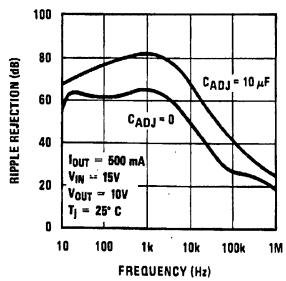
Minimum Operating Current



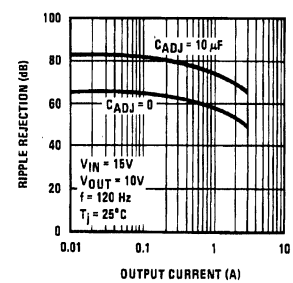
Ripple Rejection



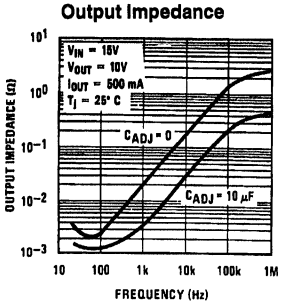
Ripple Rejection



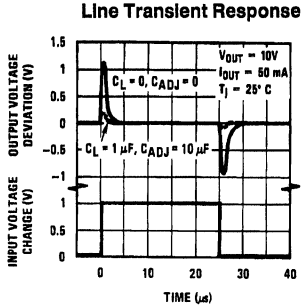
Ripple Rejection



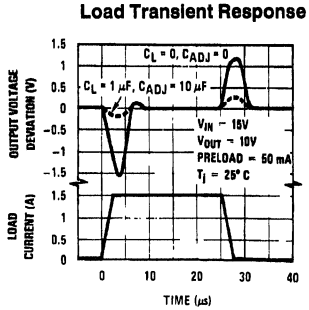
Output Impedance



Line Transient Response



Load Transient Response



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Application Hints

In operation, the LM150 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2.$$

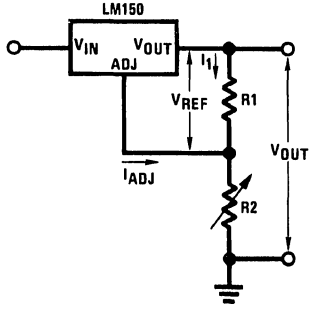

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FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

EXTERNAL CAPACITORS

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 86 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

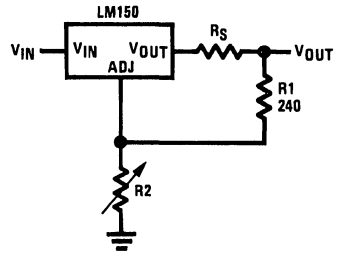
In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

LOAD REGULATION

The LM150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω × I_{OUT}. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.



TL/H/9061–8

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

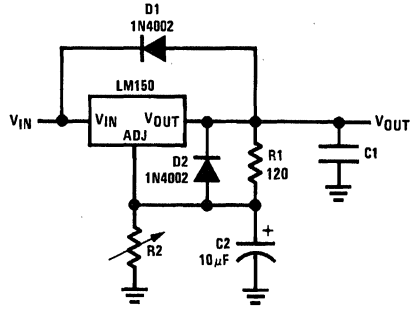
PROTECTION DIODES

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

Application Hints (Continued)



D1 protects against C1
D2 protects against C2

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

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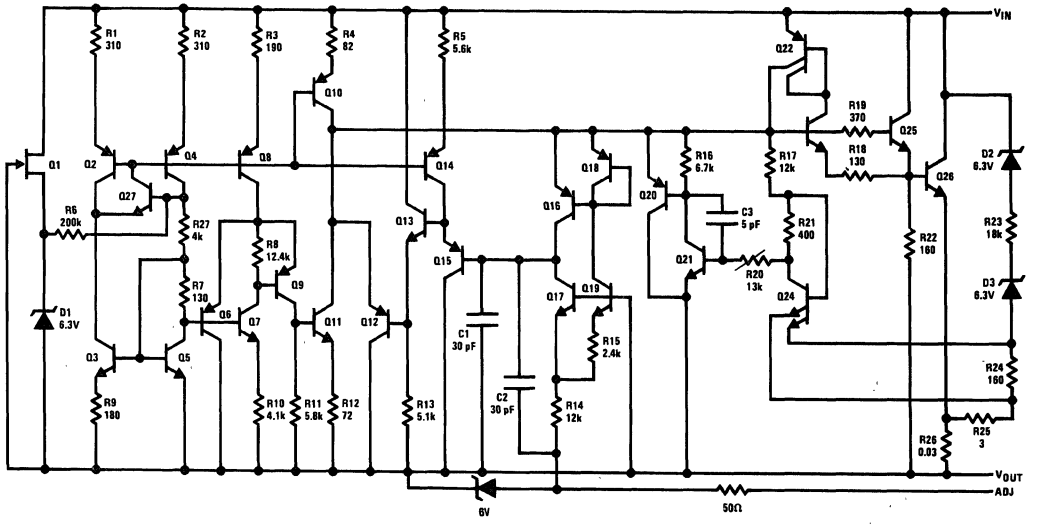
FIGURE 3. Regulator with Protection Diodes

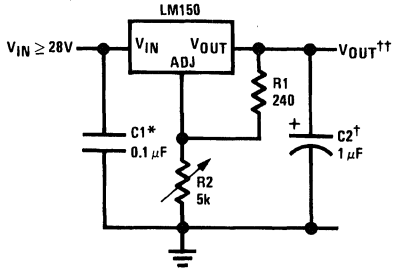
Schematic Diagram



TL/H/9061–10

Typical Applications

1.2V—25V Adjustable Regulator



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Full output current not available at high input-output voltages.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

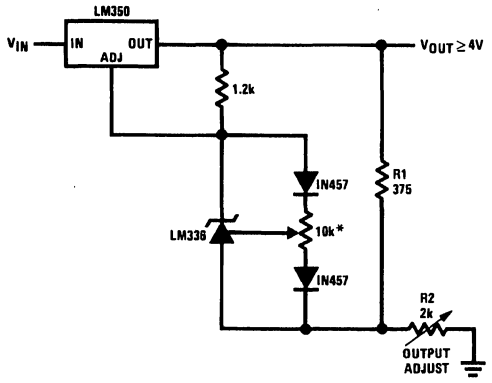
*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,(R2)$$

Note: Usually R1 = 240Ω for LM150 and R1 = 120Ω for LM350.

Typical Applications (Continued)

Precision Power Regulator with Low Temperature Coefficient



*Adjust for 3.75V across R1

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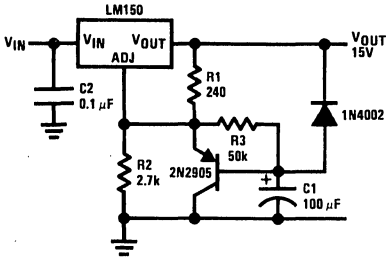
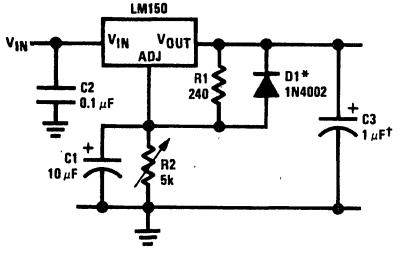
Slow Turn-ON 15V Regulator



TL/H/9061–14

Adjustable Regulator with Improved Ripple Rejection

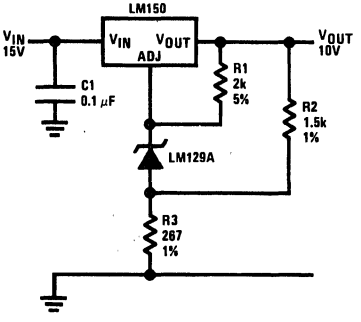


†Solid tantalum

*Discharges C1 if output is shorted to ground

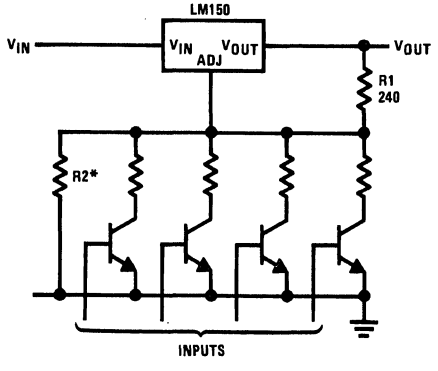
TL/H/9061–15

High Stability 10V Regulator



TL/H/9061–16

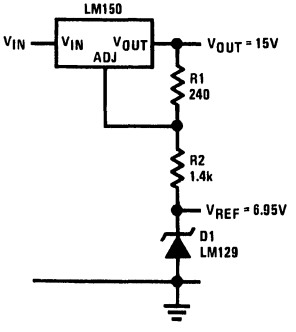
Digitally Selected Outputs



TL/H/9061–17

*Sets maximum V_{OUT}

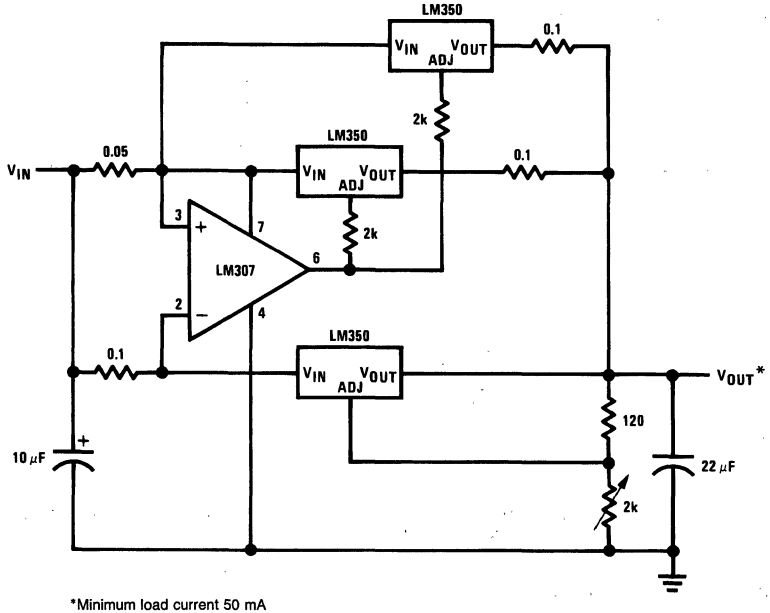
Regulator and Voltage Reference



TL/H/9061–3

Typical Applications (Continued)

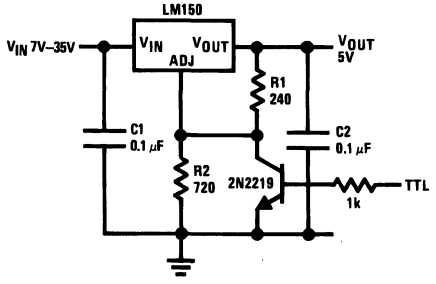
10A Regulator



*Minimum load current 50 mA

TL/H/9061–18

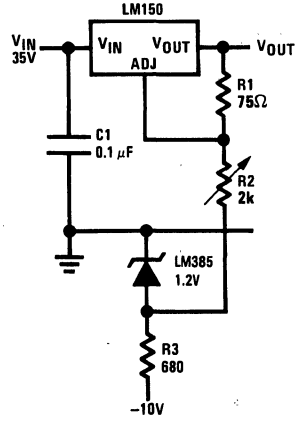
5V Logic Regulator with Electronic Shutdown*



TL/H/9061–19

*Min output ≈ 1.2V

0 to 30V Regulator

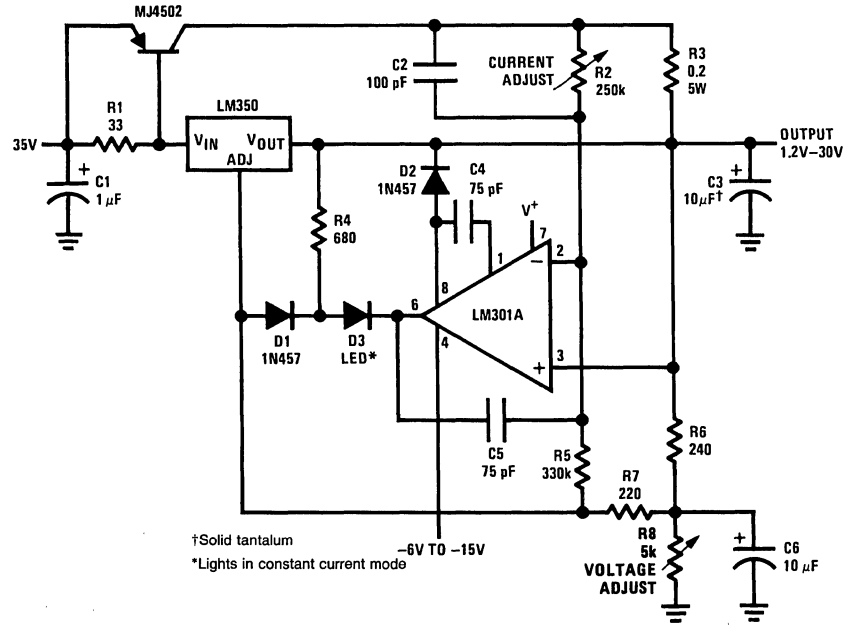


TL/H/9061–20

Full output current not available at high input-output voltages

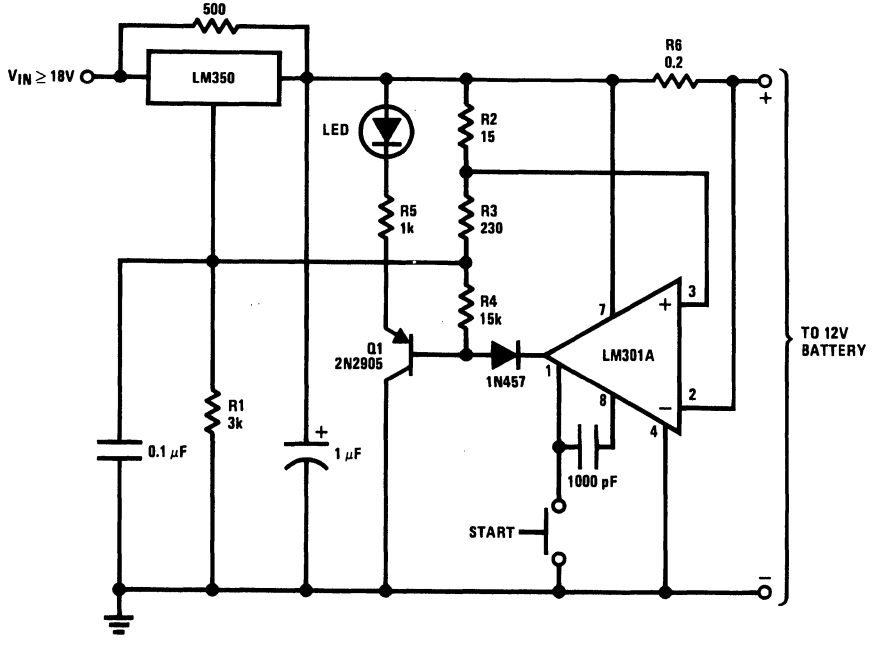
Typical Applications (Continued)

5A Constant Voltage/Constant Current Regulator



TL/H/9061–21

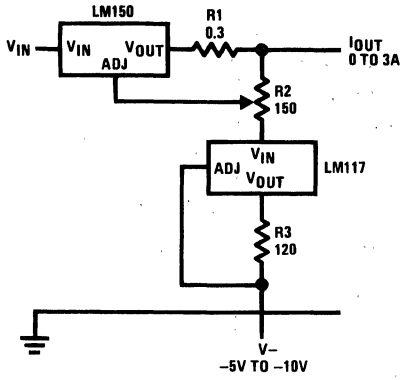
12V Battery Charger



TL/H/9061–22

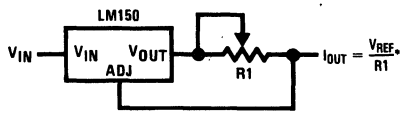
Typical Applications (Continued)

Adjustable Current Regulator



TL/H/9061–23

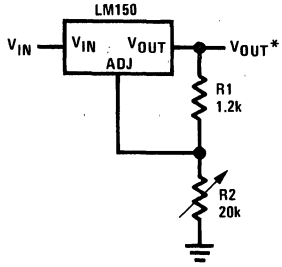
Precision Current Limiter



TL/H/9061–24

*0.4 ≤ R_1 ≤ 120Ω

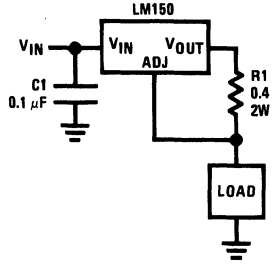
1.2V–20V Regulator with Minimum Program Current



TL/H/9061–25

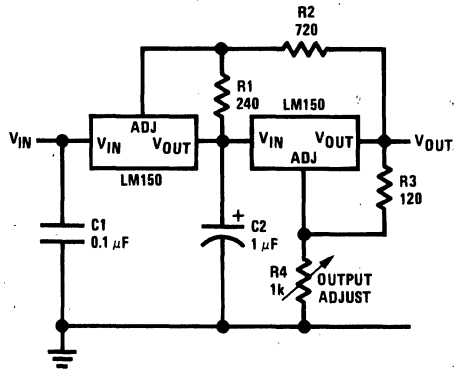
*Minimum output current ≈ 4 mA

3A Current Regulator



TL/H/9061–26

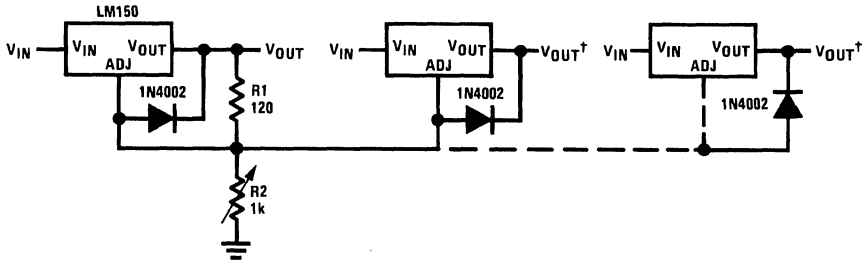
Tracking Preregulator



TL/H/9061–27

Typical Applications (Continued)

Adjusting Multiple On-Card Regulators with Single Control*

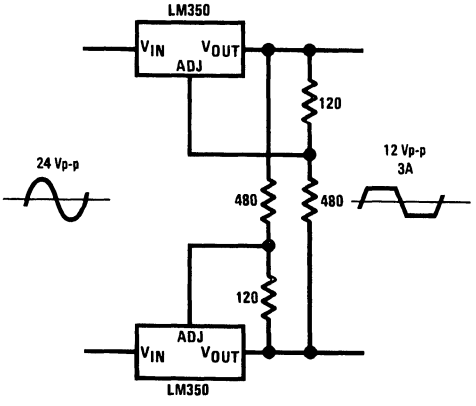


TL/H/9061–28

†Minimum load—10 mA

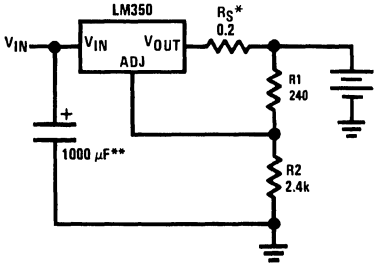
*All outputs within ±100 mV

AC Voltage Regulator



TL/H/9061–29

Simple 12V Battery Charger



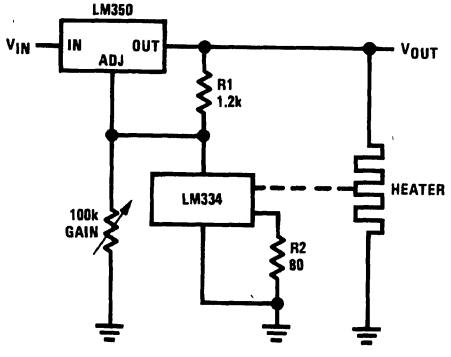
TL/H/9061–30

*R_S—sets output impedance of charger: $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$

Use of R_S allows low charging rates with fully charged battery.

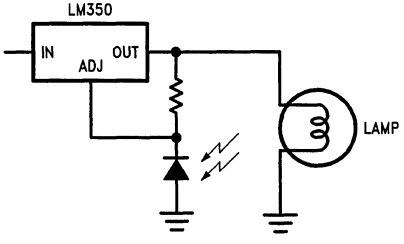
**1000 μF is recommended to filter out any input transients

Temperature Controller



TL/H/9061–11

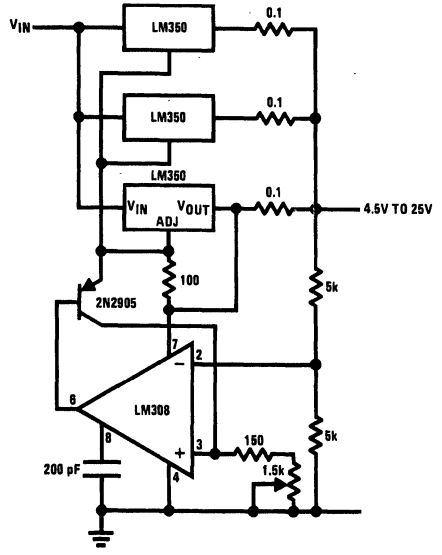
Light Controller



TL/H/9061–12

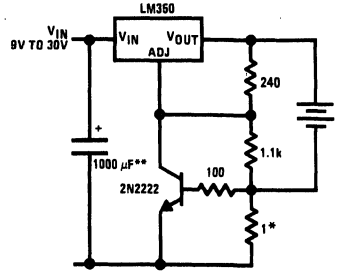
Typical Applications (Continued)

Adjustable 10A Regulator



TL/H/9061–31

Current Limited 6V Charger

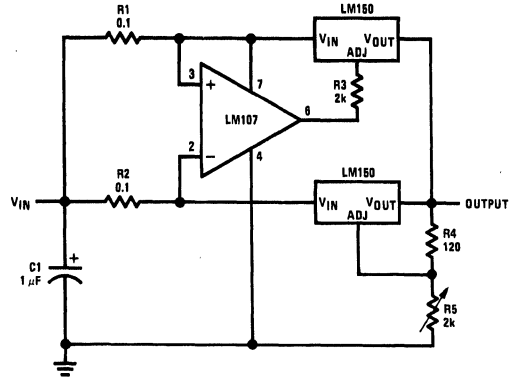


TL/H/9061–32

*Sets peak current (2A for 0.3Ω)

**1000 μF is recommended to filter out any input transients.

6A Regulator



TL/H/9061–2

National Semiconductor

LM196/LM396 10 Amp Adjustable Voltage Regulator

General Description

The LM196 is a 10 amp regulator, adjustable from 1.25V to 15V, which uses a revolutionary new IC fabrication structure to combine high power discrete transistor technology with modern monolithic linear IC processing. This combination yields a high-performance single-chip regulator capable of supplying in excess of 10 amps and operating at power levels up to 70 watts. The regulators feature on-chip trimming of reference voltage to ±0.8% and simultaneous trimming of reference temperature drift to 30 ppm/°C typical. Thermal interaction between control circuitry and the pass transistor which affects the output voltage has been reduced to extremely low levels by strict attention to isothermal layout. This interaction, called thermal regulation, is 100% tested.

These new regulators have all the protection features of popular lower power adjustable regulators such as LM117 and LM138, including current limiting and thermal limiting. The combination of these features makes the LM196 immune to blowout from output overloads or shorts, even if the adjustment pin is accidentally disconnected. All devices are "burned-in" in thermal shutdown to guarantee proper operation of these protective features under actual overload conditions.

Output voltage is continuously adjustable from 1.25V to 15V. Higher output voltages are possible if the maximum input-output voltage differential specification is not exceeded. Full load current of 10A is available at all output voltages, subject only to the maximum power limit of 70W and of course, maximum junction temperature.

The LM196 is exceptionally easy to use. Only two external resistors are used to to set output voltage. On-chip adjustment of the reference voltage allows a much tighter specification of output voltage, eliminating any need for trimming in most cases. The regulator will tolerate an extremely wide range of reactive loads, and does not depend on external capacitors for frequency stabilization. Heat sink requirements are much less stringent, because overload situations do not have to be accounted for—only worst-case full load conditions.

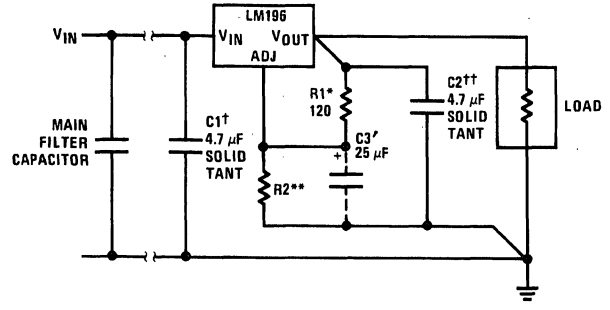
The LM196 is in a TO-3 package with oversized (0.060") leads to provide best possible load regulation. Operating junction temperature range is −55°C to +150°C. The LM396 is specified for a 0°C to +125°C junction temperature range.

Features

- Output pre-trimmed to ±0.8%
- 10A guaranteed output current
- 100% burn-in in thermal limit
- 70W maximum power dissipation
- Adjustable output—1.25V to 15V
- Internal current and power limiting
- Guaranteed thermal resistance
- Output voltage guaranteed under worst-case conditions
- Output is short circuit protected

Typical Applications

$$V_{OUT} = (1.25V)\left(\frac{R1 + R2}{R1}\right) + I_{ADJ}(R2)$$



TL/H/9059–1

FIGURE 1. Basic 1.25V to 15V Regulator

*For best TC of V_{OUT}, R1 should be wirewound or metal film, 1% or better.

**R2 should be same type as R1, with TC tracking of 30 ppm/°C or better.

†C1 is necessary only if main filter capacitor is more than 6" away, assuming #18 or larger leads.

††C2 is not absolutely necessary, but is suggested to lower high frequency output impedance. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

'C3 improves ripple rejection, output impedance, and noise. C2 should be 1 μF or larger close to the regulator if C3 is used.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	20V
Operating Junction Temperature Range	
LM196 Control Section	−55°C to +150°C
Power Transistor	−55°C to +200°C
LM396 Control Section	0°C to +125°C
Power Transistor	0°C to +175°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating to be determined	

Pre-Conditioning

100% Burn-In in Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM196			LM396			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage	I_{OUT} = 10 mA	1.24	1.25	1.26	1.23	1.25	1.27	V
Reference Voltage (Note 2)	$V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$ 10 mA $\le I_{OUT}$ 10A, $P \le P_{MAX}$ Full Temperature Range	1.22	1.25	1.28	1.21	1.25	1.29	V
Line Regulation (Note 3)	$V_{MIN} \le (V_{IN} - V_{OUT}) \le 20V$ Full Temperature Range		0.005	0.01 0.05		0.005	0.02 0.05	%/V %/V
Load Regulation LM196/LM396 (Note 4)	10 mA $\le I_{OUT} \le$ 10A $V_{MIN} \le V_{IN} - V_{OUT} \le 10V$, $P \le P_{MAX}$ Full Temperature Range			0.1 0.15			0.1 0.15	%/V %/A
Ripple Rejection (Note 5)	C_{ADJ} = 25 µF, f = 120 Hz Full Temperature Range	60 54	74		66 54	74		dB dB
Thermal Regulation (Note 6)	$V_{IN} - V_{OUT}$ = 5V, I_{OUT} = 10A		0.003	0.005		0.003	0.015	%/W
Average Output Voltage Temperature Coefficient	$T_{jMIN} \le T_j \le T_{jMAX}$ (See Curves for Limits)		0.003			0.003		%/°C
Adjustment Pin Current			50	100		50	100	µA
Adjustment Pin Current Change (Note 7)	10 mA $\le I_{OUT} \le$ 10A 3V $\le V_{IN} - V_{OUT} \le$ 20V $P \le P_{MAX}$, Full Temperature Range			3			3	µA
Minimum Load Current (Note 9)	2.5V $\le (V_{IN} - V_{OUT}) \le$ 20V Full Temperature Range			10			10	mA
Current Limit (Note 8)	2.5 $\le (V_{IN} - V_{OUT} \le$ 7V $V_{IN} - V_{OUT}$ = 20V	10 1.5	14 3	20 8	10 1.5	14 3	20 8	A A
Rms Output Noise	10 Hz $\le$ f $\le$ 10 kHz		0.001			0.001		$\%V_{OUT}$
Long Term Stability	T_j = 125°C, t = 1000 Hours		0.3	1.0		0.3	1.0	%
Thermal Resistance Junction to Case (Note 10)	Control Circuitry Power Transistor		0.3 1.0	0.5 1.2		0.3 1.0	0.5 1.2	°C/W °C/W

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions	LM196			LM396			Units
		Min	Typ	Max	Min	Typ	Max	
Power Dissipation (P_{MAX}) (Note 11)	$7.0V \le V_{IN} - V_{OUT} \le 12V$	70	100		70	100		W
	$V_{IN} - V_{OUT} = 15V$	50			50			W
	$V_{IN} - V_{OUT} = 18V$	36			36			W
Drop-Out Voltage LM196/LM396	I_{OUT} = 10A, Full Temperature Range		2.1	2.5 2.75		2.1	2.5 2.75	V

Note 1: Unless otherwise stated, these specifications apply for T_j = 25°C, $V_{IN} - V_{OUT}$ = 5V, I_{OUT} = 10 mA to 10A.

Note 2: This is a worst-case specification which includes all effects due to input voltage, output current, temperature, and power dissipation. Maximum power (P_{MAX}) is specified under Electrical Characteristics.

Note 3: Line regulation is measured on a short-pulse, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Line Regulation under Application Hints.

Note 4: Load regulation on the 2-pin package is determined primarily by the voltage drop along the output pin. Specifications apply for an external Kelvin sense connnection at a point on the output pin ¼" from the bottom of the package. Testing is done on a short-pulse-width, low-duty-cycle basis to maintain constant junction temperature. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately. See discussion of Load Regulation under Application Hints.

Note 5: Ripple rejection is measured with the adjustment pin bypassed with 25 μF capacitor, and is therefore independent of output voltage. With no load or bypass capacitor, ripple rejection is determined by line regulation and may be calculated from; RR = 20 $\log_{10}$ [100/(K × V_{OUT})] where K is line regulation expressed in %/V. At frequencies below 100 Hz, ripple rejection may be limited by thermal effects, if load current is above 1A.

Note 6: Thermal regulation is defined as the change in output voltage during the time period of 0.2 ms to 20 ms after a change in power dissipation in the regulator, due to either a change in input voltage or output current. See graphs and discussion of thermal effects under Application Hints.

Note 7: Adjustment pin current change is specified for the worst-case combination of input voltage, output current, and power dissipation. Changes due to temperature must be taken into account separately. See graph of adjustment pin current vs temperature.

Note 8: Current limit is measured 10 ms after a short is applied to the output. DC measurements may differ slightly due to the rapidly changing junction temperature, tending to drop slightly as temperature increases. A minimum available load current of 10A is guaranteed over the full temperature range as long as power dissipation does not exceed 70W, and $V_{IN} - V_{OUT}$ is less than 7.0V.

Note 9: Minimum load current of 10 mA is normally satisfied by the resistor divider which sets up output voltage.

Note 10: Total thermal resistance, junction-to-ambient, will include junction-to-case thermal resistance plus interface resistance and heat sink resistance. See discussion of Heat Sinking under Application Hints.

Note 11: Although power dissipation is internally limited, electrical specifications apply only for power dissipation up to the limits shown. Derating with temperature is a function of both power transistor temperature and control area temperature, which are specified differently. See discussion of Heat Sinking under Application Hints. For $V_{IN} - V_{OUT}$ less than 7V, power dissipation is limited by current limit of 10A.

Note 12: Dropout voltage is input-output voltage differential measured at a forced reference voltage of 1.15V, with a 10A load, and is a measurement of the minimum input/output differential at full load.

Application Hints

Further improvements in efficiency can be obtained by using Schottky diodes or high efficiency diodes with lower forward voltage, combined with larger filter capacitors to reduce ripple. However, this reduces the voltage difference between input and drive pins and may not allow sufficient voltage to fully saturate the pass transistor. Special transformers are available from Signal Transformer that have a 1V tap on the output winding to provide the extra voltage for the drive pin. The transformers are available as standard items for 5V applications at 5A, 10A and 20A. Other voltages are available on special request.

Heat Sinking

Because of its extremely high power dissipation capability, the *major limitation* in the load driving capability of the LM196 is *heat sinking*. Previous regulators such as LM109, LM340, LM117, etc., had internal power limiting circuitry which limited power dissipation to about 30W. The LM196 is guaranteed to dissipate up to 70W continuously, as long as the maximum junction temperature limit is not exceeded. This requires careful attention to all sources of thermal resistance from junction-to-ambient, including junction-to-case resistance, case-to-heat sink interface resistance (0.1–1.0°C/W), and heat sink resistance itself. A good thermal joint compound such as Wakefield type 120 or Thermalloy Thermocote must be used when mounting the LM196, especially if an electrical insulator is used to isolate the regulator from the heat sink. Interface resistance without this compound will be no better than 0.5°C/W, and probably much worse. With the compound, and no insulator, interface resistance will be 0.2°C/W or less, assuming 0.005" or less combined flatness run-out of TO-3 and heat sink. Proper torquing of the mounting bolts is important to achieve minimum thermal resistance. Four to six inch pounds is recommended. Keep in mind that good electrical, as well as thermal, contact must be made to the case.

Application Hints (Continued)

The actual heat sink chosen for the LM196 will be determined by the worst-case continuous full load current, input voltage and maximum ambient temperature. Overload or short circuit output conditions do not normally have to be considered when selecting a heat sink because the thermal shutdown built into the LM196 will protect it under these conditions. An exception to this is in situations where the regulator must recover very quickly from overload. The LM196 may take some time to recover to within specified output tolerance following an extended overload, if the regulator is cooling from thermal shutdown temperature (approximately 175°) to specified operating temperature (125°C or 150°C). The procedure for heat sink selection is as follows:

Calculate worst-case *continuous* average power dissipation in the regulator from $P = (V_{IN} - V_{OUT}) \times (I_{OUT})$. To do this, you must know the raw power supply voltage/current characteristics fairly accurately. For example, consider a 10V output with 15V nominal input voltage. At full load of 10A, the regulator will dissipate $P = (15 - 10) \times (10) = 50W$. If input voltage rises by 10%, power dissipation will increase to $(16.5 - 10) \times (10) = 65W$, a *30% increase.* It is strongly suggested that a raw supply be assembled and tested to determine its average DC output voltage *under full load with maximum line voltage.* Do not over-design by using unloaded voltage as a worst-case, since the regulator will not be dissipating any power under no load conditions. Worst-case regulator dissipation normally occurs under full load conditions except when the effective DC resistance of the raw supply ($\Delta V/\Delta I$) is larger than $(V_{IN}^* - V_{OUT})/2I_{fL}$, where V_{IN}^* is the lightly-loaded raw supply voltage and I_{fL} is full load current. For $(V_{IN}^* - V_{OUT}) = 5V - 8V$, and $I_{fL} = 5A-10A$, this gives a resistance of 0.25Ω to 0.8Ω. If raw supply resistance is higher than this, the regulator power dissipation may be *less* at full load current, then at some intermediate current, due to the large drop in input voltage. Fortunately, most well designed raw supplies have low enough output resistance that regulator dissipation does maximize at full load current, or very close to it, so tedious testing is not usually required to find worst-case power dissipation.

A very important consideration is the size of the filter capacitor in the raw supply. At these high current levels, capacitor size is usually dictated by ripple current ratings rather than just obtaining a certain ripple voltage. Capacitor ripple current (rms) is 2–3 times the DC output current of the filter. If the capacitor has just 0.05Ω DC resistance, this can cause 30W internal power dissipation at 10A output current. Capacitor life is very sensitive to operating temperature, decreasing by a factor of two for each 15°C rise in internal temperature. Since capacitor life is not all that great to start with, it is obvious that a small capacitor with a large internal temperature rise is inviting very short mean-time-to-failure. A second consideration is the loss of usable input voltage to the regulator. If the capacitor is small, the large dips in the input voltage may cause the LM196 to drop out of regulation. 2000 μF per ampere of load current is the *minimum* recommended value, yielding about 2 Vp-p ripple of 120 Hz. Larger values will have longer life and the reduced ripple will allow lower DC input voltage to the regulator, with subsequent cost savings in the transformer and heat sink. Sometimes several capacitors in parallel are better to decrease series resistance and increase heat dissipating area.

After the raw supply characteristics have been determined, and worst-case power dissipation in the LM196 is known, the heat sink thermal resistance can be found from the graphs titled Maximum Heat Sink Thermal Resistance. These curves indicate the minimim size heat sink required as a function of ambient temperature. They are derived from a case-to-control area thermal resistance of 0.5°C/W and a case-to-power transistor thermal resistance of 1.2°C/W. 0.2°C/W is assumed for interface resistance. A maximum control area temperature of 150°C is used for the LM196 and 125°C for the LM396. Maximum power transistor temperature is 200°C for the LM196 and 175°C for the LM396. For conservative designs, it is suggested that when using these curves, you assume an ambient temperature 25°C–50°C higher than is actually anticipated, to avoid running the regulator right at its design limits of operating temperature.

A quick look at the curves show that heat sink resistance (θ_{SA}) will normally fall into the range of 0.2°C/W–1.5°C/W. These are *not* small heat sinks. A model 441, for instance, which is sold by several manufacturers, has a θ_{SA} of 0.6°C/W with natural convection and is about five inches on a side. Smaller sinks are more volumetrically efficient, and larger sinks, less so. A rough formula for estimating the volume of heat sink required is: $V = 50/\theta_{SA}^{1.5}$ CU. IN. This holds for natural convection only. If the heat sink is inside a small sealed enclosure, θ_{SA} will increase substantially because the air is not free to form natural convection currents. Fan-forced convection can reduce θ_{SA} by a factor of two at 200 FPM air velocity, and by four at 1000 FPM.

Ripple Rejection

Ripple rejection at the normal ripple frequency of 120 Hz is a function of both electrical and thermal effects in the LM196. If the adjustment pin is not bypassed with a capacitor, it is also dependent on output voltage. A 25 μF capacitor from the adjustment pin to ground will make ripple rejection independent of output voltage for frequencies above 100 Hz. If lower ripple frequencies are encountered, the capacitor should be increased proportionally.

To keep in mind that the bypass capacitor on the adjustment pin will limit the turn-on time of the regulator. A 25 μF capacitor, combined with the output divider resistance, will give an extended output voltage settling time following the application of input power.

Load Regulation (LM196/LM396)

Because the LM196 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the output pin and the wire connecting the regulator to the load. For the data sheet specification, regulation is measured 1/4″ from the bottom of the package on the output pin. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load.

Application Hints (Continued)

Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the output pin, *not to the load*. This is illustrated in *Figure 2*. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$(Rw) \times \left(\frac{R2 + R1}{R1}\right)$$

Rw = Line Resistance

Connected as shown, Rw is not multiplied by the divider ratio. Rw is about 0.004Ω per foot using 16 gauge wire. This translates to 40 mV/ft at 10A load current, so it is important to keep the positive lead between regulator and load as short as possible.

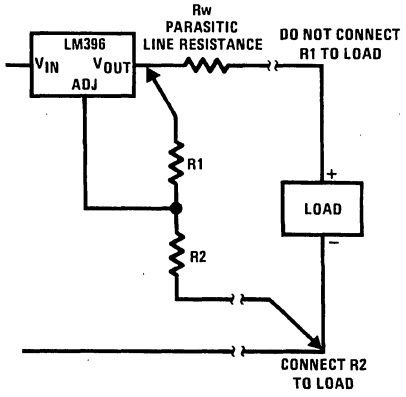


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FIGURE 2. Proper Divider Connection

The input resistance of the sense pin is typically 6 kΩ, modeled as a resistor between the sense pin and the output pin. Load regulation will start to degrade if a resistance higher than 10Ω is inserted in series with the sense. This assumes a worst-case condition of 0.5V between output and sense pins. Lower differential voltage will allow higher sense series resistance.

Thermal Load Regulation

Thermal, as well as electrical, load regulation must be considered with IC regulators. Electrical load regulation occurs in microseconds, thermal regulation due to die thermal gradients occurs in the 0.2 ms-20 ms time frame, and regulation due to overall temperature changes in the die occurs over a 20 ms to 20 minute period, depending on the time constant of the heat sink used. Gradient induced load regulation is calculated from

$$\Delta V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (\beta)$$

β = Thermal regulation specified on data sheet.

For V_{IN} = 9V, V_{OUT} = 5V, ΔI_{OUT} = 10A, and β = 0.005%/W, this yields a 0.2% change in output voltage. Changes in output voltage due to overall temperature rise are calculated from

$$V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (TC) \times (\theta_{jA})$$

TC = Temperature coefficient of output voltage.

θ_{jA} = Thermal resistance from junction to ambient. θ_{jA} is approximately 0.5°C/W + θ of heat sink.

For the same conditions as before, with TC = 0.003%/°C, and θ_{jA} = 1.5°C/W, the change in output voltage will be 0.18%. Because these two thermal terms can have either polarity, they may subtract from, or add to, electrical load regulation. For worst-case analysis, they must be assumed to add. If the output of the regulator is trimmed under load, only that portion of the load that changes need be used in the previous calculations, significantly improving output accuracy.

Line Regulation

Electrical line regulation is very good on the LM196—typically less than 0.005% change in output voltage for a 1V change in input. This level of regulation is achieved only for very low load currents, however, because of thermal effects. Even with a thermal regulation of 0.002%.W, and a temperature coefficient of 0.003%/°C, DC line regulation will be dominated by thermal effects as shown by the following example:

Assume V_{OUT} = 5V, V_{IN} = 9V, I_{OUT} = 8A

Following a 10% change in input voltage (0.9), the output will change quickly (≤100 μs), due to electrical effects, by (0.005%V) × (0.9V) = 0.0045%. In the next 20 ms, the output will change an additional (0.002%/W) × (8A) × (0.9V) = 0.0144% due to thermal gradients across the die. After a much longer time, determined by the time constant of the heat sink, the output will change an additional (0.003%/°C) × (8A) × (0.9V) × (2°C/W) = 0.043% due to the temperature coefficient of output voltage and the thermal resistance from die to ambient. (2°C/W was chosen for this calculation). The sign of these last two terms varies from part to part, so no assumptions can be made about any cancelling effects. All three terms must be added for a proper analysis. This yields 0.0045 + 0.0144 + 0.043 = 0.062% using *typical* values for thermal regulation and temperature coefficient. For worst-case analysis, the maximum data sheet specifications for thermal regulation and temperature coefficient should be used, along with the *actual* thermal resistance of the heat sink being used.

Paralleling Regulators

Direct paralleling of regulators is not normally recommended because they do not share currents equally. The regulator with the highest reference voltage will supply all the current to the load until it current limits. With an 18A load, for instance, one regulator might be operating in current limit at 16A while the second device is only carrying 2A. Power dissipation in the high current regulator is extremely high with attendant high junction temperatures. Long term reliability cannot be guaranteed under these conditions.

Quasi-paralleling may be accomplished if load regulation is not critical. The connection shown in *Figure 5a* will typically share to within 1A, with a worst-case of about 3A. Load regulation is degraded by 150 mV at 20A loads. An external op amp may be used as in *Figure 5b* to improve load regulation and provide remote sensing.

Application Hints (Continued)

Input and Output Capacitors

The LM196 will tolerate a wide range of input and output capacitance, but long wire runs or small values of output capacitance can sometimes cause problems. If an output capacitor is used, it should be 1 μF or larger. We suggest 10 μF solid tantalum if significant improvements in high frequency output impedance are needed (see output impedance graph). This capacitor should be as close to the regulator as possible, with short leads, to reduce the effects of lead inductance. No input capacitor is needed if the regulator is within 6 inches of the power supply filter capacitor, using 18 gauge stranded wire. For longer wire runs, the LM196 input should be bypassed locally with a 4.7 μF (or larger) solid tantalum capacitor, or a 100 μF (or larger) aluminum electrolytic capacitor.

Correcting for Output Wire Losses (LM196/LM396)

Three-terminal regulators can only provide partial Kelvin load sensing (see Load Regulation). Full remote sensing can be added by using an external op amp to cancel the effect of voltage drops in the unsensed positive output lead. In *Figure 7*, the LM301A op amp forces the voltage loss across the unsensed output lead to appear across R3. The current through R3 then flows out the V^- pin of the op amp through R4. The voltage drop across R4 will raise the output voltage by an amount equal to the line loss, just cancelling the line loss itself. A small (≅ 40 mV) initial output voltage error is created by the quiescent current of the op amp. Cancellation range is limited by the maximum output current of the op amp, about 300 mV as shown. This can be raised by increasing R3 or R4 at the expense of more initial output error.

Transformers and Diodes

Proper transformer ratings are very important in a high current supply because of the conflicting requirements of efficiency and tolerance to low-line conditions. A transformer with a high secondary voltage will waste power and cause unnecessary heating in the regulator. Too low a secondary voltage will cause loss of regulation under low-line conditions. The following formulas may be used to calculate the required secondary voltage and current ratings using a full-wave center tap:

$$V_{rms} = \left(\frac{V_{OUT} + V_{REG} + V_{RECT} + V_{RIPPLE}}{\sqrt{2}}\right) \left(\frac{V_{NOM}}{V_{LOW}}\right) \left((1.1)^*\right)$$

$I_{rms} = (I_{OUT})\,(1.2)$ (Full-wave center tap)

where:

V_{OUT} = DC regulated output voltage

V_{REG} = Minimum input-output voltage of regulator

V_{RECT} = Rectifier forward voltage drop at three times DC output current

V_{RIPPLE} = 1/2 peak-to-peak capacitor ripple voltage

$$= \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$$

*The factor of 1.1 is only an approximate factor accounting for load regulation of the transformer.

V_{NOM} = Nominal line voltage AC rms

V_{LOW} = Low line voltage AC rms

I_{OUT} = DC output current

Example: I_{OUT} = 10A, V_{OUT} = 5V

Assume: V_{REG} = 2.2V, V_{RECT} = 1.2V

V_{RIPPLE} = 2 Vp-p, V_{NOM} = 115V,

V_{LOW} = 105V

$$V_{rms} = \left(\frac{5 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{115}{105}\right) 1.1$$

$$= 8.01\ V_{rms}$$

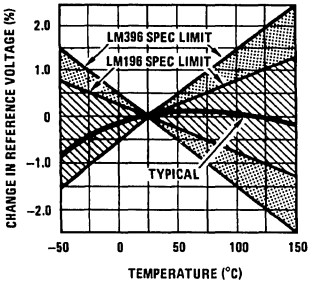
$$\text{Capacitor C} = \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2 \times V_{RIPPLE}}$$

$$= \frac{(5.3 \times 10^{-3})(10)}{2} = 26{,}500\ \mu F$$

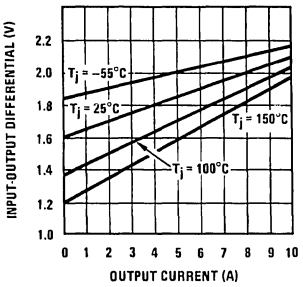
The diodes used in a full-wave rectified capacitor input supply must have a DC current rating considerably higher than the average current flowing through them. In a 10A supply, for instance, the average current through each diode is only 5A, but the diodes should have a rating of 10A–15A. There are many reasons for this, both thermal and electrical. The diodes conduct current in pulses about 3.5 ms wide with a peak value of 5–8 times the average value, and an rms value 1.5–2.0 times the average value. This results in long term diode heating roughly equivalent to 10A DC current. The most demanding condition however, may be the one cycle surge through the diode during power turn on. The peak value of the surge is about 10–20 times the DC output current of the supply, or 100A–200A for a 10A supply. The diodes must have a one cycle non-repetitive surge rating of 200A or more, and this is usually not found in a diode with less than 10A average current rating. Keep in mind that even though the LM196 may be used at current levels below 10A, the diodes may still have to survive shorted output conditions where average current could rise to 12A–15A. Smaller transformers and filter capacitors used in lower current supplies will reduce surge currents, but unless specific information is available on worst-case surges, it is best not to economize on diodes. Stud-mounted devices in a DO-4 package are recommended. Cathode-to-case types may be bolted directly to the same heat sink as the LM196 because the case of the regulator is its power input. Part numbers to consider are the 1N1200 series rated at 12A average current in a DO-4 stud package. Additional types include common cathode duals in a TO-3 package, both standard and Schottky, and various duals in plastic filled assemblies. Schottky diodes will improve efficiency, especially in low voltage applications. In a 5V supply for instance, Schottky diodes will decrease wasted power by up to 6W, or alternatively provide an additional 5% "drop out" margin for low-line conditions. Several manufacturers are producing "high efficiency" diodes with a forward voltage drop nearly as good as Schottkys at high current levels. These devices do not have the low breakdown voltages of Schottkys, so are much less prone to reverse breakdown induced failures.

Typical Performance Characteristics

Reference Drift

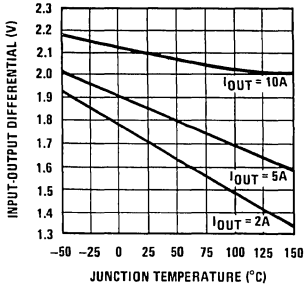


Minimum Input-Output Differential*



*V_{IN} is reduced until output drops 2%

Minimum Input-Output Differential*



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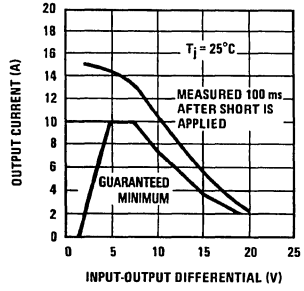
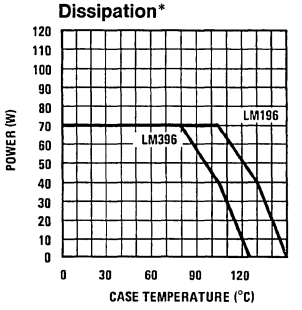
*V_{IN} is reduced until output drops 2%

Current Limit

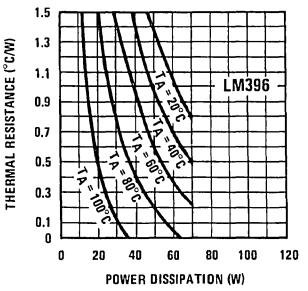


Maximum Power Dissipation*



*As limited by maximum junction temperature.

Maximum Heat Sink Thermal Resistance*



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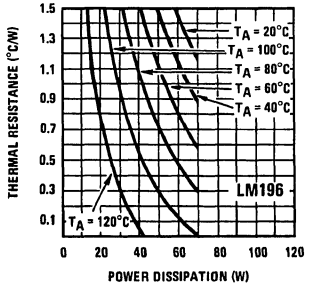
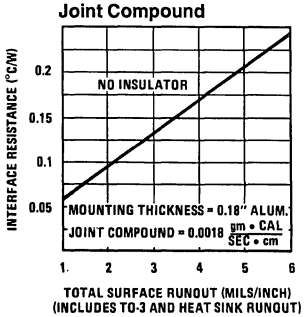
*See "Heat Sinking" under Applications Hints.

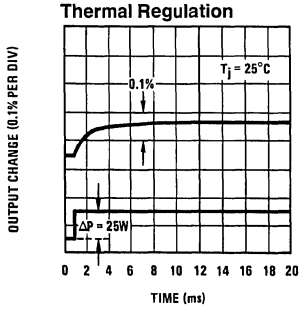
Maximum Heat Sink Thermal Resistance*



TO-3 Interface Thermal Resistance Using Thermal Joint Compound



Thermal Regulation



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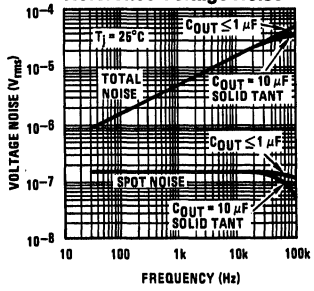
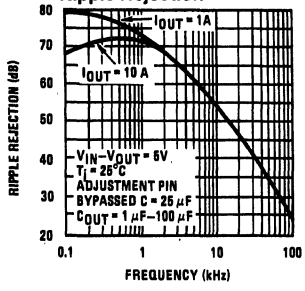
*See "Heat Sinking" under Application Hints.

Typical Performance Characteristics (Continued)

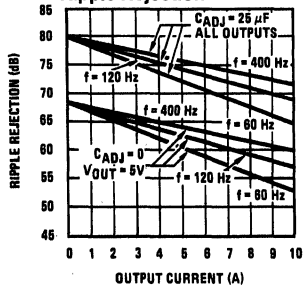
Reference Voltage Noise*



Ripple Rejection



Ripple Rejection



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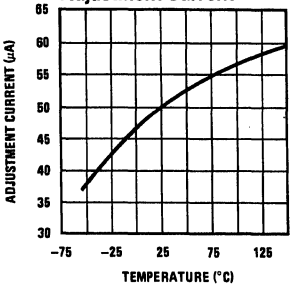
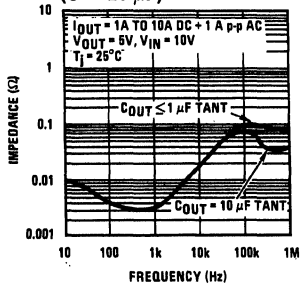
*To obtain output noise, multiply by $V_{OUT}/1.25$ if adjustment pinis not bypassed.

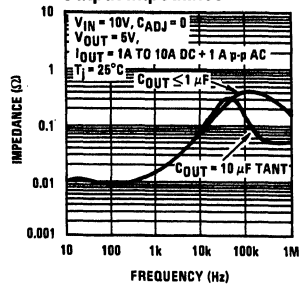
Adjustment Current



Output Impedance Adjustment Pin Bypassed (C = 25 μF)



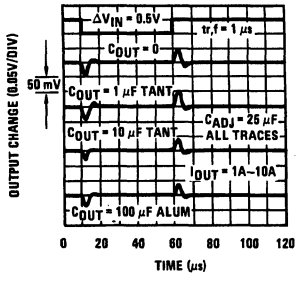
Output Impedance*



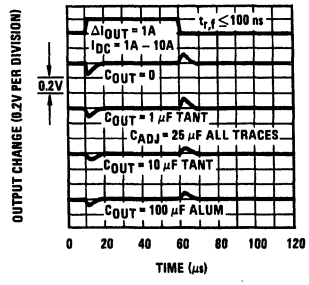
TL/H/9059–7

*For output voltages other than 5V, multiply vertical scale readings by $V_{OUT}/5$.

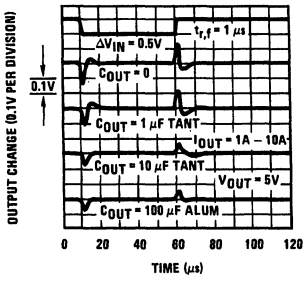
Line Transient Response Adjustment Pin Bypassed



Load Transient Response Adjustment Pin Bypassed



Line Transient Response*



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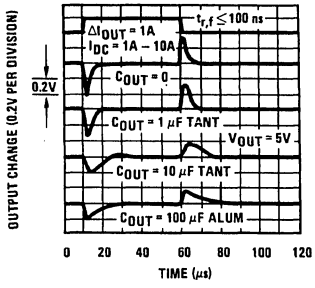
*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

Typical Performance Characteristics (Continued)

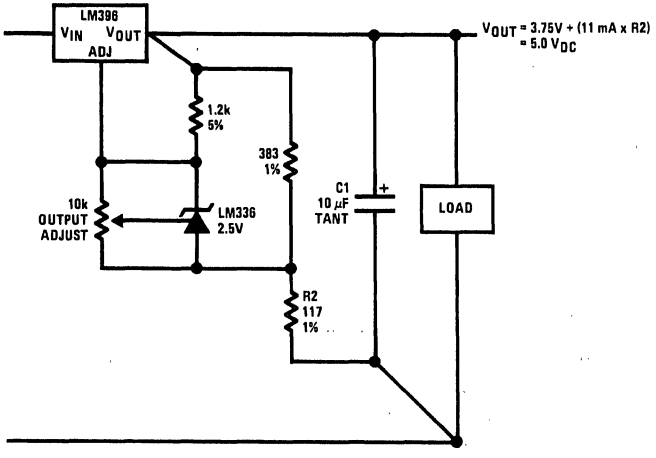
Load Transient Response*



TL/H/9059–9

*With no adjustment pin bypass. For output voltages other than 5V, multiply vertical scale by $V_{OUT}/5$.

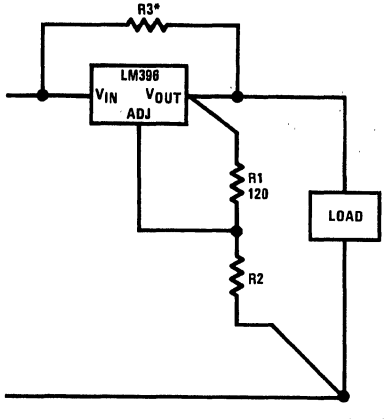
Typical Applications (Continued)



TL/H/9059–10

*Regulation can be improved by adding an LM336 reference diode to increase the effective reference voltage to 3.75V. Load and line regulation are improved by 3:1, including thermal effects.

FIGURE 3. Improving Regulation*



TL/H/9059–11

*R3 is selected to supply partial load current. Therefore, a minimum load must always be maintained to prevent the regulated output from rising uncontrolled. R3 must be greater than $(V_{MAX} - V_{OUT})/I_{MIN}$, where V_{MAX} is worst-case high input voltage, and I_{MIN} is the minimum load current. R3 must be rated for at least $(V_{IN} - V_{OUT})^2/R3$ watts. Regulator power dissipation will be reduced by a factor of 2–3 in a typical situation where minimum load current is 1/2 full load current. Regulator dissipation will peak at:

$$V_{IN} = \frac{(R3)(I_{OUT})}{2} + V_{OUT}$$

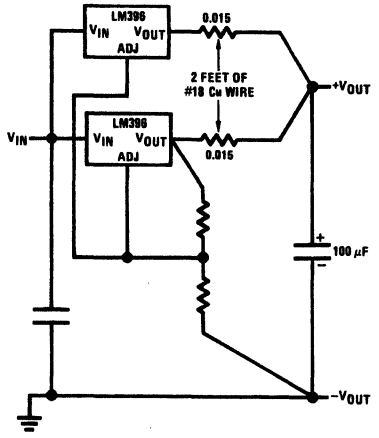
and will be equal to:

$$P_{MAX} = \frac{(R3)(I_{OUT})^2}{4} \text{ Assuming: } (R3)(I_{OUT}) \leq V_{MAX} - V_{OUT}$$

A few words of caution; (1) R3 power rating must be increased to $(V_{MAX})^2/R3$ if continuous output shorts are possible. (2) Under normal load conditions, system power dissipation is not changed, but under short circuit conditions *system* power dissipation increases by $(V_{IN})^2/R3$ watts over the already high power of a shorted regulator. The LM196 will not be harmed and neither will R3 if it is rated properly, but the raw supply components must be able to withstand the overload also. Thermal shutdown of the LM196 will probably occur for sustained shorts, somewhat alleviating the problem.

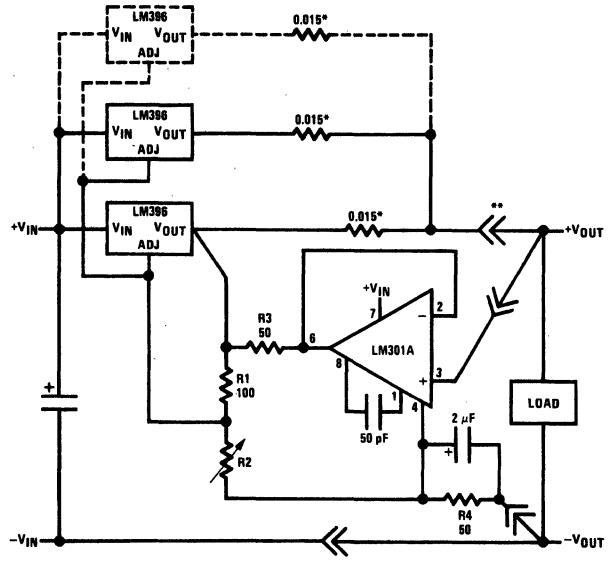
FIGURE 4. Reducing Regulator Power Dissipation

Typical Applications (Continued)



TL/H/9059–12

FIGURE 5a. Paralleling Regulators

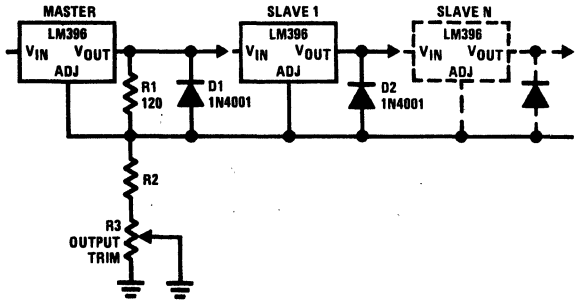


TL/H/9059–13

*2 feet of #18 CU wire

**Total voltage drop across output wire and connector should not exceed 0.3V

FIGURE 5b

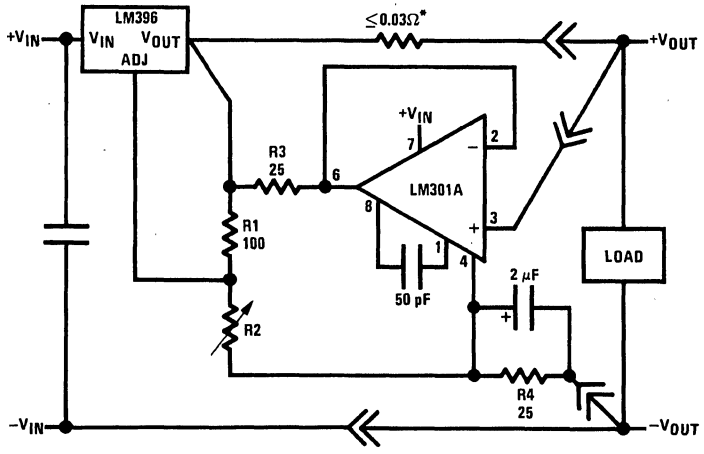


TL/H/9059–14

Output will be within ±20 mV at 25°C, no load. Regulation of tracking units is improved by $V_{OUT}/1.25$ compared to a normal connection. Regulation of master unit is unchanged. Load or input voltage changes on slave units do not affect other units, but all units will be affected by changes on master. A short on any output will cause all other outputs to drop to approximately 2V.

FIGURE 6. Tracking Regulators

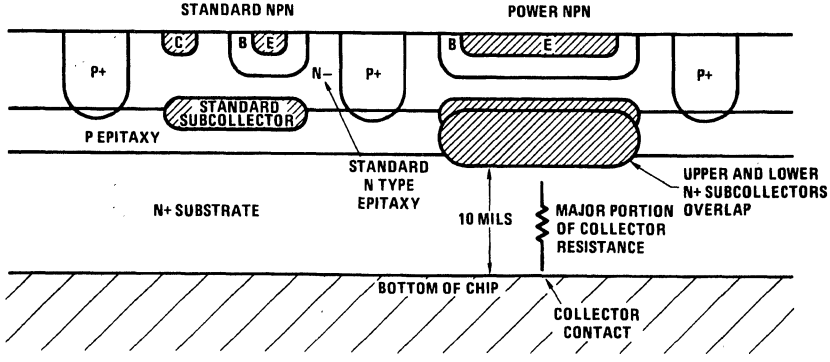
Typical Applications (Continued)



TL/H/9059–15

*Parasatic line resistance created by wiring connectors, or parallel ballasting.

FIGURE 7. Correcting for Line Losses



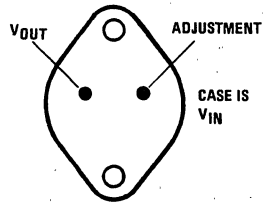
TL/H/9059–16

Power NPNs have low collecter resistance, and do not require collector bond wires. Collectors are all common to substrate. Standard NPNs are still isolated.

FIGURE 8. Process Technology

Connection Diagram

Metal Can Package

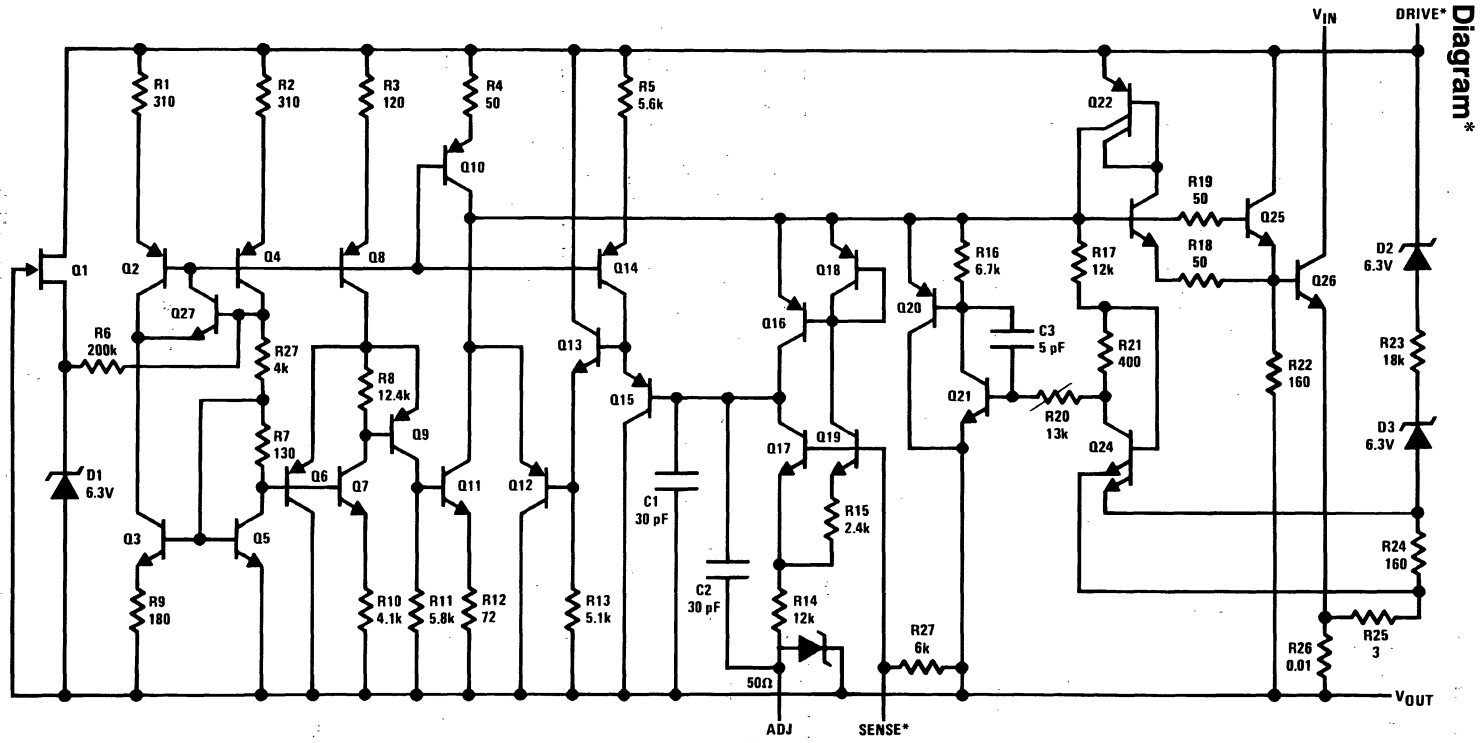


TL/H/9059–18

Bottom View

Order Number LM196K STEEL or LM396K STEEL
See NS Package Number K02B

Schematic Diagram*



TL/H/9059–17

*Drive is tied to V_{IN} and sense is tied to V_{OUT} on LM196 and LM396.

National Semiconductor

LM317L 3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is available packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

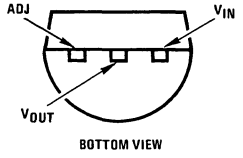
The LM317L is available in a standard TO-92 transistor package and the SO-8 package. The LM317L is rated for operation over a −25°C to 125°C range.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

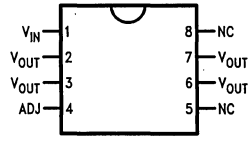
Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Connection Diagram



TL/H/9064-4

Order Number LM317LZ
See NS Package
Number Z03A

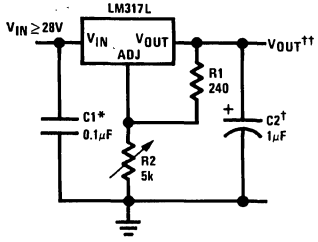


TL/H/9064-5

Order Number LM317LM
See NS Package
Number M08A

Typical Applications

1.2V–25V Adjustable Regulator



TL/H/9064-1

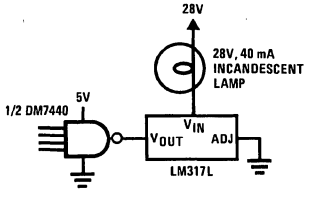
Full output current not available at high input-output voltages

†Optional—improves transient response

*Needed if device is more than 6 inches from filter capacitors

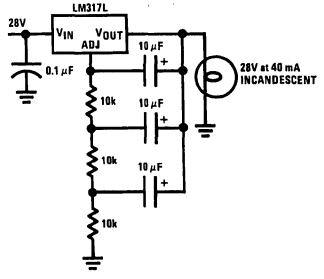
$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

Fully Protected (Bulletproof) Lamp Driver



TL/H/9064-2

Lamp Flasher



TL/H/9064-3

Output rate—4 flashes per second at 10% duty cycle

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Output is Short Circuit Protected

ESD rating to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_j = 25°C$, $3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_L \le 20$ mA (Note 2)		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, 5 mA $\le I_{OUT} \le I_{MAX}$, (Note 2)		0.1	0.5	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	5 mA $\le I_L \le$ 100 mA $3V \le (V_{IN} - V_{OUT}) \le 40V$, P ≤ 625 mW		0.2	5	μA
Reference Voltage	$3V \le (V_{IN} - V_{OUT}) \le 40V$, (Note 3) 5 mA $\le I_{OUT} \le$ 100 mA, P ≤ 625 mW	1.20	1.25	1.30	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $I_L \le 20$ mA (Note 2)		0.02	0.07	%/V
Load Regulation	5 mA $\le I_{OUT} \le$ 100 mA, (Note 2)		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{Max}$		0.65		%
Minimum Load Current	$(V_{IN} - V_{OUT}) \le 40V$ $3V \le (V_{IN} - V_{OUT}) \le 15V$		3.5 1.5	5 2.5	mA
Current Limit	$3V \le (V_{IN} - V_{OUT}) \le 13V$ $(V_{IN} - V_{OUT}) = 40V$	100 25	200 50	300 150	mA mA
Rms Output Noise, % of V_{OUT}	$T_j = 25°C$, 10 Hz ≤ f ≤ 10 kHz		0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, $C_{ADJ} = 0$ C_{ADJ} = 10 μF	 66	65 80		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1	%
Thermal Resistance Junction to Ambient	Z Package 0.4" Leads Z Package 0.125 Leads SO-8 Package		180 160 165		°C/W °C/W °C/W
Thermal Rating of SO Package			165		°C/W

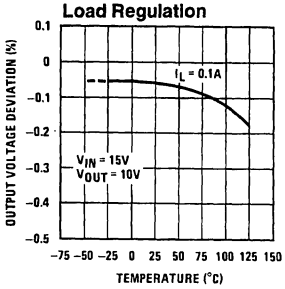
Note 1: Unless otherwise noted, these specifications apply: $-25°C \le T_j \le 125°C$ for the LM317L; $V_{IN} - V_{OUT} = 5V$ and I_{OUT} = 40 mA. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

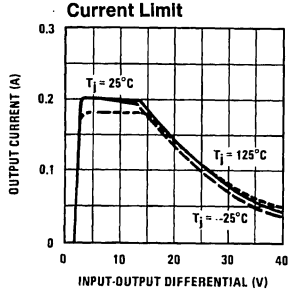
Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to PC board.

Typical Performance Characteristics (Output capacitor = 0 μF unless otherwise noted.)

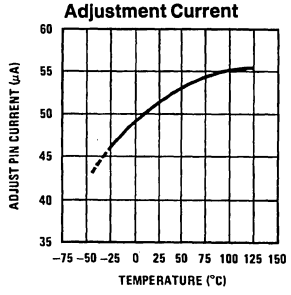
Load Regulation



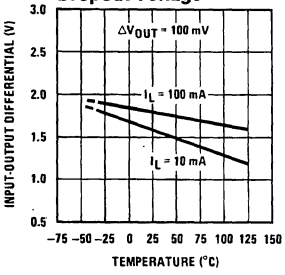
Current Limit



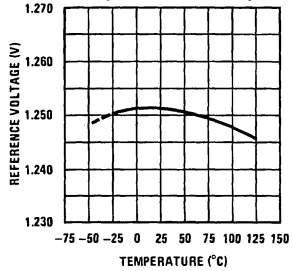
Adjustment Current



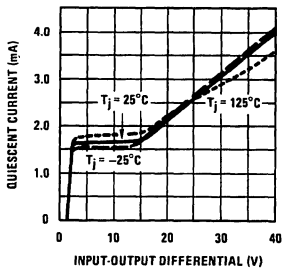
Dropout Voltage



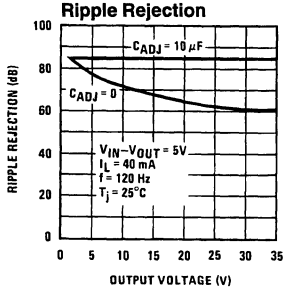
Reference Voltage Temperature Stability



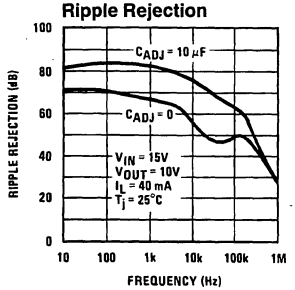
Minimum Operating Current



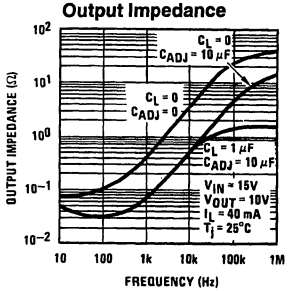
Ripple Rejection



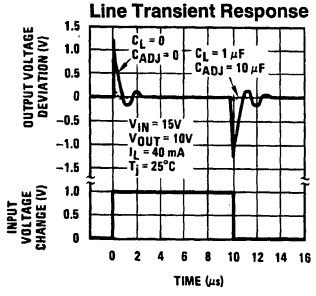
Ripple Rejection



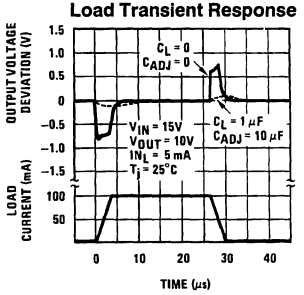
Output Impedance



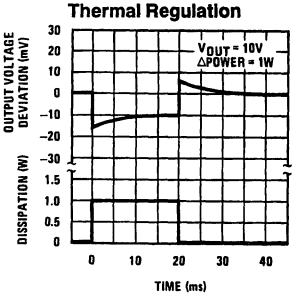
Line Transient Response



Load Transient Response



Thermal Regulation



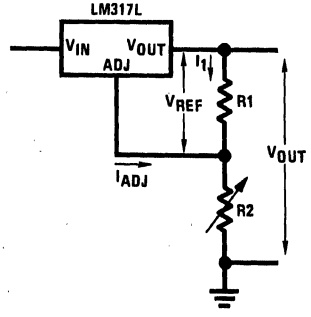
TL/H/9064–6

Application Hints

In operation, the LM317L develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R2)$$

Since the 100 μA current from the adjustment terminal represents an error term, the LM317L was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.



TL/H/9064–7

FIGURE 1

External Capacitors

An input bypass capacitor is recommended in case the regulator is more than 6 inches away from the usual large filter capacitor. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possiblity of problems.

The adjustment terminal can be bypassed to ground on the LM317L to improve ripple rejection and noise. This bypass capacitor prevents ripple and noise from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. *Solid tantalum capacitors have low impedance even at high frequencies.* Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, a 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

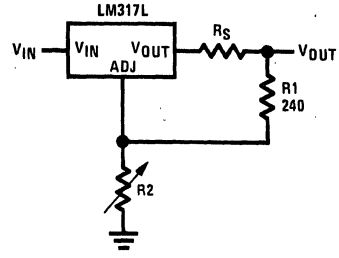
Although the LM317L is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM317L is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

With the TO-92 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the output pin. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.



TL/H/9064–8

FIGURE 2. Regulator with Line Resistance in Output Lead

Application Hints (Continued)

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per watt, within the first 10 ms after a step of power is applied. The LM317L specification is 0.2%/W, maximum.

In the Thermal Regulation curve at the bottom of the Typical Performance Characteristics page, a typical LM317L's output changes only 7 mV (or 0.07% of $V_{OUT} = -10V$) when a 1W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.2%/W × 1W = 0.2% maximum. When the 1W pulse is ended, the thermal regulation again shows a 7 mV change as the gradients across the LM317L chip die out. Note that the load regulation error of about 14 mV (0.14%) is additional to the thermal regulation error.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM317L, this discharge path is through a large junction that is able to sustain a 2A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, the LM317L's ballast resistors and output structure limit the peak current to a low enough level so that there is no need to use a protection diode.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM317L is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM317L with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

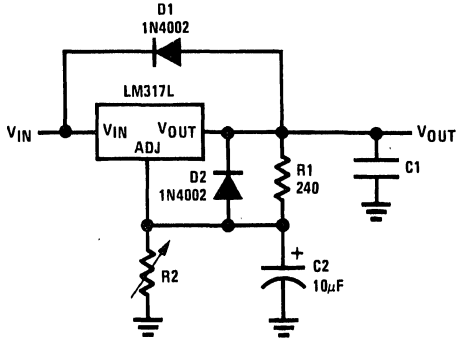


FIGURE 3. Regulator with Protection Diodes

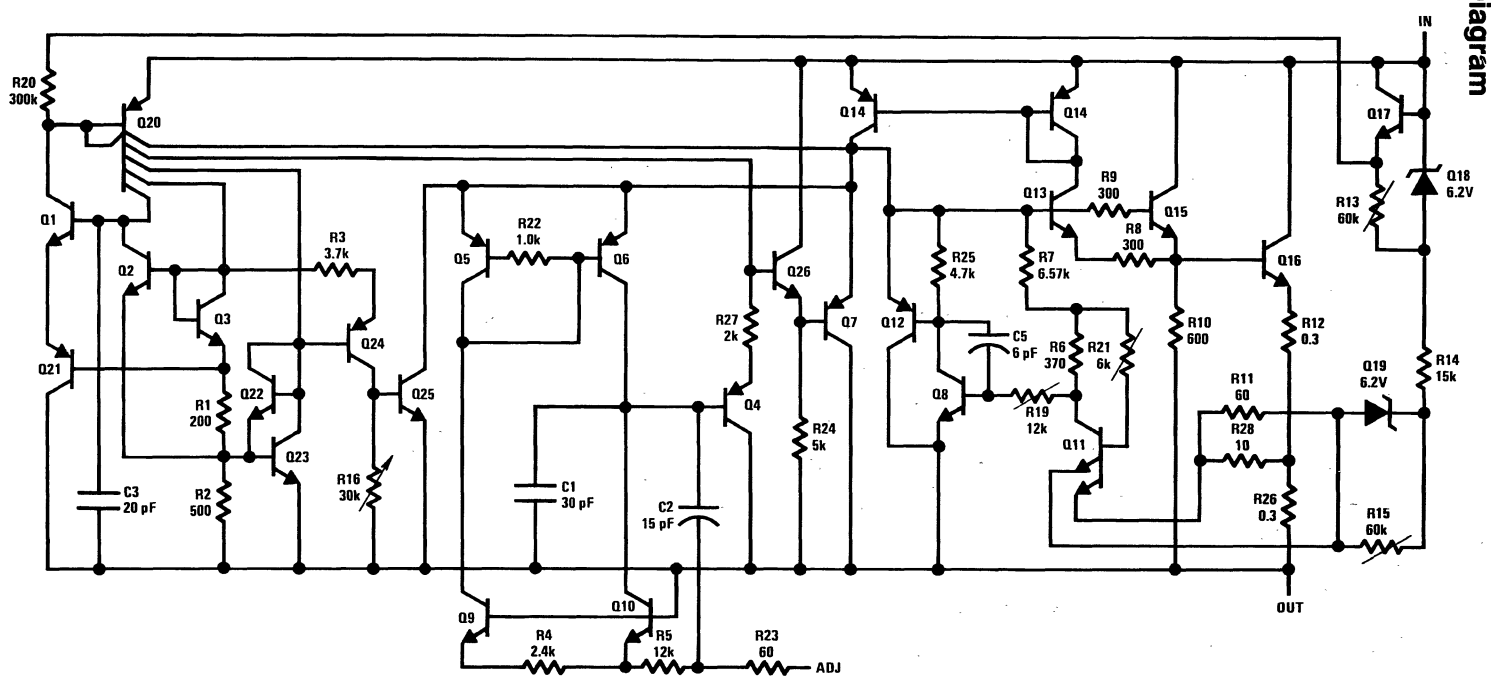
TL/H/9064–9

$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$

D1 protects against C1

D2 protects against C2

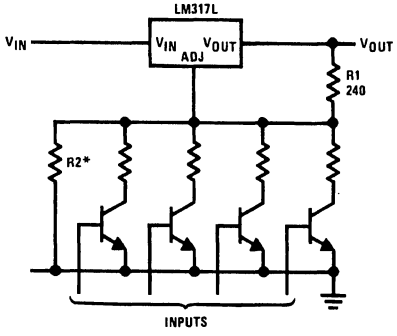
Schematic Diagram



TL/H/9064–10

Typical Applications (Continued)

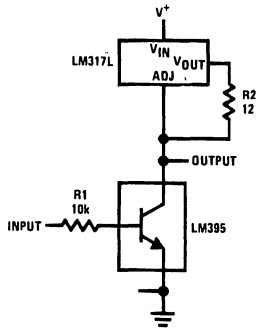
Digitally Selected Outputs



TL/H/9064–11

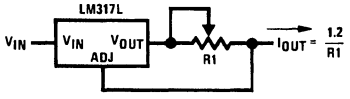
*Sets maximum V_{OUT}

High Gain Amplifier



TL/H/9064–12

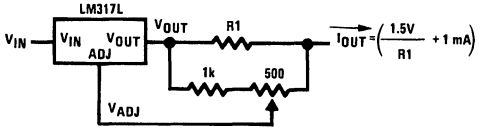
Adjustable Current Limiter



TL/H/9064–13

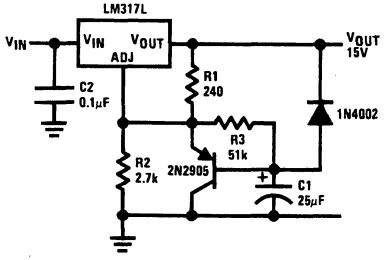
$12 \leq R1 \leq 240$

Precision Current Limiter



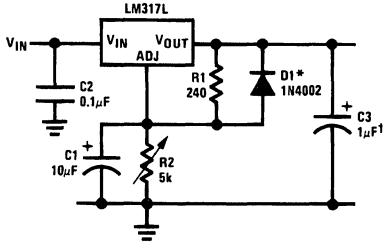
TL/H/9064–14

Slow Turn-On 15V Regulator



TL/H/9064–15

Adjustable Regulator with Improved Ripple Rejection

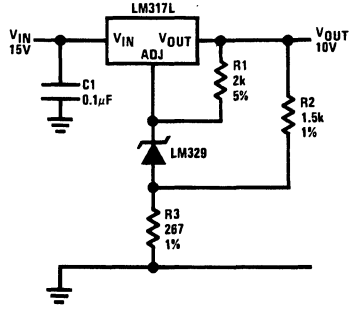


†Solid tantalum

*Discharges C1 if output is shorted to ground

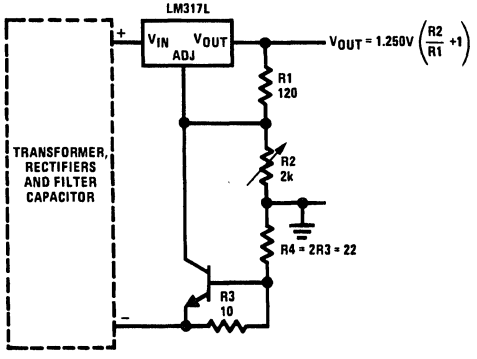
TL/H/9064–16

High Stability 10V Regulator



TL/H/9064–17

Adjustable Regulator with Current Limiter



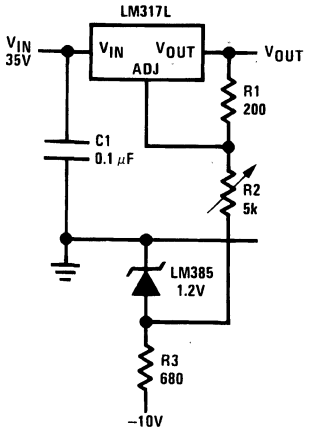
TL/H/9064–18

Short circuit current is approximately 600 mV/R3, or 60 mA (compared to LM317LZ's 200 mA current limit).

At 25 mA output only 3/4V of drop occurs in R3 and R4.

Typical Applications (Continued)

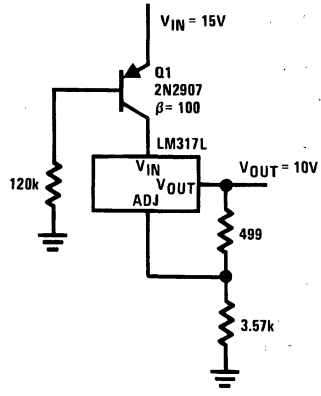
0V–30V Regulator



TL/H/9064–19

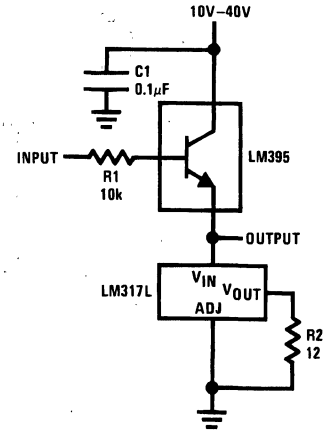
Full output current not available at high input-output voltages

Regulator With 15 mA Short Circuit Current



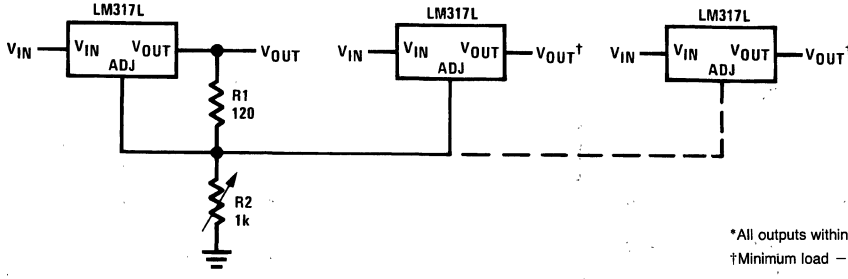
TL/H/9064–20

Power Follower



TL/H/9064–21

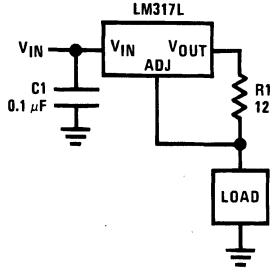
Adjusting Multiple On-Card Regulators with Single Control*



*All outputs within ± 100 mV
†Minimum load −5mA

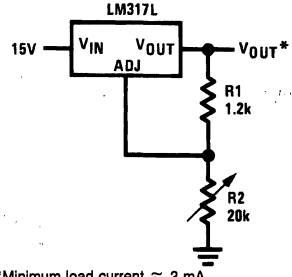
TL/H/9064–22

100 mA Current Regulator



TL/H/9064–23

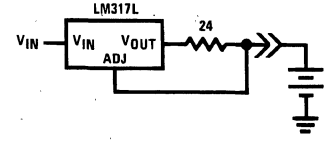
1.2V–12V Regulator with Minimum Program Current



*Minimum load current ≈ 2 mA

TL/H/9064–24

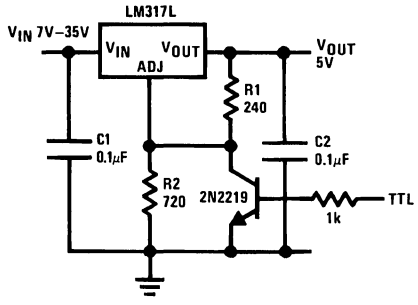
50 mA Constant Current Battery Charger for Nickel-Cadmium Batteries



TL/H/9064–25

Typical Applications (Continued)

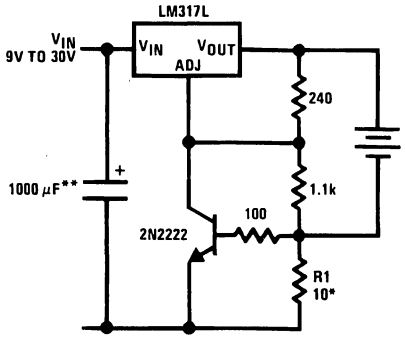
5V Logic Regulator with Electronic Shutdown*



TL/H/9064–26

*Minimum output ≈ 1.2V

Current Limited 6V Charger

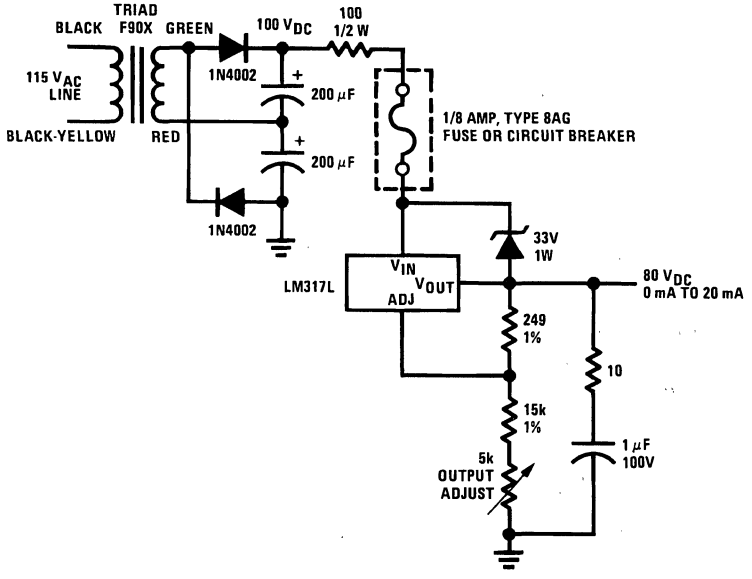


TL/H/9064–27

*Sets peak current, I_{PEAK} = 0.6V/R1

**1000 μF is recommended to filter out any input transients.

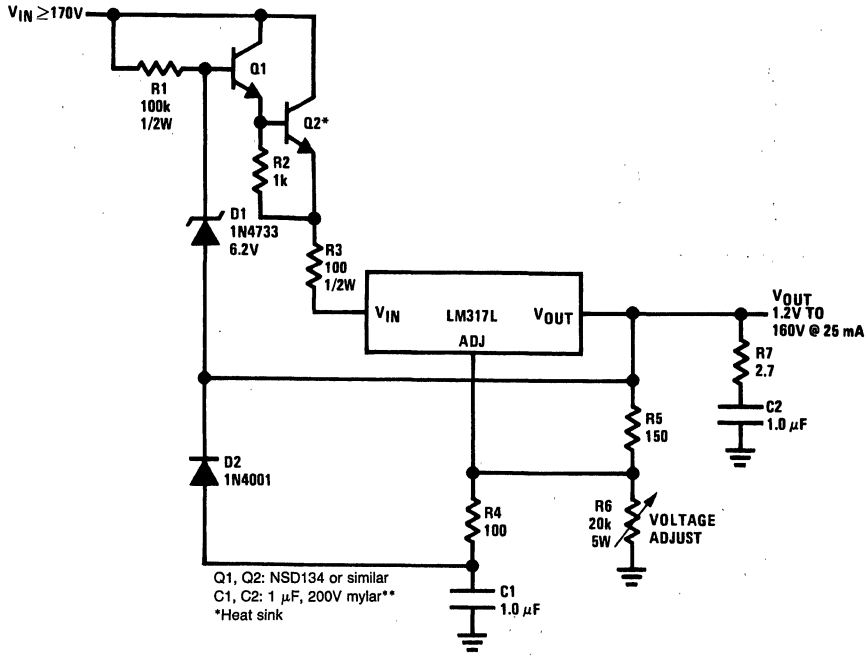
Short Circuit Protected 80V Supply



TL/H/9064–28

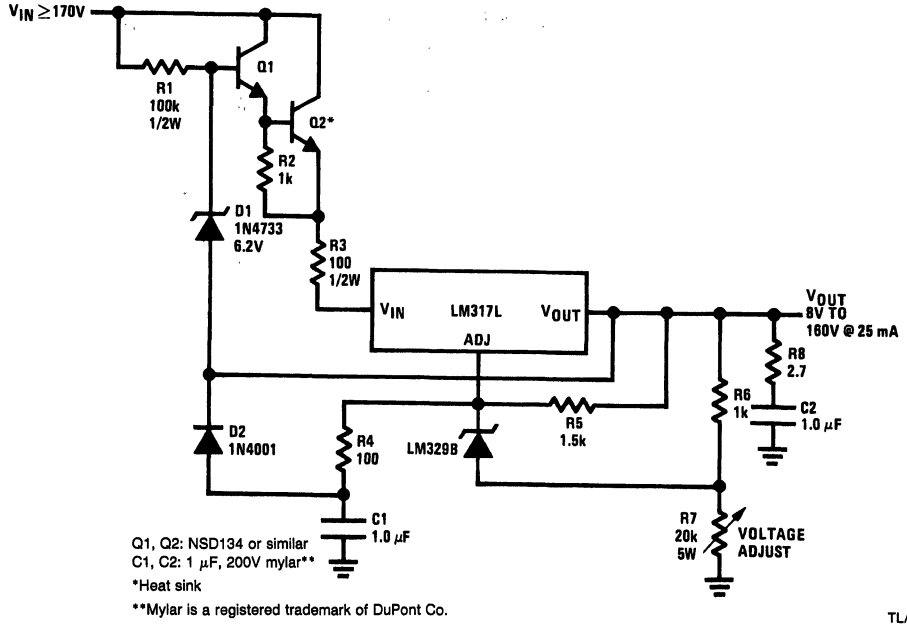
Typical Applications (Continued)

Basic High Voltage Regulator



TL/H/9064–29

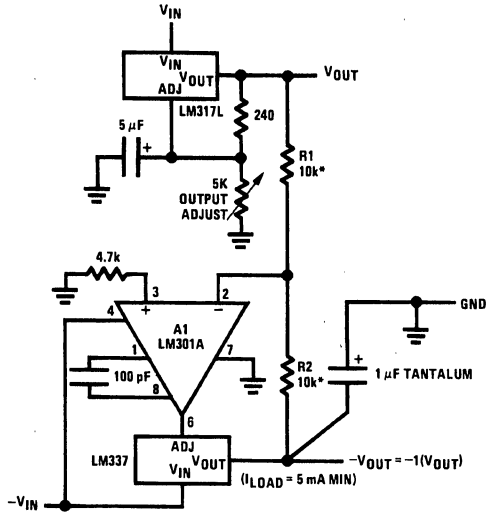
Precision High Voltage Regulator



TL/H/9064–30

Typical Applications (Continued)

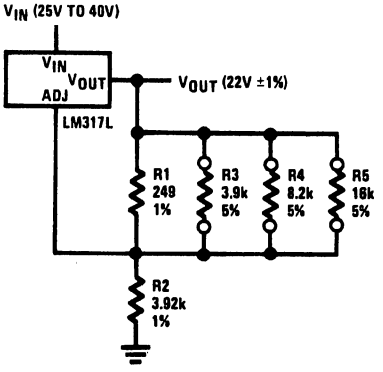
Tracking Regulator



TL/H/9064–31

A1 = LM301A, LM307, or LF13741 only
R1, R2 = matched resistors with good TC tracking

Regulator With Trimmable Output Voltage



TL/H/9064–32

Trim Procedure:

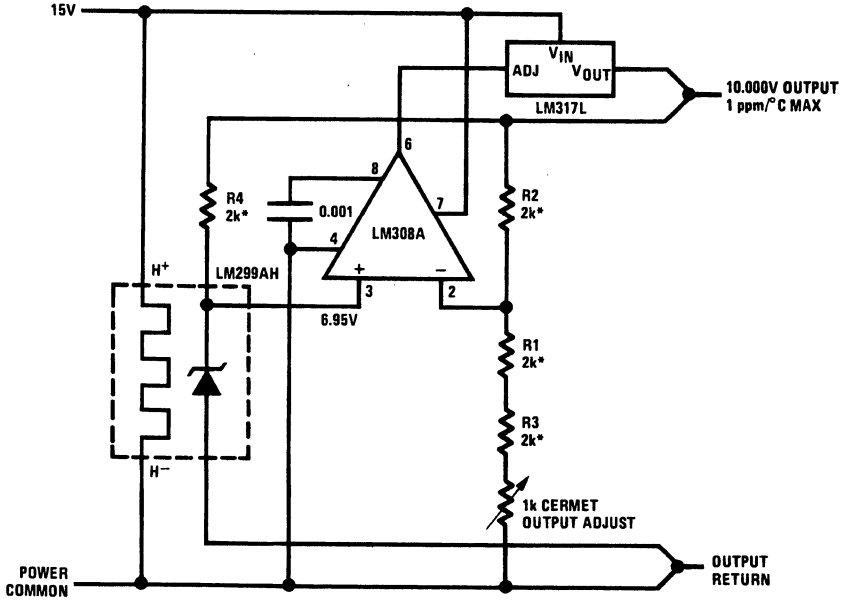
— If V_{OUT} is 23.08V or higher, cut out R3 (if lower, don't cut it out).

— Then if V_{OUT} is 22.47V or higher, cut out R4 (if lower, don't).

— Then if V_{OUT} is 22.16V or higher, cut out R5 (if lower, don't).

This will trim the output to well within ±1% of 22.00 V_{DC}, without any of the expense or uncertainty of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Precision Reference with Short-Circuit Proof Output



TL/H/9064–33

*R1–R4 from thin-film network,
Beckman 694-3-R2K-D or similar

National Semiconductor

LM320L 3-Terminal Negative Regulators

General Description

The LM320L series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V, with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM320L series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM320L series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM320L series is available in the 3-lead TO-92 package.

For output voltages other than −5V, −12V and −15V, the LM137 and LM137HV series provide an output voltage range from −1.2V to −47V.

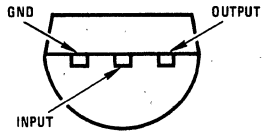
Features

- Preset output voltage error is less than ±5% over load, line and temperature
- LM320L is specified at an output current of 100 mA
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}/mA
- Easily compensated with a small 0.1 μF output capacitor

Device	Package	Rated Power Dissipation	Design Output Current
LM320L	TO-92 (Z)	0.6W	0.1A

Connection Diagram

TO-92 Plastic Package (Z)



TL/H/7621–1

Order Number LM320LZ-5.0, LM320LZ-12 or LM320LZ-15
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage
V_{OUT} = −5V 12V and 15V −35V
Internal Power Dissipation
(Notes 1 and 3) Internally Limited

Operating Temperature Range 0°C to +70°C
Maximum Junction Temperature +125°C
Storage Temperature Range
Molded TO-92 −55°C to +150°C
Lead Temperature
(Soldering, 10 sec.) 260°C

Electrical Characteristics (Note 2) T_A = 0°C to +70°C unless otherwise noted.

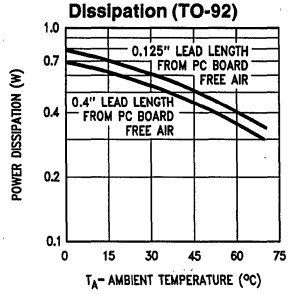
Output Voltage			**−5V**			**−12V**			**−15V**			**Units**
Input Voltage (unless otherwise noted)			**−10V**			**−17V**			**−20V**			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
V_O	Output Voltage	T_j = 25°C, I_O = 100 mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	
		1 mA ≤ I_O ≤ 100 mA $V_{MIN} \le V_{IN} \le V_{MAX}$	−5.25 (−20 ≤ V_{IN} ≤ −7.5)		−4.75	−12.6 (−27 ≤ V_{IN} ≤ −14.8)		−11.4	−15.75 (−30 ≤ V_{IN} ≤ −18)		−14.25	V
		1 mA ≤ I_O ≤ 40 mA $V_{MIN} \le V_{IN} \le V_{MAX}$	−5.25 (−20 ≤ V_{IN} ≤ −7)		−4.75	−12.6 (−27 ≤ V_{IN} ≤ −14.5)		−11.4	−15.75 (−30 ≤ V_{IN} ≤ −17.5)		−14.25	
ΔV_O	Line Regulation	T_j = 25°C, I_O = 100 mA			60			45			45	mV
		$V_{MIN} \le V_{IN} \le V_{MAX}$	(−20 ≤ V_{IN} ≤ −7.3)			(−27 ≤ V_{IN} ≤ −14.6)			(−30 ≤ V_{IN} ≤ −17.7)			V
		T_j = 25°C, I_O = 40 mA			60			45			45	mV
		$V_{MIN} \le V_{IN} \le V_{MAX}$	(−20 ≤ V_{IN} ≤ −7)			(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)			V
ΔV_O	Load Regulation	T_j = 25°C 1 mA ≤ I_O ≤ 100 mA			50			100			125	mV
ΔV_O	Long Term Stability	I_O = 100 mA		20			48			60		mV/khr
I_Q	Quiescent Current	I_O = 100 mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1 mA ≤ I_O ≤ 100 mA			0.3			0.3			0.3	mA
		1 mA ≤ I_O ≤ 40 mA			0.1			0.1			0.1	
		I_O = 100 mA $V_{MIN} \le V_{IN} \le V_{MAX}$			0.25 (−20 ≤ V_{IN} ≤ −7.5)			0.25 (−27 ≤ V_{IN} ≤ −14.8)			0.25 (−30 ≤ V_{IN} ≤ −18)	mA V
V_n	Output Noise Voltage	T_j = 25°C, I_O = 100 mA f = 10 Hz–10 kHz		40			96			120		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	T_j = 25°C, I_O = 100 mA f = 120 Hz	50			52			50			dB
	Input Voltage Required to Maintain Line Regulation	T_j = 25°C I_O = 100 mA			−7.3			−14.6			−17.7	V
		I_O = 40 mA			−7.0			−14.5			−17.5	

Note 1: Thermal resistance of Z package is typically 60°C/W θ_{JC}, 232°C/W θ_{JA} at still air, and 88°C/W at 400 ft/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

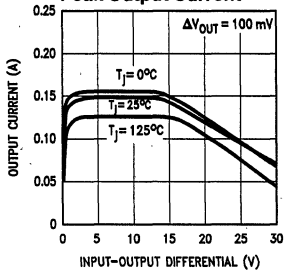
Note 2: To ensure constant junction temperature pulse testing is used.

Typical Performance Characteristics

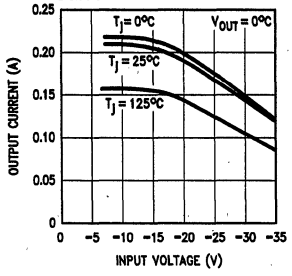
Maximum Average Power Dissipation (TO-92)



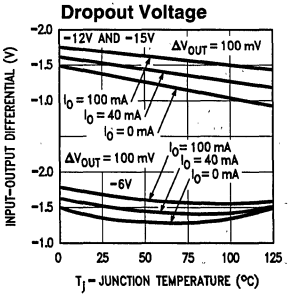
Peak Output Current



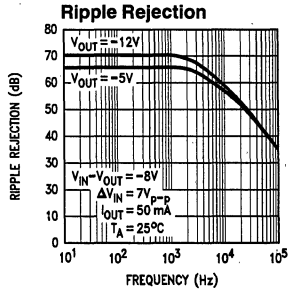
Short Circuit Output Current



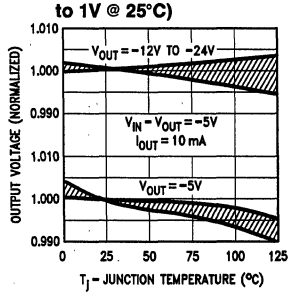
Dropout Voltage



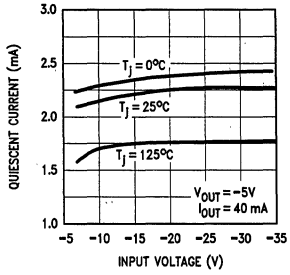
Ripple Rejection



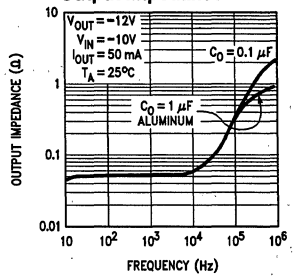
Output Voltage vs Temperature (Normalized to 1V @ 25°C)



Quiescent Current



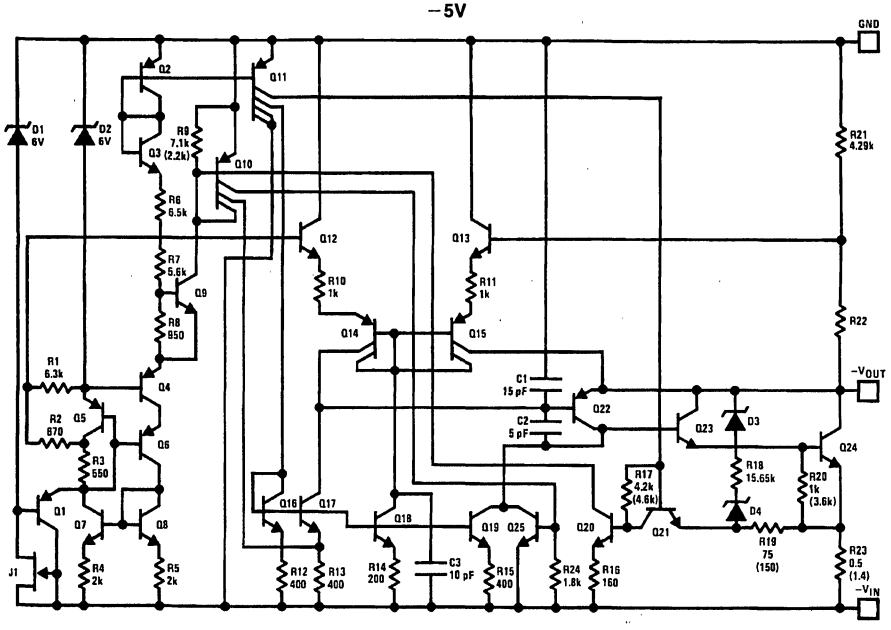
Output Impedance



TL/H/7821–2

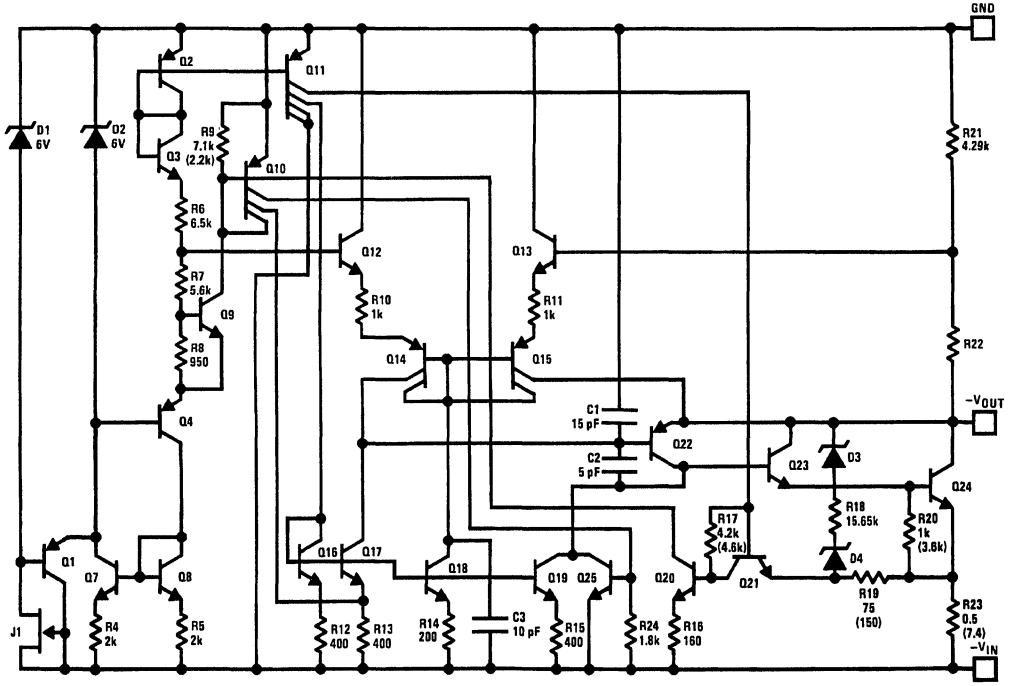
Schematic Diagrams

−5V



TL/H/7821–3

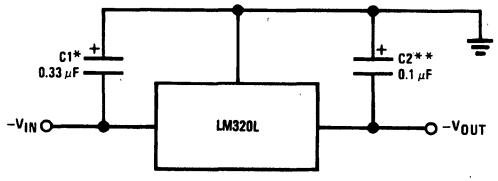
−12V and −15V



TL/H/7821–4

Typical Applications

Fixed Output Regulator

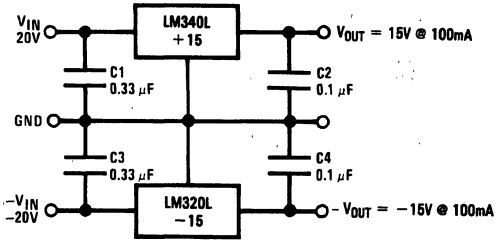


TL/H/7821–5

*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

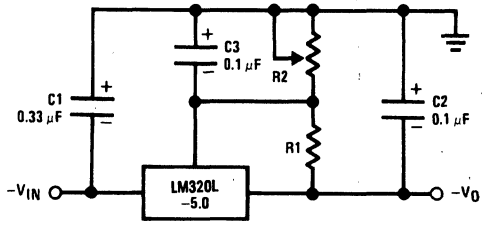
**Required for stability. A 1 μF aluminum electrolytic may be substituted.

±15V, 100 mA Dual Power Supply



TL/H/7821–7

Adjustable Output Regulator



TL/H/7821–6

$$-V_O = -5V - (5V/R1 + I_Q) \bullet R2,$$
$$5V/R1 > 3\,I_Q$$

National Semiconductor

LM330 3-Terminal Positive Regulator

General Description

The LM330 5V 3-terminal positive voltage regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

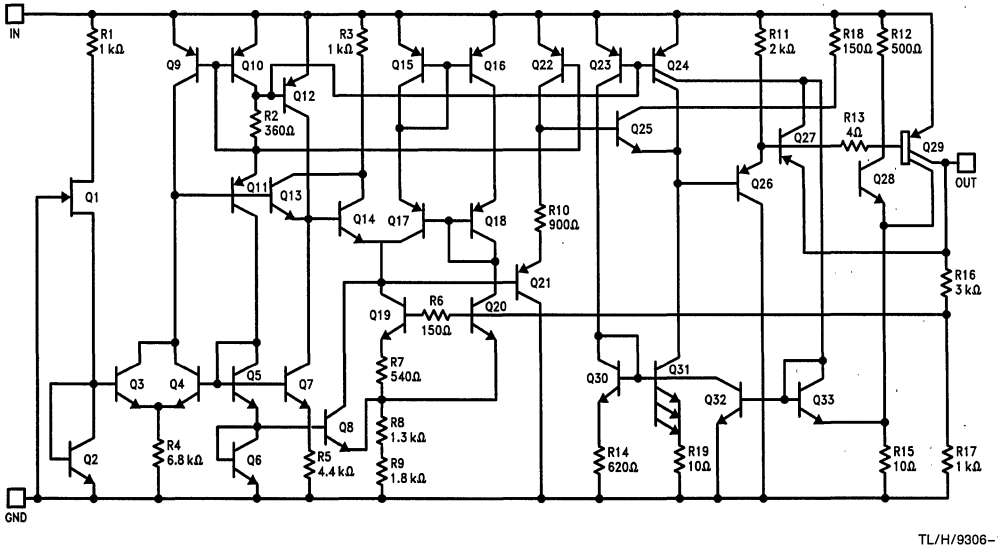
The low dropout voltage makes the LM330 useful for certain battery applications since this feature allows a longer battery discharge before the output falls out of regulation. For example, a battery supplying the regulator input voltage may discharge to 5.6V and still properly regulate the system and load voltage. Supporting this feature, the LM330 protects both itself and regulated systems from negative voltage inputs resulting from reverse installations of batteries.

Other protection features include line transient protection up to 26V, when the output actually shuts down to avoid damaging internal and external circuits. Also, the LM330 regulator cannot be harmed by a temporary mirror-image insertion.

Features

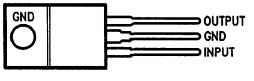
- Input-output differential less than 0.6V
- Output current of 150 mA
- Reverse battery protection
- Line transient protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in the thermal limit

Schematic and Connection Diagrams



TL/H/9306–1

(TO-220)
Plastic Package



TL/H/9306–2

Front View

Order Number LM330T-5.0
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Line Transient Protection (1000 ms)	40V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

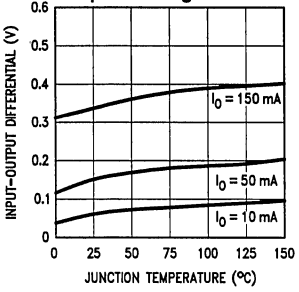
Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_o	Output Voltage	$T_j = 25°C$	4.8	5	5.2	V
	Output Voltage Over Temp	$5 < I_o < 150$ mA $6 < V_{IN} < 26V$; $0°C \le T_j \le 100°C$	4.75		5.25	
ΔV_o	Line Regulation	$9 < V_{IN} < 16V$, $I_o = 5$ mA $6 < V_{IN} < 26V$, $I_o = 5$ mA		7 30	25 60	mV
	Load Regulation	$5 < I_o < 150$ mA		14	50	
	Long Term Stability			20		mV/1000 hrs
I_Q	Quiescent Current	$I_o = 10$ mA $I_o = 50$ mA $I_o = 150$ mA		3.5 5 18	7 11 40	mA
	Line Transient Reverse Polarity	$V_{IN} = 40V$, $R_L = 100\Omega$, 1s $V_{IN} = -6V$, $R_L = 100\Omega$		14 −80		
ΔI_Q	Quiescent Current Change	$6 < V_{IN} < 26V$		10		%
V_{IN}	Overvoltage Shutdown Voltage		26	38		V
	Max Line Transient			60		
		1s, $V_o \le 5.5V$		50		
	Reverse Polarity Input Voltage			−30		
		DC $V_o > -0.3V$, $R_L = 100\Omega$		−12		
	Output Noise Voltage	10 Hz–100 kHz		50		μV
	Output Impedance	$I_o = 100$ mADC + 10 mArms		200		mΩ
	Ripple Rejection			56		dB
	Current Limit		150	400	700	mA
	Dropout Voltage	$I_o = 150$ mA		0.32	0.6	V
	Thermal Resistance	Junction to Case Junction to Ambient		4 50		°C/W

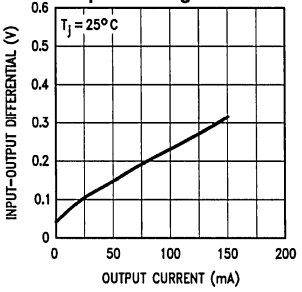
Note 1: Unless otherwise specified: $V_{IN} = 14V$, $I_o = 150$ mA, $T_j = 25°C$, C1 = 0.1 μF, C2 = 10 μF. All characteristics except noise voltage and ripple rejection are measured using pulse techniques ($t_W \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

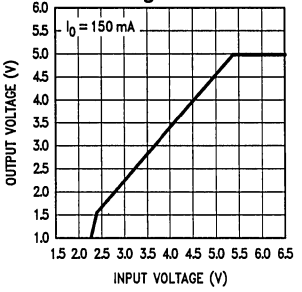
Dropout Voltage



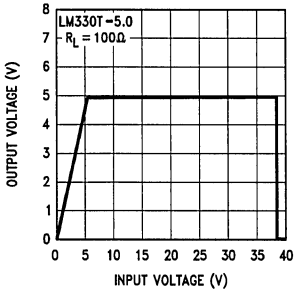
Dropout Voltage



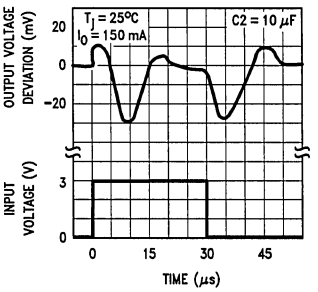
Low Voltage Behavior



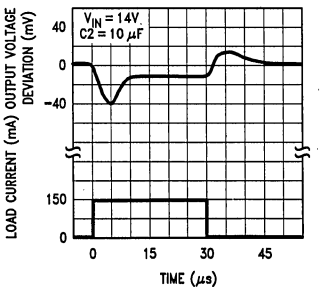
High Voltage Behavior



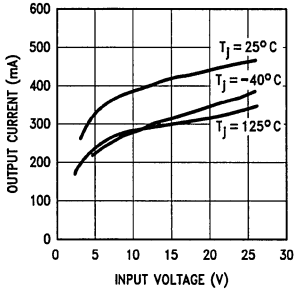
Line Transient Response



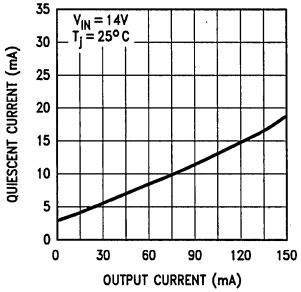
Load Transient Response



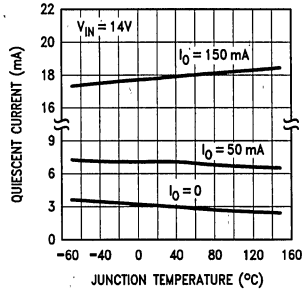
Peak Output Current



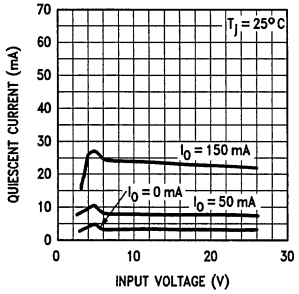
Quiescent Current



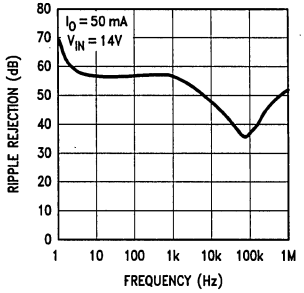
Quiescent Current



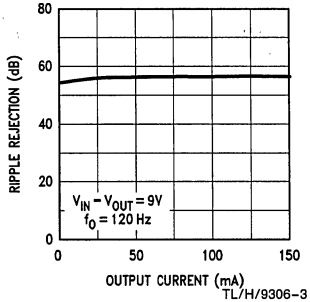
Quiescent Current



Ripple Rejection



Ripple Rejection



TL/H/9306-3

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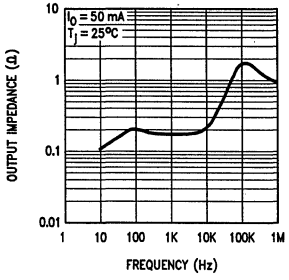
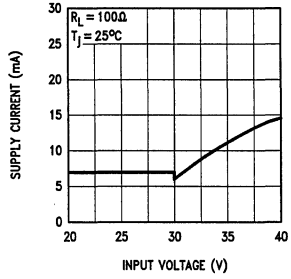
Typical Performance Characteristics (Continued)

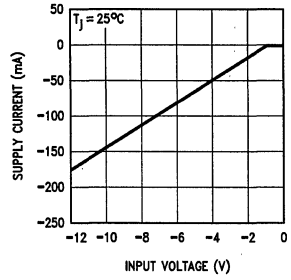
Output Impedance



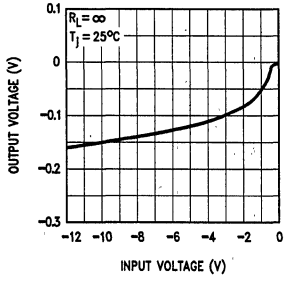
Overvoltage Supply Current



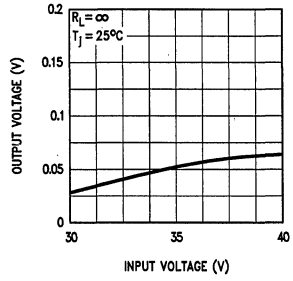
Reverse Supply Current



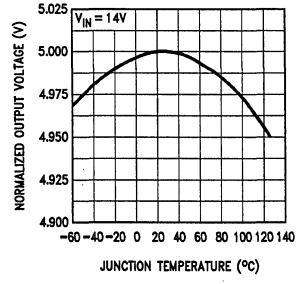
Output at Reverse Supply



Output at Overvoltage



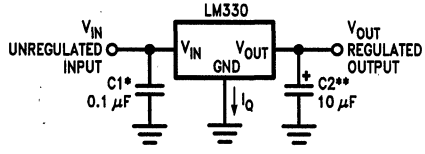
Output Voltage (Normalized to 5V at T_J = 25°C)



TL/H/9306–4

Typical Applications

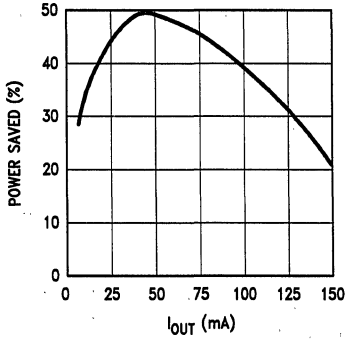
The LM330 is designed specifically to operate at lower input to output voltages. The device is designed utilizing a power lateral PNP transistor which reduces dropout voltage from 2.0V to 0.3V when compared to IC regulators using NPN pass transistors. Since the LM330 can operate at a much lower input voltage, the device power dissipation is reduced, heat sinking can be simpler and device reliability improved through lower chip operating temperature. Also, a cost savings can be utilized through use of lower power/voltage components. In applications utilizing battery power, the LM330 allows the battery voltage to drop to within 0.3V of output voltage prior to the voltage regulator dropping out of regulation.



TL/H/9306–5

* Required if regulator is located far from power supply filter.

** C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 10 μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulation.



TL/H/9306–6

Note: Compared to IC regulator with 2.0V dropout voltage and $I_{Qmax.}$ = 6.0 mA.

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM337L 3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, only a single 1 μF solid tantalum output capacitor is needed unless the device is situated more than 6 inches from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM337L is available in a standard TO-92 transistor package and a SO-8 surface mount package. The LM337L is rated for operation over a −25°C to +125°C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

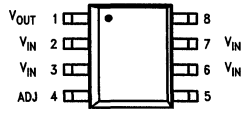
Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

Connection Diagram

TL/H/9134-1

Bottom View



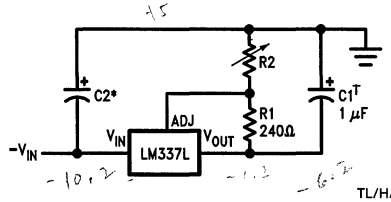
TL/H/9134-2

Top View

Order Number LM337LM or LM337LZ
See NS Package Number M08A or Z03A

Typical Applications

1.2V–25V Adjustable Regulator



TL/H/9134-3

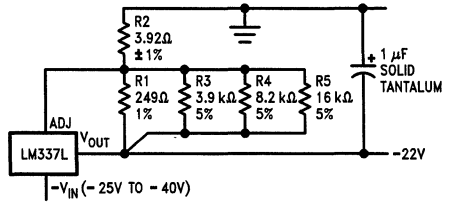
Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{240\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power supply filter capacitor

Regulator with Trimmable Output Voltage



TL/H/9134-4

Trim Procedure:

—If V_{OUT} is −23.08V or bigger, cut out R3 (if smaller, don't cut it out).

—Then if V_{OUT} is −22.47V or bigger, cut out R4 (if smaller, don't).

—Then if V_{OUT} is −22.16V or bigger, cut out R5 (if smaller, don't).

This will trim the output to well within 1% of −22.00 V_{DC}, without any of the expense or trouble of a trim pot (see LB-46). Of course, this technique can be used at any output voltage level.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input–Output Voltage Differential	40V
Operating Junction Temperature Range	−25°C to +125°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering 4 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $5\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)		0.1	0.5	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.04	0.2	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	$5\ mA \le I_L \le 100\ mA$ $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$		0.2	5	μA
Reference Voltage	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3) $10\ mA \le I_{OUT} \le 100\ mA$, $P \le 625\ mW$	1.20	1.25	1.30	V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.07	%/V
Load Regulation	$5\ mA \le I_{OUT} \le 100\ mA$, (Note 2)		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.65		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$ $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 15V$		3.5 2.2	5 3.5	mA mA
Current Limit	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 13V$ $\lvert V_{IN} - V_{OUT} \rvert = 40V$	100 25	200 50	320 120	mA mA
Rms Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, $F = 120\ Hz$, $C_{ADJ} = 0$ $C_{ADJ} = 10\ \mu F$	 66	65 80		dB dB
Long-Term Stability	$T_A = 125°C$		0.3	1	%

Note 1: Unless otherwise specified, these specifications apply $-25°C \le T_j \le +125°C$ for the LM337L; $\lvert V_{IN} - V_{OUT} \rvert = 5V$ and $I_{OUT} = 40\ mA$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 625 mW. I_{MAX} is 100 mA.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 3: Thermal resistance of the TO-92 package is 180°C/W junction to ambient with 0.4" leads from a PC board and 160°C/W junction to ambient with 0.125" lead length to PC board. The M package θ_{JA} is 180°C/W in still air.

National Semiconductor

LM341 Series 3-Terminal Positive Regulators

General Description

The LM341-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM341-XX series is available in TO-202 and TO-220 plastic packages allowing these regulators to deliver over 0.5A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

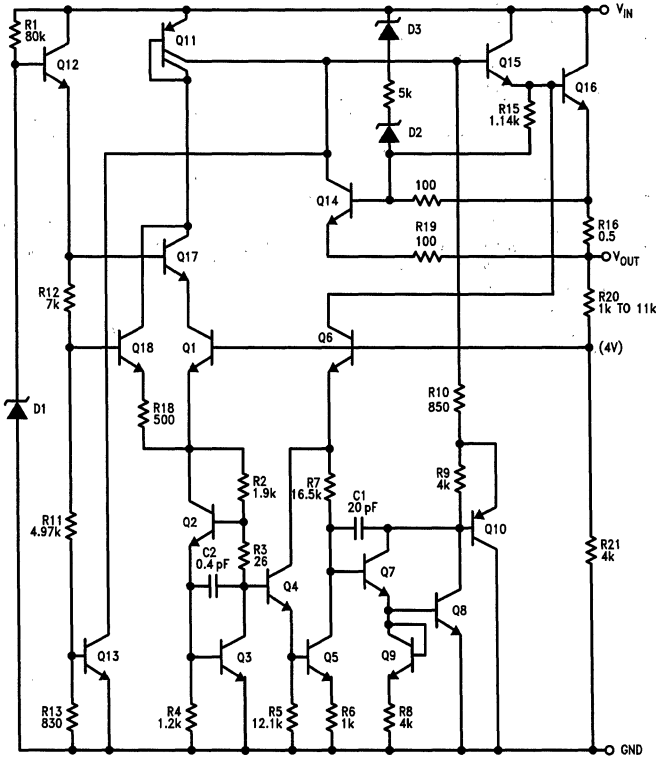
Considerable effort was expended to make the LM341-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

- Output current in excess of 0.5A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 and TO-220 package
- Special circuitry allows start-up even if output is pulled to negative voltage (± supplies)

Schematic Diagram



TL/H/10484–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	35V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	+125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+230°C
ESD Susceptibility	TBD

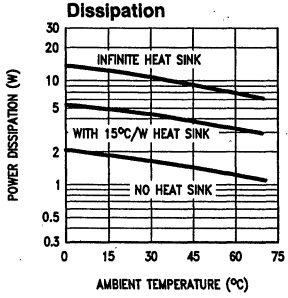
Electrical Characteristics T_A = 0°C to +70°C, I_O = 500 mA, unless otherwise noted

Output Voltage			5V			12V			15V			
Input Voltage (unless otherwise noted)			10V			19V			23V			Units
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Min	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		$P_D \le 7.5W$, 5 mA $\le I_O \le$ 500 mA and $V_{MIN} \le V_{IN} \le V_{MAX}$	4.75 (7.5≤V_{IN}≤20)		5.25	11.4 (14.8≤V_{IN}≤27)		12.6	14.25 (18≤V_{IN}≤30)		15.75	V
ΔV_O	Line Regulation	T_J = 25°C, I_O = 100 mA T_J = 25°C, I_O = 500 mA	(7.2≤V_{IN}≤25)		50 100	(14.5≤V_{IN}≤30)		120 240	(17.6≤V_{IN}≤30)		150 300	mV mV
ΔV_O	Load Regulation	T_J = 25°C, 5 mA $\le I_O \le$ 500 mA			100			240			300	mV
ΔV_O	Long Term Stability				20			48			60	mV/khrs
I_Q	Quiescent Current	T_J = 25°C		4	10		4	10		4	10	mA
ΔI_Q	Quiescent Current Change	T_J = 25°C 5 mA $\le I_O \le$ 500 mA			0.5			0.5			0.5	mA
		T_J = 25°C $V_{MIN} \le V_{IN} \le V_{MAX}$	(7.5≤V_{IN}≤25)		1	(14.8≤V_{IN}≤30)		1	(18≤V_{IN}≤30)		1	mA
V_n	Output Noise Voltage	T_J = 25°C, f = 10 Hz–100 kHz		40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz		78			71			69		dB
	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, I_O = 500 mA	7.2			14.5			17.6			V
	Thermal Resistance Junction to Case	P Package T Package		12 5			12 5			12 5		°C/W °C/W
	Thermal Resistance Junction to Ambient	P Package T Package		70 60			70 60			70 60		°C/W °C/W

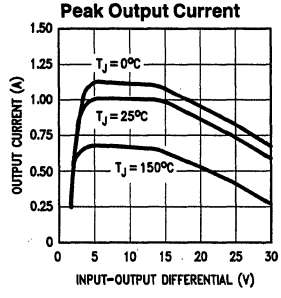
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Typical Performance Characteristics

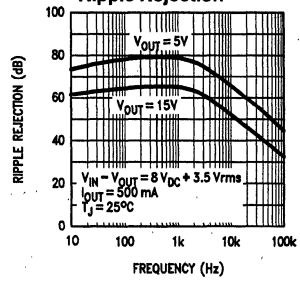
Maximum Average Power Dissipation



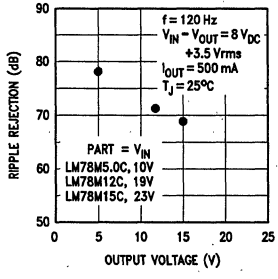
Peak Output Current



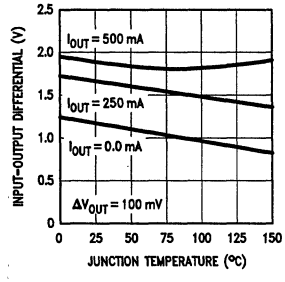
Ripple Rejection



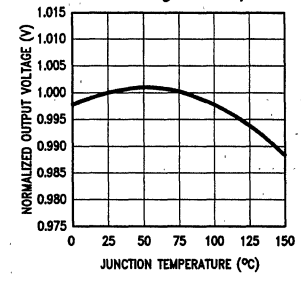
Ripple Rejection



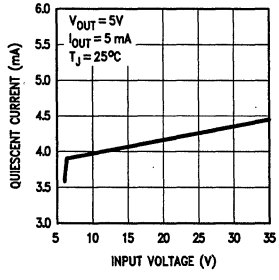
Dropout Voltage



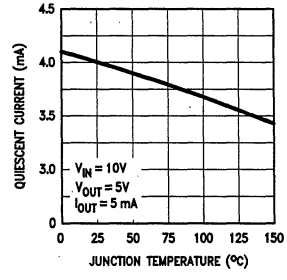
Output Voltage (Normalized to 1V at T_J = 25°C)



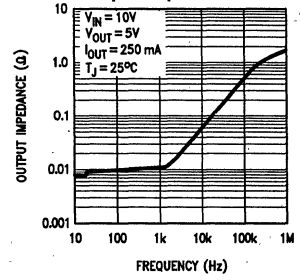
Quiescent Current



Quiescent Current



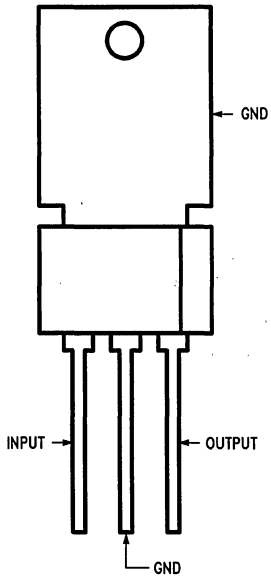
Output Impedance



TL/H/10484–4

Connection Diagrams

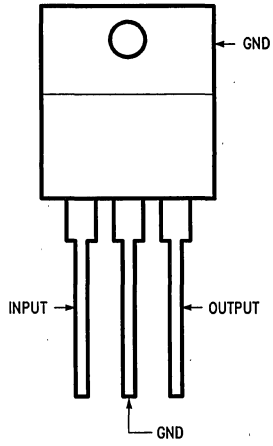
TO-202 (P)
Plastic Package



TL/H/10484–2

Order Numbers
LM341P-5.0
LM341P-12
LM341P-15
See NS Package Number P03A

TO-220 (T)
Plastic Package



TL/H/10484–3

Order Numbers
LM341T-5.0
LM341T-12
LM341T-15
See NS Package Number T03B

National Semiconductor

LM342 Series
3-Terminal Positive Regulators

General Description

The LM342-XX series of three-terminal regulators is available with several fixed output voltages, making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM342-XX series is available in the plastic TO-202 package. This package allows these regulators to deliver over 0.25A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over, preventing the IC from overheating.

Considerable effort was expended to make the LM342-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

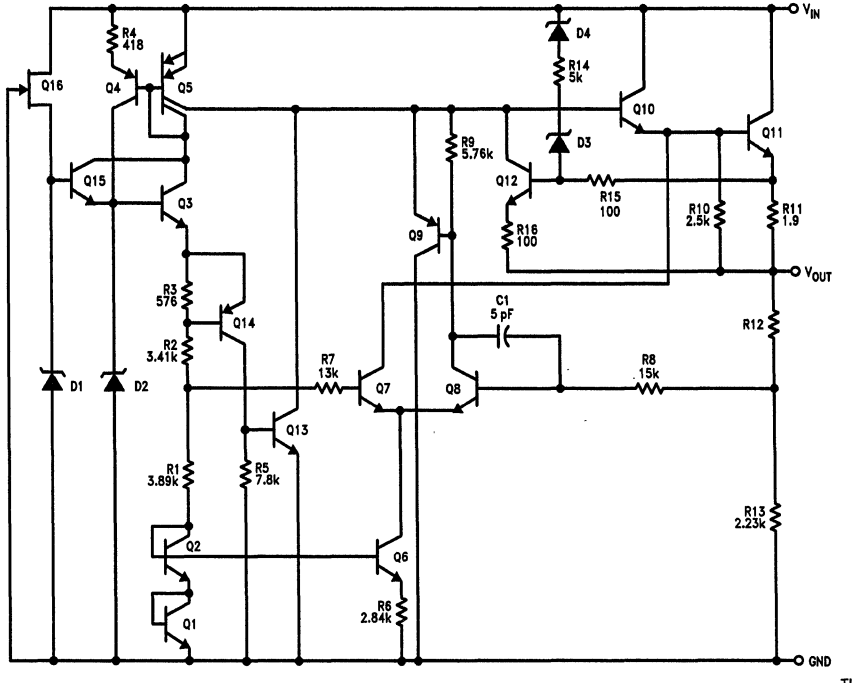
Features

- Output current in excess of 0.25A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-202 package
- Special circuitry allows start-up even if output is pulled to negative voltage (±supplies)

Voltage Range

LM342-5.0	5V
LM342-12	12V
LM342-15	15V

Schematic Diagram



TL/H/10485–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
V_O = 5V	30V
V_O = 12V and 15V	35V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Susceptibility	TBD

Electrical Characteristics T_A = 0°C to +70°C, I_O = 250 mA (Note 2) unless noted

Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
V_O	Output Voltage (Note 3)	T_J = 25°C	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		1 mA ≤ I_O ≤ 250 mA and V_{MIN} ≤ V_{IN} ≤ V_{MAX}	4.75 (7.5≤V_{IN}≤20)		5.25	11.4 (14.8≤V_{IN}≤27)		12.6	14.25 (18≤V_{IN}≤30)		15.75	V
ΔV_O	Line Regulation	T_J = 25°C, I_O = 250 mA			55 (7.3≤V_{IN}≤25)			100 (14.6≤V_{IN}≤30)			100 (17.7≤V_{IN}≤30)	mV
ΔV_O	Load Regulation	T_J = 25°C, 1 mA ≤ I_O ≤ 250 mA			50			120			150	mV
ΔV_O	Long Term Stability			20			48			60		mV/khrs
I_Q	Quiescent Current	T_J = 25°C			6			6			6	mA
ΔI_Q	Quiescent Current Change	T_J = 25°C, 1 mA ≤ I_O ≤ 250 mA			0.5			0.5			0.5	mA
		T_J = 25°C, V_{MIN} ≤ V_{IN} ≤ V_{MAX}			1.5 (7.3≤V_{IN}≤25)			1.5 (14.6≤V_{IN}≤30)			1.5 (17.7≤V_{IN}≤30)	mA
V_n	Output Noise Voltage	T_J = 25°C, f = 10 Hz–10 kHz		40			96			120		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	50	64		44	56		42	56		dB
	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, I_O = 250 mA	7.3			14.6			17.7			V
	Thermal Resistance Junction to Case	P Package		15			15			15		°C/W
	Thermal Resistance Junction to Ambient	P Package		80			80			80		°C/W

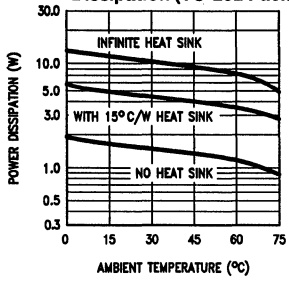
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The electrical characteristics data represent pulse test conditions with junction temperatures as shown at the initiation of tests.

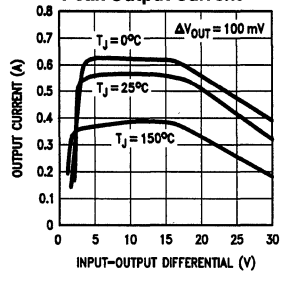
Note 3: The temperature coefficient of V_{OUT} is typically within 0.01% V_O/°C.

Typical Performance Characteristics

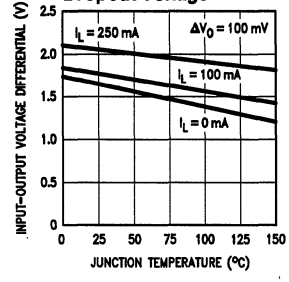
Maximum Average Power Dissipation (TO-202 Package)



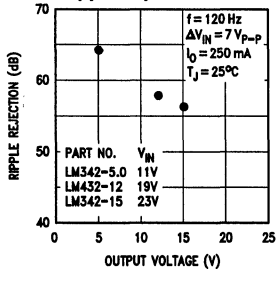
Peak Output Current



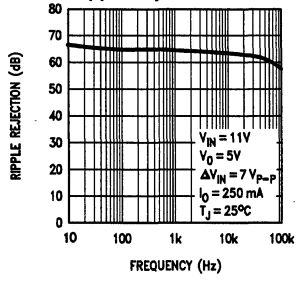
Dropout Voltage



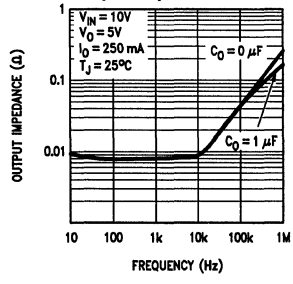
Ripple Rejection



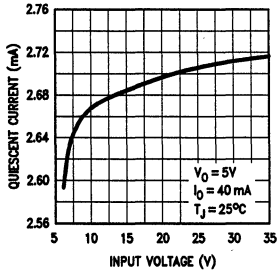
Ripple Rejection



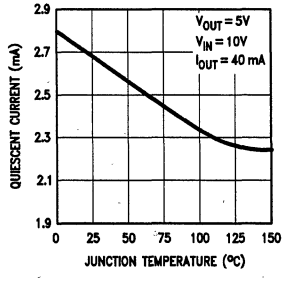
Output Impedance



Quiescent Current



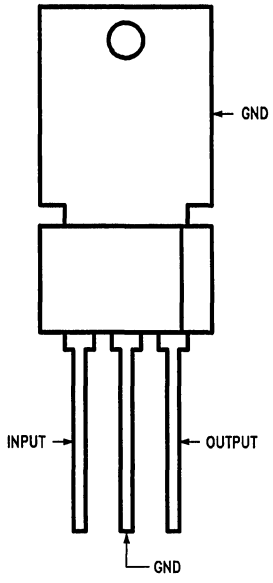
Quiescent Current



TL/H/10485–3

Connection Diagram

TO-202 (P) Plastic Package

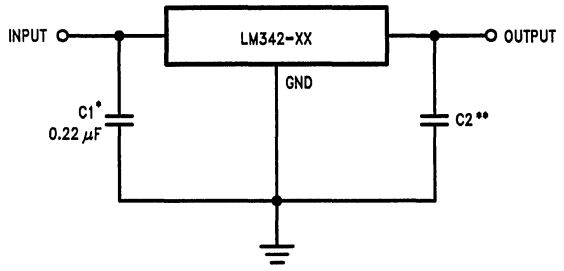


TL/H/10485–2

Order Number LM342P-5.0, LM342P-12 or LM342P-15
See NS Package Number P03A

Typical Applications

Fixed Output Regulator

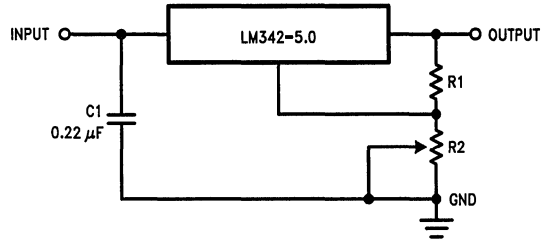


TL/H/10485–4

*Required if the regulator is located far from power supply filter

**Although not required, C2 does improve transient response. (If needed, use 0.1 μF ceramic disc.)

Adjustable Output Regulator

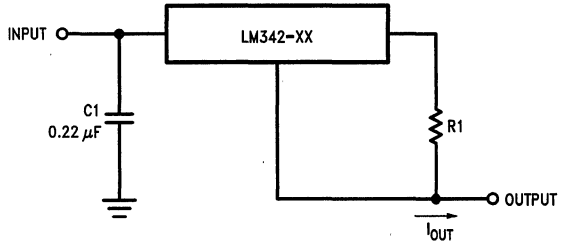


TL/H/10485–5

$V_O = 5V + (5V/R1 + I_Q) R2$

$5V/R1 > 3I_Q$, Load Regulation $(L_R) = [(R1 + R2)/R1] \times (L_r$ of LM342-05)

Current Regulator



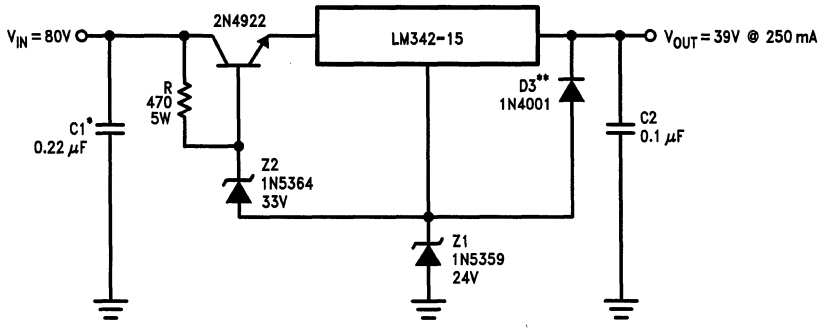
TL/H/10485–6

$I_{OUT} = V^{2-3}/R1 + I_Q$

$\Delta I_Q \leq 1.5$ mA over line and load changes

Typical Applications (Continued)

High Output Voltage Regulator

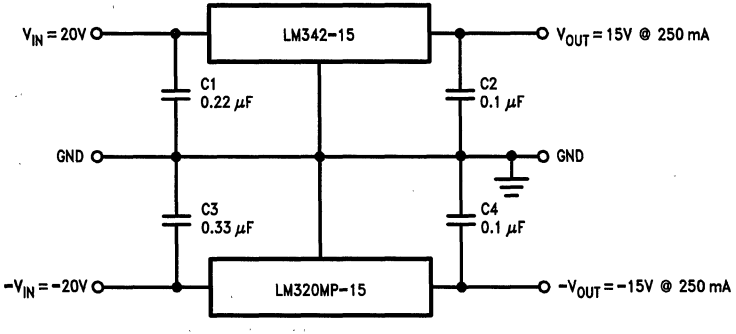


TL/H/10485–7

*Necessary if regulator is located far from the power supply filter

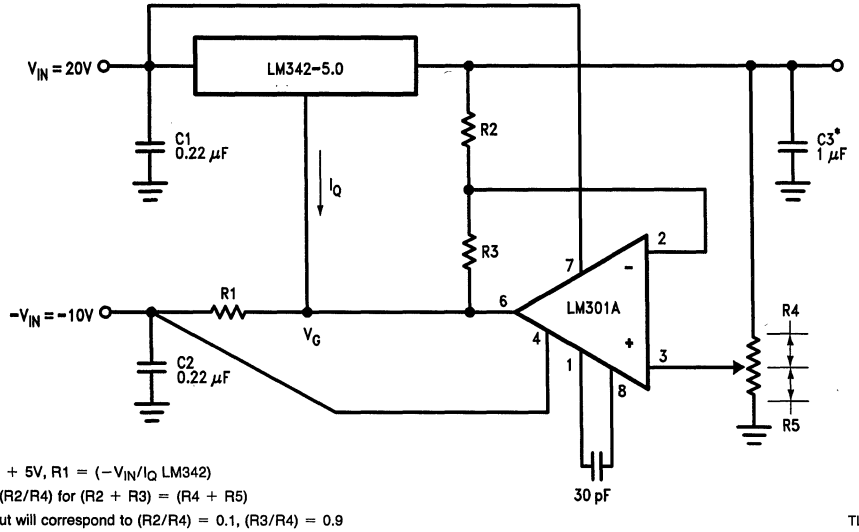
**D3 aids in full load start-up and protects the regulator during short circuits from high input to output voltage differentials

±15V, 250 mA Dual Power Supply



TL/H/10485–8

Variable Output Regulator 0.5V–18V



$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_Q$ LM342)

$V_{OUT} = 5V(R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1$, $(R3/R4) = 0.9$

*Solid tantalum

TL/H/10485–9

National Semiconductor

LM431A
Adjustable Precision Zener Shunt Regulator

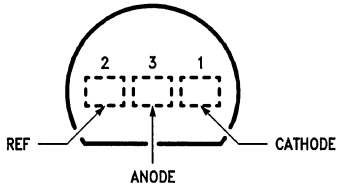
General Description

The LM431A is a 3-terminal adjustable shunt regulator with guaranteed temperature stability over the entire temperature range of operation. The output voltage may be set at any level greater than 2.5V (V_{REF}) up to 36V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.

Features

- Average temperature coefficient 50 ppm/°C
- Temperature compensated for operation over the full temperature range
- Programmable output voltage
- Fast turn-on response
- Low output noise

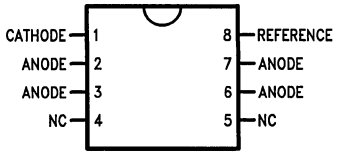
Connection Diagrams



TL/H/10055–1

Top View

Order Number LM431ACZ or LM431AIZ
See NS Package Number Z03A



TL/H/10055–2

Top View

Order Number LM431ACM
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial (LM431AI)	−40°C to +85°C
Commercial (LM431AC)	0°C to +70°C
Lead Temperature	
TO-92 Package/SO-8 Package (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1, 2)	
TO-92 Package	0.78W
SO-8 Package	0.81W
Cathode Voltage	37V
Continuous Cathode Current	−10 mA to +150 mA
Reference Voltage	−0.5V
Reference Input Current	10 mA

Operating Conditions	Min	Max
Cathode Voltage	V_{REF}	37V
Cathode Current	1.0 mA	100 mA

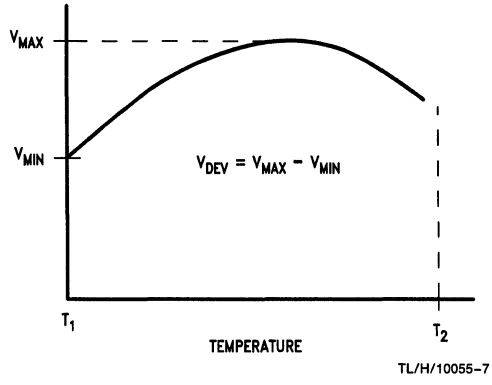
Note 1: $T_{J\ Max}$ = 150°C.

Note 2: Ratings appy to ambient temperature at 25°C. Above this temperature, derate the TO-92 at 6.2 mW/°C, and the SO-8 at 6.5 mW/°C.

LM431A
Electrical Characteristics T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, I_I = 10 mA *(Figure 1)*		2.440	2.495	2.550	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature (Note 3)	$V_Z = V_{REF}$, I_I = 10 mA, T_A = Full Range *(Figure 1)*			8.0	17	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	I_Z = 10 mA *(Figure 2)*	V_Z from V_{REF} to 10V		−1.4	−2.7	mV/V
			V_Z from 10V to 36V		−1.0	−2.0	
I_{REF}	Reference Input Current	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA *(Figure 2)*			2.0	4.0	μA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	R_1 = 10 kΩ, R_2 = ∞, I_I = 10 mA, T_A = Full Range *(Figure 2)*			0.4	1.2	μA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$ *(Figure 1)*			0.4	1.0	mA
$I_{Z(OFF)}$	Off-State Current	V_Z = 36V, V_{REF} = 0V *(Figure 3)*			0.3	1.0	μA
r_Z	Dynamic Output Impedance (Note 4)	$V_Z = V_{REF}$, Frequency = 0 Hz *(Figure 1)*				0.75	Ω

Note 3: Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.



TL/H/10055–7

The average temperature coefficient of the reference input voltage, $\propto V_{REF}$, is defined as:

$$\propto V_{REF}\ \frac{ppm}{°C} = \frac{\pm\left[\frac{V_{Max} - V_{Min}}{V_{REF\ (at\ 25°C)}}\right]10^6}{T_2 - T_1} = \frac{\pm\left[\frac{V_{DEV}}{V_{REF\ (at\ 25°C)}}\right]10^6}{T_2 - T_1}$$

Where:

$T_2 - T_1$ = full temperature change.

$\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.

Example: V_{DEV} = 8.0 mV, V_{REF} = 2495 mV, $T_2 - T_1$ = 70°C, slope is positive.

$$\propto V_{REF} = \frac{\left[\frac{8.0\ mV}{2495\ mV}\right]10^6}{70°C} = +46\ ppm/°C$$

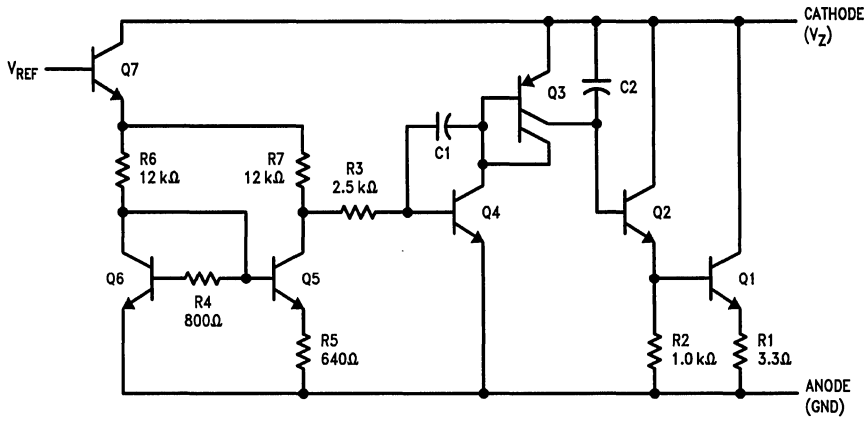
Note 4: The dynamic output impedance, r_Z, is defined as:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (see *Figure 2*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

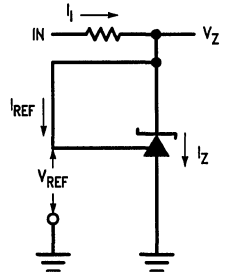
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\ 1 + \frac{R1}{R2}\right]$$

Equivalent Circuit



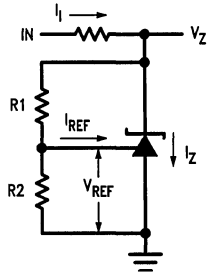
TL/H/10055–3

DC Test Circuits



TL/H/10055–4

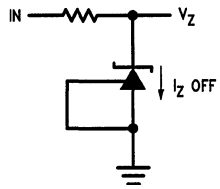
FIGURE 1. Test Circuit for $V_Z = V_{REF}$



TL/H/10055–5

Note: $V_Z = V_{REF}(1 + R1/R2) + I_{REF} \bullet R1$

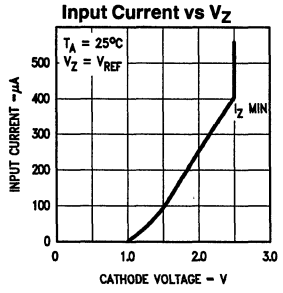
FIGURE 2. Test Circuit for $V_Z > V_{REF}$

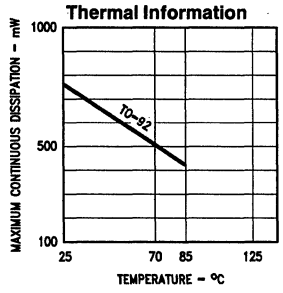


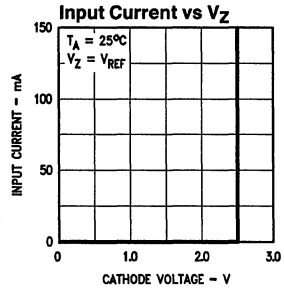
TL/H/10055–6

FIGURE 3. Test Circuit for Off-State Current

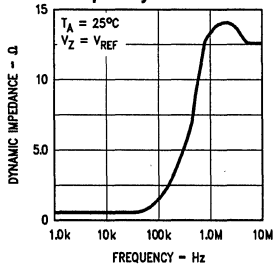
Typical Performance Characteristics



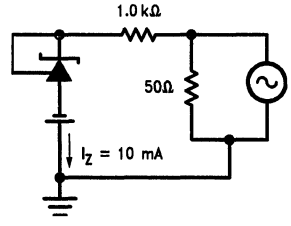




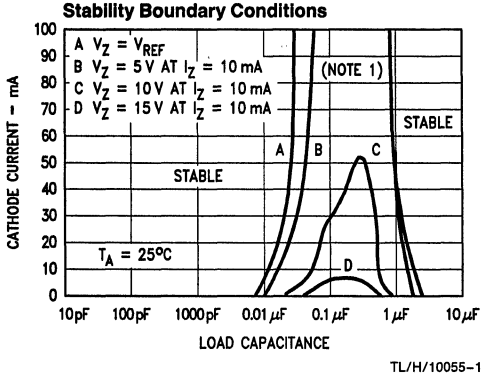
TL/H/10055–8



TL/H/10055–9



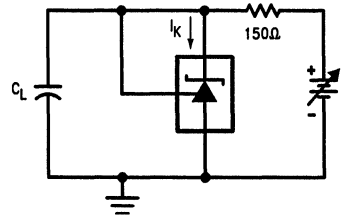
TL/H/10055–10



TL/H/10055–11

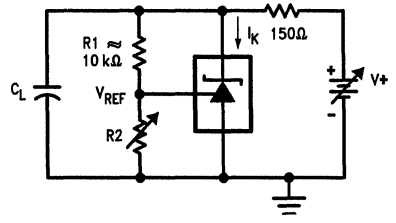
Note 1: The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_Z and I_Z conditions with C_L = 0. V+ and C_L were then adjusted to determine the ranges of stability.

Test Circuit for Curve A Above



TL/H/10055–12

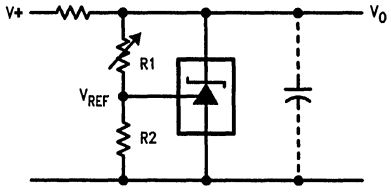
Test Circuit for Curves B, C and D Above



TL/H/10055–13

Typical Applications

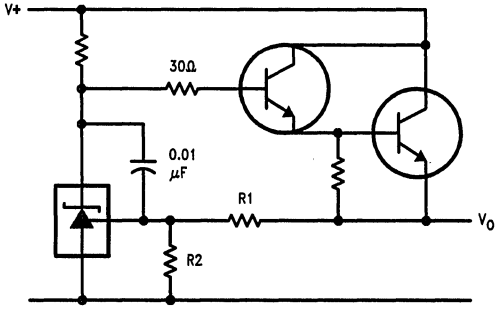
Shunt Regulator



TL/H/10055–14

$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

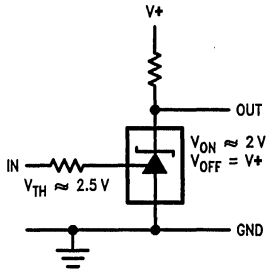
Series Regulator



TL/H/10055–16

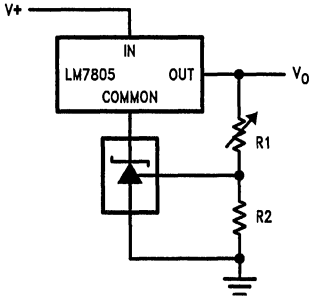
$$V_O \approx \left(1 + \frac{R1}{R2}\right) V_{REF}$$

Single Supply Comparator with Temperature Compensated Threshold



TL/H/10055–15

Output Control of a Three Terminal Fixed Regulator



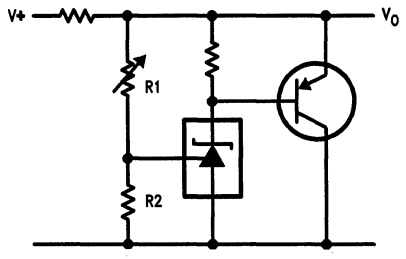
TL/H/10055–17

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{REF}$$

$$V_{O\,MIN} = V_{REF} + 5V$$

Typical Applications (Continued)

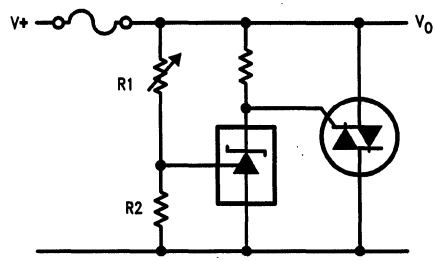
Higher Current Shunt Regulator



TL/H/10055–18

$$V_O = \left(1 + \frac{R1}{R2}\right)V_{REF}$$

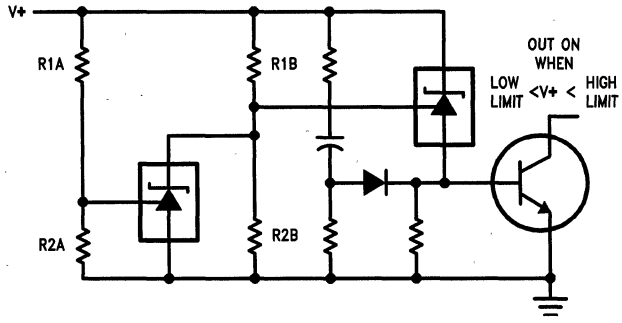
Crow Bar



TL/H/10055–19

$$V_{LIMIT} \approx \left(1 + \frac{R1}{R2}\right)V_{REF}$$

Over Voltage/Under Voltage Protection Circuit

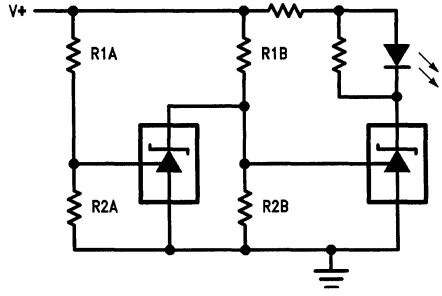


TL/H/10055–20

$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right) + V_{BE}$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

Voltage Monitor



TL/H/10055–21

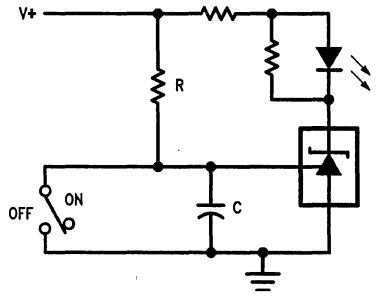
$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right)$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

LED ON WHEN
LOW LIMIT < V^+ < HIGH LIMIT

Typical Applications (Continued)

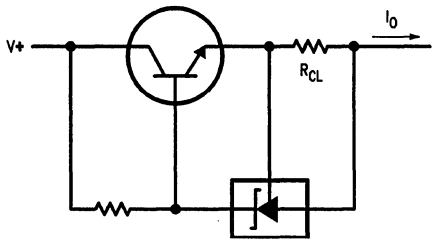
Delay Timer



TL/H/10055–22

$$\text{DELAY} = R \bullet C \bullet \ell n \frac{V+}{(V^+) - V_{REF}}$$

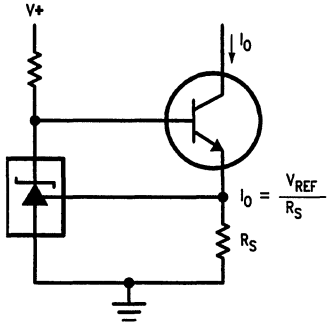
Current Limiter or Current Source



TL/H/10055–23

$$I_O = \frac{V_{REF}}{R_{CL}}$$

Constant Current Sink



TL/H/10055–24

National Semiconductor

LM723/LM723C Voltage Regulator

General Description

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

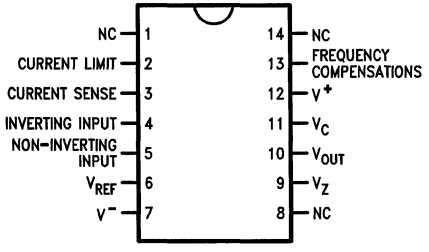
The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

Connection Diagrams

Dual-In-Line Package

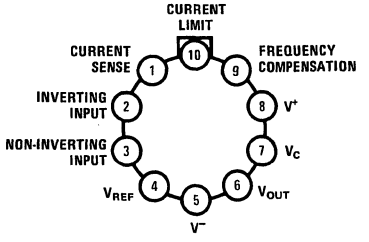


TL/H/8563–2

Top View

Order Number LM723J, LM723CJ, LM723CM or LM723CN
See NS Package J14A, M14A or N14A

Metal Can Package



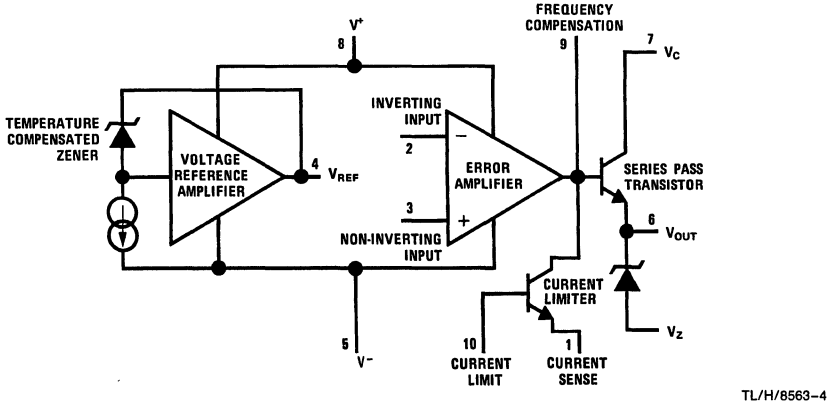
TL/H/8563–3

Note: Pin 5 connected to case.

Top View

Order Number LM723H or LM723CH
See NS Package H10C

Equivalent Circuit*



TL/H/8563–4

*Pin numbers refer to metal can package.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	8.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA

Internal Power Dissipation Metal Can (Note 1)	800 mW
Cavity DIP (Note 1)	900 mW
Molded DIP (Note 1)	660 mW
Operating Temperature Range LM723	−55°C to +150°C
LM723C	0°C to +70°C
Storage Temperature Range Metal Can	−65°C to +150°C
Molded DIP	−55°C to +150°C
Lead Temperature (Soldering, 4 sec. max.)	
Hermetic Package	300°C
Plastic Package	260°C
ESD Tolerance (Human body model, 1.5 kΩ in series with 100 pF)	1200V

Electrical Characteristics (Note 2)

Parameter	Conditions	LM723			LM723C			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1		0.01	0.1	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.3				% V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.3	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2		0.1	0.5	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15		0.03	0.2	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.6				% V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Average Temperature Coefficient of Output Voltage (Note 8)	−55°C ≤ T_A ≤ +125°C		0.002	0.015				%/°C
	0°C ≤ T_A ≤ +70°C					0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		86			86		μVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μVrms
Long Term Stability			0.05			0.05		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.7	3.5		1.7	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V
θ_{JA}	Molded DIP		105			105		°C/W
θ_{JA}	Cavity DIP		150			150		°C/W
θ_{JA}	H10C Board Mount in Still Air		165			165		°C/W
θ_{JA}	H10C Board Mount in 400 LF/Min Air Flow		66			66		°C/W
θ_{JA}	SO					125		°C/W
θ_{JC}			22			22		°C/W

Note 1: See derating curves for maximum power rating above 25°C.

Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in *Figure 1.* Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

Note 5: Replace R1/R2 in figures with divider shown in *Figure 13.*

Note 6: V^+ and V_{CC} must be connected to a +3V or greater supply.

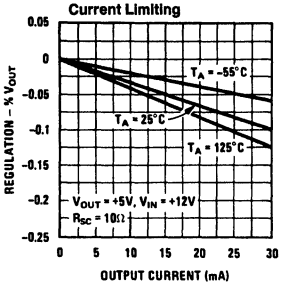
Note 7: For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT}.

Note 8: Guaranteed by correlation to other tests.

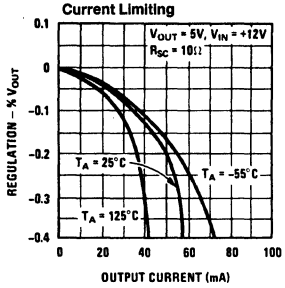
Note 9: Refer to RETS723X military specifications for the LM723.

Typical Performance Characteristics

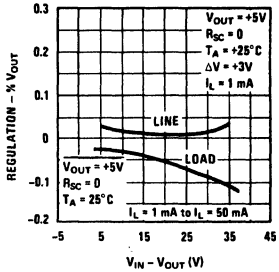
Load Regulation Characteristics with Current Limiting



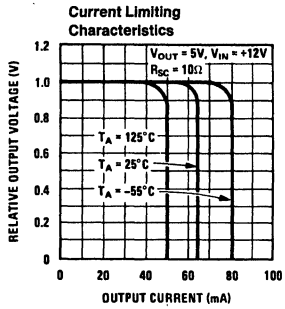
Load Regulation Characteristics with Current Limiting



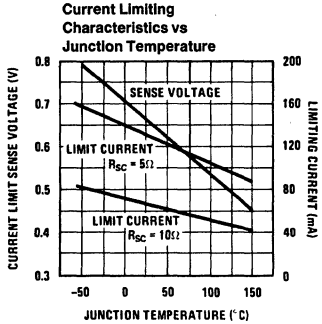
Load & Line Regulation vs Input-Output Voltage Differential



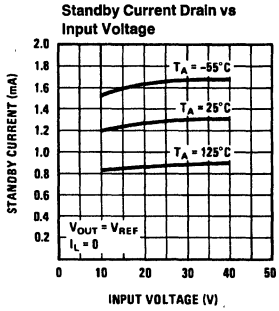
Current Limiting Characteristics



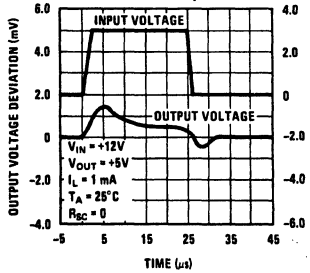
Current Limiting Characteristics vs Junction Temperature



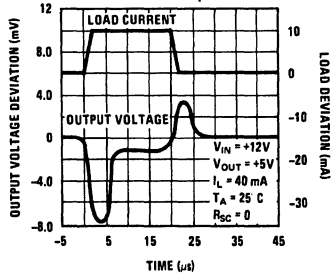
Standby Current Drain vs Input Voltage



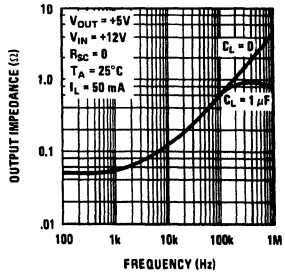
Line Transient Response



Load Transient Response



Output Impedence vs Frequency



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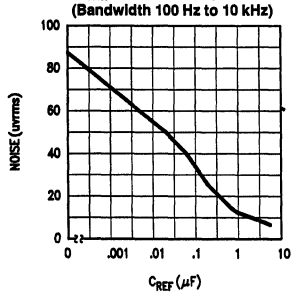
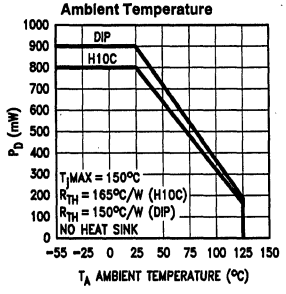
Maximum Power Ratings

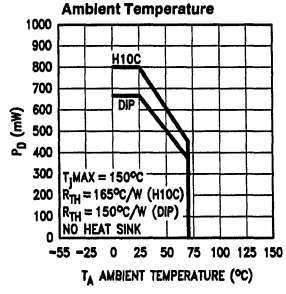
Noise vs Filter Capacitor (C_{REF} in Circuit of *Figure 1*) (Bandwidth 100 Hz to 10 kHz)



LM723 Power Dissipation vs Ambient Temperature



LM723C Power Dissipation vs Ambient Temperature



TL/H/8563–7

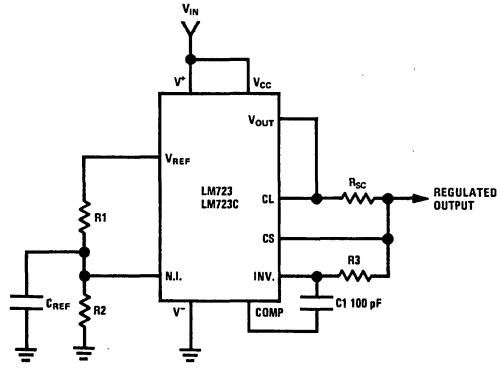
TABLE I. Resistor Values (kΩ) for Standard Output Voltage

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 4)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts (*Figures 1, 5, 6, 9, 12, [4]*) $V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2}\right)$	**Outputs from +4 to +250 volts** (*Figure 7*) $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right)$; R3 = R4	**Current Limiting** $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts (*Figures 2, 4, [5, 6, 9, 12]*) $V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2}\right)$	**Outputs from −6 to −250 volts** (*Figures 3, 8, 10*) $V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right)$; R3 = R4	**Foldback Current Limiting** $I_{KNEE} = \left(\frac{V_{OUT}\,R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right)$ $I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right)$

Typical Applications



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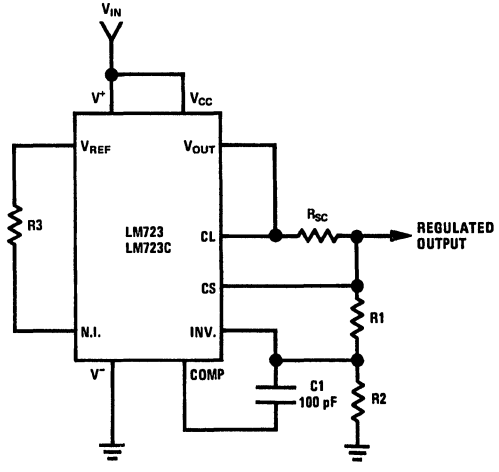
Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift.

Typical Performance

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 1. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)



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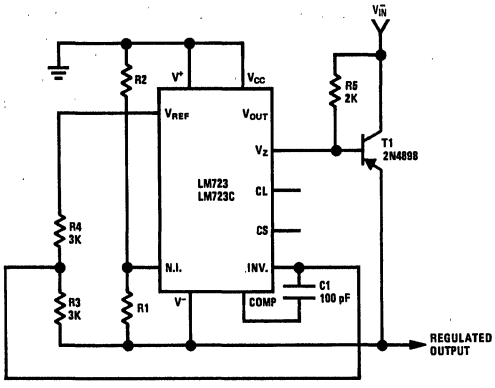
Note: $R3 = \frac{R1\,R2}{R1 + R2}$ for minimum temperature drift. R3 may be eliminated for minimum component count.

Typical Performance

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

FIGURE 2. Basic High Voltage Regulator (V_{OUT} = 7 to 37 Volts)

Typical Applications (Continued)



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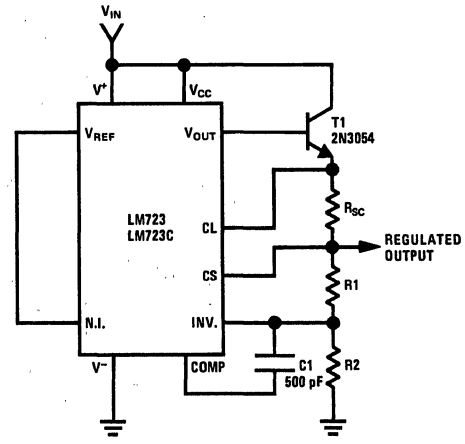
Typical Performance

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

FIGURE 3. Negative Voltage Regulator

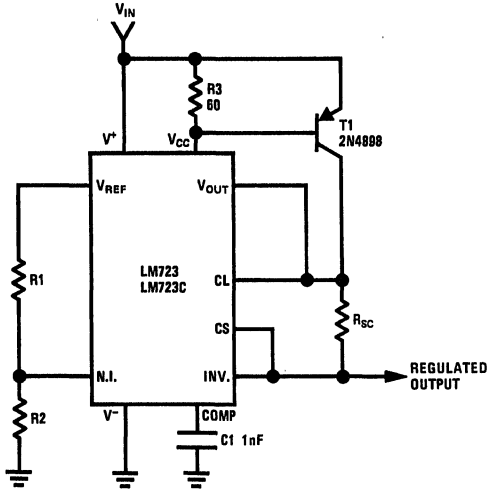


TL/H/8563–11

Typical Performance

Regulated Output Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

FIGURE 4. Positive Voltage Regulator (External NPN Pass Transistor)

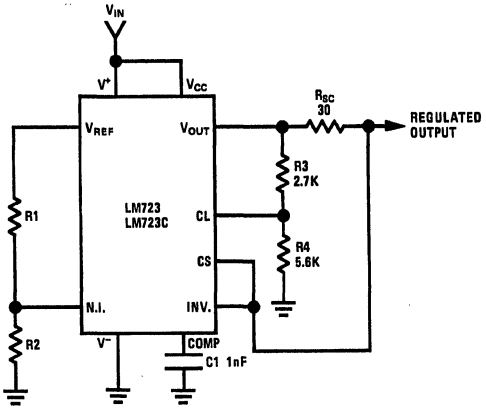


TL/H/8563–12

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

FIGURE 5. Positive Voltage Regulator (External PNP Pass Transistor)



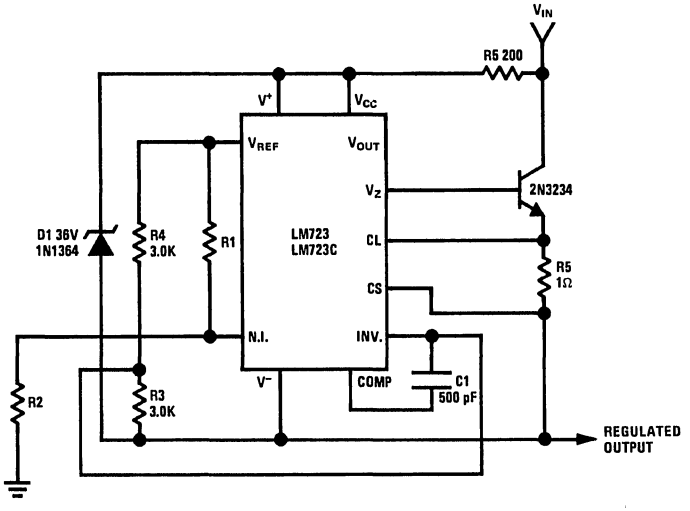
TL/H/8563–13

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

FIGURE 6. Foldback Current Limiting

Typical Applications (Continued)

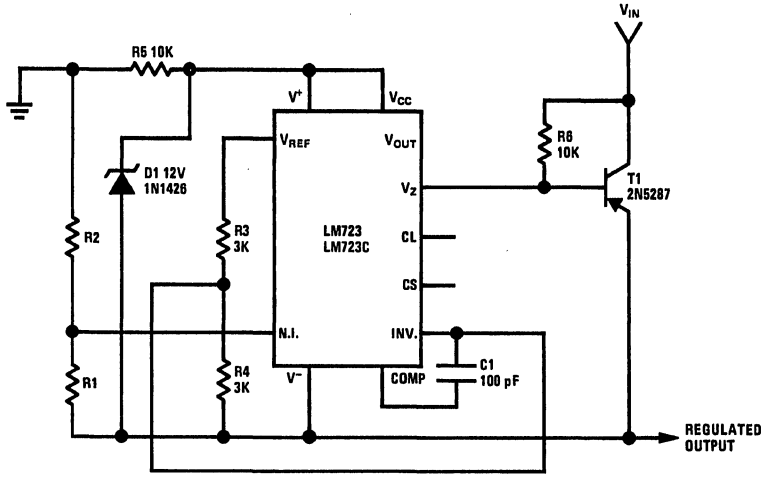


TL/H/8563–14

Typical Performance

Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

FIGURE 7. Positive Floating Regulator



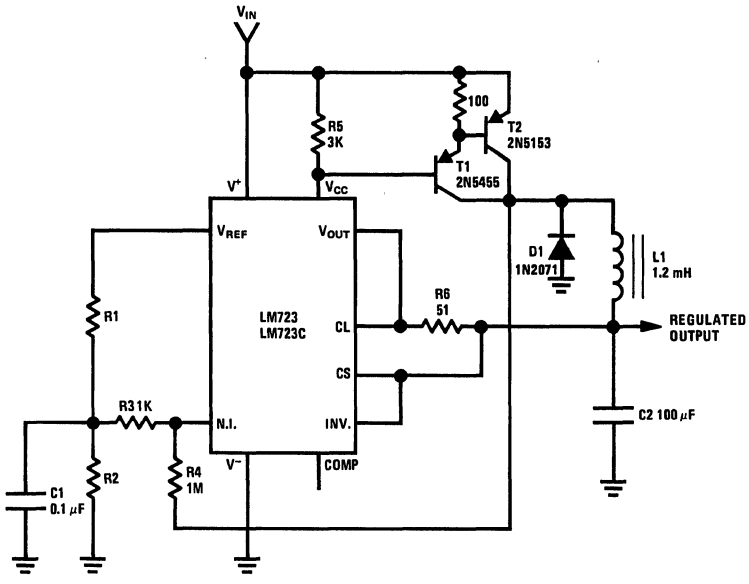
TL/H/8563–15

Typical Performance

Regulated Output Voltage	−100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

FIGURE 8. Negative Floating Regulator

Typical Applications (Continued)

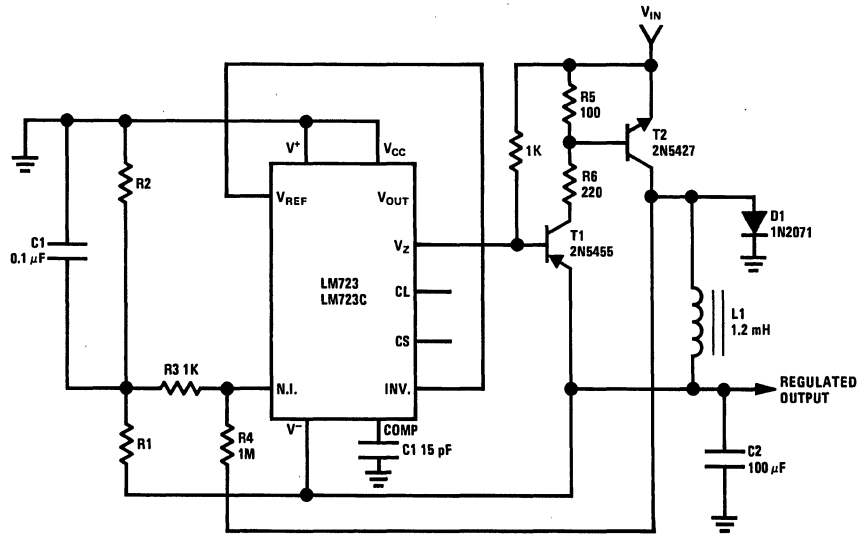


TL/H/8563–16

Typical Performance

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

FIGURE 9. Positive Switching Regulator



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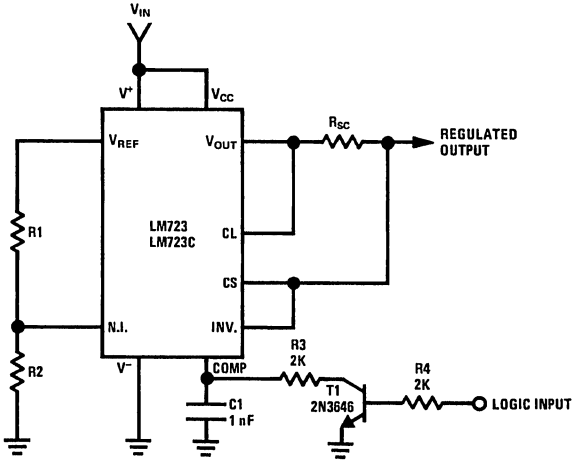
Typical Performance

Regulated Output Voltage	−15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

FIGURE 10. Negative Switching Regulator

Typical Applications (Continued)



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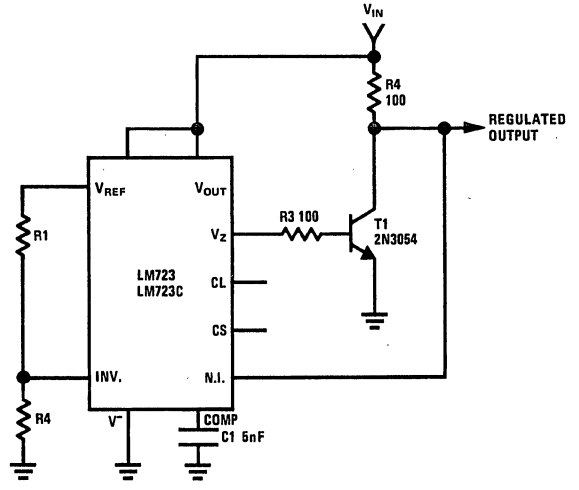
Note: Current limit transistor may be used for shutdown if current limiting is not required.

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 11. Remote Shutdown Regulator with Current Limiting



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Typical Performance	
Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

FIGURE 12. Shunt Regulator

Typical Applications (Continued)

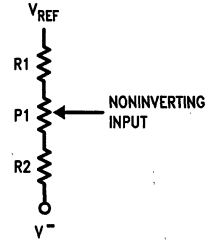

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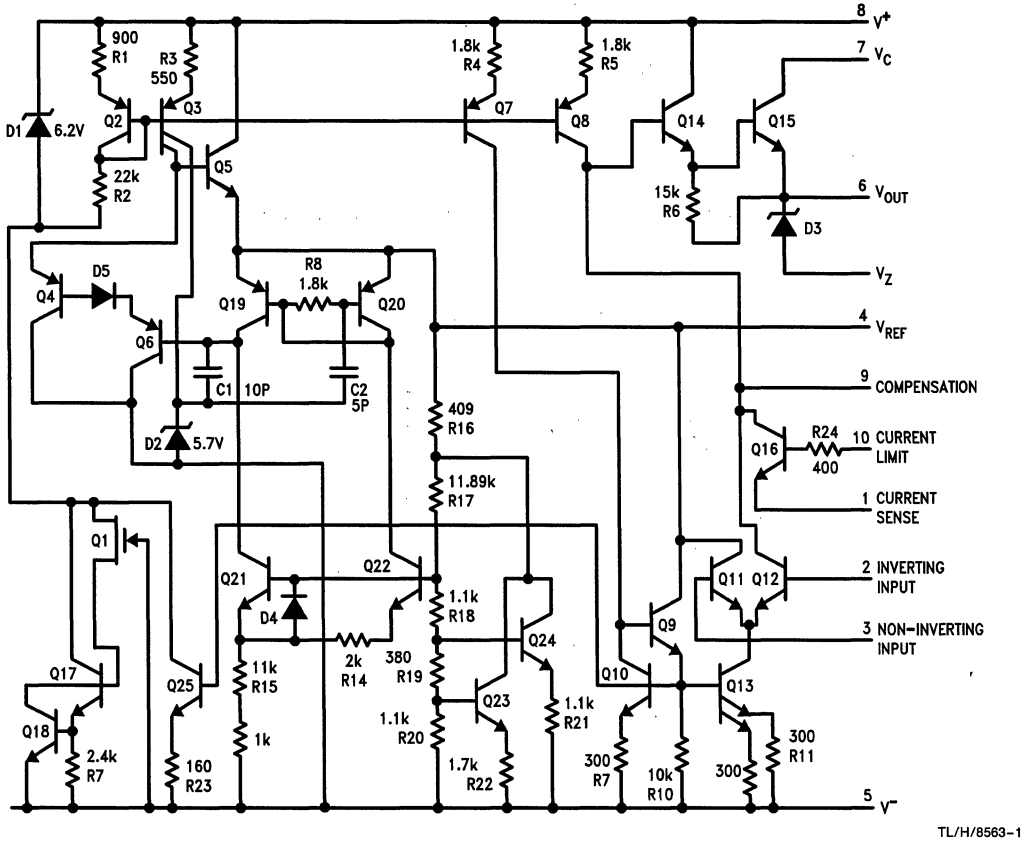
FIGURE 13. Output Voltage Adjust (See Note 5)

Schematic Diagram



TL/H/8563–1

National Semiconductor

LM2925 Low Dropout Regulator with Delayed Reset

General Description

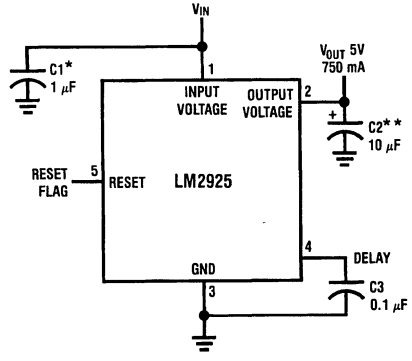
The LM2925 features a low dropout, high current regulator. Also included on-chip is a reset function with an externally set delay time. Upon power up, or after the detection of any error in the regulated output, the reset pin remains in the active low state for the duration of the delay. Types of errors detected include any that cause the output to become unregulated: low input voltage, thermal shutdown, short circuit, input transients, etc. No external pull-up resistor is necessary. The current charging the delay capacitor is very low, allowing long delay times.

Designed primarily for automotive applications, the LM2925 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load. The LM2925 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- 5V, 750 mA output
- Externally set delay for reset
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- Long delay times available
- 100% electrical burn-in in thermal limit

Typical Application Circuit



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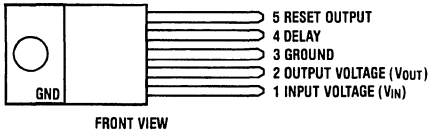
*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



FRONT VIEW

TL/H/5268–2

Order Number LM2925T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to + 125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD rating is to be determined	

Electrical Characteristics for V_{OUT}

V_{IN} = 14V, C2 = 10 µf, I_O = 500 mA, T_J = 25°C (Note 3) (unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
			Note 2		
Output Voltage	6V ≤ V_{IN} ≤ 26V, I_O ≤ 500 mA, −40°C ≤ T_J ≤ +125°C	4.75	5.00	5.25	V
Line Regulation	9V ≤ V_{IN} ≤ 16V, I_O = 5 mA 6V ≤ V_{IN} ≤ 26V, I_O = 5 mA		4 10	25 50	mV mV
Load Regulation	5 mA ≤ I_O ≤ 500 mA		10	50	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O ≤ 10 mA I_O = 500 mA I_O = 750 mA		3 40 90	 100 	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		µVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz		66		dB
Dropout Voltage	I_O = 500 mA I_O = 750 mA		0.45 0.82	0.6 	V V
Current Limit		0.75	1.2		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	V_O ≤ 5.5V	60	70		V
Reverse Polarity Input Voltage, DC	V_O ≥ − 0.6V, 10Ω Load	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ ≤ 100 ms, 10Ω Load	−50	−80		V

Electrical Characteristics for Reset Output

V_{IN} = 14V, C3 = 0.1 µF, T_A = 25°C (Note 3) (unless otherwise specified)

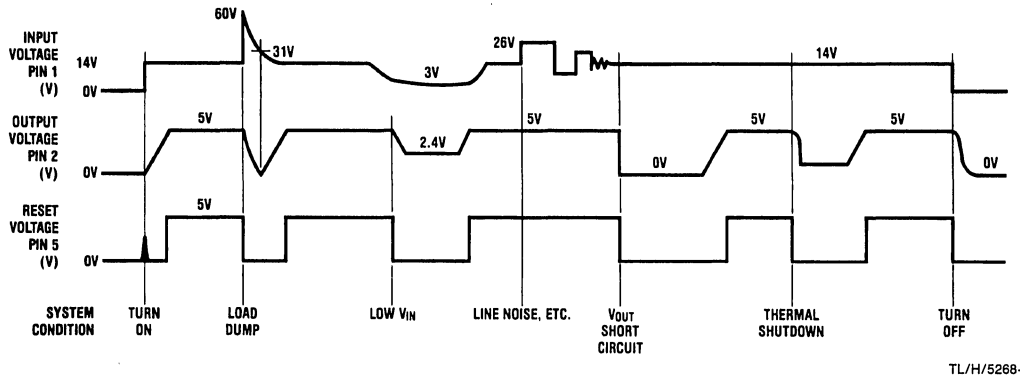
Parameter	Conditions	Min	Typ	Max	Units
			Note 2		
Reset Voltage Output Low Output High	 I_{SINK} = 1.6 mA, V_{IN} = 35V I_{SOURCE} = 0	 4.5	 0.3 5.0	 0.6 5.5	 V V
Reset Internal Pull-up Resistor			30		kΩ
Reset Output Current Limit	V_{RESET} = 1.2 V		5		mA
V_{OUT} Threshold			4.5		V
Delay Time	C_3 = .005 µF C_3 = 0.1 µF C_3 = 4.7 µF tantalum	 150 	12 250 12	 300 	ms ms s
Delay Current	Pin 4	1.2	1.95	2.5	µA

Note 1: Thermal resistance without a heat sink for junction to case temperature is 3°C/W (TO-220). Thermal resistance for TO-220 case to ambient temperature is 50°C/W.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Circuit Waveforms

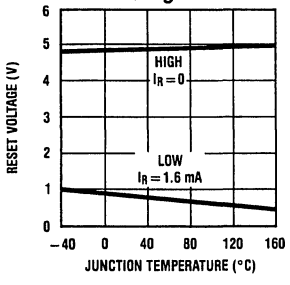


TL/H/5268-3

FIGURE 2

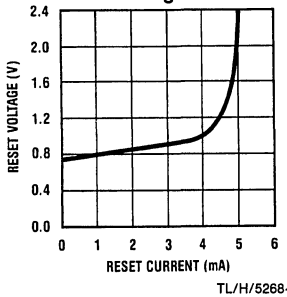
Typical Performance Characteristics

Reset Voltage



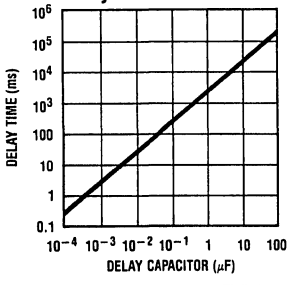
TL/H/5268-4

Reset Voltage



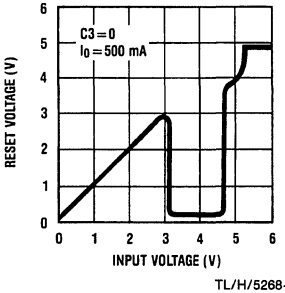
TL/H/5268-5

Delay Time



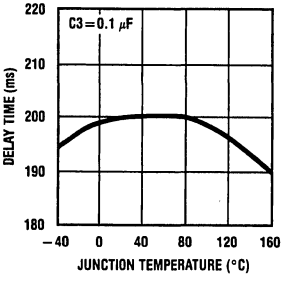
TL/H/5268-6

Reset Voltage on Power-up



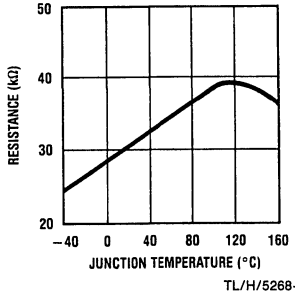
TL/H/5268-7

Delay Time



TL/H/5268-8

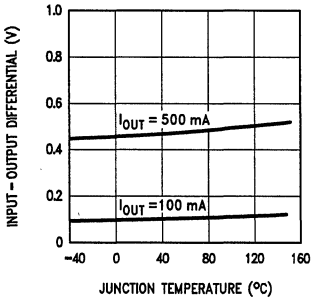
Reset Pull-up Resistor R10



TL/H/5268-9

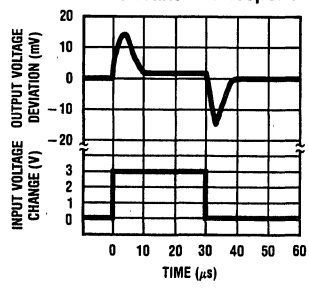
Typical Performance Characteristics (Continued)

Dropout Voltage



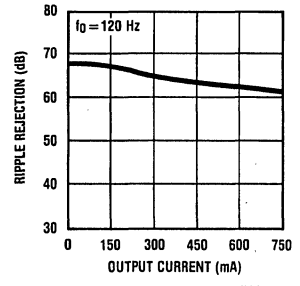
TL/H/5268–10

Line Transient Response



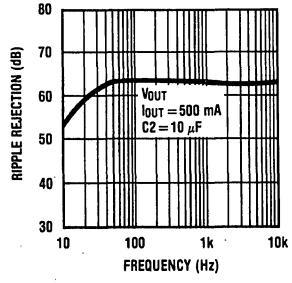
TL/H/5268–11

Ripple Rejection



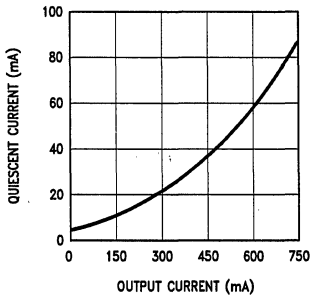
TL/H/5268–12

Ripple Rejection



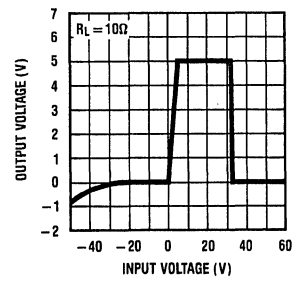
TL/H/5268–13

Quiescent Current



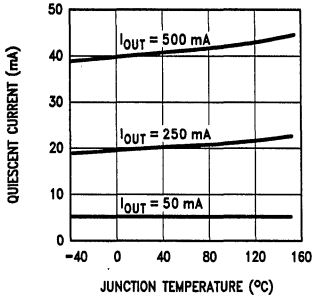
TL/H/5268–14

Output Voltage



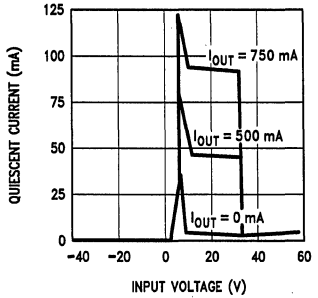
TL/H/5268–15

Quiescent Current



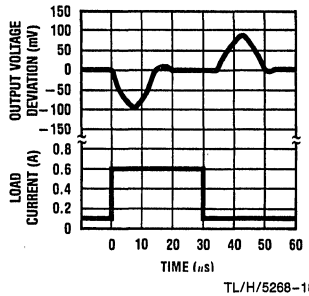
TL/H/5268–19

Quiescent Current



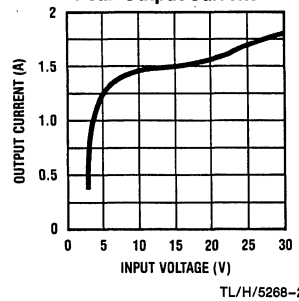
TL/H/5268–17

Load Transient Response



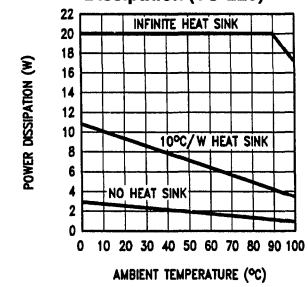
TL/H/5268–18

Peak Output Current



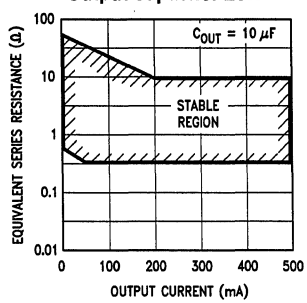
TL/H/5268–20

Maximum Power Dissipation (TO-220)



TL/H/5268–21

Output Capacitor ESR



TL/H/5268–22

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in ouput voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

EXTERNAL CAPACITORS

The LM2925 output capacitor is required for stability. Without it, the regulator output will oscillate, sometimes by many volts. Though the 10 μF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also effects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum junction and ambient temperature and maximum load expected.

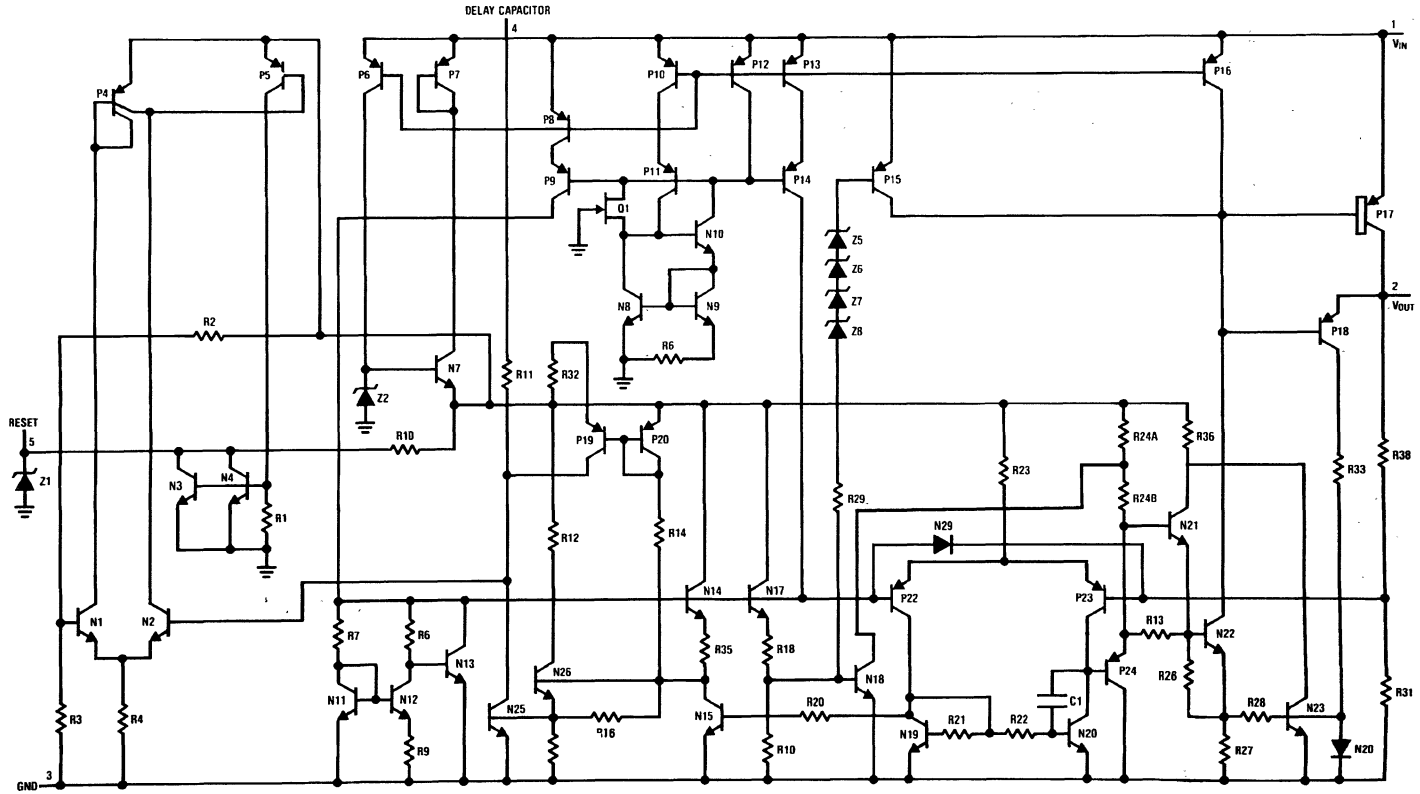
Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

RESET OUTPUT

The range of values for the delay capacitor is limited only by stray capacitances on the lower extreme and capacitance leakage on the other. Thus, delay times from microseconds to seconds are possible. The low charging current, typically 2.0 microamps, allows the use of small, inexpensive disc capacitors for the nominal range of 100 to 500 milliseconds. This is the time required in many microprocessor systems for the clock oscillator to stabilize when initially powered up. The RESET output of the regulator will thus prevent erroneous data and/or timing functions to occur during this part of operation. The same delay is incorporated after any other fault condition in the regulator output is corrected.

Circuit Schematic



TL/H/5268–23

FIGURE 3

National Semiconductor

LM2930 3-Terminal Positive Regulator

General Description

The LM2930 3-terminal positive regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Efficient use of low input voltages obtained, for example, from an automotive battery during cold crank conditions, allows 5V circuitry to be properly powered with supply voltages as low as 5.6V. Familiar regulator features such as current limit and thermal overload protection are also provided.

Designed originally for automotive applications, the LM2930 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (40V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2930 cannot be harmed by temporary mirror-image insertion.

Fixed outputs of 5V and 8V are available in the plastic TO-220 power package.

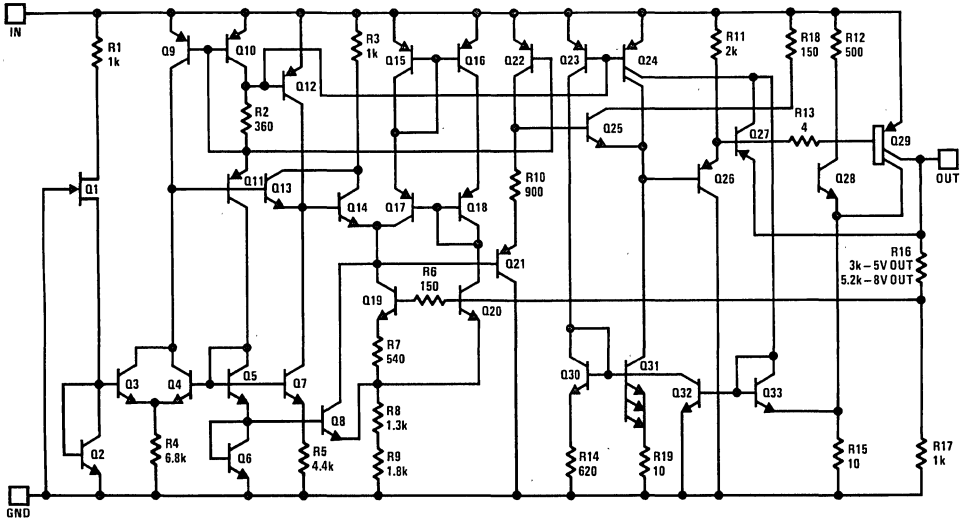
Features

- Input-output differential less than 0.6V
- Output current in excess of 150 mA
- Reverse battery protection
- 40V load dump protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in thermal limit

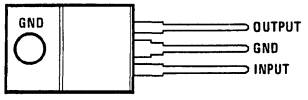
Voltage Range

LM2930T-5.0	5V
LM2930T-8.0	8V

Schematic and Connection Diagrams



(TO-220)
Plastic Package



FRONT VIEW

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Order Number LM2930T-5.0 or LM2930T-8.0
See NS Package T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	40V
Reverse Voltage (100 ms)	−12V
Reverse Voltage (DC)	−6V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics (Note 2)

LM2930T-5.0 $V_{IN}=14V$, $I_O=150$ mA, $T_j=25°C$ (Note 5), C2 = 10 μF, unless otherwise specified

Parameter	Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit
Output Voltage		5	5.3 4.7		V_{MAX} V_{MIN}
	$6V \le V_{IN} \le 26V$, 5 mA ≤ I_O ≤ 150 mA $-40°C \le T_J \le 125°C$			5.5 4.5	V_{MAX} V_{MIN}
Line Regulation	$9V \le V_{IN} \le 16V$, $I_O=5$ mA $6V \le V_{IN} \le 26V$, $I_O=5$ mA	7 30	25 80		mV_{MAX} mV_{MAX}
Load Regulation	5 mA ≤ I_O ≤ 150 mA	14	50		mV_{MAX}
Output Impedance	100 mA_{DC} & 10 mA_{rms}, 100 Hz−10 kHz	200			mΩ
Quiescent Current	$I_O=10$ mA $I_O=150$ mA	4 18	7 40		mA_{MAX} mA_{MAX}
Output Noise Voltage	10 Hz−100 kHz	140			μV_{rms}
Long Term Stability		20			mV/1000 hr
Ripple Rejection	$f_O=120$ Hz	56			dB
Current Limit		400	700 150		mA_{MAX} mA_{MIN}
Dropout Voltage	$I_O=150$ mA	0.32	0.6		V_{MAX}
Output Voltage Under Transient Conditions	$-12V \le V_{IN} \le 40V$, $R_L=100\Omega$		5.5 −0.3		V_{MAX} V_{MIN}

Electrical Characteristics (Note 2)

LM2930T-8.0 ($V_{IN}=14V$, $I_O=150$ mA, $T_j=25°C$ (Note 5), C2 = 10 μF, unless otherwise specified)

Parameter	Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit
Output Voltage		8	8.5 7.5		V_{MAX} V_{MIN}
	$9.4V \le V_{IN} \le 26V$, 5 mA ≤ I_O ≤ 150 mA, $-40°C \le T_J \le 125°C$			8.8 7.2	V_{MAX} V_{MIN}
Line Regulation	$9.4V \le V_{IN} \le 16V$, $I_O=5$ mA $9.4V \le V_{IN} \le 26V$, $I_O=5$ mA	12 50	50 100		mV_{MAX} mV_{MAX}
Load Regulation	5 mA ≤ I_O ≤ 150 mA	25	50		mV_{MAX}
Output Impedance	100 mA_{DC} & 10 mA_{rms}, 100 Hz−10 kHz	300			mΩ
Quiescent Current	$I_O=10$ mA $I_O=150$ mA	4 18	7 40		mA_{MAX} mA_{MAX}
Output Noise Voltage	10 Hz−100 kHz	170			μV_{rms}
Long Term Stability		30			mV/1000 hr
Ripple Rejection	$f_O=120$ Hz	52			dB
Current Limit		400	700 150		mA_{MAX} mA_{MIN}
Dropout Voltage	$I_O=150$ mA	0.32	0.6		V_{MAX}
Output Voltage Under Transient Conditions	$-12V \le V_{IN} \le 40V$, $R_L=100\Omega$		8.8 −0.3		V_{MAX} V_{MIN}

Note 1: Thermal resistance without a heat sink for junction to case temperature is 3°C/W and for case to ambient temperature is 50°C/W.

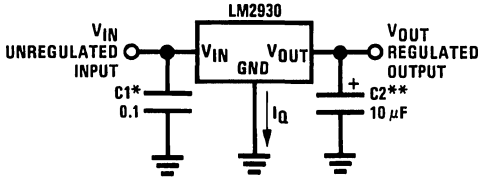
Note 2: All characteristics are measured with a capacitor across the input of 0.1 μF and a capacitor across the output of 10 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

Note 5: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Application



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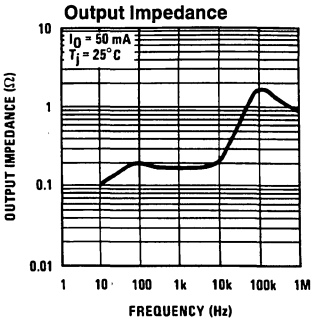
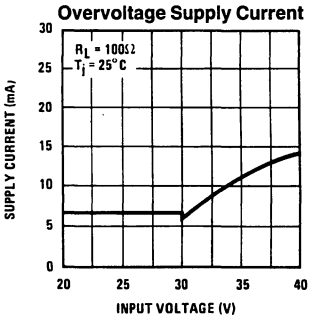
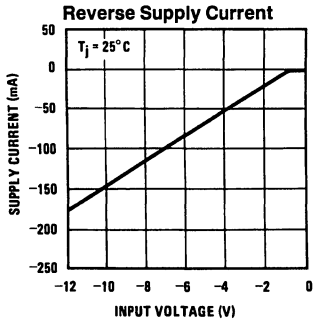
*Required if regulator is located far from power supply filter.

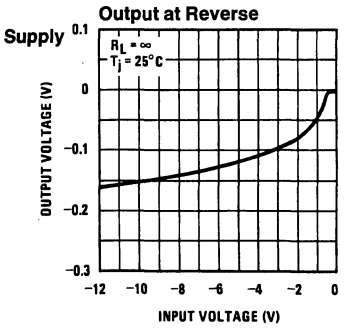
**C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor should be less than 1Ω over the expected operating temperature range.

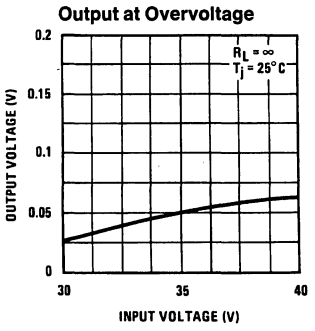
Typical Performance Characteristics

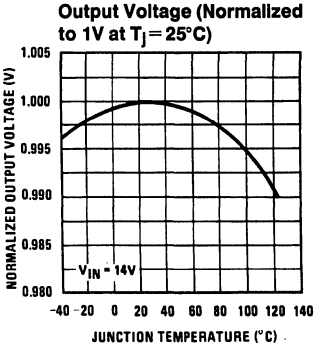












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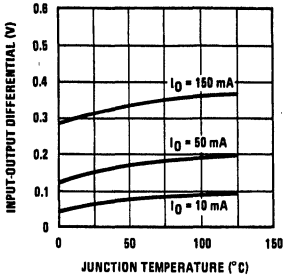
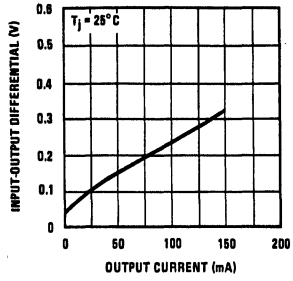
Typical Performance Characteristics (Continued)

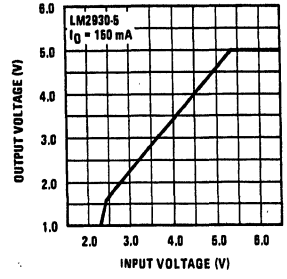
Dropout Voltage



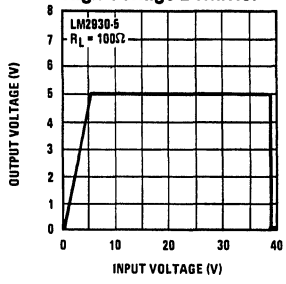
Dropout Voltage



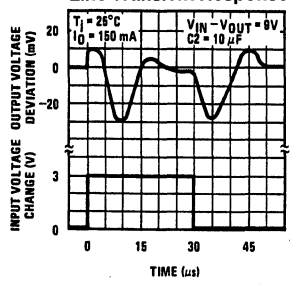
Low Voltage Behavior



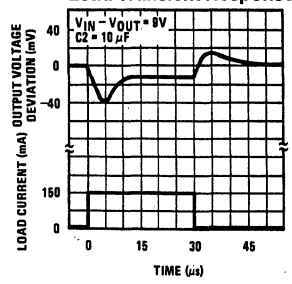
High Voltage Behavior



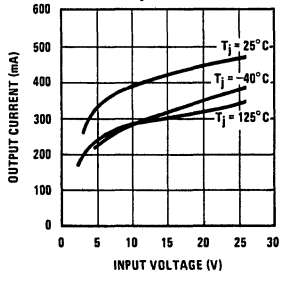
Line Transient Response



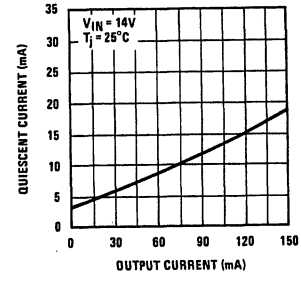
Load Transient Response



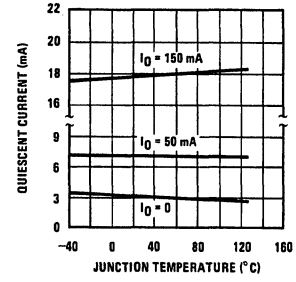
Peak Output Current



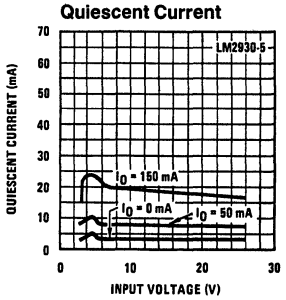
Quiescent Current



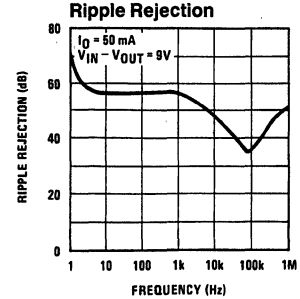
Quiescent Current



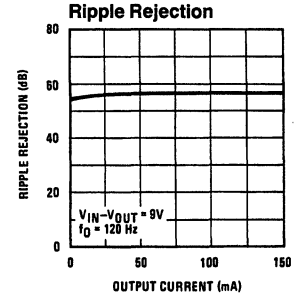
Quiescent Current



Ripple Rejection



Ripple Rejection



TL/H/5539–2

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

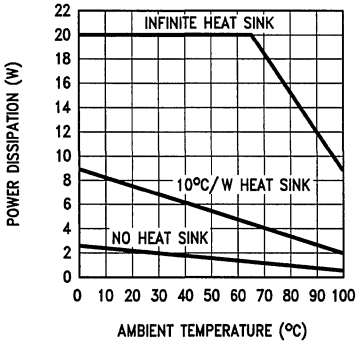
Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Maximum Power Dissipation (TO-220)



TL/H/5539–6

National Semiconductor

LM2931 Series Low Dropout Regulators

General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1 mA or less when supplying 10 mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10 mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 100 mA of output current.

Designed originally for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed output of 5V is available in the plastic TO-220 power package or the popular TO-92 package. An adjustable output version, with on/off switch, is available in a 5-lead TO-220 package.

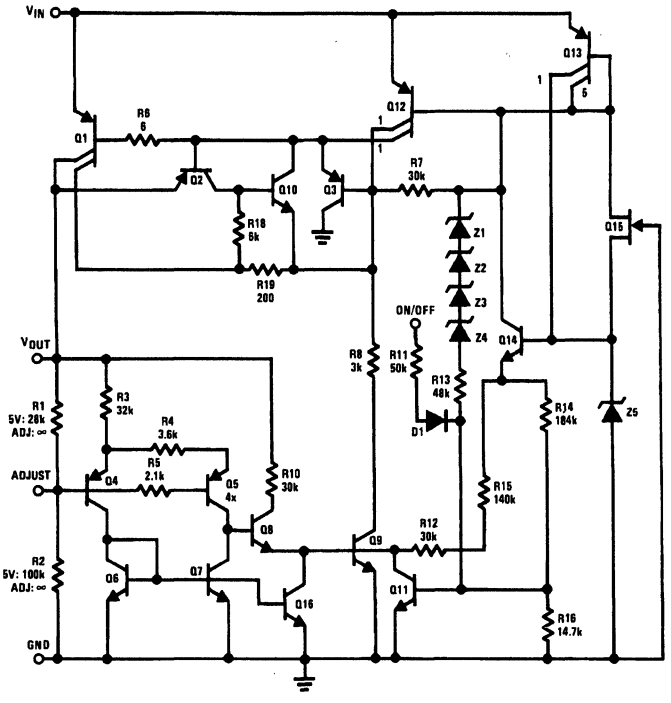
Features

- Very low quiescent current
- Output current in excess of 100 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in plastic TO-220 or TO-92
- Available as adjustable with TTL compatible switch
- 100% electrical burn-in in thermal limit

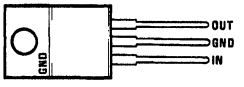
Output Voltage Options

LM2931T-5.0	5V	LM2931AT-5.0	5V
LM2931Z-5.0	5V	LM2931AZ-5.0	5V
LM2931CT	Adjustable from 3V to 26V		

Schematic and Connection Diagrams



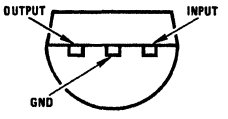
TO-220 3-Lead



Front View

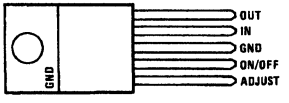
Order Number LM2931
See NS Package T03B, Z03A, T05A

TO-92



Bottom View

TO-220 5-Lead



Front View

TL/H/5254–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	26V
Operating Range	
Overvoltage Protection	
LM2931A, LM2931CT Adjustable	60V
LM2931	50V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics

V_{IN} = 14V, I_O = 10 mA, T_J = 25°C (Note 1), C2 = 100 µF (unless otherwise specified)

Parameter	Conditions	LM2931A-5.0			LM2931-5.0			Units Limit
		Typ	Test Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Output Voltage		5	5.19 4.81			5.25 4.75		V_{MAX} V_{MIN}
	6.0V≤V_{IN}≤26V, I_O 100 mA −40°C≤T_j≤125°C			5.25 4.75			5.5 4.5	V_{MAX} V_{MIN}
Line Regulation	9V≤V_{IN}≤16V 6V≤V_{IN}≤26V	2 4	10 30		2 4	10 30		mV_{MAX} mV_{MAX}
Load Regulation	5 mA≤I_O≤100 mA	14	50		14	50		mV_{MAX}
Output Impedance	100 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	200		600	200			$m\Omega_{MAX}$
Quiescent Current	I_O≤10 mA, 6V≤V_{IN}≤26V −40°C≤T_j≤125°C I_O=100 mA, V_{IN}=14V, T_j=25°C	0.4 15	1.0	1.0 30 5	0.4 15	1.0	1.0	mA_{MAX} mA_{MIN} mA_{MAX} mA_{MIN}
Output Noise Voltage	10 Hz–100 kHz, C_{OUT} = 100 µF	500		1000	500			$\mu V_{rms_{MAX}}$
Long Term Stability		20		50	20			mV/1000 hr
Ripple Rejection	f_O=120 Hz	80		55	80			dB_{MIN}
Dropout Voltage	I_O=10 mA I_O=100 mA	0.05 0.3	0.2 0.6		0.05 0.3	0.2 0.6		V_{MAX} V_{MAX}
Maximum Operational Input Voltage		33	 26		33	 26		V_{MAX} V_{MIN}
Maximum Line Transient	R_L=500Ω, V_O≤5.5V, 100 ms	70	60		70	50		V_{MIN}
Reverse Polarity Input Voltage, DC	V_O≥−0.3V, R_L = 500Ω	−30	−15		−30	−15		V_{MIN}
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100 ms, R_L = 500Ω	−80	−50		−80	−50		V_{MIN}

Note 1: To ensure constant junction temperature, low duty cycle pulse testing is used.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Thermal resistance junction-to-case (θ_{jc}) is 3°C/W; case-to-ambient is 50°C/W.

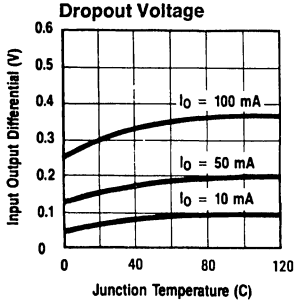
Electrical Characteristics for Adjustable LM2931CT

V_{IN} = 14V, V_{OUT} = 3V, I_O = 10 mA, T_J = 25°C (Note 1), R1 = 27k, C2 = 100 µF (unless otherwise specified)

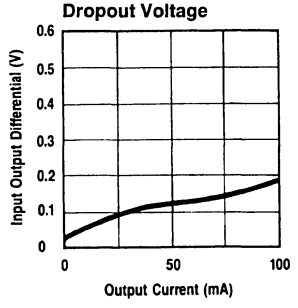
Parameter	Conditions	Typ	Tested Limit	Design Limit	Units Limit
Reference Voltage		1.20	1.26 1.14		V_{MAX} V_{MIN}
	$I_O \leq 100$ mA, $-40°C \leq T_j = \leq 125°C$, R1 = 27k Measured from V_{OUT} to Adjust Pin			1.32 1.08	V_{MAX} V_{MIN}
Output Voltage Range			24 3		V_{MAX} V_{MIN}
Line Regulation	$V_{OUT} + 0.6V \leq V_{IN} \leq 26V$	0.2	1.5		mV/V_{MAX}
Load Regulation	5 mA $\leq I_O \leq$ 100 mA	0.3	1		$\%_{MAX}$
Output Impedance	100 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	40			mΩ/V
Quiescent Current	I_O = 10 mA I_O = 100 mA During Shutdown R_L = 500Ω	0.4 15 0.8	1 1		mA_{MAX} mA mA_{MAX}
Output Noise Voltage	10 Hz–100 kHz	100			$\mu V_{rms}/V$
Long Term Stability		0.4			%/1000 hr
Ripple Rejection	f_O = 120 Hz	0.02			%/V
Dropout Voltage	$I_O \leq 10$ mA I_O = 100 mA	0.05 0.3	0.2 0.6		V_{MAX} V_{MAX}
Maximum Operational Input Voltage		33	26		V_{MIN}
Maximum Line Transient	I_O = 10 mA, Reference Voltage ≤ 1.5V	70	60		V_{MIN}
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$, R_L = 500Ω	−30	−15		V_{MIN}
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, T ≤ 100 ms, R_L = 500Ω	−80	−50		V_{MIN}
On/Off Threshold Voltage On Off	V_O = 3V	 2.0 2.2	 1.2 3.25		 V_{MAX} V_{MIN}
On/Off Threshold Current		20	50		μA_{MAX}

Typical Performance Characteristics

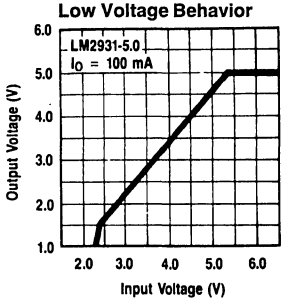
Dropout Voltage



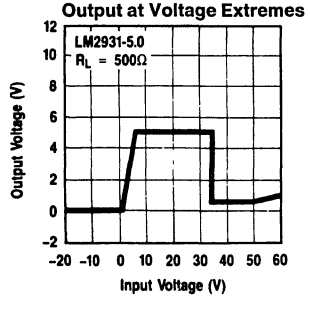
Dropout Voltage



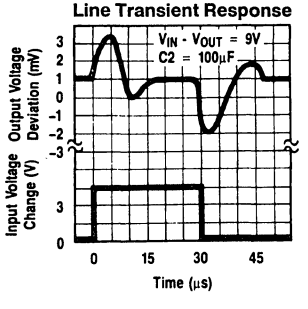
Low Voltage Behavior



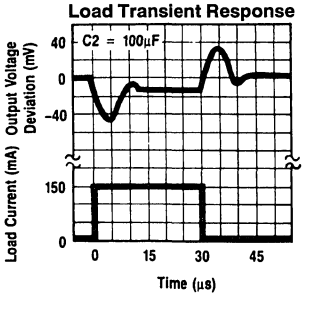
Output at Voltage Extremes



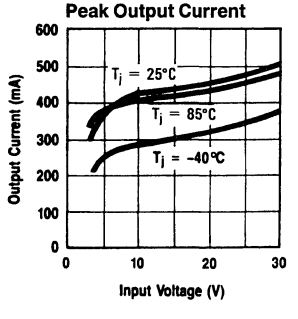
Line Transient Response



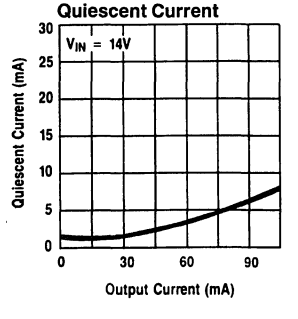
Load Transient Response



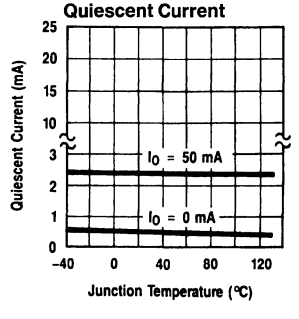
Peak Output Current



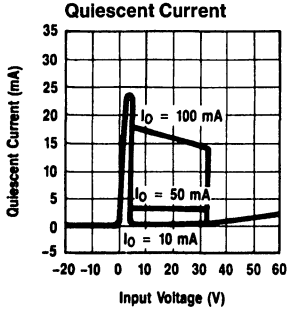
Quiescent Current



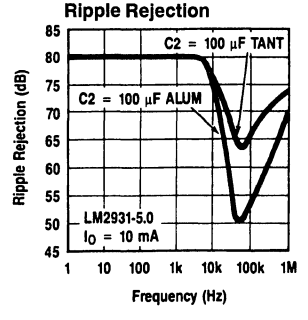
Quiescent Current



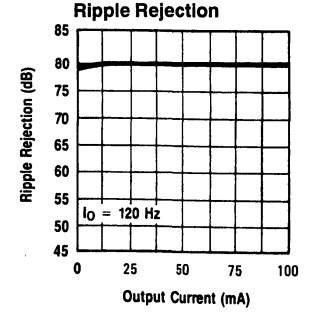
Quiescent Current



Ripple Rejection



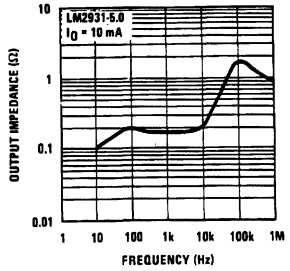
Ripple Rejection



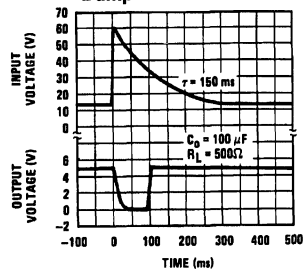
TL/H/5254–2

Typical Performance Characteristics (Continued)

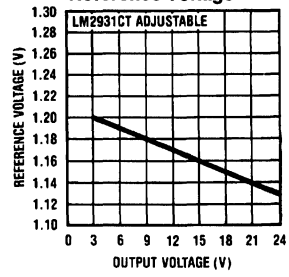
Output Impedance



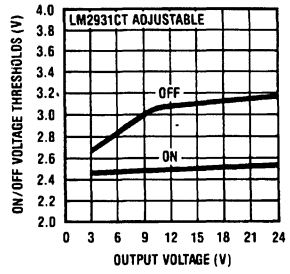
Operation During Load Dump



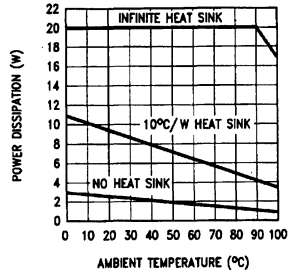
Reference Voltage



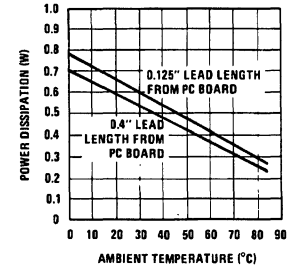
On/Off Threshold



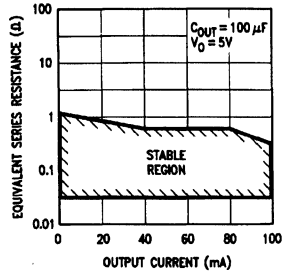
Maximum Power Dissipation (TO-220)



Maximum Power Dissipation (TO-92)

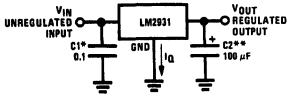


Output Capacitor ESR



TL/H/5254–3

Typical Applications

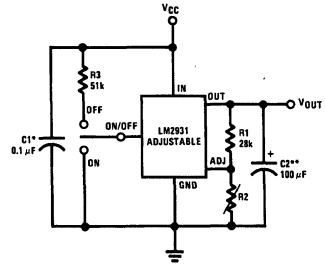


TL/H/5254–4

$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

Note: Using 28k for R1 will automatically compensate for errors in V_{OUT} due to the input bias current of the ADJ pin (approximately 1 μA).

LM2931 Adjustable



TL/H/5254–5

*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 100 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

Application Hints

One of the distinguishing factors of the LM2931 series regulators is the requirement of an output capacitor for device stability. The value required varies greatly depending upon the application circuit and other factors. Thus some comments on the characteristics of both capacitors and the regulator are in order.

High frequency characteristics of electrolytic capacitors depend greatly on the type and even the manufacturer. As a result, a value of capacitance that works well with the LM2931 for one brand or type may not necessary be sufficient with an electrolytic of different origin. Sometimes actual bench testing, as described later, will be the only means to determine the proper capacitor and value. Experience has shown that, as a rule of thumb, the more expensive and higher quality electrolytics generally allow a smaller value for regulator stability. As an example, while a high-quality 100 μF aluminum electrolytic covers all general application circuits, similar stability can be obtained with a tantalum electrolytic of only 47 μF. This factor of two can generally be applied to any special application circuit also.

Another critical characteristic of electrolytics is their performance over temperature. While the LM2931 is designed to operate to $-40°C$, the same is not always true with all electrolytics (hot is generally not a problem). The electrolyte in many aluminum types will freeze around $-30°C$, reducing their effective value to zero. Since the capacitance is needed for regulator stability, the natural result is oscillation (and lots of it) at the regulator output. For all application circuits where cold operation is necessary, the output capacitor must be rated to operate at the minimum temperature. By coincidence, worst-case stability for the LM2931 also occurs at minimum temperatures. As a result, in applications where the regulator junction temperature will never be less than 25°C, the output capacitor can be reduced approximately by a factor of two over the value needed for the entire temperature range. To continue our example with the tantalum electrolytic, a value of only 22 μF would probably thus suffice. For high-quality aluminum, 47 μF would be adequate in such an application.

Another regulator characteristic that is noteworthy is that stability decreases with higher output currents. This sensible fact has important connotations. In many applications, the LM2931 is operated at only a few milliamps of output current or less. In such a circuit, the output capacitor can be further reduced in value. As a rough estimation, a circuit that is required to deliver a maximum of 10 mA of output current from the regulator would need an output capacitor of only half the value compared to the same regulator required to deliver the full output current of 100 mA. If the example of the tantalum capacitor in the circuit rated at 25°C junction temperature and above were continued to include a maximum of 10 mA of output current, then the 22 μF output capacitor could be reduced to only 10 μF.

In the case of the LM2931CT adjustable regulator, the minimum value of output capacitance is a function of the output voltage. As a general rule, the value decreases with higher output voltages, since internal loop gain is reduced.

At this point, the procedure for bench testing the minimum value of an output capacitor in a special application circuit should be clear. Since worst-case occurs at minimum operating temperatures and maximum operating currents, the entire circuit, including the electrolytic, should be cooled to the minimum temperature. The input voltage to the regulator should be maintained at 0.6V above the output to keep internal power dissipation and die heating to a minimum. Worst-case occurs just after input power is applied and before the die has had a chance to heat up. Once the minimum value of capacitance has been found for the brand and type of electrolytic in question, the value should be doubled for actual use to account for production variations both in the capacitor and the regulator. (All the values in this section and the remainder of the data sheet were determined in this fashion.)

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM2935 Low Dropout Dual Regulator

General Description

The LM2935 dual 5V regulator provides a 750 mA output as well as a 10 mA standby output. It features a low quiescent current of 3 mA or less when supplying 10 mA loads from the 5V standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include microprocessor power supplies demanding as much as 750 mA of output current.

Designed for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- Two 5V regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in 5-lead TO-220
- ON/OFF switch controls high current output
- Reset error flag
- 100% electrical burn-in in thermal limit

Typical Application Circuit

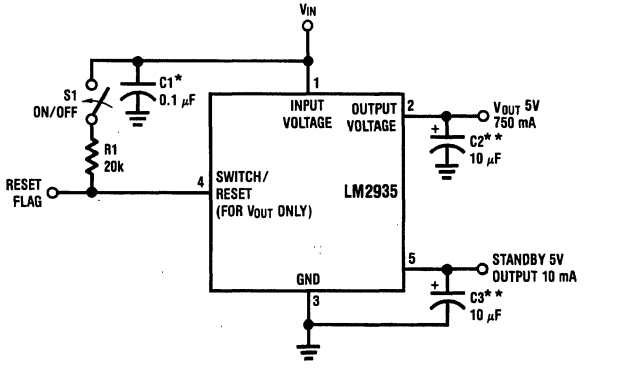


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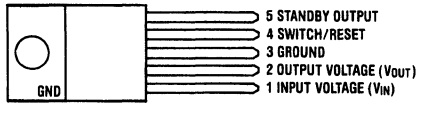
FIGURE 1. Test and Application Circuit

*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

Connection Diagram

TO-220 5-Lead



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Front View

Order Number LM2935T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection	60V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	−40°C to + 125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to + 150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics for V_{OUT}

V_{IN} = 14V, I_O = 500 mA, T_J = 25°C (Note 4), C2 = 10 μF (unless otherwise specified)

Parameter	Conditions	Typ	Tested Limit (Note 3)	Units Limit
Output Voltage	6V≤V_{IN}≤26V, 5 mA≤I_O≤500 mA, −40°C≤T_J≤125°C (Note 2)	5.00	5.25 4.75	V_{MAX} V_{MIN}
Line Regulation	9V≤V_{IN}≤16V, I_O=5 mA 6V≤V_{IN}≤26V, I_O=5 mA	4 10	25 50	mV_{MAX} mV_{MAX}
Load Regulation	5 mA≤I_O≤500 mA	10	50	mV_{MAX}
Output Impedance	500 mA_{DC} and 10 mA_{rms}, 100 Hz–10 kHz	200		mΩ
Quiescent Current	I_O≤10 mA, No Load on Standby I_O=500 mA, No Load on Standby I_O=750 mA, No Load on Standby	3 40 90	100	mA mA_{MAX} mA
Output Noise Voltage	10 Hz–100 kHz	100		μV_{rms}
Long Term Stability		20		mV/1000 hr
Ripple Rejection	f_O=120 Hz	66		dB
Dropout Voltage	I_O=500 mA I_O=750 mA	0.45 0.82	0.6	V_{MAX}
Current Limit		1.2	0.75	A_{MIN}
Maximum Operational Input Voltage		31	26	V_{MIN}
Maximum Line Transient	V_O≤5.5V	70	60	V
Reverse Polarity Input Voltage, DC		−30	−15	V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100 ms, 10Ω Load	−80	−50	V
Reset Output Voltage Low High	 R1=20k, V_{IN}=4.0V R1=20k, V_{IN}=14V	 0.9 5.0	 1.2 6.0 4.5	 V_{MAX} V_{MAX} V_{MIN}
Reset Output Current	Reset=1.2V	5		mA
ON/OFF Resistor	R1 (± 10% Tolerance)		20	$k\Omega_{MAX}$

Note 1: Thermal resistance without a heat sink for junction to case temperature is 3°C/W(TO-220). Thermal resistance for TO-220 case to ambient temperature is 50° C/W.

Note 2: The temperature extremes are guaranteed but not 100% production tested. This parameter is not used to calculate outgoing AQL.

Note 3: Tested Limits are guaranteed and 100% tested in production.

Note 4: To ensure constant junction temperature, low duty cycle pulse testing is used.

Electrical Characteristics for Standby Output

$I_O = 10$ mA, $V_{IN} = 14V$, S1 open, $C_{OUT} = 10\ \mu F$, $T_J = 25°C$ (Note 4), (unless otherwise specified)

Parameter	Standby Output Conditions	Typ	Tested Limit	Units Limit
Output Voltage	$I_O \leq 10$ mA, $6V \leq V_{IN} \leq 26V$, $-40°C \leq T_J \leq 125°C$	5.00	5.25 4.75	V_{MAX} V_{MIN}
Tracking	V_{OUT}–Standby Output Voltage	50	200	mV_{MAX}
Line Regulation	$6V \leq V_{IN} \leq 26V$	4	50	mV_{MAX}
Load Regulation	1 mA $\leq I_O \leq$ 10 mA	10	50	mV_{MAX}
Output Impedance	10 mA_{DC} and 1 mA_{rms}, 100 Hz–10 kHz	1		Ω
Quiescent Current	$I_O \leq 10$ mA, V_{OUT} OFF (Note 2)	2	3	mA_{MAX}
Output Noise Voltage	10 Hz–100 kHz	300		μV
Long Term Stability		20		mV/1000 hr
Ripple Rejection	$f_O = 120$ Hz	66		dB
Dropout Voltage	$I_O \leq 10$ mA	0.55	0.7	V_{MAX}
Current Limit		70	25	mA_{MIN}
Maximum Operational Input Voltage	$V_O \leq 6V$	70	60	V_{MIN}
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$, 510Ω Load	−30	−15	V_{MIN}
Reverse Polarity Input Voltage, Transient	1% Duty Cycle T ≤ 100 ms 500Ω Load	−80	−50	V_{MIN}

Typical Circuit Waveforms

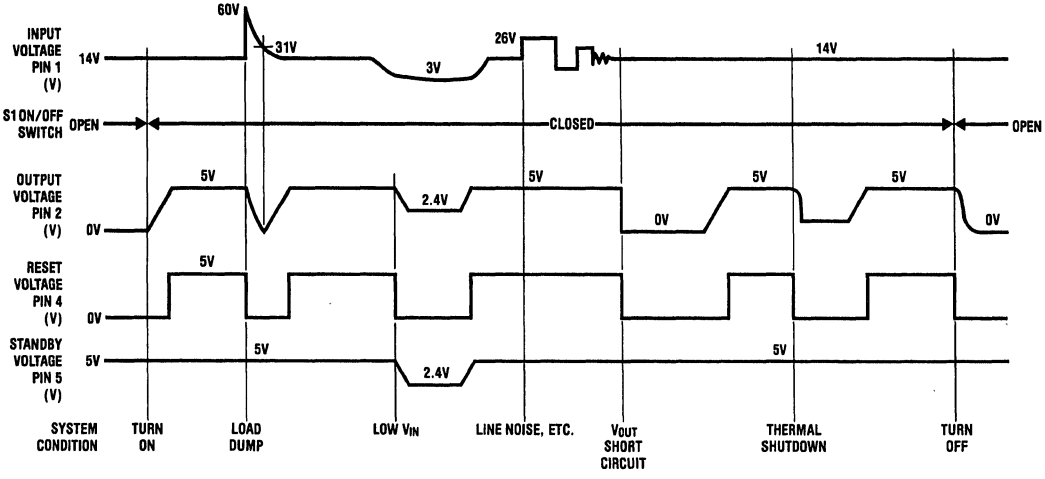

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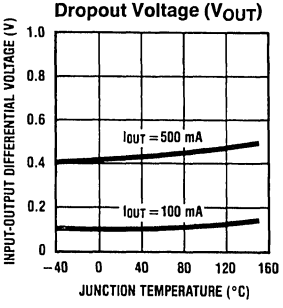
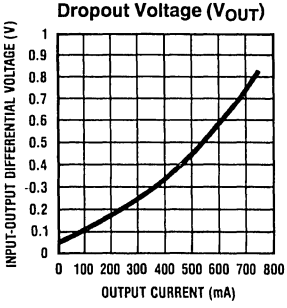
FIGURE 2

Typical Performance Characteristics

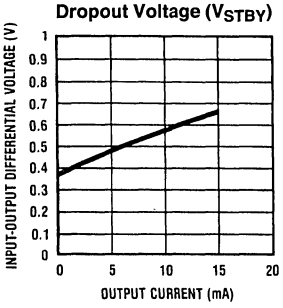
Dropout Voltage (V_{OUT})



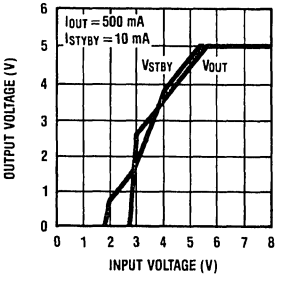
Dropout Voltage (V_{OUT})



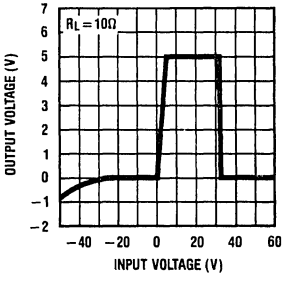
Dropout Voltage (V_{STBY})



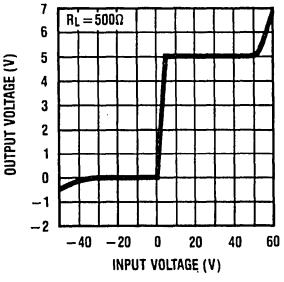
Low Voltage Behavior



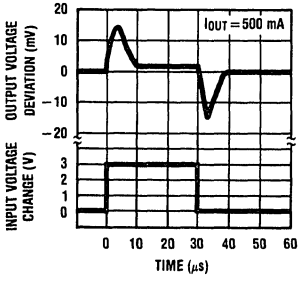
Output Voltage (V_{OUT})



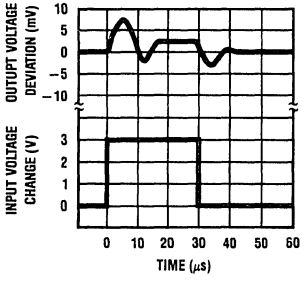
Output Voltage (V_{STBY})



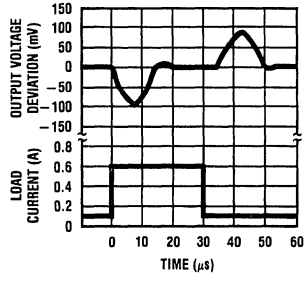
Line Transient Response (V_{OUT})



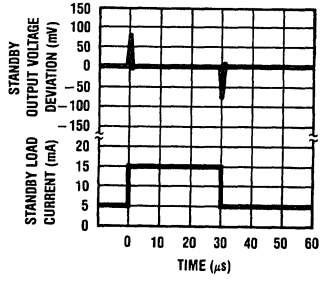
Line Transient Response (V_{STBY})



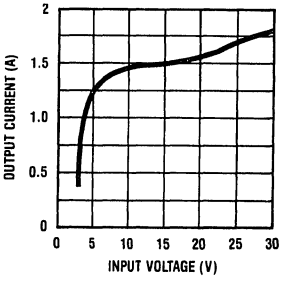
Load Transient Response (V_{OUT})



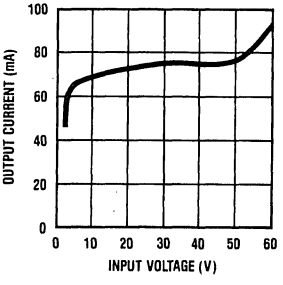
Load Transient Response (V_{STBY})



Peak Output Current (V_{OUT})



Peak Output Current (V_{STBY})



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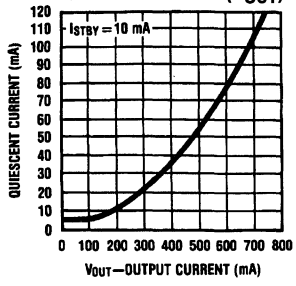
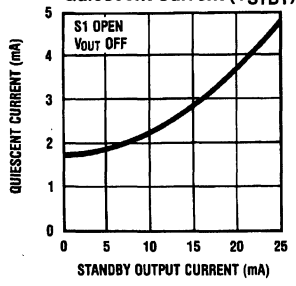
Typical Performance Characteristics (Continued)

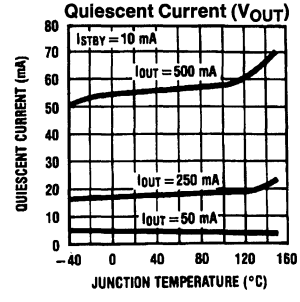
Quiescent Current (V_{OUT})



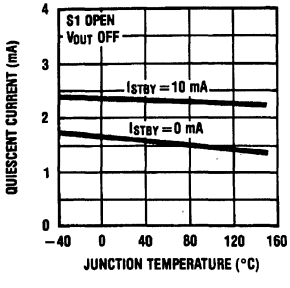
Quiescent Current (V_{STBY})



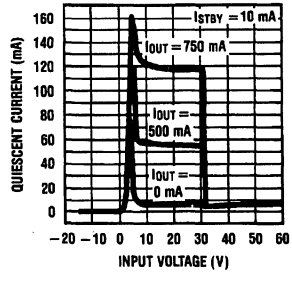
Quiescent Current (V_{OUT})



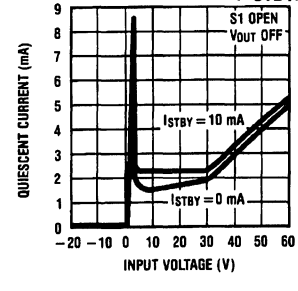
Quiescent Current (V_{STBY})



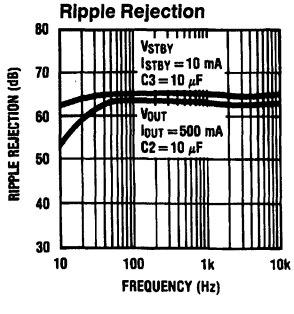
Quiescent Current



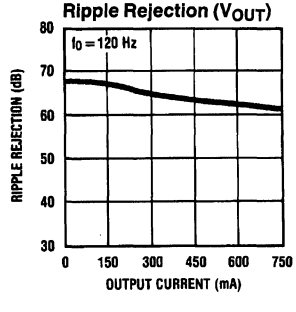
Quiescent Current (V_{STBY})



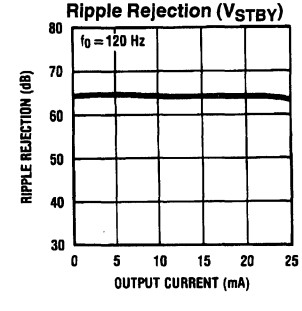
Ripple Rejection



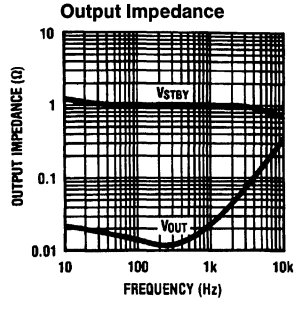
Ripple Rejection (V_{OUT})



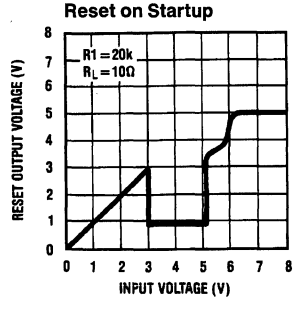
Ripple Rejection (V_{STBY})



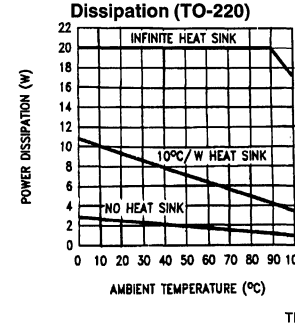
Output Impedance



Reset on Startup



Maximum Power Dissipation (TO-220)



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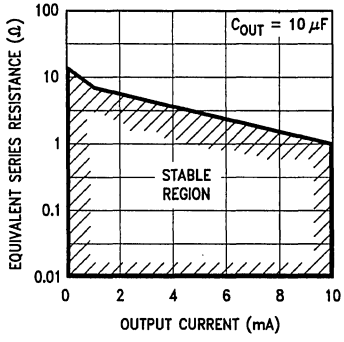
Typical Performance Characteristics (Continued)

Output Capacitor ESR (Standby Output, Pin 5)



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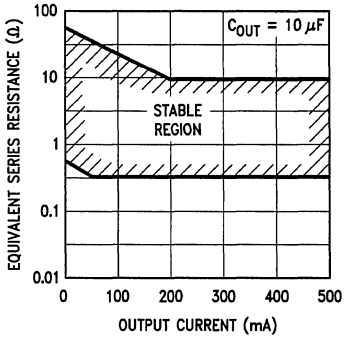
Output Capacitor ESR (Main Output, Pin 2)



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Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

EXTERNAL CAPACITORS

The LM2935 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

No capacitor must be attached to the ON/OFF and ERROR FLAG pin. Due to the internal circuits of the IC, oscillation on this pin could result.

STANDBY OUTPUT

The LM2935 differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

Application Hints (Continued)

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a more expensive capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener (*Figure 3*), the current through the external resistor should be sufficient to bias R2 and R3 up to this point. Approximately 60 μA will suffice, resulting in a 10k external resistor for most applications (*Figure 4*).

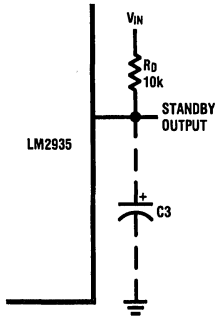

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FIGURE 4. Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

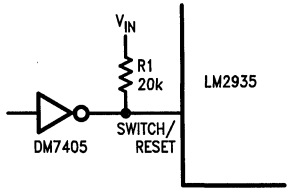

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FIGURE 5. Controlling ON/OFF Terminal with a Typical Open Collector Logic Gate

ON/OFF AND ERROR FLAG PIN

This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in *Figure 1* (common in automotive systems where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions, the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

The ON/OFF pin can also be driven directly from open collector logic circuits. The only requirement is that the 20k pull-up resistor remain in place *(Figure 5).* This will not affect the logic gate since the voltage on this pin is limited by the internal clamp in the LM2935 to 5V.

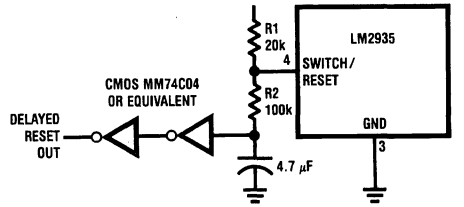

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FIGURE 6. Reset Pulse on Power-Up (with approximately 300 ms delay)

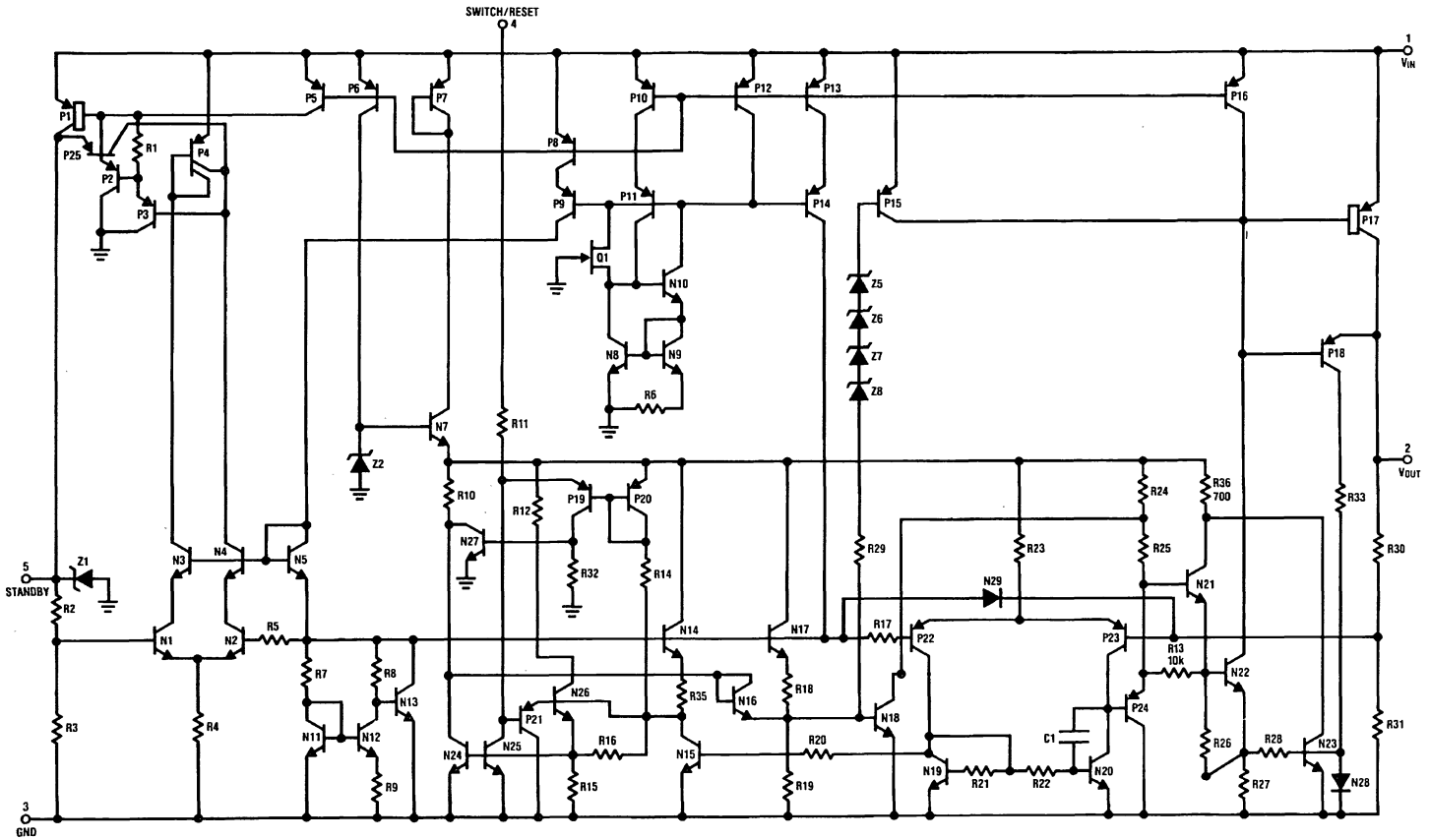

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FIGURE 3

National Semiconductor

LM2936 Ultra-Low Quiescent Current 5V Regulator

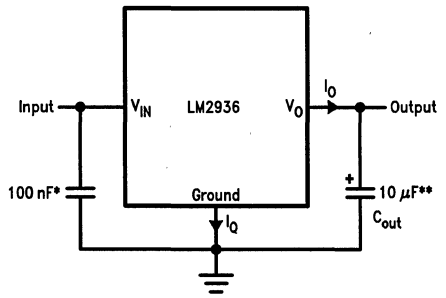
General Description

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15 μA quiescent current at a 100 μA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936 has a 40V operating voltage limit, −40°C to +125°C operating temperature range, and ±2% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936 is available in a TO-92 package with a fixed 5V output.

Features

- Ultra low quiescent current ($I_Q \leq 15$ μA for $I_O \leq 100$ μA)
- Fixed 5V, 50 mA output
- Output tolerance ±2% over line, load, and temperature
- Dropout voltage typically 200 mV @ I_O = 50 mA
- Reverse battery protection
- −50V reverse transient protection
- Internal short circuit current limit
- Internal thermal shutdown protection
- 40V operating voltage limit

Typical Application



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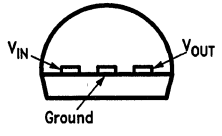
* Required if regulator is located more than 2″ from power supply filter capacitor.

** Required for stability. Must be rated for 10 μF minimum over intended operating temperature range. Effective series resistance (ESR) is critical, see curve. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagram

TO-92 Plastic Package (Z)



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Bottom View

Order Number LM2936Z
See NS Package Number Z03A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Survival)	+60V, −50V
ESD Susceptability (Note 2)	2000V
Power Dissipation (Note 3)	Internally limited
Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Maximum Input Voltage (Operational)	40V

Electrical Characteristics

V_{IN} = 14V, I_O = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Typical (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
Output Voltage	5.5V ≤ V_{IN} ≤ 26V, I_O ≤ 50 mA (Note 7)		**4.9**		V_{min}
		5			V
			5.1		V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	5	10		mV_{max}
	6V ≤ V_{IN} ≤ 40V, I_O = 1 mA	10	30		
Load Regulation	100 μA ≤ I_O ≤ 5 mA	10	30		mV_{max}
	5 mA ≤ I_O ≤ 50 mA	10	30		
Output Impedance	I_O = 30 mAdc and 10 mArms, f = 1000 Hz	450			mΩ
Quiescent Current	I_O = 100 μA, 8V ≤ V_{IN} ≤ 24V	9	15		μA_{max}
	I_O = 10 mA, 8V ≤ V_{IN} ≤ 24V	0.20	0.50		mA_{max}
	I_O = 50 mA, 8V ≤ V_{IN} ≤ 24V	1.5	2.5		mA_{max}
Output Noise Voltage	10 Hz–100 kHz	500			μV_{rms}
Long Term Stability		20			mV/1000 Hr
Ripple Rejection	V_{ripple} = 1 V_{rms}, f_{ripple} = 120 Hz	60	40		dB_{min}
Dropout Voltage	I_O = 100 μA	0.05	0.10		V_{max}
	I_O = 50 mA	0.20	0.40		V_{max}
Reverse Polarity DC Input Voltage	R_L = 500Ω, V_O ≥ −0.3V		−15		V_{min}
Reverse Polarity Transient Input Voltage	R_L = 500Ω, T = 1 ms	−80	−50		V_{min}
Output Leakage with Reverse Polarity Input	V_{IN} = −15V, R_L = 500Ω	−0.1	−600		μA_{max}
Maximum Line Transient	R_L = 500Ω, V_O ≤ 5.5V, T = 40 ms		60		V_{min}
Short Circuit Current	V_O = 0V	120	250		mA_{max}
			65		mA_{min}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 3: The maximum power dissipation is a function of T_{Jmax}, Θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2936 will go into thermal shutdown. For the LM2936Z, the junction-to-ambient thermal resistance (Θ_{JA}) is 195°C/W.

Note 4: Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

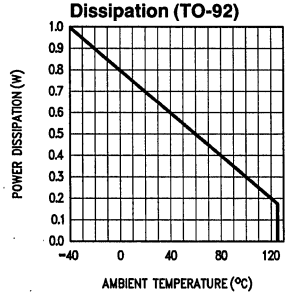
Note 5: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level) and 100% tested.

Note 6: Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but not 100% tested.

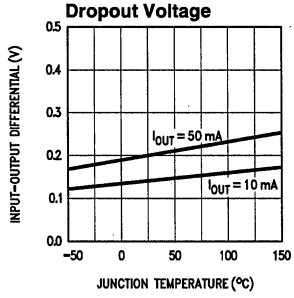
Note 7: To ensure constant junction temperature, pulse testing is used.

Typical Performance Characteristics

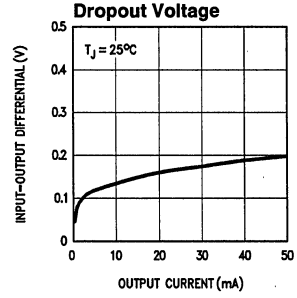
Maximum Power Dissipation (TO-92)



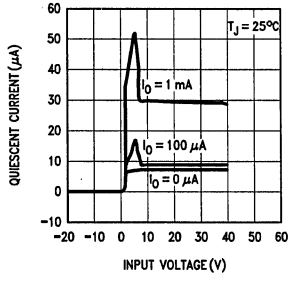
Dropout Voltage



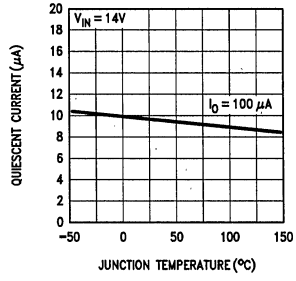
Dropout Voltage



Quiescent Current



Quiescent Current



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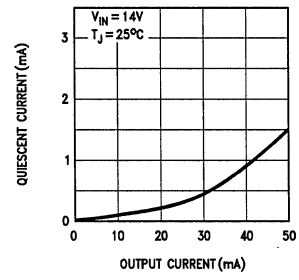
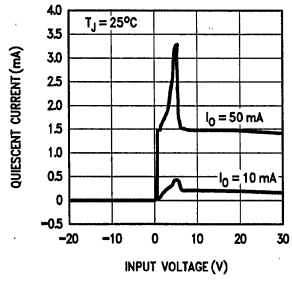
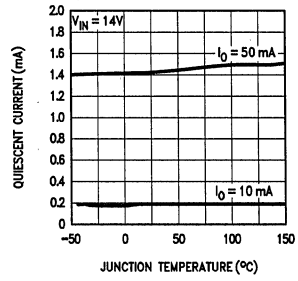


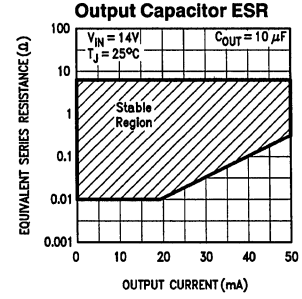
Quiescent Current



Quiescent Current



Output Capacitor ESR



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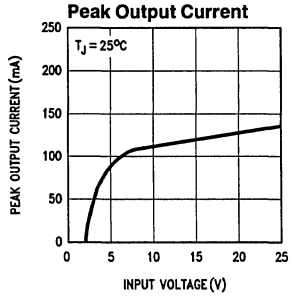
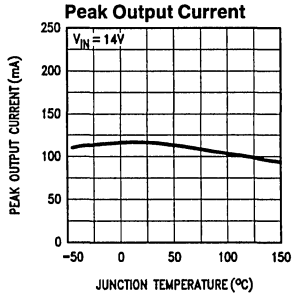
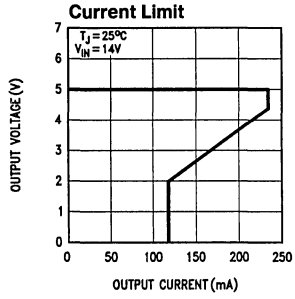
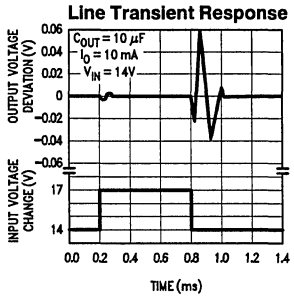
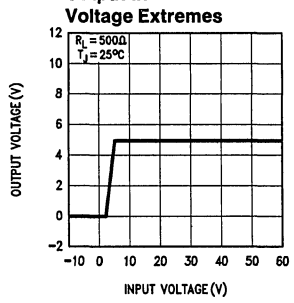
Typical Performance Characteristics (Continued)

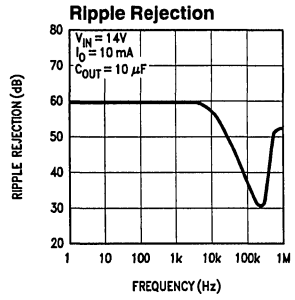


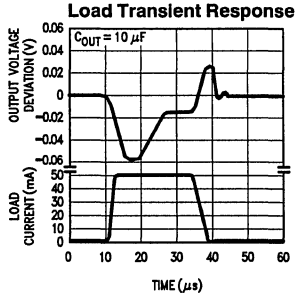


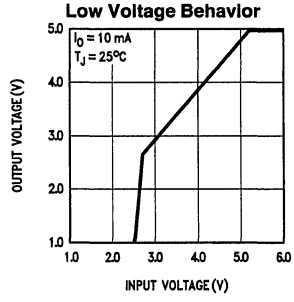


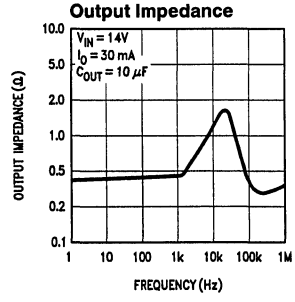












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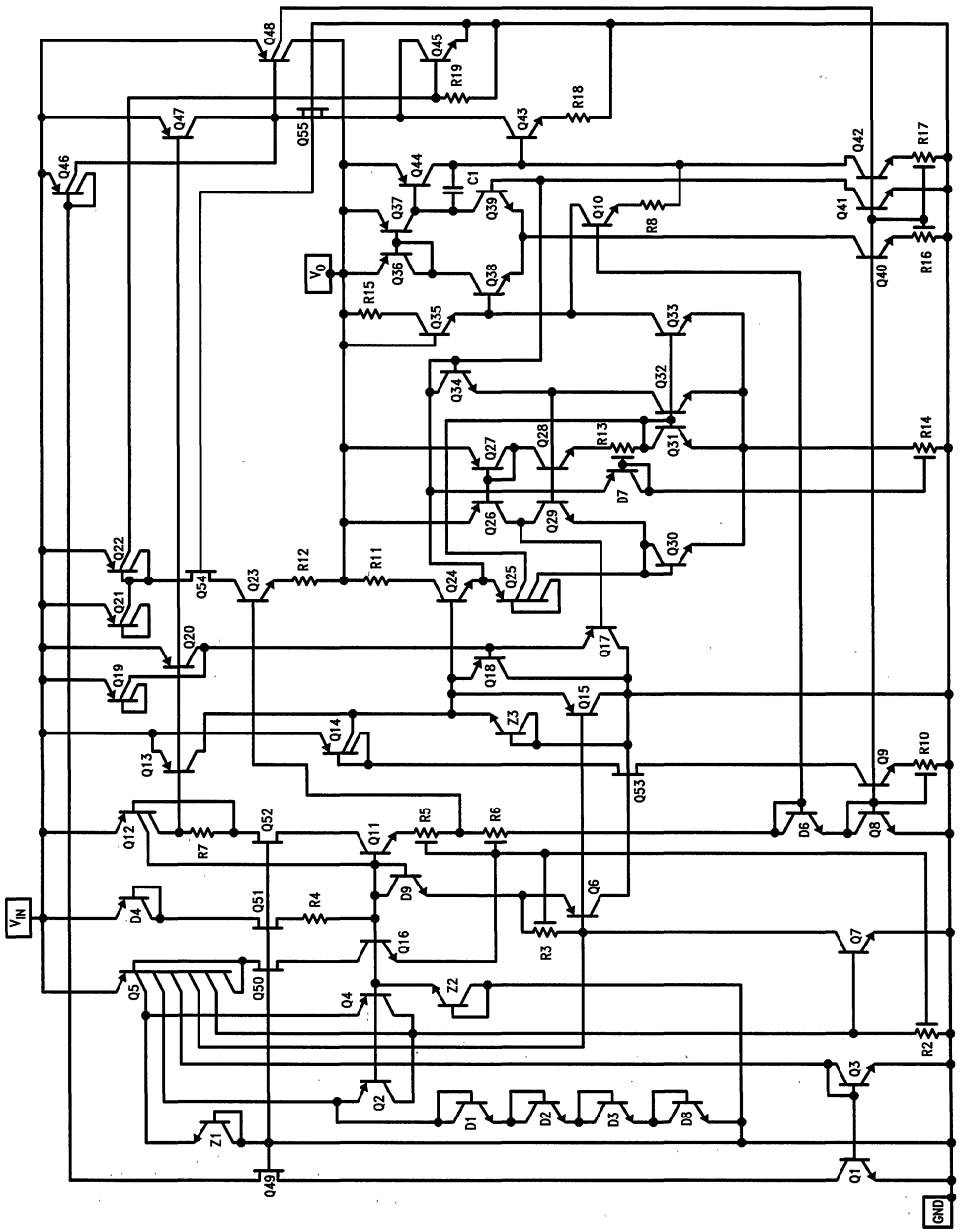
Applications Information

Unlike other PNP low dropout regulators, the LM2936 remains fully operational to 40V. Owing to power dissipation characteristics of the TO-92 package, full output current cannot be guaranteed for all combinations of ambient temperature and input voltage. As an example, consider an LM2936 operating at 25°C ambient. Using the formula for maximum allowable power dissipation given in Note 3, we find that P_{Dmax} = 641 mW at 25°C. Including the small contribution of the quiescent current to total power dissipation the maximum input voltage (while still delivering 50 mA output current) is 17.3V. The device will go into thermal shutdown if it attempts to deliver full output current with an input voltage of more than 17.3V. Similarly, at 40V input and 25°C ambient the LM2936 can deliver 18 mA maximum.

Under conditions of higher ambient temperatures, the voltage and current calculated in the previous examples will drop. For instance, at the maximum ambient of 125°C the LM2936 can only dissipate 128 mW, limiting the input voltage to 7.34V for a 50 mA load, or 3.5 mA output current for a 40V input.

While the LM2936 maintains regulation to 60V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 60V the LM2936 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 60V.

Equivalent Schematic Diagram



National Semiconductor

LM2940 1A Low Dropout Regulator

General Description

The LM2940 positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Futhermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{in} - V_{out} \leq 3V$).

Designed also for vehicular applications, the LM2940 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as load dump (60V) when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

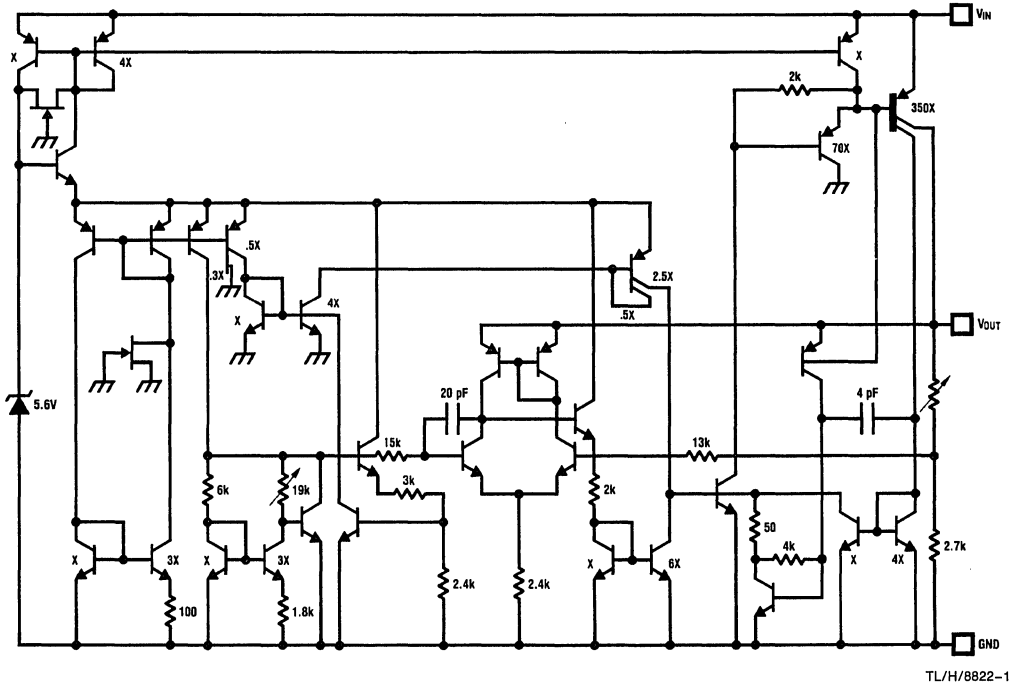
- Dropout voltage typically 0.5V @I_O = 1A
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- 100% electrical burn-in in thermal limit

Output Voltages

LM2940T-5.0	5V
LM2940T-8.0	8V
LM2940T-10	10V

For output voltages of 5V, 12V, and 15V, refer to the LM2940C datasheet.

Equivalent Schematic Diagram



TL/H/8822–1

Order Number LM2940T-5.0, LM2940T-8.0, LM2940T-10
See NS Package Number TO3B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage
- Survival Voltage (≤100 ms) 60V
- Operational Voltage 26V

Internal Power Dissipation (Note 1) Internally Limited

Operating Temperature Range (T_A) −40°C to +125°C
Maximum Junction Temperature 150°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) 230°C
ESD susceptibility rating is to be determined

Electrical Characteristics $V_{in} = V_o + 5V$, $I_o = 1A$, $C_{out} = 22\ \mu F$, $T_j = 25°C$ unless otherwise specified.

Output Voltage (V_o)		5V			8V			10V			Units
Parameter	**Conditions**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	
		6.25V ≤ V_{IN} ≤ 26V			**9.4V ≤ V_{IN} ≤ 26V**			**11.5V ≤ V_{IN} ≤ 26V**			
Output Voltage	5 mA ≤ I_o ≤ 1A	5.00	4.85 5.15	4.75 5.25	8.00	7.76 8.24	7.60 8.40	10.00	9.70 10.30	9.50 10.50	V_{MIN} V_{MAX}
Line Regulation	$V_o + 2V \le V_{in} \le 26V$, $I_o = 5$ mA	20	50		20	80		20	100		mV_{MAX}
Load Regulation	50 mA ≤ I_o ≤ 1A	35	50	80	55	80	130	65	100	165	mV_{MAX}
Output Impedance	100 mADC and 20 mArms $f_o = 120$ Hz	35			55			65			mΩ
Quiescent Current	$V_o + 2V \le V_{in} < 26V$, $I_o = 5$ mA	10	15	20	10	15	20	10	15	20	mA_{MAX}
	$V_{in} = V_o + 5V$, $I_o = 1A$	30	45	60	30	45	60	30	45	60	mA_{MAX}
Output Noise Voltage	10 Hz − 100 kHz $I_o = 5$ mA	150			240			300			μV_{RMS}
Ripple Rejection	$f_o = 120$ Hz, 1 Vrms; $I_l = 100$ mA	72	60	54	66	54	48	63	51	45	dB_{MIN}
Long Term Stability		20			32			36			mV/ 1000 Hr
Dropout Voltage	$I_o = 1A$	0.5	0.8	1.0	0.5	0.8	1.0	0.5	0.8	1.0	V_{MAX}
	$I_o = 100$ mA	110	150	200	110	150	200	110	150	200	mV_{MAX}
Short Circuit Current		1.9	1.6		1.9	1.6		1.9	1.6		A_{MIN}
Maximum Line Transient	$R_o = 100\ \Omega$ T ≤ 100 ms	$V_o \le 6V$			$V_o < 9V$			$V_o < 11V$			
		75	60	60	75	60	60	75	60	60	V_{MIN}
Maximum Operational Input Voltage		31	26	26	31	26	26	31	26	26	V_{dc}
Reverse Polarity Input Voltage DC	$R_O = 100\ \Omega$	−30	−15	−15	−30	−15	−15	−30	−15	−15	V_{MIN}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, $R_o = 100\ \Omega$	−75	−50	−50	−75	−50	−50	−75	−50	−50	V_{MIN}

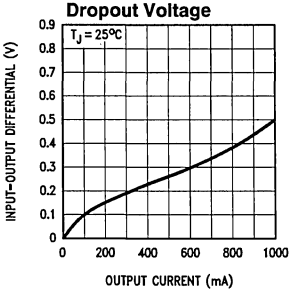
Note 1: Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

Note 2: Tested Limits are guaranteed and 100% production tested.

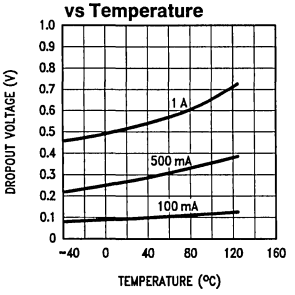
Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

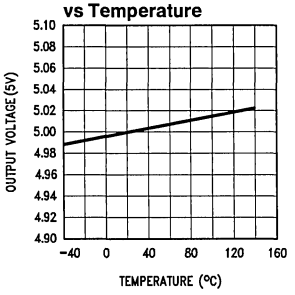
Dropout Voltage



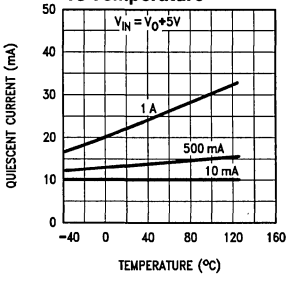
Dropout Voltage vs Temperature



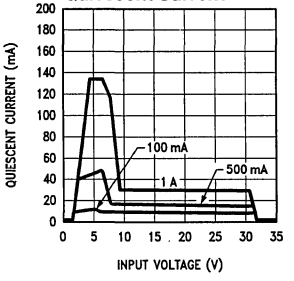
Output Voltage vs Temperature



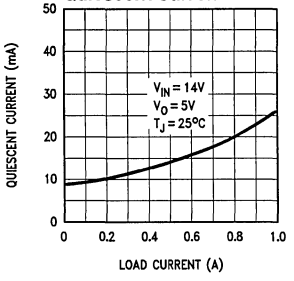
Quiescent Current vs Temperature



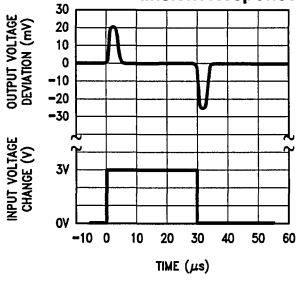
Quiescent Current



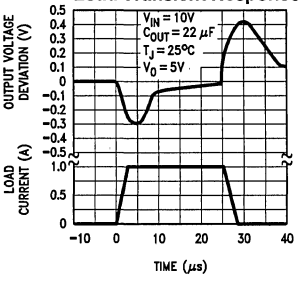
Quiescent Current



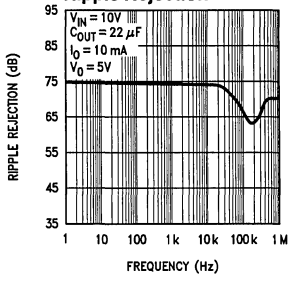
Line Transient Response



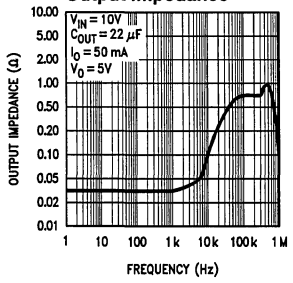
Load Transient Response



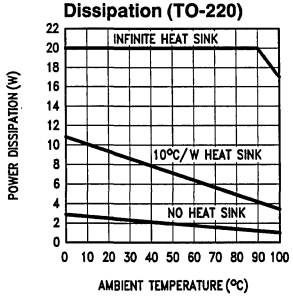
Ripple Rejection



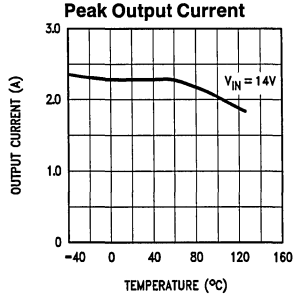
Output Impedance



Maximum Power Dissipation (TO-220)

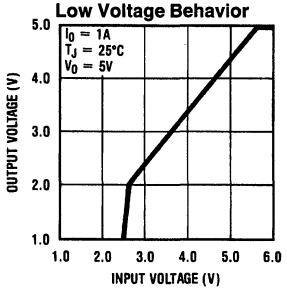


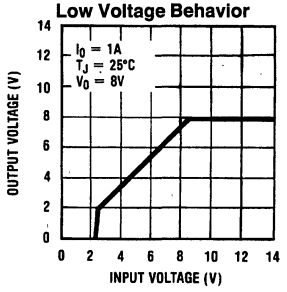
Peak Output Current

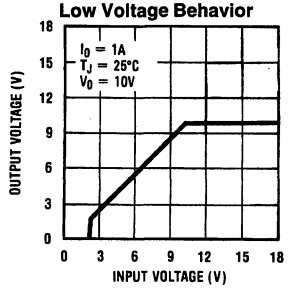


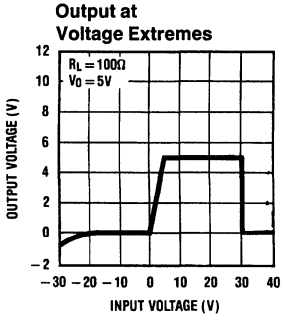
TL/H/8822–4

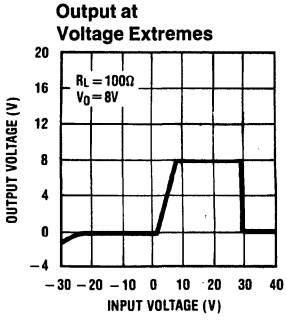
Typical Performance Characteristics (Continued)

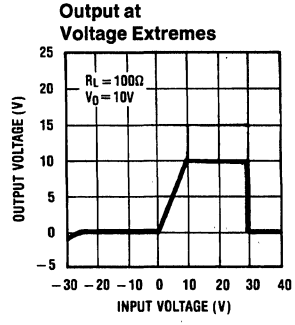




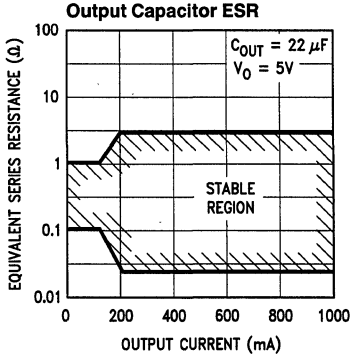






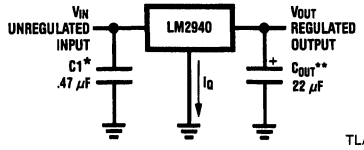


TL/H/8822–5



TL/H/8822–6

Typical Application



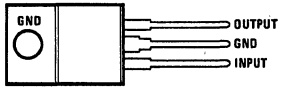
TL/H/8822–3

*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Connection Diagram

(TO-220) Plastic Package



TL/H/8822–2

Front View
Order Number LM2940T-5.0, LM2940T-8.0, LM2940T-10
See NS Package Number T03B

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_O + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentange change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM2940C 1A Low Dropout Regulator

General Description

The LM2940C positive voltage regulator features the ability to source 1A of output current with an input-output differential of typically 0.5V and a maximum of 1V over the entire temperature range. Familiar regulator features such as internal current limit and thermal overload protection are also provided. Furthermore, a quiescent current reduction circuit has been added which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

The low dropout voltage coupled with the high output current capability make the LM2940C useful in applications where the input voltage is maintained at a level within one or two volts of the output voltage to reduce power dissipation and increase overall system efficiency.

The LM2940C is particularly suited for applications where battery life and reverse installation of batteries is a concern.

For automotive temperature range (−40°C to +125°C) applications, refer to the LM2940 datasheet.

Features

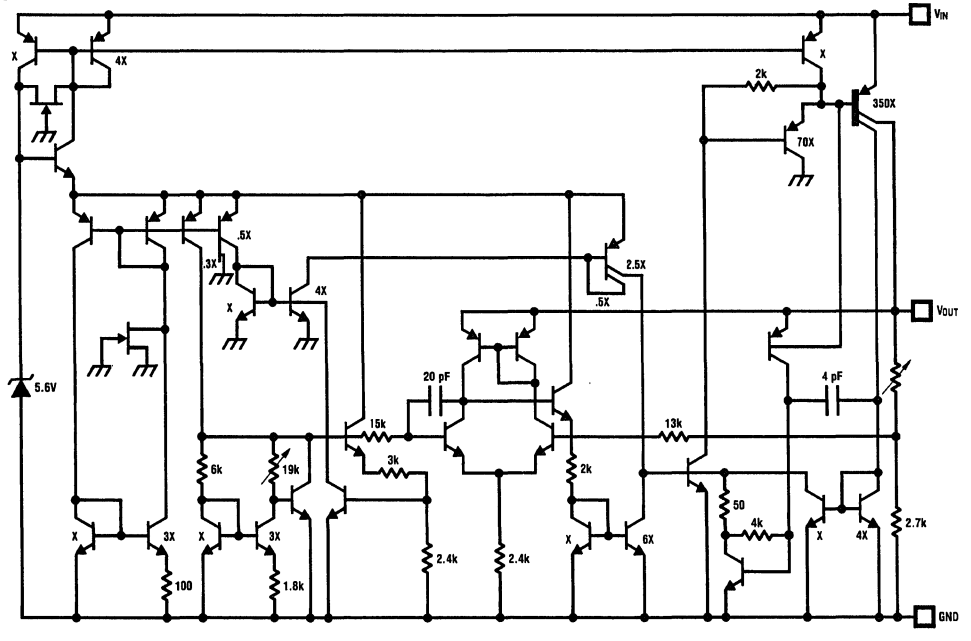
- Dropout voltage typically 0.5V @ I_O = 1A
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- 100% electrical burn-in in thermal limit

Output Voltages

LM2940CT-5.0	5V
LM2940CT-12	12V
LM2940CT-15	15V

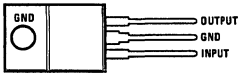
For output voltages of 5V, 8V, and 10V, refer to the LM2940 datasheet.

Equivalent Schematic



TL/H/6158–1

TO-220 3-Lead Plastic Package



Front View

TL/H/6158–4

Order Number LM2940CT-5.0, LM2940CT-12, and LM2940CT-15
See NS Package T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Survival Voltage (≤ 1 ms)	45V
Operational Voltage	26V
Internal Power Dissipation (Note 1)	Internally limited
Operating Temp. Range (T_A)	0°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Susceptability (Note 5)	2000V

Electrical Characteristics

$V_{IN} = V_O + 5V$, $I_O = 1A$, $C_{OUT} = 22\ \mu F$, $T_j = 25°C$, unless otherwise specified.

Output Voltage (V_O)		5V			12V			15V			Units
Parameter	**Conditions**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	**Typ**	**Tested Limit (Note 2)**	**Design Limit (Note 3)**	
Output Voltage	5 mA ≤ I_O ≤ 1A	5.00	4.85 5.15	4.75 5.25	12.00	11.64 12.36	11.40 12.60	15.00	14.55 15.45	14.25 15.75	V_{MIN} V_{MAX}
		6.25V ≤ V_{IN} ≤ 26V			13.6V ≤ V_{IN} ≤ 26V			16.75V ≤ V_{IN} ≤ 26V			
Line Regulation	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5$ mA	20	50		20	120		20	150		mV_{MAX}
Load Regulation	50 mA ≤ I_O ≤ 1A	35	50		55	120		70	150		mV_{MAX}
Output Impedance	100 mADC and 20 mArms f_O = 120 Hz	35			80			100			mΩ
Quiescent Current	$V_O + 2V \le V_{IN} \le 26V$, $I_O = 5$ mA	10	15		10	15		10	15		mA_{MAX}
	$V_{IN} = V_O + 5V$, $I_O = 1A$	30	45	60	30	45	60	30	45	60	mA_{MAX}
Output Noise Voltage	10 Hz–100 kHz I_O = 5 mA	150			360			450			μVrms
Ripple Rejection	f_O = 120 Hz, 1 Vrms, I_O = 100 mA	72	60		66	54		64	52		dBmin
Long Term Stability		20			48			60			mV/1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8	1.0	0.5	0.8	1.0	0.5	0.8	1.0	V_{MAX}
	I_O = 100 mA	110	150	200	110	150	200	110	150	200	mV_{MAX}
Short Circuit Current	$V_{IN\ MAX}$ = 26V (Note 4)	1.9	1.6		1.9	1.6		1.9	1.6		A_{MIN}
Maximum Line Transient	$R_L = 100\Omega$, T ≤ 1 ms	55	45		55	45		55	45		V_{MIN}
		V_O < 6V			V_O < 13V			V_O < 16V			
Reverse Polarity DC Input Voltage	$R_L = 100\Omega$, $V_O \ge -0.6V$	−30	−15		−30	−15		−30	−15		V_{MIN}
Reverse Polarity, Transient Input Voltage	T ≤ 1 ms, $R_L = 100\Omega$	−55	−45	−45	−55	−45	−45	−55	−45	−45	V_{MIN}

Note 1: Thermal resistance without a heat sink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

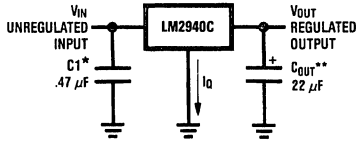
Note 2: Tested Limits are guaranteed and 100% production tested.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

Note 4: Output current will decrease with increasing temperature, but will not go below 1A at the maximum specified temperature.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Application



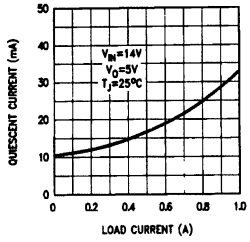
TL/H/6158–2

*Required if regulator is located far from power supply filter.

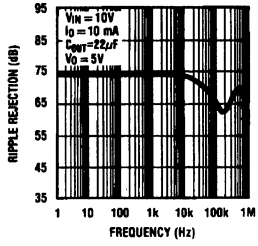
**C_{OUT} must be at least 22 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

Typical Performance Characteristics

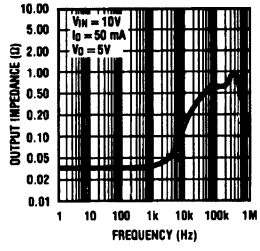
Quiescent Current



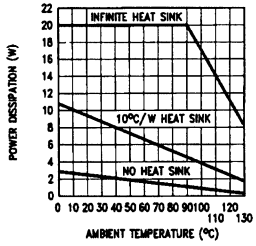
Ripple Rejection



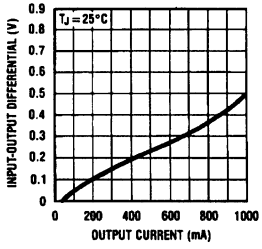
Output Impedance



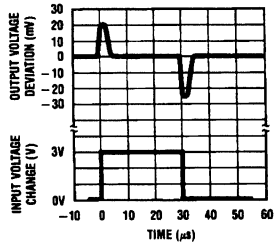
Maximum Power Dissipation (TO-220)



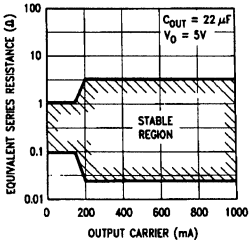
Dropout Voltage



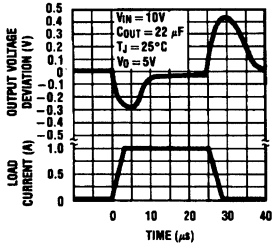
Line Transient Response



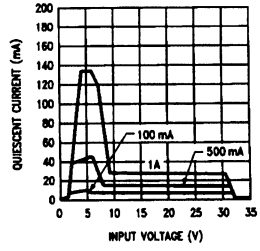
Output Capacitor ESR



Load Transient Response



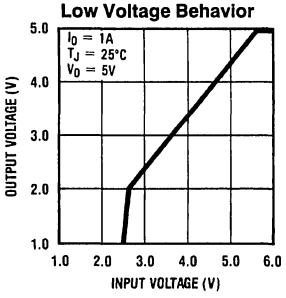
Quiescent Current



TL/H/6158–3

Typical Performance Characteristics (Continued)

Low Voltage Behavior



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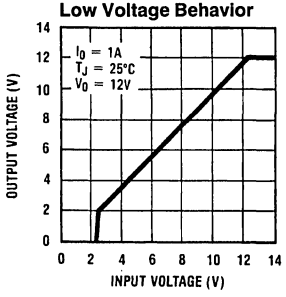
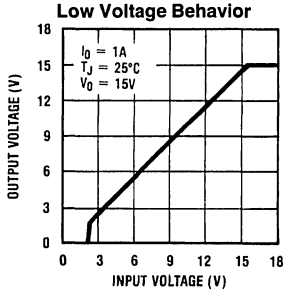
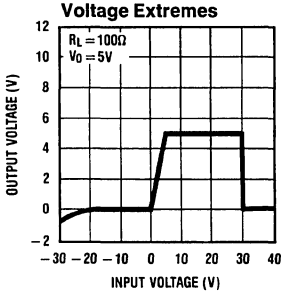


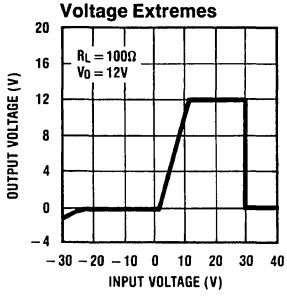
Low Voltage Behavior



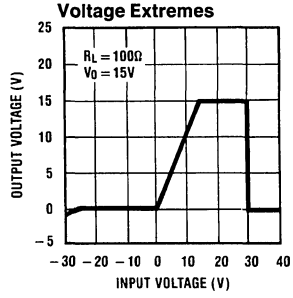
Output at Voltage Extremes



Output at Voltage Extremes



Output at Voltage Extremes



TL/H/6158–5

National Semiconductor

LM2941 1A Low Dropout Adjustable Regulator

General Description

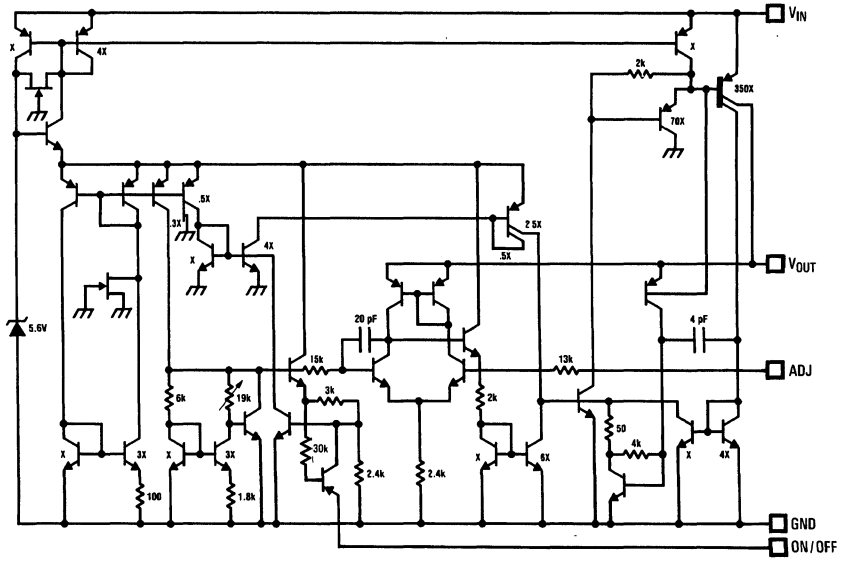
The LM2941 positive voltage regulator features the ability to source 1A of output current with a typical dropout voltage of 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

Designed also for vehicular applications, the LM2941 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as load dump (60V) when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

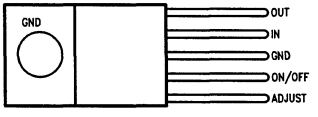
- Output voltage adjustable from 5V to 20V
- Dropout voltage typically 0.5V @ I_O = 1A
- Output current in excess of 1A
- Trimmed reference voltage
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- 100% electrical burn-in in thermal limit
- TTL, CMOS compatible ON/OFF switch

Equivalent Schematic and Connection Diagram



TL/H/8823-1

(TO-220)
Plastic Package



TL/H/8823-2

Front View
Order Number LM2941T
See NS Package Number TO5A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage
- Survival Voltage (≤ 100 ms) 60V
- Operational Voltage 26V

Internal Power Dissipation (Note 1) Internally limited

Operating Temperature Range (T_A) −40°C to +125°C

Maximum Junction Temperature 150°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 260°C

ESD susceptibility rating is to be determined.

Electrical Characteristics

5V ≤ V_O ≤ 20V, V_{IN} = V_O + 5V, C_O = 22 μF, T_J = 25°C (unless otherwise specified)

Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Reference Voltage	5 mA ≤ I_O ≤ 1A, (Note 4)	1.275	1.237 1.313	1.211 1.339	V(min) V(max)
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5 mA	4	10		mV/V(max)
Load Regulation	50 mA ≤ I_O ≤ 1A	7	10	16	mV/V(max)
Output Impedance	100 mADC and 20 mArms f_O = 120 Hz	7			mΩ/V
Quiescent Current	V_O + 2V ≤ V_{IN} < 26V, I_O = 5 mA	10	15	20	mA(max)
	V_{IN} = V_O + 5V, I_O = 1A	30	45	60	mA(max)
RMS Output Noise, % of V_{OUT}	10 Hz–100 kHz I_O = 5 mA	0.003			%
Ripple Rejection	f_O = 120 Hz, 1 Vrms, I_L = 100 mA	0.005	0.02	0.04	%/V(max)
Long Term Stability		0.4			%/1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8	1.0	V(max)
	I_O = 100 mA	110	200	200	mV(max)
Short Circuit Current	V_{IN} max = 26V (Note 5)	1.9	1.6		A(min)
Maximum Line Transient	V_O max 1V above nominal V_O R_O = 100Ω, T ≤ 100 ms	75	60	60	V(min)
Maximum Operational Input Voltage		31	26	26	V_{DC}
Reverse Polarity DC Input Voltage	R_O = 100Ω, V_O ≥ −0.6V	−30	−15	−15	V(min)
Reverse Polarity Transient Input Voltage	T ≤ 100 ms, R_O = 100Ω	−75	−50	−50	V(min)
ON/OFF Threshold Voltage ON	I_O ≤ 1A	1.30	0.80	0.80	V(max)
ON/OFF Threshold Voltage OFF	I_O ≤ 1A	1.30	2.00	2.00	V(min)
ON/OFF Threshold Current	$V_{ON/OFF}$ = 2.0V, I_O ≤ 1A	50	100	300	μA(max)

Note 1: The maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2941 will go into thermal shutdown. For the LM2941, the junction-to-ambient thermal resistance is 53°C/W, and the junction-to-case thermal resistance is 3°C/W.

Note 2: Tested Limits are guaranteed and 100% production tested.

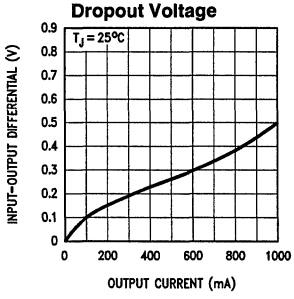
Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

Note 4: The output voltage range is 5V to 20V and is determined by the two external resistors, R1 and R2. See Typical Application Circuit.

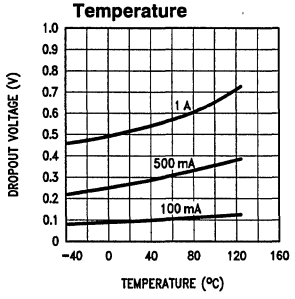
Note 5: Output current will decrease with increasing temperature, but will not go below 1A at the maximum specified temperatures.

Typical Performance Characteristics

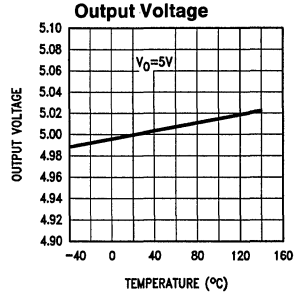
Dropout Voltage



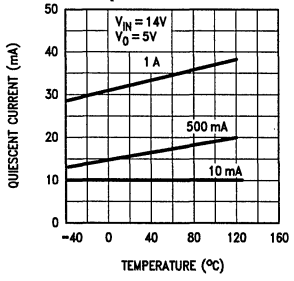
Dropout Voltage vs Temperature



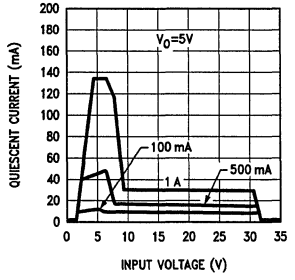
Output Voltage



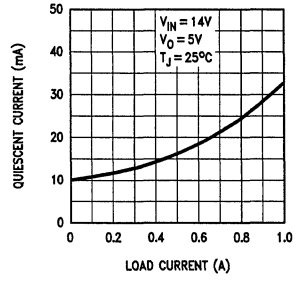
Quiescent Current vs Temperature



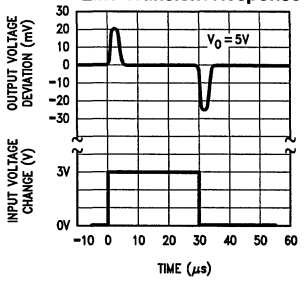
Quiescent Current



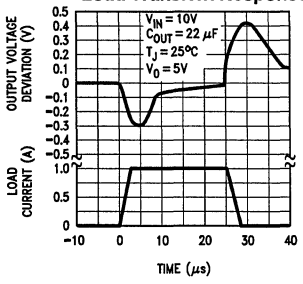
Quiescent Current



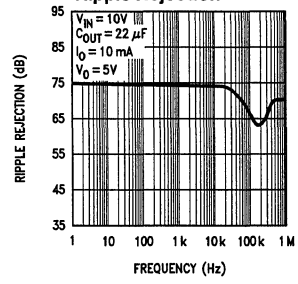
Line Transient Response



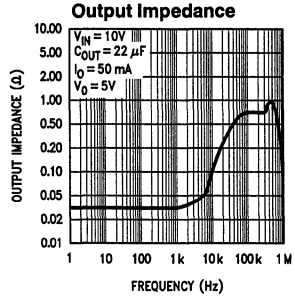
Load Transient Response



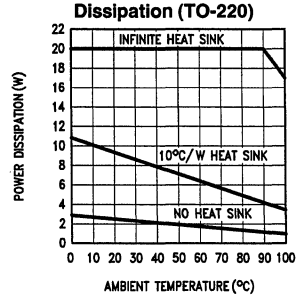
Ripple Rejection



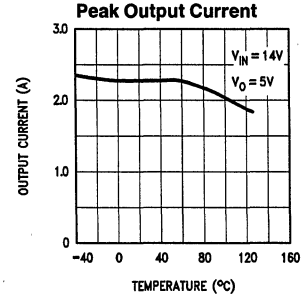
Output Impedance



Maximum Power Dissipation (TO-220)

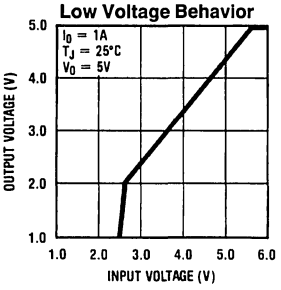


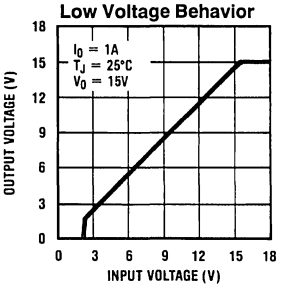
Peak Output Current

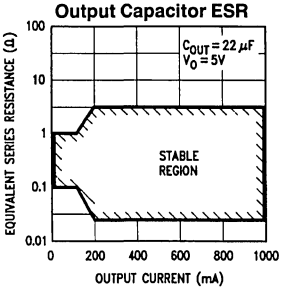


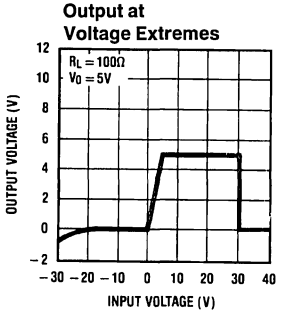
TL/H/8823–4

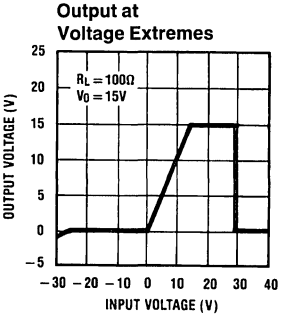
Typical Performance Characteristics (Continued)











TL/H/8823–5

Definition of Terms

Dropout Voltage: The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_{OUT} + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

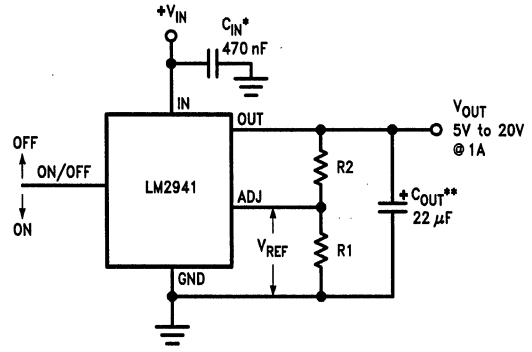
Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Typical Applications

5V to 20V Adjustable Regulator



TL/H/8823–3

V_{OUT} = Reference voltage $\times \frac{R1 + R2}{R1}$ where V_{REF} = 1.275 typical

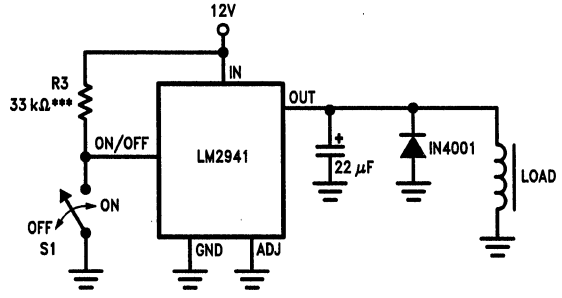
Solving for R2: $R2 = R1 \left(\frac{V_O}{V_{REF}} - 1\right)$

Note: Using 1k for R1 will ensure that the input bias current error of the adjust pin will be negligible. Do not bypass R1 or R2. This will lead to instabilities.

*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

1A Switch



TL/H/8823–6

***To assure shutdown, select Resistor R3 to guarantee at least 300 µA of pull-up current when S1 is open. (Assume 2V at the ON/OFF pin.)

National Semiconductor

LM2941C 1A Low Dropout Adjustable Regulator

General Description

The LM2941C positive voltage regulator features the ability to source 1A of output current with a typical dropout voltage of 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

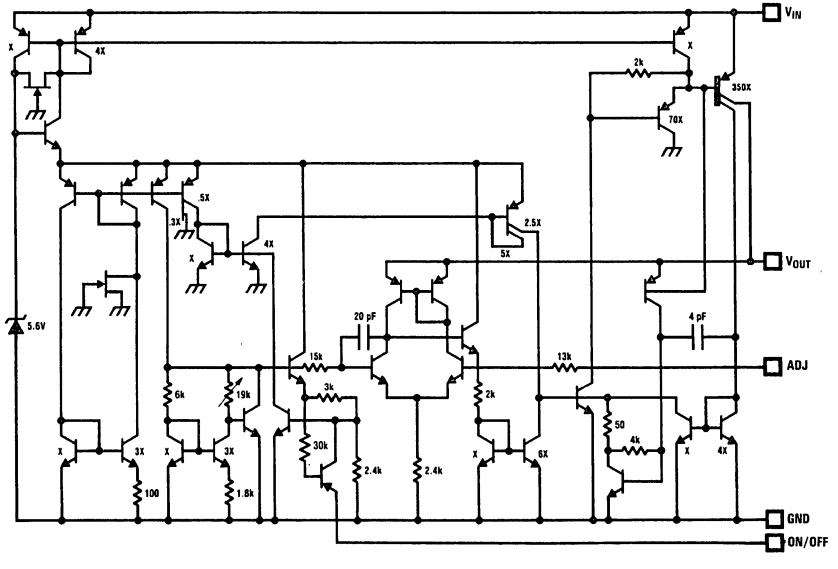
Low dropout voltage, coupled with 1A current capability, makes the LM2941C useful in applications where the input voltage is maintained at a level within one or two volts of the output voltage. Operation at these low input-output voltage differentials reduces regulator power dissipation and increases overall system efficiency.

The LM2941C can be used to provide on-board regulation and post-switcher regulation. Other applications include fault protected 1A switches.

Features

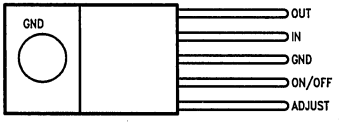
- Output voltage adjustable from 5V to 20V
- Dropout voltage typically 0.5V @ I_O = 1A
- Output current in excess of 1A
- Trimmed reference voltage
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- 100% electrical burn-in in thermal limit
- TTL, CMOS compatible ON/OFF switch

Equivalent Schematic and Connection Diagram



TL/H/10367–1

(TO-220)
Plastic Package



TL/H/10367–2

Front View
Order Number LM2941CT
See NS Package Number TO5A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Survival Voltage (≤ 100 ms)	45V
Operational Voltage	26V
Internal Power Dissipation (Note 1)	Internally limited
Operating Temperature Range (T_A)	0°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

ESD susceptibility rating is to be determined.

Electrical Characteristics

5V ≤ V_O ≤ 20V, V_{IN} = V_O + 5V, C_O = 22 μF, T_J = 25°C (unless otherwise specified)

Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Reference Voltage	5 mA ≤ I_O ≤ 1A, (Note 4)	1.275	1.237 1.313	1.211 1.339	V(min) V(max)
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5 mA	4	10		mV/V(max)
Load Regulation	50 mA ≤ I_O ≤ 1A	7	10		mV/V(max)
Output Impedance	100 mADC and 20 mArms f_O = 120 Hz	7			mΩ/V
Quiescent Current	V_O + 2V ≤ V_{IN} < 26V, I_O = 5 mA	10	15		mA(max)
	V_{IN} = V_O + 5V, I_O = 1A	30	45	60	mA(max)
RMS Output Noise, % of V_{OUT}	10 Hz–100 kHz I_O = 5 mA	0.003			%
Ripple Rejection	f_O = 120 Hz, 1 Vrms, I_L = 100 mA	0.005	0.02		%/V(max)
Long Term Stability		0.4			%/1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8	1.0	V(max)
	I_O = 100 mA	110	200	200	mV(max)
Short Circuit Current	V_{IN} max = 26V (Note 5)	1.9	1.6		A(min)
Maximum Line Transient	V_O max 1V above nominal V_O R_O = 100Ω, T ≤ 100 ms	55	45		V(min)
Maximum Operational Input Voltage		31	26		V_{DC}
Reverse Polarity DC Input Voltage	R_O = 100Ω, V_O ≥ −0.6V	−30	−15		V(min)
Reverse Polarity Transient Input Voltage	T ≤ 100 ms, R_O = 100Ω	−55	−45		V(min)
ON/OFF Threshold Voltage ON	I_O ≤ 1A	1.30	0.80		V(max)
ON/OFF Threshold Voltage OFF	I_O ≤ 1A	1.30	2.00		V(min)
ON/OFF Threshold Current	$V_{ON/OFF}$ = 2.0V I_O ≤ 1A	50	100		μA(max)

Note 1: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(max)} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2941C will go into thermal shutdown. For the LM2941C, the junction-to-ambient thermal resistance is 53°C/W, and the junction-to-case thermal resistance is 3°C/W.

Note 2: Tested Limits are guaranteed and 100% production tested.

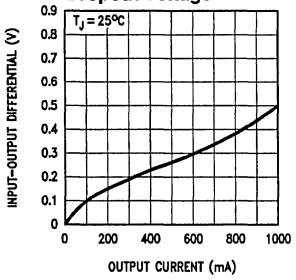
Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

Note 4: The output voltage range is 5V to 20V and is determined by the two external resistors, R1 and R2. See Typical Application Circuit.

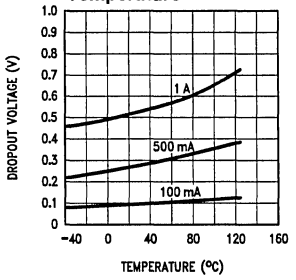
Note 5: Output current will decrease with increasing temperature, but will not go below 1A at the maximum specified temperatures.

Typical Performance Characteristics

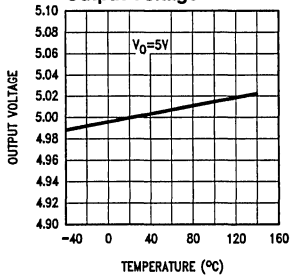
Dropout Voltage



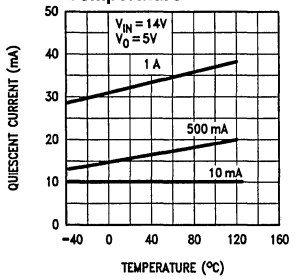
Dropout Voltage vs Temperature



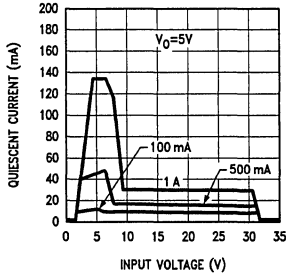
Output Voltage



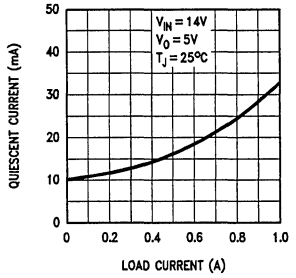
Quiescent Current vs Temperature



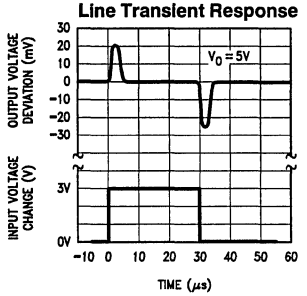
Quiescent Current



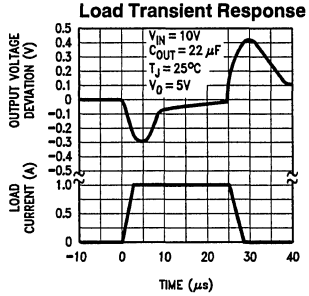
Quiescent Current



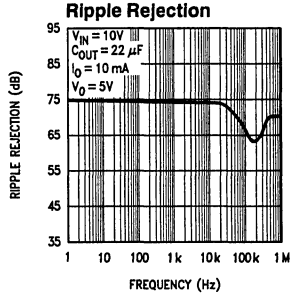
Line Transient Response



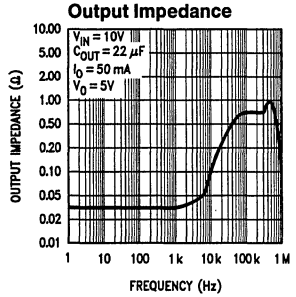
Load Transient Response



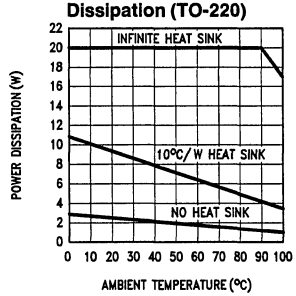
Ripple Rejection



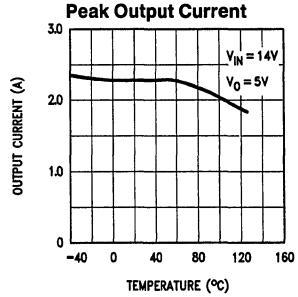
Output Impedance



Maximum Power Dissipation (TO-220)

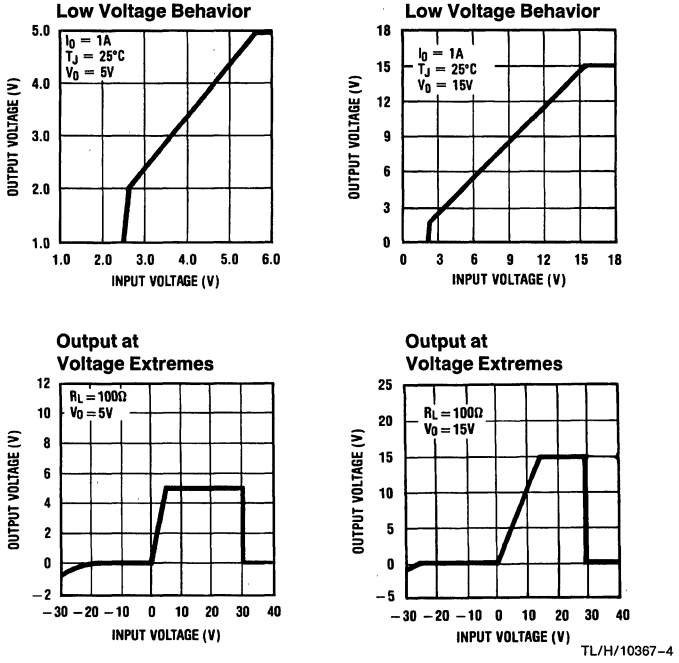


Peak Output Current



TL/H/10367–3

Typical Performance Characteristics (Continued)



TL/H/10367–4

Definition of Terms

Dropout Voltage: The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_{OUT} + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

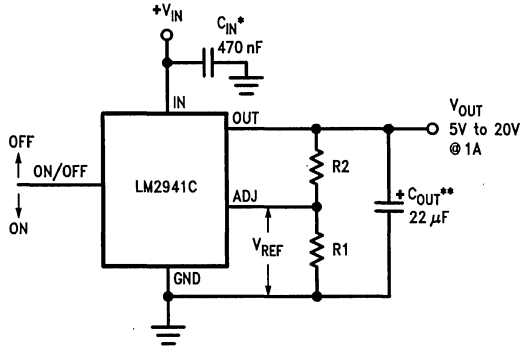
Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Typical Applications

5V to 20V Adjustable Regulator



TL/H/10367–5

$$V_{OUT} = \text{Reference voltage} \times \frac{R1 + R2}{R1} \text{ where } V_{REF} = 1.275 \text{ typical}$$

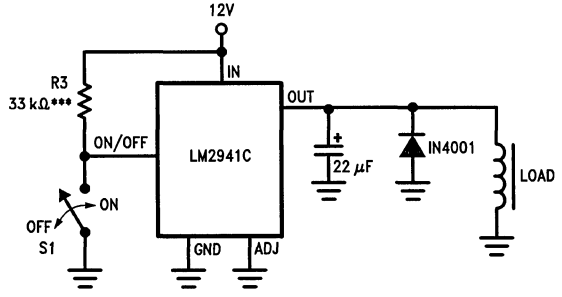
Solving for R2: $R2 = R1\left(\frac{V_O}{V_{REF}} - 1\right)$

Note: Using 1k for R1 will ensure that the input bias current error of the adjust pin will be negligible. Do not bypass R1 or R2. This will lead to instabilities.

*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and should have an ESR less than 1Ω to maintain stability.

1A Switch



TL/H/10367–6

***To assure shutdown, select resistor R3 to guarantee at least 300 µA of pull-up current when S1 is open. (Assume 2V at the ON/OFF pin.)

National Semiconductor

LM2984C Microprocessor Power Supply System

General Description

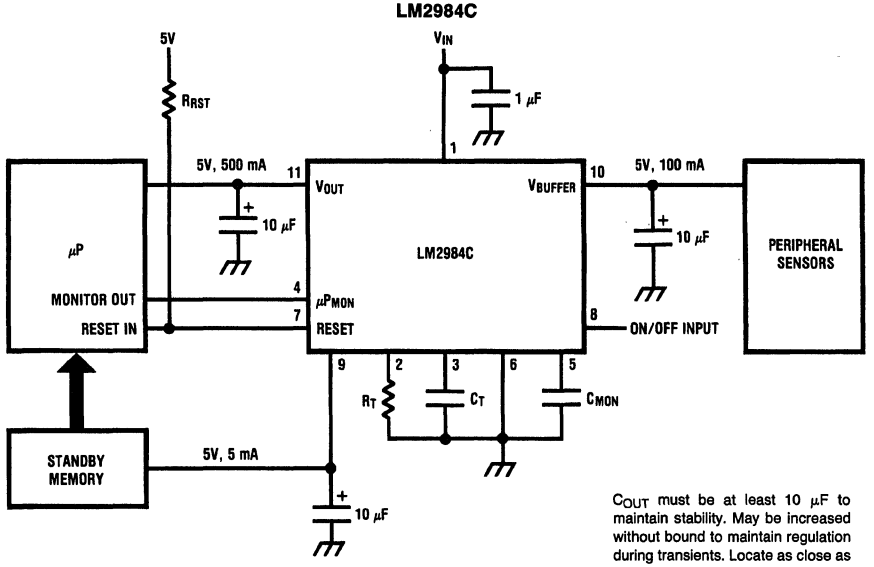
The LM2984C positive voltage regulator features three independent and tracking outputs capable of delivering the power for logic circuits, peripheral sensors and standby memory in a typical microprocessor system. The LM2984C includes circuitry which monitors both its own high-current output and also an external μP. If any error conditions are sensed in either, a reset error flag is set and maintained until the malfunction terminates. Since these functions are included in the same package with the three regulators, a great saving in board space can be realized in the typical microprocessor system. The LM2984C also features very low dropout voltages on each of its three regulator outputs (0.6V at the rated output current). Furthermore, the quiescent current can be reduced to 1 mA in the standby mode.

Designed also for vehicular applications, the LM2984C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. Familiar regulator features such as short circuit and thermal overload protection are also provided. Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Three low dropout tracking regulators
- Output current in excess of 500 mA
- Low quiescent current standby regulator
- Microprocessor malfunction RESET flag
- Delayed RESET on power-up
- Accurate pretrimmed 5V outputs
- Reverse battery protection
- Overvoltage protection
- Reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current outputs
- 100% electrical burn-in in thermal limit

Typical Application Circuit



Order Number LM2984CT
See NS Package Number TA11B

C_{OUT} must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

TL/H/8821–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage
- Survival Voltage (<100 ms) 35V
- Operational Voltage 26V

Internal Power Dissipation	Internally Limited
Operating Temperature Range (T_A)	0°C to +125°C
Maximum Junction Temperature (Note 1)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	230°C

ESD rating is to be determined.

Electrical Characteristics

V_{IN} = 14V, I_{OUT} = 5 mA, C_{OUT} = 10 μF, T_j = 25°C (Note 6) unless otherwise indicated

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
V_{OUT} (Pin 11)					
Output Voltage	5 mA ≤ I_o ≤ 500 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85 5.15	4.75 5.25	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25		mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50		mV_{max}
Load Regulation	5 mA ≤ I_{OUT} ≤ 500 mA	12	50		mV_{max}
Output Impedance	250 mA_{dc} and 10 mA_{rms}, f_o = 120 Hz	24			mΩ
Quiescent Current	I_{OUT} = 500 mA	38	100		mA_{max}
	I_{OUT} = 250 mA	14	50		mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100			μV
Long Term Stability		20			mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60		dB_{min}
Dropout Voltage	I_{OUT} = 500 mA	0.53	0.80	1.00	V_{max}
	I_{OUT} = 250 mA	0.28	0.50	0.60	V_{max}
Current Limit		0.92	0.75		A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26	26	V_{min}
Maximum Line Transient	V_{OUT} ≤ 6V, R_{OUT} = 100Ω	45	35	35	V_{min}
Reverse Polarity Input Voltage DC	V_{OUT} ≥ −0.6V, R_{OUT} = 100Ω	−30	−15	−15	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{OUT} = 100Ω	−55	−35	−35	V_{min}

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{buf} = 5 mA, C_{buf} = 10 μF, T_j = 25°C (Note 6) unless otherwise indicated

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
V_{buffer} (Pin 10)					
Output Voltage	5 mA ≤ I_o ≤ 100 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85 5.15	4.75 5.25	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25		mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50		mV_{max}
Load Regulation	5 mA ≤ I_{buf} ≤ 100 mA	15	50		mV_{max}
Output Impedance	50 mA_{dc} and 10 mA_{rms},	200			mΩ
Quiescent Current	I_{buf} = 100 mA	8.0	15.0		mA_{max}
Output Noise Voltage	10 Hz–100 kHz, I_{OUT} = 100 mA	100			μV
Long Term Stability		20			mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60		dB_{min}
Dropout Voltage	I_{buf} = 100 mA	0.35	0.50	0.60	V_{max}
Current Limit		0.23	0.15		A_{min}
Maximum Operational Input Voltage	Continuous DC	32	26	26	V_{min}
Maximum Line Transient	V_{buf} ≤ 6V, R_{buf} = 100Ω	45	35	35	V_{min}
Reverse Polarity Input Voltage DC	V_{buf} ≥ −0.6V, R_{buf} = 100Ω	−30	−15	−15	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{buf} = 100Ω	−55	−35	−35	V_{min}

Electrical Characteristics

V_{IN} = 14V, I_{stby} = 1 mA, C_{stby} = 10 μF, T_j = 25°C (Note 6) unless otherwise indicated

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
$V_{standby}$ (Pin 9)					
Output Voltage	1 mA ≤ I_o ≤ 7.5 mA 6V ≤ V_{IN} ≤ 26V	5.00	4.85 5.15	4.75 5.25	V_{min} V_{max}
Line Regulation	9V ≤ V_{IN} ≤ 16V	2	25		mV_{max}
	7V ≤ V_{IN} ≤ 26V	5	50		mV_{max}
Load Regulation	0.5 mA ≤ I_{stby} ≤ 7.5 mA	6	50		mV_{max}
Output Impedance	5 mA_{dc} and 1 mA_{rms}, f_o = 120 Hz	0.9			Ω
Quiescent Current	I_{stby} = 7.5 mA	1.2	2.0		mA_{max}
	I_{stby} = 2 mA	0.9	1.5		mA_{max}

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{stby} = 1 mA, C_{stby} = 10 μF, T_j = 25°C (Note 6) unless otherwise indicated

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
$V_{standby}$ (Continued)					
Output Noise Voltage	10 Hz–100 kHz, I_{stby} = 1 mA	100			μV
Long Term Stability		20			mV/1000 hr
Ripple Rejection	f_o = 120 Hz	70	60		dB_{min}
Dropout Voltage	I_{stby} = 1 mA	0.26	0.50	0.50	V_{max}
Dropout Voltage	I_{stby} = 7.5 mA	0.38	0.60	0.70	V_{max}
Current Limit		15	12		mA_{min}
Maximum Operational Input Voltage	4.5V ≤ V_{stby} ≤ 6V R_{stby} = 1000Ω	45	35	35	V_{min}
Maximum Line Transient	V_{stby} ≤ 6V, R_{stby} = 1000Ω	45	35	35	V_{min}
Reverse Polarity Input Voltage DC	V_{stby} ≥ −0.6V, R_{stby} = 1000Ω	−30	−15	−15	V_{min}
Reverse Polarity Input Voltage Transient	T ≤ 100 ms, R_{stby} = 1000Ω	−55	−35	−35	V_{min}

Electrical Characteristics

V_{IN} = 14V, T_j = 25°C (Note 6) C_{OUT} = 10 μF, C_{buf} = 10 μF, C_{stby} = 10 μF unless otherwise specified

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Tracking and Isolation					
Tracking V_{OUT}–V_{stby}	I_{OUT} ≤ 500 mA, I_{buf} = 5 mA, I_{stby} ≤ 7.5 mA	±30	±100		mV_{max}
Tracking V_{buf}–V_{stby}	I_{OUT} = 5 mA, I_{buf} ≤ 100 mA, I_{stby} ≤ 7.5 mA	±30	±100		mV_{max}
Tracking V_{OUT}–V_{buf}	I_{OUT} ≤ 500 mA, I_{buf} ≤ 100 mA, I_{stby} = 1 mA	±30	±100		mV_{max}
Isolation* V_{buf} from V_{OUT}	R_{OUT} = 1Ω, I_{buf} ≤ 100 mA	5.00	4.50 5.50		V_{min} V_{max}
Isolation* V_{stby} from V_{OUT}	R_{OUT} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50 5.50		V_{min} V_{max}
Isolation* V_{OUT} from V_{buf}	R_{buf} = 1Ω, I_{OUT} ≤ 500 mA	5.00	4.50 5.50		V_{min} V_{max}
Isolation* V_{stby} from V_{buf}	R_{buf} = 1Ω, I_{stby} ≤ 7.5 mA	5.00	4.50 5.50		V_{min} V_{max}

*Isolation refers to the ability of the specified output to remain within the tested limits when the other output is shorted to ground.

Electrical Characteristics (Continued)

V_{IN} = 14V, I_{OUT} = 5 mA, I_{buf} = 5 mA, I_{stby} = 5 mA, R_t = 130k, C_t = 0.33 μF, C_{mon} = 0.47 μF, T_j = 25°C (Note 6) unless otherwise specified

Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Computer Monitor/Reset Functions					
I_{reset} Low	V_{IN} = 4V, V_{rst} = 0.4V	5	2	1	mA_{min}
V_{reset} Low	V_{IN} = 4V, I_{rst} = 1 mA	0.10	0.40		V_{max}
R_t voltage	(Pin 2)	1.22	1.15		V_{min}
		1.22	1.30		V_{max}
Power On Reset Delay	$V\mu P_{mon}$ = 5V (T_{dly} = 1.2 R_t C_t)	50	45		ms_{min}
		50	55		ms_{max}
V_{OUT} Low Reset Threshold	(Note 4)	4.00	3.60		V_{min}
		4.00	4.40		V_{max}
V_{OUT} High Reset Threshold	(Note 4)	5.50	5.25		V_{min}
		5.50	6.00		V_{max}
Reset Output Leakage	$V\mu P_{mon}$ = 5V, V_{rst} = 12V	0.01	1		μA_{max}
μP_{mon} Input Current (Pin 4)	$V\mu P_{mon}$ = 2.4V	7.5	25		μA_{max}
	$V\mu P_{mon}$ = 0.4V	0.01	10		μA_{max}
μP_{mon} Input Threshold Voltage		1.22	0.80	0.80	V_{min}
		1.22	2.00	2.00	V_{max}
μP Monitor Reset Oscillator Period	$V\mu P_{mon}$ = 0V (T_{window} = 0.82 $R_t C_{mon}$)	50	45		ms_{min}
		50	55		ms_{max}
μP Monitor Reset Oscillator Pulse Width	$V\mu P_{mon}$ = 0V ($RESET_{pw}$ = 2000 C_{mon})	1.0	0.7	0.5	ms_{min}
		1.0	1.3	2.0	ms_{max}
Minimum μP Monitor Input Pulse Width	(Note 5)	2			μs_{max}
Reset Fall Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.20	1.00		μs_{max}
Reset Rise Time	R_{rst} = 10k, V_{rst} = 5V, C_{rst} ≤ 10 pF	0.60	1.00		μs_{max}
On/Off Switch Input Current (Pin 8)	V_{ON} = 2.4V	7.5	25		μA_{max}
	V_{ON} = 0.4V	0.01	10		μA_{max}
On/Off Switch Input Threshold Voltage		1.22	0.80	0.80	V_{min}
		1.22	2.00	2.00	V_{max}

Note 1: Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 40°C/W.

Note 2: Tested Limits are guaranteed and 100% production tested.

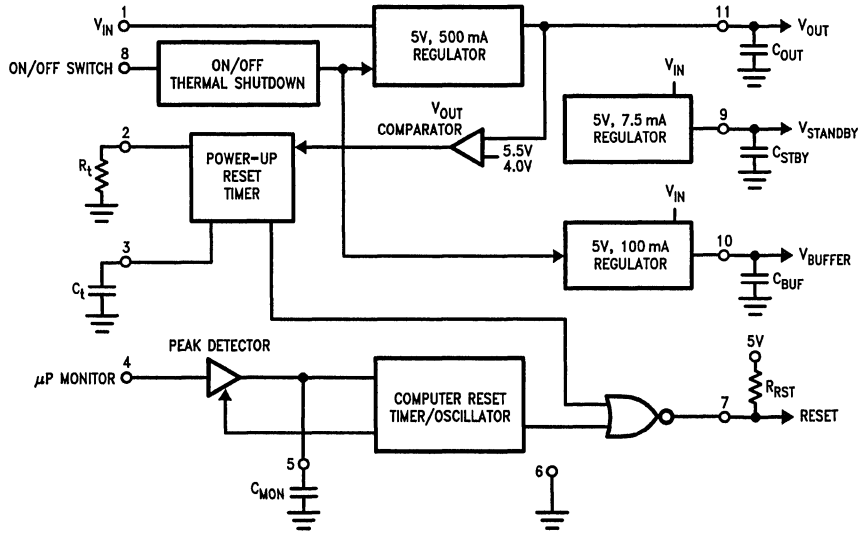
Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

Note 4: An internal comparator detects when the main regulator output (V_{OUT}) drops below 4.0V or rises above 5.5V. If either condition exists at the output, the Reset Error Flag is held low until the error condition has terminated. The Reset Error Flag is then allowed to go high again after a delay set by R_t and C_t. (See Applications Section.)

Note 5: This parameter is a measure of how short a pulse can be detected at the μP Monitor Input. This parameter is primarily influenced by the value of C_{mon}. (See Typical Performance Characteristics and Applications Section.)

Note 6: To ensure constant junction temperature, low duty cycle pulse testing is used.

Block Diagram



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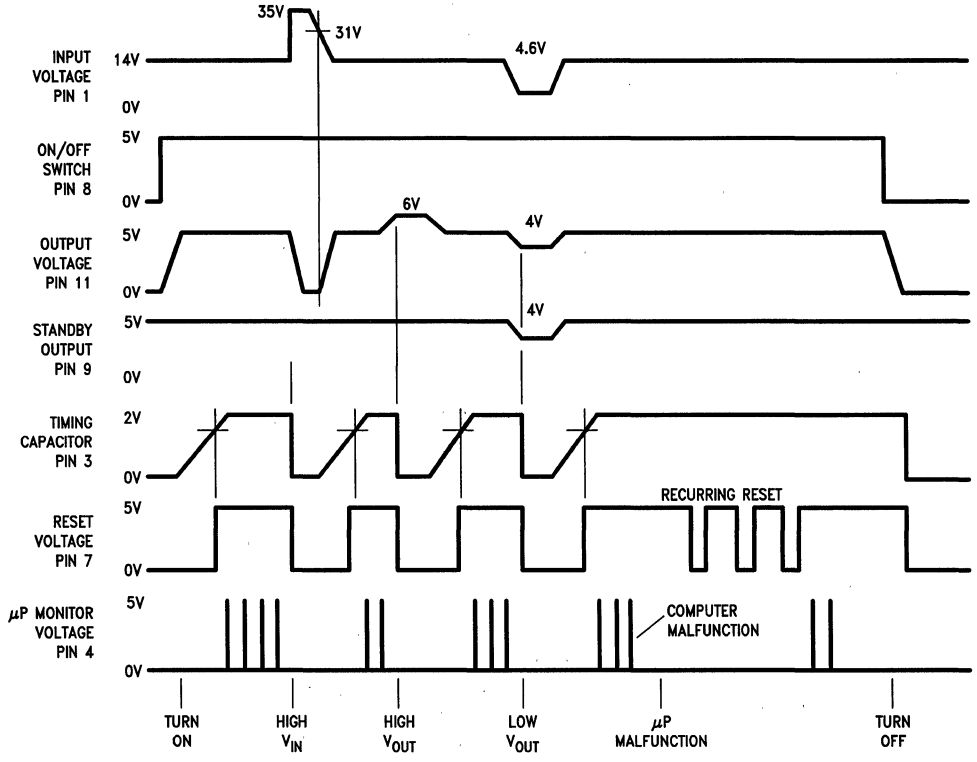
Pin Description

Pin No.	Pin Name	Comments
1	V_{IN}	Positive supply input voltage
2	R_t	Sets internal timing currents
3	C_t	Sets power-up reset delay timing
4	μP_{mon}	Microcomputer monitor input
5	C_{mon}	Sets μC monitor timing
6	Ground	Regulator ground
7	Reset	Reset error flag output
8	ON/OFF	Enables/disables high current regulators
9	$V_{standby}$	Standby regulator output (7.5 mA)
10	V_{buffer}	Buffer regulator output (100 mA)
11	V_{OUT}	Main regulator output (500 mA)

External Components

Component	Typical Value	Component Range	Comments
C_{IN}	1 μF	0.47 μF–10 μF	Required if device is located far from power supply filter.
R_t	130k	24k–1.2M	Sets internal timing currents.
C_t	0.33 μF	0.033 μF–3.3 μF	Sets power-up reset delay.
C_{tc}	0.01 μF	0.001 μF–0.1 μF	Establishes time constant of AC coupled computer monitor.
R_{tc}	10k	1k–100k	Establishes time constant of AC coupled computer monitor. (See applications section.)
C_{mon}	0.47 μF	0.047 μF–4.7 μF	Sets time window for computer monitor. Also determines period and pulse width of computer malfunction reset. (See applications section.)
R_{rst}	10k	5k–100k	Load for open collector reset output. Determined by computer reset input requirements.
C_{stby}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{buf}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.
C_{OUT}	10 μF	10 μF–no bound	A 10 μF is required for stability but larger values can be used to maintain regulation during transient conditions.

Typical Circuit Waveforms



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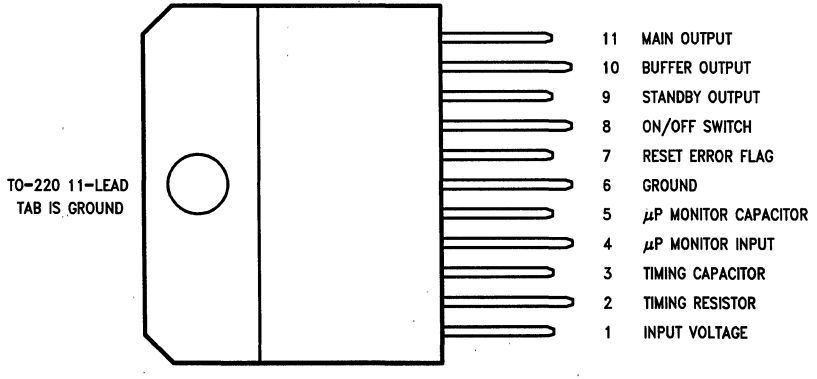
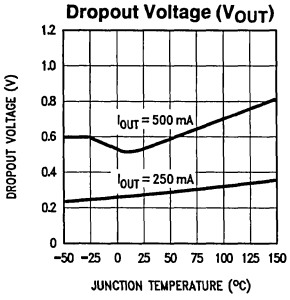
Connection Diagram

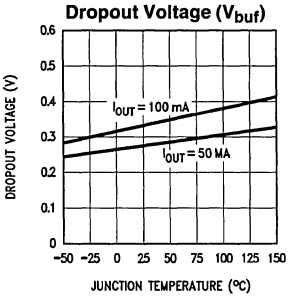


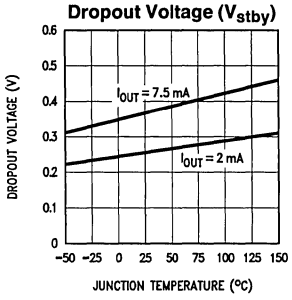
TL/H/8821–4

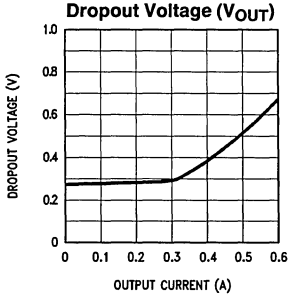
Order Number LM2984CT
See NS Package Number TA11B

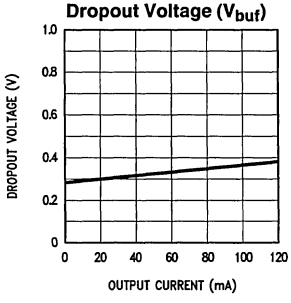
Typical Performance Characteristics

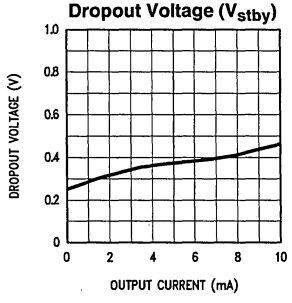


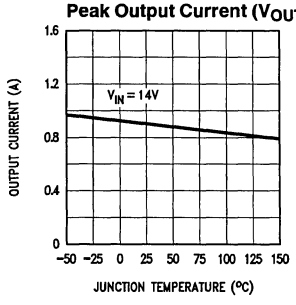


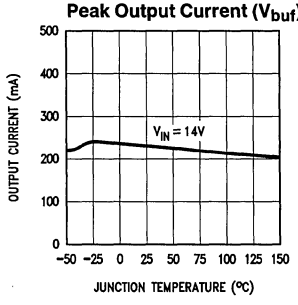


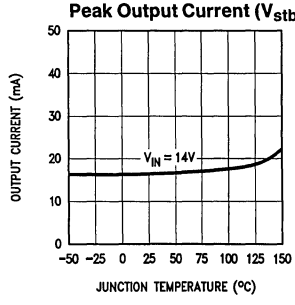


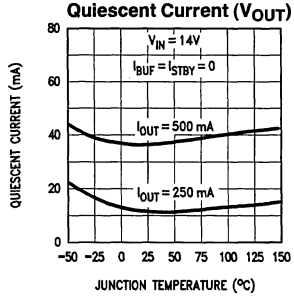


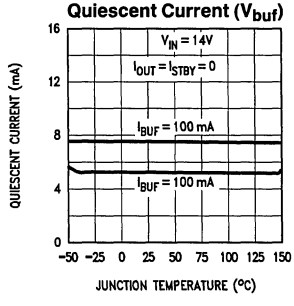


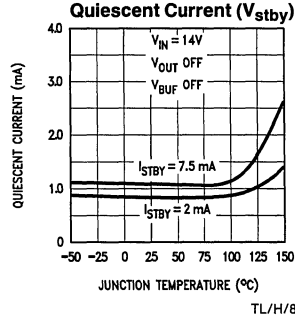












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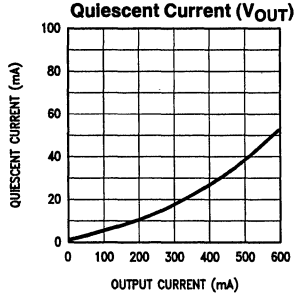
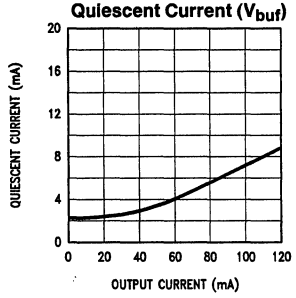
Typical Performance Characteristics (Continued)

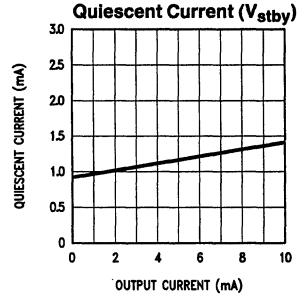
Quiescent Current (V_{OUT})



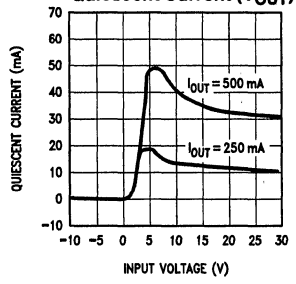
Quiescent Current (V_{buf})



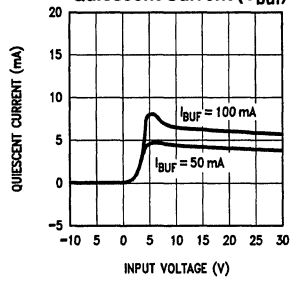
Quiescent Current (V_{stby})



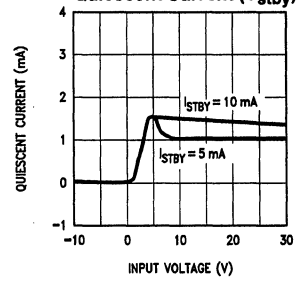
Quiescent Current (V_{OUT})



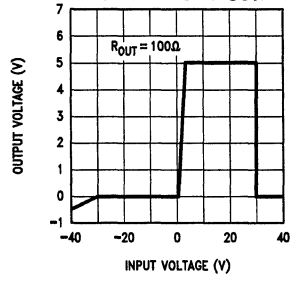
Quiescent Current (V_{buf})



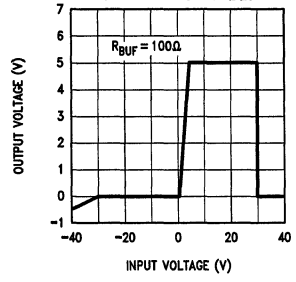
Quiescent Current (V_{stby})



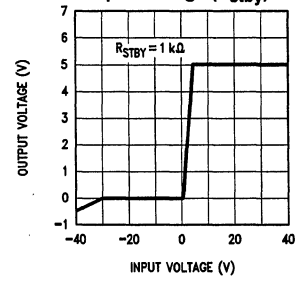
Output Voltage (V_{OUT})



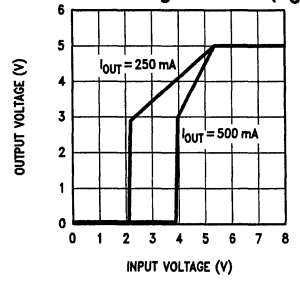
Output Voltage (V_{buf})



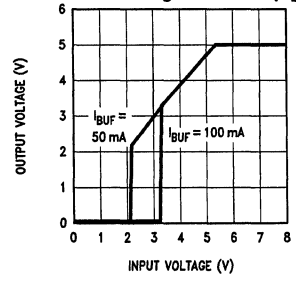
Output Voltage (V_{stby})



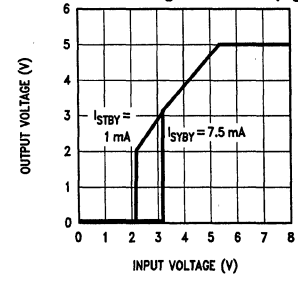
Low Voltage Behavior (V_{OUT})



Low Voltage Behavior (V_{buf})



Low Voltage Behavior (V_{stby})



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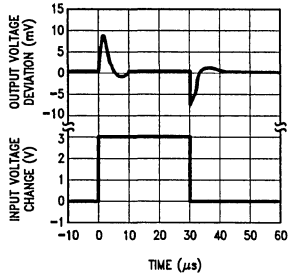
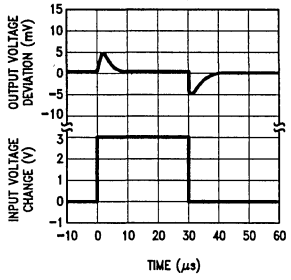
Typical Performance Characteristics (Continued)

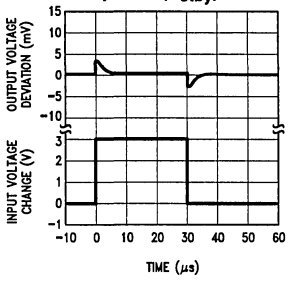
Line Transient Response (V_{OUT})



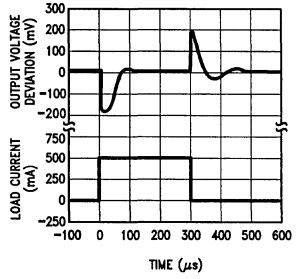
Line Transient Response (V_{buf})



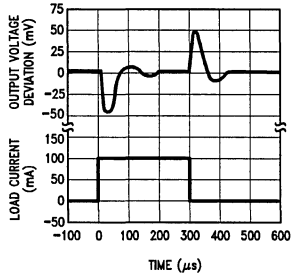
Line Transient Response (V_{stby})



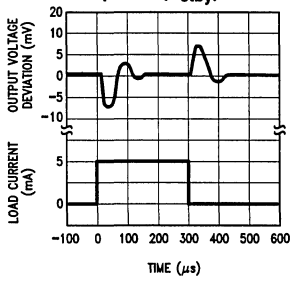
Load Transient Response (V_{OUT})



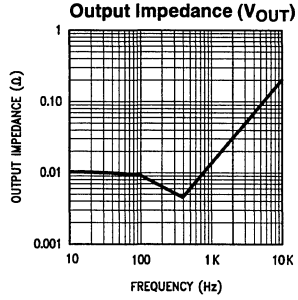
Load Transient Response (V_{buf})



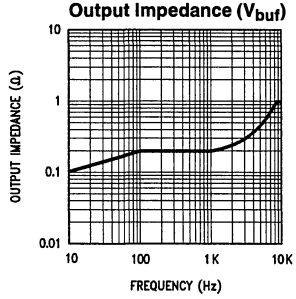
Load Transient Response (V_{stby})



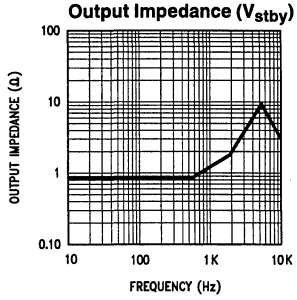
Output Impedance (V_{OUT})



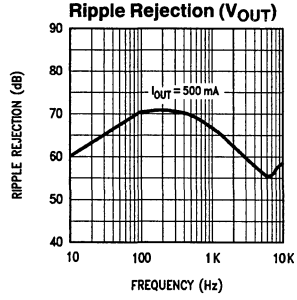
Output Impedance (V_{buf})



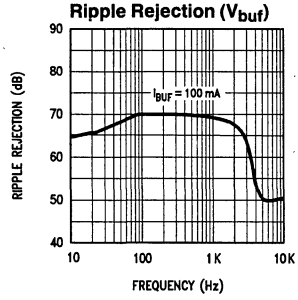
Output Impedance (V_{stby})



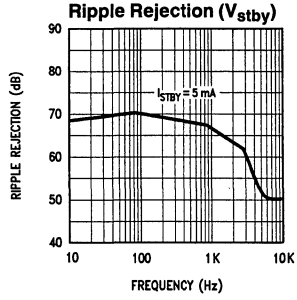
Ripple Rejection (V_{OUT})



Ripple Rejection (V_{buf})



Ripple Rejection (V_{stby})



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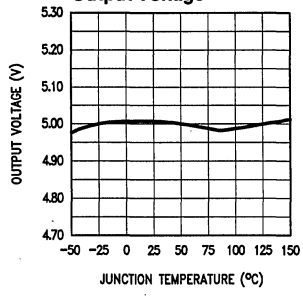
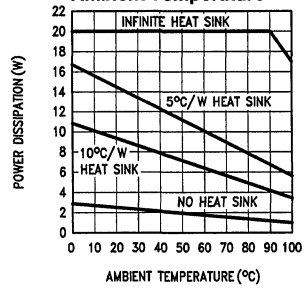
Typical Performance Characteristics (Continued)

Output Voltage



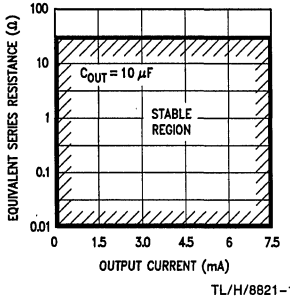
TL/H/8821–8

Device Dissipation vs Ambient Temperature



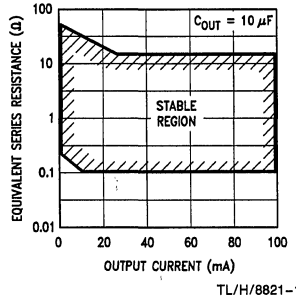
TL/H/8821–9

Output Capacitor ESR (Standby Output, Pin 9)



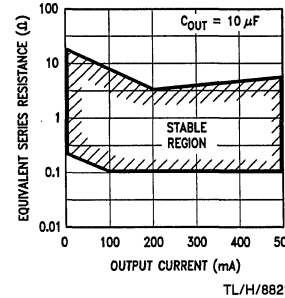
TL/H/8821–13

Output Capacitor ESR (Buffer Output, Pin 10)



TL/H/8821–14

Output Capacitor ESR (Main Output, Pin 11)



TL/H/8821–15

Application Hints

OUTPUT CAPACITORS

The LM2984C output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10 µF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also affects the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst case is usually determined at the minimum ambient temperature and the maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

Each output **must** be terminated by a capacitor, even if it is not used.

STANDBY OUTPUT

The standby output is intended for use in systems requiring standby memory circuits. While the high current regulator outputs are controlled with the ON/OFF pin described later, the standby output remains on under all conditions as long as sufficient input voltage is supplied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<1.5 mA) when the other regulator outputs are off.

The capacitor on the output of this regulator can be increased without bound. This will help maintain the output voltage during negative input transients and will also help to reduce the noise on all three outputs. Because the other two track the standby output: therefore any noise reduction here will also reduce the other two noise voltages.

BUFFER OUTPUT

The buffer output is designed to drive peripheral sensor circuitry in a µP system. It will track the standby and main regulator within a few millivolts in normal operation. Therefore, a peripheral sensor can be powered off this supply and have the same operating voltage as the µP system. This is important if a ratiometric sensor system is being used.

The buffer output can be short circuited while the other two outputs are in normal operation. This protects the µP system from disruption of power when a sensor wire, etc. is temporarily shorted to ground, i.e. only the sensor signal would be interrupted, while the µP and memory circuits would remain operational.

The buffer output is similar to the main output in that it is controlled by the ON/OFF switch in order to save power in

Application Hints (Continued)

the standby mode. It is also fault protected against overvoltage and thermal overload. If the input voltage rises above approximately 30V (e.g. load dump), this output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is necessary since this output is one of the dominant sources of power dissipation in the IC.

MAIN OUTPUT

The main output is designed to power relatively large loads, i.e. approximately 500 mA. It is therefore also protected against overvoltage and thermal overload.

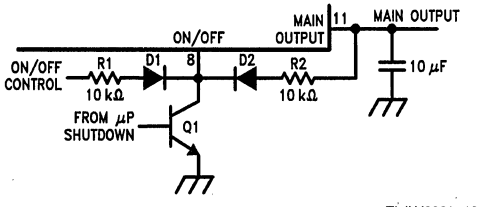
This output will track the other two within a few millivolts in normal operation. It can therefore be used as a reference voltage for any signal derived from circuitry powered off the standby or buffer outputs. This is important in a ratiometric sensor system or any system requiring accurate matching of power supply voltages.

ON/OFF SWITCH

The ON/OFF switch controls the main output and the buffer output. The threshold voltage is compatible with most logic families and has about 20 mV of hysteresis to insure 'clean' switching from the standby mode to the active mode and vice versa. This pin can be tied to the input voltage through a 10 kΩ resistor if the regulator is to be powered continuously.

POWER DOWN OVERRIDE

Another possible approach is to use a diode in series with the ON/OFF signal and another in series with the main output in order to maintain power for some period of time after the ON/OFF signal has been removed (see *Figure 1*). When the ON/OFF switch is initially pulled high through diode D1, the main output will turn on and supply power through diode D2 to the ON/OFF switch effectively latching the main output. An open collector transistor Q1 is connected to the ON/OFF pin along with the two diodes and forces the regulators off after a period of time determined by the μP. In this way, the μP can override a power down command and store data, do housekeeping, etc. before reverting back to the standby mode.



TL/H/8821–10

FIGURE 1. Power Down Override

RESET OUTPUT

This output is an open collector NPN transistor which is forced low whenever an error condition is present at the main output or when a μP error is sensed (see μP Monitor section). If the main output voltage drops below 4V or rises above 5.5V, the RESET output is forced low and held low for a period of time set by two external components, R_t and C_t. There is a slight amount of hysteresis in these two threshold voltages so that the RESET output has a fast rise and fall time compatible with the requirements of most μP RESET inputs.

DELAYED RESET

Resistor R_t and capacitor C_t set the period of time that the RESET output is held low after a main output error condition has been sensed. The delay is given by the formula:

$$T_{dly} = 1.2\ R_tC_t \text{ (seconds)}$$

The delayed RESET will be initiated any time the main output is outside the 4V to 5.5V window, i.e. during power-up, short circuit, overvoltage, low line, thermal shutdown or power-down. The μP is therefore RESET whenever the output voltage is out of regulation. (It is important to note that a RESET is only initiated when the main output is in error. The buffer and standby outputs are not directly monitored for error conditions.)

μP MONITOR RESET

There are two distinct and independent error monitoring systems in the LM2984C. The one described above monitors the main regulator output and initiates a delayed RESET whenever this output is in error. The other error monitoring system is the μP watchdog. These two systems are OR'd together internally and both force the RESET output low when either type of error occurs.

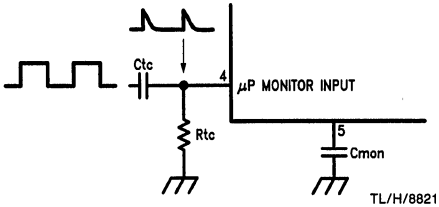
This watchdog circuitry continuously monitors a pin on the μP that generates a positive going pulse during normal operation. The period of this pulse is typically on the order of milliseconds and the pulse width is typically on the order of 10's of microseconds. If this pulse ever disappears, the watchdog circuitry will time out and a RESET low will be sent to the μP. The time out period is determined by two external components, R_t and C_{mon}, according to the formula:

$$T_{window} = 0.82\ R_tC_{mon} \text{ (seconds)}$$

The width of the RESET pulse is set by C_{mon} and an internal resistor according to the following:

$$RESET_{pw} = 2000\ C_{mon} \text{ (seconds)}$$

A square wave signal can also be monitored for errors by filtering the C_{mon} input such that only the positive edges of the signal are detected. *Figure 2* is a schematic diagram of a typical circuit used to differentiate the input signal. Resistor R_{tc} and capacitor C_{tc} pass only the rising edge of the square wave and create a short positive pulse suitable for the μP monitor input. If the incoming signal continues in a high state or in a low state for too long a period of time, a RESET low will be generated.



TL/H/8821–11

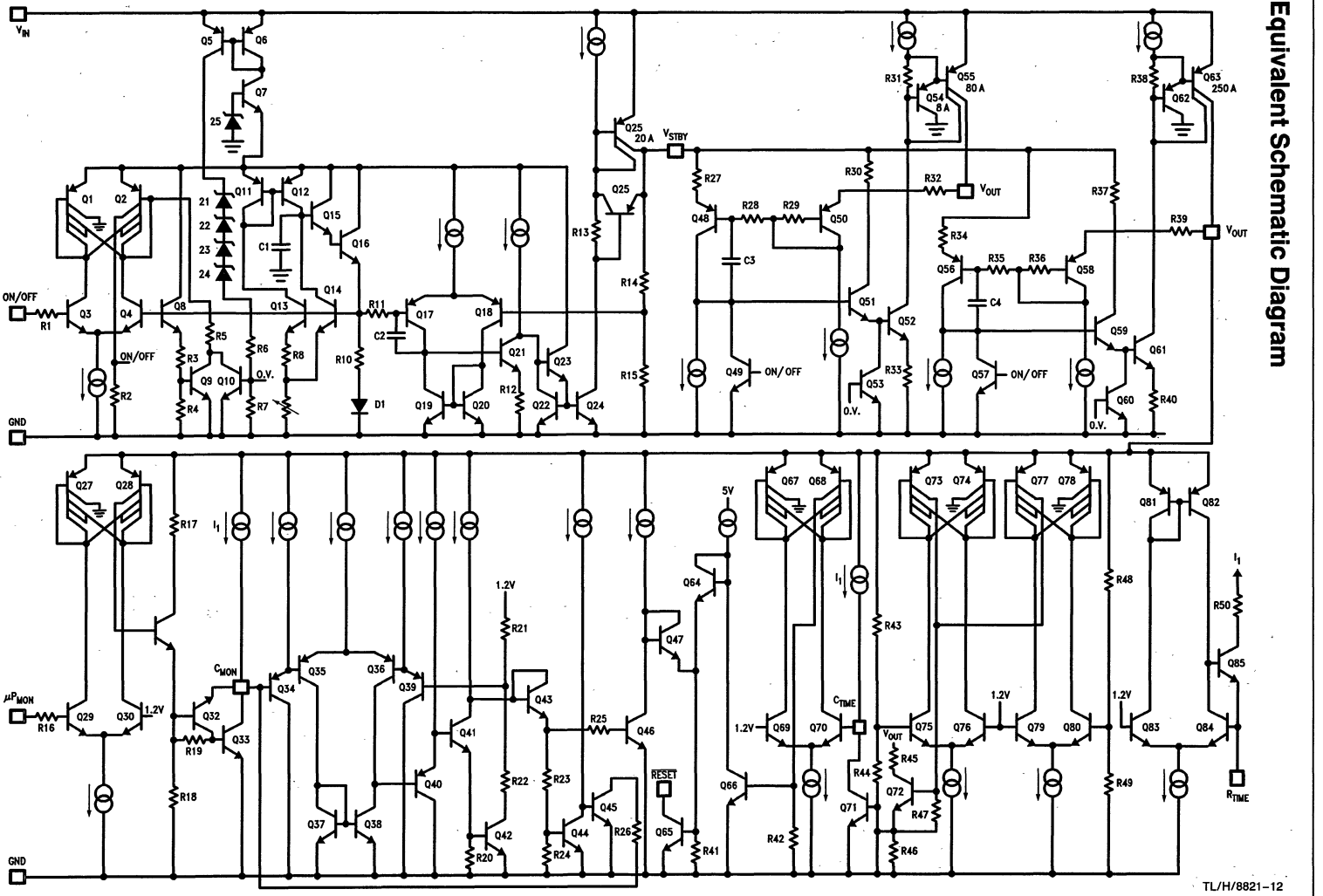
FIGURE 2. Monitoring Square Wave μP Signals

The threshold voltage and input characteristics of this pin are compatible with nearly all logic families.

There is a limit on the width of a pulse that can be reliably detected by the watchdog circuit. This is due to the output resistance of the transistor which discharges C_{mon} when a high state is detected at the input. The minimum detectable pulse width can be determined by the following formula:

$$PW_{min} = 20\ C_{mon} \text{ (seconds)}$$

Equivalent Schematic Diagram



National Semiconductor

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and mininize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

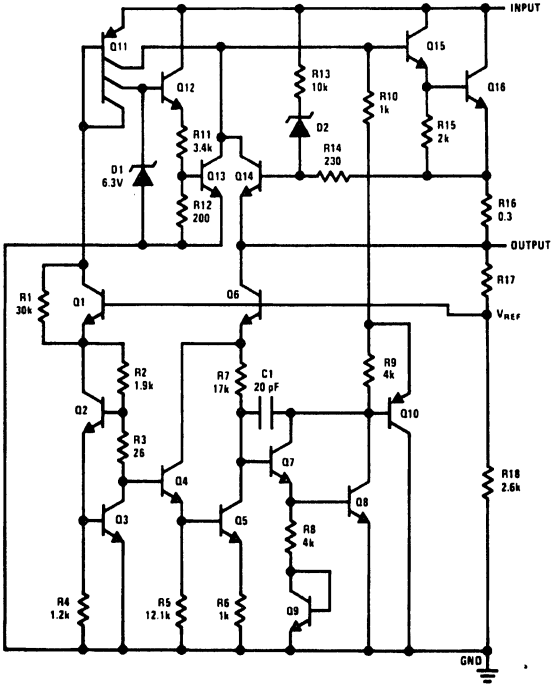
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

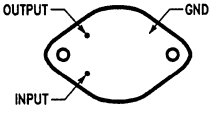
LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



TL/H/7746–1

Metal Can Package
TO-3 (K)
Aluminum

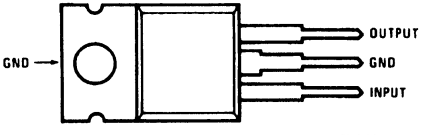


TL/H/7746–2

Bottom View

Order Number LM7805CK, LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



TL/H/7746–3

Top View

Order Number LM7805CT, LM7812CT or LM7815CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

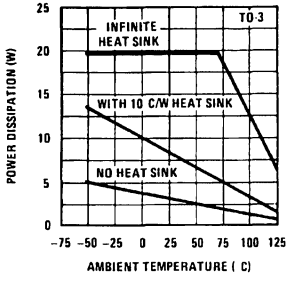
Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A	Tj = 25°C			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
			0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA	62			55			54			dB
			0°C ≤ Tj ≤ +125°C										
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	Tj = 25°C			2.1			1.5			1.2		A
	Peak Output Current	Tj = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ Tj ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O ≤ 1A			7.5		14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

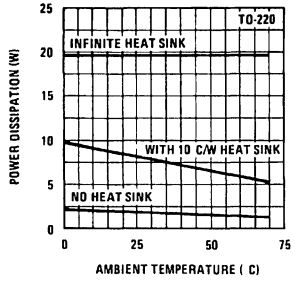
Note 2: All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

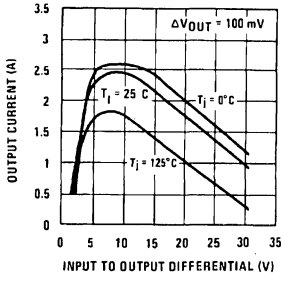
Maximum Average Power Dissipation



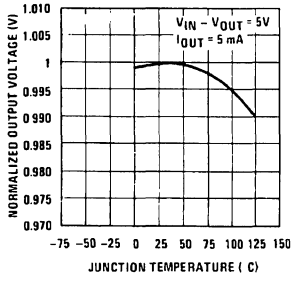
Maximum Average Power Dissipation



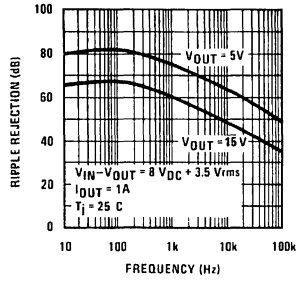
Peak Output Current



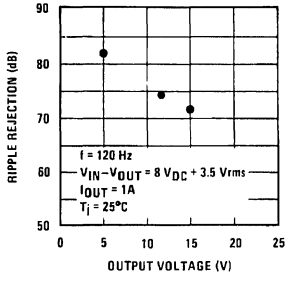
Output Voltage (Normalized to 1V at Tj = 25°C)



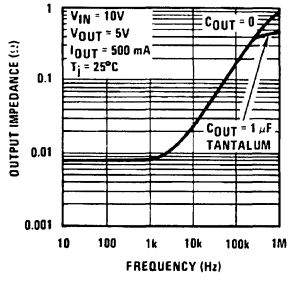
Ripple Rejection



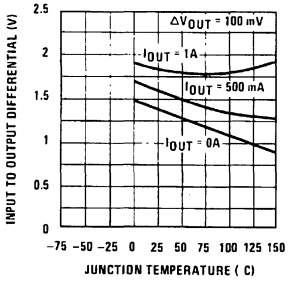
Ripple Rejection



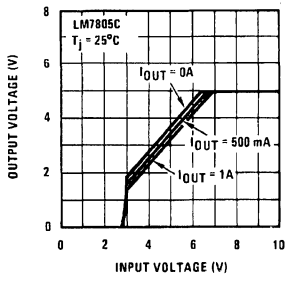
Output Impedance



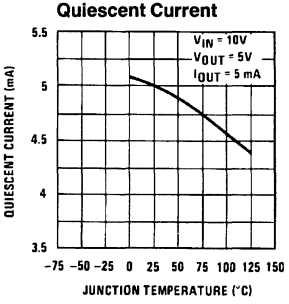
Dropout Voltage



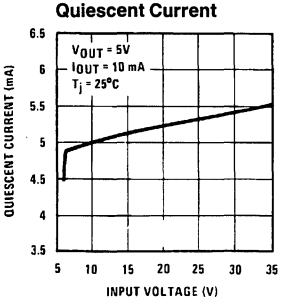
Dropout Characteristics



Quiescent Current



Quiescent Current



TL/H/7746–4

National Semiconductor

LM7800 Series
3-Terminal Positive Voltage Regulators

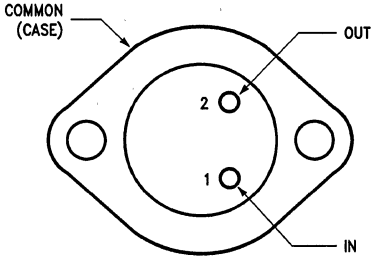
General Description

The LM7800 series of monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Features

- Output current in excess of 1.0A
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Output transistor safe-area compensation
- Available in JEDEC TO-220 and TO-3 packages
- Output voltages of 6V, 8V, 18V and 24V (See Note)
- Available in extended temperature range

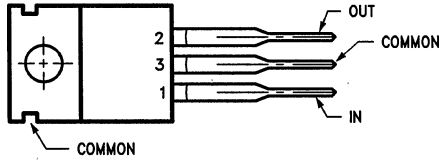
Connection Diagrams



TL/H/10052–1

Top View

Order Number LM7806K, LM7808K, LM7818K, LM7824K, LM7806CK, LM7808CK, LM7818CK or LM7824CK
See NS Package Number K02A



Lead 3 connected to tab.

TL/H/10052–2

Top View

Order Number LM7806CT, LM7808CT LM7818CT or LM7824CT
See NS Package Number T03B

Note: See General Purpose Linear Databook for specifications on similar devices with 5V, 12V, or 15V outputs. These parts can be found under LM140/LM340, LM140A/LM340A (for tighter output tolerance) and LM78XX datasheets.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- TO-3 Metal Can: −65°C to +175°C
- TO-220 Package: −65°C to +150°C

Operating Junction Temperature Range
- Extended (LM7800): −55°C to +150°C
- Commercial (LM7800C): 0°C to +150°C

Lead Temperature
- TO-3 Metal Can (Soldering, 60 sec.): 300°C
- TO-220 Package (Soldering, 10 sec.): 265°C

Power Dissipation: Internally Limited

Input Voltage
- 6.0V to 18V: 35V
- 24V: 40V

ESD Susceptibility: (to be determined)

LM7806C
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 11V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		5.75	6.0	6.25	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.0V \le V_I \le 25V$		5.0	120	mV
				$9.0V \le V_I \le 13V$		1.5	60	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		14	120	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	60	
V_O	Output Voltage		$8.0V \le V_I \le 21V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		5.7		6.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	With Line	$8.0V \le V_I \le 25V$				1.3	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			45		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$		59	75		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0\ kHz$			19		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			550		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0\ mA$, $0°C \le T_A \le +125°C$			0.8		mV/°C

LM7808
Electrical Characteristics

$-55°C \le T_A \le +125°C$, $V_I = 14V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$10.5V \le V_I \le 25V$		6.0	80	mV
				$11V \le V_I \le 17V$		2.0	40	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	100	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	40	
V_O	Output Voltage		$11.5V \le V_I \le 23V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	6.0	mA
ΔI_Q	Quiescent Current Change	With Line	$11.5V \le V_I \le 25V$				0.8	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	

LM7808
Electrical Characteristics (Continued)

$-55°C \le T_A \le +125°C$, $V_I = 14V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter	Conditions (Note 1)		Min	Typ	Max	Units
N_O	Noise	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		62	72		dB
V_{DO}	Dropout Voltage	$I_O = 1.0A$, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance	f = 1.0 kHz			16		mΩ
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35V$			0.75	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \le T_A \le +25°C$			0.4	mV/°C/ V_O
			$+25°C \le T_A \le +125°C$			0.3	

LM7808C
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 14V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	10.5V ≤ V_I ≤ 25V		6.0	160	mV
				11V ≤ V_I ≤ 17V		2.0	80	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 1.5A		12	160	mV
				250 mA ≤ I_O ≤ 750 mA		4.0	80	
V_O	Output Voltage		10.5V ≤ V_I ≤ 23V, 5.0 mA ≤ I_O ≤ 1.0A, P ≤ 15W		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	With Line	10.5V ≤ V_I ≤ 25V				1.0	mA
		With Load	5.0 mA ≤ I_O ≤ 1.0A				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			52		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		56	72		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			16		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			450		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			0.8		mV/°C

LM7818
Electrical Characteristics

$-55°C \le T_A \le +125°C$, $V_I = 27V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		17.3	18.0	18.7	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$21V \le V_I \le 33V$		15	180	mV
				$24V \le V_I \le 30V$		5.0	90	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	180	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	90	
V_O	Output Voltage		$22V \le V_I \le 33V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		17.1		18.9	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	6.0	mA
ΔI_Q	Quiescent Current Change	With Line	$22V \le V_I \le 33V$				0.8	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$		59	69		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0\ kHz$			22		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			0.75		A
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0\ mA$	$-55°C \le T_A \le +25°C$			0.4	mV/°C/ V_O
				$+25°C \le T_A \le +125°C$			0.3	

LM7818C
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 27V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified.

Symbol	Parameter	Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage	$T_J = 25°C$		17.3	18.0	18.7	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	$21V \le V_I \le 33V$		15	360	mV
			$24V \le V_I \le 30V$		5.0	180	
$V_{R\ LOAD}$	Load Regulation	$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	360	mV
			$250\ mA \le I_O \le 750\ mA$		4.0	180	
V_O	Output Voltage	$21V \le V_I \le 33V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		17.1		18.9	V
I_Q	Quiescent Current	$T_J = 25°C$			4.5	8.0	mA

LM7818C
Electrical Characteristics (Continued)

$0°C \le T_A \le +125°C$, $V_I = 27V$, $I_O = 500\ mA$, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)	Min	Typ	Max	Units
ΔI_Q	Quiescent Current Change	With Line	$21V \le V_I \le 33V$			1.0	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$			0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$		110		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$	53	69		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$		2.0		V
R_O	Output Resistance		$f = 1.0\ kHz$		22		$m\Omega$
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$		200		mA
I_{pk}	Peak Output Current		$T_J = 25°C$		2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0\ mA$		1.0		mV/°C

LM7824
Electrical Characteristics

$-55°C \le T_A \le +125°C$, $V_I = 33V$, $I_O = 500\ mA$, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$27V \le V_I \le 38V$		18	240	mV
				$30V \le V_I \le 36V$		6.0	120	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	240	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	120	
V_O	Output Voltage		$28V \le V_I \le 38V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		22.8		25.2	V
I_Q	Quiescent Current		$T_J = 25°C$			4.6	6.0	mA
ΔI_Q	Quiescent Current Change	With Line	$28V \le V_I \le 38V$				0.8	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$		56	66		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance		$f = 1.0\ kHz$			28		$m\Omega$
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			0.75	1.2	A
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0\ mA$	$-55°C \le T_A \le +25°C$			0.4	mV/°C/ V_O
				$+25°C \le T_A \le +125°C$			0.3	

LM7824C
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 33V$, $I_O = 500\ mA$, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Characteristics	Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage	$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	$27V \le V_I \le 38V$		18	480	mV
			$30V \le V_I \le 36V$		6.0	240	
$V_{R\ LOAD}$	Load Regulation	$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	480	mV
			$250\ mA \le I_O \le 750\ mA$		4.0	240	
V_O	Output Voltage	$27V \le V_I \le 38V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		22.8		25.2	V
I_Q	Quiescent Current	$T_J = 25°C$			4.6	8.0	mA

LM7824C

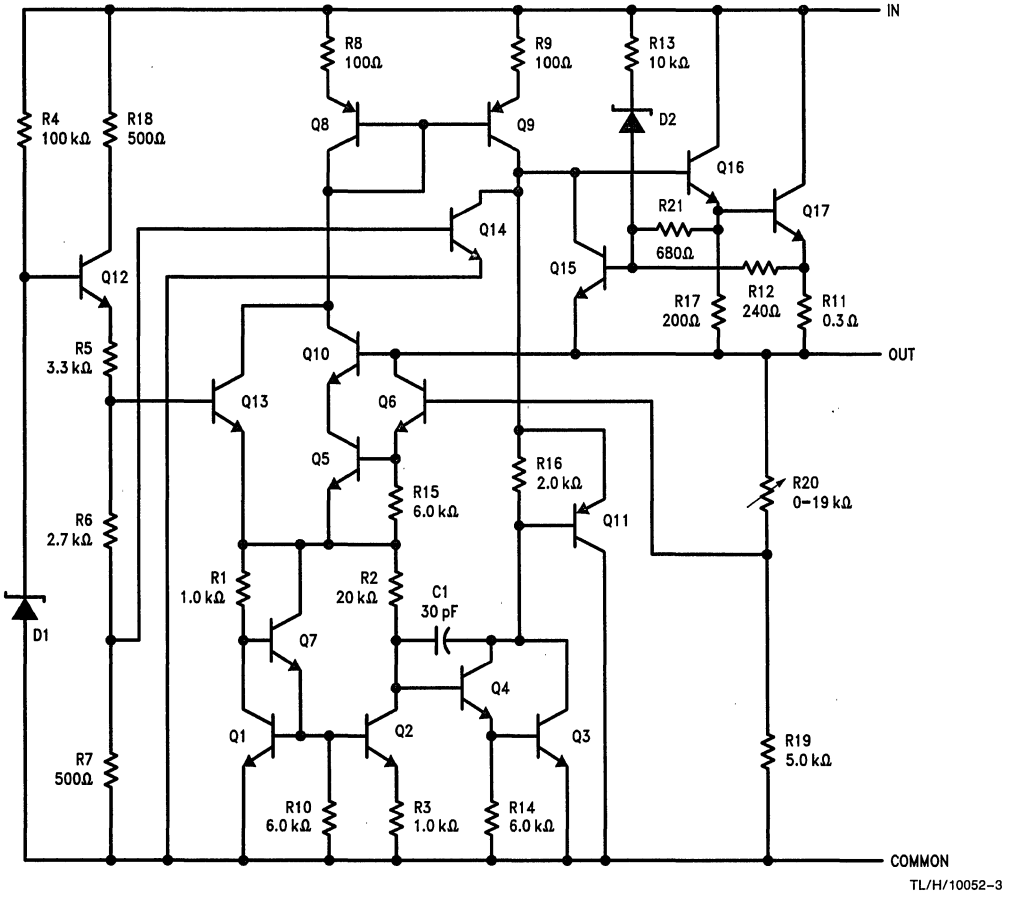
Electrical Characteristics (Continued)

$0°C \le T_A \le +125°C$, $V_I = 33V$, $I_O = 500$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)	Min	Typ	Max	Units
ΔI_Q	Quiescent Current Change	With Line	$27V \le V_I \le 38V$			1.0	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$			0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$		170		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$	50	66		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$		2.0		V
R_O	Output Resistance		$f = 1.0\ kHz$		28		$m\Omega$
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$		150		mA
I_{pk}	Peak Output Current		$T_J = 25°C$		2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA		1.5		mV/°C

Note 1: For all tables, all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \le 10$ ms, duty cycle $\le 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

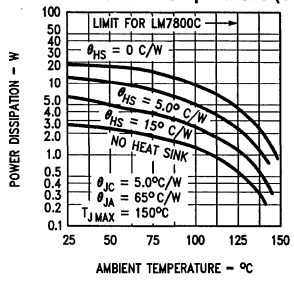
Equivalent Circuit



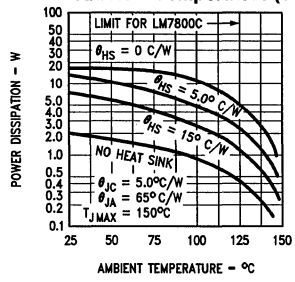
TL/H/10052–3

Typical Performance Characteristics

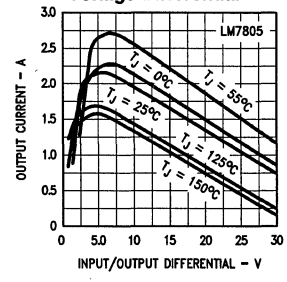
Worst Case Power Dissipation vs Ambient Temperature (TO-3)



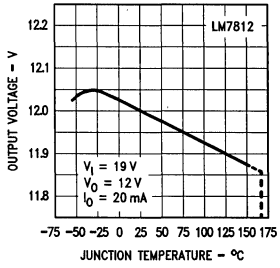
Worst Case Power Dissipation vs Ambient Temperature (TO-220)



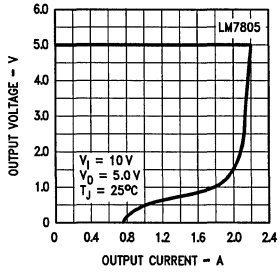
Peak Output Current vs Input/Output Voltage Differential



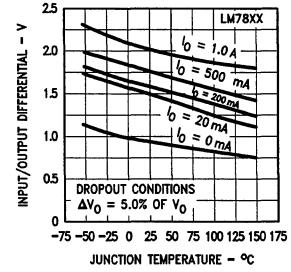
Output Voltage vs Junction Temperature



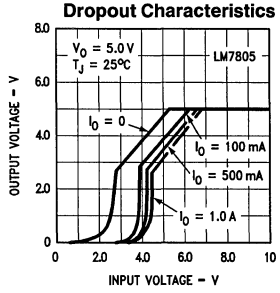
Current-Limiting Characteristics



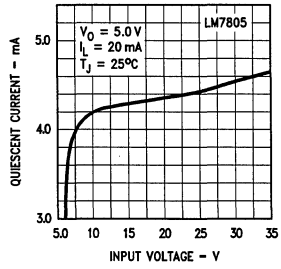
Dropout Voltage vs Junction Temperature



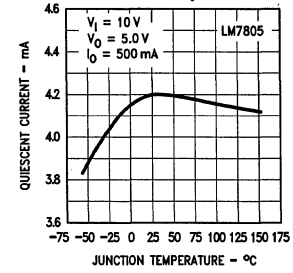
Dropout Characteristics



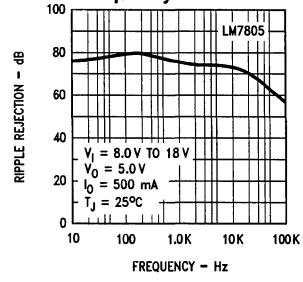
Quiescent Current vs Input Voltage



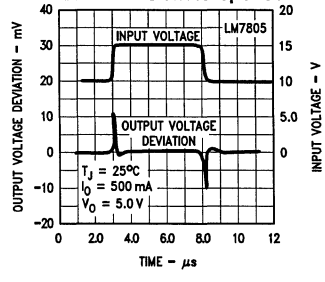
Quiescent Current vs Junction Temperature



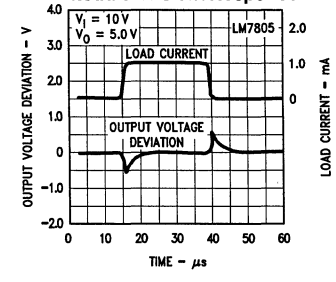
Ripple Rejection vs Frequency



Line Transient Response



Load Transient Response



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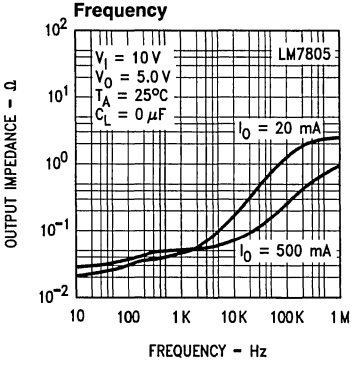
Typical Performance Characteristics (Continued)

Output Impedance vs Frequency



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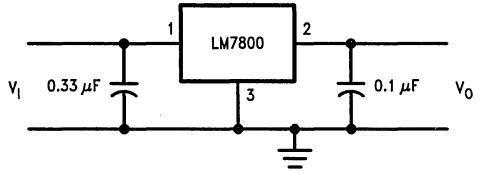
Note: The other LM7800 series devices have similar curves.

DC Parameter Test Circuit



TL/H/10052–6

1

Design Considerations

The LM7800 fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the regulator's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for LM7800, 125°C for LM7800C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
TO-3	3.5	5.5	35	40
TO-220	3.0	5.0	40	60

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max}\, T_A}{\theta_{JA}} \text{ (without heat sink)}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

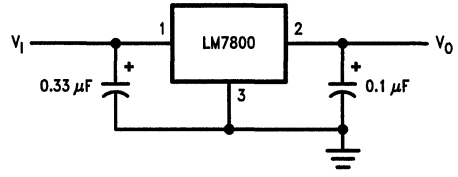
$= T_A + P_D\theta_{JA}$ (without heat sink)

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{CA} = Case-to-Ambient Thermal Resistance
θ_{CS} = Case-to-Heat Sink to Thermal Resistance
θ_{SA} = Heat Sink-to-Ambient Thermal Resistance
θ_{JA} = Junction-to-Ambient Thermal Resistance

Typical Applications

Fixed Output Regulator



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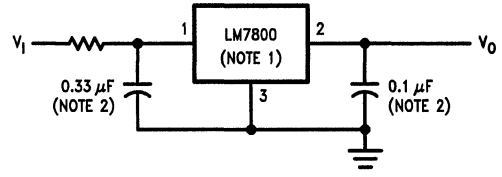
Note 1: To specify an output voltage, substitute voltage value for "00".

Note 2: Bypass capacitors are recommended for optimum stability and transient response, and should be located as close as possible to the regulator.

High Input Voltage Circuits



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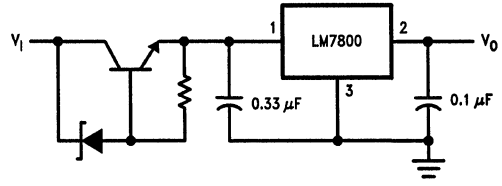

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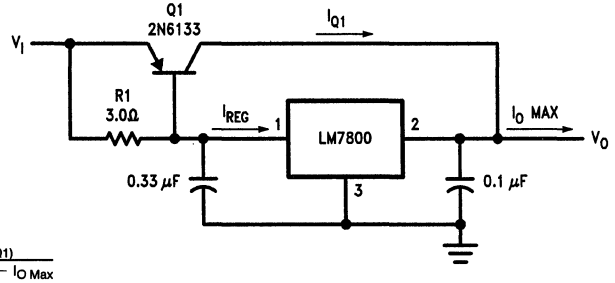
High Current Voltage Regulator



$$\beta(Q1) \geq \frac{I_{O\,Max}}{I_{REG\,Max}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)\, V_{BE(Q1)}}{I_{REG\,Max}(\beta + 1) - I_{O\,Max}}$$

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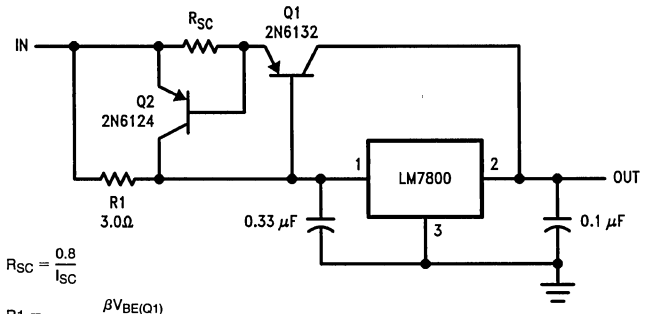
Typical Applications (Continued)

High Output Current, Short Circuit Protected



$$R_{SC} = \frac{0.8}{I_{SC}}$$

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REG\ Max}(\beta + 1) - I_{O\ Max}}$$

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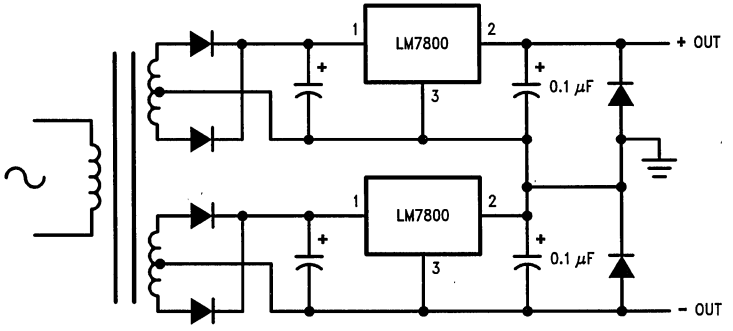
Positive and Negative Regulator



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National Semiconductor

LM78G/LM79G
4-Terminal Adjustable Voltage Regulators

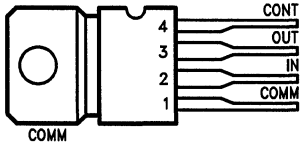
General Description

The LM78G and LM79G are 4-terminal adjustable voltage regulators. They are designed to deliver continuous load currents of up to 1.0A with a maximum input voltage of +40V for the positive regulator LM78G and −40V for the negative regulator LM79G. Output current capability can be increased to greater than 1.0A through use of one or more external transistors. The output voltage range of the LM78G positive voltage regulator is +5V to +30V and the output voltage range of the negative LM79G is −30V to −2.55V. For systems requiring both a positive and negative, the LM78G and LM79G are excellent for use as a dual tracking regulator with appropriate external circuitry.

Features

- Output current in excess of 1A
- LM78G positive output +5V to +30V
- LM79G negative output −30V to −2.55V
- Internal thermal overload protection
- Internal short circuit protection
- Output transistor safe-area protection

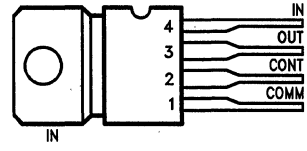
Connection Diagrams



TL/H/10054–1

Top View

Heat sink tabs connected to common through device substrate.



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Top View

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Number LM78GCP or LM79GCP
See NS Package Number P04A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
Power Dissipation	Internally Limited
Input Voltage	
LM78G	+40V
LM79G	−40V
Control Lead Voltage	
LM78G	$0V \le V^+ \le V_O$
LM79G	$V_O^- \le V^- \le 0V$

LM78G
Electrical Characteristics

$0°C \le T_A \le 125°C$, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, $V_I = 10V$, $I_O = 500$ mA, Test Circuit 1, unless otherwise specified

Symbol	Parameter	Conditions (Notes 1, 3)		Min	Typ	Max	Units
V_{IR}	Input Voltage Range	$T_J = 25°C$		7.5		40	V
V_{OR}	Output Voltage Range	$V_I = V_O + 5.0V$		5.0		30	V
V_O	Output Voltage Tolerance	$(V_O + 3.0V) \le V_I \le (V_O + 15V)$, $5.0\ mA \le I_O \le 1.0A$, $P_D \le 15W$, $V_{I\ Max} = 38V$	$T_J = 25°C$			4.0	% V_O
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $V_O \le 10V$, $(V_O + 2.5V) \le V_I \le (V_O + 20V)$				1.0	% V_O
$V_{O\ LOAD}$	Load Regulation	$T_J = 25°C$, $V_I \le V_O + 5.0V$	$250\ mA \le I_O \le 750\ mA$			1.0	% V_O
			$5.0\ mA \le I_O \le 1.5A$			2.0	
I_C	Control Lead Current	$T_J = 25°C$			1.0	5.0	μA
						8.0	
I_Q	Quiescent Current	$T_J = 25°C$			3.2	6.0	mA
						7.0	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$8.0V \le V_I \le 18V$, f = 2400 Hz, $V_O = 5.0V$, $I_C = 350$ mA		68	78		dB
N_O	Noise	$T_J = 25°C$, 10 Hz < f < 100 kHz, $V_O = 5.0V$, $I_O = 5.0$ mA			8.0	40	μV/V_O
V_{DO}	Dropout Voltage (Note 2)				2.0	2.5	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 30V$			0.750	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = 5.0V$, $I_O = 5.0$ mA	$T_A = -55°C$ to $+25°C$			0.4	mV/°C/V_O
			$T_A = 25°C$ to $+125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
				4.75		5.25	

Note 1: V_O is defined for the LM78G as $V_O = \frac{R1 + R2}{R2}(5.0)$;

Note 2: Dropout Voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.

Note 3: All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

LM79G

Electrical Characteristics

$0°C \le T_A \le 125°C$ for LM79G, $V_I = -10V$, $I_O = 500$ mA, $C_I = 2.0\ \mu F$, $C_O = 0.1\ \mu F$, Test Circuit 2 and Note 3, unless otherwise specified

Symbol	Parameter	Conditions (Note 1)		Min	Typ	Max	Units
V_{IR}	Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
V_{OR}	Nominal Output Voltage Range	$V_I = V_O - 5.0V$		−30		−2.55	V
V_O	Output Voltage Tolerance	$(V_O - 15V) \le V_I \le (V_O - 3.0V)$, $5.0\ mA \le I_O \le 1.0A$, $P_D \le 15W$, $V_{I\,Max} = -3.8V$	$T_J = 25°C$			4.0	% V_O
						5.0	
$V_{O\,LINE}$	Line Regulation	$T_J = 25°C$, $V_O \ge -10V$, $(V_O - 20V) \le V_I \le (V_O - 2.5V)$				1.0	% V_O
$V_{O\,LOAD}$	Load Regulation	$T_J = 25°C$, $V_I = V_O = -5.0V$	$250\ mA \le I_O \le 750\ mA$			1.0	% V_O
			$5.0\ mA \le I_O \le 1.5A$			2.0	
I_C	Control Lead Current	$T_J = 25°C$			0.4	2.0	μA
						3.0	
I_Q	Quiescent Current	$T_J = 25°C$			2.5	2.0	mA
						8.0	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_O = -8.0V$, $V_I = -13V$, $f = 2400$ Hz, $I_C = 350$ mA		50	60		dB
N_O	Noise	$T_J = 25°C$, $10\ Hz \le f \le 100\ kHz$, $V_O = -8.0V$, $I_O = 5.0$ mA			25	80	μV/V_O
V_{DO}	Dropout Voltage (Note 2)				1.1	2.3	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = -30V$			0.25	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = -5.0V$, $I_O = 5.0$ mA	$T_A = -55°C$ to $+25°C$			0.3	mV/°C/V_O
			$T_A = 25°C$ to $125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		−2.65	−2.55	−2.45	V
				−2.68		−2.43	

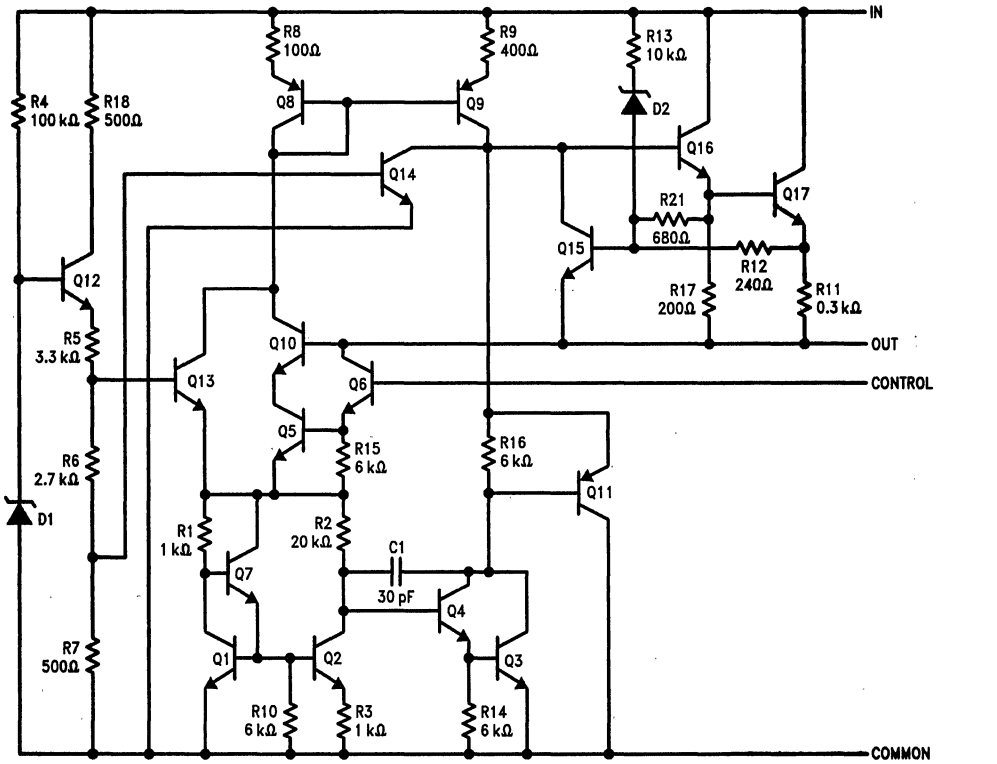
Note 1: V_O is defined for the LM79G as $V_O = \frac{R1 + R2}{R2}(-2.55)$.

Note 2: Dropout Voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.

Note 3: The convention for negative regulators is the algebraic value, thus −15V is less than −10V.

Note 4: All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

LM78G Equivalent Circuit



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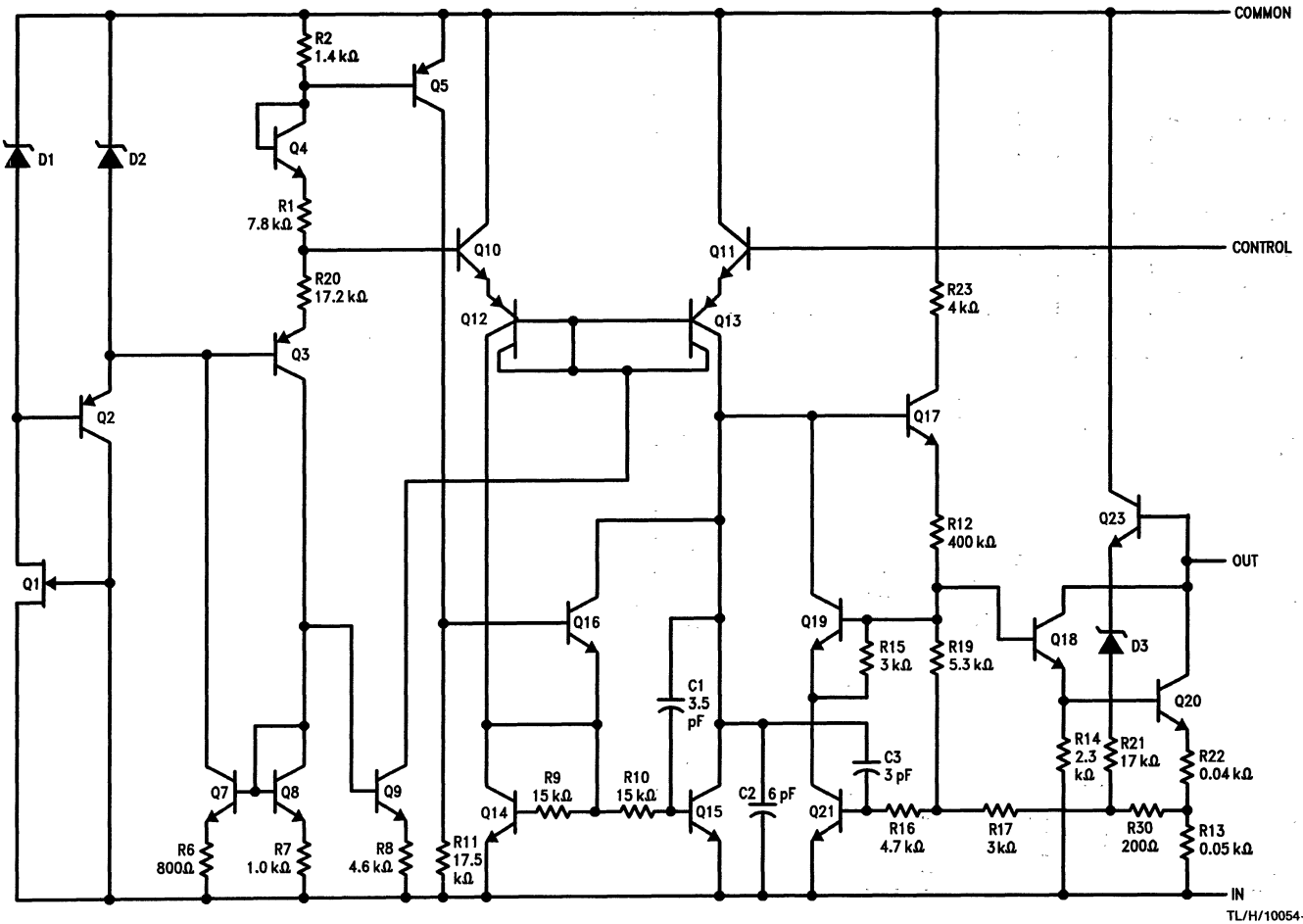
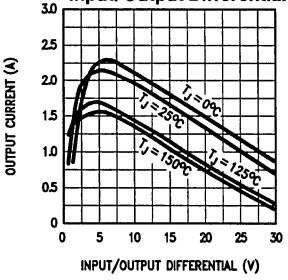
LM79G Equivalent Circuit

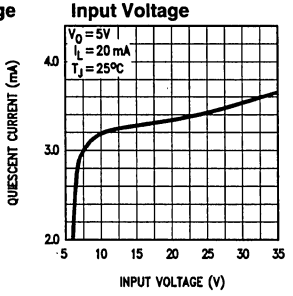


Typical Performance Curves for LM78G

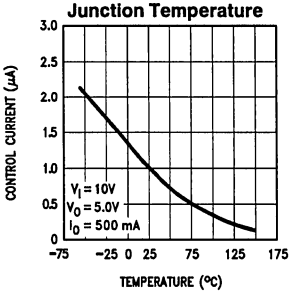
Peak Output Current vs Input/Output Differential Voltage



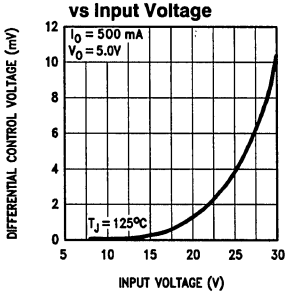
Quiescent Current vs Input Voltage



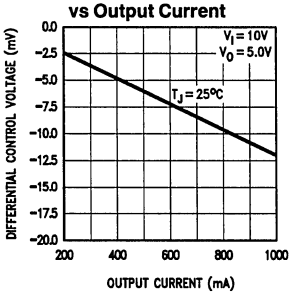
Control Current vs Junction Temperature



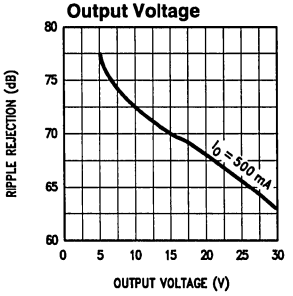
Differential Control Voltage vs Input Voltage



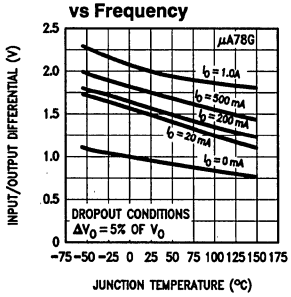
Differential Control Voltage vs Output Current



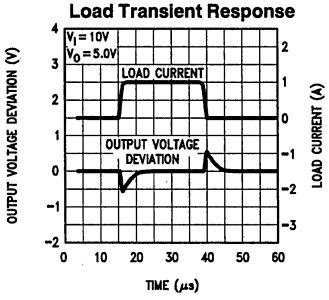
Ripple Rejection vs Output Voltage



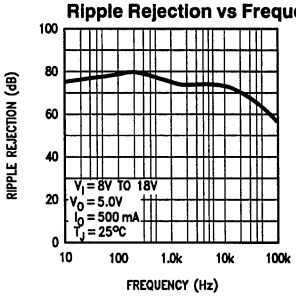
Dropout Voltage vs Junction Temperature vs Frequency



Load Transient Response



Ripple Rejection vs Frequency



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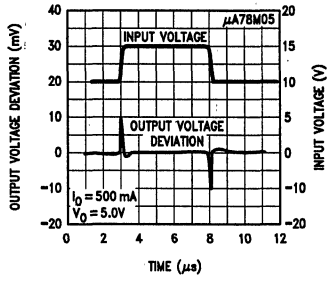
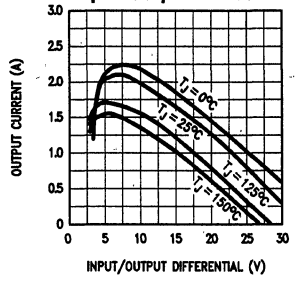
Typical Performance Curves for LM79G

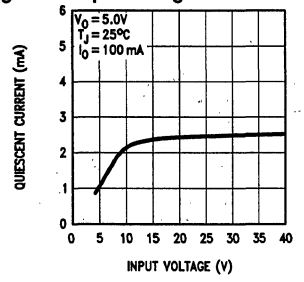
Line Transient Response for LM78G



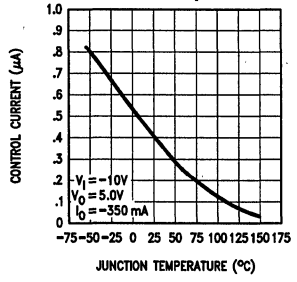
Peak Output Current vs Input/Output Differential Voltage



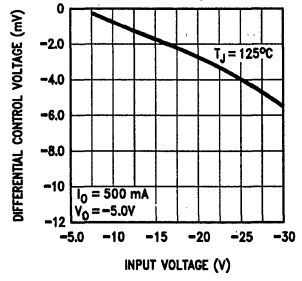
Quiescent Current vs Input Voltage



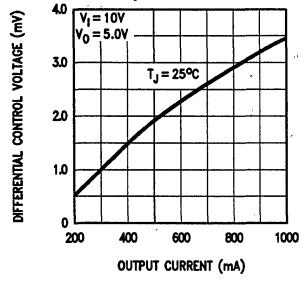
Control Current vs Junction Temperature



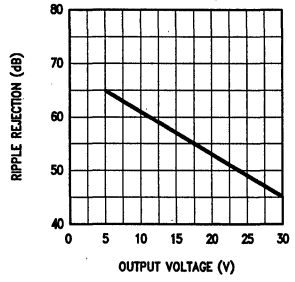
Differential Control Voltage vs Input Voltage



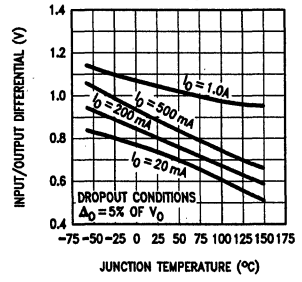
Differential Control Voltage vs Output Current



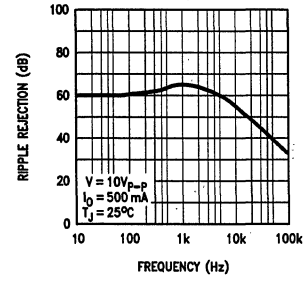
Ripple Rejection vs Output Voltage



Dropout Voltage vs Junction Temperature



Ripple Rejection vs Frequency



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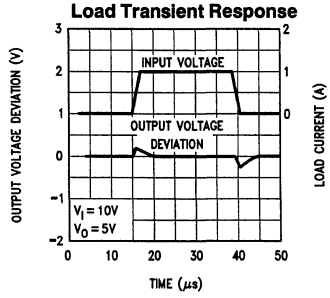
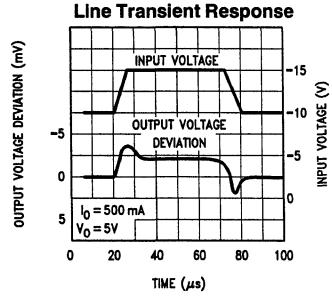
Load Transient Response



TL/H/10054–7

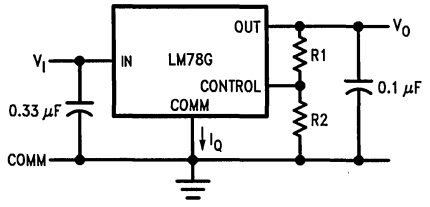
Line Transient Response



TL/H/10054–10

Test Circuits

LM78G Test Circuit 1

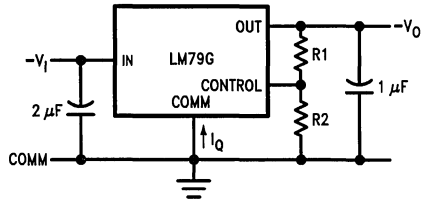


TL/H/10054–8

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{CONT}$$

V_{CONT} Nominal = 5.0V

LM79G Test Circuit 2



TL/H/10054–9

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{CONT}$$

V_{CONT} Nominal = −2.55V

Recommended R2 current ≈ 1.0 mA
∴ R2 = 5.0 kΩ (LM78G)
R2 = 2.55 kΩ (LM79G)

Design Considerations

The LM78G and LM79G Adjustable Voltage Regulators have an output voltage which varies from V_{CONT} to typically

$$V_I - 2.0V \text{ by } V_O = V_{CONT}\frac{R1 + R2}{R2}$$

The nominal reference in the LM78G is 5.0V and LM79G is −2.55V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5.0 kΩ in the LM78G. Then, the output voltage is; V_O = (R1 + R2)V, where R1 and R2 are in kΩs.

Example: If R2 = 5.0 kΩ and R1 = 10 kΩ then
V_O = 15V nominal, for the LM78G
R2 = 2.55 kΩ and R1 = 12.8 kΩ then
V_O = −15.35 nominal, for the LM79G

By proper wiring of the feedback resistors, load regulation of the device can be improved significantly.

Both LM78G and LM79G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	Typ °C/W	Max °C/W	Typ °C/W	Max °C/W
Package	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
Power Watt	7.5	11	75	80

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta CS + \theta_{SA}$$

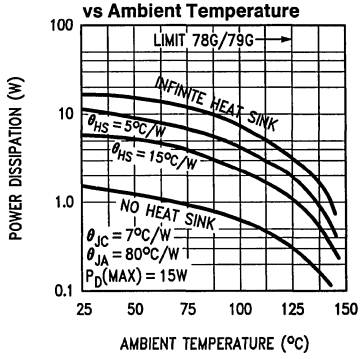
Solving for T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$
$$= T_A + P_D\theta_{JA} \text{ (without heat sink)}$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junctiuon to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
θ_{CA} = Case to Ambient Thermal Resistance
θ_{CS} = Case to Heat Sink Resistance
θ_{SA} = Heat Sink to Ambient Thermal Resistance

LM78G and LM79G Power Tab (U1) Package Worst Case Power Dissipation vs Ambient Temperature

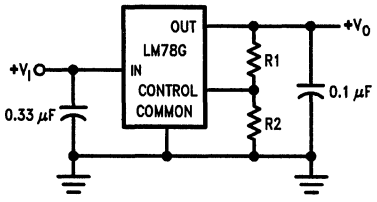


TL/H/10054–11

Typical Applications for LM78G

Bypassing of the input and output (0.33 μF and 0.1 μF, respectively) is necessary.

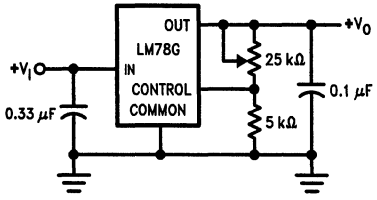
Basic Positive Regulator



TL/H/10054–12

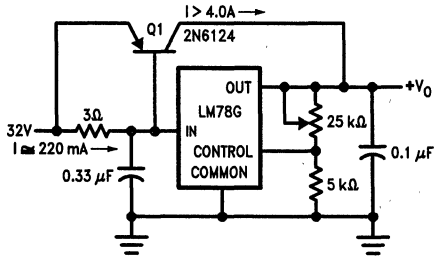
$$V_O = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Positive 5.0V to 30V Adjustable Regulator



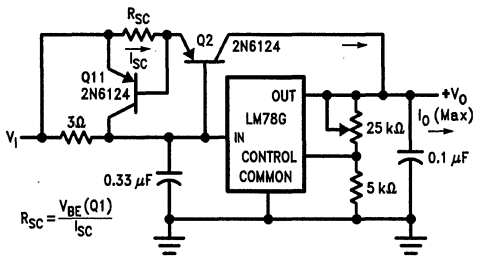
TL/H/10054–13

Positive 5.0V to 30V Adjustable Regulator (I_O > 5.0A) (Note 1)



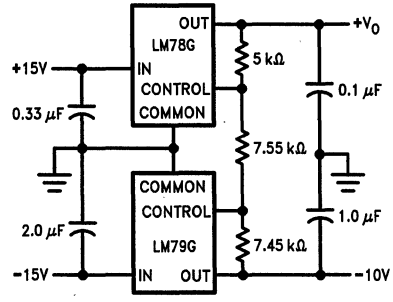
TL/H/10054–14

Positive High Current Short Circuit, Protected Regulator



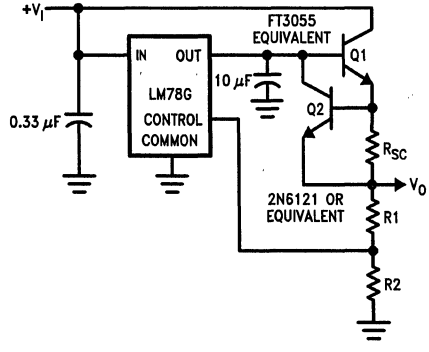
TL/H/10054–15

± 10V, 1.0A, Dual Tracking Regulator (Note 2)



TL/H/10054–16

Positive High Current, Short Circuit Protected Regulator



TL/H/10054–17

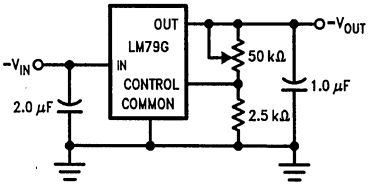
Note 1: External series pass device is not short circuit protected.

Note 2: If load is not ground referenced, connect reverse biased diodes from outputs to ground.

Typical Applications for LM79G

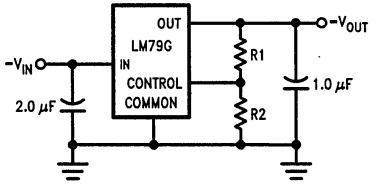
All LM78G applications apply to the LM79G under the following conditions: R2 values are 2.5 kΩ, all external transistors and diodes reverse polarity.

−30V to −2.5V Adjustable Regulator



TL/H/10054–18

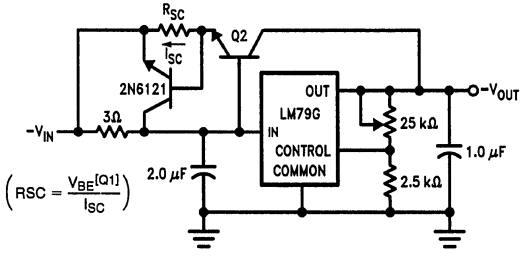
Basic Negative Regulator



TL/H/10054–19

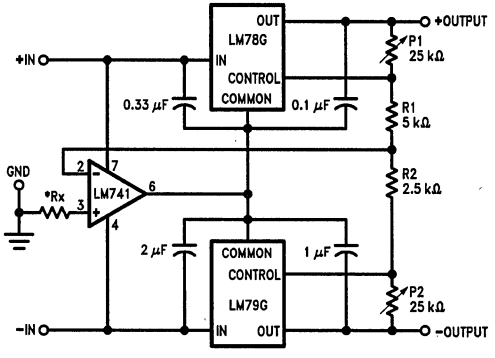
$$V_{OUT} = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Negative High Current Short Circuit Protected Regulator



TL/H/10054–20

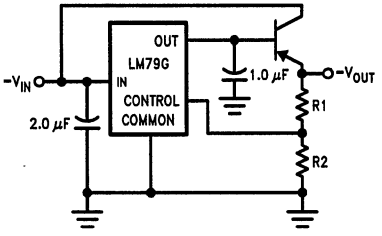
Adjustable Dual Tracking Regulator



TL/H/10054–21

*Rx = Parallel combination of (R1 + P1) and (R2 + P2).

Negative High Current Voltage Regulator External Series Pass



TL/H/10054–22

Applications Hints

Bypass capacitors are recommended for stable operation of the LM79G series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors (2 μF on the input, 1 μF on the output), should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

National Semiconductor

LM78LXX Series 3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustment voltages and currents.

The LM78LXX is available in the metal three lead TO-39(H) the plastic TO-92 (Z), and SO-8 plastic. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

For output voltage other than 5V, 12V and 15V the LM117L series provides an output voltage range from 1.2V to 37V.

Features

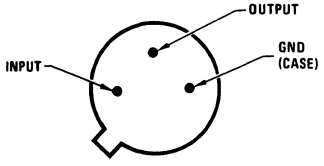
- Output voltage tolerances of ±5% (LM78LXXAC) over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and metal TO-39 and plastic SO-8 low profile packages

Voltage Range

LM78L05	5V
LM78L12	12V
LM78L15	15V

Connection Diagrams

Metal Can Package

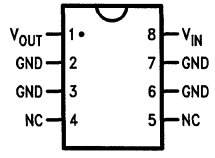


TL/H/7744–1

Bottom View

**Order Number LM78L05ACH,
LM78L12ACH or LM78L15ACH
See NS Package Number H03A**

**SO-8 Plastic
(Narrow Body)**

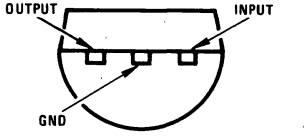


TL/H/7744–2

Top View

**Order Number LM78L05ACM,
LM78L12ACM or LM78L15ACM
See NS Package Number M08A**

Plastic Package



TL/H/7744–3

Bottom View

**Order Number LM78L05ACZ,
LM78L12ACZ or LM78L15ACZ
See NS Package Number Z03A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
V_O = 5V	30V
V_O = 12V to 15V	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	125°C
Storage Temperature Range	
Metal Can (H Package)	−65°C to +150°C
Molded TO-92 (Z Package)	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance (Note 5)	2000V

LM78LXXAC Electrical Characteristics

(Note 2) T_j = 0°C to 125°C, I_O = 40 mA, C_{IN} = 0.33 µF, C_O = 0.1 µF (unless noted)

LM78LXXAC Output Voltage			5V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
V_O	Output Voltage (Note 4)	Tj = 25°C	4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		1 mA ≤ I_O ≤ 70 mA	4.75		5.25	11.4		12.6	14.25		15.75	V
		1 mA ≤ I_O ≤ 40 mA and V_{MIN} ≤ V_{IN} ≤ V_{MAX}	4.75 (7 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75	V
ΔV_O	Line Regulation	Tj = 25°C		10	54		20	110		25	140	mV
			(8 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤27)			(20 ≤ V_{IN} ≤ 30)			V
				18	75		30	180		37	250	mV
			(7 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Load Regulation	Tj = 25°C, 1 mA ≤ I_O ≤ 40 mA		5	30		10	50		12	75	mV
		Tj = 25°C, 1 mA ≤ I_O ≤ 100 mA		20	60		30	100		35	150	mV
ΔV_O	Long Term Stability			12			24			30		mV/1000 hrs
I_Q	Quiescent Current	Tj = 25°C		3	5		3	5		3.1	5	mA
		Tj = 125°C			4.7			4.7			4.7	
ΔI_Q	Quiescent Current Change	1 mA ≤ I_O ≤ 40 mA			0.1			0.1			0.1	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			1.0			1.0			1.0	mA
			(8 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 27)			(20 ≤ V_{IN} ≤ 30)			V
V_n	Output Noise Voltage	Tj = 25°C, (Note 3) f = 10 Hz − 10 kHz		40			80			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	47 (8 ≤ V_{IN} ≤ 16)	62		40 (15 ≤ V_{IN} ≤ 25)	54		37 (18.5 ≤ V_{IN} ≤ 28.5)	51		dB V
	Input Voltage Required to Maintain Line Regulation	Tj = 25°C	7			14.5			17.5			V

Note 1: Thermal resistance of H package is typically 26°C/W θ_{jc} still Air, and 94°C/W θ_{ja} 400 ft/min of air. For the Z package is 60°C/W θ_{jc}, 232°C/W θ_{ja} still air, and 88°C/W θ_{ja} at 400 ft/min of air. For the M package, θ_{ja} is 180°C/W in still air. The maximum junction temperature shall not exceed 125°C on Electrical parameters.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

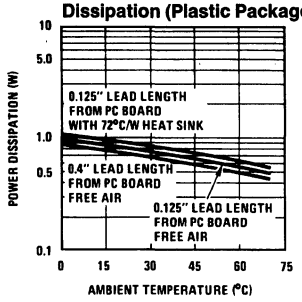
Note 3: Recommended minimum load capacitance of 0.01 µF to limit high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within ±0.01% V_O/°C.

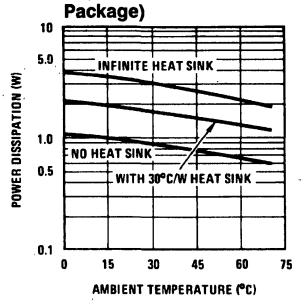
Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

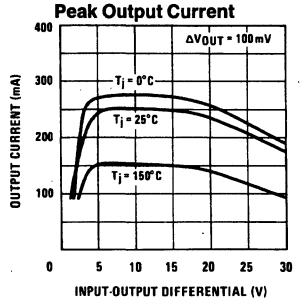
Maximum Average Power Dissipation (Plastic Package)



Maximum Average Power Dissipation (Metal Can Package)

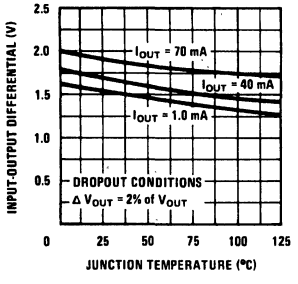


Peak Output Current

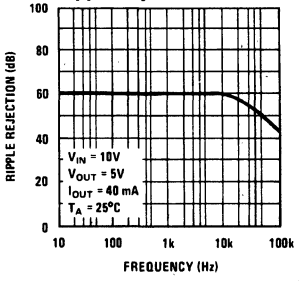


TL/H/7744–4

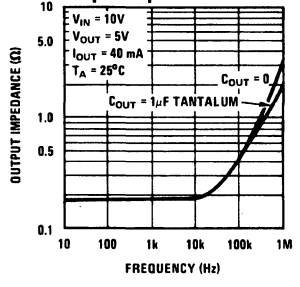
Dropout Voltage



Ripple Rejection

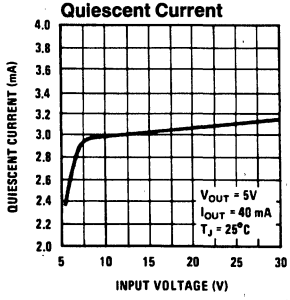


Output Impedance

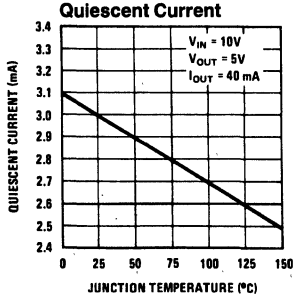


TL/H/7744–5

Quiescent Current



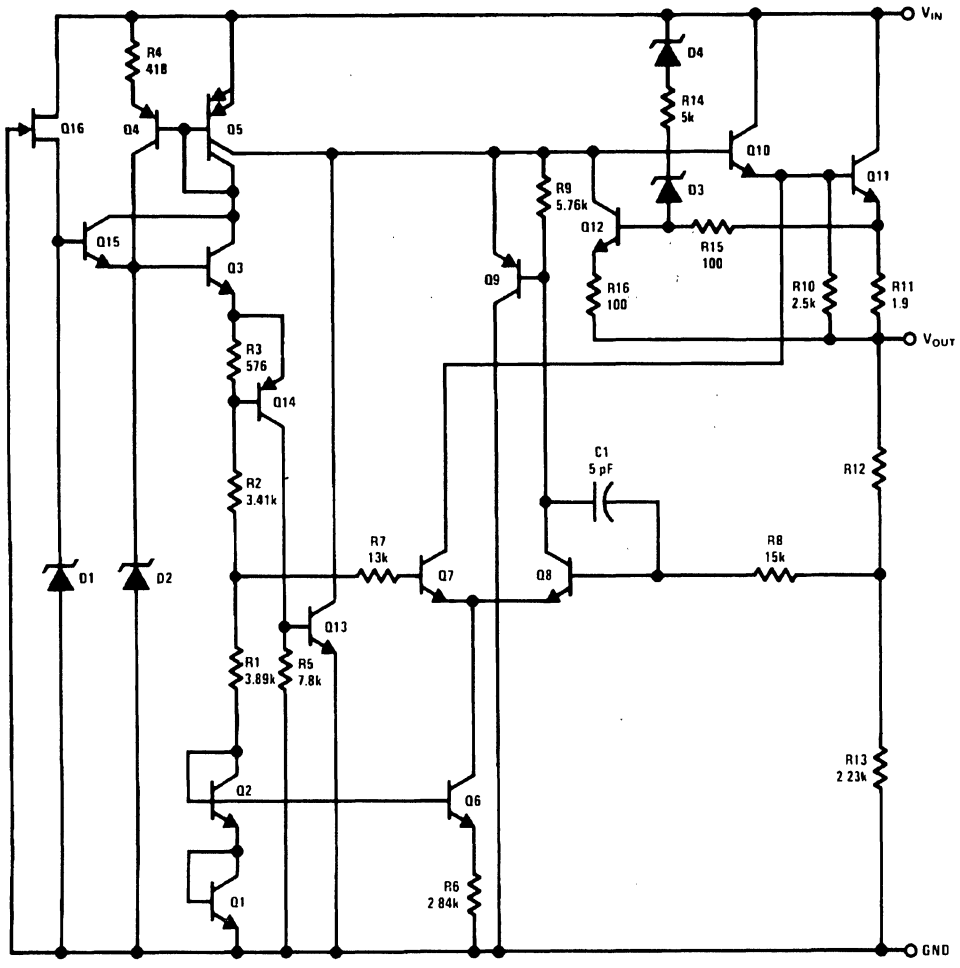
Quiescent Current



TL/H/7744–6

Equivalent Circuit

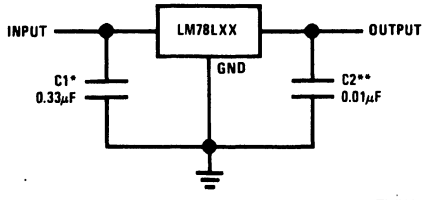
LM78LXX



TL/H/7744–7

Typical Applications

Fixed Output Regulator

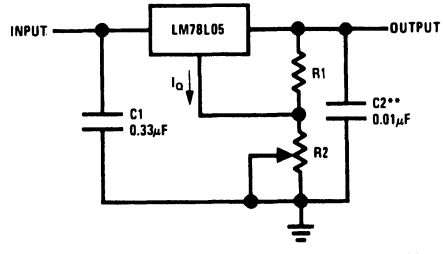


TL/H/7744–8

*Required if the regulator is located far from the power supply filter.

**See Note 3 in the electrical characteristics table.

Adjustable Output Regulator



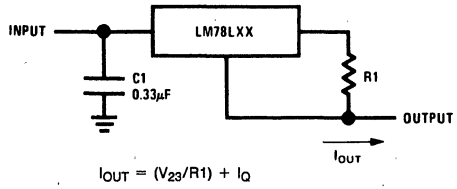
TL/H/7744–9

$V_{OUT} = 5V + (5V/R1 + I_Q) R2$

$5V/R1 > 3\ I_Q$, load regulation $(L_r) \approx [(R1 + R2)/R1]$ (L_r of LM78L05)

Typical Applications (Continued)

Current Regulator

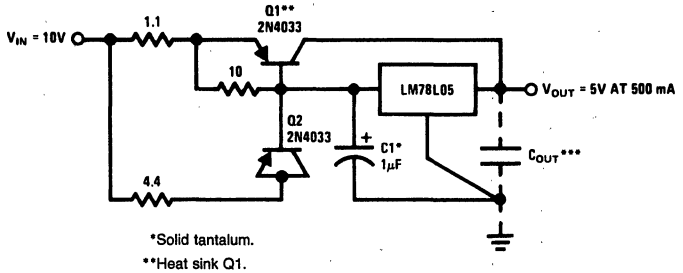


$I_{OUT} = (V_{23}/R1) + I_Q$

$>I_Q$ = 1.5 mA over line and load changes

TL/H/7744–10

5V, 500 mA Regulator with Short Circuit Protection



*Solid tantalum.

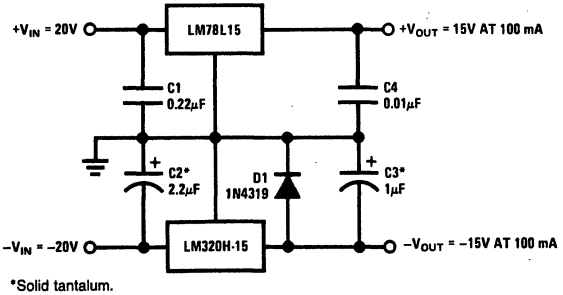
**Heat sink Q1.

***Optional: Improves ripple rejection and transient response.

Load Regulation: 0.6% $0 \leq I_L \leq 250$ mA pulsed with t_{ON} = 50 ms.

TL/H/7744–11

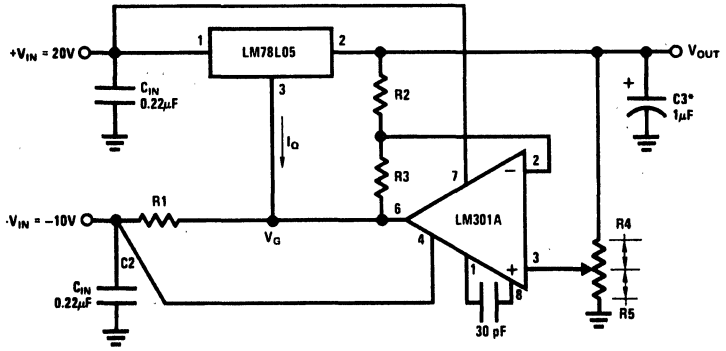
±15V, 100 mA Dual Power Supply



*Solid tantalum.

TL/H/7744–12

Variable Output Regulator 0.5V-18V



*Solid tantalum.

$V_{OUT} = V_G + 5V$, $R1 = (-V_{IN}/I_{Q\ LM78L05})$

$V_{OUT} = 5V\ (R2/R4)$ for $(R2 + R3) = (R4 + R5)$

A 0.5V output will correspond to $(R2/R4) = 0.1\ (R3/R4) = 0.9$

TL/H/7744–13

National Semiconductor

LM78L00 Series
3-Terminal Positive Voltage Regulators

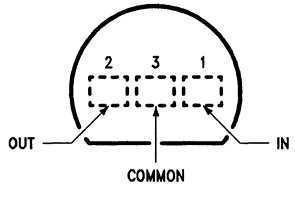
General Description

The LM78L00 series of 3-terminal positive voltage regulators employ internal current-limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The LM78L00, used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

Features

- Output current up to 100 mA
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Available in JEDEC TO-92
- Output Voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V
- Output voltage tolerances of ±5% over the temperature range

Connection Diagram



TL/H/10051–1

Top View

Order Number LM78L05ACZ, LM78L09ACZ, LM78L12ACZ, LM78L15ACZ, LM78L62ACZ or LM78L82ACZ
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operation Junction Temperature Range	
Commercial (LM78L00AC)	0°C to +125°C
Lead Temperature	
TO-92 Package/SO-8	
(Soldering, 10 sec.)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0V to 15V	35V
ESD Susceptibility	to be determined

LM78L05AC
Electrical Characteristics

0°C ≤ T_A ≤ +125°C, V_I = 10V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		T_J = 25°C		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	7.0V ≤ V_I ≤ 20V		55	150	mV
				8.0V ≤ V_I ≤ 20V		45	100	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	1.0 mA ≤ I_O ≤ 100V		11	60	mV
				1.0 mA ≤ I_O ≤ 40 mA		5.0	30	
V_O	Output Voltage (Note 2)		7.0V ≤ V_I ≤ 20V	1.0 mA ≤ I_O ≤ 40 mA	4.75		5.25	V
			7.0V ≤ V_I ≤ V_{Max}	1.0 mA ≤ I_O ≤ 70 mA	4.75		5.25	
I_Q	Quiescent Current					2.0	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	8.0V ≤ V_I ≤ 20V				1.5	mA
		With Load	1.0 mA ≤ I_O ≤ 40 mA				0.1	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 120 Hz, 8.0V ≤ V_I ≤ 18V, T_J = 25°C		41	49		dB
V_{DO}	Dropout Voltage		T_J = 25°C			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		T_J = 25°C			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			−0.65		mV/°C

Note 1: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

Note 2: Power Dissipation ≤ 0.75W.

LM78L62AC
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 12V$, $I_O = 40$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		5.95	6.2	6.45	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.5V \le V_I \le 20V$		65	175	mV
				$9.0V \le V_I \le 20V$		55	125	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \le I_O \le 100\ mA$		13	80	mV
				$1.0\ mA \le I_O \le 40\ mA$		6.0	40	
V_O	Output Voltage (Note 2)		$8.5V \le V_I \le 20V$	$1.0\ mA \le I_O \le 40\ mA$	5.90		6.5	V
			$8.5V \le V_I \le V_{Max}$	$1.0\ mA \le I_O \le 70\ mA$	5.90		6.5	
I_Q	Quiescent Current					2.0	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	$8.0V \le V_I \le 20V$				1.5	mA
		With Load	$1.0\ mA \le I_O \le 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			50		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120\ Hz$, $10V \le V_I \le 20V$, $T_J = 25°C$		40	46		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−0.75		mV/°C

LM78L82AC
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 14V$, $I_O = 40$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		7.87	8.2	8.53	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$11V \le V_I \le 23V$		80	175	mV
				$12V \le V_I \le 23V$		70	125	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \le I_O \le 100\ mA$		15	80	mA
				$1.0\ mA \le I_O \le 40\ mA$		8.0	40	
V_O	Output Voltage (Note 2)		$11V \le V_I \le 23V$	$1.0\ mA \le I_O \le 40\ mA$	7.8		8.5	V
			$11V \le V_I \le V_{Max}$	$1.0\ mA \le I_O \le 70\ mA$	7.8		8.6	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	$12V \le V_I \le 23V$				1.5	mA
		With Load	$1.0\ mA \le I_O \le 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			60		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120\ Hz$, $12V \le V_I \le 22V$, $T_J = 25°C$		39	45		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−0.8		mV/°C

Note 1: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

Note 2: Power Dissipation ≤ 0.75W.

LM78L09AC
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 15V$, $I_O = 40$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		8.64	9.0	9.36	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$11.5V \le V_I \le 24V$		90	200	mV
				$13V \le V_I \le 24V$		100	150	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \le I_O \le 100\ mA$		20	90	mV
				$1.0\ mA \le I_O \le 40\ mA$		10	45	
V_O	Output Voltage (Note 2)		$11.5V \le V_I \le 24V$	$1.0\ mA \le I_O \le 40\ mA$	8.55		9.45	V
			$11.5V \le V_I \le V_{Max}$	$1.0\ mA \le I_O \le 70\ mA$	8.55		9.45	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	$11.5V \le V_I \le 24V$				1.5	mA
		With Load	$1.0\ mA \le I_O \le 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			70		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120\ Hz$, $15V \le V_I \le 25V$, $T_J = 25°C$		38	44		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−0.9		mV/°C

LM78L12AC
Electrical Characteristics

$0°C \le T_A \le +125°C$, $V_I = 19V$, $I_O = 40$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		11.5	12	12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$14.5V \le V_I \le 27V$		120	250	mV
				$16V \le V_I \le 27V$		100	200	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \le I_O \le 100\ mA$		20	100	mV
				$1.0\ mA \le I_O \le 40\ mA$		10	50	
V_O	Output Voltage (Note 2)		$14.5V \le V_I \le 27V$	$1.0\ mA \le I_O \le 40\ mA$	11.4		12.6	V
			$14.5V \le V_I \le V_{Max}$	$1.0\ mA \le I_O \le 70\ mA$	11.4		12.6	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	$16V \le V_I \le 27V$				1.5	mA
		With Load	$1.0\ mA \le I_O \le 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			80		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120\ Hz$, $15V \le V_I \le 25V$, $T_J = 25°C$		37	42		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−1.0		mV/°C

Note 1: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

Note 2: Power Dissipation ≤ 0.75W.

LM78L15AC
Electrical Characteristics

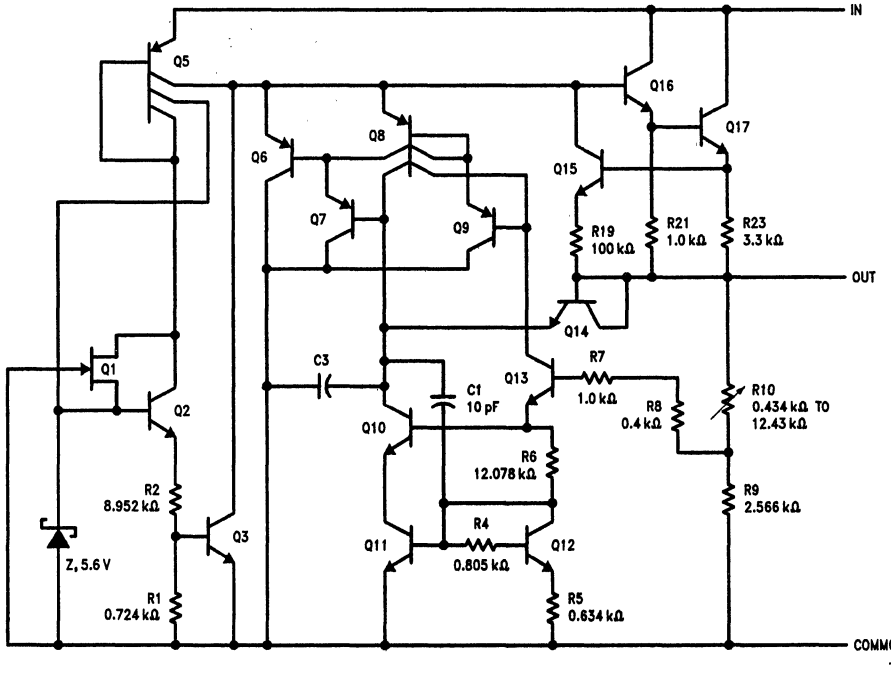
$0°C \le T_A \le +125°C$, $V_I = 23V$, $I_O = 40$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Note 1)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		14.4	15	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$17.5V \le V_I \le 30V$		130	300	mV
				$20V \le V_I \le 30V$		110	250	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \le I_O \le 100\ mA$		25	150	mV
				$1.0\ mA \le I_O \le 40\ mA$		12	75	
V_O	Output Voltage (Note 2)		$17.5V \le V_I \le 30V$	$1.0\ mA \le I_O \le 40\ mA$	14.25		15.75	V
			$17.5V \le V_I \le V_{Max}$	$1.0\ mA \le I_O \le 70\ mA$	14.25		15.75	
I_Q	Quiescent Current					2.2	5.5	mA
ΔI_Q	Quiescent Current Change	With Line	$20V \le V_I \le 30V$				1.5	mA
		With Load	$1.0\ mA \le I_O \le 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			90		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120\ Hz$, $18.5V \le V_I \le 28.5V$, $T_J = 25°C$		34	39		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−1.3		mV/°C

Note 1: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

Note 2: Power Dissipation ≤ 0.75W.

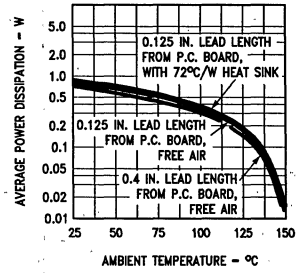
Equivalent Circuit



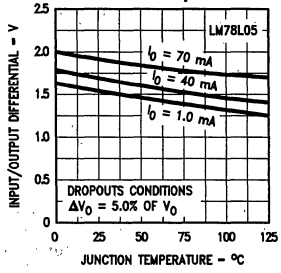
TL/H/10051–2

Typical Performance Characteristics

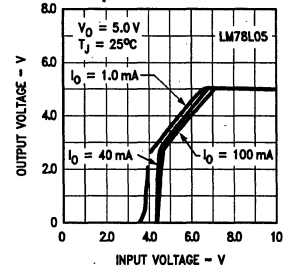
Worst Case Power Dissipation vs Ambient Temperature (TO-92)



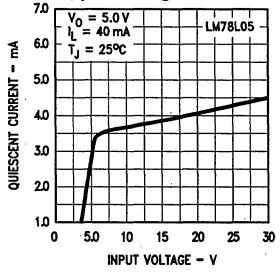
Dropout Voltage vs Junction Temperature



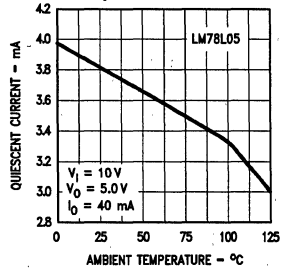
Dropout Characteristics



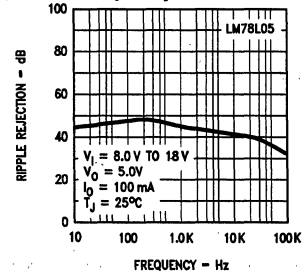
Quiescent Current vs Input Voltage



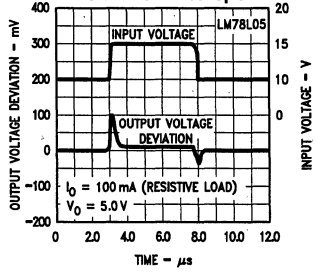
Quiescent Current vs Temperature



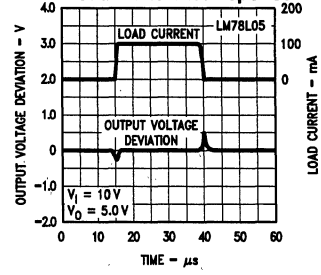
Ripple Rejection vs Frequency



Line Transient Response



Load Transient Response



TL/H/10051–3

Note: Other LM78L00 Series devices have similar curves.

Design Considerations

The LM78L series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-92			160	160

Thermal Considerations

The TO-92 molded package is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the leads, in parallel with the case path, to ambient temperature, as shown in *Figure 1*.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}} \quad (1)$$

Where:

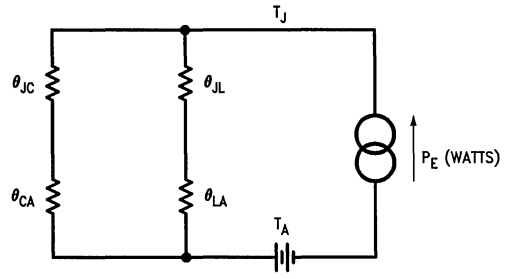
θ_{JC}= thermal resistance of the case between the regulator die and a point on the case directly above the die location.

θ_{CA}= thermal resistance between the case and air at ambient temperature.

θ_{JL}= thermal resistance from regulator die through the input lead to a point $1/16$ inch below the regulator case.

θ_{LA}= total thermal resistance of the input/output ground leads to ambient temperature.

θ_{JA}= junction to ambient thermal resistance.



TL/H/10051–4

FIGURE 1. TO-92 Thermal Equivalent Circuit

Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72 °C/W flag type heat sink, such as the Staver F1-7D-2, on the LM78L00 molded case. The heat sink effectively replaces the θ_{CA} *(Figure 2)* and the new thermal resistance, θ'_{JA}, equals 145 °C/W (assuming, 0.125 inch lead length).

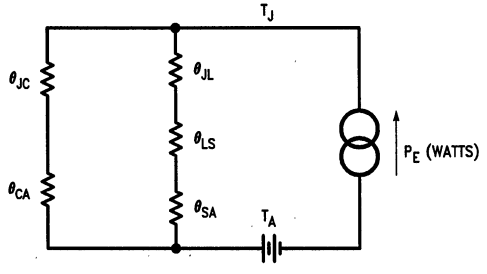
The net change of 15 °C/W increases the allowable power dissipation to 0.86W with a minimal inserted cost. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46 °C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the leads at the mounting point to ambient, that is, the mounting medium. θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in *Figure 2*.

In the case of a socket, θ_{SA} could be as high as 270 °C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but lead sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

Methods of Heat Sinking (Continued)

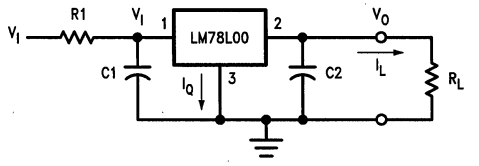
The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.



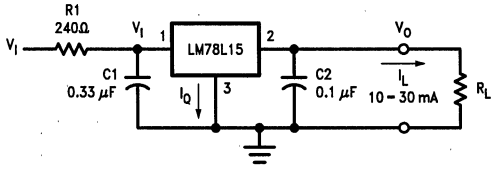
TL/H/10051–5

FIGURE 2. TO-92 Thermal Equivalent Circuit (Lead at other than Ambient Temperature)

High Dissipation Applications



TL/H/10051–6



TL/H/10051–7

Where it is necessary to operate a LM78L00 regulator with a large input/output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 = \frac{V_{I\,Min} - V_O - 2.0V}{I_{L\,Max} + I_Q} \qquad (2)$$

where:

I_Q is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D\,Max} = (V_1 - V_O)\, I_{L\,Max} + V_1\, I_Q \qquad (3)$$

where:

$$V_1 = V_{I\,Max} - (I_{L\,Max} + I_Q)\, R1$$

The presence of R1 will affect load regulation according to the equation:

Load regulation (at constant V_I) (4)
= load regulation (at constant V_1)
+ line regulation (mV per V)
× (RI) × (ΔI_L).

As an example, consider a 15V regulator with a supply voltage of 30 ±5.0V, required to supply a maximum load current of 30 mA. I_Q is 4.3 mA, and minimum load current is to be 10 mA.

$$R1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{8}{34.3} \cong 240\Omega \qquad (5)$$

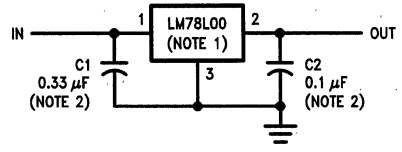
$V_1 = 35 - (30 + 4.3)\, 0.24 = 35 - 8.2 = 26.8V$

$P_{D\,Max} = (26.8 - 15)\, 30 + 26.8\, (4.3)$
$= 354 + 115$
$= 470$ mW, which permit operation up to 70°C in most applications.

Line regulation of this circuit is typically 110 mV for an input range of 25V–35V at a constant load current; i.e. 11 mV/V.

Load regulation = constant V_1 load regulation (6)
(typically 10 mV, 10 mA–30 mA I_L)
+ (11 mV/V) × 0.24 × 20 mA
(typically 53 mV)
= 63 mV for a load current change of 20 mA at a constant V_I of 30V.

Typical Applications



TL/H/10051–8

Note 1: To specify an output voltage, substitute voltage value for "00".

Note 2: Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

National Semiconductor

LM78MG/LM79MG
4-Terminal Adjustable Voltage Regulators

General Description

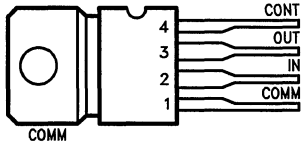
The LM78MG and LM79MG are 4-terminal adjustable voltage regulators. They are designed to deliver continuous load currents of up to 500 mA with a maximum input voltage of +40V for the positive regulator LM78MG and −40V for the negative regulator LM79MG. Output current capability can be increased to greater than 10A through use of one or more external transistors. The output voltage range of the LM78MG positive voltage regulator is 5.0V to 30V and the output voltage range of the negative LM79MG is −30V to −2.2V. For systems requiring both a positive and negative, the LM78MG and LM79MG are excellent for use as a dual tracking regulator.

Features

- Output current in excess of 0.5A
- LM78MG positive output voltage +5.0V to +30V
- LM79MG negative output voltage −30V to −2.2V
- Internal thermal overload protection
- Internal short circuit current protection
- Output transistor safe-area protection

Connection Diagrams

LM78MG

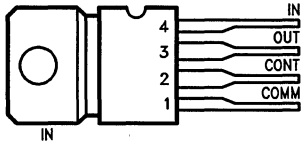


TL/H/10058–1

Top View

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

LM79MG



TL/H/10058–2

Top View

Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Ordering Information

Device Code	Package Code	Package Description
LM78MGCT	P04A	Molded 4-Lead TO-202
LM79MGCT	P04A	Molded 4-Lead TO-202

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
Internal Power Dissipation	Internally Limited
Input Voltage	
LM78MGC	+40V
LM79MGC	−40V
Control Lead Voltage	
LM78MGC	$0V \le V^+ \le V_O$
LM79MGC	$V_O^- \le V^- \le 0V$

LM78MGC

Electrical Characteristics

0°C ≤ T_A ≤ 125°C for LM78MGC, V_I = 10V, I_O = 350 mA, C_I = 0.33 µF, C_O = 0.1 µF, Test Circuit 1, unless otherwise specified

Symbol	Parameter	Conditions (Notes 1, 3)		Min	Typ	Max	Units
V_{IR}	Input Voltage Range	T_J = 25°C		7.5		40	V
V_{OR}	Output Voltage Range	$V_I = V_O + 5.0V$		5.0		30	V
V_O	Output Voltage Tolerance	$(V_O + 3.0V) \le V_I \le (V_O + 15V)$, 5.0 mA ≤ I_O ≤ 350 mA, $P_D \le 5.0W$, $V_{I\,Max}$ = 38V	T_J = 25°C			4.0	% (V_O)
						5.0	
$V_{O\,LINE}$	Line Regulation	T_J = 25°C, I_O = 200 mA, $V_O \le 10V$, $(V_O + 2.5V) \le V_I \le (V_O + 20V)$, T_J = 25°C, I_O = 200 mA, $V_O \ge 10V$				1.0	%(V_O)
$V_{O\,LOAD}$	Load Regulation	T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA, $V_I = V_O + 7.0V$				1.0	%(V_O)
I_C	Control Lead Current	T_J = 25°C			1.0	6.0	µA
						7.0	
I_Q	Quiescent Current	T_J = 25°C			2.8	5.0	mA
						6.0	
RR	Ripple Rejection	I_O = 125 mA, 8.0V ≤ V_I ≤ 18V, V_O = 5.0V, f = 2400 Hz		62	80		dB
N_O	Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, V_O = 5.0V			8	40	µV/V_O
V_{DO}	Dropout Voltage (Note 2)				2	2.5	V
I_{OS}	Short Circuit Current	V_I = 35V, T_J = 25°C				600	mA
I_{pk}	Peak Output Current	T_J = 25°C		0.4	0.8	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	V_O = 5.0V, I_O = 5.0 mA	T_A = −55°C to +25°C			0.4	mV/°C/V_O
			T_A = 25°C to 125°C			0.3	
V_C	Control Lead Voltage (Reference)	T_J = 25°C		4.8	5.0	5.2	V
				4.75		5.25	

LM79MGC

Electrical Characteristics

$0°C \le T_J \le 125°C$ for LM79MGC, $V_I = -14V$, $I_O = 350$ mA, $C_I = 2.0\ \mu F$, $C_O = 1.0\ \mu F$, Test Circuit 2, unless otherwise specified

Symbol	Parameter	Conditions (Notes 1, 3 & 5)		Min	Typ	Max	Units
V_{IR}	Input Voltage Range	$T_J = 25°C$		−40		−7.0	V
V_{OR}	Output Voltage Range	$V_I = V_O - 5.0V$		−30		−2.23	V
V_O	Output Voltage Tolerance	$(V_O - 15V) \le V_I \le (V_O - 3.0V)$, $5.0\ mA \le I_O \le 350\ mA$, $P_D \le 5.0W$, $V_{I\ Max} = -38V$	$T_J = 25°C$			4.0	% (V_O)
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $I_O = 200\ mA$, $V_O \le -10V$, $(V_O - 20V) \le V_I \le (V_O - 2.5V)$, $T_J = 25°C$, $I_O = 200\ mA$, $V_O \le -10V$				1.0	%(V_O)
$V_{O\ LOAD}$	Load Regulation	$V_I = V_O - 7.0V$, $5.0\ mA \le I_O \le 500\ mA$, $T_J = 25°C$				1.0	%(V_O)
I_C	Control Lead Current	$T_J = 25°C$				2.0	μA
						3.0	
I_Q	Quiescent Current	$T_J = 25°C$			0.5	2.5	mA
						3.5	
RR	Ripple Rejection	$T_J = 25°C$, $I_O = 125\ mA$, $V_I = -13V$, $V_O = -5.0V$, $f = 2400\ Hz$		50			dB
N_O	Noise	$10\ Hz \le f \le 100\ kHz$, $V_O = -8.0V$, $I_L = 50\ mA$			25	80	μV/V_O
V_{DO}	Dropout Voltage				1.1	2.3	V
I_{OS}	Short Circuit Current	$V_I = 35V$, $T_J = 25°C$				600	mA
I_{pk}	Peak Output Current			0.4	0.65	1.4	mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = -5.0V$, $I_O = -5.0\ mA$	$T_A = -55°C$ to $+25°C$			0.3	mV/°C/V_O
			$T_A = 25°C$ to $125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		−2.32	−2.23	−2.14	V
				−2.35		−2.11	

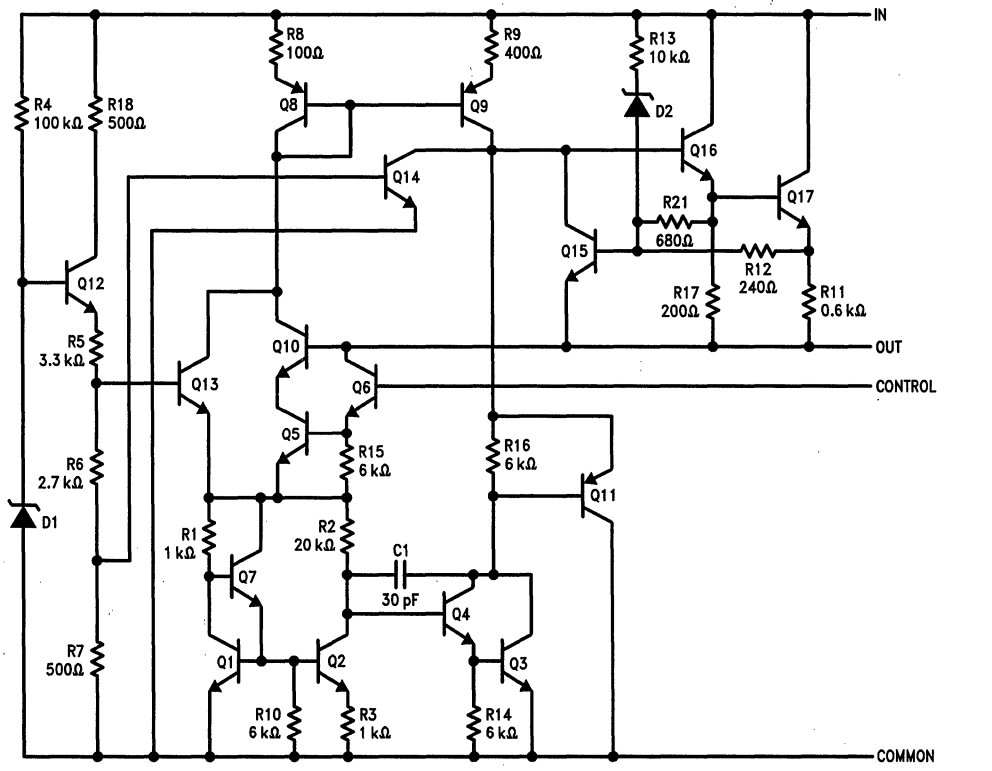
Note 1: V_O is defined for the LM78MGC as $V_O = \frac{R1 + R2}{R2}(5.0)$; the LM79MGC as $V_O = \frac{R1 + R2}{R2}(-2.23)$.

Note 2: Dropout voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.

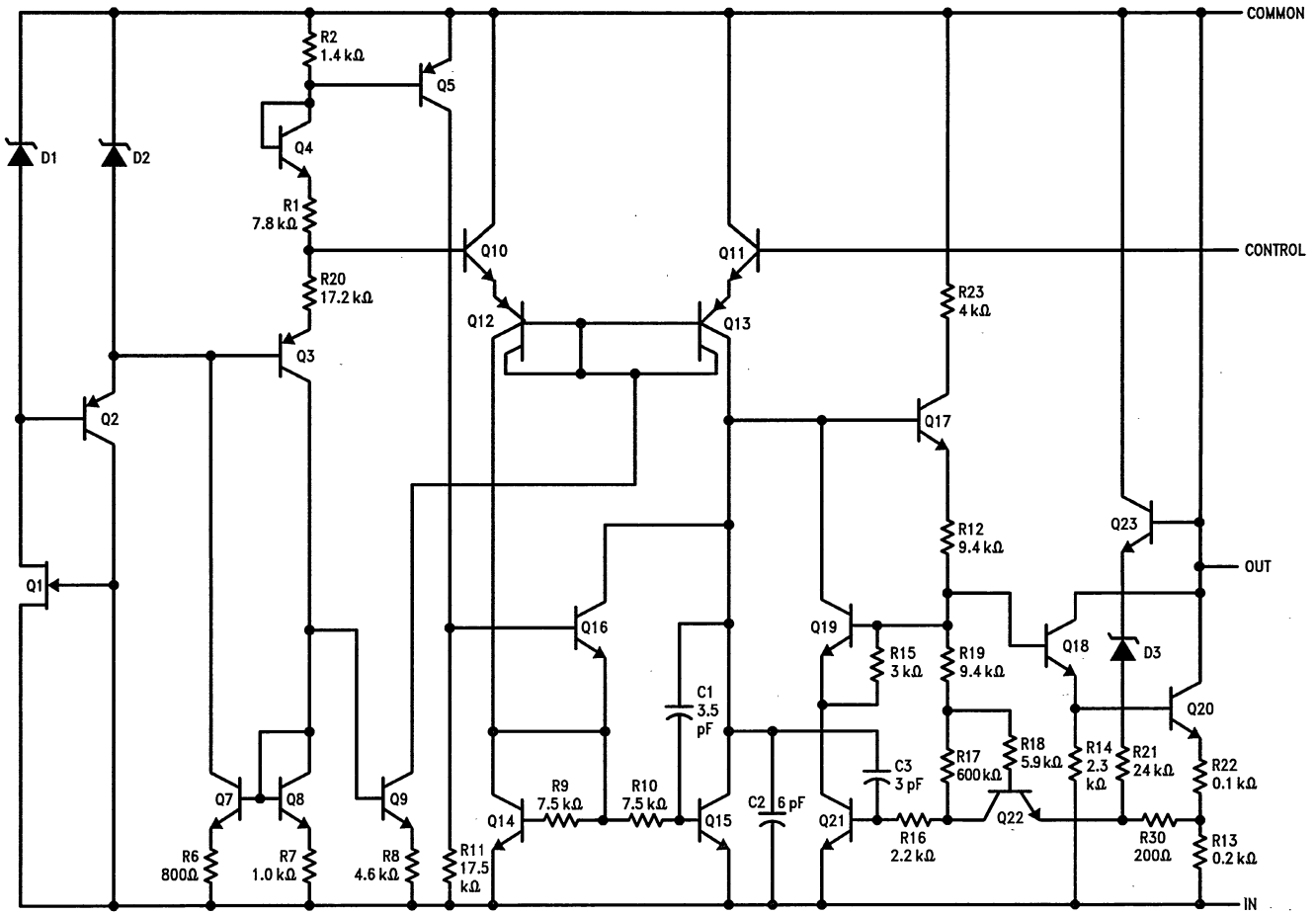
Note 3: All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Note 4: The convention for negative regulators is the Algebraic value, thus −15V is less than −10V.

LM78MG Equivalent Circuit



TL/H/10058–3



TL/H/10058–4

Note 1: Resistor values in Ω unless otherwise noted.

Design Considerations

The LM78MG and LM79MG variable voltage regulators have an output voltage which varies from V_{CONT} to typically

$$V_I - 2.0V \text{ by } V_O = V_{CONT}\frac{(R1 + R2)}{R2}$$

The nominal reference in the LM78MG is 5.0V and LM79MG is −2.23V. If we allow 1.0 mA to flow in the control swing to eliminate bias current effects, we can make R2 = 5 kΩ in the LM78MG. The output voltage is then: V_O = (R1 + R2) Volts, where R1 and R2 are in kΩs.

Example: If R2 = 5.0 kΩ and R1 = 10 kΩ then
V_O = 15V nominal, for the LM78MG;
R2 = 2.2 kΩ and R1 = 12.8 kΩ then
V_O = −15.2V nominal, for the LM79MG.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both LM78MG and LM79MG regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
Power Watt	8.0	12.0	70	75

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$\frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$
$$T_A + P_D\theta_{JA} \text{ (without heat sink)}$$

Where

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{CA} = Case-to-Ambient Thermal Resistance
θ_{CS} = Case-to-Heat Sink Thermal Resistance
θ_{SA} = Heat Sink-to-Ambient Thermal Resistance
θ_{JA} = Junction-to-Ambient Thermal Resistance

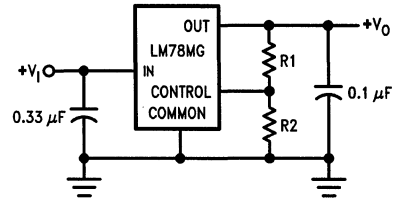
Typical Applications for LM78MG (Note 1)

Bypass capacitors are recommended for stable operation of the LM78MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (0.33 μF on the input, 0.1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Note 1: All resistor values in ohms.

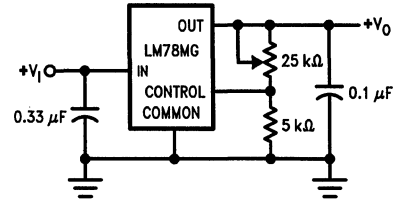
Basic Positive Regulator



TL/H/10058–8

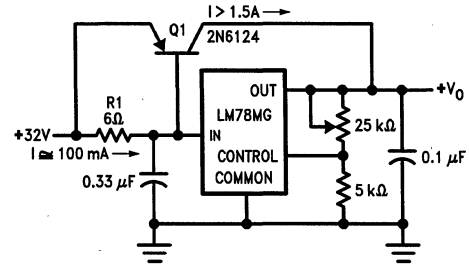
$$V_O = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Positive 5.0V to 30V Adjustable Regulator



TL/H/10058–9

Positive 5.0V to 30V Adjustable Regulator I_O > 1.5A

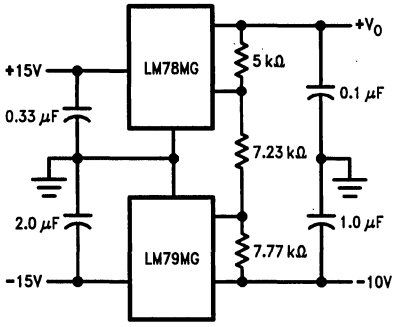


TL/H/10058–10

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{R\,Max(\beta)} - I_O}$$

Typical Applications for LM78MG (Note 1) (Continued)

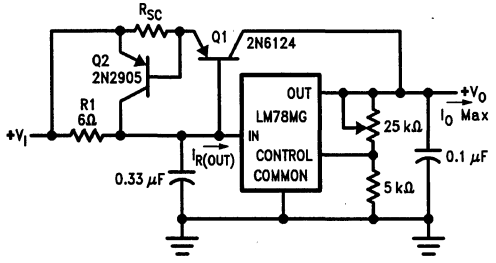
± 10V, 500 mA Dual Tracking Regulator



TL/H/10058–11

Note: External series pass device is not short circuit protected.

Positive High Current Short Circuit Protected Regulator

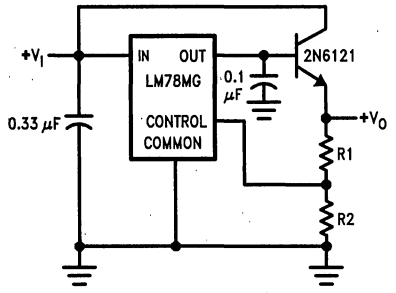


TL/H/10058–14

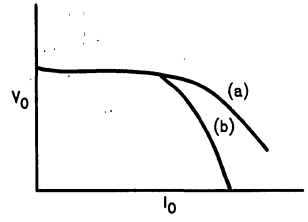
$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R\ Max(\beta + 1)} - I_{O\ Max}}$$

If load is not ground referenced, connect reverse biased diodes from outputs to ground.

Positive High-Current Voltage Regulator



TL/H/10058–12



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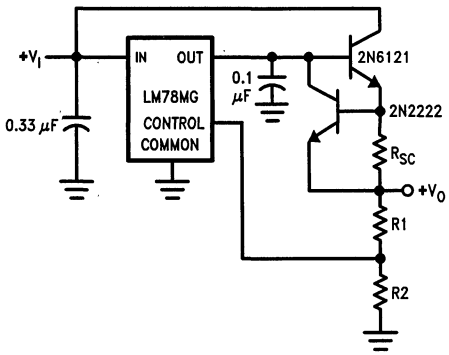
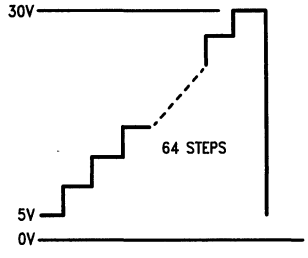
External Series Pass (a)



TL/H/10058–15

Short-Circuit Limit (b)

Output Waveform



TL/H/10058–16

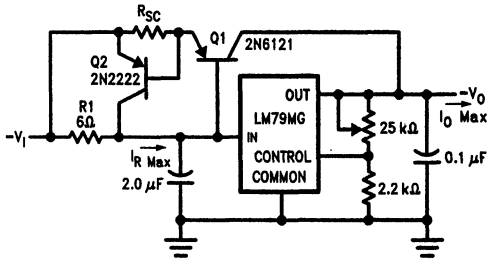
Note 1: All resistor values in ohms.

Typical Applications for LM79MG (Note 1)

Bypass capacitors are recommended for stable operation of the LM79MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.0 μF on the input, 1.0 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

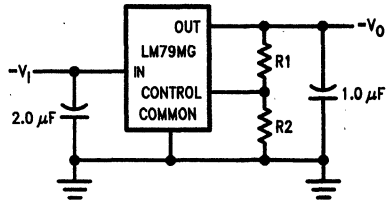
Negative High Current Short Circuit Protected Regulator



TL/H/10058–17

$$T_1 = \frac{\beta V_{BE(Q1)}}{I_{R\ Max(\beta)} - I_{O\ Max}}$$

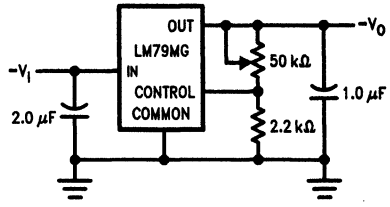
Basic Negative Regulator



TL/H/10058–19

$$V_O = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

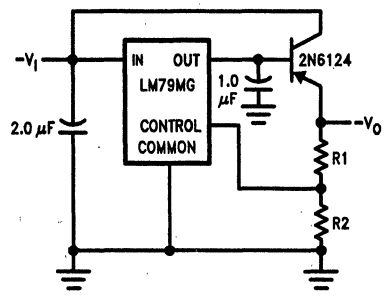
−30V to −2.2V Adjustable Regulator



TL/H/10058–21

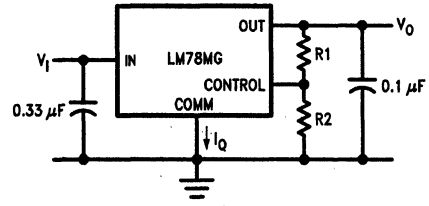
Note 1: All resistor values in ohms.

Negative High Current Voltage Regulator External Series Pass



TL/H/10058–18

LM78MG Test Circuit 1

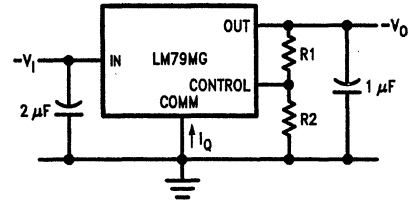


TL/H/10058–20

$$V_O = \left(\frac{R1 + R2}{R2}\right)V_{CONT}$$

V_{CONT} Nominally = 5V

LM79MG Test Circuit 2



TL/H/10058–22

$$V_O = \left(\frac{R1 + R2}{R2}\right)V_{CONT}$$

V_{CONT} Nominally = −2.23V

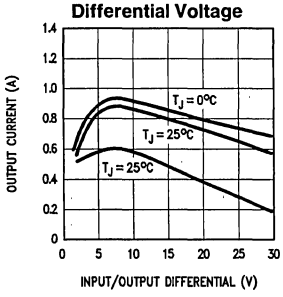
Recommended R2 current ≈ 1 mA

∴R2 = 5 kΩ (LM78MG)

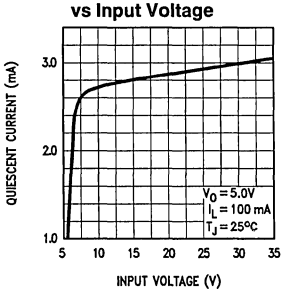
R2 = 2.2 kΩ (LM79MG)

Typical Performance Characteristics for LM78MG

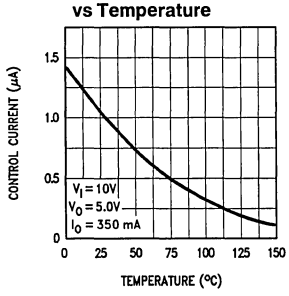
Peak Output Current vs Input/Output Differential Voltage



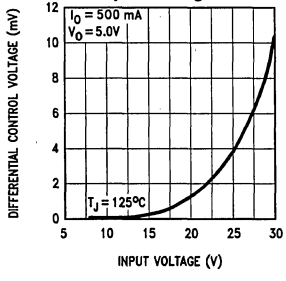
Quiescent Current vs Input Voltage



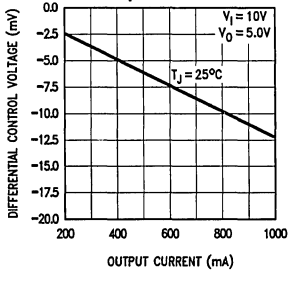
Control Current vs Temperature



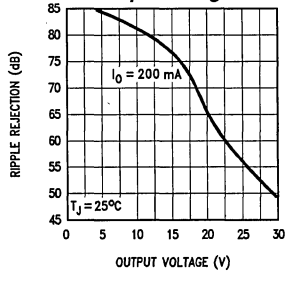
Differential Control Voltage vs Input Voltage



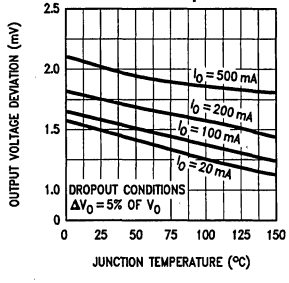
Differential Control Voltage vs Output Current



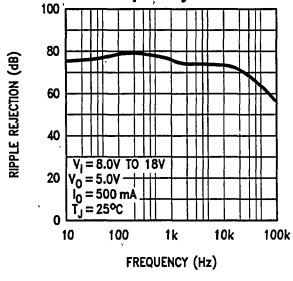
Ripple Rejection vs Output Voltage



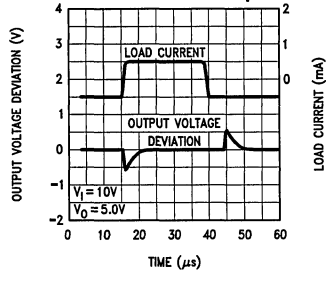
Dropout Voltage vs Junction Temperature



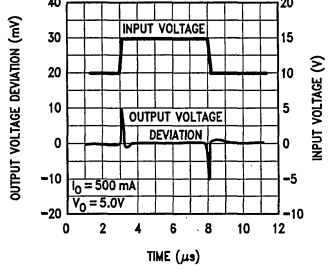
Ripple Rejection vs Frequency



Load Transient Response



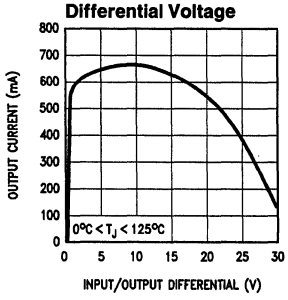
Line Transient Response



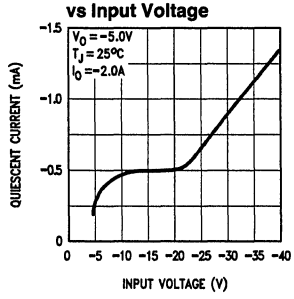
TL/H/10058–5

Typical Performance Characteristics for LM79MG

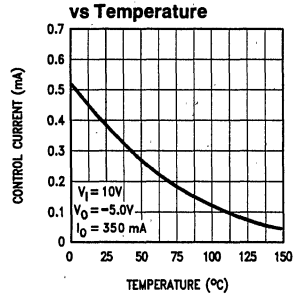
Peak Output Current vs Input/Output Differential Voltage



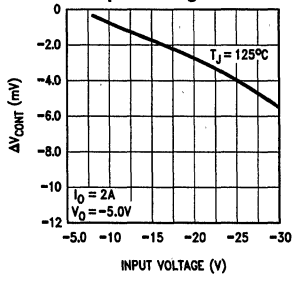
Quiescent Current vs Input Voltage



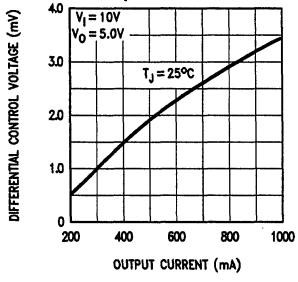
Control Current vs Temperature



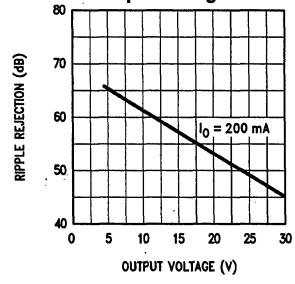
Differential Control Voltage vs Input Voltage



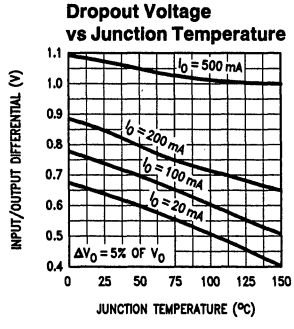
Differential Control Voltage vs Output Current



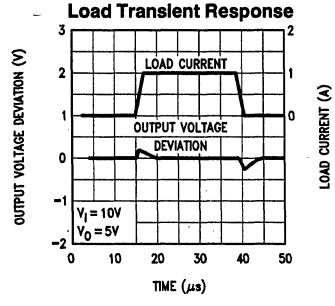
Ripple Rejection vs Output Voltage



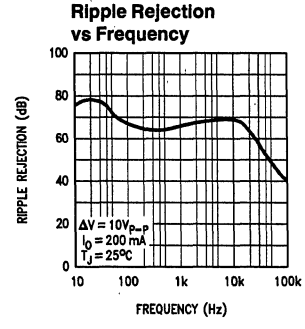
Dropout Voltage vs Junction Temperature



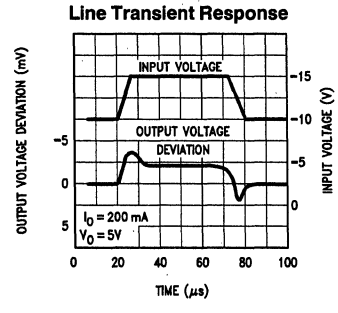
Load Transient Response



Ripple Rejection vs Frequency



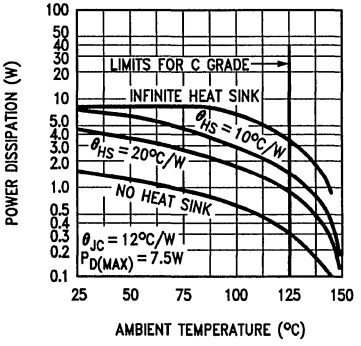
Line Transient Response



TL/H/10058-6

Typical Performance Characteristics for LM78MG and LM79MG

Worst Case Power Dissipation vs Ambient Temperature



TL/H/10058–7

National Semiconductor

LM78MXX Series
3-Terminal Positive Voltage Regulators

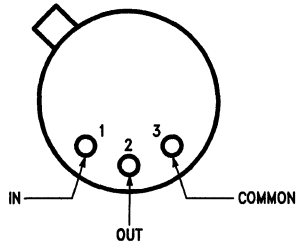
General Description

The LM78M00 series of 3-terminal medium current positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver in excess of 0.5A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Features

- Output current in excess of 0.5A
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Output transistor safe-area compensation
- Available in JEDEC TO-220 and TO-39 packages
- Output voltages of 5V, 6V, 8V, 12V, 15V, and 24V

Connection Diagrams

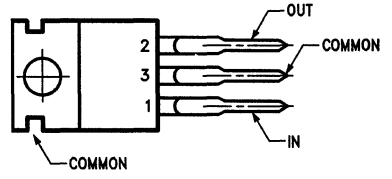


TL/H/10053–1

Lead 3 connected to case.

Top View

Order Number LM78M05CH, LM78M06CH, LM78M08CH, LM78M12CH, LM78M15CH or LM78M24CH
See NS Package Number H03B



TL/H/10053–2

Top View

Lead 3 connected to tab.

Order Number LM78M05CT, LM78M06CT, LM78M08CT, LM78M12CT, LM78M15CT or LM78M24CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
TO-39 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to +150°C
Operating Junction Temperature Range	0°C to +150°C
Lead Temperature	
TO-39 Metal Can (Soldering, 60 sec.)	300°C
TO-220 Package (Soldering, 60 sec.)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0V to 15V	35V
24V	40V
ESD Susceptibility	(to be determined)

LM78M05C Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 10V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$7.0V \le V_I \le 25V$, $I_O = 200$ mA		3.0	100	mV
				$8.0V \le V_I \le 20V$, $I_O = 200$ mA		1.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 500$ mA		20	100	mV
				$5.0\ mA \le I_O \le 200$ mA		10	50	
V_O	Output Voltage		$7.0V \le V_I \le 20V$, $5.0\ mA \le I_O \le 350$ mA		4.75		5.25	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	$8.0V \le V_I \le 25V$, $I_O = 200$ mA				0.8	mA
		with Load	$5.0\ mA \le I_O \le 350$ mA				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 125$ mA, $T_J = 25°C$		62	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			300		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.0		mV/°C

LM78M06C Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 11V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		5.75	6.0	6.25	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.0V \le V_I \le 25V$, $I_O = 200$ mA		5.0	100	mV
				$9.0V \le V_I \le 20V$, $I_O = 200$ mA		1.5	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 500$ mA		20	120	mV
				$5.0\ mA \le I_O \le 200$ mA		10	60	
V_O	Output Voltage		$8.0V \le V_I \le 21V$, $5.0\ mA \le I_O \le 350$ mA		5.7		6.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	$9.0V \le V_I \le 25V$, $I_O = 200$ mA				0.8	mA
		with Load	$5.0\ mA \le I_O \le 350$ mA				0.5	

LM78M06C
Electrical Characteristics (Continued)

$0°C \le T_A \le 125°C$, $V_I = 11V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified.

Symbol	Parameter	Conditions (Note 1)	Min	Typ	Max	Units
N_O	Noise	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz		45		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$	59	80		dB
V_{DO}	Dropout Voltage	$T_A = 25°C$		2.0		V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35V$		270		mA
I_{pk}	Peak Output Current	$T_J = 25°C$		700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA		0.5		mV/°C

LM78M08C
Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 14V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	10.5V ≤ V_I ≤ 25V, I_O = 200 mA		6.0	100	mV
				11V ≤ V_I ≤ 20V, I_O = 200 mA		2.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 500 mA		25	160	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	80	
V_O	Output Voltage		10.5V ≤ V_I ≤ 23V, 5.0 mA ≤ I_O ≤ 350 mA		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			4.6	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	10.5V ≤ V_I ≤ 25V, I_O = 200 mA				0.8	mA
		with Load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			52		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$		56	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35V$			250		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			0.5		mV/°C

LM78M12C
Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 19V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter	Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage	$T_J = 25°C$		11.5	12.0	12.5	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	14.5V ≤ V_I ≤ 30V, I_O = 200 mA		8.0	100	mV
			16V ≤ V_I ≤ 25V, I_O = 200 mA		2.0	50	

LM78M12C
Electrical Characteristics (Continued)

$0°C \le T_A \le 125°C$, $V_I = 19V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 500 mA		25	240	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	120	
V_O	Output Voltage		14.5V ≤ V_I ≤ 27V, 5.0 mA ≤ I_O ≤ 350 mA		11.4		12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			4.8	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	14.5V ≤ V_I ≤ 30V, I_O = 200 mA				0.8	mA
		with Load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			75		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, V_I = 17V, $T_J = 25°C$		55	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, V_I = 35V			240		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			1.0		mV/°C

LM78M15C
Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 23V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified (Continued)

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		14.4	15.0	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	17.5V ≤ V_I ≤ 30V, I_O = 200 mA		10	100	mV
				20V ≤ V_I ≤ 28V, I_O = 200 mA		3.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 500 mA		25	300	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	150	
V_O	Output Voltage		17.5V ≤ V_I ≤ 30V, 5.0 mA ≤ I_O ≤ 350 mA		14.25		15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			4.8	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	17.5V ≤ V_I ≤ 30V, I_O = 200 mA				0.8	mA
		with Load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			90		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, V_I = 20V, $T_J = 25°C$		54	70		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, V_I = 35V			240		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			1.0		mV/°C

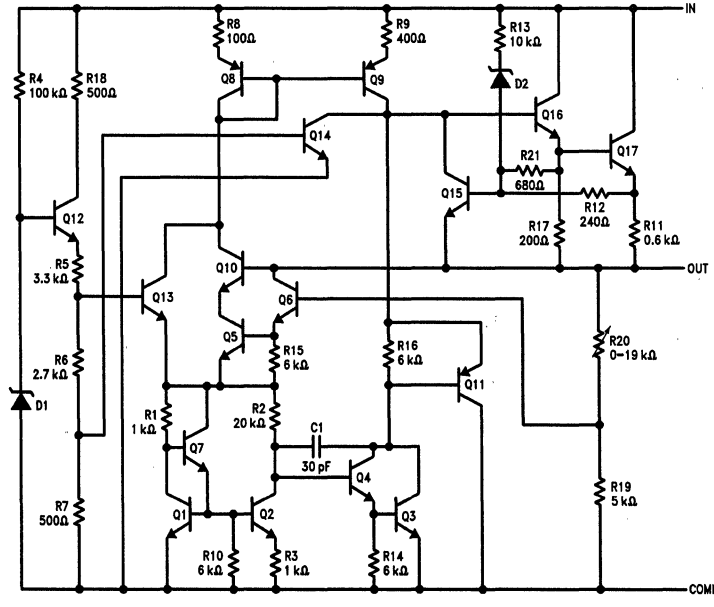
LM78M24C
Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = 33V$, $I_O = 350$ mA, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$27V \le V_I \le 38V$, $I_O = 200$ mA		10	100	mV
				$28V \le V_I \le 36V$, $I_O = 200$ mA		5.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 500$ mA		30	480	mV
				$5.0\ mA \le I_O \le 200$ mA		10	240	
V_O	Output Voltage		$27V \le V_I \le 38V$, $5.0\ mA \le I_O \le 350$ mA		22.8		25.2	V
I_Q	Quiescent Current		$T_J = 25°C$			5.0	8.0	mA
ΔI_Q	Quiescent Current Change	with Line	$27V \le V_I \le 38V$, $I_O = 200$ mA				0.8	mA
		with Load	$5.0\ mA \le I_O \le 350$ mA				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			170		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 125$ mA, $V_I = 30V$, $T_J = 25°C$		50	70		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 35°C$, $V_I = 35V$			240		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.2		mV/°C

Note 1: All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($T_W \le 10$ ms, duty cycle $\le 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

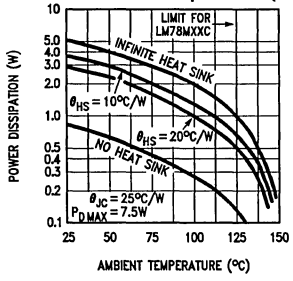
Equivalent Circuit



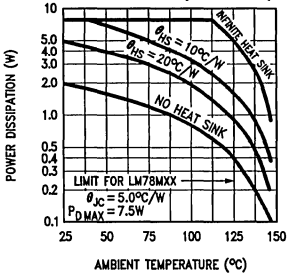
TL/H/10053–3

Typical Performance Characteristics

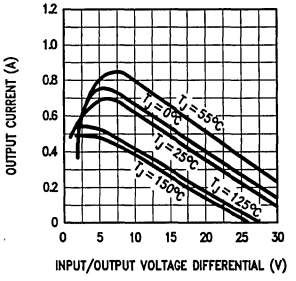
Worst Case Power Dissipation vs Ambient Temperature (TO-39)



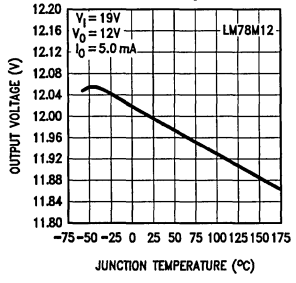
Worst Case Power Dissipation vs Ambient Temperature (TO-220)



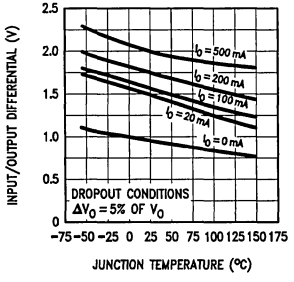
Peak Output Current vs Input/Output Voltage Differential



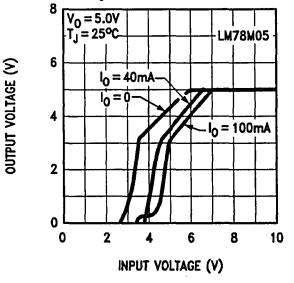
Output Voltage vs Junction Temperature



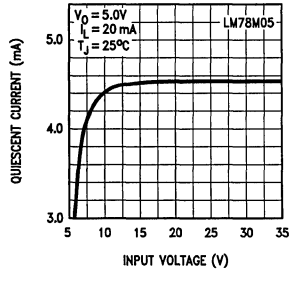
Dropout Voltage vs Junction Temperature



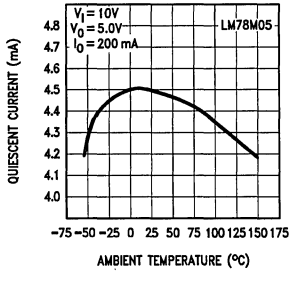
Dropout Characteristics



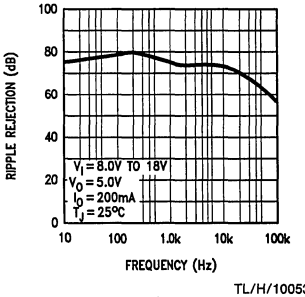
Quiescent Current vs Input Voltage



Quiescent Current vs Temperature



Ripple Rejection vs Frequency

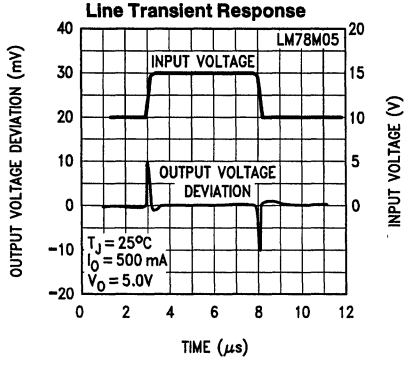


TL/H/10053–4

Note: Other LM78M00 Series devices have similar curves.

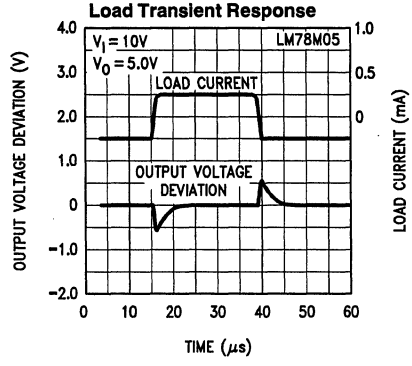
Typical Performance Characteristics (Continued)

Line Transient Response



TL/H/10053–5

Load Transient Response



TL/H/10053–6

Design Considerations

The LM78MXX fixed voltage regulator series has thermal-overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (+125°C for LM78MXXC) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJ_C	Max θJ_C	Typ θJ_A	Max θJ_A
TO-39	18	25	120	140
TO-220	3.0	5.0	60	40

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (Without a Heat Sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

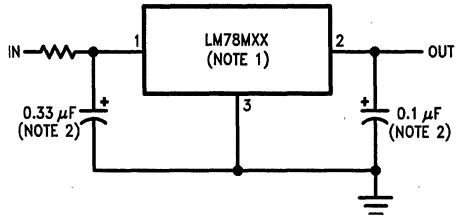
$= T_A + P_D\,\theta_{JA}$ (Without a Heat Sink)

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JC} = Junction to Case Thermal Resistance
- θ_{CA} = Case-to-Ambient Thermal Resistance
- θ_{CS} = Case-to-Heat Sink to Resistance
- θ_{SA} = Heat Sink-to-Ambient Thermal Resistance
- θ_{JA} = Junction-to-Ambient Thermal Resistance

Typical Applications

Fixed Output Regulator



TL/H/10053–7

Note 1: To specify an output voltage, substitue voltage value for "XX".

Note 2: Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

National Semiconductor

LM79XX Series 3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

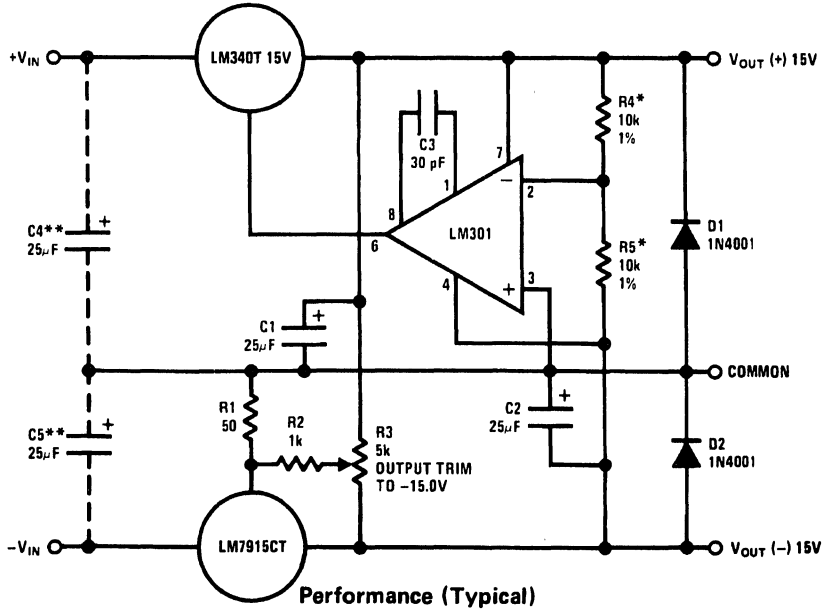
For applications requiring other voltages, see LM137 data sheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

Typical Applications

±15V, 1 Amp Tracking Regulators



Performance (Typical)

TL/H/7340–1

	(−15)	(+15)
Load Regulation at ΔI_L = 1A	40 mV	2 mV
Output Ripple, C_{IN} = 3000 μF, I_L = 1A	100 μVrms	100 μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150 μVrms	150 μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 3" from regulators.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
(V_O = 5V)	−35V
(V_O = 12V and 15V)	−40V
Input-Output Differential	
(V_O = 5V)	25V
(V_O = 12V and 15V)	30V
Power Dissipation (Note 1)	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	230°C

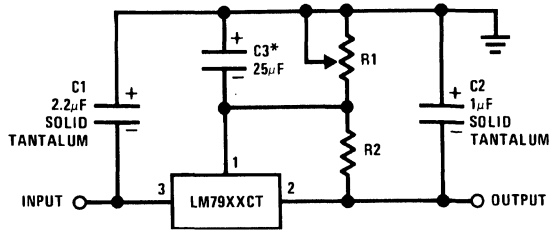
Electrical Characteristics

Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2 µF, C_{OUT} = 1 µF, 0°C ≤ T_J ≤ +125°C, Power Dissipation ≤ 1.5W.

Part Number			LM7905C			Units
Output Voltage			5V			
Input Voltage (unless otherwise specified)			−10V			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	
V_O	Output Voltage	T_J = 25°C	−4.8	−5.0	−5.2	V
		5 mA ≤ I_{OUT} ≤ 1A, P ≤ 15W	−4.75		−5.25	V
			(−20 ≤ V_{IN} ≤ −7)			V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		8	50	mV
				(−25 ≤ V_{IN} ≤ −7)		V
				2	15	mV
				(−12 ≤ V_{IN} ≤ −8)		V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)				mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	100	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
I_Q	Quiescent Current	T_J = 25°C		1	2	mA
ΔI_Q	Quiescent Current Change	With Line			0.5	mA
				(−25 ≤ V_{IN} ≤ −7)		V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		125		µV
	Ripple Rejection	f = 120 Hz	54	66		dB
				(−18 ≤ V_{IN} ≤ −8)		V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0 C ≤ T_J ≤ 100°C		0.4		mV/°C

Typical Applications (Continued)

Variable Output



TL/H/7340–2

*Improves transient response and ripple rejection. Do not increase beyond 50 µF.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

LM7905CT	300Ω
LM7912CT	750Ω
LM7915CT	1k

Electrical Characteristics (Continued) Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2 µF, C_{OUT} = 1 µF, 0°C ≤ T_J ≤ +125°C, Power Dissipation = 1.5W.

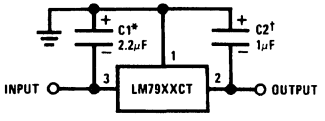
Part Number			LM7912C			LM7915C			Units
Output Voltage			12V			15V			
Input Voltage (unless otherwise specified)			−19V			−23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C	−11.5	−12.0	−12.5	−14.4	−15.0	−15.6	V
		5 mA ≤ I_{OUT} ≤ 1A,	−11.4		−12.6	−14.25		−15.75	V
		P ≤ 15W	(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)			V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		5	80		5	100	mV
				(−30 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)		V
				3	30		3	50	mV
				−22 ≤ V_{IN} ≤ −16)			(−26 ≤ V_{IN} ≤ −20)		V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)		15	200		15	200	mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	200		15	200	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	75		5	75	mV
I_Q	Quiescent Current	T_J = 25°C		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line			0.5			0.5	mA
				(−30 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)		V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		300			375		µV
	Ripple Rejection	f = 120 Hz	54	70		54	70		dB
			(−25 ≤ V_{IN} ≤ −15)			(−30 ≤ V_{IN} ≤ −17.5)			V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1			1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2			2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0 C ≤ T_J ≤ 100°C		−0.8			−1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Typical Applications (Continued)

Fixed Regulator



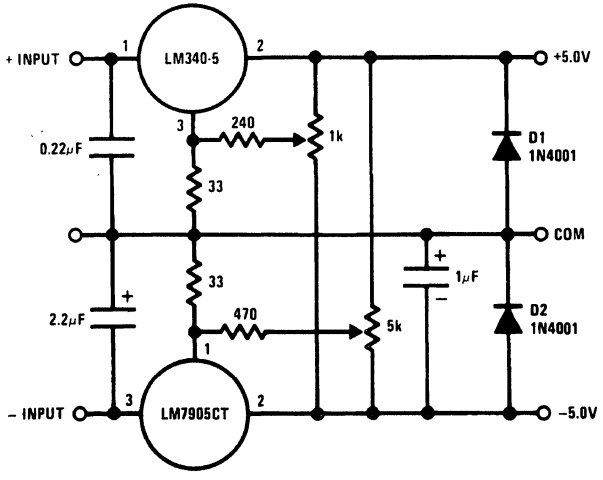
TL/H/7340–3

*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25 µF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 µF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100 µF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

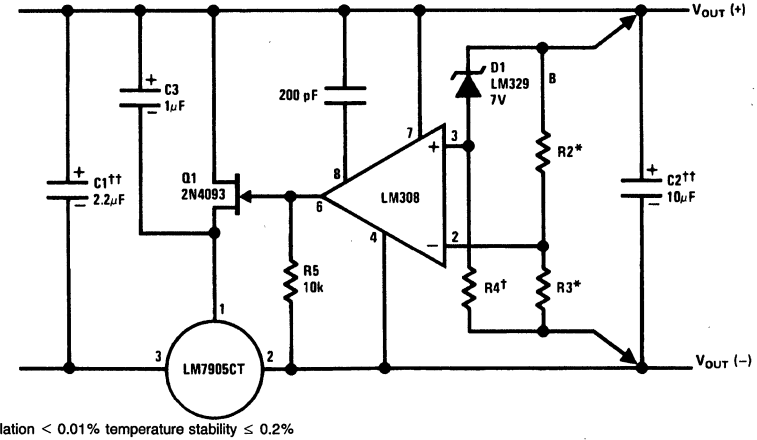
Dual Trimmed Supply



TL/H/7340–4

Typical Applications (Continued)

High Stability 1 Amp Regulator



Load and line regulation < 0.01% temperature stability ≤ 0.2%

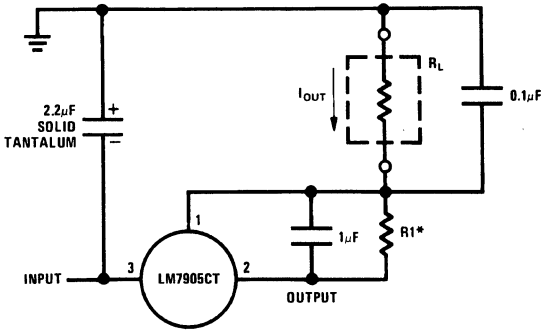
TL/H/7340–5

†Determine Zener current

††Solid tantalum

*Select resistors to set output voltage. 2 ppm/°C tracking suggested

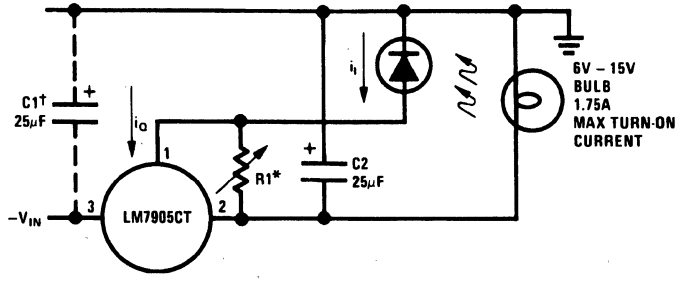
Current Source



*I_{OUT} = 1 mA + $\frac{5V}{R1}$

TL/H/7340–7

Light Controllers Using Silicon Photo Cells

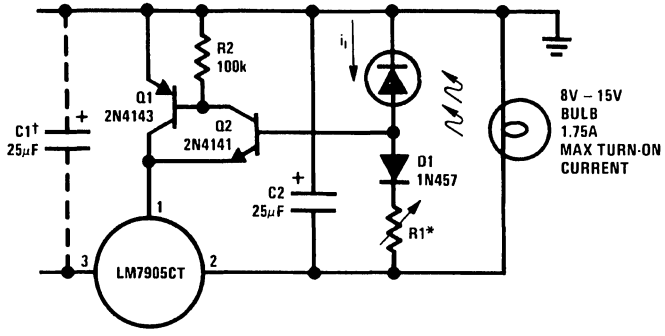


TL/H/7340–8

*Lamp brightness increase until $i_I = i_Q$ (≈ 1 mA) + 5V/R1.

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

Typical Applications (Continued)



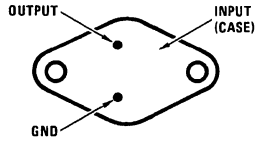
TL/H/7340–9

*Lamp brightness increases until i_I = 5V/R1 (I_I can be set as low as 1 μA)

†Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

Connection Diagrams

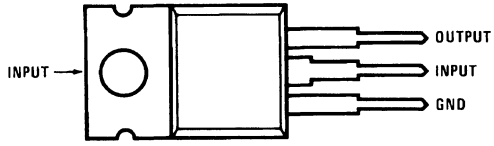
TO-3 Package



TL/H/7340–10

Bottom View
Order Number LM7905CK, LM7912CK or LM7915CK
See NS Package Number KC02A

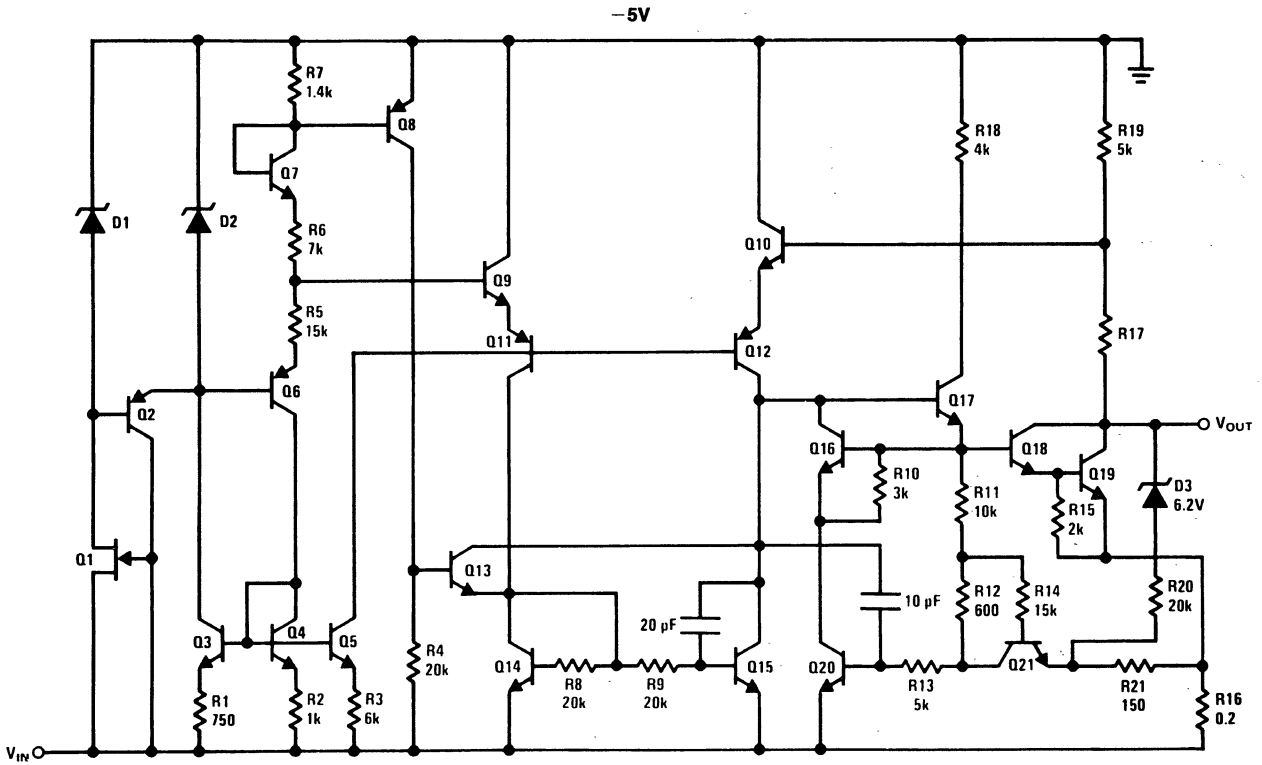
TO-220 Package



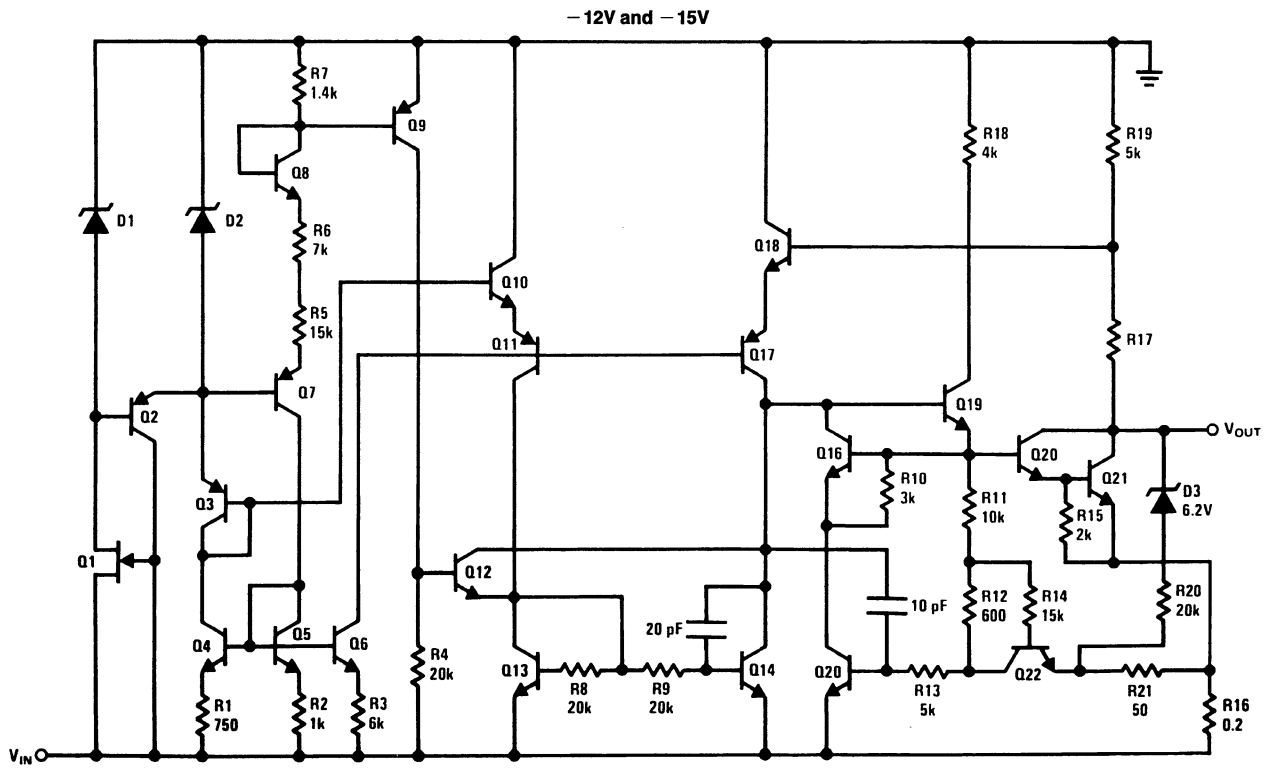
TL/H/7340–11

Top View
Order Number LM7905CT, LM7912CT or LM7915CT
See NS Package Number TO3B

Schematic Diagrams



TL/H/7340–12


−12V and −15V
R7
1.4k
Q9
Q8
D1
D2
R6
7k
R5
15k
Q7
Q2
Q3
Q1
Q4
Q5
Q6
R1
750
R2
1k
R3
6k
R4
20k
Q10
Q11
Q12
Q13
R8
20k
R9
20k
20 pF
Q14
Q18
Q17
R18
4k
R19
5k
R17
Q19
Q16
R10
3k
R11
10k
Q20
Q21
D3
6.2V
R15
2k
10 pF
R12
600
R14
15k
R20
20k
Q20
R13
5k
Q22
R21
50
R16
0.2
VIN
VOUT

TL/H/7340–13

National Semiconductor

LM7900 Series
3-Terminal Negative Voltage Regulators

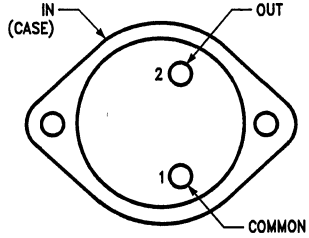
General Description

The LM7900 series of monolithic 3-terminal negative regulators are intended as complements to the popular LM7800 series of positive voltage regulators, and they are available in voltage options from −5.0V to −15V. The LM7900 series employ internal current-limiting, thermal shutdown, and safe-area compensation, making them virtually indestructible.

Features

- Output current in excess of 1.0A
- Internal thermal overload protection
- Internal short circuit current-limiting
- Output transistor safe-area compensation
- Available in JEDEC TO-220 and TO-3 packages
- Output voltage of −8V (See Note)

Connection Diagrams

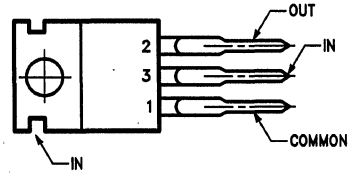


TL/H/10050–1

Top View

Order Number LM7908K and LM7908CK
See NS Package Number K02A

Note: See the LM79xx datasheet in the General Purpose Linear Databook for specifications on products in this series with −5V, −12V, and −15V outputs. Refer to the LM120/LM320 datasheet for −5V, −12V, and −15V regulators specified over extended temperature ranges.



TL/H/10050–2

Lead 3 connected to case.

Top View

Order Number LM7908CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- TO-3 Metal Can: −65°C to +175°C
- TO-220 Package: −65°C to +150°C

Operating Junction Temperature Range
- Extended (LM7900): −55°C to +150°C
- Commercial (LM7900C): 0°C to +150°C

Lead Temperature
- TO-3 Metal (soldering, 60 sec.): 300°C
- TO-220 Package (soldering, 10 sec.): 265°C

Power Dissipation: Internally Limited

Input Voltage
- −5V to −15V: −35V

ESD Susceptibility: 2000V

Note 1: The convention for Negative Regulators is the Algebraic value, thus −15V is less then −10V.

LM7908
Electrical Characteristics

$-55°C \le T_A \le 125°C$, $V_I = -14V$, $I_O = 500$ mA, $C_I = 2.0\ \mu F$, $C_O = 1.0\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		−7.7	−8.0	−8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-10.5V \le V_I \le -25V$		6.0	80	mV
				$-11V \le V_I \le -17V$		2.0	40	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	100	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	40	
V_O	Output Voltage		$-11.5V \le V_I \le -23V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		−7.6		−8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			3.5	7.0	mA
ΔI_Q	Quiescent Current Change	With Line	$-11.5V \le V_I \le -25V$				1.0	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -13V$, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			1.1	2.3	V
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $-55°C \le T_A \le 125°C$				0.3	$mV/°C/V_O$
I_{OS}	Output Short Circuit Current		$V_I = -35V$, $T_J = 25°C$				1.2	A

1

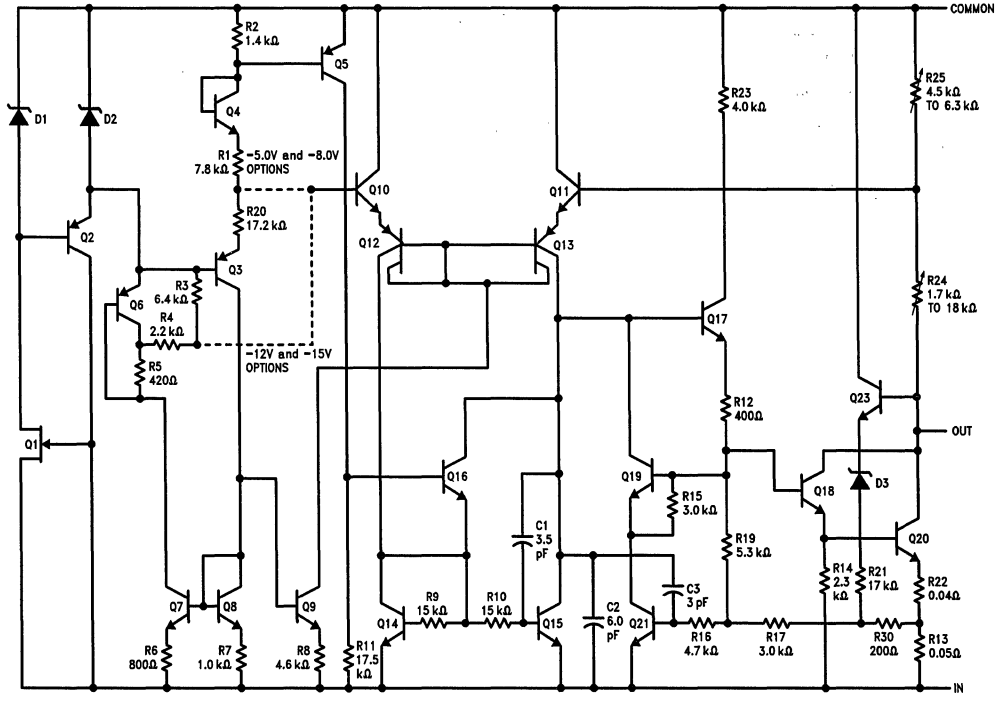
LM7908C
Electrical Characteristics

$0°C \le T_A \le 125°C$, $V_I = -14V$, $I_O = 500$ mA, $C_I = 2.0\ \mu F$, $C_O = 1.0\ \mu F$, unless otherwise specified

Symbol	Parameter		Conditions (Note 1)		Min	Typ	Max	Units
V_O	Output Voltage		$T_J = 25°C$		−7.7	−8.0	−8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-10.5V \le V_I \le -25V$		6.0	160	mV
				$-11V \le V_I \le -17V$		2.0	80	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \le I_O \le 1.5A$		12	160	mV
				$250\ mA \le I_O \le 750\ mA$		4.0	80	
V_O	Output Voltage		$-10.5V \le V_I \le 23V$, $5.0\ mA \le I_O \le 1.0A$, $P \le 15W$		−7.6		−8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			3.5	7.0	mA
ΔI_Q	Quiescent Current Change	With Line	$-10.5V \le V_I \le -25V$				1.0	mA
		With Load	$5.0\ mA \le I_O \le 1.0A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \le f \le 100\ kHz$			200		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -13V$, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0A$, $T_J = 25°C$			1.1		V
I_{pk}	Peak Output Current		$T_J = 25°C$			2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \le T_A \le 125°C$			0.6		mV/°C

Note 1: All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \le 10$ ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

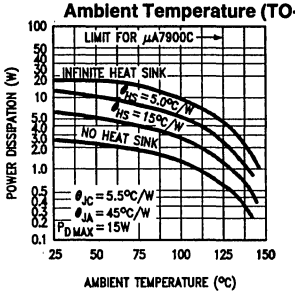
Equivalent Circuit



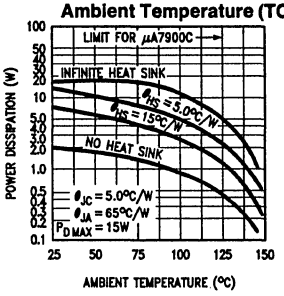
TL/H/10050–3

Typical Performance Characteristics

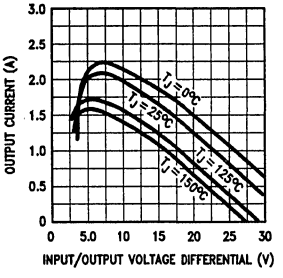
Worst Case Power Dissipation vs Ambient Temperature (TO-3)



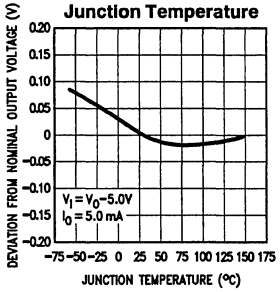
Worst Case Power Dissipation vs Ambient Temperature (TO-220)



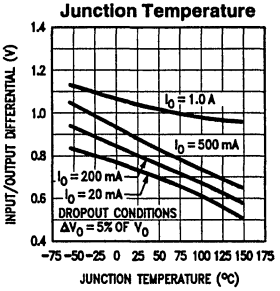
Peak Output Current vs Input/Output Voltage Differential



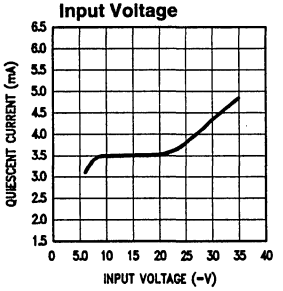
Output Voltage vs Junction Temperature



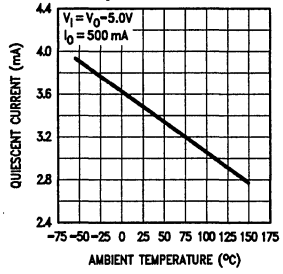
Dropout Voltage vs Junction Temperature



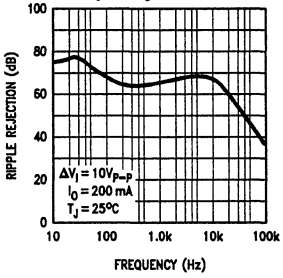
Quiescent Current vs Input Voltage



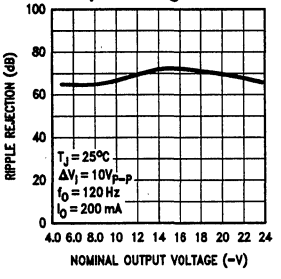
Quiescent Current vs Temperature



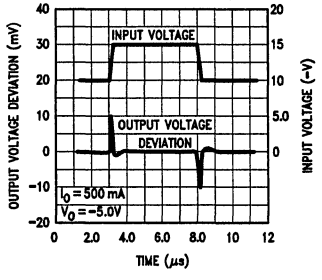
Ripple Rejection vs Frequency



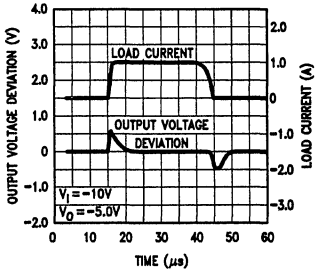
Ripple Rejection vs Output Voltages



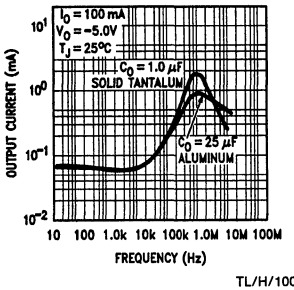
Line Transient Response



Load Transient Response



Output Impedance vs Frequency



TL/H/10050-4

Design Considerations

The LM7900 fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for LM7900, 125°C for LM7900C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
TO-3	3.5	5.5	40	35
TO-220	3.0	5.0	60	40

$$P_{D\,MAX} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\,Max}\,T_A}{\theta_{JA}}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$ (without heat sink)

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

$= T_A + P_D\theta_{JA}$ (without heat sink)

Where:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation

θ_{JA} = Junction-to-Ambient Thermal Resistance

θ_{JC} = Junction-to-Case Thermal Resistance

θ_{CA} = Case-to-Ambient Thermal Resistance

θ_{CS} = Case-to-Heat Sink Thermal Resistance

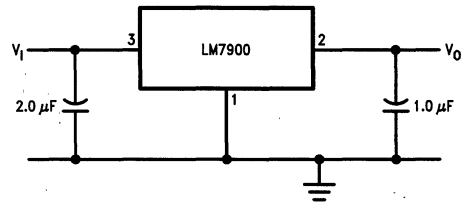
θ_{SA} = Heat Sink-to-Ambient Thermal Resistance

Typical Applications

Bypass capacitors are necessary for stable operation of the LM7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response by the regulator.

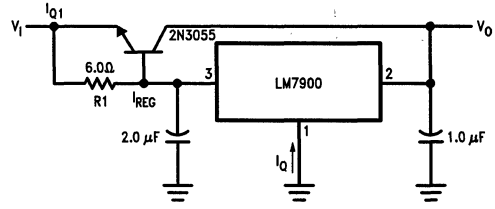
The bypass capacitors, (2.0 μF on the input, 1.0 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



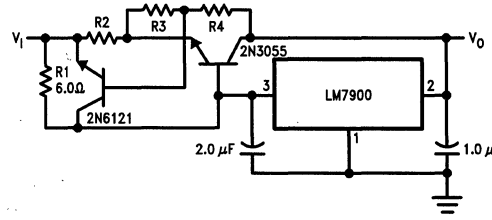
TL/H/10050–5

High Current Voltage Regulator



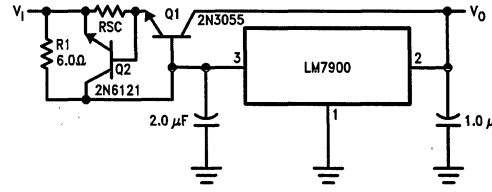
TL/H/10050–6

Output Current HIGH, Foldback Current-Limited



TL/H/10050–7

Output Current HIGH, Short Circuit Protected



TL/H/10050–8

$$RSC = \frac{V_{BE(Q2)}}{I_{OS}}$$

National Semiconductor

LM79LXXAC Series 3-Terminal Negative Regulators

General Description

The LM79LXXAC series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V with output current capabilities in excess of 100 mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead TO-92 package, and SO-8; 8 lead package.

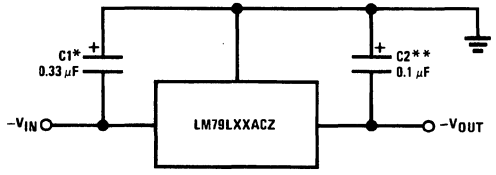
For output voltage other than −5V, −12V and −15V the LM137L series provides an output voltage range from 1.2V to 47V.

Features

- Preset output voltage error is less than ±5% overload, line and temperature
- Specified at an output current of 100 mA
- Easily compensated with a small 0.1 μF output capacitor
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}mA
- TO-92 package

Typical Applications

Fixed Output Regulator

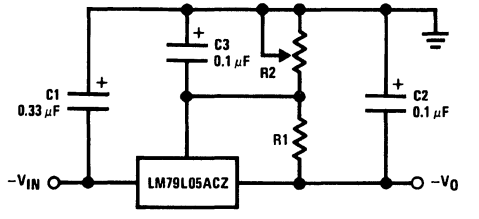


TL/H/7748–1

*Required if the regulator is located far from the power supply filter. A 1 μF aluminum electrolytic may be substituted.

**Required for stability. A 1 μF aluminum electrolytic may be substituted.

Adjustable Output Regulator



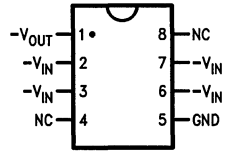
TL/H/7748–3

$-V_O = -5V - (5V/R1 + I_Q) \bullet R2$,

$5V/R1 > 3\,I_Q$

Connection Diagrams

SO-8 Plastic (Narrow Body)

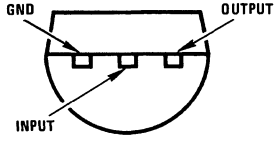


TL/H/7748–4

Top View

Order Number LM79L05ACM, LM79L12ACM or LM79L15ACM
See NS Package Number M08A

TO-92 Plastic Package (Z)



TL/H/7748–2

Bottom View

Order Number LM79L05ACZ, LM79L12ACZ or LM79L15ACZ
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage
V_O = −5V, −12V, −15V −35V
Internal Power Dissipation (Note 1) Internally Limited

Operating Temperature Range 0°C to +70°C
Maximum Junction Temperature +125°C
Storage Temperature Range −55°C to +150°C
Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics (Note 2) T_A = 0°C to +70°C unless otherwise noted.

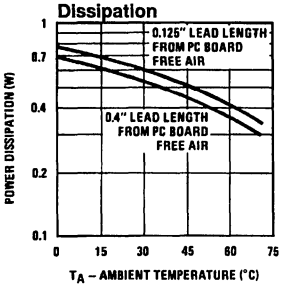
Output Voltage			−5V			−12V			−15V			Units
Input Voltage (unless otherwise noted)			−10V			−17V			−20V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, I_O = 100 mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	
		1 mA ≤ I_O ≤ 100 mA $V_{MIN} \le V_{IN} \le V_{MAX}$	−5.25 (−20 ≤ V_{IN} ≤ −7.5)		−4.75	−12.6 (−27 ≤ V_{IN} ≤ −14.8)		−11.4	−15.75 (−30 ≤ V_{IN} ≤ −18)		−14.25	V
		1 mA ≤ I_O ≤ 40 mA $V_{MIN} \le V_{IN} \le V_{MAX}$	−5.25 (−20 ≤ V_{IN} ≤ −7)		−4.75	−12.6 (−27 ≤ V_{IN} ≤ −14.5)		−11.4	−15.75 (−30 ≤ V_{IN} ≤ −17.5)		−14.25	
ΔV_O	Line Regulation	Tj = 25°C, I_O = 100 mA			60			45			45	mV
		$V_{MIN} \le V_{IN} \le V_{MAX}$	(−20 ≤ V_{IN} ≤ −7.3)			(−27 ≤ V_{IN} ≤ −14.6)			(−30 ≤ V_{IN} ≤ −17.7)			V
		Tj = 25°C, I_O = 40 mA			60			45			45	mV
		$V_{MIN} \le V_{IN} \le V_{MAX}$	(−20 ≤ V_{IN} ≤ −7)			(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)			V
ΔV_O	Load Regulation	Tj = 25°C 1 mA ≤ I_O ≤ 100 mA			50			100			125	mV
ΔV_O	Long Term Stability	I_O = 100 mA		20			48			60		mV/khrs
I_Q	Quiescent Current	I_O = 100 mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1 mA ≤ I_O ≤ 100 mA			0.3			0.3			0.3	mA
		1 mA ≤ I_O ≤ 40 mA			0.1			0.1			0.1	
		I_O = 100 mA			0.25			0.25			0.25	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$	(−20 ≤ V_{IN} ≤ −7.5)			(−27 ≤ V_{IN} ≤ −14.8)			(−30 ≤ V_{IN} ≤ −18)			V
V_n	Output Noise Voltage	Tj = 25°C, I_O = 100 mA f = 10 Hz − 10 kHz		40			96			120		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	Tj = 25°C, I_O = 100 mA f = 120 Hz	50			52			50			dB
	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O = 100 mA			−7.3			−14.6			−17.7	V
		I_O = 40 mA			−7.0			−14.5			−17.5	V

Note 1: Thermal resistance of Z package is 60°C/W θ_{jc}, 232°C/W θ_{ja} at still air, and 88°C/W at 400 ft/min of air. The M package θ_{ja} is 180°C/W in still air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

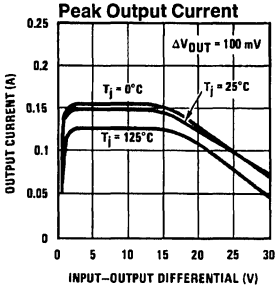
Note 2: To ensure constant junction temperature, low duty cycle pulse testing is used.

Typical Performance Characteristics

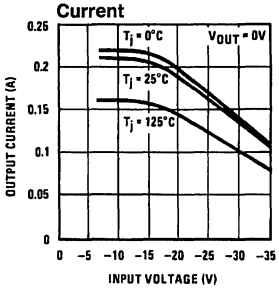
Maximum Average Power Dissipation



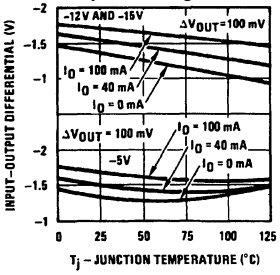
Peak Output Current



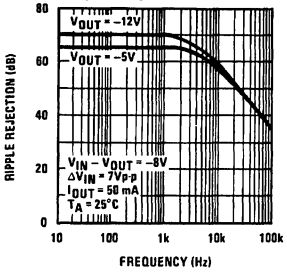
Short Circuit Output Current



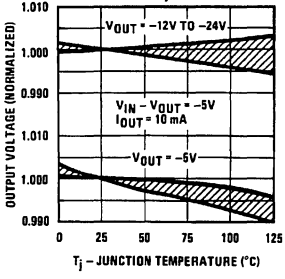
Dropout Voltage



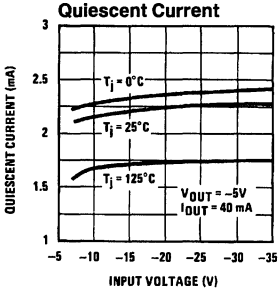
Ripple Rejection



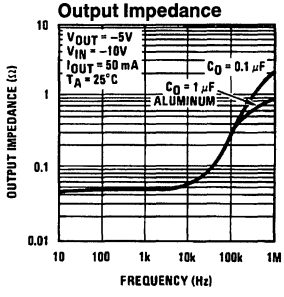
Output Voltage vs. Temperature (Normalized to 1V @ 25°C)



Quiescent Current



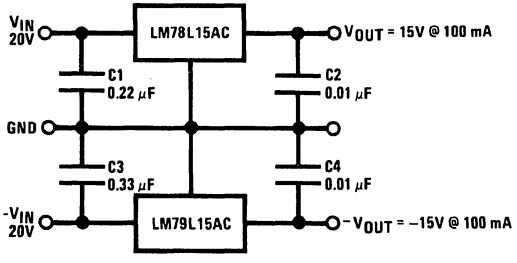
Output Impedance



TL/H/7748–5

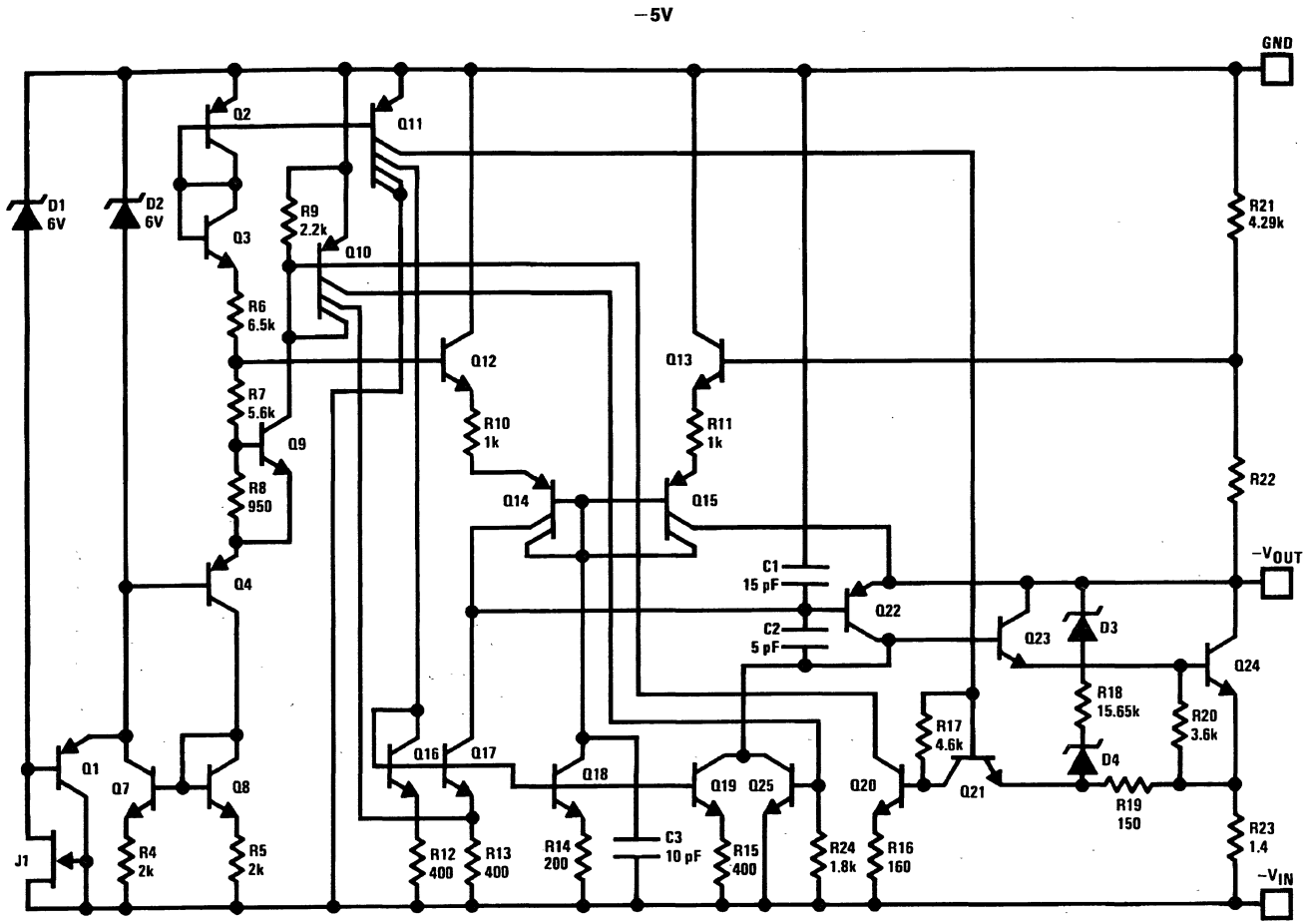
Typical Applications (Continued)

± 15V, 100 mA Dual Power Supply



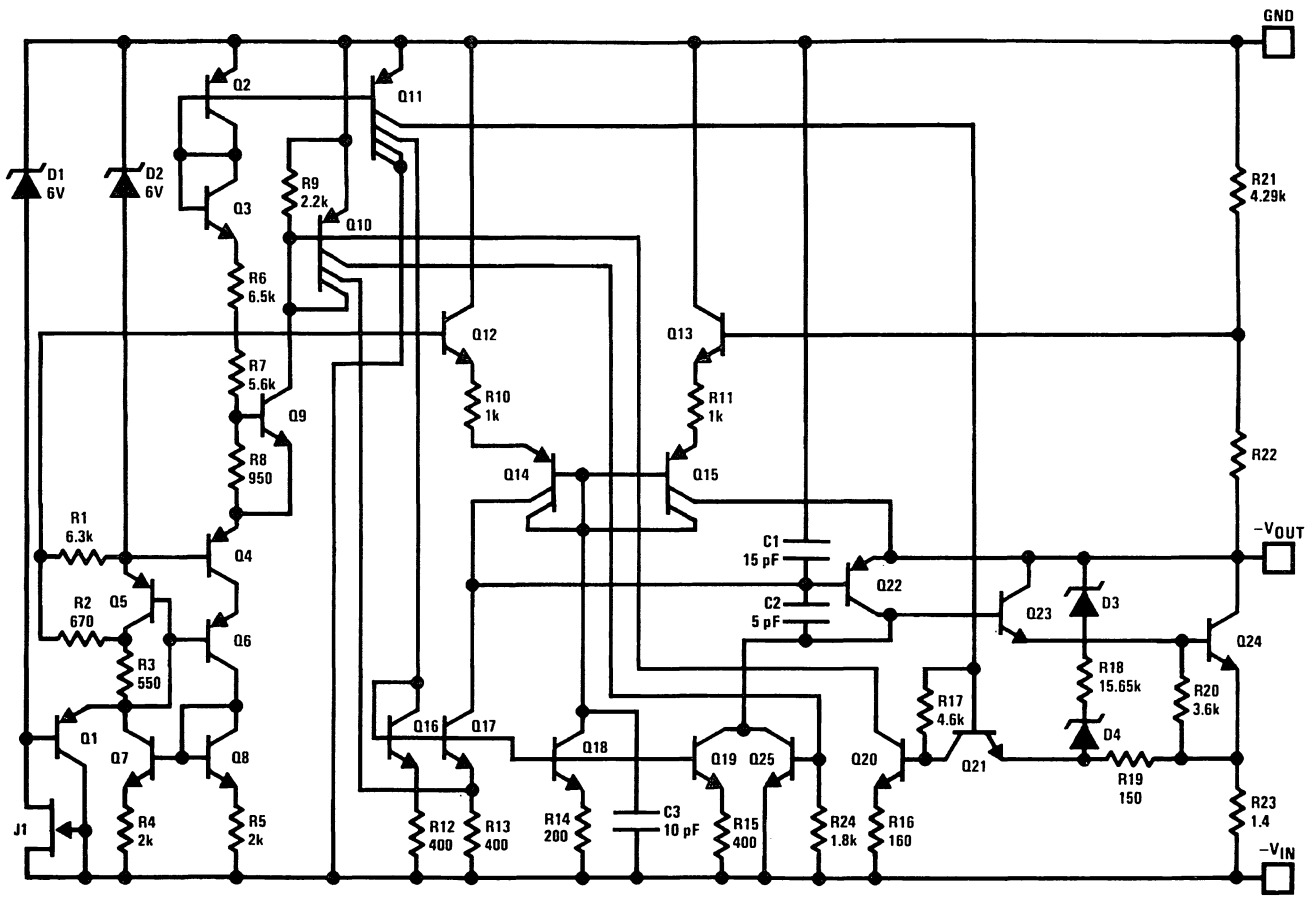
TL/H/7748–6

Schematic Diagrams



TL/H/7748–7

−12V and −15V



TL/H/7748–8

National Semiconductor

LM79MXX Series
3-Terminal Negative Regulators

General Description

The LM79MXX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79MXX series is packaged in the TO-202 power package and TO-39 metal can and is capable of supplying 0.5A of output current.

These regulators employ internal current limiting, safe area protection, and thermal shotdown for protection against virtually all overload conditions.

Low ground pin current of the LM79MXX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

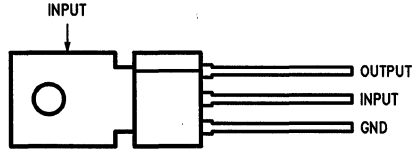
For output voltage other than −5V, −12V, and −15V the LM137 series provides an output voltage range from 1.2V to 57V.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 0.5A output current
- 4% preset output voltage

Connection Diagram

TO-202 (P) Plastic Package



TL/H/10483–5

Front View

Order Number LM79M05CP, LM79M12CP or LM79M15CP
See NS Package Number P03A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
V_O = 5V	−25V
V_O = 12V and 15V	−35V
Input/Output Differential	
V_O = 5V	25V
V_O = 12V and 15V	30V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	230°C
ESD Susceptability	TBD

Electrical Characteristics

Conditions unless otherwise noted: I_{OUT} = 350 mA, C_{IN} = 2.2 μF, C_{OUT} = 1 μF, 0°C ≤ T_J ≤ +125°C

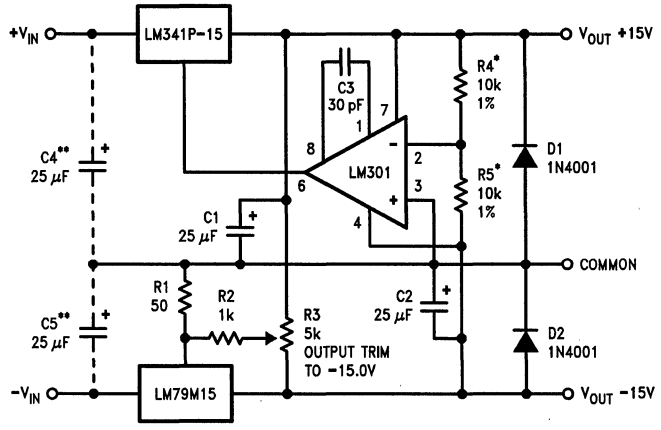
Part Number			LM79M05C			LM79M12C			LM79M15C			Units
Output Voltage			−5V			−12V			−15V			
Input Voltage (Unless Otherwise Specified)			−10V			−19V			−23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C	−4.8	−5.0	−5.2	−11.5	−12.0	−12.5	−14.4	−15.0	−15.6	V
		5 mA ≤ I_{OUT} ≤ 350 mA	−4.75 (−25 ≤ V_{IN} ≤ −7)		−5.25	−11.4 (−27 ≤ V_{IN} ≤ −14.5)		−12.6	−14.25 (−30 ≤ V_{IN} ≤ −17.5)		−15.75	V
ΔV_O	Line Regulation	T_J = 25°C (Note 2)		8 (−25 ≤ V_{IN} ≤ −7)	50		5 (−30 ≤ V_{IN} ≤ −14.5)	80		5 (−30 ≤ V_{IN} ≤ −17.5)	80	mV
				2 (−18 ≤ V_{IN} ≤ −8)	30		3 (−25 ≤ V_{IN} ≤ −15)	30		3 (−28 ≤ V_{IN} ≤ −18)	50	mV
ΔV_O	Load Regulation	T_J = 25°C, (Note 2) 5 mA ≤ I_{OUT} ≤ 0.5A		30	100		30	240		30	240	mV
I_Q	Quiescent Current	T_J = 25°C		1	2		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Input Voltage			0.4 (−25 ≤ V_{IN} ≤ −8)			0.4 (−30 ≤ V_{IN} ≤ −14.5)			0.4 (−30 ≤ V_{IN} ≤ −27)	mA
		With Load, 5 mA ≤ I_{OUT} ≤ 350 mA			0.4			0.4			0.4	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		750			400			400		μV
	Ripple Rejection	f = 120 Hz	54 (−18 ≤ V_{IN} ≤ −8)	66		54 (−25 ≤ V_{IN} ≤ −15)	70		54 (−30 ≤ V_{IN} ≤ −17.5)	70		dB
	Dropout Voltage	T_J = 25°C, I_{OUT} = 0.5A		1.1			1.1			1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		800			800			800		mA
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 100°C		−0.4			−0.8			−1.0		mV/°C
	Thermal Resistance Junction to Case	P Package		12			12			12		°C/W
	Thermal Resistance Junction to Ambient	P Package		70			70			70		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Typical Applications

±15V, 1 Amp Tracking Regulators



TL/H/10483–1

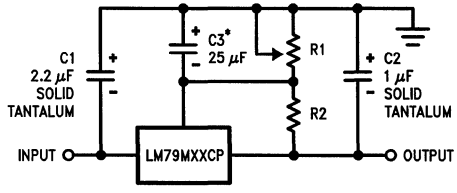
Performance (Typical)

	(−15)	(+15)
Load Regulation at 0.5A	40 mV	2 mV
Output Ripple, C_{IN} = 3000 μF, I_L = 0.5A	100 μVrms	100 μVrms
Temperature Stability	50 mV	50 mV
Output Noise 10 Hz ≤ f ≤ 10 kHz	150 μVrms	150 μVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs

**Necessary only if raw supply filter capacitors are more than 3″ from regulators

Variable Output



TL/H/10483–3

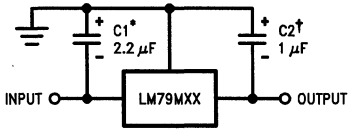
*Improves transient response and ripple rejection. Do not increase beyond 50 μF.

$$V_{OUT} = V_{SET}\left(\frac{R1 + R2}{R2}\right)$$

Select R2 as follows:

LM79M05C	300Ω
LM79M12C	750Ω
LM79M15C	1k

Fixed Regulator



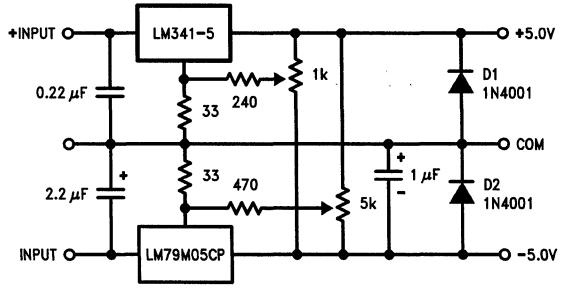
TL/H/10483–2

*Required if regulator is separated from filter capacitor by more than 3″. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100 μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



TL/H/10483–4

National Semiconductor

LP2950/LP2950AC/LP2950C 5V and LP2951/LP2951AC/LP2951C Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 μA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950 in the popular 3-pin TO-92 package is pin-compatible with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Features

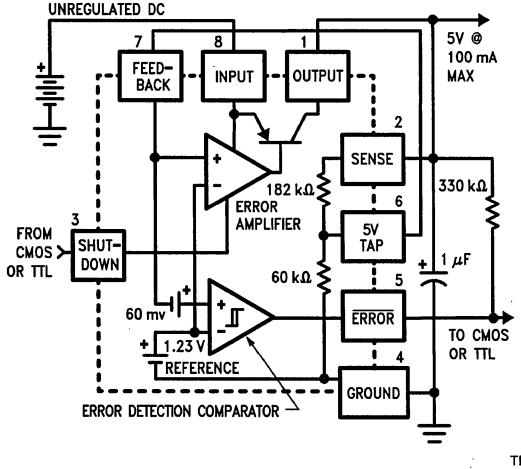
- High accuracy 5V, guaranteed 100 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs only 1 μF for stability
- Current and Thermal Limiting

LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block and Connection Diagrams

(LP2951 Pinout for H, J, M and N Packages)

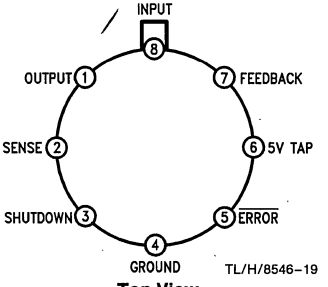


TL/H/8546–1

Order Number LP2951J, LP2951ACJ, LP2951CJ, LP2951ACN or LP2951CN
See NS Package Number J08A or N08E

Order Number LP2951ACM or LP2951CM for SO-8
See NS Package Number M08A

Metal Can Package (H)

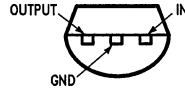


TL/H/8546–19

Top View

Order Number LP2951H
See NS Package Number H08C

TO-92 Plastic Package (Z)



TL/H/8546–2

Bottom View
Order Number LP2950ACZ-5.0 or LP2950CZ-5.0
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	−65° to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951	−55° to +150°C
LP2950AC/LP2950C, LP2951AC/LP2951C	−40° to +125°C
Input Supply Voltage	−0.3 to +30V
Feedback Input Voltage (Notes 9 and 10)	−1.5 to +30V
Shutdown Input Voltage (Note 9)	−0.3 to +30V
Error Comparator Output Voltage (Note 9)	−0.3 to +30V

ESD Rating is to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	LP2951		LP2950AC LP2951AC			LP2950C LP2951C			Units
		Typ	Tested Limit (Note 3)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Output Voltage	T_J = 25°C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	−25°C ≤ T_J ≤ 85°C					5.05 4.95			5.075 4.925	V max V min
	Full Operating Temperature Range		**5.06** **4.94**			**5.06** **4.94**			**5.1** **4.9**	V max V min
Output Voltage	100 μA ≤ I_L ≤ 100 mA T_J ≤ $T_{J_{MAX}}$		**5.075** **4.925**			**5.07** **4.93**			**5.12** **4.88**	V max V min
Output Voltage Temperature Coefficient	(Note 12)	**20**	**120**	**20**		**100**	**50**		**150**	ppm/°C
Line Regulation (Note 14)	6V ≤ V_{in} ≤ 30V (Note 15)	0.03	0.1 **0.5**	0.03	0.1	 **0.2**	0.04	0.2	 **0.4**	% max % max
Load Regulation (Note 14)	100 μA ≤ I_L ≤ 100 mA	0.04	0.1 **0.3**	0.04	0.1	 **0.2**	0.1	0.2	 **0.3**	% max % max
Dropout Voltage (Note 5)	I_L = 100 μA	50	80 **150**	50	80	 **150**	50	80	 **150**	mV max mV max
	I_L = 100 mA	380	450 **600**	380	450	 **600**	380	450	 **600**	mV max mV max
Ground Current	I_L = 100 μA	75	120 **140**	75	120	 **140**	75	120	 **140**	μA max μA max
	I_L = 100 mA	8	12 **14**	8	12	 **14**	8	12	 **14**	mA max mA max
Dropout Ground Current	V_{in} = 4.5V I_L = 100 μA	110	170 **200**	110	170	 **200**	110	170	 **200**	μA max μA max
Current Limit	V_{out} = 0	160	200 **220**	160	200	 **220**	160	200	 **220**	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 KHz	C_L = 1 μF	430		430			430			μV rms
	C_L = 200 μF	160		160			160			μV rms
	C_L = 3.3 μF (Bypass = 0.01 μF Pins 7 to 1 (LP2951))	100		100			100			μV rms
8-Pin Versions only		**LP2951**		**LP2951AC**			**LP2951C**			
Reference Voltage		1.235	1.25 **1.26** 1.22 **1.2**	1.235	1.25 1.22	 **1.26** **1.2**	1.235	1.26 1.21	 **1.27** **1.2**	V max V max V min V min
Reference Voltage	(Note 7)		**1.27** **1.19**			**1.27** **1.19**			**1.285** **1.185**	V max V min

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951		LP2951AC			LP2951C			Units
		Typ	Tested Limit (Note 3)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
8-Pin Versions only (Continued)										
Feedback Pin Bias Current		20	40 **60**	20	40	 **60**	20	40	 **60**	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1 **2**	0.01	1	 **2**	0.01	1	 **2**	µA max µA max
Output Low Voltage	V_{in} = 4.5V I_{OL} = 400 µA	150	250 **400**	150	250	 **400**	150	250	 **400**	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 **25**	60	40	 **25**	60	40	 **25**	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 **140**	75	95	 **140**	75	95	 **140**	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	 Low (Regulator ON) High (Regulator OFF)	1.3	 **0.6** **2.0**	1.3		 **0.7** **2.0**	1.3		 **0.7** **2.0**	V V max V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50 **100**	30	50	 **100**	30	50	 **100**	µA max µA max
	$V_{shutdown}$ = 30V	450	600 **750**	450	600	 **750**	450	600	 **750**	µA max µA max
Regulator Output Current in Shutdown	(Note 11)	3	10 **20**	3	10	 **20**	3	10	 **20**	µA max µA max

Note 1: Boldface limits apply at temperature extremes.

Note 2: Unless otherwise specified all limits guaranteed for T_J = 25°C, V_{in} = 6V, I_L = 100 µA and C_L = 1 µF. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense (V_{out} = 5V) and $V_{shutdown} \leq 0.8V$.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V **(2.3V over temperature)** must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV × 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: $V_{ref} \leq V_{out} \leq (V_{in} - 1V)$, $2.3V \leq V_{in} \leq 30V$, 100 µA $\leq I_L \leq$ 100 mA, $T_J \leq T_{JMAX}$.

Note 8: The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistance of the 8-pin DIP packages is 105°C/W for the molded plastic (N) and 130°C/W for the cerdip (J) junction to ambient when soldered directly to a PC board. Thermal resistance for the metal can (H) is 160°C/W junction to ambient and 20°C/W junction to case. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown} \geq 2V$, $V_{in} \leq 30V$, V_{out} = 0, Feedback pin tied to 5V Tap.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

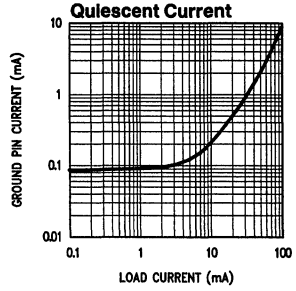
Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10 ms.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

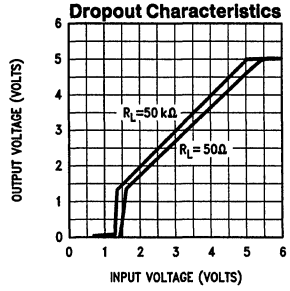
Note 15: Line regulation for the LP2951 is tested at 150°C for I_L = 1 mA. For I_L = 100 µA and T_J = 125°C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Typical Performance Characteristics

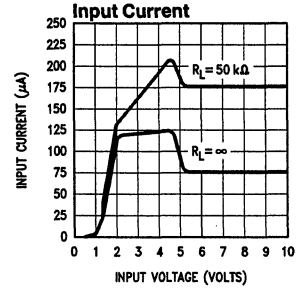
Quiescent Current



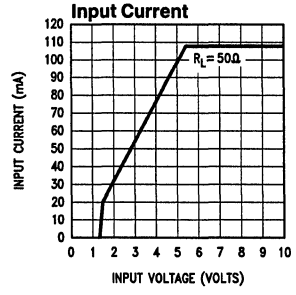
Dropout Characteristics



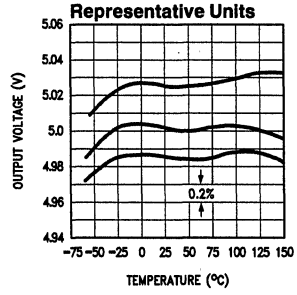
Input Current



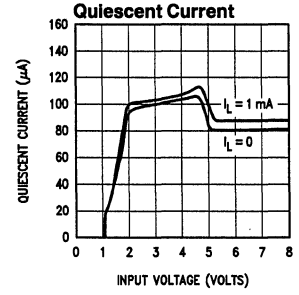
Input Current



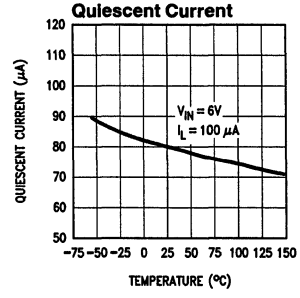
Output Voltage vs. Temperature of 3 Representative Units



Quiescent Current



Quiescent Current



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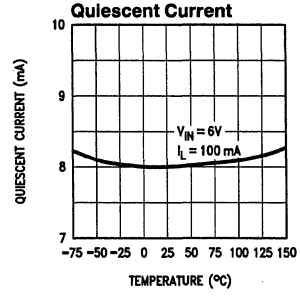
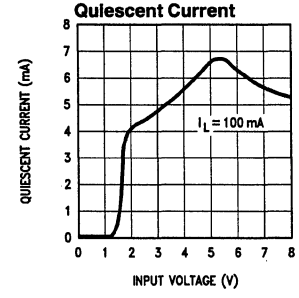
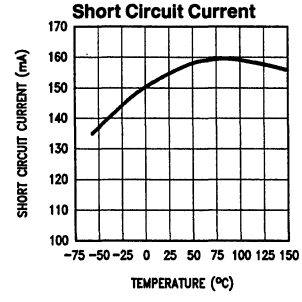


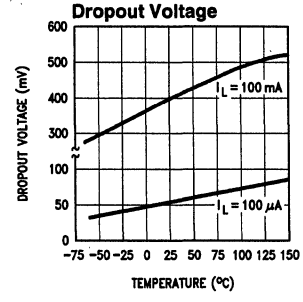
Quiescent Current



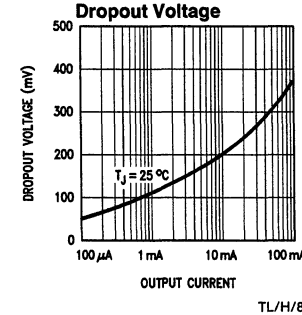
Short Circuit Current



Dropout Voltage



Dropout Voltage



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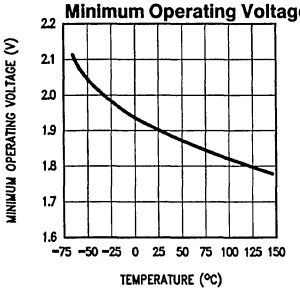
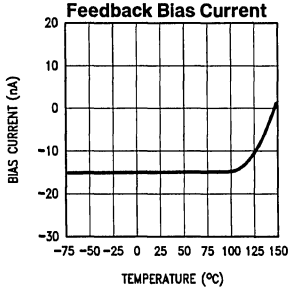
Typical Performance Characteristics (Continued)

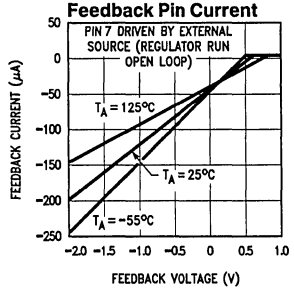
LP2951
Minimum Operating Voltage



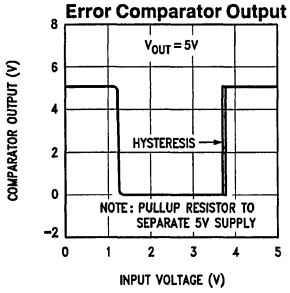
LP2951
Feedback Bias Current



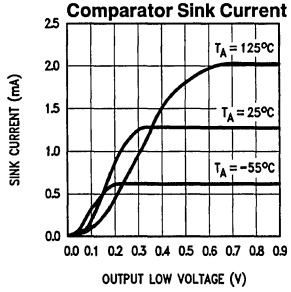
LP2951
Feedback Pin Current



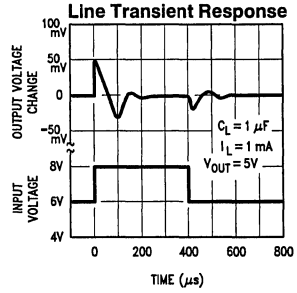
LP2951
Error Comparator Output



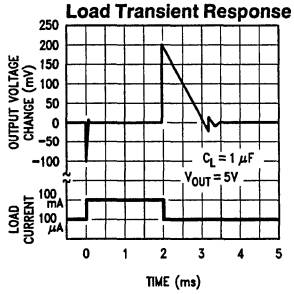
LP2951
Comparator Sink Current



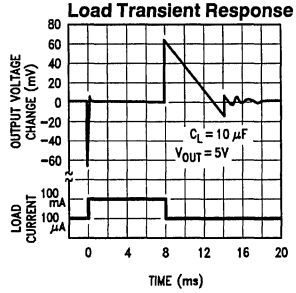
Line Transient Response



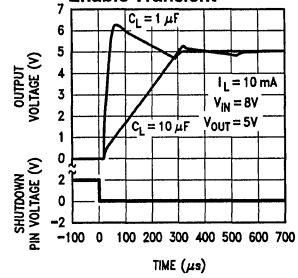
Load Transient Response



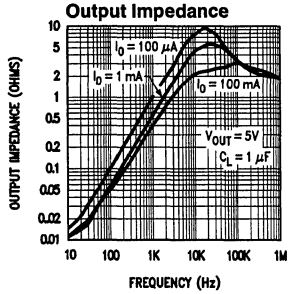
Load Transient Response



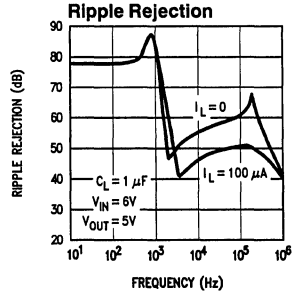
LP2951
Enable Transient



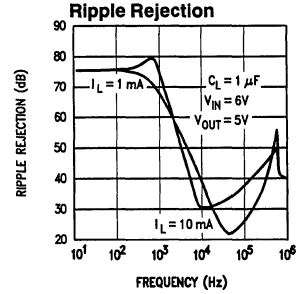
Output Impedance



Ripple Rejection



Ripple Rejection



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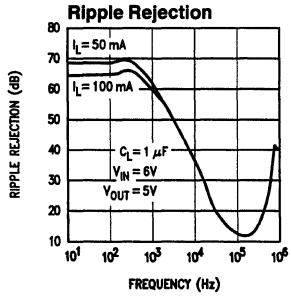
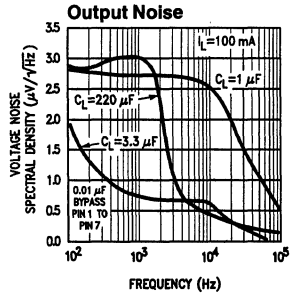
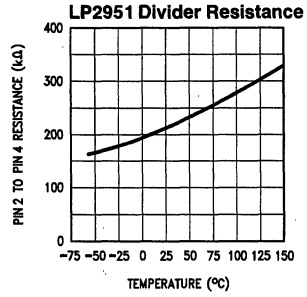
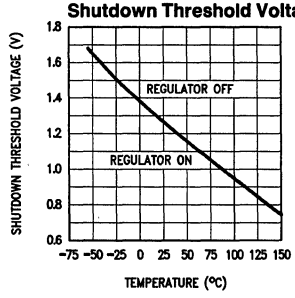
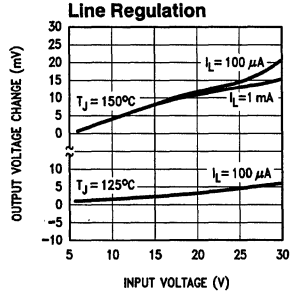
Typical Performance Characteristics (Continued)

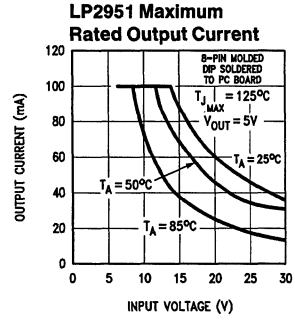


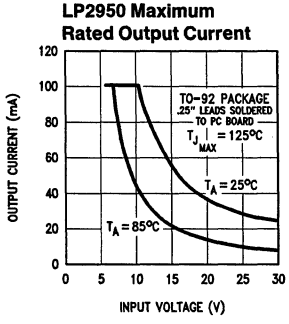


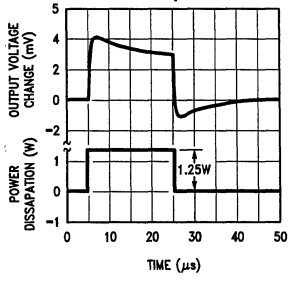












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Application Hints

EXTERNAL CAPACITORS

A 1.0 µf (or greater) capacitor is required between the LP2950/LP2951 output and ground for stability. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about −30°C, so solid tantalums are recommended for operation below −25°C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 µf for currents below 10 mA or 0.1 µf for currents below 1 mA. Using the 8-Pin versions at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 µf (or greater) capacitor should be used.

Unlike many other regulators, the L2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 version with external resistors, a minimum load of 1 µA is recommended.

A 0.1 µf capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem

Application Hints (Continued)

when using high value external resistors to set the output voltage. Adding a 100 pf capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μf will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

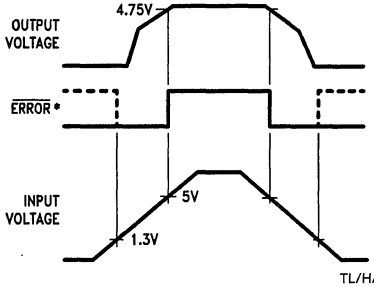
The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the LP2951's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the 5V output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 μA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 MΩ. The resistor is not required if this output is unused.

PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in *Figure 2,* an external pair of resistors is required.



TL/H/8546–20

*In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5V supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT} (see *Figure 2*).

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1 μA forces an upper limit of 1.2 MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 μA. Since the LP2951 typically draws 60 μA at no load with Pin 2 open-circuited, this is a small price to pay.

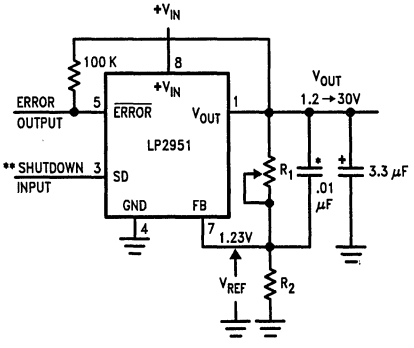
REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 μV to 160 μV rms for a 100 kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 μF. When doing this, the output capacitor must be increased to 3.3 μF to maintain stability. These changes reduce the output noise from 430 μV to 100 μV rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



TL/H/8546–7

FIGURE 2. Adjustable Regulator

*See Application Hints

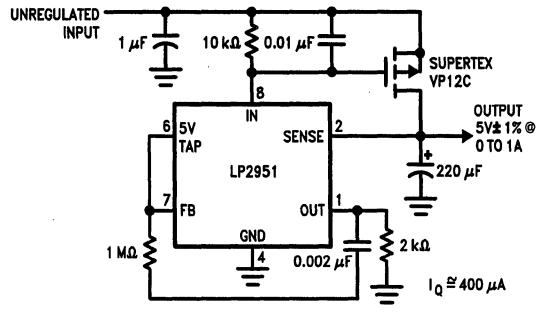
$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

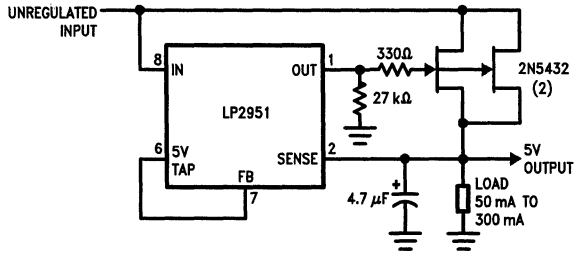
Typical Applications

1A Regulator with 1.2V Dropout



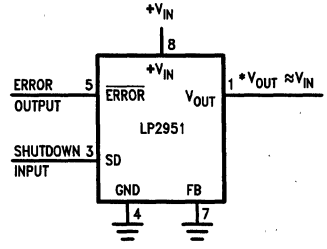
TL/H/8546–22

300 mA Regulator with 0.75V Dropout



TL/H/8546–21

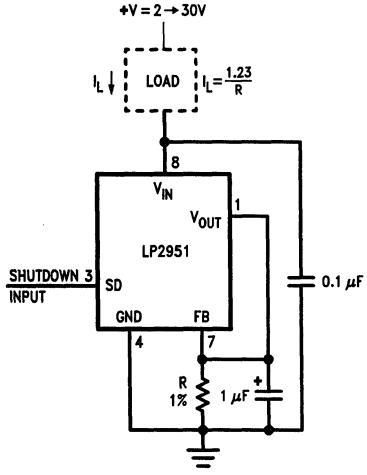
Wide Input Voltage Range Current Limiter



TL/H/8546–9

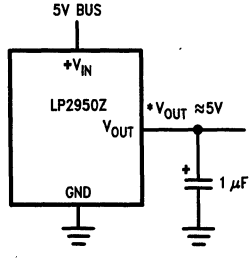
*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Low Drift Current Source



TL/H/8546–8

5 Volt Current Limiter

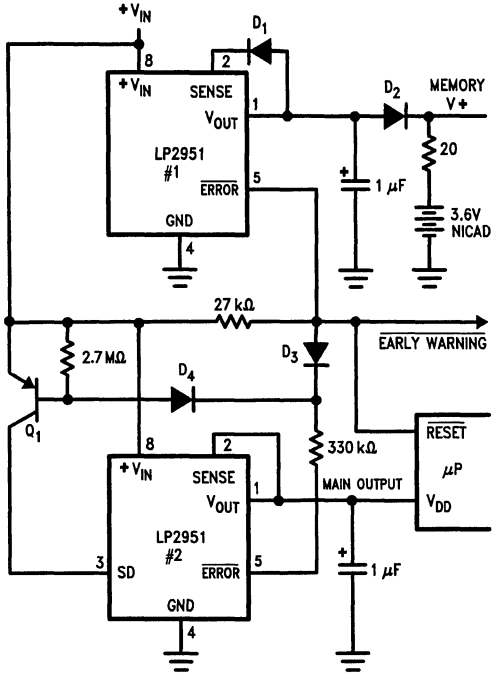


TL/H/8546–10

*Minimum input-output voltage ranges from 40 mV to 400 mV, depending on load current. Current limit is typically 160 mA.

Typical Applications (Continued)

Regulator with Early Warning and Auxiliary Output

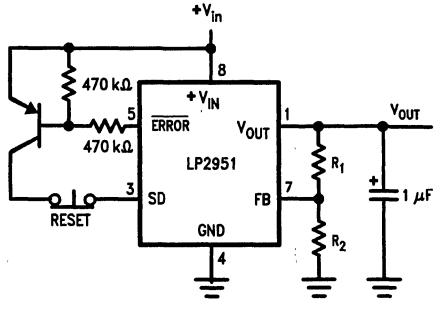


TL/H/8546–11

- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output

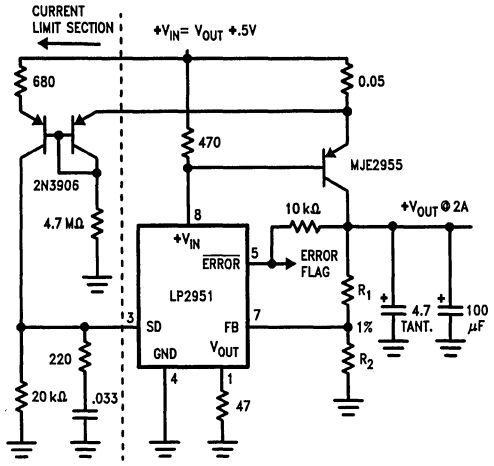
Operation: Reg. #1's V_{out} is programmed one diode drop above 5V. Its error flag becomes active when $V_{in} \leq 5.7V$. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Latch Off When Error Flag Occurs



TL/H/8546–12

2 Ampere Low Dropout Regulator

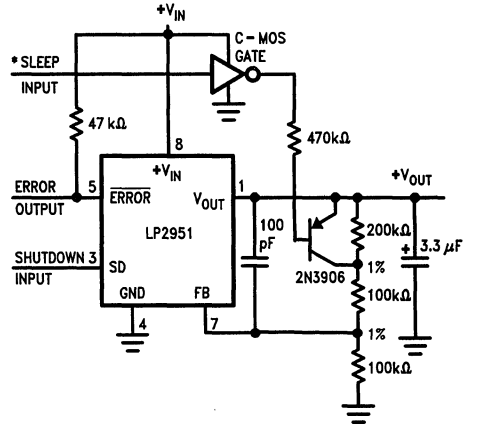


$$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$$

TL/H/8546–13

For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 2 to $+V_{out}$ Buss.

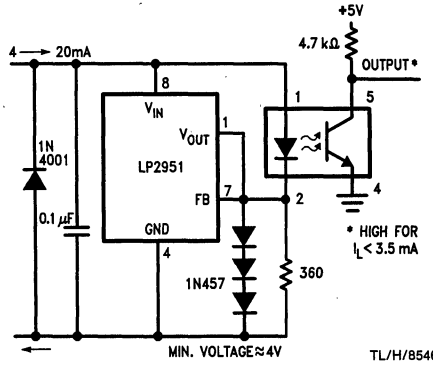
5V Regulator with 2.5V Sleep Function



*High input lowers V_{out} to 2.5V

TL/H/8546–14

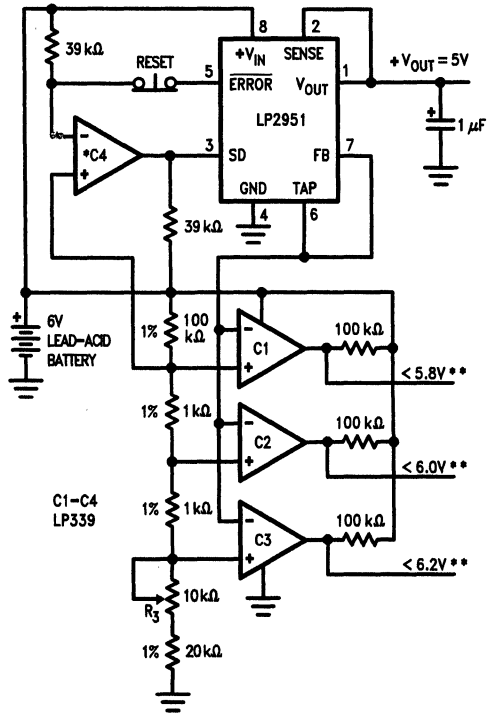
Open Circuit Detector for 4 → 20 mA Current Loop



TL/H/8546–15

Typical Applications (Continued)

Regulator with State-of-Charge Indicator



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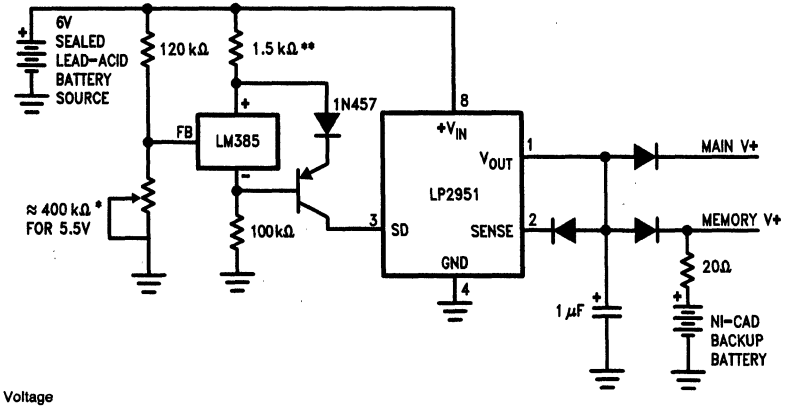
*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

Low Battery Disconnect

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ≈ 150 µA.



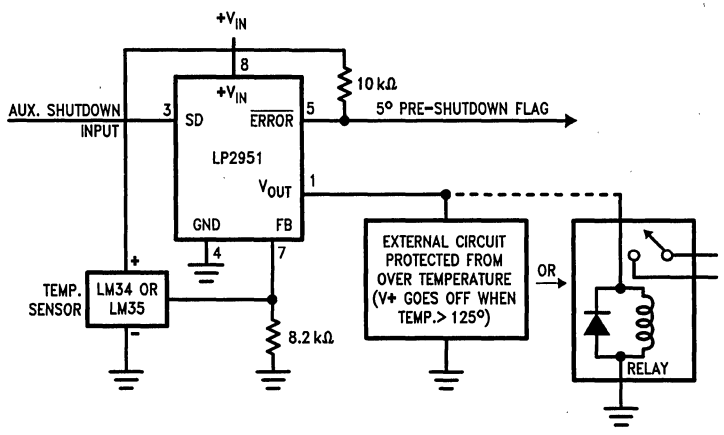
TL/H/8546–17

*Sets disconnect Voltage

**Sets disconnect Hysteresis

Typical Applications (Continued)

System Overtemperature Protection Circuit



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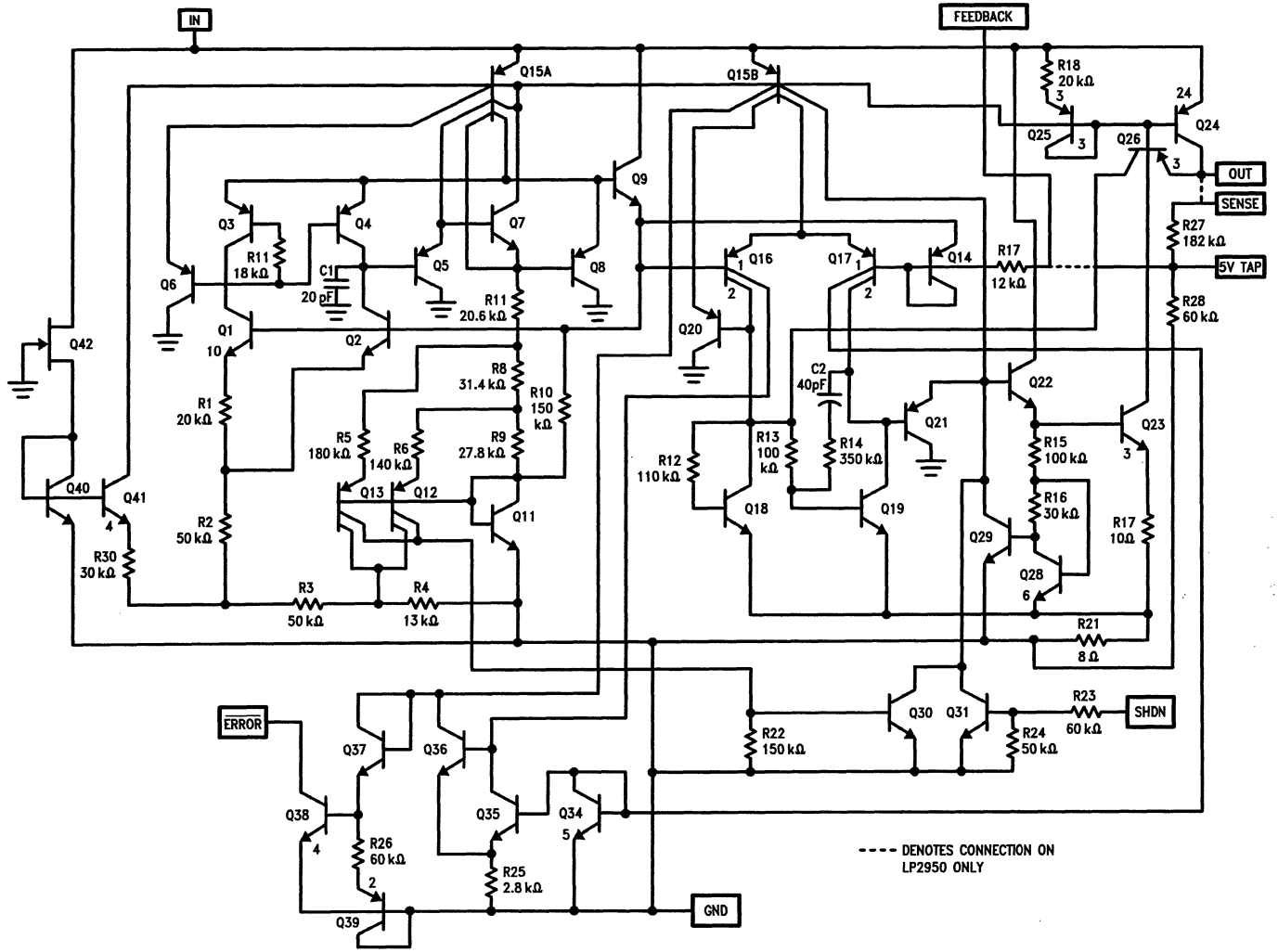
LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

Schematic Diagram



TL/H/8546–23

Section 2

Switching Voltage Regulators

Section 2 Contents

National Semiconductor

Switching Voltage Regulators Selection Guide

Switching Voltage Regulators

Amps	Device	Operation Modes	V_{IN} Range	Package
7.0	†HS7107CK	Step-Down, Invert, Flyback	10V–100V	TO-3
	†HS7067CK	Step-Down, Invert, Flyback	10V–60V	TO-3
5.0	LH1605CK	Step-Down		TO-3
3.0	LM2579	Step-Up, Step-Down, Invert	2V–50V	TO-220
1.5	†LM78S40CN	Step-Up, Step-Down, Invert	2.5V–40V	16-Pin DIP
1.0	LM1575-5.0	Step-Down	8V–40V	TO-220
0.75	†LM1578H LM2578H, N LM3578N, H, M	Step-Up, Step-Down, Invert, Flyback	2V–40V	TO-39, 8-Pin DIP SO-8
0.05	LMC7660IN	Invert	1.5V–10V	8-Pin DIP

Switching Controllers

Device	Title	Package
LM1524/2524/3524	Switching Regulator	16-Pin Plastic DIP, SO-16 16-Pin Ceramic DIP
LM1525A/3525A	Switching Regulator	16-Pin Plastic DIP 16-Pin Ceramic DIP
LM1527A/3527A	Switching Regulator	16-Pin Plastic DIP 16-Pin Ceramic DIP
LM494	Pulse Width Modulated Control Circuit	16-Pin Plastic and Ceramic DIP

†Military qualified device. For more information, consult the Military/Aerospace Selection Guide.

National Semiconductor

PRELIMINARY

HS7067/HS7107 7 Amp, Multimode, High Efficiency Switching Regulator

General Description

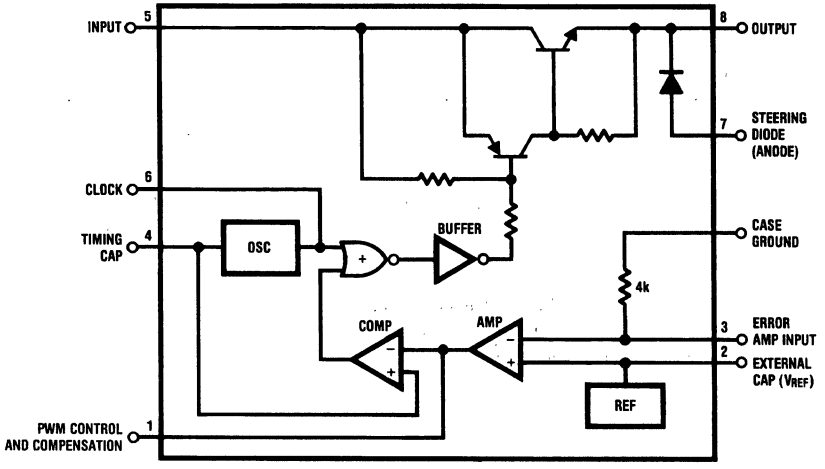
The HS7067/HS7107 is a hybrid high efficiency switching regulator with high output current capability. The device is housed in a standard TO-3 package containing a temperature compensated voltage reference, a pulse-width modulator with programmable oscillator frequency, error amplifier, high current, high voltage output switch and steering diode. The HS7067/HS7107 operates in a step-down, inverting, as well as in a transformer-coupled mode.

The HS7067/HS7107 can supply up to 7A of continuous output current over a wide range of input and output voltages.

Features

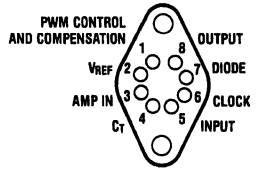
- HS7067—10V to 60V input
- HS7107—10V to 100V input
- 7A continuous output current
- Step-down, inverting, and transformer-coupled operation
- Frequency adjustable to 200 kHz
- High-efficiency (>75%)
- Standard 8-pin TO-3 package

Block and Connection Diagrams



TL/K/6746–1

Metal Can Package



TL/K/6746–2

Top View

Case is ground

Order Number HS7067CK, HS7067K, HS7107CK or HS7107K
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{IN}, Input Voltage
- HS7067: 65V
- HS7107: 105V

I_{OUT}, Output Current: 8A

T_J, Operating Temperature: 150°C

P_D, Internal Power Dissipation: 25W

T_A, Operating Temperature Range
- HS7067C/7107C: −25°C to +85°C
- HS7067/7107: −55°C to +125°C

T_{STG}, Storage Temperature Range: −65°C to +150°C

$V_R(V_{8-7})$, Steering Diode Reverse Voltage: 105V

$I_D(I_{7-8})$, Steering Diode Forward Current: 8A

Electrical Characteristics $T_C = 25°C$, $V_{IN} = 20V$ (unless otherwise specified)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
$V_{IN}-V_{OUT}$	Min V_{IN}/V_{OUT} Differential	HS7067	$10V \le V_{IN} \le V_{IN(MAX)}$, $I_{OUT} = 2A$ (Note 6)			3.0		V
		HS7107				3.0		V
V_S	Switch Saturation Voltage		$I_C = 7.0A$, $V_{IN} = 10V$	HS7107		1.6	TBD	V
				HS7607			1.9	V
			$I_C = 2.0A$, $V_{IN} = 10V$			1.0		V
V_F	Steering Diode On Voltage		$I_D = 7.0A$	HS7107		1.3	TBD	V
				HS7607		1.7	TBD	
			$I_D = 2.0A$			0.9		V
V_{IN}	Supply Voltage Range (Note 7)	HS7067	$T_{MIN} \le T_A \le T_{MAX}$		10		60	V
		HS7107	$T_{MIN} \le T_A \le T_{MAX}$		10		100	V
I_R	Steering Diode Reverse Current		$V_R = 100V$				60	μA
I_Q	Quiescent Current (Note 3)		0% Duty Cycle ($V_3 = 3.0V$)			6		mA
			100% Duty Cycle ($V_3 = 0V$)			26		mA
V_2	Reference Voltage on Pin 2		$T_{MIN} \le T_A \le T_{MAX}$		2.3	2.5	2.7	V
$V_{CLK\,H}$	Clock Output High		$I_{CLK} = -750\ \mu A$		1.2	1.6		V
$V_{CLK\,L}$	Clock Output Low		$I_{CLK} = 80\ \mu A$				0.9	V
ΔV_2	Line Regulation of Reference Voltage on Pin 2		$V_{MIN} \le V_{IN} \le V_{MAX}$			5		mV
R_A	Resistance on Pin 3 to Ground		(Note 4)			4.0		kΩ
V_{OUT}	Feedback Resistor R_f Tol. ±1%			HS7107		4	TBD	%
				HS7067			9	
V_4	Voltage Swing—Pin 4					3.0		V
I_4	Charging Current—Pin 4					330		μA
I_{CLK}	Clock Input Current — Pin 6		$V_{CLK} = 3.5V$			1.75	4	mA
t_r	Transistor Current Rise Time		$I_O = 2.0A$ (Note 6)			70		ns
			$I_O = 7.0A$ (Note 6)			120		ns
t_f	Transistor Current Fall Time		$I_O = 2.0A$ (Note 6)			100		ns
			$I_O = 7.0A$ (Note 6)			160		ns
t_s	Diode Storage Time		$I_O = 7.0A$ (Note 6)			120		ns
t_d	Delay Time		$I_O = 7.0A$ (Note 6)			600		ns
f_{MAX}	Max Clock Frequency		(Note 5)				200	kHz

Electrical Characteristics $T_C = 25°C$, $V_{IN} = 20V$ (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$Z_{PIN\,1}$	Impedance at Pin 1	(Note 6)			5		MΩ
η	Efficiency	V_{OUT} = 5V, I_{OUT} = 1A	f_O = 25 kHz (Note 6)		80		%
			f_O = 200 kHz (Note 5)		70		%
θ_{JC}	Thermal Resistance	(Note 1)			4.0		°C/W

Note 1: θ_{JA} is typically 35°C/W for natural convection cooling.

Note 2: V_{OUT} and I_{OUT} refer to the output DC voltage and output current of a switching supply after the output LC filter as shown in *Figure 1.*

Note 3: Quiescent current depends on the duty cycle of the switching translator.

Note 4: This test includes the input bias current of the error amplifier.

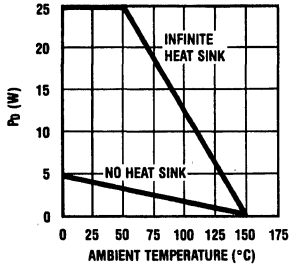
Note 5: Circuit configured as shown in *Figure 1.*

Note 6: These parameters are not tested. They are given for informational purposes only.

Note 7: Functionally tested at limits only (pass-fail).

Typical Performance Characteristics

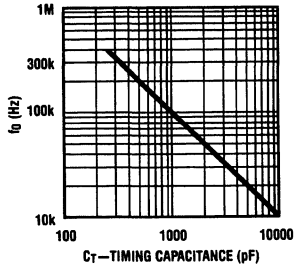
Power Derating Curve



θ_{JC} = 4°C/W

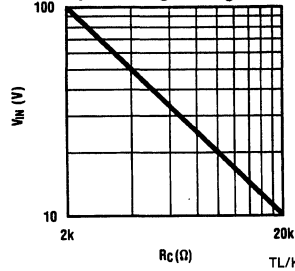
θ_{JA} = 35°C/W

Frequency vs Timing Capacitance



$$f_O = \frac{1}{10k \times C_T}$$

Typical Compensation Input Voltage vs R_C



TL/K/6746–3

$$R_C = \left[\frac{200k}{V_{IN(MAX)}}\right] \Omega$$

$$C_C = \frac{\sqrt{LC} \times \sqrt{10}}{R_C} F$$

Typical Applications

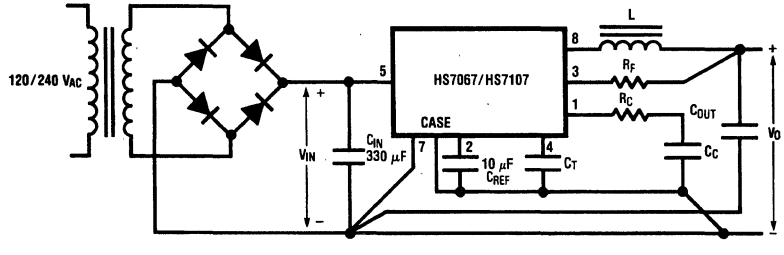
THE BUCK CONVERTER (Step Down)

The buck converter is the most common application in switching-power conversion. It allows to step down a voltage with a minimum of components and a maximum of efficiency (for further information on the theory of operation of a buck converter, see AN-343).

f_O	25 kHz	200 kHz
L	86 μH	21 μH
C_T	0.0039 μF	330 pF
C_C	0.2 μF	0.068 μF
R_f	4 kΩ	4 kΩ
R_C	5.7 kΩ	5.7 kΩ
C_{OUT}	1500 μF	680 μF

V_{IN} = 10V to 35V
V_{OUT} = 5V
I_{OUT} = 1A to 6A

Load Regulation = 40 mV
Line Regulation = 5 mV



TL/K/6746–4

Typical Applications (Continued)

Design equations:

Following are the design equations for a buck converter application using the HS 7107/7067:

$$C_T = \frac{1}{10^4 \times f_O}$$

$$L_{MIN} = \frac{(V_{IN(MAX)} - V_O)\, V_O}{V_{IN(MAX)} \times f_O \times \Delta I} \quad \text{(Note 7, 9)}$$

$$C_{MIN} = \frac{\Delta I}{4\, f_O\, (e_O - \Delta I \times ESR)} \quad \text{(Note 8, 9)}$$

$$C_C = \frac{\sqrt{10\,LC}}{R_C}$$

$$R_C = \frac{2 \times 10^5}{V_{IN(MAX)}}$$

$$R_f = 4k\left(\frac{V_O - 2.5}{2.5}\right)\Omega$$

Note 7: L_{MIN} is the minimum value of output filter inductance, L, for stable operation.

Note 8: C_{MIN} is the minimum value of output filter capacitance, C, necessary to achieve an output ripple voltage, e_O. ESR is the Effective Series Resistance of the output filter capacitor, C, at the operating frequency, f_O.

Note 9: ΔI = Peak to Peak Ripple current through the inductor and the capacitor. $\frac{\Delta I}{2} < I_{O\,MIN}$ and $\frac{\Delta I}{2} < 7 - I_{O\,MAX}$.

Efficiency Equations

Since high efficiency is the principal advantage of switched-mode power conversion, switching regulator losses are an important design concern. Losses and efficiency of a buck converter can be calculated with the following equations.

Note: Pin 7 is grounded; I_O = average output current at pin 8

Switching Period (T)

$$T = \frac{1}{f_O} = t_{ON} + t_{OFF}$$

Duty Cycle (D)

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_O + V_F}{V_{IN} - V_S + V_F}$$

Transistor DC Losses (P_T)

$$P_T = V_S \times I_O \times D$$

Transistor Switching Losses (P_S)

$$P_S = (V_{IN} + V_F) \times I_O \times \frac{(t_r + t_f + 2t_S)\, f_O}{2}$$

Capacitor Losses (P_C)

$$P_C = ESR \times \left(\frac{V_O\,(T - DT)}{4L}\right)^2$$

Diode DC Losses (P_D)

$$P_D = V_f \times I_O \times (1 - D)$$

Drive Circuit Losses (D_L)

$$D_L = 0.02 \times V_{IN} \times D$$

Inductor Losses (P_L)

$$P_L = I_O{}^2 \times R_L \text{ (DC winding resistance)}$$

Power Output (P_O)

$$P_O = \frac{((V_{IN} - V_S)\, t_{ON}) - ((V_F)\, t_{OFF})}{t_{ON} + t_{OFF}} \times I_O$$

Efficiency (η)

$$\eta = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_T + P_S + P_D + D_L + P_L + P_C}$$

TRANSFORMER COUPLED CONVERTERS

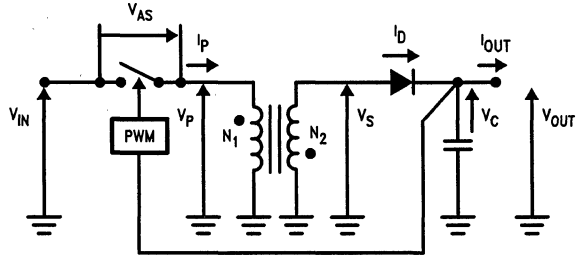
In addition to the implementation of a buck converter, the HS 7107/7067 can be used in various transformer coupled configurations. They can be used in various topologies such as: step-up, step-down, inverter, multiple outputs and isolated converters.

There are basically two different methods in implementing transformer coupled converters: the flyback and the foward topology

The Flyback Principle

Figure 1 shows a functional diagram of a flyback converter. Depending on the turn ratio N2/N1 and the feedback voltage, it can be implemented as a step-down or step-up converter.

When the switch is on, the current (I_p) flows through the primary winding creating a magnetic flux in the core and storing the energy. At this time, the voltage at the secondary keeps the same polarity (with respect to the dotted terminals), the diode is off and no current flows through it. When the switch is off, the voltage at the secondary and primary becomes reversed and the diode turns-on (I_d). The stored energy is then transferred to the load and the output filter capacitor. The energy stored in the capacitor will supply the load current during the next turn-on.

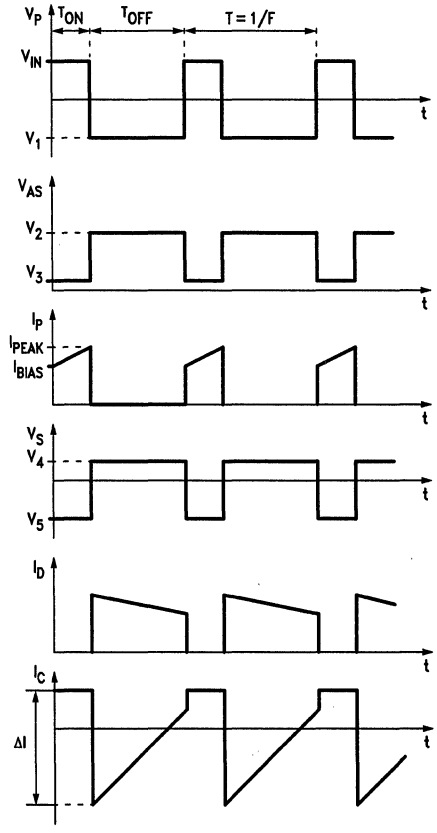


TL/K/6746–5

FIGURE 1. Typical Flyback Functional Diagram

Typical Applications (Continued)

V_p = Voltage at primary
V_{as} = Voltage across the switch
V_s = Voltage at the secondary
I_p = Current at primary
I_d = Current through diode
I_c = Current through output cap
I_{out} = Output current of the converter
ΔI = Ripple current
D = $T_{on}/(T_{off} + T_{on})$
F = Switching frequency
V_{df} = Forward voltage drop of the diode
$V_1 = V_{out} \times N_1/N_2$ $V_2 = V_{in} + V_{out}\, N_1/N_2$
V_3 = Saturation voltage of the switch
$V_4 = V_{out} + V_{df}$ $V_5 = V_{in} \times N_2/N_1$



TL/K/6746–6

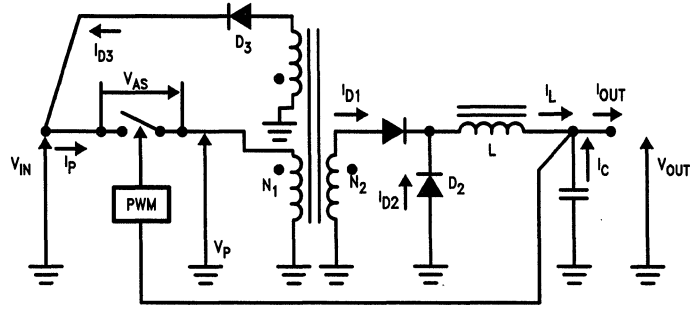
FIGURE 2. Typical Flyback Waveforms

The load current is not supplied directly by the input source when the switch is on, but only by the energy stored in the output capacitor. The output voltage is monitored by the feedback loop which controls the duty cycle (D) through the PWM (Pulse Width Modulator) which in turn, modulates the amount of energy being transferred from the input to the output. *Figure 2* shows the waveforms of a continuous mode flyback converter (primary current I_p is DC biased).

The Forward Principle

The forward converter is a little more complex and requires more components than the flyback, but the output ripple voltage is smaller. *Figure 3* shows a simplified diagram of a forward converter.

When the switch turns-on, a voltage $V_5 = V_1 \times N_2/N_1$ appears at the secondary of the transformer. The diode D_2



TL/K/6746–7

FIGURE 3. Typical Forward Functional Diagram

Typical Applications (Continued)

is off while D_1 turns-on, allowing the current to flow through the inductor L (I_{d1} and I_L), storing energy in its core, and supplying the load current (I_{out}) and the capacitor current (I_C) at the same time. When the switch turns-off, the magnetic energy stored in the core of the inductor creates a current (I_{d2}) which flows through the diode D_2. The load current I_{out} therefore, equals to $I_{d2} + I_C$.

During the "off" time of the switch, some residual magnetism will stay in the core of the transformer and has to be removed before the next cycle, so that it does not accumulate, leading to core saturation.

A demagnetizing winding is used to "dump" the residual energy back to the input or output of the converter. The functional principle of the demagnetizing winding is similar to the flyback in the sense that, during the turn-off time, the residual magnetism will generate a reverse voltage at the demagnetizing winding (with respect to the dotted terminals) turning on the diode D_3.

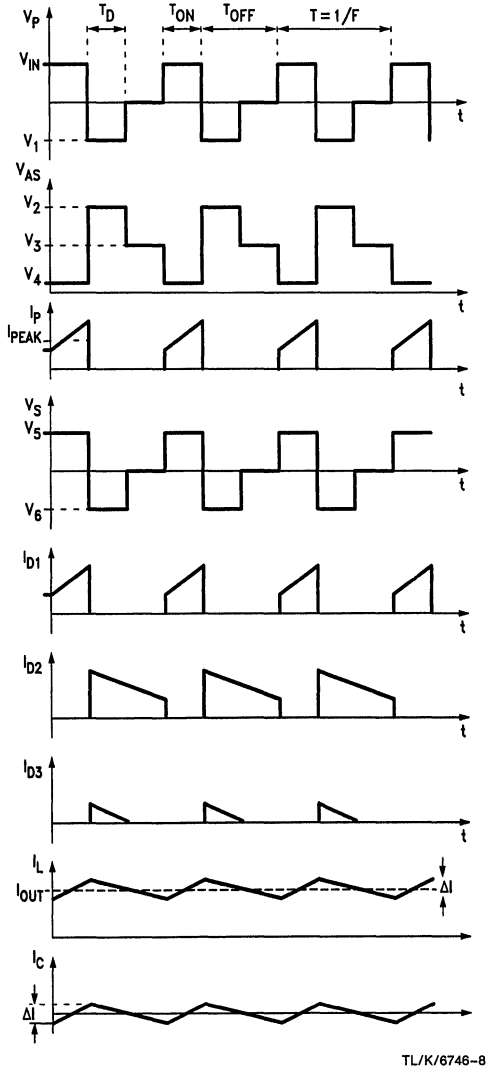
In the forward mode, when the switch is off, the load current is supplied by the energy stored in the output capacitor and the choke inductor but when the switch is on, it is supplied by the input source through the transformer. This accounts for the lower output ripple voltage.

The output voltage is monitored by the feedback loop, which controls the duty cycle through the PWM, which in turn modulates the amount of energy being transferred from the input to the output.

V_p = Voltage at primary
V_{as} = Voltage across the switch
V_s = Voltage at secondary
I_p = Current at primary
I_{d1} = Current through diode D_1
I_{d2} = Current through diode D_2
I_{d3} = Current through diode D_3
I_L = Current through inductor L
I_c = Current through output cap
I_{out} = Output current of the converter
Δ_I = Ripple current
F = Switching frequency
D = $T_{on} / (T_{off} + T_{on})$
V_1 = $V_{in} \times N_1/N_3$ $V_3 = V_{in}$
V_2 = $V_{in} + V_1$
V_4 = Saturation voltage of the switch
V_5 = $V_{in} \times N_2/N_1$ $V_6 = V_{in} \times N_2/N_3$

Figure 4 shows the waveforms of the forward converter.

When the switch is off, $V_{as} = V_{in} + (V_{in} \times N_1/N_3)$ during the demagnetization time (T_d) and then, drops to $V_{as} = V_{in}$ as indicated in *Figure 4*.

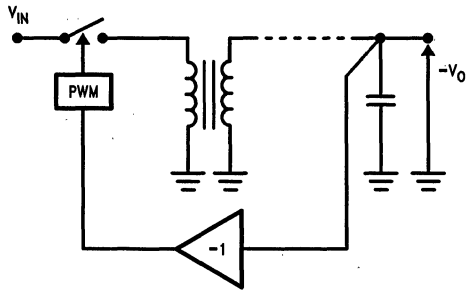


TL/K/6746–8

FIGURE 4. Typical Forward Waveforms

Typical Applications (Continued)

With both flyback and forward topologies, it is possible to design an inverting converter by using an external op-amp (*Figure 5*).



TL/K/6746–10

FIGURE 5

Flyback Step-Up Application

Figure 6 shows flyback converter in a step-up mode where an input voltage of +12V to +30V will be converted into a regulated output voltage of +50V.

Performance Data

Parameter	Conditions	Result
Efficiency	V_{out} = 50V @300 mA V_{in} = 15V	82%
Line Regulation	V_{out} = 50V @300 mA 12V ≤ V_{in} ≤ 30V	0.2%
Load Regulation	V_{in} = 15V V_{out} = 50V 50 mA ≤ I_{out} ≤ 300 mA	0.2%

Isolated Flyback Converter

Figure 7 shows an isolated flyback converter using a sense winding for feedback. Although, in practice the line regulation is acceptable, the load regulation can be marginal if the coupling between the windings is poor. However, the sense winding cannot detect any ohmic voltage drop in the main output so, a heavier gauge wire should be used to reduce this regulation error. Also, the sense winding will not sense the non-linear voltage drop across the diode, and this accounts for most of the load regulation inaccuracy. Therefore, the sense winding method is only recommended for applications where load variations are small.

Figure 7 shows an isolated flyback converter with an output of 5V at 2A. The input voltage range is from +10V to +40V. The output can be adjusted to +5V by using the 5 kΩ trimpot.

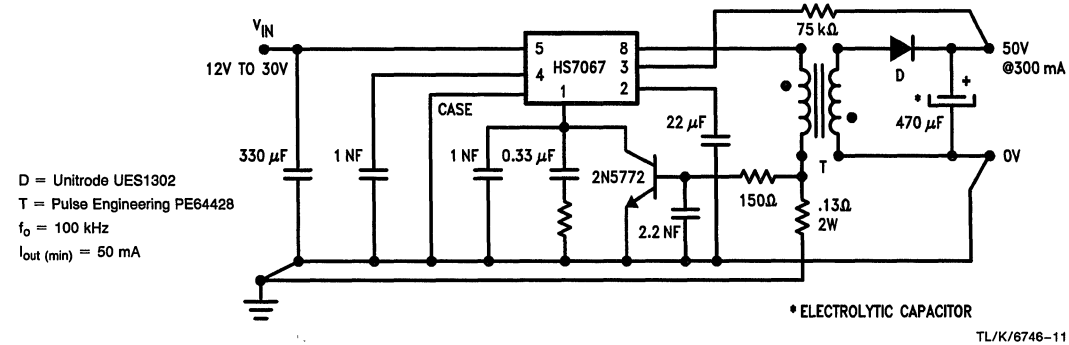
Performance Data

Parameter	Conditions	Result
Efficiency	V_{out} = 5V @ 2A V_{in} = 30V	75%
Line Regulation	V_{out} = 5V @ 2A 10V ≤ V_{in} ≤ 40V	5%
Load Regulation	V_{in} = 30V 1A ≤ I_{out} ≤ 2A	7%

Isolated Forward Converter

As described previously, forward converters exhibit lower output ripple voltage and the opto-coupler feedback scheme provides good regulation as well as input to output isolation.

An opto-coupler feedback is usually difficult to implement because the transfer function of the opto-coupler is non-linear, the current transfer ratio changes with time and temperture and also from one unit to another. *Figure 8* shows the circuit diagram of a 5V @ 3A power converter with an input voltage range of +14V to +30V using an isolated forward topology.



D = Unitrode UES1302
T = Pulse Engineering PE64428
f_o = 100 kHz
$I_{out\ (min)}$ = 50 mA

TL/K/6746–11

A 12V to 60V input Voltage Range is possible by replacing the HS7067 with a HS7107. The converter will operate in a discontinuous mode above 30V with a 300 mA load (the transformer's secondary current drops to zero before the switch turns on) and therefore, may generate more switching noise.

FIGURE 6. Flyback Step-Up Converter

Typical Applications (Continued)

D_1 = International Rectifier 50SQ060
D_2 = 1N4148
$I_{out\ (min)}$ = 1A
f_O = 100 kHz
T = Transformer made of a core Fenoxcube 1811PA2503B7
Primary = 8 turns with 5 strands #29
Secondary = 6 turns with 15 strands #30
Sense = 25 turns with 1 strand #30
windings should be interleaved in order to improve the coupling and regulation.

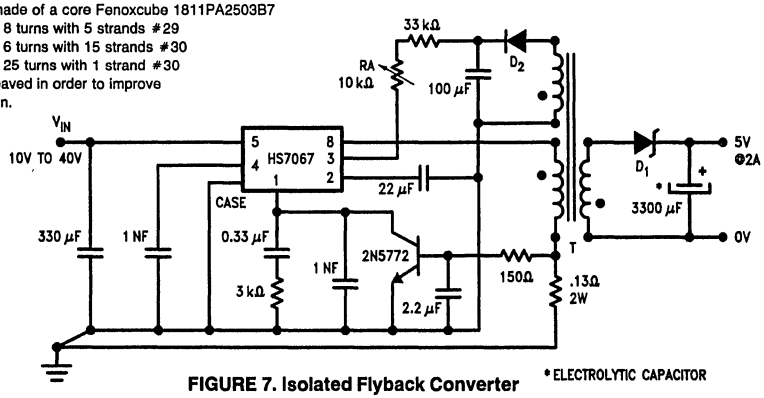
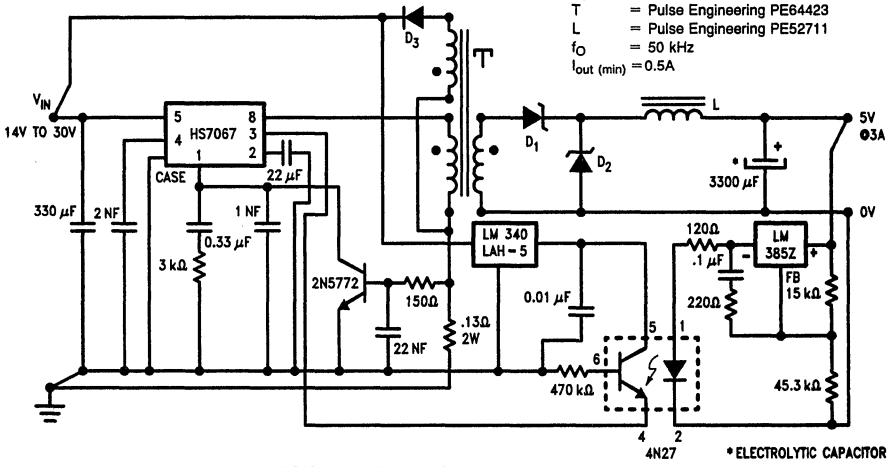


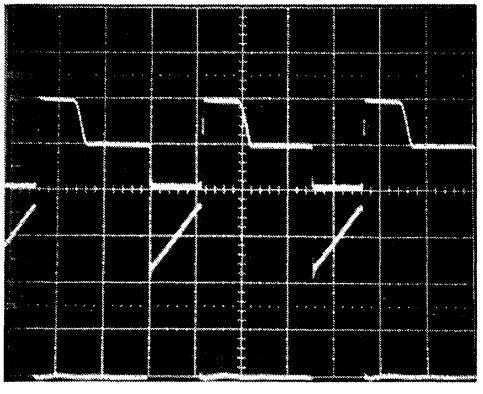
FIGURE 7. Isolated Flyback Converter * ELECTROLYTIC CAPACITOR TL/K/6746-12

D_1 = D_2 = International Rectifier 50SQ060
D_3 = Unitrode UES1302
T = Pulse Engineering PE64423
L = Pulse Engineering PE52711
f_O = 50 kHz
$I_{out\ (min)}$ = 0.5A



* ELECTROLYTIC CAPACITOR

FIGURE 8a. Isolated Forward Converter TL/K/6746-13



TL/K/6746-9

Figure 8b shows the typical forward converter waveforms in continuous mode which can be observed using the circuit from *Figure 8a*. Top waveform is the voltage across the switch (20V/div). Bottom waveform is the current throughout the switch (1A/dv). Horizontal Scale = 5 µS/dir. V_{in} = 20V; V_{out} = 5V @ 3A.

Figure 8b.

Typical Applications (Continued)

An LM 385z (adjustable reference) is used as a comparator and error amplifier. This reference always wants to maintain 1.2V between pins 1 and 2 and will draw as much current as necessary from the opto-coupler to achieve this. Therefore, the feedback loop is virtually independent of the gain of the opto-coupler.

Performance Data

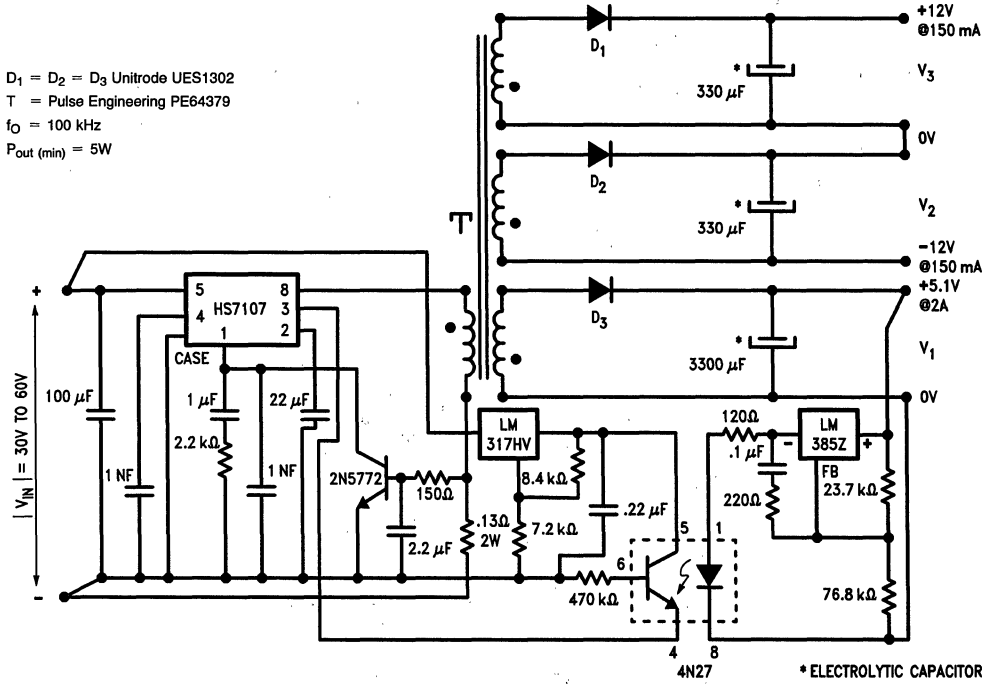
Parameter	Conditions	Result
Efficiency	V_{out} = 5V @ 3A V_{in} = 30V	78%
Line Regulation	V_{out} = 5V @ 3A 14V ≤ V_{in} ≤ 30V	0.1%
Load Regulation	V_{out} = 5V V_{in} = 20V 0.5A ≤ I_{out} ≤ 3A	0.1%

Isolated Telecom Converter

Figure 9 shows an isolated triple output converter which will transform a positive or negative input voltage of 32V to 60V to an uncommitted triple output of +12V, −12V, and 5V, which may be later referenced to the system ground. This converter is ideal for a step down converter of high positive voltage or high negative voltage such as −48V used in telecom circuits.

Performance Data

Parameter	Conditions	Result
Efficiency	V_1 = 5.1V @ 2A V_2 = −12V @ 150 mA V_3 = 12V @ 100 mA $\|V_{in}\|$ = 48V	62%
Line Regulation on Main Secondary	40V ≤ $\|V_{in}\|$ ≤ 60V V_1 = 5.1V @ 2A V_2 = −12V @ 150 mA V_3 = +12V @ 150 mA	0.8%
Load Regulation on Main Secondary	$\|V_{in}\|$ = 48V V_1 = 5.1V V_2 = 12V @ 150 mA V_3 = 12V @ 150 mA 0.5 ≤ I_{out} ≤ 2A	1%
Load Regulation on 12V Secondary for Simultaneous Load Changes	$\|V_{in}\|$ = 48V V_1 = 5.1V @ 2A V_2 = −12V V_3 = 12V 75 mA ≤ I_{out} ≤ 150 mA	5%



TL/K/6746–14

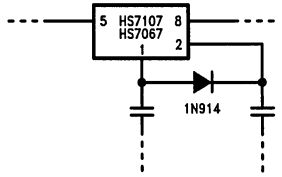
Note 10: An input voltage of −10V to −30V may cause the transformer to operate at a higher temperature at full load.

FIGURE 9. Telecom Flyback Converter

Application Hints

DUTY CYCLE LIMITING

In a flyback converter, the error amplifier sees 0V at the output of the converter during the initial turn-on, and forces the duty cycle to 100% until it sees the output voltage rising to the final value; but no voltage will appear if the switch does not turn off (see flyback principle). The result is that the core will saturate, reducing the effective impedance of the transformer to about 0Ω, and destroying the pass transistor. To prevent this, the duty cycle must be limited to a value at which the core does not saturate. A diode connected between pins 1 and 2 (*Figure 10*), will limit the duty cycle to about 80%.



TL/K/6746–15

FIGURE 10. Duty Cycle Limiting Circuit

SOFT START

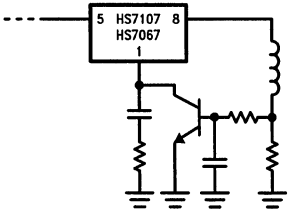
For any converter, connecting a large capacitor (20 to 200 μF) between pin 2 and the case is recommended to allow the reference voltage to slowly reach its final value after start-up. This allows the HS 7067/7107 to start-up smoothly and minimizes the inrush current. The time constant can be calculated by:

$$T = 10^3 \times C$$

It is always a good practice to incorporate soft start and duty cycle limiting when designing a switching power converter, especially when a current limit circuitry is not utilized.

CURRENT LIMIT

The schematic in *Figure 11* shows how to protect the pass transistor against excessive current, by sensing the current through a series resistor, and shorting the PWM control voltage at pin 1 to ground, using transistor 2N5772 (this is made possible by the 5 MΩ output impedance of the error amplifier), which will cause the pass transistor to turn off.



TL/K/6746–16

FIGURE 11. Current Limit Circuitry

The sense resistor should be a low inductance type, otherwise the series inductance creates a high impedance at transients and activates the shutdown circuitry. If such a resistor cannot be found, a 0.1 μF connected in parallel with it will compensate the series inductance.

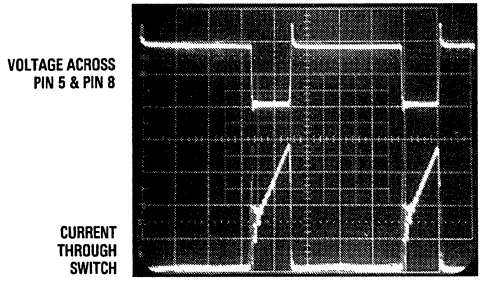
When such a circuitry is used, the duty cycle limiting diode becomes optional, but the soft start capacitor should still be at least 10 μF.

DECOUPLING AND GROUNDING

Special attention should be given to the decoupling of the HS 7107/7067 itself at the input (pin 5), where the capacitor must be at least 100 μF and connected as close to the device as possible. Large switching spikes at the input of the pass transistor can cause breakdown of the junction and destroy the device. (See Figure 12.)

The waveform at the top of the picture represents the voltage across the switch of a typical BUCK (step down) converter. When the switch is turned off, the current in the inductor falls to zero (see waveform at the bottom) and a switching spike occurs across the switch. This spike can reach several tens of volts on top of the normally expected voltage across the switch and lead to stress on the device if the overall voltage exceeds the maximum rating.

The picture below shows a spike of about ten volts with a 330 μF capacitor of average quality.



TL/K/6746–17

FIGURE 12

The reference voltage (pin 2) must be decoupled with at least 10 μF and the compensation network (pin 1) should be decoupled with a ceramic capacitor of 1 nF to 10 nF. Switching noise on the reference voltage pin (pin 2) or on the compensation pin (pin 1) can create different types of oscillations and instabilities.

Because of the high current and high voltage capability of the HS 7107/7067 a single point grounding or, at least a grounding where the force ground is separated from the circuit ground, is highly recommended.

Ordering Information (Transformers and Inductors)

PULSE ENGINEERING INC.
7250 Convoy Court
San Diego, CA 92111
USA

Tel: (619) 268-2400
TWX: 910-335-1527
FAX: 619 268-2515

National Semiconductor

PRELIMINARY

LH1605/LH1605C
5 Amp, High Efficiency Switching Regulator

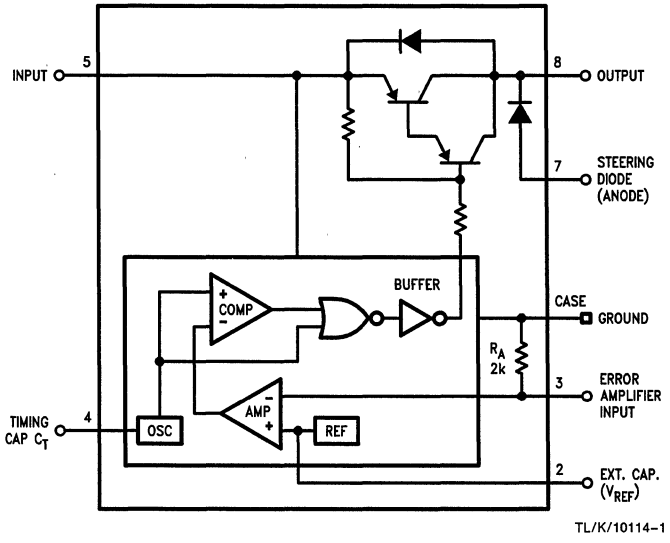
General Description

The LH1605 is a hybrid switching regulator with high output current capabilities. It incorporates a temperature-compensated voltage reference, a duty cycle modulator with the oscillator frequency programmable, error amplifier, high current-high voltage output switch, and a power diode. The LH1605 can supply up to 5A of output current over a wide range of regulated output voltage.

Features

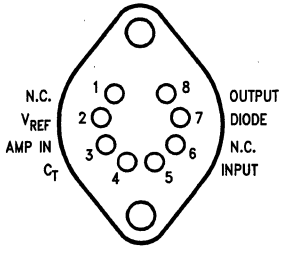
- Step down switching regulator
- Output adjustable from 3.0V to 30V
- 5A output current
- High efficiency
- Frequency adjustable to 100 kHz
- Standard 8-pin TO-3 package

Block and Connection Diagrams



TL/K/10114–1

Case is Ground



TL/K/10114–2

Top View

Order Number LH1605K or LH1605CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

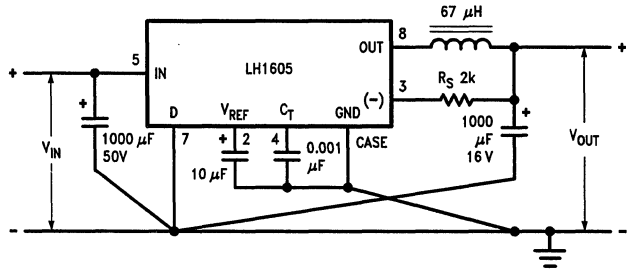
Input Voltage (V_{IN})	35V max
Output Current (I_O)	6A
Operating Temperature (T_J)	150°C
Internal Power Dissipation (P_D) (Note 1)	20W
Operating Temperature (T_A)	
LH1605C	−25°C to +85°C
LH1605	−55°C to +125°C
Storage Temperature Range (T_{STG})	−65°C to +150°C
Duty Cycle (D.C.)	20% to 80%
Steering Diode Reverse Voltage (V_R) (V_{8-7})	60V
Steering Diode Forward Current (I_D) (I_{7-8})	6A

Electrical Characteristics T_C = 25°C, V_{IN} = 15V, V_{OUT} = 10V unless otherwise specified

Symbol	Characteristics	Conditions	LH1605			LH1605C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output Voltage Range	$V_{IN} \geq V_O + 5V$ I_O = 2A (Note 2)	3.0		30	3.0		30	
V_S	Switch Saturation Voltage	I_C = 5.0A I_C = 2.0A		1.6 1.0	2.0 1.2		1.6 1.0	2.0 1.2	V
V_F	Steering Diode On Voltage	I_D = 5.0A I_D = 2.0A		1.2 1.0	2.8 2.0		1.2 1.0	2.8 2.0	
V_{IN}	Supply Voltage Range		10		35	10		35	
I_R	Steering Diode Reverse Current	V_R = 25V		0.1	5.0		0.1	5.0	μA
I_Q	Quiescent Current	I_{OUT} = 0.2A		20			20		mA
V_2	Voltage on Pin 2			2.5			2.5		V
$\Delta V_2/\Delta T$	V_2 Temperature Coeff.			100			100		ppm/°C
V_4	Voltage Swing—Pin 4			3.0			3.0		V
I_4	Charging Current—Pin 4			70			70		μA
R_A	Resistance Pin 3 to GND			2.0			2.0		kΩ
$\Delta R_A/\Delta T$	Resistance Temp. Coeff.			75			75		ppm/°C
t_r	Voltage Rise Time	I_{OUT} = 2.0A I_{OUT} = 5.0A		350 500			350 500		ns
t_f	Voltage Fall Time	I_{OUT} = 2.0A I_{OUT} = 5.0A		300 400			300 400		
t_s	Storage Time	I_{OUT} = 5.0A		1.5			1.5		μs
t_d	Delay Time			100			100		ns
P_D	Power Dissipation	V_{OUT} = 10V I_{OUT} = 5.0A		16			16		W
η	Efficiency			75			75		%
θ_{JC}	Thermal Resistance (Note 1)			5.0			5.0		°C/W

Note 1: θ_{JA} is typically 30°C/W for natural convection cooling.

Note 2: V_{OUT} refers to the output voltage range of switching supply after the output LC filter as shown in the Typical Application circuit.



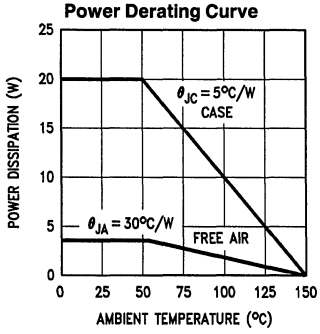
Minimum $V_{IN} - V_{OUT} = 5V$ for Proper Operation

$$R_S = \frac{2 \times 10^3 (V_{OUT} - 2.5)}{2.5}$$

$V_{IN} = 10 - 18V$
$V_{OUT} = 5V$
$I_{OUT} = 3A$ (Max)
$I_{OUT} = 1A$ (Min)
$\eta \cong 70\%$

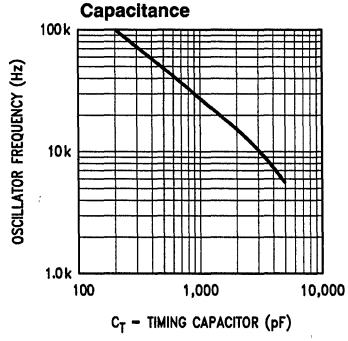
Load Reg. = 50 mV
Line Reg. = 10 mV
Ripple = 20 mV

Power Derating Curve



TL/K/10114-4

Frequency vs Timing Capacitance



TL/K/10114-5

Design Equations

$$\text{Efficiency } (\eta) = \frac{P_{OUT} \times 100}{P_{IN}}$$

$$\text{Transistor DC Losses } (P_T) = I_{OUT} \times V_S \left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)$$

$$\text{Diode DC Losses } (P_D) = I_{OUT} \times V_F \left(\frac{t_{OFF}}{t_{ON} + t_{OFF}}\right)$$

$$\text{Drive Circuit Losses } (D_L) = \frac{V_{IN}^2}{300} \times \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

$$\text{Switching Losses Transistor } (P_S) = V_{IN} \times I_{OUT} \times \frac{t_r + t_f}{2(t_{ON} + t_{OFF})}$$

$$\text{Transistor Duty Cycle} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Diode Duty Cycle} = \frac{t_{OFF}}{t_{ON} + t_{OFF}} = 1 - \frac{V_{OUT}}{V_{IN}}$$

$$\text{Power Inductor } (P_L) = I_{OUT}^2 \times R_L \text{ (Winding Resistance)}$$

$$\text{Efficiency } (\eta) = \frac{V_{OUT} I_{OUT}}{V_{OUT} I_{OUT} + P_T + P_D + D_L + P_S + P_L} \times 100\%$$

National Semiconductor

LM494
Pulse Width Modulated Control Circuit

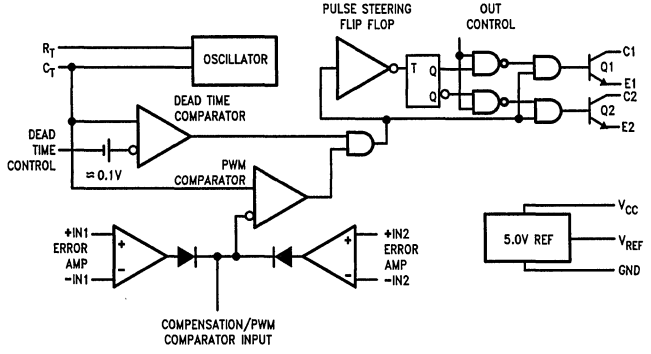
General Description

The LM494 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulated (PWM) switching power supplies, including push-pull, bridge and series configurations. The device can operate at switching frequencies between 1.0 kHz and 300 kHz and output voltages up to 40V. The operating temperature range specified for the LM494C is 0°C to 70°C and for the LM494V is −40°C to +85°C.

Features

- Uncommitted output transistors capable of 200 mA source or sink
- On-chip error amplifiers
- On-chip 5.0V reference
- Internal protection from double pulsing of outputs with narrow pulse widths or with supply voltages below specified limits
- Dead time control comparator
- Output control selects single ended or push-pull operation
- Easily synchronized (slaved) to other circuits

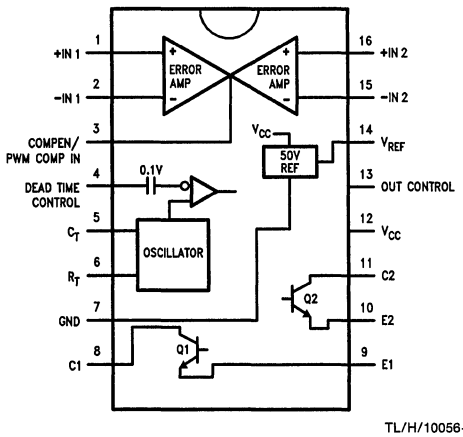
Block Diagram



TL/H/10056–2

Connection Diagram

16-Lead DIP



TL/H/10056–1

Top View

Ordering Information

Device Code	Package Code	Package Description
LM494IN	N16A	Molded DIP
LM494CJ	J16A	Ceramic DIP
LM494CN	N16A	Molded DIP

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Industrial (LM494I)	−40°C to +85°C
Commercial (LM494C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1, 2)	
16L-Ceramic DIP	1.50W
16L-Molded DIP	1.04W
Supply Voltage	42V
Voltage from Any Lead to Ground (except Lead 8 and Lead 11)	V_{CC} + 0.3V
Output Collector Voltage	42V
Peak Collector Current (I_{C1} and I_{C2})	250 mA
ESD Susceptibility	(to be determined)

Recommended Operating Conditions

Power Supply Voltage (V_{CC})	7.0V to 40V
Voltage on Any Lead except Leads 8 and 11 (Referenced to Ground) (V_I)	−0.3V to V_{CC} + 0.3V
Output Voltage Collector (V_{C1}, V_{C2})	−0.3V to 40V
Output Collector Current (I_{C1}, I_{C2})	200 mA
Timing Capacitor (C_T)	470 pF to 10 μF
Timing Resistor (R_T)	1.8 kΩ to 500 kΩ
Oscillator Frequency (f_{OSC})	1.0 kHz to 300 kHz

LM494

Electrical Characteristics

T_A = 0°C to +70°C for the LM494C, T_A = −40°C to +85°C for the LM494I, V_{CC} = 15V, f_{OSC} = 10 kHz, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
REFERENCE SECTION							
V_{REF}	Reference Voltage (Note 3)	I_{REF} = 1.0 mA		4.75	5.0	5.25	V
Reg_{LINE}	Line Regulation of Reference Voltage	7.0V ≤ V_{CC} ≤ 40V			2.0	25	mV
TCV_{REF}	Temperature Coefficient of Reference Voltage	0°C ≤ T_A ≤ 70°C			0.01	0.03	%/°C
Reg_{LOAD}	Load Regulation of Reference Voltage	1.0 mA ≤ I_{REF} ≤ 10 mA			1.0	15	mV
I_{OS}	Output Short Circuit Current	V_{REF} = 0V	0°C ≤ T_A ≤ +70°C	10	35	50	mA
			−40°C ≤ T_A ≤ +85°C		35		
OSCILLATOR SECTION							
f_{OSC}	Oscillator Frequency *(Figure 10)*	C_T = 0.01 μF, R_T = 12 kΩ			10		kHz
Δf_{OSC}	Oscillator Frequency Change	C_T = 0.01 μF, R_T = 12 kΩ	0°C ≤ T_A ≤ +70°C			2.0	%
			−40°C ≤ T_A ≤ +85°C			2.0	
DEAD TIME CONTROL SECTION							
$I_{IB\ (DT)}$	Input Bias Current	V_{CC} = 15V, 0V ≤ V_4 ≤ 5.25V			−2.0	−10	μA
$DC_{(Max)}$	Maximum Duty Cycle, Each Output	V_{CC} = 15V, Lead 4 = 0V, Output Control = V_{REF}		45			%
$V_{TH(in)}$	Input Threshold Voltage	Zero Duty Cycle			3.0	3.3	V
		Maximum Duty Cycle		0			
ERROR AMPLIFIER SECTIONS							
V_{IO}	Input Offset Voltage	V_3 = 2.5V			2.0	10	mV
I_{IO}	Input Offset Current	V_3 = 2.5V			25	250	nA
I_{IB}	Input Bias Current	V_3 = 2.5V			0.2	1.0	μA
V_{ICR}	Input Common Mode Voltage Range	7.0V ≤ V_{CC} ≤ 40V		−0.3		V_{CC}	V
A_{VS}	Large Signal Voltage Gain	0.5V ≤ V_3 ≤ 3.5V		60	74		dB
BW	Bandwidth				650		kHz

LM494

Electrical Characteristics $T_A = 0°C$ to $+70°C$ for the LM494C, $T_A = -40°C$ to $+85°C$ for the LM494I, $V_{CC} = 15V$, $f_{OSC} = 10$ kHz, unless otherwise specified (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PWM COMPARATOR SECTION *(Figure 9)*							
V_{THI}	Inhibit Threshold Voltage	Zero Duty Cycle			4.0	4.5	V
I_O^-	Output Sink Current (Note 4)	$0.5V \le V_3 \le 3.5V$		−0.2	−0.6		mA
I_O^+	Output Source Current (Note 4)	$0.5V \le V_3 \le 3.5V$		2.0			mA
OUTPUT SECTION							
$V_{CE(sat)}$	Output Saturation Voltage Common Emitter Configuration *(Figure 3)*	$V_E = 0V$, $I_C = 200$ mA	$0°C \le T_A \le +70°C$ $-40°C \le T_A \le +85°C$		1.1	1.3	V
	Emitter Follower Configuration *(Figure 4)*	$V_C = 15V$, $I_E = 200$ mA			1.5	2.5	
$I_{C(off)}$	Collector Off-State Current	$V_{CC} = 40V$, $V_{CE} = 40V$			2.0	100	μA
$I_{E(off)}$	Emitter Off-State Current	$V_{CC} = V_C = 40V$, $V_E = 0$	$0°C \le T_A \le +70°C$, $-40°C \le T_A \le +85°C$			−100	μA
OUTPUT CONTROL *(Figure 6)*							
V_{OCL}	Output Control Voltage Required for Single Ended or Parallel Output Operation					0.4	V
V_{OCH}	Output Control Voltage Required for Push-Pull Operation			2.4			V
TOTAL DEVICE							
I_{CC}	Standby Power Supply Current				6.0	10	mA
OUTPUT AC CHARACTERISTICS Use Recommended Operating Conditions with $T_A = 25°C$							
t_r	Rise Time of Output Voltage Common Emitter Configuration *(Figure 3)*				100	200	ns
	Emitter Follower Configuration *(Figure 4)*				100	200	
t_f	Fall Time of Output Voltage Common Emitter Configuration *(Figure 3)*				25	100	ns
	Emitter Follower Configuration *(Figure 4)*				40	100	

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Note 3: Selected devices with tightened tolerance reference voltage available.

Note 4: These limits apply when the voltage measured at Lead 3 is within the range specified.

Functional Description

The basic oscillator (switching) frequency is controlled by an external resistor (R_T) and capacitor (C_T). The relationship between the values of R_T, C_T and frequency is shown in *Figure 10*.

The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip-flop and the output control logic.

The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5.0V internal reference. See *Figure 7* for error amp sensing techniques. The second error amp is typically used to implement current-limiting.

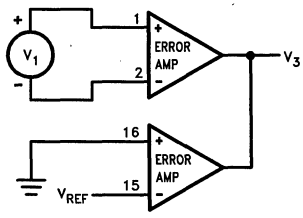
The output control logic selects either push-pull or single-ended operation of the output transistors (see *Figure 6*).

The dead time control prevents on-state overlap of the output transistors as can be seen in *Figure 5*. The dead time is approximately 3.0% or 5.0% of the total period if the dead time control is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5.0V.

The frequency response of the error amps *(Figure 11)* can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal and the inverting input of the error amps.

The switching frequency of two or more LM494 circuits can be synchronized. The timing capacitor, C_T, is connected as shown in *Figure 8*. Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master. R_T is required only for the master circuit.

Test Circuits



TL/H/10056–3

FIGURE 1. Error Amplifier Test Circuit

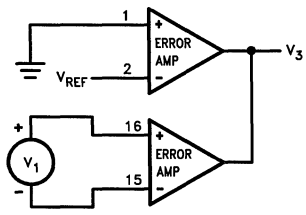


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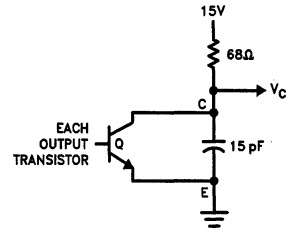
FIGURE 2. Current Limit Sense Amplifier Test Circuit



TL/H/10056–5

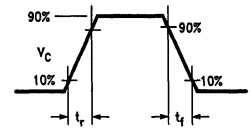


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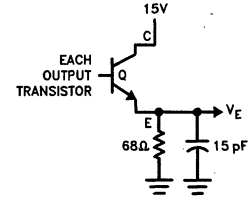
FIGURE 3. Common Emitter Configuration Test Circuit and Waveform



TL/H/10056–7

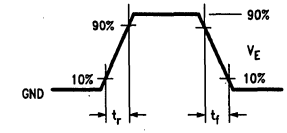


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FIGURE 4. Emitter Follower Configuration Test Circuit and Waveform

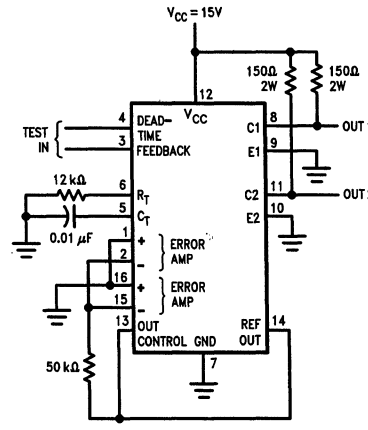

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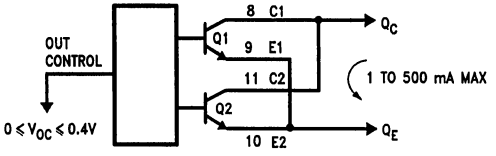
FIGURE 5. Dead Time and Feedback Control Test Circuit

Typical Applications



TL/H/10056–10

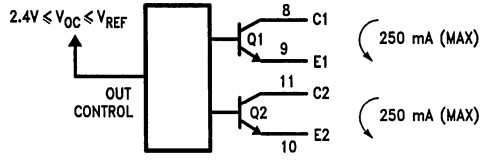


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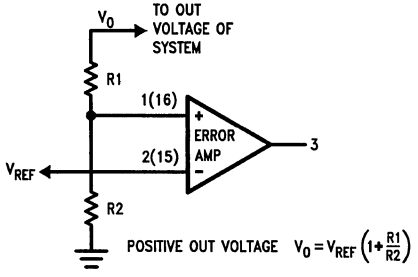
FIGURE 6. Output Connections for Single Ended and Push-Pull Configurations



TL/H/10056–12

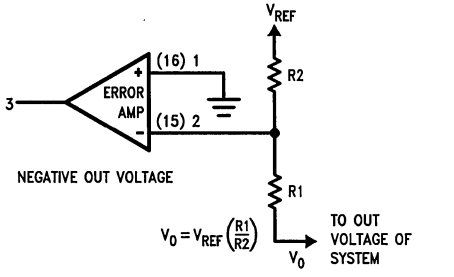


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FIGURE 7. Error Amplifier Sensing Techniques

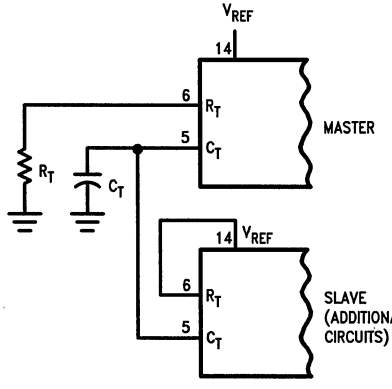

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FIGURE 8. Slaving Two or More Control Circuits

Typical Applications (Continued)

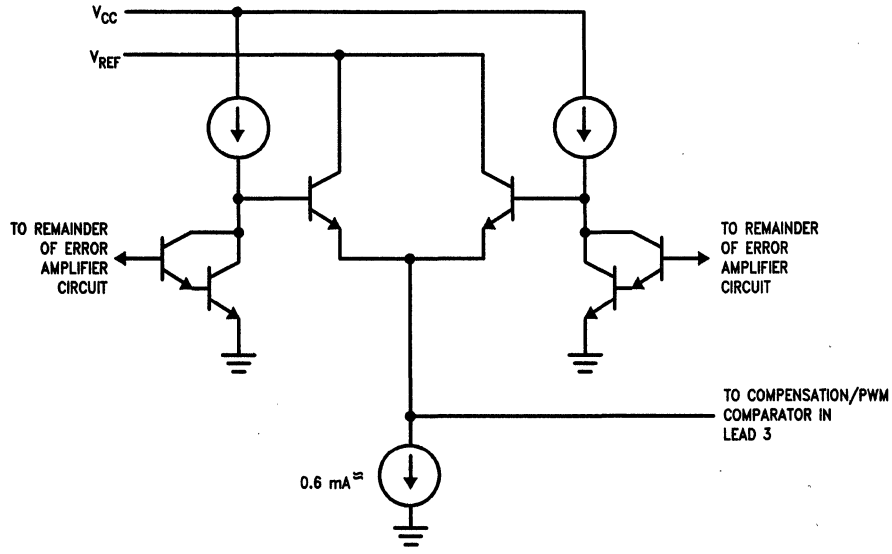


FIGURE 9. Error Amplifier and Current Limit Sense Amplifier Output Circuits

Typical Performance Characteristics

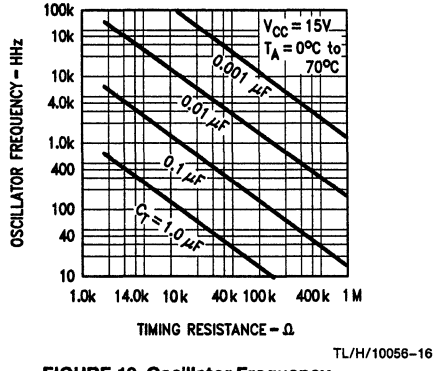


FIGURE 10. Oscillator Frequency vs Timing Resistance

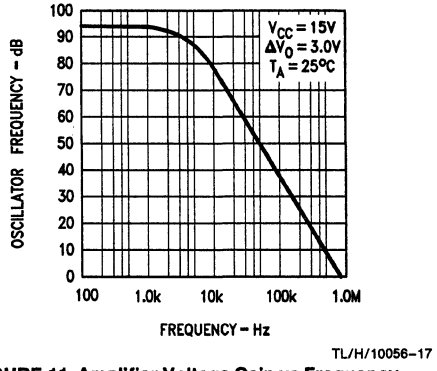
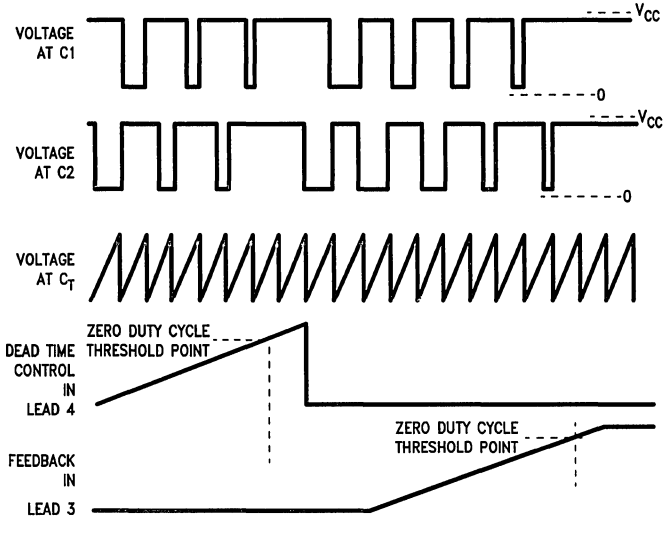


FIGURE 11. Amplifier Voltage Gain vs Frequency

Voltage Waveforms



TL/H/10056–18

National Semiconductor

LM1524D/LM2524D/LM3524D Regulating Pulse Width Modulator

General Description

The LM1524D family is an improved version of the industry standard LM1524. It has improved specifications and additional features yet is pin for pin compatible with existing 1524 families. New features reduce the need for additional external circuitry often required in the original version.

The LM1524D has a ±1% precision 5V reference. The current carrying capability of the output drive transistors has been raised to 200 mA while reducing V_{CEsat} and increasing V_{CE} breakdown to 60V. The common mode voltage range of the error-amp has been raised to 5.5V to eliminate the need for a resistive divider from the 5V reference.

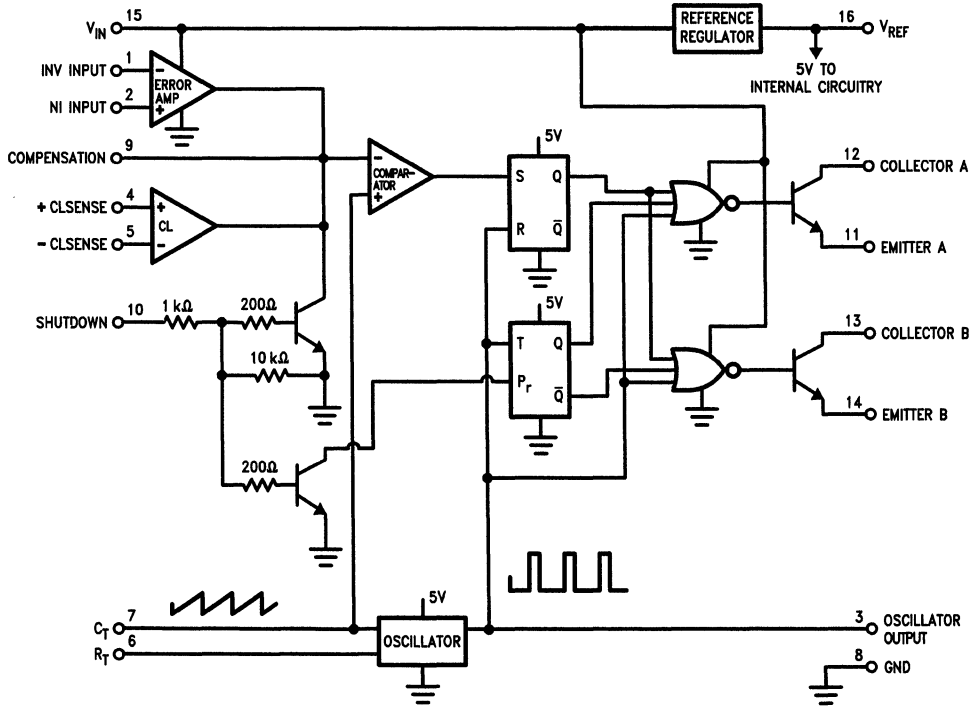
In the LM1524D the circuit bias line has been isolated from the shut-down pin. This prevents the oscillator pulse amplitude and frequency from being disturbed by shut-down. Also at high frequencies (≅300 kHz) the max. duty cycle per output has been improved to 44% compared to 35% max. duty cycle in other 1524s.

In addition, the LM1524D can now be synchronized externally, through pin 3. Also a latch has been added to insure one pulse per period even in noisy environments. The LM1524D includes double pulse suppression logic that insures when a shut-down condition is removed the state of the T-flip-flop will change only after the first clock pulse has arrived. This feature prevents the same output from being pulsed twice in a row, thus reducing the possibility of core saturation in push-pull designs.

Features

- Fully interchangeable with standard LM1524 family
- ±1% precision 5V reference with thermal shut-down
- Output current to 200 mA DC
- 60V output capability
- Wide common mode input range for error-amp
- One pulse per period (noise suppression)
- Improved max. duty cycle at high frequencies
- Double pulse suppression
- Synchronize through pin 3

Block Diagram



TL/H/8650–1

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	40V
Collector Supply Voltage	
(LM1524D)	60V
(LM2524D)	55V
(LM3524D)	40V
Output Current DC (each)	200 mA
Oscillator Charging Current (Pin 7)	5 mA
Internal Power Dissipation	1W
Operating Junction Temperature Range J Package (Note 2)	
LM1524D	−55°C to +150°C
LM2524D	−40°C to +150°C
Operating Maximum Junction Temperature N Package (Note 2)	
LM2524D	−40°C to +125°C
LM3524D	0°C to +125°C
Maximum Junction Temperature	150°
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec.) J Pkg.	300°C
Lead Temperature (Soldering 4 sec.) N Pkg.	260°C

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	LM1524D			LM2524D			LM3524D			Units
			Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
REFERENCE SECTION												
V_{REF}	Output Voltage		5	4.95 **4.90**		5	4.85	**4.80**	5	4.75		V_{Min}
				5.05 **5.10**			5.15	**5.20**		5.25		V_{Max}
V_{RLine}	Line Regulation	V_{IN} = 8V to 40V	10	**20**		10	15	**30**	10	25	50	mV_{Max}
V_{RLoad}	Load Regulation	I_L = 0 mA to 20 mA	5	**15**		10	15	**25**	10	25	50	mV_{Max}
$\frac{\Delta V_{IN}}{\Delta V_{REF}}$	Ripple Rejection	f = 120 Hz	66			66			66			dB
I_{OS}	Short Circuit Current	V_{REF} = 0	50	25		50	25		50	25		mA Min
				150			180			200		mA Max
N_O	Output Noise	10 Hz ≤ f ≤ 10 kHz	40		100	40		100	40		100	$\mu V_{rms\ Max}$
	Long Term Stability	T_A = 125°C	20			20			20			mV/kHr
OSCILLATOR SECTION												
f_{OSC}	Max. Freq.	R_T = 1k, C_T = 0.001 μF (Note 7)	550		500	550		500	350			kHz_{Min}
f_{OSC}	Initial Accuracy	R_T = 5.6k, C_T = 0.01 μF (Note 7)	20	18.5		20	17.5		20	17.5		kHz_{Min}
				21.5			22.5			22.5		kHz_{Max}
		R_T = 2.7k, C_T = 0.01 μF (Note 7)	38	36		38	34		38	30		kHz_{Min}
				40			42			46		kHz_{Max}
Δf_{OSC}	Freq. Change with V_{IN}	V_{IN} = 8 to 40V	0.5	1		0.5	1		0.5	1.0		$\%_{Max}$
Δf_{OSC}	Freq. Change with Temp.	T_A = −55°C to +125°C at 20 kHz R_T = 5.6k, C_T = 0.01 μF	5			5			5			%
V_{OSC}	Output Amplitude (Pin 3) (Note 8)	R_T = 5.6k, C_T = 0.01 μF	3	2.4		3	2.4		3	2.4		V_{Min}
t_{PW}	Output Pulse Width (Pin 3)	R_T = 5.6k, C_T = 0.01 μF	0.5	1.5		0.5	1.5		0.5	1.5		μs_{Max}

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	LM1524D			LM2524D			LM3524D			Units
			Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
OSCILLATOR SECTION (Continued)												
	Sawtooth Peak Voltage	R_T = 5.6k, C_T = 0.01 μF	3.4	**3.6**		3.4	3.6	**3.8**		3.8		V_{Max}
	Sawtooth Valley Voltage	R_T = 5.6k, C_T = 0.01 μF	1.1	**0.8**		1.1	0.8	**0.6**		0.6		V_{Min}
ERROR-AMP SECTION												
V_{IO}	Input Offset Voltage	V_{CM} = 2.5V	0.5	**5**		2	8	**10**	2	10		mV_{Max}
I_{IB}	Input Bias Current	V_{CM} = 2.5V	1	**5**		1	8	**10**	1	10		μA_{Max}
I_{IO}	Input Offset Current	V_{CM} = 2.5V	0.5	**1**		0.5	1.0	**1**	0.5	1		μA_{Max}
I_{COSI}	Compensation Current (Sink)	$V_{IN(I)} - V_{IN(NI)}$ = 150 mV	95	75 115		95	65 125		95	65 125		μA_{Min} μA_{Max}
I_{COSO}	Compensation Current (Source)	$V_{IN(NI)} - V_{IN(I)}$ = 150 mV	−95	−115 −75		−95	−125 −65		−95	−125 −65		μA_{Min} μA_{Max}
A_{VOL}	Open Loop Gain	R_L = ∞, V_{CM} = 2.5 V	80	**74**		80	74	**60**	80	70	60	dB_{Min}
VCMR	Common Mode Input Voltage Range			**1.5** **5.5**			1.5 5.5	**1.4** **5.4**		1.5 5.5		V_{Min} V_{Max}
CMRR	Common Mode Rejection Ratio		90	80		90	80		90	70		dB_{Min}
G_{BW}	Unity Gain Bandwidth	A_{VOL} = 0 dB, V_{CM} = 2.5V	3			3			2			MHz
V_O	Output Voltage Swing	R_L = ∞		0.5 5.5			0.5 5.5			0.5 5.5		V_{Min} V_{Max}
PSRR	Power Supply Rejection Ratio	V_{IN} = 8 to 40V	80		76	80		70	80	65		db_{Min}
COMPARATOR SECTION												
$\frac{t_{ON}}{t_{OSC}}$	Minimum Duty Cycle	Pin 9 = 0.8V, [R_T = 5.6k, C_T = 0.01 μF]	0	0		0	0		0	0		$\%_{Max}$
$\frac{t_{ON}}{t_{OSC}}$	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 5.6k, C_T = 0.01 μF]	49	47		49	45		49	45		$\%_{Min}$
$\frac{t_{ON}}{t_{OSC}}$	Maximum Duty Cycle	Pin 9 = 3.9V, [R_T = 1k, C_T = 0.001 μF]	44	40		44	35		44	35		$\%_{Min}$
V_{COMPZ}	Input Threshold (Pin 9)	Zero Duty Cycle	1			1			1			V
V_{COMPM}	Input Threshold (Pin 9)	Maximum Duty Cycle	3.5			3.5			3.5			V
I_{IB}	Input Bias Current		−1			−1			−1			μA

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	LM1524D			LM2524D			LM3524D			Units
			Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
CURRENT LIMIT SECTION												
V_{SEN}	Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$ 150 mV	200	190 210		200	180 220		200	180 220		mV_{Min} mV_{Max}
TC-V_{sense}	Sense Voltage T.C.		0.2			0.2			0.2			mV/°C
	Common Mode Voltage Range	$V_5 - V_4$ = 300 mV	−0.7 1			−0.7 1			−0.7 1			V_{Min} V_{Max}
SHUT DOWN SECTION												
V_{SD}	High Input Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq$ 150 mV	1	0.5 1.5		1	0.5 1.5		1	0.5 1.5		V_{Min} V_{Max}
I_{SD}	High Input Current	$I_{(pin\ 10)}$	1			1			1			mA
OUTPUT SECTION (EACH OUTPUT)												
V_{CES}	Collector Emitter Voltage Breakdown	$I_C \leq 100\ \mu A$		60			55			40		V_{Min}
I_{CES}	Collector Leakage Current	V_{CE} = 60V	0.1	50								μA_{Max}
		V_{CE} = 55V				0.1	50					
		V_{CE} = 40V							0.1	50		
V_{CESAT}	Saturation Voltage	I_E = 20 mA	0.2	0.4		0.2	0.5		0.2	0.7		V_{Max}
		I_E = 200 mA	1.5	2.2		1.5	2.2		1.5	2.5		
V_{EO}	Emitter Output Voltage	I_E = 50 mA	18	17		18	17		18	17		V_{Min}
t_R	Rise Time	V_{IN} = 20V, I_E = −250 μA R_C = 2k	200			200			200			ns
t_F	Fall Time	R_C = 2k	100			100			100			ns
SUPPLY CHARACTERISTICS SECTION												
V_{IN}	Input Voltage Range	After Turn-on		8 40			8 40			8 40		V_{Min} V_{Max}
T	Thermal Shutdown Temp.	(Note 2)	160			160			160			°C
I_{IN}	Stand By Current	V_{IN} = 40V (Note 6)	5	10		5	10		5	10		mA

Note 1: Unless otherwise stated, these specifications apply for $T_A = T_J = 25°C$. Boldface numbers apply over the rated temperature range: LM1524D is −55°C to 125°C, LM2524D is −40° to 85°C and LM3524D is 0°C to 70°C. V_{IN} = 20V and f_{OSC} = 20 kHz.

Note 2: For operation at elevated temperatures, devices in the J package must be derated based on a thermal resistance of 132°C/W, junction to ambient, and devices in the N package must be derated based on a thermal resistance of 86°C/W, junction to ambient.

Note 3: Tested limits are guaranteed and 100% tested in production.

Note 4: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage range. These limits are not used to calculate outgoing quality level.

Note 5: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

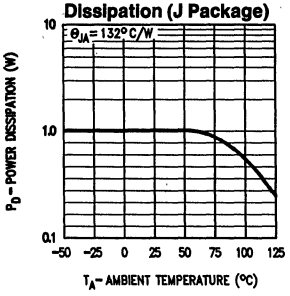
Note 6: Pins 1, 4, 7, 8, 11, and 14 are grounded; Pin 2 = 2V. All other inputs and outputs open.

Note 7: The value of a C_t capacitor can vary with frequency. Careful selection of this capacitor must be made for high frequency operation. Polystyrene was used in this test. NPO ceramic or polypropylene can also be used.

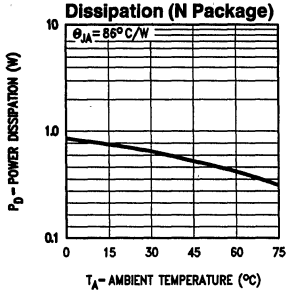
Note 8: OSC amplitude is measured open circuit. Available current is limited to 1 mA so care must be exercised to limit capacitive loading of fast pulses.

Typical Performance Characteristics

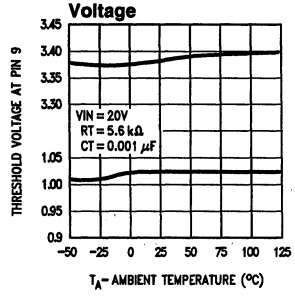
Maximum Average Power Dissipation (J Package)



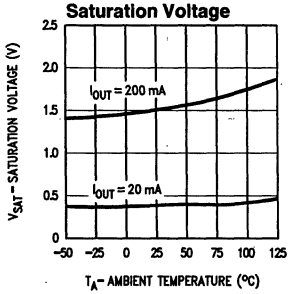
Maximum Average Power Dissipation (N Package)



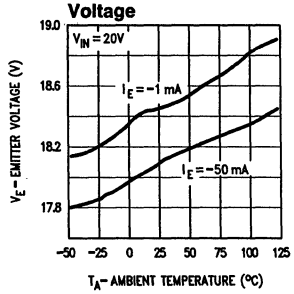
Maximum & Minimum Duty Cycle Threshold Voltage



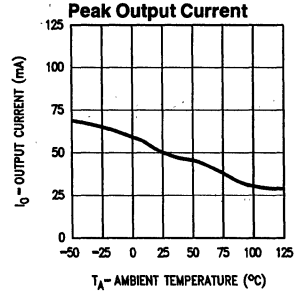
Output Transistor Saturation Voltage



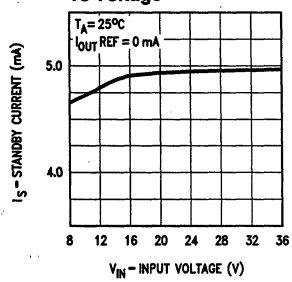
Output Transistor Emitter Voltage



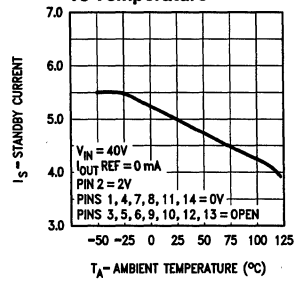
Reference Transistor Peak Output Current



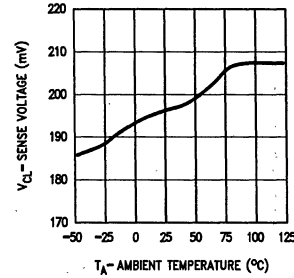
Standby Current vs Voltage



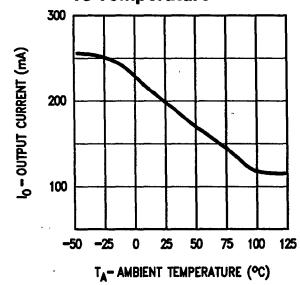
Standby Current vs Temperature



Current Limit Sense Voltage



Switching Transistor Peak Output Current vs Temperature



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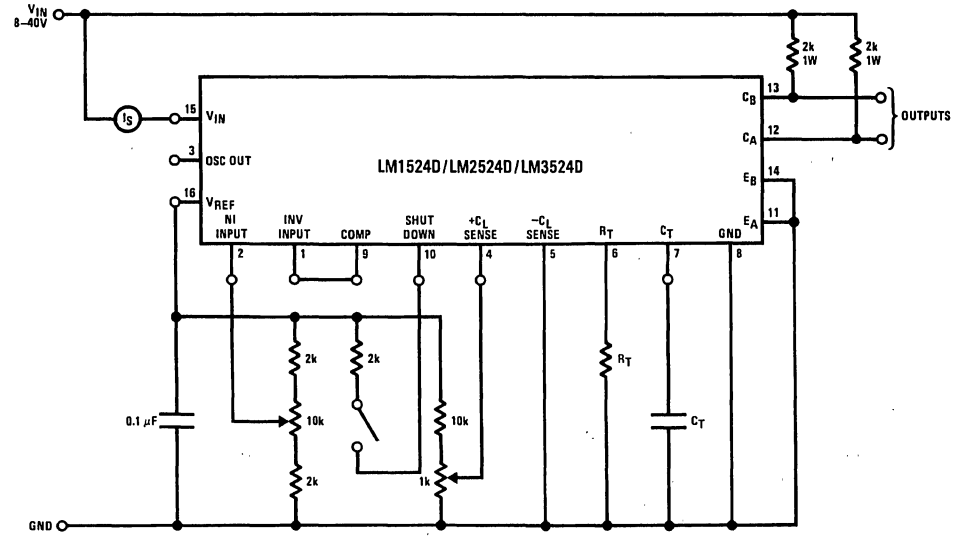
Test Circuit



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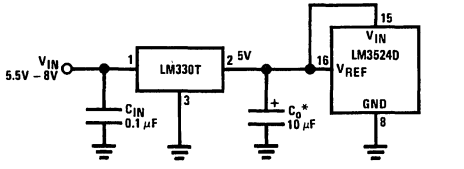
Functional Description

INTERNAL VOLTAGE REGULATOR

The LM1524D has an on-chip 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6V–8V are to be used, a pre-regulator, as shown in *Figure 1*, must be added.



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*Minimum C_O of 10 μF required for stability.

FIGURE 1

OSCILLATOR

The LM1524D provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown is *Figure 2*. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in *Figure 3*. The recommended values of R_T are 1.8 kΩ to 100 kΩ, and for C_T, 0.001 μF to 0.1 μF.

If two or more LM1524D's must be synchronized together, the easiest method is to interconnect all pin 3 terminals, tie all pin 7's (together) to a single C_T, and leave all pin 6's open except one which is connected to a single R_T. This method works well unless the LM1524D's are more than 6" apart.

A second synchronization method is appropriate for any circuit layout. One LM1524D, designated as master, must have its R_TC_T set for the correct period. The other slave LM1524D(s) should each have an R_TC_T set for a 10% longer period. All pin 3's must then be interconnected to allow the master to properly reset the slave units.

The oscillator may be synchronized to an external clock source by setting the internal free-running oscillator frequency 10% slower than the external clock and driving pin 3 with a pulse train (approx. 3V) from the clock. Pulse width should be greater than 50 ns to insure full synchronization.

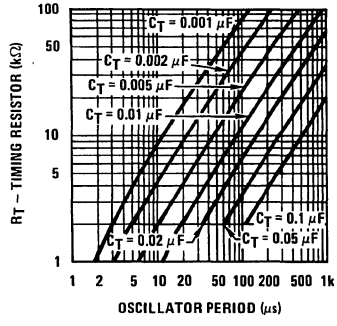

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FIGURE 2

Functional Description (Continued)

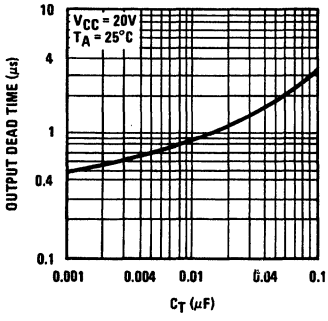

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FIGURE 3

ERROR AMPLIFIER

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 86 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in *Figure 4*.

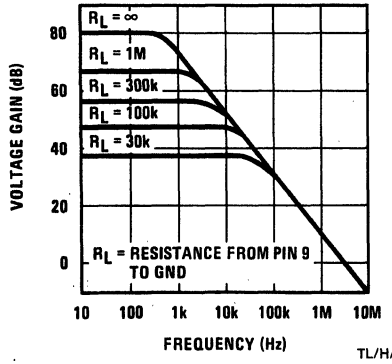

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FIGURE 4

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \cong 5\ M\Omega$). For this reason a DC voltage can be applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in *Figure 5*.

The duty cycle is calculated as the percentage ratio of each output's ON-time to the oscillator period. Paralleling the outputs doubles the observed duty cycle.

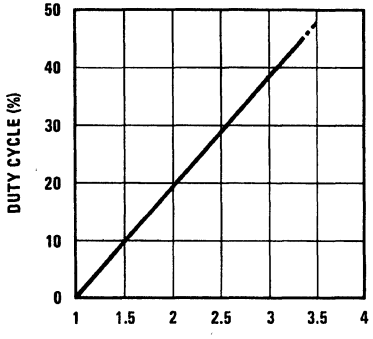

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FIGURE 5

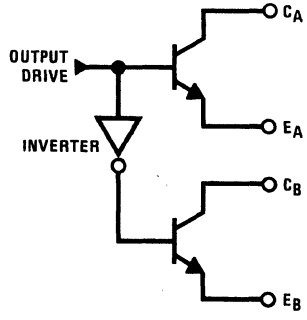
The amplifier's inputs have a common-mode input range of 1.5V–5.5V. The on board regulator is useful for biasing the inputs to within this range.

CURRENT LIMITING

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$ sense terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

OUTPUT STAGES

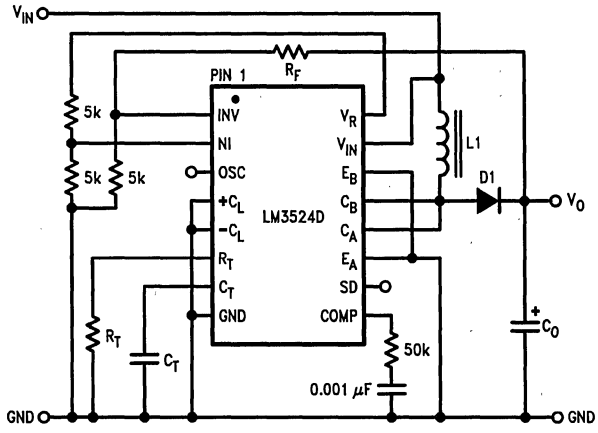
The outputs of the LM1524D are NPN transistors, capable of a maximum current of 200 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in *Figure 6*.



TL/H/8650–9

FIGURE 6

Typical Applications



Design Equations

$$R_F = 5k\left(\frac{V_O}{2.5} - 1\right)$$

$$f_{OSC} \approx \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN}^2 (V_O - V_{IN})}{f_{OSC} I_O V_O^2}$$

$$C_O = \frac{I_O (V_O - V_{IN})}{f_{OSC} \Delta V_O V_O}$$

$$I_{O(MAX)} = I_{IN} \frac{V_{IN}}{V_O}$$

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FIGURE 7. Positive Regulator, Step-Up Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

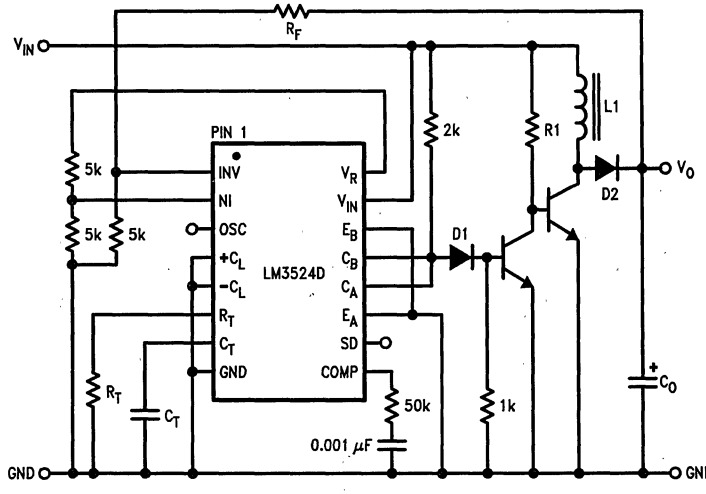

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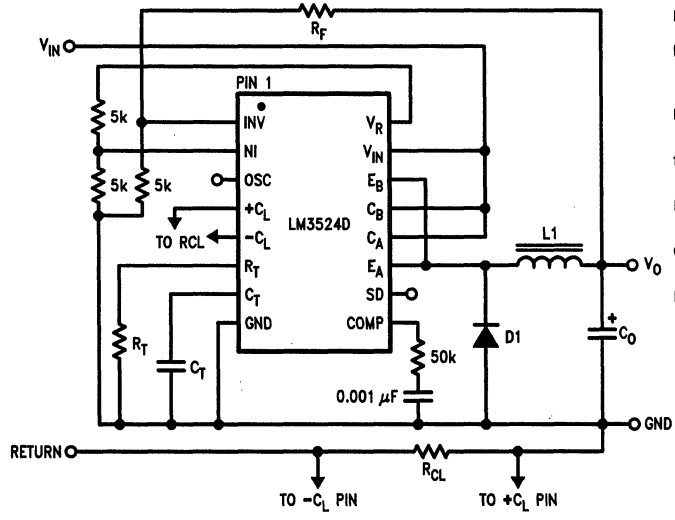
FIGURE 8. Positive Regulator, Step-Up Boosted Current Configuration

2

Typical Applications (Continued)



Design Equations

$$R_F = 5\,k\Omega\left(\frac{V_o}{2.5} - 1\right)$$

$$R_{CL} = \frac{\text{Current Limit Sense Volt}}{I_{o(MAX)}}$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5V_o\,(V_{IN} - V_o)}{I_o\,V_{IN}\,f_{OSC}}$$

$$C_o = \frac{(V_{IN} - V_o)\,V_o T^2}{8\,\Delta V_o\,V_{IN} L1}$$

$$I_{o(MAX)} = I_{IN}\frac{V_{IN}}{V_o}$$

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FIGURE 9. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

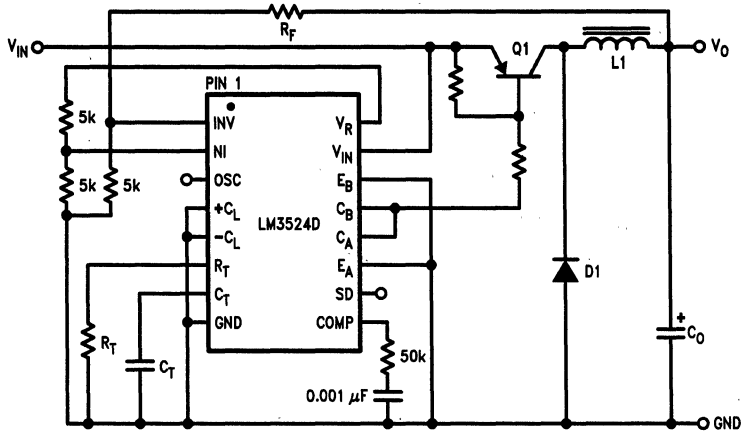

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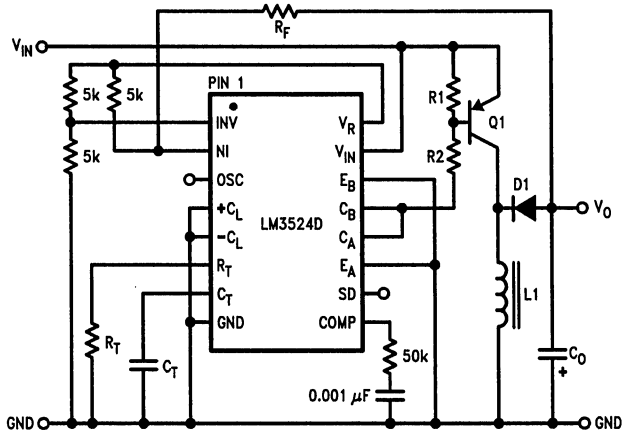
FIGURE 10. Positive Regulator, Step-Down Boosted Current Configuration

Typical Applications (Continued)



Design Equations

$$R_F = 5k\left(1 - \frac{V_o}{2.5}\right)$$

$$f_{OSC} \cong \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN}\, V_o}{f_{OSC}\,(V_o + V_{IN})\, I_o}$$

$$C_o = \frac{I_o V_o}{\Delta V_o\, f_{OSC}\,(V_o + V_{IN})}$$

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FIGURE 11. Boosted Current Polarity Inverter

BASIC SWITCHING REGULATOR THEORY AND APPLICATIONS

The basic circuit of a step-down switching regulator circuit is shown in *Figure 12*, along with a practical circuit design using the LM3524D in *Figure 15*.

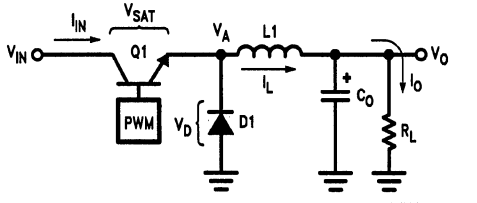

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FIGURE 12. Basic Step-Down Switching Regulator

The circuit works as follows: Q1 is used as a switch, which has ON and OFF times controlled by the pulse width modulator. When Q1 is ON, power is drawn from V_{IN} and supplied to the load through L1; V_A is at approximately V_{IN}, D1 is reverse biased, and C_O is charging. When Q1 turns OFF the inductor L1 will force V_A negative to keep the current flowing in it, D1 will start conducting and the load current will flow through D1 and L1. The voltage at V_A is smoothed by the L1, C_O filter giving a clean DC output. The current flowing through L1 is equal to the nominal DC load current plus some ΔI_{IL} which is due to the changing voltage across it. *A good rule of thumb is to set* $\Delta I_{Lp\text{-}p} \cong 40\% \times I_O$.

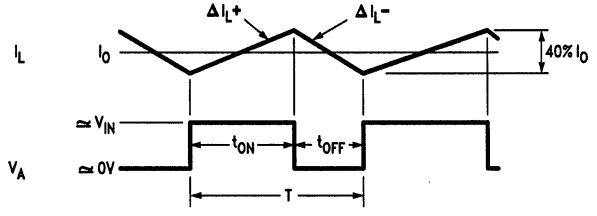

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FIGURE 13

Typical Applications (Continued)

From the relation $V_L = L\frac{d_i}{d_t}$, $\Delta I_L \cong \frac{V_L T}{L1}$

$$\Delta I_L^+ = \frac{(V_{IN} - V_O)\, t_{ON}}{L1};\ \Delta I_L^- = \frac{V_O\, t_{OFF}}{L1}$$

Neglecting V_{SAT}, V_D, and settling $\Delta I_L^+ = \Delta I_L^-$;

$$\boxed{V_O \cong V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right)} = V_{IN}\left(\frac{t_{ON}}{T}\right);$$

where T = Total Period

The above shows the relation between V_{IN}, V_O and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right),$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)}\, V_{IN} = (I_{O(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right) V_{IN}$$

$$P_O = I_O V_O$$

The efficiency, η, of the circuit is:

$$\eta MAX = \frac{P_O}{P_{IN}} = \frac{I_O V_O}{I_O \frac{(t_{ON})}{T} V_{IN} + \frac{(V_{SAT}\, t_{ON} + V_{D1} t_{OFF})}{T} I_O}$$

$$= \boxed{\frac{V_O}{V_O + 1}} \text{ for } V_{SAT} = V_{D1} = 1V.$$

ηMAX will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} \cong \frac{(\Delta I_L^+) \times L1}{(V_{IN} - V_O)},\ t_{OFF} = \frac{(\Delta I_L^-) \times L1}{V_O}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta I_L^+) \times L1}{(V_{IN} - V_Q)} + \frac{(\Delta I_L^-) \times L1}{V_O}$$

$$= \frac{0.4 I_O L1}{(V_{IN} - V_O)} + \frac{0.4 I_O L1}{V_O}$$

Since $\Delta I_L^+ = \Delta I_L^- = 0.4 I_O$

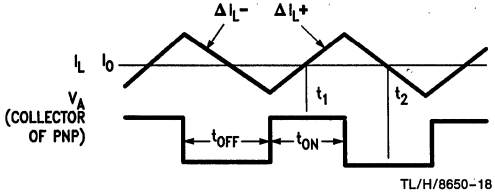

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FIGURE 14

Solving the above for L1

$$\boxed{L1 = \frac{2.5\, V_O (V_{IN} - V_O)}{I_O V_{IN} f}}$$

where: L1 is in Henrys

f is switching frequency in Hz

Also, see LM1578 data sheet for graphical methods of inductor selection.

CALCULATING OUTPUT FILTER CAPACITOR C_O:

Figure 14 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times. This curent must flow to the load and C_O. C_O's current will then be the difference between I_L, and I_O.

$$Ic_O = I_L - I_O$$

From *Figure 14* it can be seen that current will be flowing into C_O for the second half of t_{ON} through the first half of t_{OFF}, or a time, $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta I_L/4$. The resulting ΔV_C or ΔV_O is described by:

$$\Delta V_{op\text{-}p} = \frac{1}{C} \times \frac{\Delta I_L}{4} \times \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta I_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

Since $\Delta I_L = \frac{V_O(T - t_{ON})}{L1}$ and $t_{ON} = \frac{V_O T}{V_{IN}}$

$$\Delta V_{op\text{-}p} = \frac{V_O\left(T - \frac{V_O T}{V_{IN}}\right)}{4C\, L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_O)\, V_O T^2}{8 V_{IN} C_O L1} \text{ or}$$

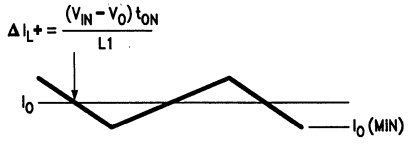
$$\boxed{C_O = \frac{(V_{IN} - V_O)\, V_O\, T^2}{8 \Delta V_O V_{IN} L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$

ΔV_O is p-p output ripple

For best regulation, the inductor's current cannot be allowed to fall to zero. Some minimum load current I_O, and thus inductor current, is required as shown below:

$$I_{O(MIN)} = \frac{(V_{IN} - V_O)\, t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_O)\, V_O}{2 f V_{IN} L1}}$$



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Typical Applications (Continued)

A complete step-down switching regulator schematic, using the LM3524D, is illustrated in *Figure 15*. Transistors Q1 and Q2 have been added to boost the output to 1A. The 5V regulator of the LM3524D has been divided in half to bias the error amplifier's non-inverting input to within its common-mode range. Since each output transistor is on for half the period, actually 45%, they have been paralleled to allow longer possible duty cycle, up to 90%. This makes a lower possible input voltage. The output voltage is set by:

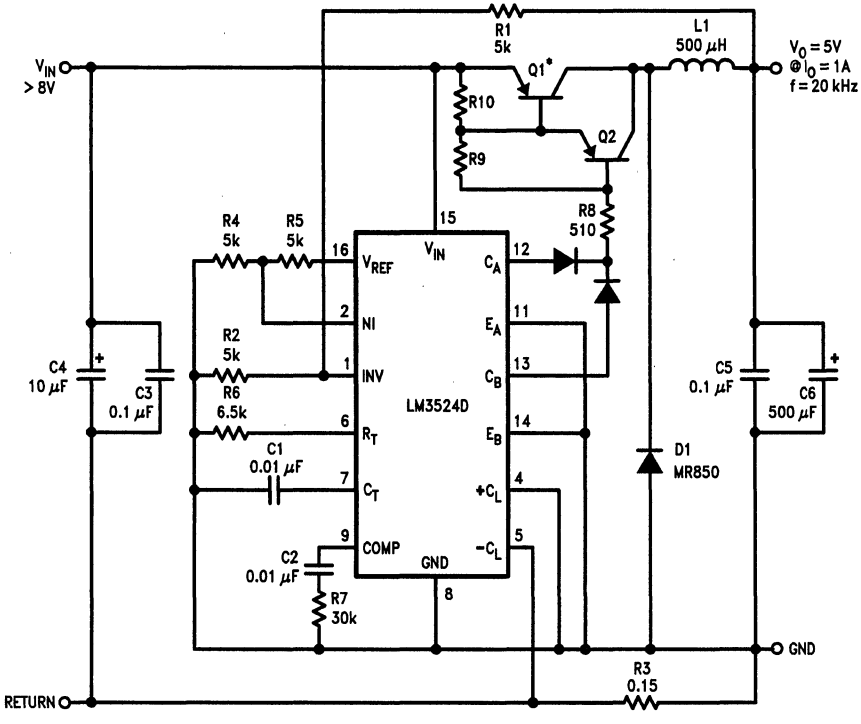
$$V_o = V_{NI}\left(1 + \frac{R1}{R2}\right),$$

where V_{NI} is the voltage at the error amplifier's non-inverting input.

Resistor R3 sets the current limit to:

$$\frac{200\ mV}{R3} = \frac{200\ mV}{0.15} = 1.3A.$$

Figure 16 and *17* show a PC board layout and stuffing diagram for the 5V, 1A regulator of *Figure 15*. The regulator's performance is listed in Table I.



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*Mounted to Staver Heatsink No. V5-1.

Q1 = BD344

Q2 = 2N5023

L1 = >40 turns No. 22 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 15. 5V, 1 Amp Step-Down Switching Regulator

Typical Applications (Continued)

TABLE I

Parameter	Conditions	Typical Characteristics
Output Voltage	V_{IN} = 10V, I_o = 1A	5V
Switching Frequency	V_{IN} = 10V, I_o = 1A	20 kHz
Short Circuit Current Limit	V_{IN} = 10V	1.3A
Load Regulation	V_{IN} = 10V I_o = 0.2 − 1A	3 mV
Line Regulation	ΔV_{IN} = 10 − 20V, f_o = 1A	6 mV
Efficiency	V_{IN} = 10V, I_o = 1A	80%
Output Ripple	V_{IN} = 10V, I_o = 1A	10 mVp-p

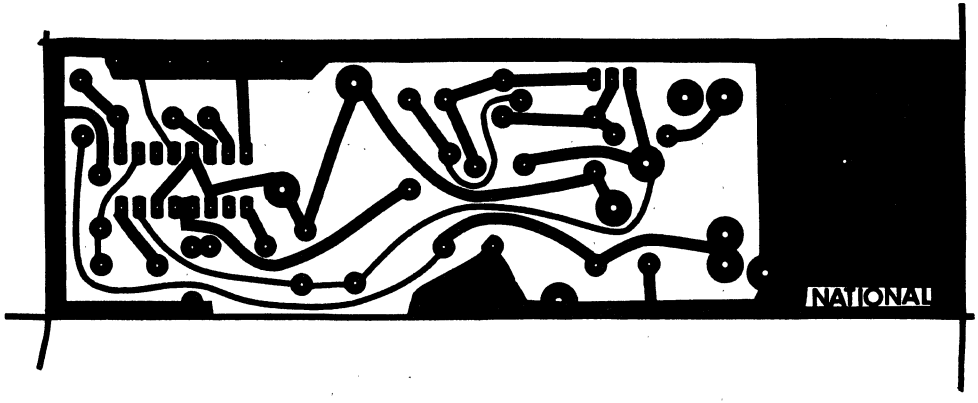

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FIGURE 16. 5V, 1 Amp Switching Regulator, Foil Side

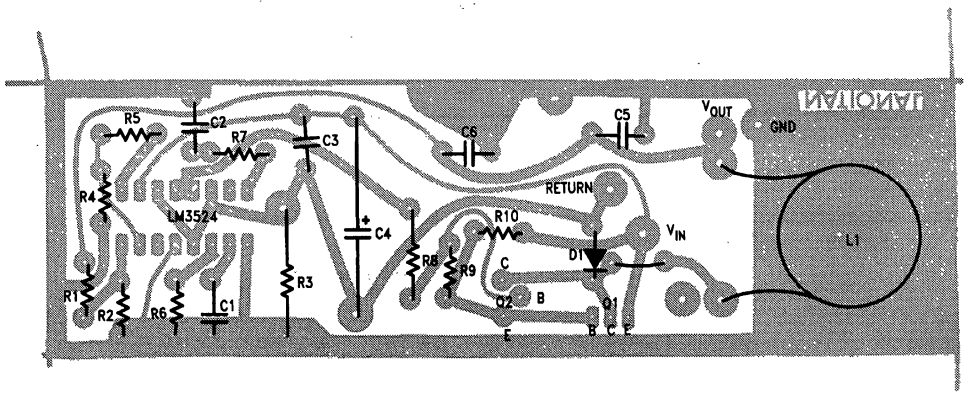

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FIGURE 17. Stuffing Diagram, Component Side

Typical Applications (Continued)

THE STEP-UP SWITCHING REGULATOR

Figure 18 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}, Q1 is ON and energy is drawn from V_{IN} and stored in L1; D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens, t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1, D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here also, as in the step-down regulator, the current through L1 has a DC component plus some ΔI_L. ΔI_L is again selected to be approximately 40% of I_L. *Figure 19* shows the inductor's current in relation to Q1's ON and OFF times.

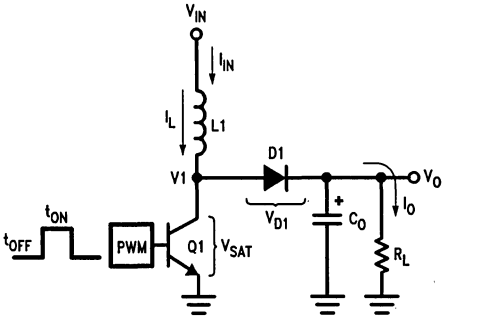

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FIGURE 18. Basic Step-Up Switching Regulator

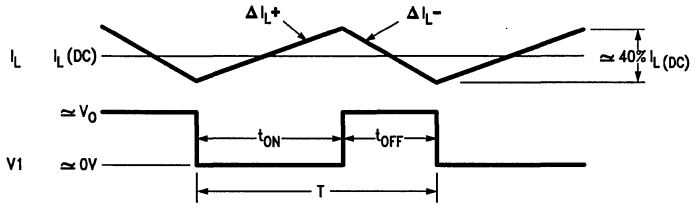

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FIGURE 19

Typical Applications (Continued)

From $\Delta I_L = \frac{V_L T}{L}$, $\Delta I_L{}^+ \cong \frac{V_{IN} t_{ON}}{L1}$

and $\Delta I_L{}^- \cong \frac{(V_o - V_{IN})\, t_{OFF}}{L1}$

Since $\Delta I_L{}^+ = \Delta I_L{}^-$, $V_{IN} t_{ON} = V_o t_{OFF} - V_{IN} t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \cong V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)}\, V_{IN}$$

$$P_{OUT} = I_o V_o = I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

for $\eta = 100\%$, $P_{OUT} = P_{IN}$

$$I_o\, V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\, V_{IN}$$

$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)}$$

So far it is assumed $\eta = 100\%$, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1} = 1V$ this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\Delta_{MAX} = \frac{P_o}{P_{IN}} = \frac{V_o I_o}{V_o I_o + I_{IN}(1V)} = \frac{V_o I_o}{V_o I_o + I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

From $V_o = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}}$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_o t_{ON}}{C_o} \text{ or } C_o = \frac{I_o t_{ON}}{\Delta V_o}$$

From $V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right)$; $t_{OFF} = \frac{V_{IN}}{V_o} T$

where $T = t_{ON} + t_{OFF} = \frac{1}{f}$

$$t_{ON} = T - \frac{V_{IN}}{V_o} T = T\left(\frac{V_o - V_{IN}}{V_o}\right) \text{ therefore:}$$

$$C_o = \frac{I_o T\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o\,(V_o - V_{IN})}{f \Delta V_o V_o}}$$

where: C_o is in farads, f is the switching frequency,
ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$$L1 = \frac{V_{IN} t_{ON}}{\Delta I_L{}^+}, \text{ since during } t_{ON},$$

V_{IN} is applied across L1

$$\Delta I_{Lp\text{-}p} = 0.4\, I_L = 0.41\, I_{IN} = 0.4\, I_o\left(\frac{V_o}{V_{IN}}\right), \text{ therefore:}$$

$$L1 = \frac{V_{IN} t_{ON}}{0.4\, I_o\left(\frac{V_o}{V_{IN}}\right)} \text{ and since } t_{ON} = \frac{T\,(V_o - V_{IN})}{V_o}$$

$$\boxed{L1 = \frac{2.5\, V_{IN}{}^2\,(V_o - V_{IN})}{f\, I_o V_o{}^2}}$$

where: L1 is in henrys, f is the switching frequency in Hz

Typical Applications (Continued)

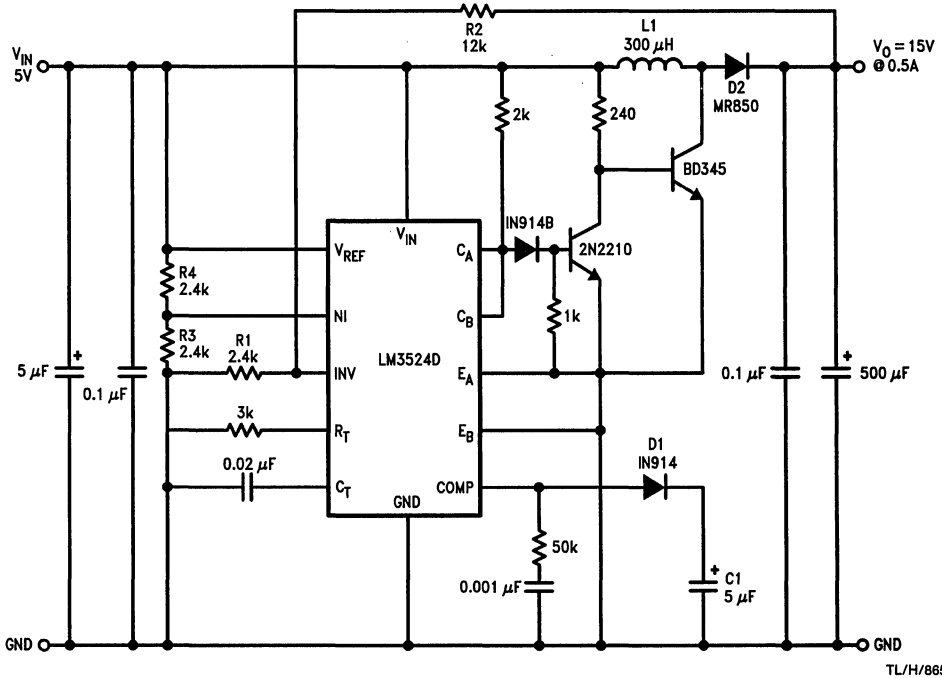
To apply the above theory, a complete step-up switching regulator is shown in *Figure 20*. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \times V_{INV} = 2.5 \times \left(1 + \frac{R2}{R1}\right)$$

The network D1, C1 forms a slow start circuit.

This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from 0V. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see *Figure 21*, the input voltage variations are rejected.

The LM3524D can also be used in inductorless switching regulators. *Figure 22* shows a polarity inverter which if connected to *Figure 20* provides a −15V unregulated output.



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L1 = > 25 turns No. 24 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 20. 15V, 0.5A Step-Up Switching Regulator

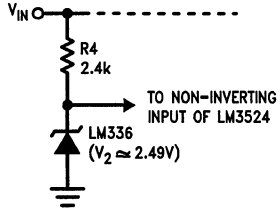

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FIGURE 21

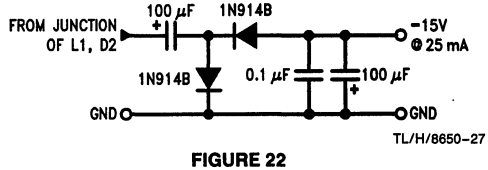

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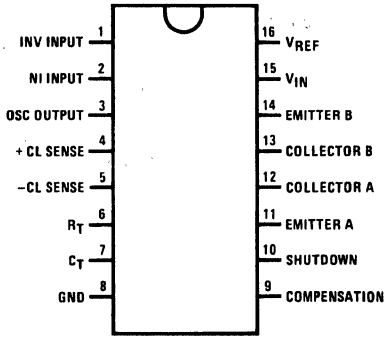
FIGURE 22

Connection Diagram



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Top View

**Order Number LM1524DJ,
LM2524DN or LM3524DN
See NS Package Number J16A and N16A**

National Semiconductor

LM1525A/LM3525A/LM1527A/LM3527A Pulse Width Modulator

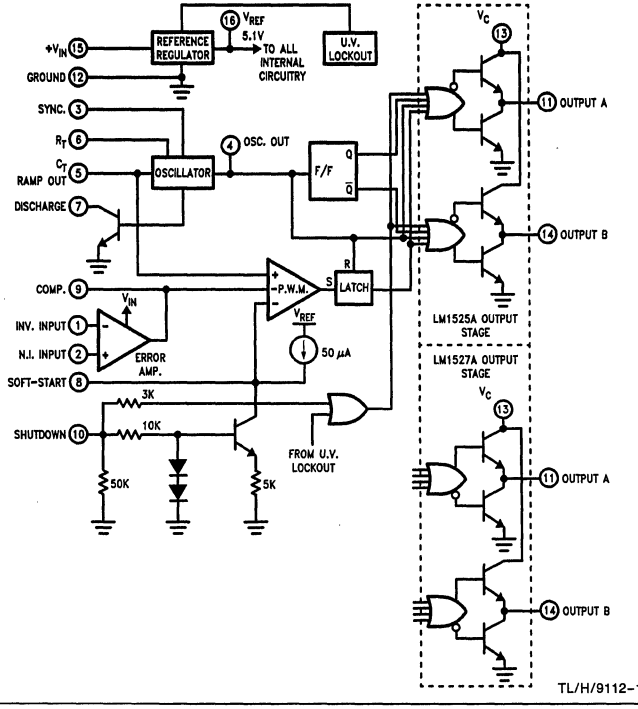
General Description

The LM1525A/1527A series of pulse-width-modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% initial accuracy, and the input common mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and dividers. A Sync input to the oscillator permits multiple devices to be slaved together, or a single device to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides a wide range of deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. The undervoltage lockout circuitry features approximately 200 mV of hysteresis to prevent threshold oscillations. Another unique feature of these improved PWM integrated circuits is the latch following the comparator (thus preventing double-pulsing). Once a PWM pulse has been terminated for any reason, the outputs will remain OFF for the duration of that period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking more than 200 mA. The LM1525A output stage features NOR logic, resulting in LOW outputs for an OFF stage. The LM1527A uses OR logic which results in HIGH outputs when OFF.

Features

- 8 to 35V operation
- 5.1V reference trimmed to ±1%
- 100 Hz to 500 kHz oscillator range
- Separate oscillator sync terminal
- Adjustable deadtime control
- Internal soft-start
- Input undervoltage lockout with hysteresis
- Latching P.W.M. to prevent multiple pulses
- Dual source/sink output drivers

Block & Connection Diagrams



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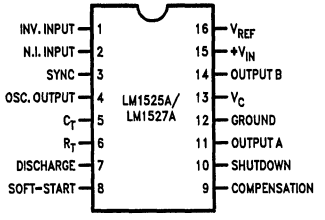


TL/H/9112-2

Top View

Order Number LM1525AJ, LM3525AJ, LM1527AJ, LM3527AJ, LM3525AN or LM3527AN
See NS Package Number J16A or N16A

2

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (Pins 13, and 15)	−0.3V to +40V
Reference Output Current (Pin 16)	50 mA DC
Reference Output Short Circuit	5 Seconds
Output Current (Pins 11, 14)	±200 mA
Oscillator Current (Pins 5, 6, 7) (Note 8)	5 mA DC
Op Amp Inputs: V_{CM} (Pins 1, 2) V_{DIFF}	−0.3V to $+V_{in}$ ±6V
Logic Inputs	−0.3V to +5.5V
Storage Temperature	−65°C to +150°C
Operating Temperature Range ($T_{min} \le T_j \le T_{max}$)	
LM1525A, LM1527A	−55°C to +150°C
LM3525A, LM3527A	0°C to +150°C
Lead Temperature (Soldering, 4 Seconds)	
J Package	+300°C
N Package	+260°C
Power Dissipation (Note 9)	1 Watt
ESD Tolerance	
Czap = 100 pF, Rzap = 1.5k	2000V

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
REFERENCE SECTION								
Reference Voltage Output	T_j = 25°C	5.10	5.05 5.15		5.10	5.00 5.20		V_{min} V_{max}
Line Regulation	$+8.0V \le V_{in} \le +35V$	10	**20**		10	15	**20**	mV_{max}
Load Regulation	$0\ mA \le I_L \le 20\ mA$	20	**50**		20	20	**50**	mV_{max}
Temperature Stability		20		**50**	20		**50**	mV_{max}
Reference Voltage Output	$+8.0V \le V_{in} \le +35V$ $0\ mA \le I_L \le 20\ mA$ And Over Operating Temp.	5.08	**5.20** **5.00**		5.08		**5.25** **4.95**	V_{max} V_{min}
Short Circuit Current	T_j = 25°C V_{ref} = 0V	70	100		70	100		mA_{max}
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz T_j = 25°C	40		200	40		200	μV_{rms} max
Long Term Stability	T_j = 125°C	20		50	20		50	mV/KHour
OSCILLATOR SECTION (Note 4) Unless otherwise specified								
Initial Accuracy	T_j = 25°C	±2	±6		±2	±6		%
Accuracy of Freq. vs. Temp.		±3	**±8**		±3		**±10**	%
Voltage Stability	$8.0V \le V_{in} \le 35V$	±0.3	**±1**		±0.3	±2	**±2**	%
Temperature Stability	$\Delta F_{osc}/F_{osc}$	±3		**±6**	±3		**±6**	%
Minimum Frequency	R_T = 300 kΩ, C_T = 0.1 μF, R_D = 0 (Note 5)	70	**100**		70	90	**100**	Hz max
Maximum Frequency	R_T = 2.0 kΩ, C_T = 1 nF, R_D = 0	450	**400**		450	430	**400**	kHz min
Current Mirror $I_{pin\ 5}$	I_{RT} = 2.0 mA	2.0	**1.7** **2.2**		2.0	1.8 2.1	**1.7** **2.2**	mA_{min} mA_{max}
Clock Amplitude	At pin 4	3.5		**3.0**	3.5		**3.0**	V_{min}
Clock Width	T_j = 25°C	0.5		1.0 0.3	0.5		1.0 0.3	μs max μs min
Sync Threshold	(Note 6)	1.8	**1.2** **2.8**		1.8	1.25 2.8	**1.2** **2.8**	V min V max
Sync Input Current	Sync Voltage = 3.5V	1.0	**2.5**		1.0	2.30	**2.5**	mA_{max}

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
ERROR AMPLIFIER SECTION V_{CM} = 5.1V, Unless otherwise noted								
Input Offset Voltage		0.5	**5**		2	7	**10**	mV_{max}
Input Bias Current		1	**10**		1	2	**10**	μA_{max}
Input Offset Current		0.1	**1**		0.1	0.8	**1**	μA_{max}
DC Open Loop Gain	$R_L \geq 10\ M\Omega$	80	**66**		80	66	**60**	dB min
Gain Bandwidth Product	A_V = 0, T_j = 25°C $C_L \leq 30$ pF	2		1	2		1	MHz_{min}
Output Low Level		0.2	**0.5**		0.2	0.4	**0.5**	V_{max}
Output High Level		5.6	**3.8**		5.6	4.1	**3.8**	V_{min}
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	80	**66**		80	70	**66**	dB min
Supply Voltage Rejection	V_{IN} = 8V to 35V	90	**60**		90	64	**60**	dB min
P.W.M. COMPARATOR								
Minimum Duty Cycle			**0**			0	**0**	% max
Maximum Duty Cycle		49	**45**		49	46	**45**	% min
Input Threshold	Zero Duty Cycle	0.9	**0.6**		0.9	0.70	**0.6**	V_{min}
Input Threshold	Max. Duty Cycle	3.3	**3.6**		3.3	3.6	**3.6**	V_{max}
Input Bias Current		0.05		**1.0**	0.05		**1.0**	μA_{max}
SOFT-START SECTION								
Soft Start Current	$V_{SHUTDOWN}$ = 0V	50	**80** **25**		50	74 36	**80** **25**	μA_{max} μA_{min}
Soft Start Voltage	$V_{SHUTDOWN}$ = 2.0V	0.35	**0.6**		0.35	0.5	**0.6**	V_{max}
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V	0.4	**1.0**		0.4	0.85	**1.0**	mA_{max}
OUTPUT DRIVERS (Each Output) V_C = 20V, Unless otherwise noted								
Undervoltage Lockout Hysteresis		0.2			0.2			V
Output Low Level	I_{SINK} = 20 mA	0.2	**0.4**		0.2	0.35	**0.4**	V_{max}
	I_{SINK} = 100 mA	1.0	**2.0**		1.0	1.9	**2.0**	V_{max}
Output High Level	I_{SOURCE} = 20 mA	19	**18**		19	18.2	**18**	V_{min}
	I_{SOURCE} = 100 mA	18	**17**		18	17.4	**17**	V_{min}
Undervoltage Lockout	V_{COMP} and V_{SS} = High	7	**8** **6**		7	7.7 6.3	**8** **6**	V_{max} V_{min}
Collector Leakage	LM1525A and LM3525A Only V_C = 35V		**200**			120	**200**	μA_{max}
Rise Time	C_L = 1 nf, T_j = 25°C	100		600	100		600	ns max
Fall Time	C_L = 1 nf, T_j = 25°C	50		300	50		300	ns max

Electrical Characteristics

V_{in} = 20 V_{dc}, **Boldface** limits apply from T_{MIN} to T_{MAX} (Note 1), all other limits T_j = 25°C unless otherwise noted (Continued)

Parameter	Conditions	LM1525A LM1527A			LM3525A LM3527A			Units
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
Shutdown Delay	V_{SD} = 3V, C_L = 0, T_j = 25°C	200		500	200		500	ns max
TOTAL STANDBY CURRENT								
Supply Current	V_{IN} = 35V	13	**18**		13	14.5	**20**	mA

Note 1: Unless otherwise noted these specifications apply: −55°C < T_j < +125°C for LM1525A and LM1527A, 0°C < T_j < +125°C for LM3525A and LM3527A.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply ranges.

Note 4: Tested at F_{osc} = 40 kHz (Rt = 3.6k, Ct = 0.01 μF, Rd = 0).

Note 5: These specifications are also guaranteed with Rt = 150k, Ct = 0.2 μF, Rd = 0.

Note 6: Tested with a pulse of width 500 ns and amplitudes of 1.2 and 2.8V at 50 kHz.

Note 7: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1 and conditions.

Note 8: Do not ground pin 6.

Note 9: For operation at elevated temperatures, devices in the J package must be derated based on thermal resistance of 90°C/W (junction to ambient), or 85°C/W in the N package.

SHUTDOWN OPTIONS (See Block Diagram)

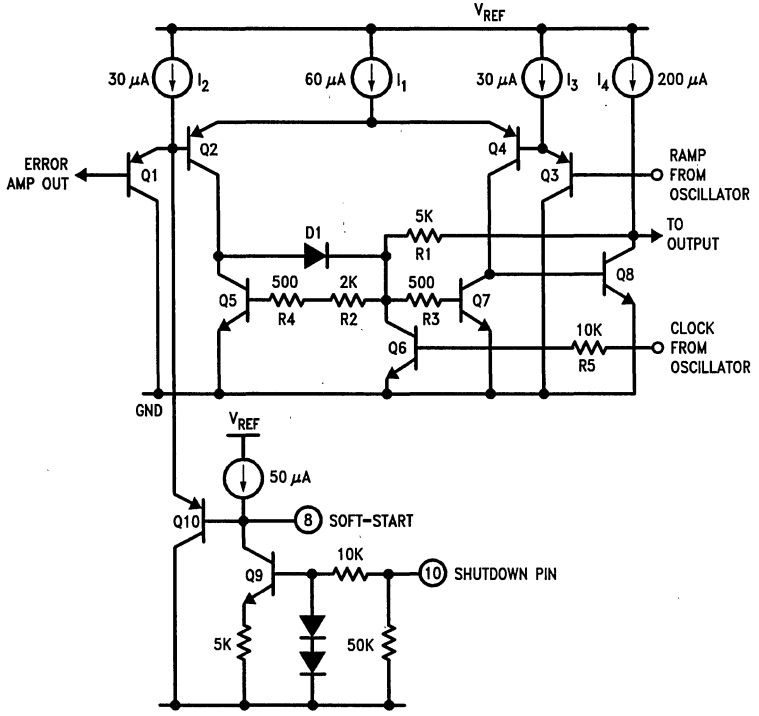
1. Since both the compensation and soft-start terminals (pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.
2. An alternative approach is the use of the shutdown circuitry of pin 10. Activating this circuit by applying a positive-going pulse at pin 10 will result in the output of the comparator going high, and thus turning off the outputs. The pulse will start the fast discharge of the soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding pin 10 high for a long time will ultimately discharge the soft-start capacitor, thus recycling slow turn on upon release. This method of shutdown is the fastest shutdown possible.

SYNCHRONIZATION PROCEDURE

The device may be synchronized to an external clock; however the following points have to be observed: a) The frequency of the free-running oscillator of the device must be set at least 10% less than the frequency of the external clock. b) The external clock pulse must be at least 300 ns wide but must not exceed the free-running pulse width (pin 4) by more than 200 ns. c) The amplitude of the external pulse must be between 2 and 5V.

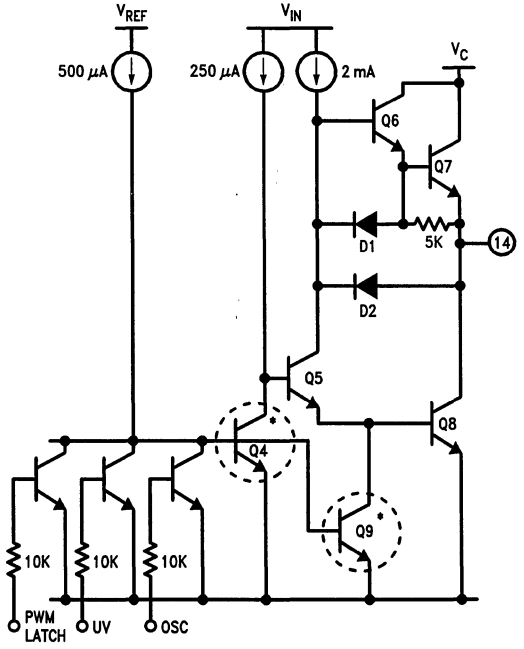
Multiple devices may be synchronized together by connecting all pin 4's together and all pin 5's together; pins 6 and 7 of slave oscillator must be left open.

LM1525A Comparator



TL/H/9112-3

LM1525A Output Section



*Q_4 omitted in LM1527A.
Q_9 replaced by a 2K resistor in LM1527A.

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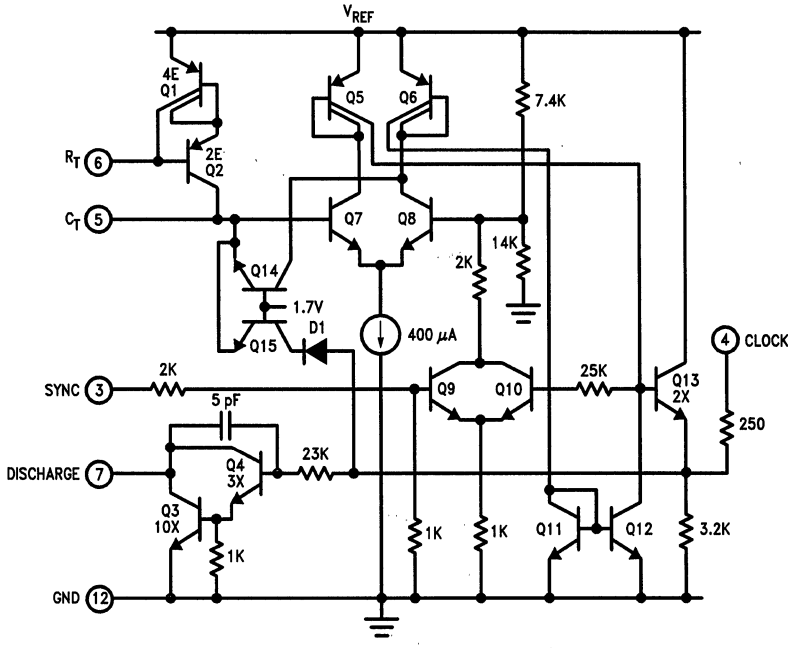
LM1525A Oscillator



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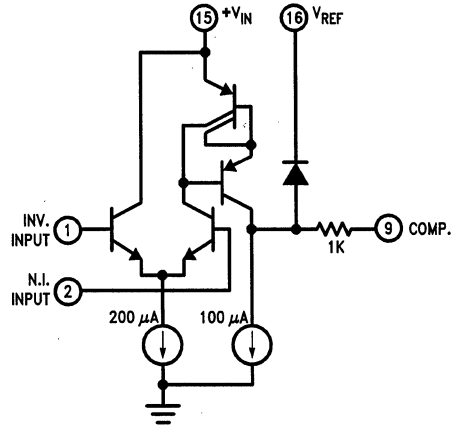
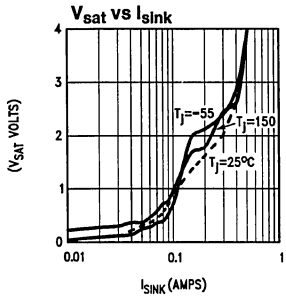
LM1525A Error Amplifier

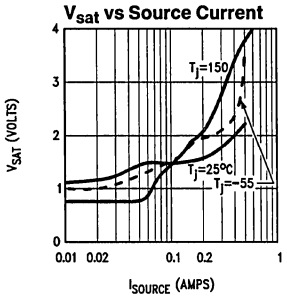


TL/H/9112–4

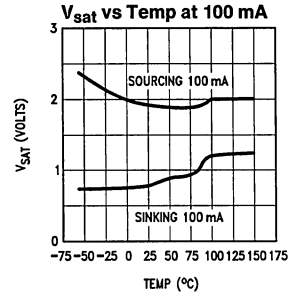
V_{sat} vs I_{sink}



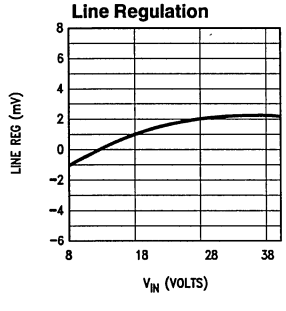
V_{sat} vs Source Current



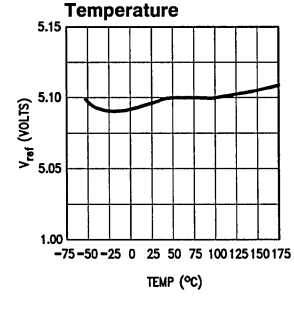
V_{sat} vs Temp at 100 mA



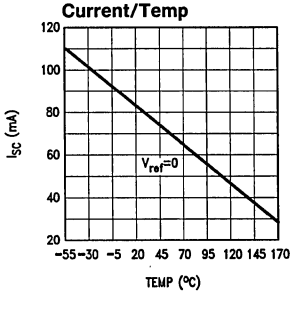
Line Regulation



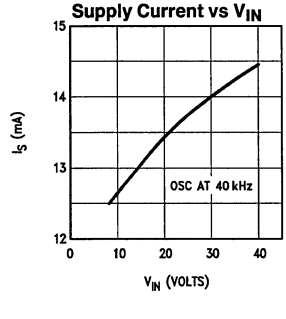
Typical V_{ref} vs Temperature



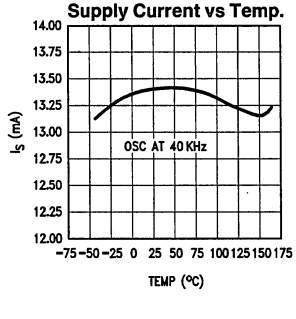
V_{ref} Short-Circuit Current/Temp



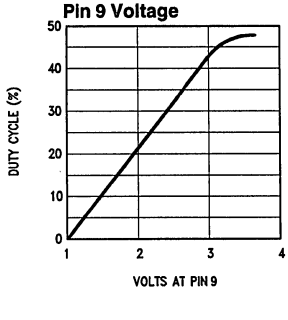
Supply Current vs V_{IN}



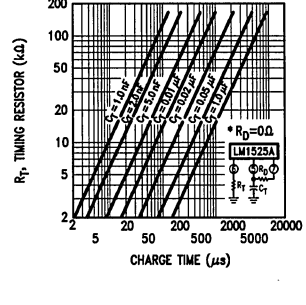
Supply Current vs Temp.



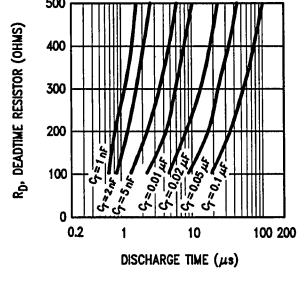
Duty Cycle vs Pin 9 Voltage



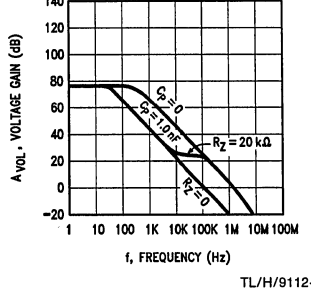
Oscillator Charge Time vs R_T



Oscillator Discharge Time vs R_D and C_T



Error Amplifier Open-Loop Frequency Response



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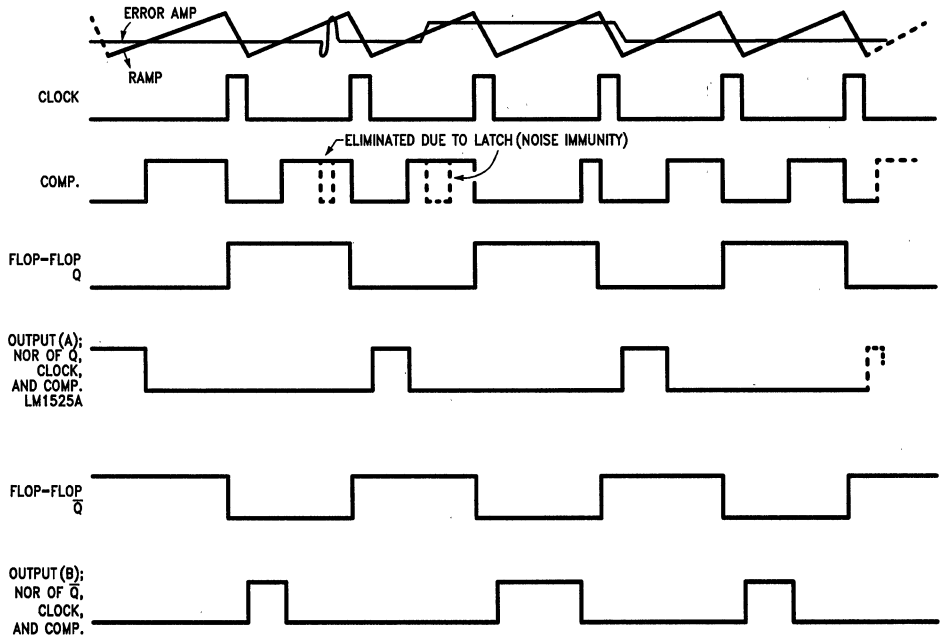
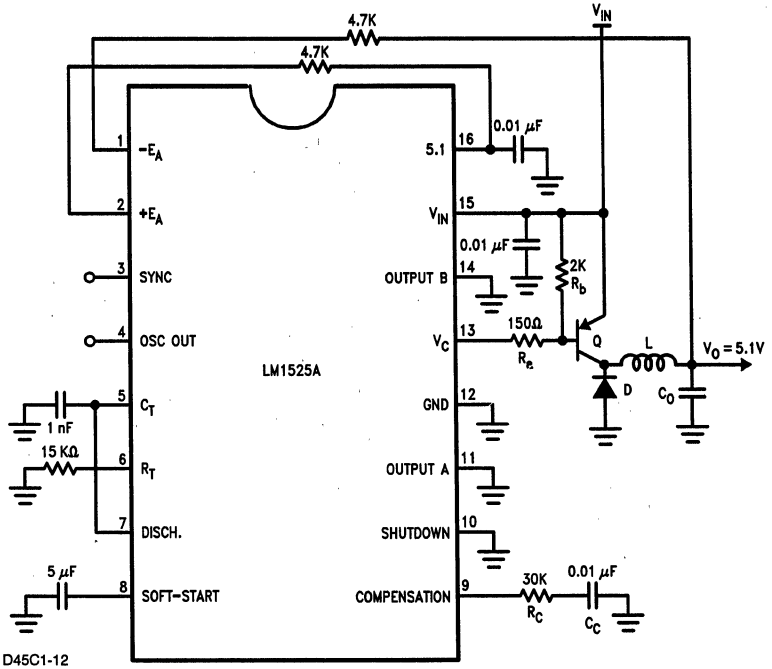
LM1525A Typical Timing Diagram



TL/H/9112-7

Typical Applications

5 Watt Single Ended Step Down Converter

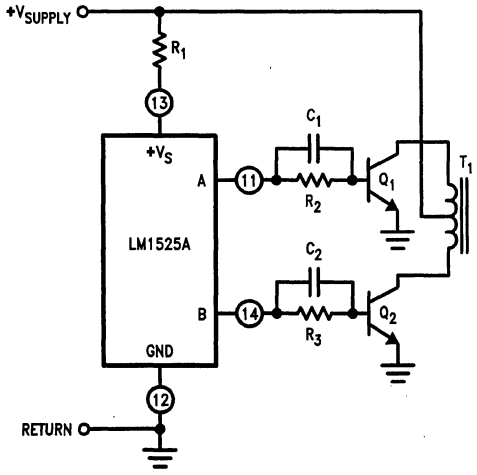


TL/H/9112-8

V_{IN} = 28V Q = D45C1-12
V_{OUT} = 5.1V D = IN5821
L = 150 μH
C_O = 500 μF

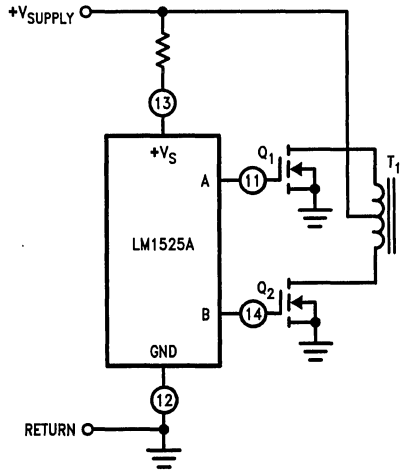
Typical Applications (Continued)

Bipolar Drive for Push-Pull Converters



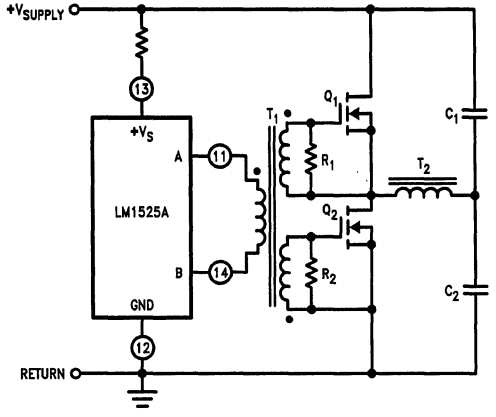
TL/H/9112–9

3 MOSFET Drive for Push-Pull Converters



TL/H/9112–10

Direct Drive for Transformer



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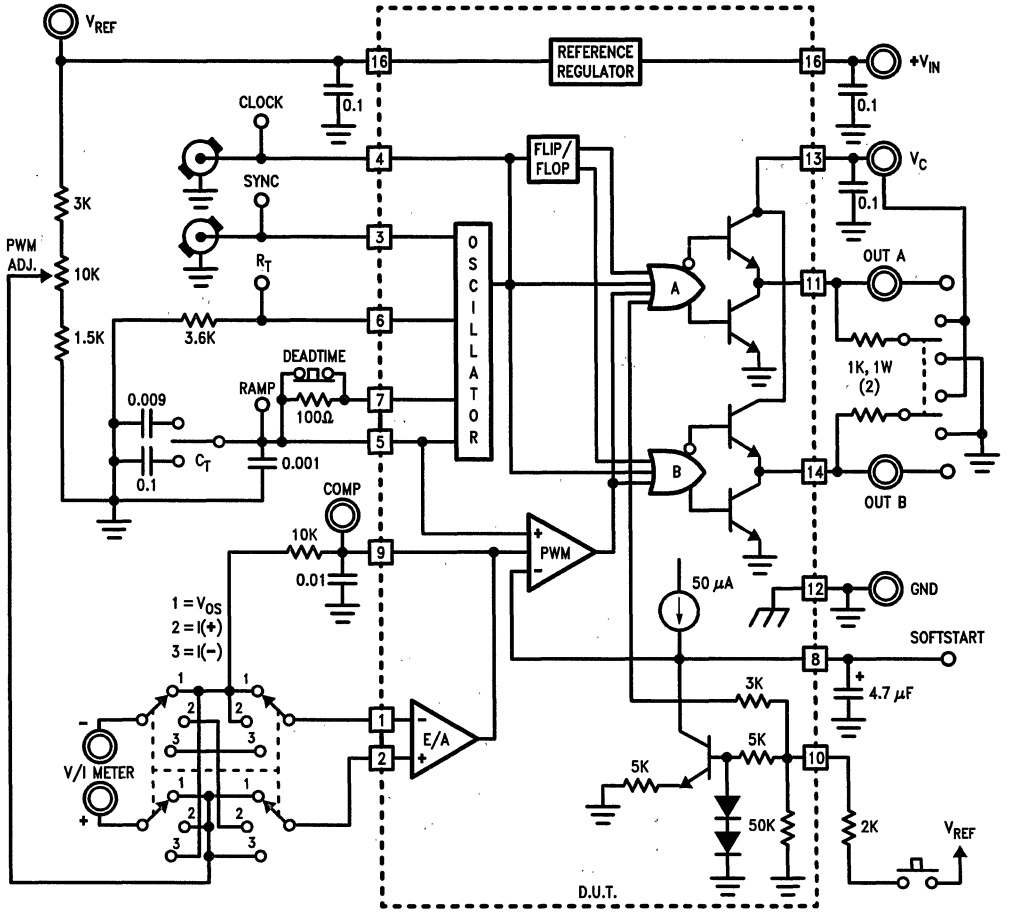
2

Typical Applications (Continued)

LM1525A/1527A Lab Test Fixture



TL/H/9112–12

National Semiconductor

LM1575-5.0/LM2575-5.0
Simple Switcher Step-Down Voltage Regulator

General Description

The LM1575/LM2575 are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator. These devices feature a 5V output capable of driving a 1A load with excellent line and load regulation.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM1575/2575 offers a high efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors are available from several different manufacturers optimized for use with the LM1575/LM2575. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±3% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring less than 200 μA standby current. The output switch includes current limiting, as well as thermal shutdown for full protection under fault conditions.

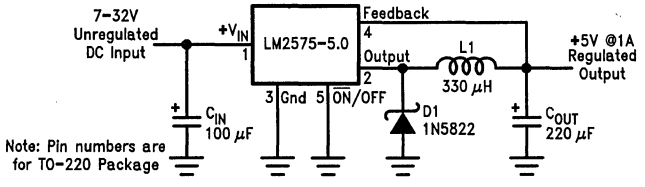
Features

- 5V output, ±3% Max over line and load conditions
- Guaranteed 1A output current
- Wide input voltage range, 7V to 35V
- Requires only 4 external components
- 52 kHz fixed frequency internal oscillator
- Low power standby mode, I_Q typically <200 μA
- 82% efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators

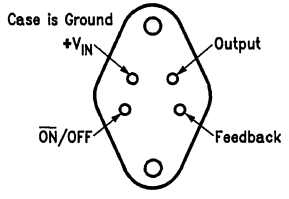
Typical Application



TL/H/10527–1

Connection Diagram and Order Information

4-Lead TO-3 (K)

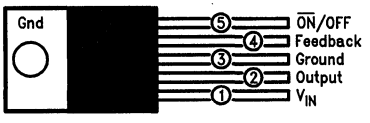


TL/H/10527–2

Bottom View

Order Number LM1575K-5.0, LM2575K-5.0
See NS Package Number K04A

5-Lead TO-220 (T)



TL/H/10527–3

Top View

Order Number LM2575T-5.0
See NS Package Number T05A

For information about LM2575 in dual-in-line or surface-mount packages, contact the factory.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (see *Figure 5*)	40V
$\overline{ON}$/OFF Pin Input Voltage	$-1 \le V \le 15V$
Output Voltage to Ground (Steady State)	$-1V$
Power Dissipation	Internally Limited
Storage Temperature Range	$-65°C$ to $+150°C$
Minimum ESD Rating ($C = 100$ pF, $R = 1.5$ kΩ)	2 kV
Lead Temperature (Soldering, 10 sec.)	260°C
Maximum Junction Temperature	150°C
Operating Temperature Range	
LM1575-5.0	$-55°C \le T_J \le +150°C$
LM2575-5.0	$-40°C \le T_J \le +125°C$

Electrical Characteristics

Specifications with standard type face are for $T_J = 25°C$, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, $V_{IN} = 12V$, and $I_{LOAD} = 200$ mA.

Symbol	Parameter	Conditions	Typ	LM1575-5.0 Limit (Note 2)	LM2575-5.0 Limit (Note 3)	Units (Limits)
SYSTEM PARAMETERS (Note 4) Test Circuit *Figure 1*						
V_{OUT}	Output Voltage	$V_{IN} = 12V$, $I_{LOAD} = 0.2A$	5.0			V
				4.950	4.900	V (Min)
				5.050	5.100	V (Max)
V_{OUT}	Output Voltage	$0.2A \le I_{LOAD} \le 1A$, $8V \le V_{IN} \le 35V$	5.0			V
				4.850/**4.800**	4.800/**4.750**	V (Min)
				5.150/**5.200**	5.200/**5.250**	V (Max)
η	Efficiency	$V_{IN} = 12V$, $I_{LOAD} = 1A$, $V_{OUT} = 5V$	82			%
DEVICE PARAMETERS						
f_O	Oscillator Frequency		52			kHz
				47/**43**	47/**42**	kHz (Min)
				58/**62**	58/**63**	kHz (Max)
V_{SAT}	Saturation Voltage	$I_{OUT} = 1A$ (Note 5)	0.9			V
				1.2/**1.4**	1.2/**1.4**	V (Max)
DC	Max Duty Cycle (ON)	(Note 6)	98			%
				93	93	% (Min)
I_{CL}	Current Limit	Peak Current, $t_{ON} \le 3$ μs (Note 5)	2.2			A
				1.7/**1.3**	1.7/**1.3**	A (Min)
				3.0/**3.2**	3.0/**3.2**	A (Max)
I_L	Output Leakage Current	$V_{IN} = 35V$, (Note 7), Output = 0V		2	2	mA (Max)
		Output = $-1V$	7.5			mA
				30	30	mA (Max)
I_Q	Quiescent Current	(Note 7)	5			mA
				10/**12**	10	mA (Max)
I_{STBY}	Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF)	50			μA
				200/**500**	200	μA (Max)
θ_{JA}	Thermal Resistance	K Package, Junction to Ambient	35			°C/W
θ_{JC}		K Package, Junction to Case	1.5			
θ_{JA}		T Package, Junction to Ambient	40			
θ_{JC}		T Package, Junction to Case	2			
ON/OFF CONTROL Test Circuit *Figure 1*						
V_{IH}	$\overline{ON}$/OFF Pin Threshold Voltage	$V_{OUT} = 5V$	1.4	22/**2.4**	2.2/**2.4**	V (Min)
V_{IL}		$V_{OUT} = 0V$	1.2	1.0/**0.8**	1.0/**0.8**	V (Max)
I_{IH}	$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF)	12			μA
				30	30	μA (Max)
I_{IL}		$\overline{ON}$/OFF Pin = 0V (ON)	0			μA
				10	10	μA (Max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All limits are used to calculate Average Outgoing Quality Level, and all are 100% production tested.

Note 3: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All room temperature limits are 100% production tested. All limits at **temperature extremes** are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 4: External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM1575/LM2575 is used as shown in the *Figure 1* test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.

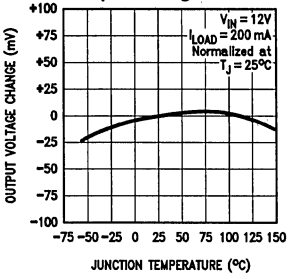
Note 5: Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.

Note 6: Feedback (pin 4) removed from output and connected to 0V.

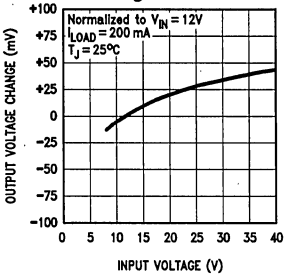
Note 7: Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.

Typical Performance Characteristics (Circuit of *Figure 1*)

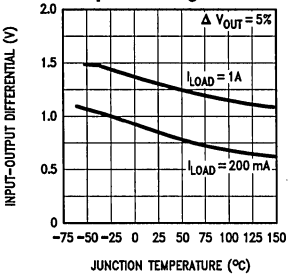
Normalized Output Voltage



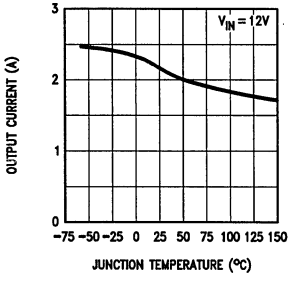
Line Regulation



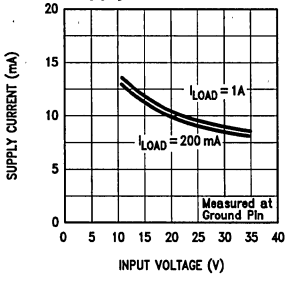
Dropout Voltage



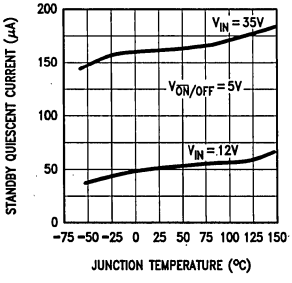
Current Limit



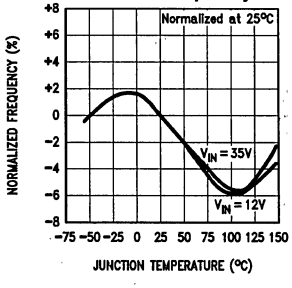
Supply Current



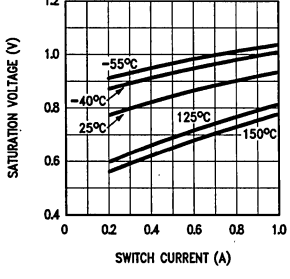
Standby Quiescent Current



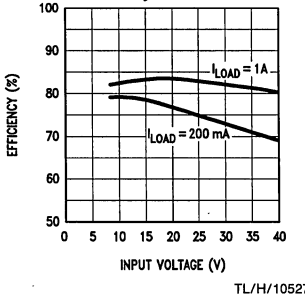
Oscillator Frequency



Switch Saturation Voltage



Efficiency



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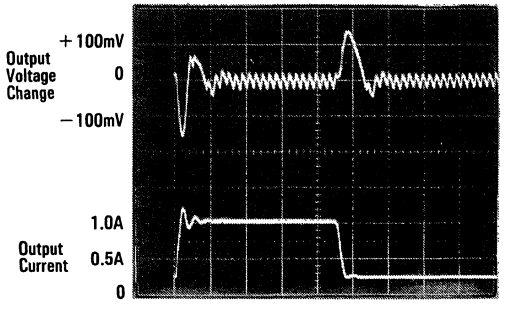
Typical Performance Characteristics (Continued)

Load Transient Response



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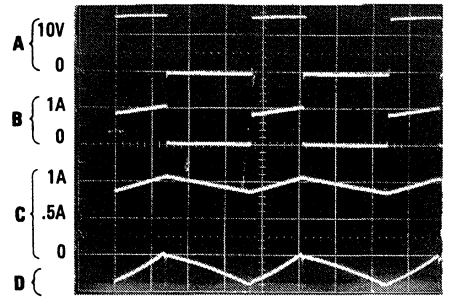
Switching Waveforms



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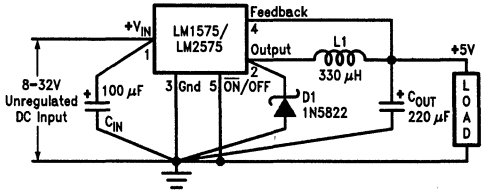
A: Output pin voltage, 10V/div
B: Output pin current, 1A/div
C: Inductor current, 0.5A/div
D: Output ripple voltage, 20 mV/div, AC-coupled
Horizontal: 5 μsec/div

Test Circuit and Layout Guidelines



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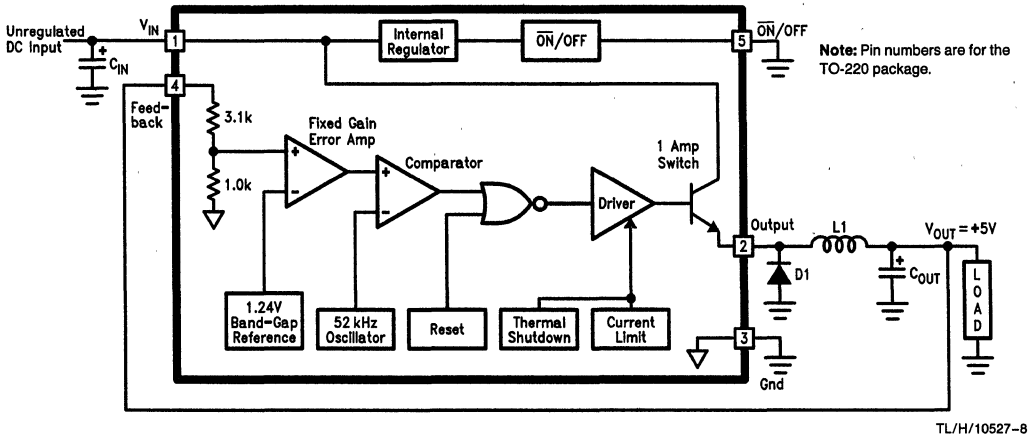
Note: Pin numbers are for the TO-220 package.

C_{IN} — 509DRSA107M050S (Sprague)
C_{OUT} — 509DRSA227M010S (Sprague)
D1 — any manufacturer
*for $V_{IN} \leq 35V$, D1 should be 31DQ05 or MBR350.
L1 — 415-0926 (AIE) for $I_{LOAD} \leq 0.9A$, 430-0635 (AIE) for $I_{LOAD} \leq 1.0A$
5-pin TO-220 socket—2396 (Loranger Mfg. Co.)
4-pin TO-3 socket—8112-AG7 (Augat Inc.)

FIGURE 1

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be **kept** as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

Block Diagram and Typical Application



Note: Pin numbers are for the TO-220 package.

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FIGURE 2

LM1575/LM2575 Design Procedure

Procedure	Example
Given: V_{IN} (Max) = Maximum input voltage I_{LOAD} (Max) = Maximum load current	**Given:** V_{IN} (Max) = 18V I_{LOAD} (Max) = 0.8A
1. Inductor Selection (L1) A. From *Figure 3*, identify inductor code for region indicated by V_{IN} (Max) and I_{LOAD} (Max). B. From *Figure 4*, identify inductor value from the inductor code. C. Select from the three manufacturer's part numbers listed in *Figure 4*. Alternately, another inductor of the appropriate value may be used. It must be rated for operation at the LM2575 switching frequency (typically 52 kHz), and for a current rating of 1.25 × I_{LOAD} (Max).	**1. Inductor Selection (L1)** A. Code = L330 B. Value = 330 μH C. Choose AIE 415-0926, Pulse Engineering PE 52627, or Renco RL1952

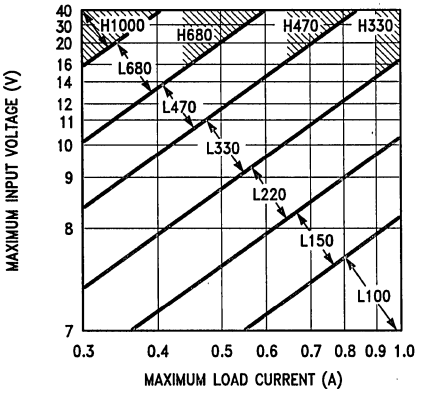

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FIGURE 3. Inductor Value Selection Guide

Inductor Code	Inductor Valve	AIE[8]	Pulse Eng.[9]	Renco[10]
L100	100 μH	415-0930	PE-92108	RL1955
L150	150 μH	415-0953	PE-53113	RL1954
L220	220 μH	415-0922	PE-52626	RL1953
L330	330 μH	415-0926	PE-52627	RL1952
L470	470 μH	415-0927	PE-53114	RL1951
L680	680 μH	415-0928	PE-52629	RL1950
H330	330 μH	430-0635	PE-53117	RL1962
H470	470 μH	430-0634	PE-53118	RL1961
H680	680 μH	415-0935	PE-53119	RL1960
H1000	1000 μH	415-0934	PE-53120	RL1959

FIGURE 4. Inductor Selection by Manufacturer's Part Number

Note 8: AIE Magnetics, Div. Vernatron Corp. Passive Components Group, (813) 347-2181
2801 72nd Street North, St. Petersburg, FL 33710

Note 9: Pulse Engineering, (619) 268-2400
P.O. Box 12235, San Diego, CA 92112

Note 10: Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

LM1575/LM2575 Design Procedure (Continued)

Procedure (Continued)	Example (Continued)
2. Output Capacitor Selection (C_{OUT}) A. The output capacitor value and the type of capacitor used will determine the amount of ripple voltage that appears as the output. A value of between 220 µF and 1000 µF is recommended. Selecting a low ESR (Equivalent Series Resistance) capacitor will result in the lowest amount of ripple. The lower capacitor values will allow typically 50 mV to 150 mV of output ripple, while larger-value capacitors will reduce the ripple to approximately 35 mV to 50 mV. To further reduce the output ripple voltage, several low-value standard capacitors may be paralleled, or a higher-grade capacitor may be used. Such capacitors are often called "high-frequency", "low-inductance", or "low-ESR". These will reduce the output ripple to 10 mV to 20 mV. However, reducing the ESR below 0.05Ω can cause instability. For this reason, the use of tantalum capacitors is not recommended. B. The capacitor's voltage rating should be at least 1.25 times greater than the output voltage. For a 5V regulator, a rating of at least 6.3V is appropriate, and a 10V rating is recommended.	**2. Output Capacitor Selection (C_{OUT})** A. C_{OUT} = 220 µF to 1000 µF standard aluminum electrolytic or C_{OUT} = 470 µF to 1000 µF high-grade capacitor (see text) B. Capacitor voltage rating = 10V
3. Catch Diode Selection (D1) The catch diode current rating must be at least 1.2 times greater than the maximum load current. Also, if the power supply design must withstand continuous shorted output conditions, the diode current rating should be greater than 3A. The most stressful condition for this diode is an overload or short circuit condition. A. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. B. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best efficiency, especially in 5V switching regulators. Fast-Recovery, High-Efficiency, or Ultra-Fast Recovery diodes are also suitable, but some types with an abrupt turn-off characteristic may cause instability and EMI problems. A fast-recovery diode with soft recovery characteristics is a better choice. *To prevent damage to the LM2575, fast-recovery diodes should not be used for $V_{IN} \geq 35V$.* Standard 60 Hz diodes (e.g., 1N4001, etc.) are also not suitable. See *Figure 5* for Schottky and "soft" fast-recovery diode selection guide.	**3. Catch Diode Selection (D1)** A. For this example, a 20V rating is adequate. B. Use the 1N5821 or 31DQ03 Schottky diodes, or any of the suggested fast-recovery diodes.

V_{IN} (Max)	Current Rating	Use Part Number (or Equivalent)	
		Schottky	Fast-Recovery
20V	3A	1N5821 31DQ03	FR302, HER302 or MR850 (All These are Rated over 35V)
30V	3A	1N5822 or 31DQ04	
40V	3A	31DQ05 MBR350	*Not Recommended (See Text)*

FIGURE 5. Diode Selection Guide

Application Hints

Input Capacitor (C_{IN})

To maintain stability, the regulator input pin must be bypassed with at least a 22 µF electrolytic capacitor. The capacitor's leads must be kept short, and located as close as possible to the regulator.

If the operating temperature range includes temperatures below −25°C, the input capacitor value may need to be larger. (This also applies to the output capacitor.) With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures and age. For maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be greater than 1.2 × (t_{ON}/T) × I_{LOAD}.

Feedback Connection

The LM2575 feedback circuitry is designed so that, when the output voltage is connected directly to the Feedback pin, the output voltage is 5V.

$\overline{ON}$/OFF Input

For normal operation, the $\overline{ON}$/OFF pin should be grounded or driven with a low-level TTL voltage. To put the regulator into standby mode, drive this pin with a high-level TTL signal.

Application Hints (Continued)

Grounding

To maintain output voltage stability, the power ground connections must be low-impedance (see *Figure 1*). For the TO-3 style package, the case is ground. For the 5-lead TO-220 style package, both the tab and pin 3 are ground and either connection may be used, as they are both part of the same copper leadframe.

Heat Sink/Thermal Considerations

In many cases, no heat sink is required to keep the LM2575 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1. Maximum ambient temperature (in the application).
2. Maximum regulator power dissipation (in application).
3. Maximum allowed junction temperature (150°C for LM1575 or 125°C for the LM2575). For a safe, conservative design, a temperature approximately 15°C cooler than the maximum temperatures should be selected.
4. LM2575 package thermal resistances θ_{JA} and θ_{JC}.

Total power dissipated by the LM2575 can be calculated as follows:

$$P_D = (V_{IN})(I_S) + (V_O/V_{IN})(I_{LOAD})(V_{SAT})$$

where I_S (supply current) and V_{SAT} can be found in the Characteristic Curves shown previously, V_{IN} is the applied minimum input voltage, V_O is the regulated output voltage, and I_{LOAD} is the load current. The dynamic losses during turn-on and turn-off are negligible if a Schottky is used as the catch diode.

When no heat sink is used, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JA})$$

To arrive at the actual operating junction temperature, add the junction temperature rise to the maximum ambient temperature.

$$T_J = \Delta T_J + T_A$$

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined step 3, then a heat sink is required.

When using a heat sink, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D)(\theta_{JC} + \theta\text{interface} + \theta\text{Heat sink})$$

The operating junction temperature will be:

$$T_J = T_A + \Delta T_J$$

As above, if the actual operating junction temperature is greater than the selected safe operating junction temperature, then a larger heat sink is required (one that has a lower thermal resistance).

Definition of Terms

Buck Regulator

A switching regulator topology in which a higher voltage is converted to a lower voltage. Also known as a step-down switching regulator.

Catch Diode

The diode which provides a return path for the load current when the LM2575 switch is OFF.

Duty Cycle (D)

Ratio of the output switch's on-time to the oscillator period.

$$D = \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}} \text{ for buck regulator}$$

where T is the oscillator period, typically 1/52 kHz.

Efficiency (η)

The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Equivalent Series Inductance (ESL)

The pure inductance component of a capacitor (see *Figure 6*). The amount of inductance is determined to a large extent on the capacitor's construction.

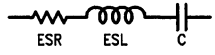

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FIGURE 6. Simple Model of a Real Capacitor

Equivalent Series Resistance (ESR)

The purely resistive component of a real capacitor's impedance. (see *Figure 6*). It causes power loss resulting in capacitor heating, which directly affects the capacitor's operating lifetime. When used as a switching regulator output filter, higher ESR values result in higher output ripple voltages.

Most standard aluminum electrolytic capacitors in the 220 μF–1000 μF range have 0.1Ω to 0.3Ω ESR. Higher-grade capacitors ("low-ESR", "high-frequency", or "low-inductance") in the 220 μF–1000 μF range generally have ESR of less than 0.15Ω.

Output Ripple Voltage

The AC component of the switching regulator's output voltage. It is usually dominated by the output capacitor's ESR multiplied by the inductor's ripple current. The peak-to-peak value of this sawtooth ripple current will be typically 40% of the maximum load current (when the Design Procedure in the datasheet is followed).

Ripple Current

RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature.

Standby Current (I_{STBY})

Supply current required by the LM2575 when in the standby mode ($\overline{ON}$/OFF pin is driven to TTL-high voltage), thus turning the output switch OFF.

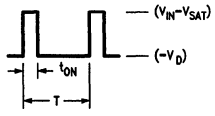
Pin Name	Pin Number (TO-220 Pkg.)	Normal Operation	Observed Problem		
		Voltage Waveform & Values	Condition	Probable Reason	Solution
Feedback	4	DC, V_{OUT} (5V Typ.) Plus Tri-Wave Ripple Voltage Plus Switching Noise	0 < V4 < 5V	V_{IN} Is Too Low Regulator Is in Current Limit	Increase V_{IN} to 7V Reduce Load to Less Than 1A
			V4 = 0V	ON/OFF Pin Is Not "Low"	Apply Correct Voltage to ON/OFF Pin
Output	2	Pulse Train  $T = 1/f_{OSC} \cong 19.2\ \mu s$ (Typ.) $\frac{t_{ON}}{T} \cong \frac{V_{OUT}}{V_{IN}}$	No Pulse Train Observed but V_{OUT} = 5V	Regulator Is Unloaded	Add 200 mA Load to Observe Switching
			Pulse Width Not Steady or Stable	Scope Not Triggered	Adjust Scope Trigger
				C_{IN} Is Too Far from LM2575	Reposition Capacitor as Close as Possible to Input Pin, so That Lead Length ≤1"
				Regulator Is in Current Limit	Reduce Load to Less Than 1A
				"Hard" Fast Recovery Diode Used	Change Diode to Schottky or "Soft" Fast Recovery Type (as Recommended)
				LM2575 Not Seated Firmly in Its Socket (if Used)	Improve Connections of Device to Circuit
ON/OFF	5	DC, 0V	V5 > 0V	Pin Control Not Set for Normal Operation (Improper Logic or Connection)	Apply Correct Voltage to Pin
Ground (Case of TO-3 Pkg.)	3 (Tab)	DC, 0V	Noisy	Probe Ground Lead Is Picking up Switching Noise	Use Short Ground Lead (≤1")
V_{IN}	1	DC, V_{IN} (from Unregulated Source)	0 < V1 < V_{IN}	Input Supply Overloaded	Verify That Input Supply Is Capable of Delivering at Least $(5V \times I_{LOAD} \times 1.3)/V_{IN}$ Amps

FIGURE 7. LM2575 Troubleshooting Guide

National Semiconductor

LM1578A/LM2578A/LM3578A Switching Regulator

General Description

The LM1578A is a switching regulator which can easily be set up for such DC-to-DC voltage conversion circuits as the buck, boost, and inverting configurations. The LM1578A features a unique comparator input stage which not only has separate pins for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. An external current limit terminal may be referenced to either the ground or the V_{in} terminal, depending upon the application. In addition, the LM1578A has an on board oscillator, which sets the switching frequency with a single external capacitor from <1 Hz to 100 kHz (typical).

The LM1578A is an improved version of the LM1578, offering higher maximum ratings for the total supply voltage and output transistor emitter and collector voltages.

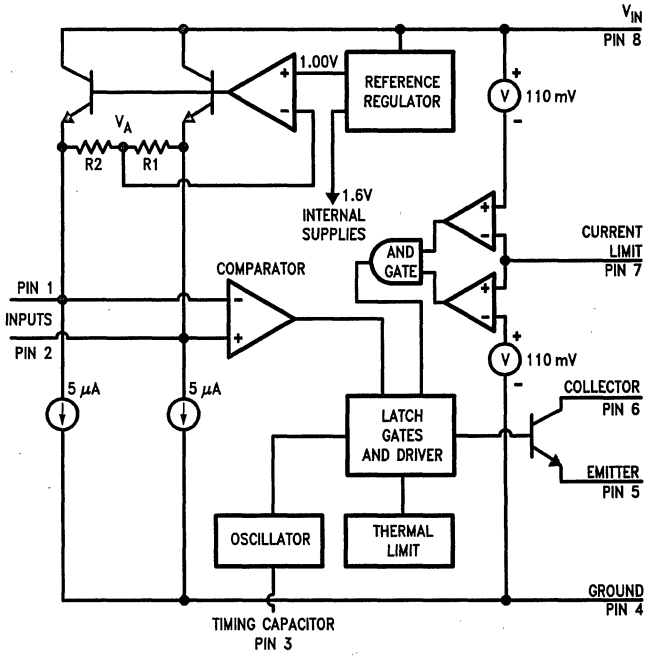
Features

- Inverting and non-inverting feedback inputs
- 1.0V reference at inputs
- Operates from supply voltages of 2V to 40V
- Output current up to 750 mA, saturation less than 0.9V
- Current limit and thermal shut down
- Duty cycle up to 90%

Applications

- Switching regulators in buck, boost, inverting, and single-ended transformer configurations
- Motor speed control
- Lamp flasher

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	50V
Collector Output to Ground	−0.3V to +50V
Emitter Output to Ground (Note 2)	−1V to +50V
Power Dissipation (Note 3)	Internally limited
Output Current	750 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	260°C
Maximum Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV

Operating Ratings

Ambient Temperature Range	
LM1578A	$-55°C \le T_A \le +125°C$
LM2578A	$-40°C \le T_A \le +85°C$
LM3578A	$0°C \le T_A \le +70°C$
Junction Temperature Range	
LM1578A	$-55°C \le T_J \le +150°C$
LM2578A	$-40°C \le T_J \le +125°C$
LM3578A	$0°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $2V \le V_{IN} \le 40V$ ($2.2V \le V_{IN} \le 40V$ for $T_J \le -25°C$), timing capacitor C_T = 3900 pF, and 25% ≤ duty cycle ≤ 75%, unless otherwise specified. Values in standard typeface are for T_J = 25°C; values in **boldface type** apply for operation over the specified operating junction temperature range.

Symbol	Parameter	Conditions	Typical (Note 5)	LM1578A Limit (Note 6)	LM2578A/ LM3578A Limit (Note 7)	Units
OSCILLATOR						
f_{OSC}	Frequency		20	 22.4 17.6	 24 16	kHz kHz (max) kHz (min)
$\Delta f_{OSC}/\Delta T$	Frequency Drift with Temperature		**−0.13**			%/°C
	Amplitude		550			mV_{p-p}
REFERENCE/COMPARATOR (Note 8)						
V_R	Input Reference Voltage	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 9)	1.0	 1.035/**1.050** 0.965/**0.950**	 1.050/**1.070** 0.950/**0.930**	V V (max) V (min)
$\Delta V_R/\Delta V_{IN}$	Input Reference Voltage Line Regulation	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 9)	0.003	 0.01/**0.02**	 0.01/**0.02**	%/V %/V (max)
I_{INV}	Inverting Input Current	$I_1 = I_2$ = 0 mA, duty cycle = 25%	0.5			μA
	Level Shift Accuracy	Level Shift Current = 1 mA	1.0	 5/**8**	 10/**13**	% % (max)
$\Delta V_R/\Delta t$	Input Reference Voltage Long Term Stability		100			ppm/1000h
OUTPUT						
V_C (sat)	Collector Saturation Voltage	I_C = 750 mA pulsed, Emitter grounded	0.7	 0.85/**1.2**	 0.90/**1.0**	V V (max)
V_E (sat)	Emitter Saturation Voltage	I_O = 80 mA pulsed, $V_{IN} = V_C$ = 40V	1.4	 1.6/**2.1**	 1.7/**2.0**	V V (max)
I_{CES}	Collector Leakage Current	$V_{IN} = V_{CE}$ = 40V, Emitter grounded, Output OFF	0.1	 50/**100**	 200/**250**	μA μA (max)
$BV_{CEO(SUS)}$	Collector-Emitter Sustaining Voltage	I_{SUST} = 0.2A (pulsed), V_{IN} = 0	60	 50	 50	V V (min)

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LM1578A Limit (Note 6)	LM2578A/ LM3578A Limit (Note 7)	Units
CURRENT LIMIT						
V_{CL}	Sense Voltage Shutdown Level	Referred to V_{IN} or Ground (Note 10)	110	95 140	80 160	mV mV (min) mV (max)
$\Delta V_{CL}/\Delta T$	Sense Voltage Temperature Drift		**0.3**			%/°C
I_{CL}	Sense Bias Current	Referred to V_{IN} Referred to ground	4.0 0.4			μA μA
DEVICE POWER CONSUMPTION						
I_S	Supply Current	Output OFF, V_E = 0V	2.0	3.0/**3.3**	3.5/**4.0**	mA mA (max)
		Output ON, I_C = 750 mA pulsed, V_E = 0V	14			mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: For $T_J \geq$ 100°C, the Emitter pin voltage should not be driven more than 0.6V below ground (see Application Information).

Note 3: At elevated temperatures, devices must be derated based on package thermal resistance. The device in the TO-99 package must be derated at 150°C/W, junction to ambient, or 45°C/W, junction to case. The device in the 8-pin DIP must be derated at 95°C/W, junction to ambient. The device in the surface-mount package must be derated at 150°C/W, junction-to-ambient.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values are for T_J = 25°C and represent the most likely parametric norm.

Note 6: All limits guaranteed and 100% production tested at room temperature (standard type face) and at **temperature extremes (bold type face).** All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** Room temperature limits are 100% production tested. Limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate AOQL.

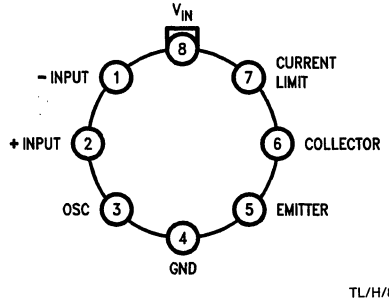
Note 8: Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage are applied, excessive current will flow and should be limited to less than 5 mA.

Note 9: I_1 and I_2 are the external sink currents at the inputs (refer to Test Circuit).

Note 10: Connection of a 10 kΩ resistor from pin 1 to pin 4 will drive the duty cycle to its maximum, typically 90%. Applying the minimum Current Limit Sense Voltage to pin 7 will not reduce the duty cycle to less than 50%. Applying the maximum Current Limit Sense Voltage to pin 7 is certain to reduce the duty cycle below 50%. Increasing this voltage by 15 mV may be required to reduce the duty cycle to 0%, when the Collector output swing is 40V or greater (see Ground-Referred Current Limit Sense Voltage typical curve).

Connection Diagram and Ordering Information

Metal Can



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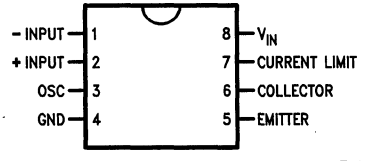
Top View
Order Number LM1578AH, LM2578AH, or LM3578AH
See NS Package Number H08C

Dual-In-Line Package

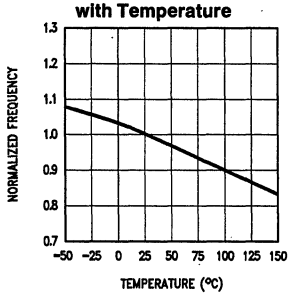


TL/H/8711–29

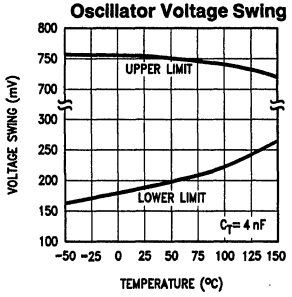
Order Number LM3578AM, LM2578AN or LM3578AN
See NS Package Number M08A or N08E

Typical Performance Characteristics

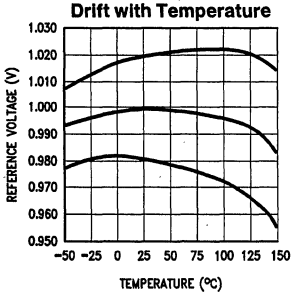
Oscillator Frequency Change with Temperature



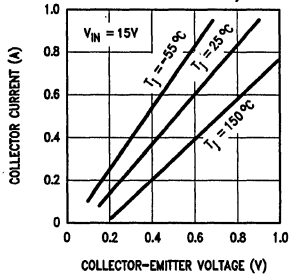
Oscillator Voltage Swing



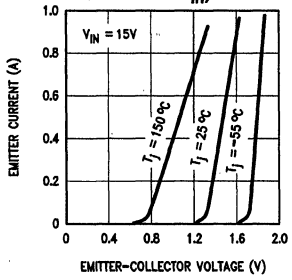
Input Reference Voltage Drift with Temperature



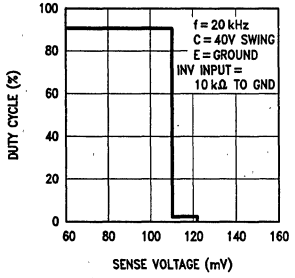
Collector Saturation Voltage (Sinking Current, Emitter Grounded)



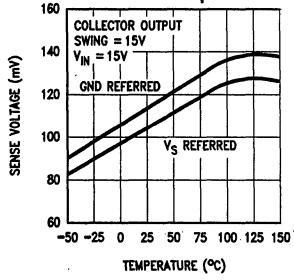
Emitter Saturation Voltage (Sourcing Current, Collector at V_{IN})



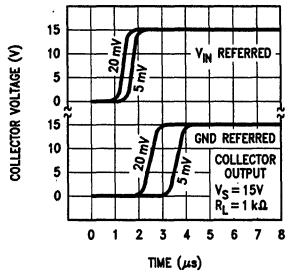
Ground Referred Current Limit Sense Voltage



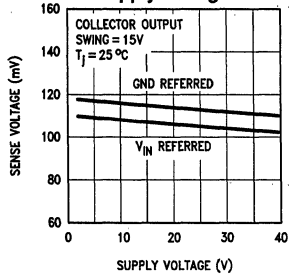
Current Limit Sense Voltage Drift with Temperature



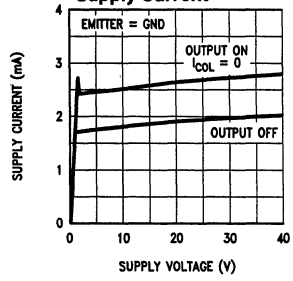
Current Limit Response Time for Various Over Drives



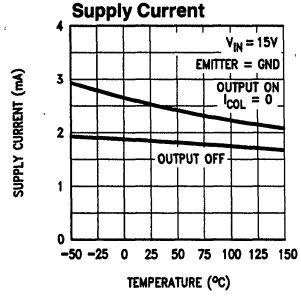
Current Limit Sense Voltage vs Supply Voltage



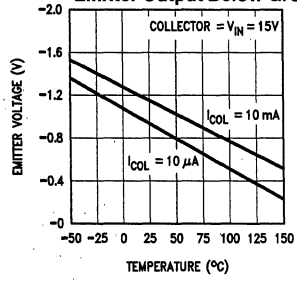
Supply Current



Supply Current



Collector Current with Emitter Output Below Ground



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Test Circuit*

Parameter tests can be made using the test circuit shown. Select the desired V_{in}, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference Voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = (T_{P3}(V)/1V) × 100%; S1 at $I_1 = I_2 = 1$ mA

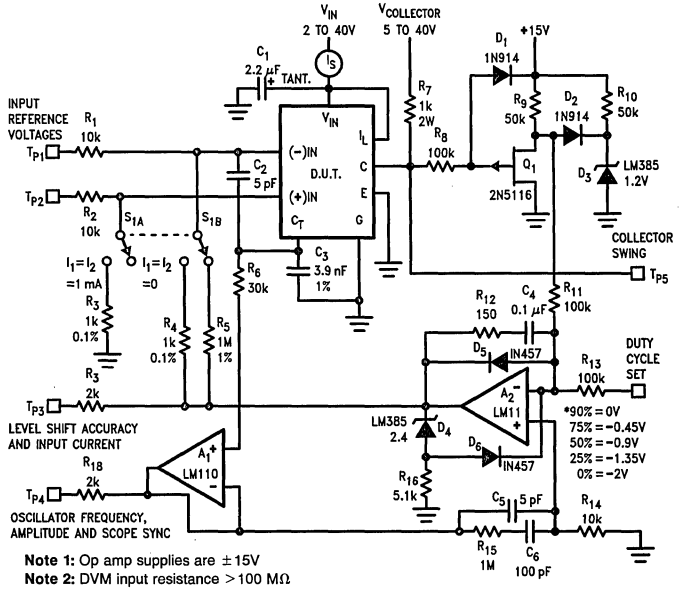
Input Current (mA) = (1V − T_{p3} (V))/1 MΩ: S1 at $I_1 = I_2 = 0$ mA.

Oscillator parameters can be measured at T_{p4} using a frequency counter or an oscilloscope.

The Current Limit Sense Voltage is measured by connecting an adjustable 0-to-1V floating power supply in series with the current limit terminal and referring it to either the ground or the V_{in} terminal. Set the duty cycle to 90% and monitor test point T_{P5} while adjusting the floating power supply voltage until the LM1578A's duty cycle just reaches 0%. This voltage is the Current Limit Sense Voltage.

The Supply Current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

*LM1578A specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.



Note 1: Op amp supplies are ±15V
Note 2: DVM input resistance >100 MΩ
Note 3: *LM1578 max duty cycle is 90%

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Definition of Terms

Input Reference Voltage: The reference voltage referred to ground, applied to either the inverting or non-inverting inputs, which will cause the output to switch ON or OFF.

Input Reference Current: The current applied to either the inverting or the non-inverting input which will cause the output to switch ON or OFF.

Input Level Shift Accuracy: If there are two equal resistors sinking current from the inverting and non-inverting input terminals, the Input Level Shift Accuracy is the ratio of the voltage across the resistors to produce a given duty cycle at the output.

Collector Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's emitter connected to ground, the Collector Saturation Voltage is the collector-to-emitter voltage for a given collector current.

Emitter Saturation Voltage: With the inverting input terminal grounded thru a 10 kΩ resistor and the output transistor's collector connected to V_{in}, the Emitter Saturation Voltage is the collector-to-emitter voltage for a given emitter current.

Collector Emitter Sustaining Voltage: The collector-emitter breakdown voltage of the output transistor, measured at a specified current.

Current Limit Sense Voltage: The voltage at the Current Limit pin, referred to either the supply or the ground terminal, which (via logic circuitry) will cause the output transistor to turn OFF and resets cycle-by-cycle at the oscillator frequency.

Current Limit Sense Current: The bias current for the Current Limit terminal with the applied voltage equal to the Current Limit Sense Voltage.

Supply Current: The IC power supply current, excluding the current drawn through the output transistor, with the oscillator operating.

Functional Description

The LM1578A is a pulse-width modulator designed for use as a switching regulator controller. It may also be used in other applications which require controlled pulse-width voltage drive.

A control signal, usually representing output voltage, fed into the LM1578A's comparator is compared with an internally-generated reference. The resulting error signal and the oscillator's output are fed to a logic network which determines when the output transistor will be turned ON or OFF. The following is a brief description of the subsections of the LM1578A.

COMPARATOR INPUT STAGE

The LM1578A's comparator input stage is unique in that both the inverting and non-inverting inputs are available to the user, and both contain a 1.0V reference. This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both input pins are open, no current flows through R1 and R2. Thus, both inputs to the comparator will have the potential of the 1.0V reference, V_A. When one input, for example the non-inverting input, is pulled ΔV away from V_A, a current of $\Delta V/R1$ will flow through R1. This same current flows through R2, and the comparator sees a total voltage of $2\Delta V$ between its inputs. The high gain of the system, through feedback, will correct for this imbalance and return both inputs to the 1.0V level.

This unusual comparator input stage increases circuit flexibility, while minimizing the total number of external components required for a voltage regulator system. The inverting switching regulator configuration, for example, can be set up without having to use an external op amp for feedback polarity reversal (see TYPICAL APPLICATIONS).

OSCILLATOR

The LM1578A provides an on-board oscillator which can be adjusted up to 100 kHz. Its frequency is set by a single external capacitor, C_1, as shown in *Figure 1*, and follows the equation

$$f_{OSC} = 8 \times 10^{-5}/C_1$$

The oscillator provides a blanking pulse to limit maximum duty cycle to 90%, and a reset pulse to the internal circuitry.

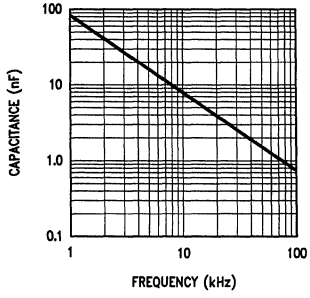

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FIGURE 1. Value of Timing Capacitor vs Oscillator Frequency

OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 750 mA with a saturation voltage of less than 0.9V. (see *Collector Saturation Voltage* and *Emitter Saturation Voltage* curves).

The emitter must not be pulled more than 1V below ground (this limit is 0.6V for $T_J \geq 100°C$). Because of this limit, an external transistor must be used to develop negative output voltages (see the Inverting Regulator Typical Application). Other configurations may need protection against violation of this limit (see the Emitter Output section of the Applications Information).

CURRENT LIMIT

The LM1578A's current limit may be referenced to either the ground or the V_{in} pins, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage 110 mV below V_{in}, the other with its inverting input referenced 110 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 110 mV away from either V_{in} or ground.

Applications Information

CURRENT LIMIT

As mentioned in the functional description, the current limit terminal may be referenced to either the V_{in} or the ground terminal. Resistor R3 converts the current to be sensed into a voltage for current limit detection.

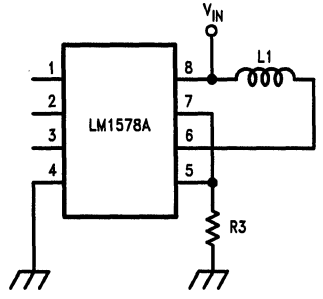

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FIGURE 2. Current Limit, Ground Referred

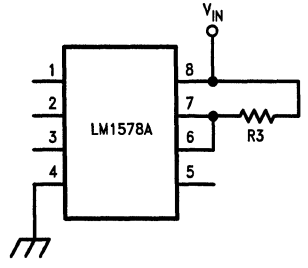

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FIGURE 3. Current Limit, V_{in} Referred

Applications Information (Continued)

CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, R1 and C1 act together as a low pass filter to control the current limit circuitry's response time.

Because the sense current of the current limit terminal varies according to where it is referenced, R1 should be less than 2 kΩ when referenced to ground, and less than 100Ω when referenced to V_{in}.

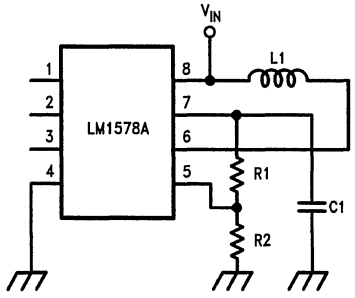

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FIGURE 4. Current Limit Transient Suppressor, Ground Referred

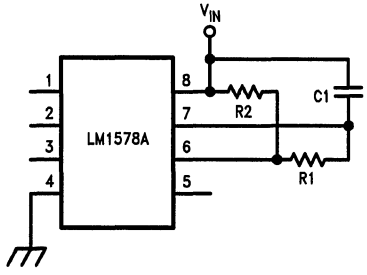

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FIGURE 5. Current Limit Transient Suppressor, V_{In} Referred

C.L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, the voltage divider network, consisting of R1 and R2, may be used. This effectively multiplies the sense voltage by (1 + R1/R2). Also, R1 can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode V_f + 110 mV).

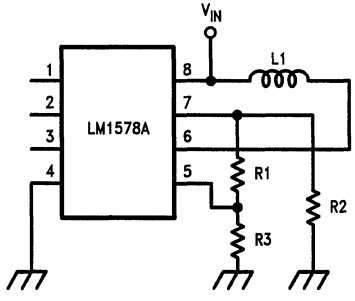

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FIGURE 6. Current Limit Sense Voltage Multiplication, Ground Referred

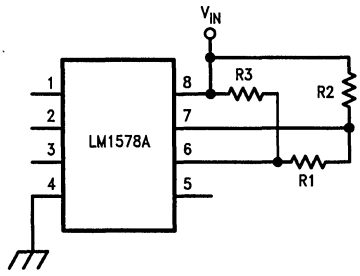

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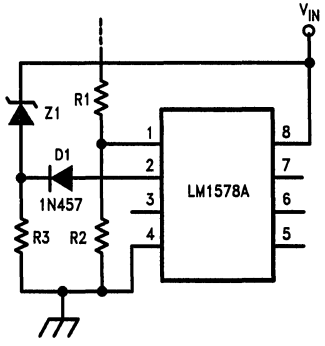
FIGURE 7. Current Limit Sense Voltage Multiplication, V_{In} Referred

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout is accomplished with few external components. When V_{in} becomes lower than the zener breakdown voltage, the output transistor is turned off. This occurs because diode D1 will then become forward biased, allowing resistor R3 to sink a greater current from the non-inverting input than is sunk by the parallel combination of R1 and R2 at the inverting terminal. R3 should be one-fifth of the value of R1 and R2 in parallel.



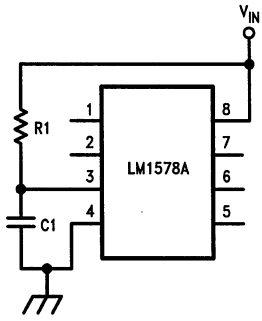
TL/H/8711–22

FIGURE 8. Under-Voltage Lockout

MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge to discharge ratio of the oscillator capacitor with a single external resistor. Typical values are 50 μA for the charge current, 450 μA for the discharge current, and a voltage swing from 200 mV to 750 mV. Therefore, R1 is selected for the desired charging and discharging slopes and C1 is readjusted to set the oscillator frequency.

Applications Information (Continued)



TL/H/8711–21

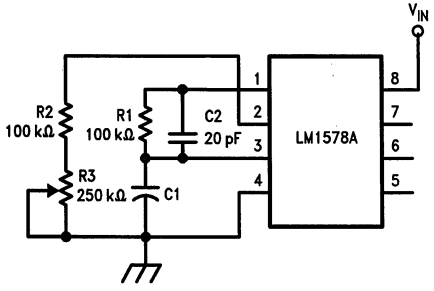
FIGURE 9. Maximum Duty Cycle Limiting

DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the cirucit shown below may be used. The output will turn on with the beginning of each oscillator cycle and turn off when the current sunk by R2 and R3 from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

With the resistor values as shown, R3 can be used to adjust the duty cycle from 0% to 90%.

When the sum of R2 and R3 is twice the value of R1, the duty cycle will be about 50%. C1 may be a large electrolytic capacitor to lower the oscillator frequency below 1 Hz.

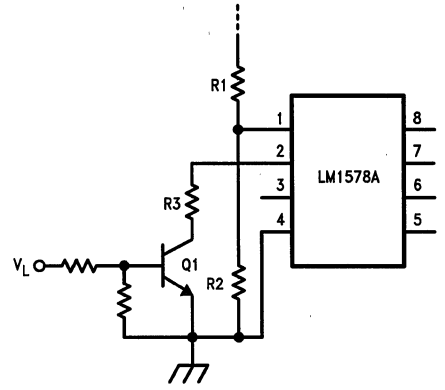


TL/H/8711–23

FIGURE 10. Duty Cycle Adjustment

REMOTE SHUTDOWN

The LM1578A may be remotely shutdown by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R3 to be approximately one-half the value of R1 and R2 in parallel.



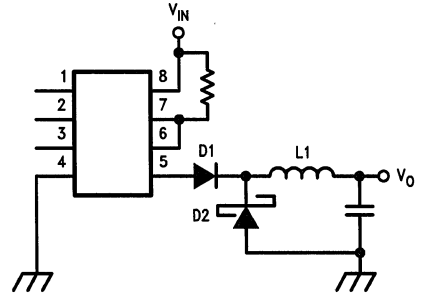
TL/H/8711–24

FIGURE 11. Shutdown Occurs when V_L is High

EMITTER OUTPUT

When the LM1578A output transistor is in the OFF state, if the Emitter output swings below the ground pin voltage, the output transistor will turn ON because its base is clamped near ground. The *Collector Current with Emitter Output Below Ground* curve shows the amount of Collector current drawn in this mode, vs temperature and Emitter voltage. When the Collector-Emitter voltage is high, this current will cause high power dissipation in the output transistor and should be avoided.

This situation can occur in the high-current high-voltage buck application if the Emitter output is used and the catch diode's forward voltage drop is greater than 0.6V. A fast-recovery diode can be added in series with the Emitter output to counter the forward voltage drop of the catch diode (see *Figure 2*). For better efficiency of a high output current buck regulator, an external PNP transistor should be used as shown in *Figure 16.*



TL/H/8711–30

FIGURE 12. D1 Prevents Output Transistor from Improperly Turning ON due to D2's Forward Voltage

Applications Information (Continued)

SYNCHRONIZING DEVICES

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal. This drive signal should be a pulse waveform with a minimum pulse width of 2 μs. and an amplitude from 1.5V to 2.0V. The signal source must be capable of 1.) driving capacitive loads and 2.) delivering up to 500 μA for each LM1578A.

Capacitors C1 thru CN are to be selected for a 20% slower frequency than the synchronization frequency.

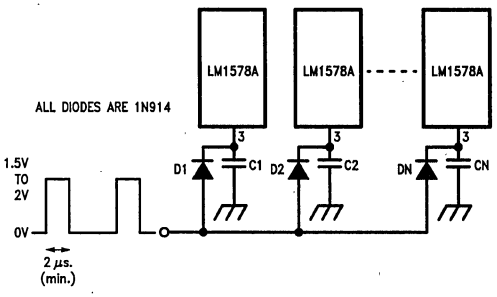


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FIGURE 13. Synchronizing Devices

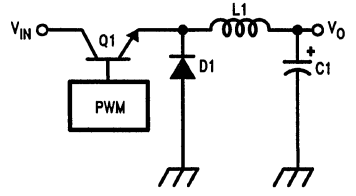
Typical Applications

The LM1578A may be operated in either the continuous or the discontinuous conduction mode. The following applications (except for the Buck-Boost Regulator) are designed for continuous conduction operation. That is, the inductor current is not allowed to fall to zero. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

BUCK REGULATOR

The buck configuration is used to step an input voltage down to a lower level. Transistor Q1 in *Figure 14* chops the input DC voltage into a squarewave. This squarewave is then converted back into a DC voltage of lower magnitude by the low pass filter consisting of L1 and C1. The duty cycle, D, of the squarewave relates the output voltage to the input voltage by the following equation:

$$V_{out} = D \times V_{in} = V_{in} \times (t_{on})/(t_{on} + t_{off}).$$



TL/H/8711–5

FIGURE 14. Basic Buck Regulator

Figure 15 is a 15V to 5V buck regulator with an output current, I_o, of 350 mA. The circuit becomes discontinuous at 20% of $I_{o(max)}$, has 10 mV of output voltage ripple, an efficiency of 75%, a load regulation of 30 mV (70 mA to 350 mA) and a line regulation of 10 mV ($12 \leq V_{in} \leq 18V$).

Component values are selected as follows:

$R1 = (V_o - 1) \times R2$ where $R2 = 10\ k\Omega$

$R3 = V/I_{sw(max)}$

$R3 = 0.15\Omega$

where:

V is the current limit sense voltage, 0.11V

$I_{sw(max)}$ is the maximum allowable current thru the output transistor.

L1 is the inductor and may be found from the inductance calculation chart (*Figure 16*) as follows:

Given $V_{in} = 15V$ $V_o = 5V$

$I_{o(max)} = 350\ mA$ $f_{OSC} = 50\ kHz$

Discontinuous at 20% of $I_{o(max)}$.

Note that since the circuit will become discontinuous at 20% of $I_{o(max)}$, the load current must not be allowed to fall below 70 mA.

Step 1: Calculate the maximum DC current through the inductor, $I_{L(max)}$. The necessary equations are indicated at the top of the chart and show that $I_{L(max)} = I_{o(max)}$ for the buck configuration. Thus, $I_{L(max)} = 350\ mA$.

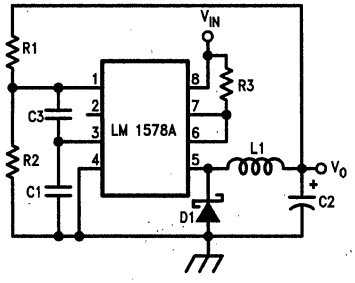
Step 2: Calculate the inductor Volts-sec product, E-T_{op}, according to the equations given from the chart. For the Buck:

$E\text{-}T_{op} = (V_{in} - V_o)(V_o/V_{in})(1000/f_{osc})$

$= (15 - 5)(5/15)(1000/50)$

$= 66V\text{-}\mu s.$

with the oscillator frequency, f_{osc}, expressed in kHz.



$V_{in} = 15V$
$V_o = 5V$
$V_{ripple} = 10\ mV$
$I_o = 350\ mA$
$f_{osc} = 50\ kHz$
$R1 = 40\ k\Omega$
$R2 = 10\ k\Omega$
$R3 = 0.15\Omega$
$C1 = 1820\ pF$
$C2 = 220\ \mu F$
$C3 = 20\ pF$
$L1 = 470\ \mu H$
$D1 = 1N5818$

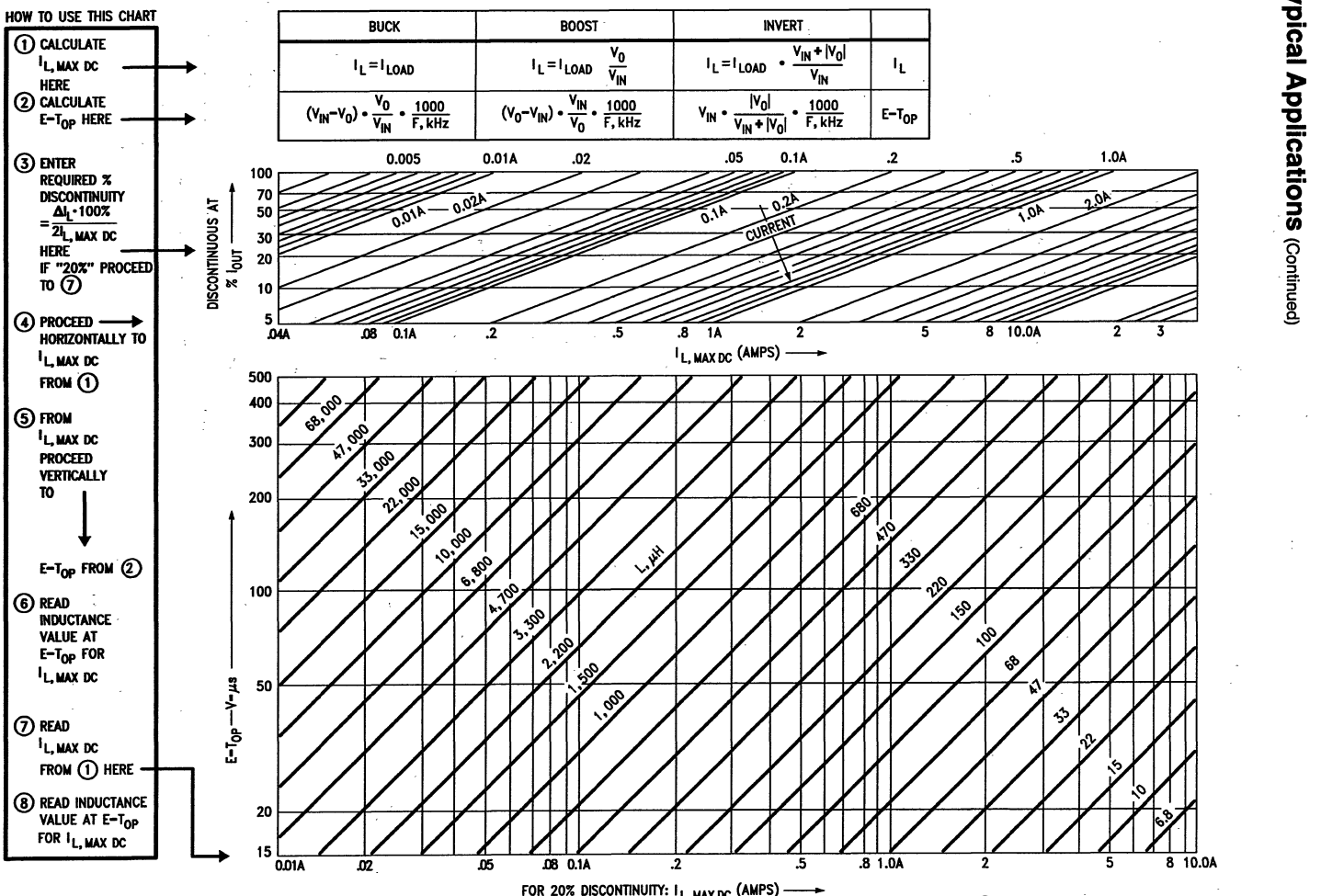
TL/H/8711–6

FIGURE 15. Buck or Step-Down Regulator

Step 3: Using the graph with axis labeled "Discontinuous At % I_{OUT}" and "$I_{L(max,\ DC)}$" find the point where the desired maximum inductor current, $I_{L(max,\ DC)}$ intercepts the desired discontinuity percentage.

In this example, the point of interest is where the 0.35A line intersects with the 20% line. This is nearly the midpoint of the horizontal axis.

Step 4: This last step is merely the translation of the point found in Step 3 to the graph directly below it. This is accomplished by moving straight down the page to the point which intercepts the desired E-T_{op}. For this example, E-T_{op} is 66V-μs and the desired inductor value is 470 μH. Since this example was for 20% discontinuity, the bottom chart could have been used directly, as noted in step 3 of the chart instructions.



TL/H/8711–31

FIGURE 17. DC/DC Inductance Calculator

Typical Applications (Continued)

For a full line of standard inductor values, contact Pulse Engineering (San Diego, Calif.) regarding their PE526XX series, or A. I. E. Magnetics (Nashville, Tenn.).

A more precise inductance value may be calculated for the Buck, Boost and Inverting Regulators as follows:

BUCK

$L = V_o (V_{in} - V_o)/(\Delta I_L V_{in} f_{osc})$

BOOST

$L = V_{in}^2 (V_o - V_{in})/(\Delta I_L f_{osc} V_o^2)$

INVERT

$L = V_{in}^2 |V_o|/[\Delta I_L (V_{in} + |V_o|)^2 f_{osc}]$

where ΔI_L is the current ripple through the inductor. ΔI_L is usually chosen based on the minimum load current expected of the circuit. For the buck regulator, since the inductor current I_L equals the load current I_O,

$$\Delta I_L = 2 \bullet I_{O(min)}$$

ΔI_L = 140 mA for this circuit. ΔI_L can also be interpreted as

$$\Delta I_L = 2 \bullet (\text{Discontinuity Factor}) \bullet I_L$$

where the Discontinuity Factor is the ratio of the minimum load current to the maximum load current. For this example, the Discontinuity Factor is 0.2.

The remainder of the components of *Figure 15* are chosen as follows:

C1 is the timing capacitor found in *Figure 1*.

$C2 \geq V_o (V_{in} - V_o)/(8 f_{osc}{}^2 V_{in} V_{ripple} L1)$

where V_{ripple} is the peak-to-peak output voltage ripple.

C3 is necessary for continuous operation and is generally in the 10 pF to 30 pF range.

D1 should be a Schottky type diode, such as the 1N5818 or 1N5819.

BUCK WITH BOOSTED OUTPUT CURRENT

For applications requiring a large output current, an external transistor may be used as shown in *Figure 17*. This circuit steps a 15V supply down to 5V with 1.5A of output current. The output ripple is 50 mV, with an efficiency of 80%, a load regulation of 40 mV (150 mA to 1.5A), and a line regulation of 20 mV (12V ≤ V_{in} ≤ 18V).

Component values are selected as outlined for the buck regulator with a discontinuity factor of 10%, with the addition of R4 and R5:

$R4 = 10 V_{BE1} B_f / I_p$

$R5 = (V_{in} - V - V_{BE1} - V_{sat}) B_f / (I_{L(max, DC)} + I_{R4})$

where:

V_{BE1} is the V_{BE} of transistor Q1.

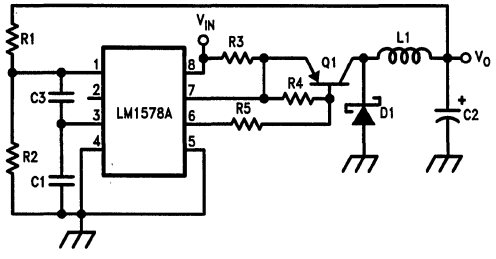
V_{sat} is the saturation voltage of the LM1578A output transistor.

V is the current limit sense voltage.

B_f is the forced current gain of transistor Q1 (B_f = 30 for *Figure 17*).

$I_{R4} = V_{BE1}/R4$

$I_p = I_{L(max, DC)} + 0.5 \Delta I_L$



V_{in} = 15V	R4 = 200Ω
V_o = 5V	R5 = 330Ω
V_{ripple} = 50 mV	C1 = 1820 pF
I_o = 1.5A	C2 = 330 µF
f_{osc} = 50 kHz	C3 = 20 pF
R1 = 40 kΩ	L1 = 220 µH
R2 = 10 kΩ	D1 = 1N5819
R3 = 0.05Ω	Q1 = D45

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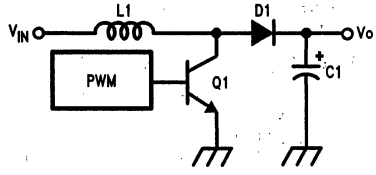
FIGURE 17. Buck Converter with Boosted Output Current

Typical Applications (Continued)

BOOST REGULATOR

The boost regulator converts a low input voltage into a higher output voltage. The basic configuration is shown in *Figure 18*. Energy is stored in the inductor while the transistor is on and then transferred with the input voltage to the output capacitor for filtering when the transistor is off. Thus,

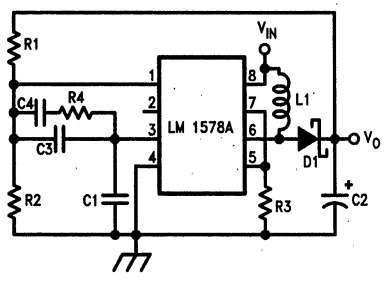
$$V_o = V_{in} + V_{in}(t_{on}/t_{off}).$$



TL/H/8711–9

FIGURE 18. Basic Boost Regulator

The circuit of *Figure 19* converts a 5V supply into a 15V supply with 150 mA of output current, a load regulation of 14 mV (30 mA to 150 mA), and a line regulation of 35 mV ($4.5V \le V_{in} \le 8.5V$).



V_{in} = 5V
V_o = 15V
V_{ripple} = 10 mV
I_o = 150 mA
f_{osc} = 50 kHz
R1 = 140 kΩ
R2 = 10 kΩ
R3 = 0.1Ω
R4 = 220 kΩ
C1 = 1820 pF
C2 = 470 µF
C3 = 20 pF
C4 = 0.0022 µF
L1 = 330 µH
D1 = 1N5818

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FIGURE 19. Boost or Step-Up Regulator

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{L(max,\,DC)} + 0.5\,\Delta I_L)$

where:

$\Delta I_L = 2(I_{LOAD(min)})(V_o/V_{in})$

R4, C3 and C4 are necessary for continuous operation and are typically 220 kΩ, 20 pF, and 0.0022 µF respectively.

C1 is the timing capacitor found in *Figure 1*.

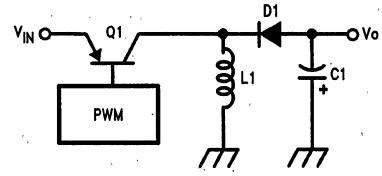
$C2 \ge I_o\,(V_o - V_{in})/(f_{osc}\,V_o\,V_{ripple})$.

D1 is a Schottky type diode such as a IN5818 or IN5819.

L1 is found as described in the buck converter section.

INVERTING REGULATOR

Figure 20 shows the basic configuration for an inverting regulator. The input voltage is of a positive polarity, but the output is negative. The output may be less than, equal to, or greater in magnitude than the input. The relationship between the magnitude of the input voltage and the output voltage is $V_o = V_{in} \times (t_{on}/t_{off})$.



TL/H/8711–10

FIGURE 20. Basic Inverting Regulator

Figure 21 shows an LM1578A configured as a 5V to −15V polarity inverter with an output current of 300 mA, a load regulation of 44 mV (60 mA to 300 mA) and a line regulation of 50 mV ($4.5V \le V_{in} \le 8.5V$).

$R1 = (|V_o| + 1)\,R2$ where $R2 = 10\,k\Omega$.

$R3 = V/(I_{L(max,\,DC)} + 0.5\,\Delta I_L)$.

$R4 = 10V_{BE1}B_f/(I_{L\,(max,\,DC)} + 0.5\,\Delta I_L)$

where:

V, V_{BE1}, V_{sat}, and B_f are defined in the "Buck Converter with Boosted Output Current" section.

$\Delta I_L = 2(I_{LOAD(min)})(V_{in} + |V_o|)/V_{IN}$

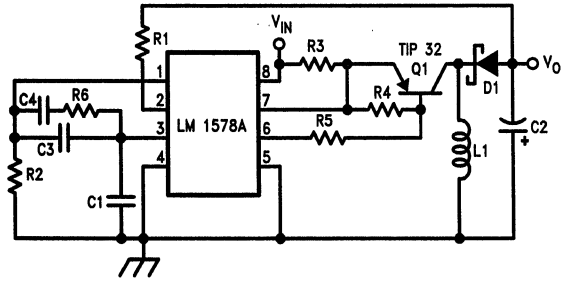
R5 is defined in the "Buck with Boosted Output Current" section.

R6 serves the same purpose as R4 in the Boost Regulator circuit and is typically 220 kΩ.

C1, C3 and C4 are defined in the "Boost Regulator" section.

$C2 \ge I_o\,|V_o|/[f_{osc}(|V_o| + V_{in})\,V_{ripple}]$

L1 is found as outlined in the section on buck converters, using the inductance chart for the invert configuration and 20% discontinuity.



V_{in} = 5V
V_o = −15V
V_{ripple} = 5 mV
I_o = 300 mA, I_{min} = 60 mA
f_{osc} = 50 kHz
R1 = 160 kΩ R2 = 10 kΩ
R3 = 0.01 Ω R4 = 190Ω
R5 = 82Ω R6 = 220 kΩ
C1 = 1820 pF
C2 = 1000 µF
C3 = 20 pF
C4 = 0.0022 µF
L1 = 150 µH
D1 = 1N5818

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FIGURE 21. Inverting Regulator

Typical Applications (Continued)

BUCK-BOOST REGULATOR

The Buck-Boost Regulator, shown in *Figure 22*, may step a voltage up or down, depending upon whether or not the desired output voltage is greater or less than the input voltage. In this case, the output voltage is 12V with an input voltage from 9V to 15V. The circuit exhibits an efficiency of 75%, with a load regulation of 60 mV (10 mA to 100 mA) and a line regulation of 52 mV.

$R1 = (V_o - 1)\,R2$ where $R2 = 10\,k\Omega$

$R3 = V/0.75A$

R4, C1, C3 and C4 are defined in the "Boost Regulator" section.

D1 and D2 are Schottky type diodes such as the 1N5818 or 1N5819.

$$C2 \geq \frac{(I_o/V_{ripple})(V_o + 2V_d)}{[f_{osc}(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})]}$$

where:

V_d is the forward voltage drop of the diodes.

V_{sat} is the saturation voltage of the LM1578A output transistor.

V_{sat1} is the saturation voltage of transistor Q1.

$$L1 \geq (V_{in} - V_{sat} - V_{sat1})(t_{on}/I_p)$$

where:

$$t_{on} = \frac{(1/f_{osc})(V_o + 2V_d)}{(V_o + V_{in} + 2V_d - V_{sat} - V_{sat1})}$$

$$I_p = \frac{2I_o(V_{in} + V_o + 2V_d - V_{sat} - V_{sat1})}{(V_{in} - V_{sat} - V_{sat1})}$$

RS-232 LINE DRIVER POWER SUPPLY

The power supply, shown in *Figure 23*, operates from an input voltage as low as 4.2V (5V nominal), and delivers an output of ±12V at ±40 mA with better than 70% efficiency. The circuit provides a load regulation of ±150 mV (from 10% to 100% of full load) and a line regulation of ±10 mV. Other notable features include a cycle-by-cycle current limit and an output voltage ripple of less than 40 mVp-p.

A unique feature of this circuit is its use of feedback from both outputs. This dual feedback configuration results in a sharing of the output voltage regulation by each output so that neither side becomes unbalanced as in single feedback systems. In addition, since both sides are regulated, it is not necessary to use a linear regulator for output regulation.

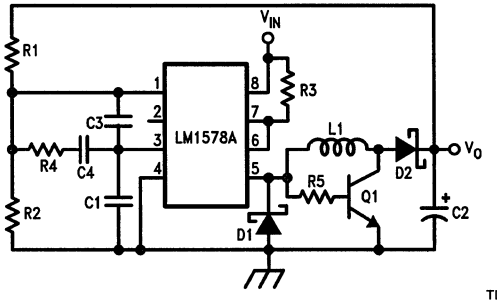
The feedback resistors, R2 and R3, may be selected as follows by assuming a value of 10 kΩ for R1;

$R2 = (V_o - 1V)/45.8\,\mu A = 240\,k\Omega$

$R3 = (|V_o| + 1V)/54.2\,\mu A = 240\,k\Omega$

Actually, the currents used to program the values for the feedback resistors may vary from 40 μA to 60 μA, as long as their sum is equal to the 100 μA necessary to establish the 1V threshold across R1. Ideally, these currents should be equal (50 μA each) for optimal control. However, as was done here, they may be mismatched in order to use standard resistor values. This results in a slight mismatch of regulation between the two outputs.

The current limit resistor, R4, is selected by dividing the current limit threshold voltage by the maximum peak current level in the output switch. For our purposes R4 = 90 mV/750 mA = 0.12Ω. A value of 0.1Ω was used.



$9V \leq V_{in} \leq 15V$
$V_o = 12V$
$I_o = 100\,mA$
$V_{ripple} = 50\,mV$
$f_{osc} = 50\,kHz$
R1 = 110 k
R2 = 10 k
R3 = 0.1
R4 = 220 k
R5 = 270
C1 = 1820 pF
C2 = 220 μF
C3 = 20 pF
C4 = 0.0022 μF
L1 = 220 μH
D1, D2 = 1N5819
Q1 = D44

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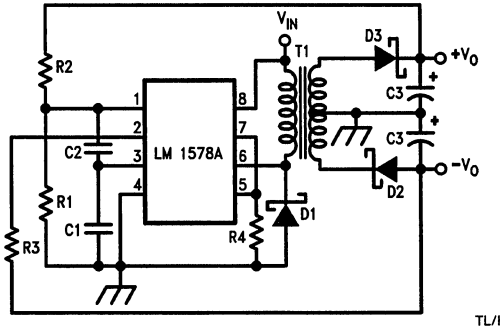
FIGURE 22. Buck-Boost Regulator



$V_{in} = 5V$
$V_o = \pm 12V$
$I_o = \pm 40\,mA$
$f_{osc} = 80\,kHz$
R1 = 10 kΩ
R2 = 240 kΩ
R3 = 240 kΩ
R4 = 0.1 Ω
C1 = 820 pF
C2 = 10 pF
C3 = 220 μF
D1, D2, D3 = 1N5819
T1 = PE-64287

TL/H/8711–14

FIGURE 23. RS-232 Line Driver Power Supply

Typical Applications (Continued)

Capacitor C1 sets the oscillator frequency and is selected from *Figure 1*.

Capacitor C2 serves as a compensation capacitor for synchronous operation and a value of 10 to 50 pF should be sufficient for most applications.

A minimum value for an ideal output capacitor C3, could be calculated as $C = I_o \times t/\Delta V$ where I_o is the load current, t is the transistor on time (typically $0.4/f_{osc}$), and ΔV is the peak-to-peak output voltage ripple. A larger output capacitor than this theoretical value should be used since electrolytics have poor high frequency performance. Experience has shown that a value from 5 to 10 times the calculated value should be used.

For good efficiency, the diodes must have a low forward voltage drop and be fast switching. 1N5819 Schottky diodes work well.

Transformer selection should be picked for an output transistor "on" time of $0.4/f_{osc}$, and a primary inductance high enough to prevent the output transistor switch from ramping higher than the transistor's rating of 750 mA. Pulse Engineering (San Diego, Calif.) and Renco Electronics, Inc. (Deer Park, N.Y.) can provide further assistance in selecting the proper transformer for a specific application need. The transformer used in *Figure 23* was a Pulse Engineering PE-64287.

National Semiconductor

LM2579 Switching Regulator

General Description

The LM2579 can easily be used in switching regulator configurations, such as the buck, boost, and inverting, to perform DC-to-DC voltage conversion. The LM2579 features a unique comparator input stage which not only has separate pins for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 3A and has output pins for both its collector and emitter to promote design flexibility. An external current limit terminal may be referenced to either the ground or the V_{IN} terminal, depending upon the application. In addition, the LM2579 has an onboard oscillator, which sets the switching frequency with a single external capacitor, from <1 Hz to 100 kHz (typical).

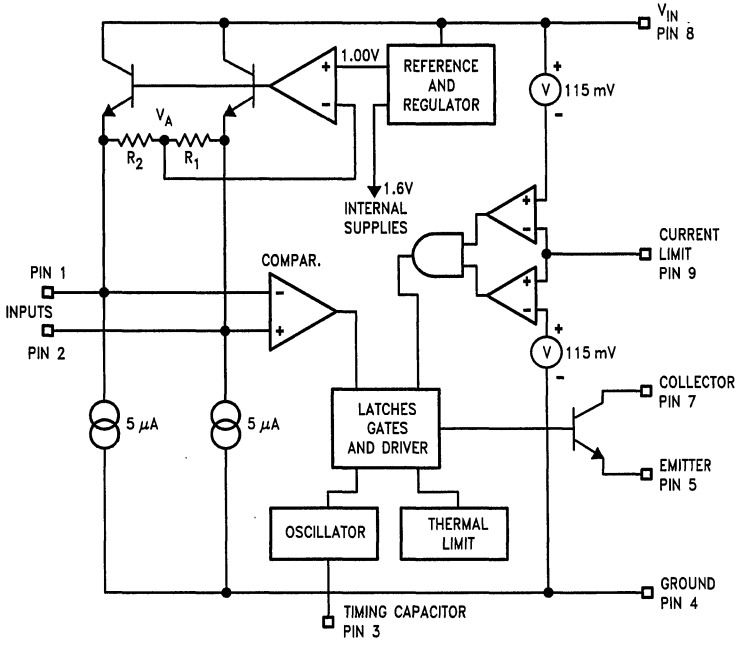
Features

- Inverting and non-inverting feedback inputs
- 1.0V reference at inputs
- Operates from supply voltages of 3.5V to 40V
- Output current up to 3A, saturation less than 0.75V
- Emitter output can swing below ground terminal, for ease of use in inverting applications
- Current limit and thermal shutdown
- Duty cycle up to 90%

Applications

- Switching regulators in buck, boost, inverting, and single-ended transformer configurations
- Motor speed control
- Lamp flasher

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	50V
Collector Output to Ground	−0.3V to +50V
Emitter Output to Ground (Note 2)	−20V to +50V
Power Dissipation (Note 3)	Internally limited
Output Current	3A
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Maximum Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV

Operating Ratings

Ambient Temperature	$-40°C \le T_A \le +85°C$
Junction Temperature	$-40°C \le T_J \le +125°C$
Supply Voltage	$3.5V \le V_{IN} \le 40V$

Electrical Characteristics

These specifications apply for $3.5V \le V_{IN} \le 40V$, timing capacitor C_T = 3900 pF, and 25% ≤ duty cycle ≤ 75%, unless otherwise specified. Values in standard typeface are for T_J = 25°C, values in **boldface type** apply for **$-40°C \le T_J \le +125°C$.**

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
OSCILLATOR					
f_{OSC}	Frequency		20	 24 16	kHz kHz (max) kHz (min)
$\Delta f_{OSC}/\Delta T$	Frequency Drift with Temperature		**−0.13**		%/°C
	Amplitude		550		mV_{p-p}
REFERENCE/COMPARATOR (Note 7)					
V_R	Input Reference Voltage	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 8)	1.0	 1.050/**1.070** 0.950/**0.930**	V V (max) V (min)
$\Delta V_R/\Delta V_{IN}$	Input Reference Voltage Line Regulation	$I_1 = I_2$ = 0 mA and $I_1 = I_2$ = 1 mA ±1% (Note 8)	0.003	 0.01/**0.02**	%/V %/V (max)
I_{INV}	Inverting Input Current	$I_1 = I_2$ = 0 mA, duty cycle = 25%	0.5		μA
	Level Shift Accuracy	Level Shift Current = 1mA	1.0	 10/**13**	% % (max)
$\Delta V_R/\Delta t$	Input Reference Voltage Long Term Stability		100		ppm/1000h
OUTPUT					
V_C(sat)	Collector Saturation Voltage	I_C = 3A Pulsed, Emitter Grounded	0.55	 0.75/**1.0**	V V (max)
V_E(sat)	Emitter Saturation Voltage	I_O = 3A Pulsed, $V_{IN} = V_C$ = 40V	1.7	 1.9/**2.0**	V V (max)
I_{CES}	Collector Leakage Current	$V_{IN} = V_{CE}$ = 40V, Emitter Grounded, Output OFF	0.1	 600/**750**	μA μA (max)
I_{CEX}	Emitter Leakage Current	$V_{IN} = V_C$ = 20V, V_E = −20V, Output OFF	0.1	 600/**750**	μA μA (max)
$BV_{CEO(SUS)}$	Collector-Emitter Sustaining Voltage	I_{SUST} = 0.2A (Pulsed), V_{IN} = 0	60	 50	V V (Min)

Electrical Characteristics (Continued)

These specifications apply for $3.5V \leq V_{IN} \leq 40V$, timing capacitor C_T = 3900 pF, and $25\% \leq$ duty cycle $\leq 75\%$, unless otherwise specified. Values in standard typeface are for $T_J = 25°C$, values in **boldface type** apply for $-40°C \leq T_J \leq +125°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
CURRENT LIMIT					
V_{CL}	Sense Voltage Shutdown Level	Referred to V_{IN} or Ground	115	 80 160	mV mV (min) mV (max)
$\Delta V_{CL}/\Delta T$	Sense Voltage Temperature Drift		**0.3**		%/°C
I_{CL}	Sense Bias Current	Referred to V_{IN} Referred to Ground	40 0.4		μA μA
DEVICE POWER CONSUMPTION					
I_S	Supply Current	Output OFF, V_E = 0V	3.0	 5.0/**7.0**	mA mA (max)
		Output ON, I_C = 3A Pulsed, V_E = 0V	55	 75/**150**	mA, peak (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Maximum voltage between emitter and collector or supply is 50V.

Note 3: At elevated temperatures, devices must be derated based on package thermal resistance. The device in the 11-lead TO-220 package must be derated at 36°C/W, junction to ambient, or 1°C/W, junction to case.

Note 4: Human body model, R = 1.5 kΩ, C = 100 pF.

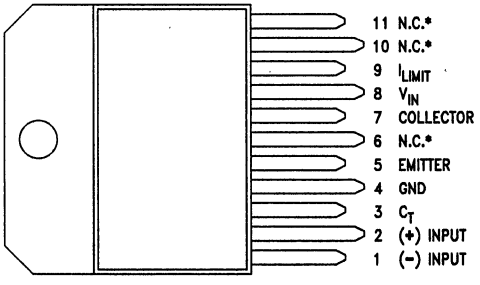
Note 5: Typical values are for $T_J = 25°C$ and represent the most likely parametric norm.

Note 6: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** Room temperature limits are 100% production tested. Limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Input terminals are protected from accidental shorts to ground but if external voltages higher than the reference voltage is applied, excessive current will flow and should be limited to less than 5 mA.

Note 8: I_1 and I_2 are the external sink currents at the inputs (refer to Test Circuit).

Connection Diagram and Ordering Information



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Top View

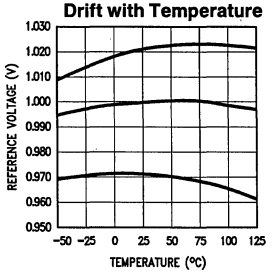
Tab connected to Pin 4 (Ground)

*N.C. = No internal connection

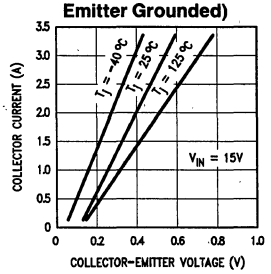
Order Number LM2579T
See NS Package Number TA11B

Typical Performance Characteristics

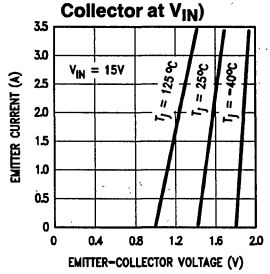
Input Reference Voltage Drift with Temperature



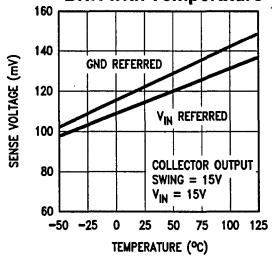
Collector Saturation Voltage (Sinking Current, Emitter Grounded)



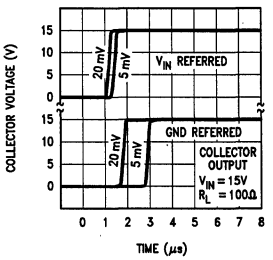
Emitter Saturation Voltage (Sourcing Current, Collector at V_{IN})



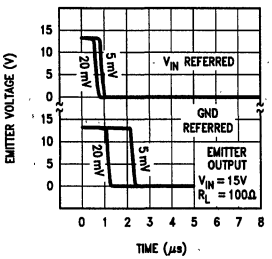
Current Limit Sense Voltage Drift with Temperature



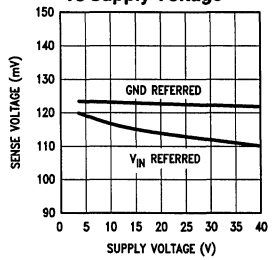
Current Limit Response Time for Various Over Drives



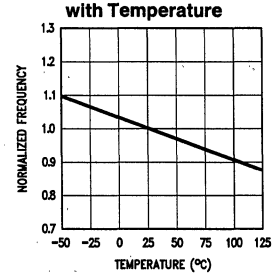
Current Limit Response Time for Various Over Drives



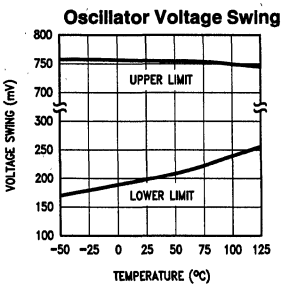
Current Limit Sense Voltage vs Supply Voltage



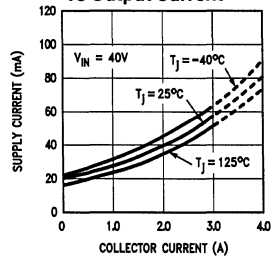
Oscillator Frequency Change with Temperature



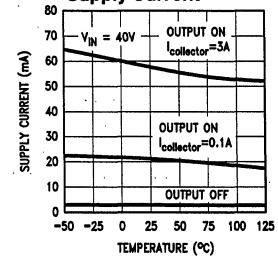
Oscillator Voltage Swing



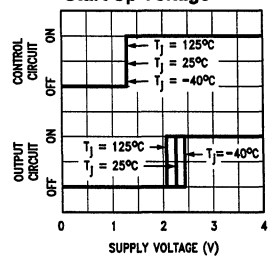
Supply Current vs Output Current



Supply Current



Start Up Voltage



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Test Circuit†

Parameter tests can be made using the test circuit shown. Select the desired V_{IN}, collector voltage and duty cycle with adjustable power supplies. A digital volt meter with an input resistance greater than 100 MΩ should be used to measure the following:

Input Reference voltage to Ground; S1 in either position.

Level Shift Accuracy (%) = $T_{P3}(V)/1V) \bullet 100\%$; S1 at $I_1 = I_2 = 1$ mA.

Input current (mA) = $(1V - T_{P3}(V))/1\ M\Omega$; S1 at $I_1 = I_2 = 0$ mA.

Oscillator parameters can be measured at TP4 using a frequency counter or an oscilloscope.

The Current Limit Sense Voltage is measured by connecting an adjustable 0-to-1V floating power supply in series with the current limit terminal and referring it to either the ground or the V_{IN} terminal. Set the duty cycle to 90% and monitor test point T_{P5} while adjusting the floating power supply voltage until the LM2579's duty cycle just reaches 0%. This voltage is the Current Limit Sense Voltage.

The Supply Current should be measured with the duty cycle at 0% and S1 in the $I_1 = I_2 = 0$ mA position.

†LM2579 specifications are measured using automated test equipment. This circuit is provided for the customer's convenience when checking parameters. Due to possible variations in testing conditions, the measured values from these testing procedures may not match those of the factory.

Definition of Terms

Input Reference Voltage: The reference voltage referred to ground, applied to either the inverting or non-inverting inputs, which will cause the output to switch ON or OFF.

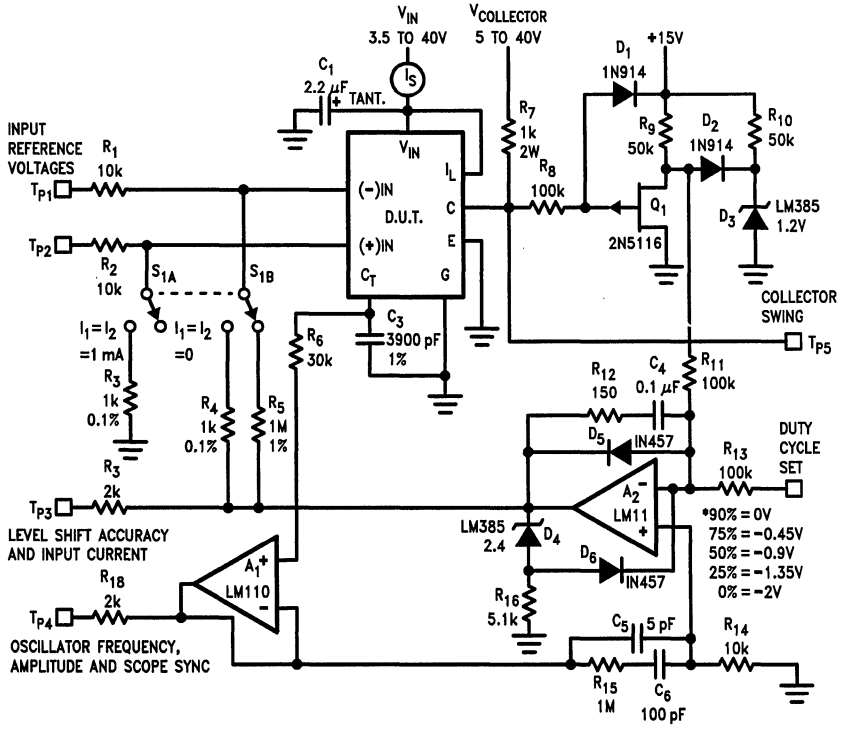
Input Reference Current: The current applied to either the inverting or the non-inverting input which will cause the output to switch ON or OFF.

Input Level Shift Accuracy: If there are two equal resistors sinking current from the inverting and non-inverting input terminals, the Input Level Shift Accuracy is the ratio of the voltage across the resistors to produce a given duty cycle at the output.

Collector Saturation Voltage: With the inverting input terminal grounded through a 10 kΩ resistor and the output transistor's emitter connected to ground, the Collector Saturation Voltage is the collector-to-emitter voltage for a given collector current.

Emitter Saturation Voltage: With the inverting input terminal grounded through a 10 kΩ resistor and the output transistor's collector connected to V_{IN}, the Emitter Saturation Voltage is the collector-to-emitter voltage for a given emitter current.

Collector-Emitter Sustaining Voltage: The collector-emitter breakdown voltage of the output transistor, measured at a specified current.



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Note 1: Op amp supplies are +15V.

Note 2: DVM input resistance > 100 MΩ.

Note 3: *LM2579 max duty cycle is 90%.

Definition of Terms (Continued)

Current Limit Sense Voltage: The voltage at the current Limit pin, referred to either the V_{IN} terminal or the ground terminal, which (via logic circuitry) will cause the output transistor to turn OFF. The logic circuitry is reset at the beginning of each oscillator cycle.

Current Limit Sense Current: The bias current for the Current Limit terminal with the applied voltage equal to the Current Limit Sense Voltage.

Supply Current: The IC power supply current, excluding current drawn through the output transistor, with the oscillator operating.

Functional Description

The LM2579 is a pulse-width modulator designed for use as a switching regulator controller. It may also be used in other applications which require controlled pulse-width voltage drive.

A control signal, usually representing output voltage, fed into the LM2579's comparator is compared with an internally-generated reference. The resulting error signal and the oscillator's output are fed to a logic network which determines when the output transistor will be turned ON or OFF. The following is a brief description of the subsections of the LM2579.

COMPARATOR INPUT STAGE

The LM2579's comparator input stage is unique in that both the inverting and non-inverting inputs are available to the user, and both contain a 1.0V reference. This is accomplished as follows: A 1.0V reference is fed into a modified voltage follower circuit (see FUNCTIONAL DIAGRAM). When both input pins are open, no current flows through R_1 and R_2. Thus, both inputs to the comparator will have the potential of the 1.0V reference, V_A. When one input, for example the non-inverting input, is pulled ΔV away from V_A, a current of $\Delta V/R_1$ will flow through R_1. This same current flows through R_2, and the comparator sees a total voltage of $2\Delta V$ between its inputs. The high gain of the system, through feedback, will correct for this imbalance and return both inputs to the 1.0V level.

This unusual comparator input stage increases circuit flexibility, while minimizing the total number of external components required for a voltage regulator system. The inverting switching regulator configuration, for example, can be set up without having to use an external op amp for feedback polarity reversal (See TYPICAL APPLICATIONS).

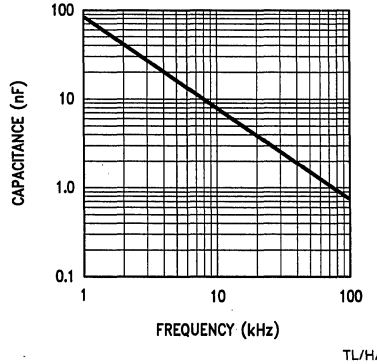

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FIGURE 1. Value of Timing Capacitor vs Oscillator Frequency

OSCILLATOR

The LM2579 provides an on-board oscillator which can be adjusted up to 100 kHz. Its frequency is set by a single external capacitor, C_1, as shown in *Figure 1*, and follows the equation

$$f_{OSC} = 8 \times 10^{-5}/C_1$$

The oscillator provides a blanking pulse to limit maximum duty cycle to 90%, and a reset pulse to the internal circuitry.

OUTPUT TRANSISTOR

The output transistor is capable of delivering up to 3A with a saturation voltage of less than 0.75V (see *Collector Saturation Voltage* and *Emitter Saturation Voltage* curves).

The emitter can be pulled below ground, as long as the total voltage between the emitter pin and collector or supply pin does not exceed 50V. This feature allows the LM2579 to be used in an inverting regulator configuration without an additional output transistor which would normally be required to protect the device from the negative output voltage.

CURRENT LIMIT

The LM2579's current limit may be referenced to either the ground or the V_{IN} pin, and operates on a cycle-by-cycle basis.

The current limit section consists of two comparators: one with its non-inverting input referenced to a voltage 115 mV below V_{IN}, the other with its inverting input referenced 115 mV above ground (see FUNCTIONAL DIAGRAM). The current limit is activated whenever the current limit terminal is pulled 115 mV away from either V_{IN} or ground.

Application Information

CIRCUIT BOARD LAYOUT

Because of fast switching of high output currents, the circuit board layout should be carefully thought out. The comparator inputs are sensitive to noise, and should be kept away from the high-energy switching signals. Feedback resistors should be located near the input terminals. A single-point ground should be used for the oscillator capacitor, device ground, and feedback (when appropriate) to avoid ground loops.

LEAD INDUCTANCE IMPACTS DIODE CHOICE

It is always important to use diodes designed for switching applications. Schottky diodes generally provide superior performance, although fast recovery diodes can also be used. Fast recovery diodes differ from Schottky diodes in their turn-on and turn-off characteristics, which can cause voltage transients that will affect circuit operation.

The turn-off, or "recovery," time of a diode refers to the time it takes for the charge that has been stored in the diode during the forward conduction period to be depleted. During this recovery period, the diode appears to be a short, causing a fast current pulse to flow through the switch. Since the LM2579's output is capable of switching current at a rate of approximately 30 A/μs, and one inch of 20-gauge wire has approximately 30 nH of inductance, a transient of nearly 1V can be generated for every inch of stray wire ($V = L\,di/dt$ = 30 nH × 30 A/μs = 0.9V). Since the LM2579's current limit sense voltage is 115 mV (typ.), transients like these can

Application Information (Continued)

greatly affect circuit operation. They can be minimized by keeping all lead lengths short, thus reducing stray inductances. Additional methods of suppressing noise spikes and switching transients are described in the Current Limit Transient Suppression section.

The turn-on time of the switching diode must also be considered. A slow turn-on can cause an increase in the voltage across the output transistor, which is rated for 50V (maximum) in the LM2579). This condition can exist in all configurations.

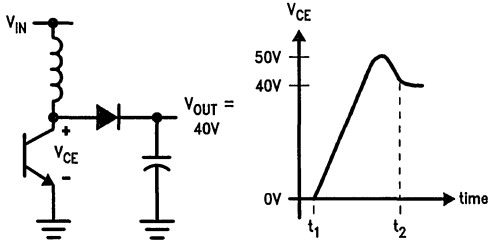

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FIGURE 2. Transient Applied to Output Transistor by Slow Turn-On of Diode

Referring to *Figure 2*, at t_1 the transistor turns OFF; at t_2, the diode turns ON. This delay allows buildup of voltage across the non-conducting diode, which is applied to the transistor until the diode begins conducting.

CURRENT LIMIT

As noted in the functional description, the current limit terminal may be referred to either V_{IN} or ground (see *Figures 3, 4*). The resistor R_{CL} converts the current to be sensed into a voltage for current limit detection.

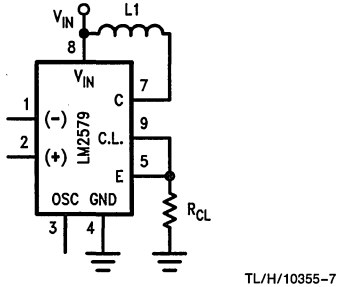

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FIGURE 3. Current Limit, Ground Referred

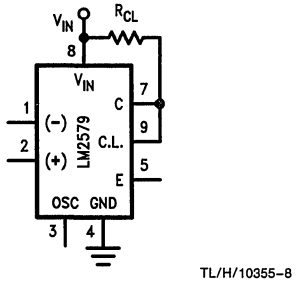

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FIGURE 4. Current Limit, V_{IN} Referred

C. L. SENSE VOLTAGE MULTIPLICATION

When a larger sense resistor value is desired, a voltage divider network may be used (see *Figures 5, 6*). This effectively multiplies the sense voltage by (1 + R1/R2). Alternatively, R1 can be replaced by a diode to increase current limit sense voltage to about 800 mV (diode V_d + 115 mV).

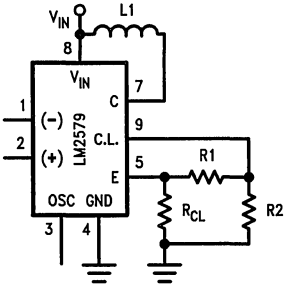

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FIGURE 5. Current Limit Sense Voltage Multiplication, Ground Referred

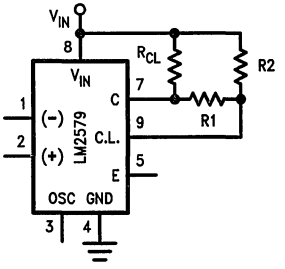

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FIGURE 6. Current Limit Sense Voltage Multiplication, V_{IN} Referred

CURRENT LIMIT TRANSIENT SUPPRESSION

When noise spikes and switching transients interfere with proper current limit operation, an RC low-pass filter can be used to control the current limit circuitry's response time (see *Figures 7, 8*).

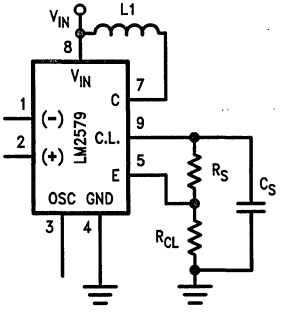

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FIGURE 7. Current Limit Transient Suppressor, Ground Referred

Application Information (Continued)

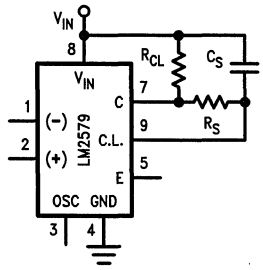

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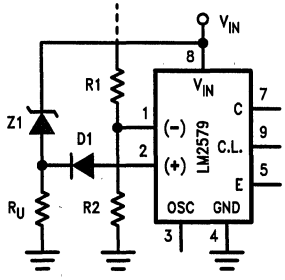
FIGURE 8: Current Limit Transient Suppressor, V_{IN} Referred

Because the input current of the current limit terminal varies according to its reference point, R_S should be less than 2 kΩ when referred to ground, and less than 100Ω when referred to V_{IN}. C_S is typically 0.01 μF.

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout requires few external components, as shown in *Figure 9*. When V_{IN} becomes lower than the zener breakdown voltage, the LM2579's output transistor is turned OFF. This occurs because diode D1 will then become forward biased, allowing resistor R_U to sink a greater current from the non-inverting input than is sunk by the parallel combination of the feedback resistors, R1 and R2, at the inverting terminal. R_U should be one-fifth of the value of R1 and R2 in parallel.



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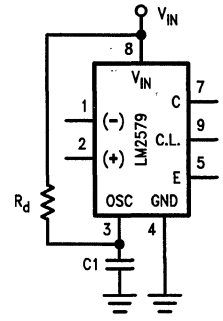
D1 = 1N457 or similar

FIGURE 9. Under-Voltage Lockout

MAXIMUM DUTY CYCLE LIMITING

The maximum duty cycle can be externally limited by adjusting the charge-to-discharge ratio of the oscillator capacitor with a single external resistor, as shown in *Figure 10*. Typical values are 50 μA for the charge current, 450 μA for the discharge current and a voltage swing from 200 mV to 750 mV. Therefore, R_d is selected for the desired charging and discharging slopes, and C1 is readjusted to set the oscillator frequency.



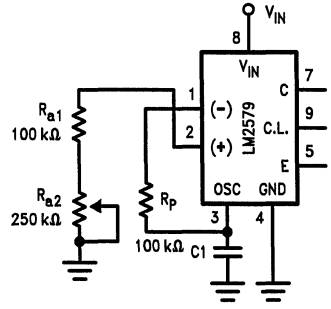
TL/H/10355–14

FIGURE 10. Maximum Duty Cycle Limiting

DUTY CYCLE ADJUSTMENT

When manual or mechanical selection of the output transistor's duty cycle is needed, the circuit shown in *Figure 11* may be used. The output will turn ON with the beginning of each oscillator cycle, and turn OFF when the current sunk by R_{a1} and R_{a2} from the non-inverting terminal becomes greater than the current sunk from the inverting terminal.

With the resistor values as shown, R_{a2} can be used to adjust the duty cycle from 0% to 90%. When the sum of R_{a1} and R_{a2} is twice the value of R_p, the duty cycle will be about 50%. C1 may be a large electrolytic capacitor, to lower the oscillator frequency below 1 Hz if appropriate for the application.



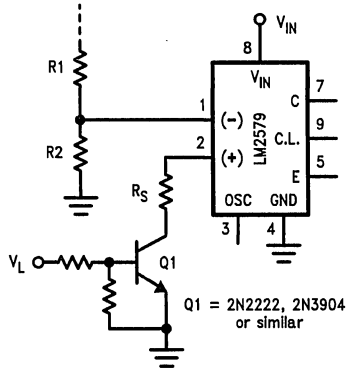
TL/H/10355–15

FIGURE 11. Duty Cycle Adjustment

REMOTE SHUTDOWN

The LM2579 may be remotely shut down by sinking a greater current from the non-inverting input than from the inverting input. This may be accomplished by selecting resistor R_S to be approximately one-half the value of the parallel combination of R1 and R2 (see *Figure 12*). Shutdown will occur when V_L is high.

Application Information (Continued)



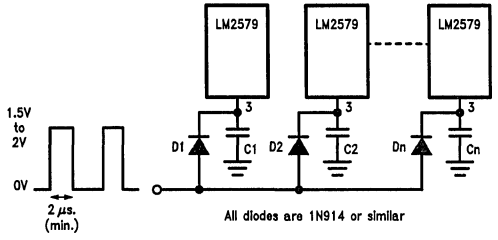
TL/H/10355–16

FIGURE 12. Remote Shutdown

SYNCHRONIZING DEVICES

When several devices are to be operated at once, their oscillators may be synchronized by the application of an external signal, as shown in *Figure 13*. This drive signal should be a pulse waveform with a minimum pulse width of 2 μs, and an amplitude of from 1.5V to 2.0V. The signal source must be capable of both driving capacitive loads and delivering up to 500 μA for each LM2579.

Capacitors C1 through Cn are to be selected for a 20% slower frequency than the synchronizing frequency.



TL/H/10355–17

FIGURE 13. Synchronizing Devices

IMPROVING TRANSISTOR SATURATION

The efficiency of a switching regulator is highest when the power transistor is allowed to fully saturate, minimizing the Collector-Emitter voltage when the transistor is ON. When the Collector is used as the output, with the Emitter grounded, the output transistor will fully saturate. Saturation voltage depends on the load current (see *Collector Saturation Voltage* curve), and is normally under 0.8V, over temperature.

However, when the Emitter is used as the output (Collector tied to V_{IN}, as in *Figure 14*), the output transistor cannot fully saturate because of the Darlington configuration of the output stage. This results in a 1.7V drop (typically) across the power device Q3 during the conduction period (refer to *Emitter Saturation Voltage* curve).

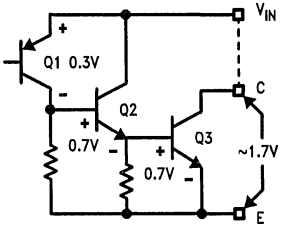


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FIGURE 14. Collector-Emitter Saturation Prevented by Darlington Construction of Output Stage (Simplified Schematic)

To achieve Collector-Emitter saturation, the base for the LM2579 output transistor Q3 must be driven higher than its Collector. This cannot happen if the Collector is tied to V_{IN}. However, by increasing V_{IN} to 1.5V or more above V_C, Collector-Emitter saturation can occur (see *Figure 15*). Techniques for accomplishing this are shown in the Typical Applications examples.

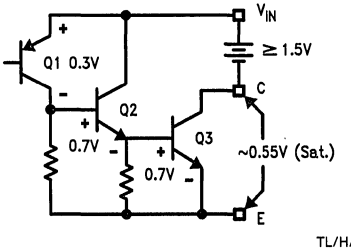

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FIGURE 15. Increasing V_{IN} Above V_C Allows Collector-Emitter Saturation

ADAPTING LM1578 DESIGNS TO THE LM2579

All LM1578 designs may be adapted for use with the LM2579 to achieve higher output power. The LM2579 is based on the design of the LM1578 switching regulator controller, with a few modifications. The output switching transistor is capable of delivering 3A (peak or DC), compared to the 0.75A maximum current rating of the LM1578, and the Emitter output can swing more negative than the ground terminal. Because of the difference in current rating, the LM2579 is in the TO-220 style package so it may be easily heat-sunk. Heat sinking is necessary for most LM2579 designs, especially those operating at high switch currents. For example, the loss of 3W in the output switch of a converter operating at 35°C ambient would raise the die temperature near its maximum rating of 150°C if no heat sink were used (see Note 3 in the Electrical Characteristics).

The other modification seen in the LM2579 is the 20 pF capacitor that is used, in LM1578 applications, to inject an end-of-cycle signal into the error comparator, improving synchronization of the switching to the oscillator. It is not necessary to add this capacitor in LM2579 applications.

Typical Applications

The LM2579 can be used in all standard configurations which require a single switching transistor. These include the buck (or step-down), boost (or step-up), invert, flyback, and forward styles.

Typical Applications (Continued)

Several design examples follow which include a variety of techniques to improve regulator performance.

Inductors having the standard values shown in the nomograph of *Figure 17* are available from Pulse Engineering (San Diego, CA); AIE Magnetics, division of Vernatron (St. Petersburg, FL); and Renco Electronics (Deer Park, NY).

BUCK REGULATOR

In the buck regulator of *Figure 16*, a 28V input is converted to 5V, with a load of up to 2.5A. Efficiency at maximum load is approximately 80%, and load regulation is approximately 0.05%/A in the range $0.3A \leq I_{LOAD} \leq 2.5A$. Switching frequency has been set to 40 kHz by the choice of 2 nF for C_1 (see *Figure 1*).

The value of the inductor, L, is determined by the use of the Inductance Calculator *(Figure 17),* or by the equation

$$L = V_O (V_{IN} - V_O) / (\Delta I_L V_{IN} f_{OSC})$$

where ΔI_L is the current ripple through the inductor. ΔI_L is usually chosen based on the minimum load current expected of the circuit: For the Buck regulator, since $I_L = I_{LOAD}$, ΔI_L is twice the minimum load current value $\Delta I_L = 350$ mA for this circuit, so operation will become discontinuous at $(\Delta I_{L(min)}/2)(100\%/I_{L(max)}) = 7\%$ of the maximum load current. (This is the "% Discontinuity" referred to in the Inductance Calculator.)

At this minimum value, the inductor current will just reach zero at the end of every switching period. Below the "minimum," the inductor will "run dry" and the regulator will be "discontinuous," as the inductor current is zero for part of each cycle. In this mode, the inductor is no longer storing energy, so is not an effective part of the output filter. Regulation will continue but performance will be degraded.

Output ripple voltage is about 40 mVpp when the output filter capacitor, C_2, is a standard 1000 μF electrolytic. Replacing this capacitor with a 1500 μF "low ESR" (equivalent series resistance) capacitor reduces the ripple to 20 mVpp. The minimum value of this capacitor can be determined by the following equation

$$C_2 \geq V_O (V_{IN} - V_O) / (8 V_{IN} V_{RIPPLE} L f_{OSC}^2)$$

where V_{RIPPLE} is the desired maximum output voltage ripple in peak-to-peak Volts. The ripple will be greater than predicted by this equation due to effects of ESR in C_2.

Figure 16 illustrates the single-point grounding and supply bypassing necessary for this type of moderate-to-high current switching regulator. For best regulation, all high-current paths, including ground, must be kept low-resistance.

***Note:** When pin 5, the Emitter of the LM2579 output transistor, is used to drive the output filter, it may oscillate when driven into positive saturation and when loaded with capacitance of between 100 pF and 500 pF. This capacitance is usually caused by socket capacitance, input capacitance of external components (such as the Schottky diode), and stray capacitance in the layout. The oscillation, which is usually near 30 MHz, can be eliminated by adding a series RC of 4.7Ω to 10Ω and 1 nF from the Emitter (pin 5) to Ground.

In the Emitter-driven configurations, the Collector output (pin 7) is normally tied to V_{IN} (pin 8). If this connection uses long lead lengths (greater than 3″ total), the Collector should be bypassed to V_{IN} with 0.01 μF (or greater), attached directly to the terminals. In addition, when current limiting is used, connections to the Current Limit pin (pin 9) should be made with short leads. Use of these techniques to minimize lead inductance will also minimize switching transients, thus reducing conducted noise.

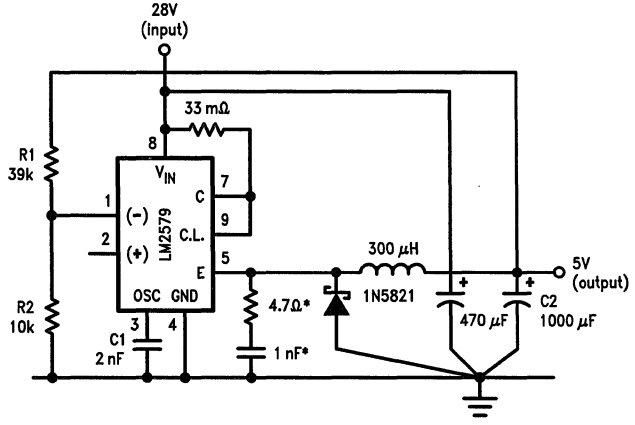

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FIGURE 16. Buck Converter: 28V to 5V at 2.5A

*Refer to Note in text.

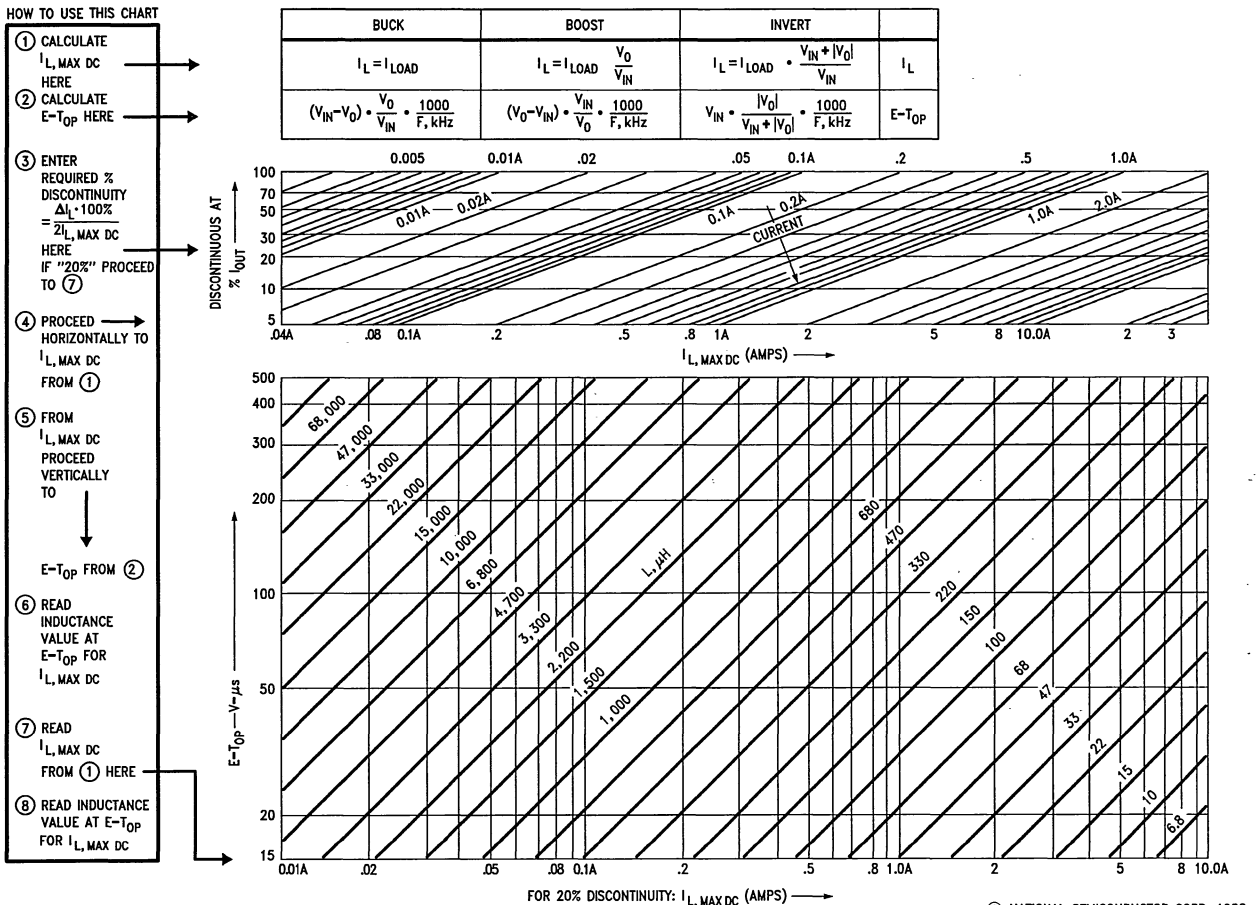

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FIGURE 17. DC/DC Inductance Calculator

Typical Applications (Continued)

BOOST REGULATOR

The boost converter of *Figure 18* produces 15V at up to 800 mA from a 5V input, with 82% efficiency. The output ripple (with an 800 mA load) is 100 mV when a standard 1000 μF electrolytic output capacitor is used, or 75 mV if a 1500 μF low-ESR electrolytic is used. The minimum value of C_2 may be calculated using the same equation as shown in the BUCK REGULATOR section.

The inductor value is selected either using the Inductance Calculator *(Figure 17),* or by the equation

$$L = V_{IN}^2 (V_O - V_{IN}) / (\Delta I_L V_O^2 f_{OSC})$$

where, as in the previous section, ΔI_L is determined by minimum expected DC inductor current. For the boost regulator,

$$\Delta I_L = 2 I_{LOAD(min)} (V_O/V_{IN})$$

Load regulation for this circuit is approximately 0.04%/A in the range 50 mA $\leq I_{LOAD} \leq$ 800 mA. Line regulation is 4 mV/V for the input range 4.5V $\leq V_{IN} \leq$ 8.5V.

Stability of the circuit is improved with the use of a series R-C network from the Current Limit pin to the Inverting Input.

INVERTING REGULATOR

The inverting regulator of *Figure 19* converts a 15V input to −15V at 1A. The load regulation is about 30 mV/A for the range 0.1A $\leq I_{LOAD} \leq$ 1.0A.

The inductor value is determined either by the Inductance Calculator *(Figure 17),* or by the equation

$$L = V_{IN}^2 |V_O| / [\Delta I_L (V_{IN} + |V_O|)^2 f_{OSC}]$$

where ΔI_L is based on minimum DC inductor current, and may be calculated as follows:

$$\Delta I_L = 2 I_{LOAD(min)} (V_{IN} + |V_O|) / V_{IN}$$

The output voltage ripple (at full load) is approximately 120 mVpp when C_2 is a 1000 μF standard electrolytic capacitor, or 60 mVpp when a 1500 μF low-ESR capacitor is used. The minimum value of C_2 may be calculated using the equation shown in the BUCK REGULATOR section.

The efficiency of this regulator is approximately 76%. To achieve higher efficiency, the circuit may be modified (as shown in *Figure 20*) to increase the supply voltage to the LM2579, which reduces the saturation voltage of the output transistor.

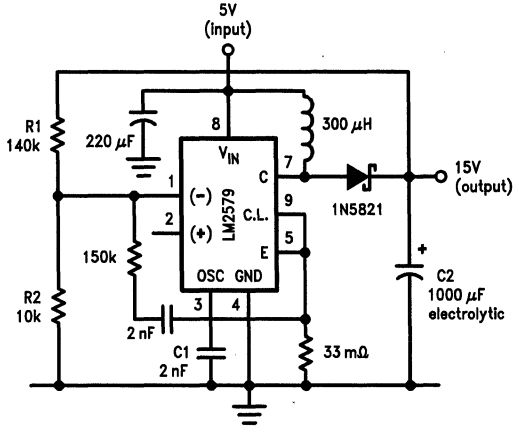

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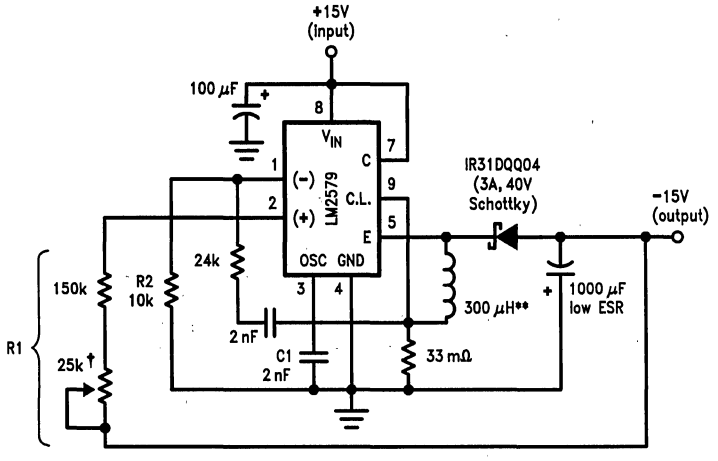
FIGURE 18. Boost Converter: 5V to 15V at 800 mA

Typical Applications (Continued)



TL/H/10355–23

†Output voltage trim
*Wire-wound resistor may be used here
**See text

FIGURE 19. Inverting Regulator: + 15V to − 15V at 1A

To improve circuit stability, a series R-C network is added from the Current Limit pin to the Inverting Input. In addition, an R-C damper may be required from the Emitter to Ground, as described in the BUCK REGULATOR section Note.

****Note:** The additional winding L_B shown in *Figure 20* is used to create a flyback effect which provides an extra 3V to the LM2579 supply voltage. In this example, the inductor L was 46 turns of 20-gauge wire on an Arnold 4F-068200-2 toroid core, providing 300 µH; booster winding L_B was 20 turns of #28 wire on the same core.

Regulator efficiency will be increased to about 86% with the boosted supply voltage, as this allows the saturation voltage of the output transistor to decrease to about 0.55V (from the typical Emitter saturation voltage of 1.7V).

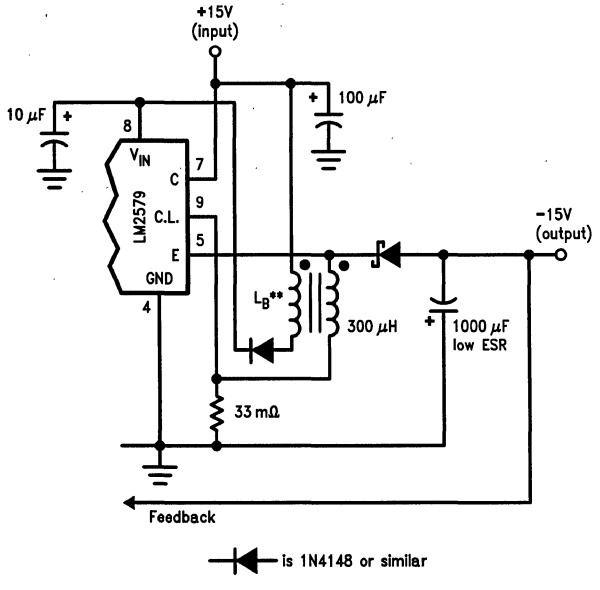


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FIGURE 20. Optional Modification to Inverting Regulator of *Figure 19* for Increased Efficiency

National Semiconductor

LM78S40
Universal Switching Regulator Subsystem

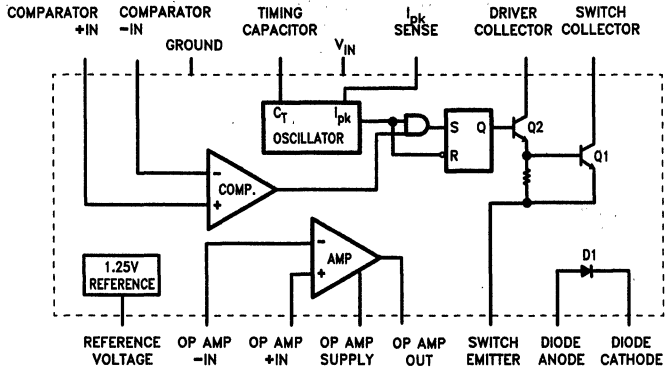
General Description

The LM78S40 is a monolithic regulator subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high current, high voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external NPN or PNP transistors when currents in excess of 1.5A or voltages in excess of 40V are required. The device can be used for step-down, step-up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part count switching system and works extremely well in battery operated systems.

Features

- Step-up, step-down or inverting switching regulators
- Output adjustable from 1.25V to 40V
- Peak currents to 1.5A without external transistors
- Operation from 2.5V to 40V input
- Low standby current drain
- 80 dB line and load regulation
- High gain, high current, independent op amp
- Pulse width modulation with no double pulsing

Block and Connection Diagrams



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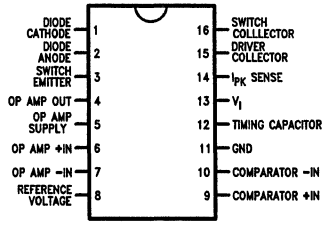
16-Lead DIP



TL/H/10057–1

Top View

Ordering Information

Device Code	Package Code	Package Description
LM78S40J	J16A	Ceramic DIP
LM78S40N	N16A	Molded DIP
LM78S40CJ	J16A	Ceramic DIP
LM78S40CN	N16A	Molded DIP

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Operating Temperature Range
- Extended (LM78S40J): −55°C to +125°C
- Industrial (LM78S40N): −40°C to +125°C
- Commercial (LM78S40CN): 0°C to +70°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 16L-Ceramic DIP: 1.50W
- 16L-Molded DIP: 1.04W

Input Voltage from V^+ to V^-: 40V

Input Voltage from V^+ Op Amp to V^-: 40V

Common Mode Input Range (Error Amplifier and Op Amp): −0.3 to V+

Differential Input Voltage (Note 3): ±30V

Output Short Circuit Duration (Op Amp): Continuous

Current from V_{REF}: 10 mA

voltage from Switch Collectors to GND: 40V

Voltage from Switch Emitters to GND: 40V

Voltage from Switch Collectors to Emitter: 40V

Voltage from Power Diode to GND: 40V

Reverse Power Diode Voltage: 40V

Current through Power Switch: 1.5A

Current through Power Diode: 1.5A

ESD Susceptibility: (to be determined)

LM78S40
Electrical Characteristics

T_A = Operating temperature range, V_I = 5.0V, $V_{Op\ Amp}$ = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
GENERAL CHARACTERISTICS							
I_{CC}	Supply Current (Op Amp Disconnected)	V_I = 5.0V			1.8	3.5	mA
		V_I = 40V			2.3	5.0	mA
I_{CC}	Supply Current (Op Amp Connected)	V_I = 5.0V				4.0	mA
		V_I = 40V				5.5	mA
REFERENCE SECTION							
V_{REF}	Reference Voltage (Note 4)	I_{REF} = 1.0 mA	Extend −55°C < T_A < +125°C, Comm 0 < T_A < +70°C, Indus −40°C < T_A < +85°C	1.180	1.245	1.310	V
$V_{R\ LINE}$	Reference Voltage Line Regulation	V_I = 3.0V to V_I = 40V, I_{REF} = 1.0 mA, T_A = 25°C			0.04	0.2	mV/V
$V_{R\ LOAD}$	Reference Voltage Load Regulation	I_{REF} = 1.0 mA to I_{REF} = 10 mA, T_A = 25°C			0.2	0.5	mV/mA
OSCILLATOR SECTION							
I_{CHG}	Charging Current	V_I = 5.0V, T_A = 25°C		20		50	μA
I_{CHG}	Charging Current	V_I = 40V, T_A = 25°C		20		70	μA
I_{DISCHG}	Discharge Current	V_I = 5.0V, T_A = 25°C		150		250	μA
I_{DISCHG}	Discharge Current	V_I = 40V, T_A = 25°C		150		350	μA
V_{OSC}	Oscillator Voltage Swing	V_I = 5.0V, T_A = 25°C			0.5		V
t_{on}/t_{off}	Ratio of Charge/ Discharge Time				6.0		μs/μs

LM78S40

Electrical Characteristics (Continued)

T_A = Operating Temperature Range, V_I = 5.0V, $V_{Op\ Amp}$ = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CURRENT LIMIT SECTION						
V_{CLS}	Current Limit Sense Voltage	T_A = 25°C	250		350	mV
OUTPUT SWITCH SECTION						
$V_{SAT\ 1}$	Output Saturation Voltage 1	I_{SW} = 1.0A *(Figure 1)*		1.1	1.3	V
$V_{SAT\ 2}$	Output Saturation Voltage 2	I_{SW} = 1.0A *(Figure 2)*		0.45	0.7	V
h_{FE}	Output Transistor Current Gain	I_C = 1.0A, V_{CE} = 5.0V, T_A = 25°C		70		
I_L	Output Leakage Current	V_O = 40V, T_A = 25°C		10		nA
POWER DIODE						
V_{FD}	Forward Voltage Drop	I_D = 1.0A		1.25	1.5	V
I_{DR}	Diode Leakage Current	V_D = 40V, T_A = 25°C		10		nA
COMPARATOR						
V_{IO}	Input Offset Voltage	$V_{CM} = V_{REF}$		1.5	15	mV
I_{IB}	Input Bias Current	$V_{CM} = V_{REF}$		35	200	nA
I_{IO}	Input Offset Current	$V_{CM} = V_{REF}$		5.0	75	nA
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		V1−2	V
PSRR	Power Supply Rejection Ratio	V_I = 3.0V to 40V, T_A = 25°C	70	96		dB
OUTPUT OPERATIONAL AMPLIFIER						
V_{IO}	Input Offset Voltage	V_{CM} = 2.5V		4.0	15	mV
I_{IB}	Input Bias Current	V_{CM} = 2.5V		30	200	nA
I_{IO}	Input Offset Current	V_{CM} = 2.5V		5.0	75	nA
A_{VS}^+	Voltage Gain+	R_L = 2.0 kΩ to GND; V_O = 1.0V to 2.5V, T_A = 25°C	25	250		V/mV
A_{VS}^-	Voltage Gain−	R_L = 2.0 kΩ to V^+ (Op Amp) V_O = 1.0V to 2.5V, T_A = 25°C	25	250		V/mV
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		V_{CC} − 2	V
CMR	Common Mode Rejection	V_{CM} = 0V to 3.0V, T_A = 25°C	76	100		dB
PSRR	Power Supply Rejection Ratio	V^+ Op Amp = 3.0V to 40V, T_A = 25°C	76	100		dB
I_O^+	Output Source Current	T_A = 25°C	75	150		mA
I_O^-	Output Sink Current	T_A = 25°C	10	35		mA
SR	Slew Rate	T_A = 25°C		0.6		V/μs
V_{OL}	Output Voltage LOW	I_L = −5.0 mA, T_A = 25°C			1.0	V
V_{OH}	Output Voltage High	I_L = 50 mA, T_A = 25°C	V + Op Amp − 3V			V

Note 1: $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.

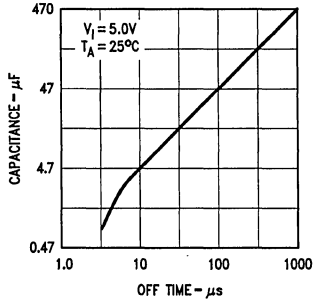
Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Note 3: For supply voltages less than 30V, the absolute maximum voltage is equal to the supply voltage.

Note 4: Selected devices with tightened tolerance reference voltage available.

Typical Performance Characteristics

Capacitance vs OFF Time



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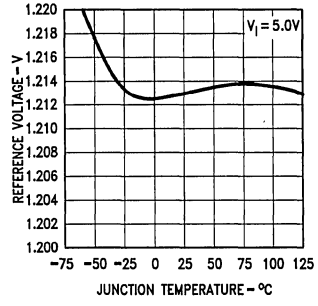
Reference Voltage vs Junction Temperature



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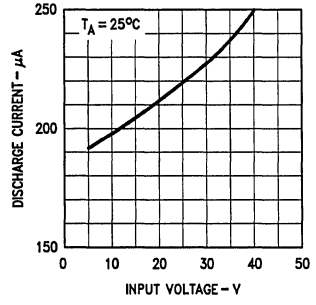
Discharge Current vs Input Voltage



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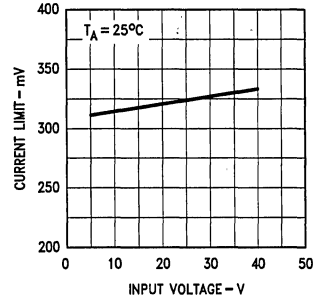
Current Limit Sense Voltage vs Input Voltage



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Design Formulas

Characteristic	Step-Down	Step-Up	Inverting	Units
$\frac{t_{on}}{t_{off}}$	$\frac{V_O + V_D}{V_I - V_{SAT} - V_O}$	$\frac{V_O + V_D - V_I}{V_I - V_{SAT}}$	$\frac{\lvert V_O \rvert + V_D}{V_I - V_{SAT}}$	
$(t_{on} + t_{off})$ Max	$\frac{1}{f_{Min}}$	$\frac{1}{f_{Min}}$	$\frac{1}{f_{MIN}}$	μs
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	μF
I_{pk}	$2\, I_{O\,Max}$	$2\, I_{O\,Max} \bullet \frac{t_{on} + t_{off}}{t_{off}}$	$2\, I_{O\,Max} \bullet \frac{t_{on} + t_{off}}{t_{off}}$	A
L_{Min}	$\left(\frac{V_I - V_{SAT} - V_O}{I_{pk}}\right) t_{on\,Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\,Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\,Max}$	μH
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$	Ω
C_O	$\frac{I_{pk}\,(t_{on} + t_{off})}{8\, V_{ripple}}$	$\approx \frac{I_O}{V_{ripple}} \bullet t_{on}$	$\approx \frac{I_O}{V_{ripple}} \bullet t_{on}$	μF

Note: V_{SAT} = Saturation voltage of the switching element.
V_D = Forward voltage of the flyback diode.

Functional Description

The LM78S40 is a variable frequency, variable duty cycle device. The initial switching frequency is set by the timing capacitor (Note 1). The initial duty cycle is 6:1. This switching frequency and duty cycle can be modified by two mechanisms—the current limit circuitry ($I_{pk\ sense}$) and the comparator.

The comparator modifies the OFF time. When the output voltage is correct, the comparator output is in the HIGH state and has no effect on the circuit operation. If the output voltage is too high then the comparator output goes LOW. In the LOW state the comparator inhibits the turn-on of the output stage switching transistors. As long as the comparator is LOW the system is in OFF time. As the output current rises the OFF time decreases. As the output current nears its maximum the OFF time approaches its minimum value. The comparator can inhibit several ON cycles, one ON cycle or any portion of an ON cycle. Once the ON cycle has begun the comparator cannot inhibit until the beginning of the next ON cycle.

The current limit modifies the ON time. The current limit is activated when a 300 mV potential appears between lead 13 (V_{CC}) and lead 14 (I_{pk}). This potential is intended to result when designed for peak current flows through R_{SC}. When the peak current is reached the current limit is turned on. The current limit circuitry provides for a quick end to ON time and the immediate start of OFF time.

Generally the oscillator is free running but the current limit action tends to reset the timing cycle.

Increasing load results in more current limited ON time and less OFF time. The switching frequency increases with load current.

V_{FD} is the forward voltage drop across the internal power diode. It is listed on the data sheet as 1.25V typical, 1.5V maximum. If an external diode is used, then its own forward voltage drop must be used for V_{FD}.

V_{SAT} is the voltage across the switch element (output transistors Q1 and Q2) when the switch is closed or ON. This is listed on the data sheet as output saturation voltage.

Output saturation voltage 1—defined as the switching element voltage for Q2 and Q1 in the Darlington configuration with collectors tied together. This applies to *Figure 1*, the step down mode.

Output saturation voltage 2—switching element voltage for Q1 only when used as a transistor switch. This applies to *Figure 2*, the step up mode.

For the inverting mode, *Figure 3*, the saturation voltage of the external transistor should be used for V_{SAT}.

Note 1: Oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to 100 kHz.

Typical Applications

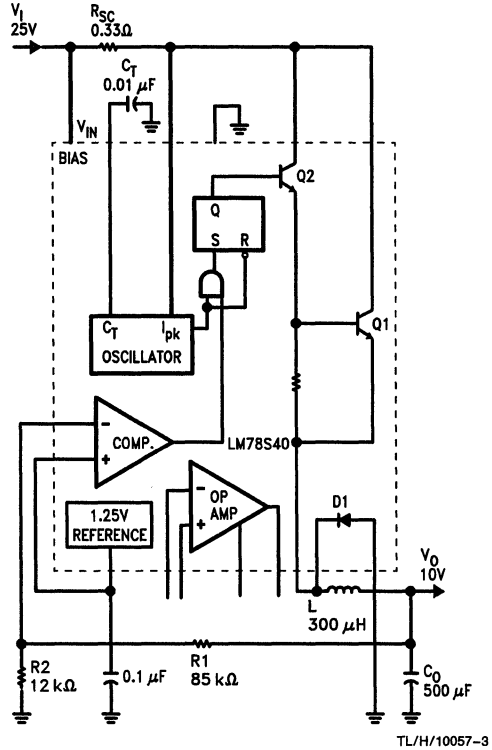

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FIGURE 1. Typical Step-Down Operational Performance (T_A = 25°C)

Characteristic	Condition	Typical Value
Output Voltage	I_O = 200 mA	10V
Line Regulation	20V ≤ V_I ≤ 30V	1.5 mV
Load Regulation	5.0 mA ≤ I_O ≤ 300 mA	3.0 mV
Max Output Current	V_O = 9.5V	500 mA
Output Ripple	I_O = 200 mA	50 mV
Efficiency	I_O = 200 mA	74%
Standby Current	I_O = 200 mA	2.8 mA

Note A: For I_O ≥ 200 mA use external diode to limit on-chip power dissipation.

Note B: It is recommended that the internal reference (lead 8) be bypassed by a 0.1 μF capacitor directly to (lead 11) the ground point of the LM78S40.

Typical Applications (Continued)

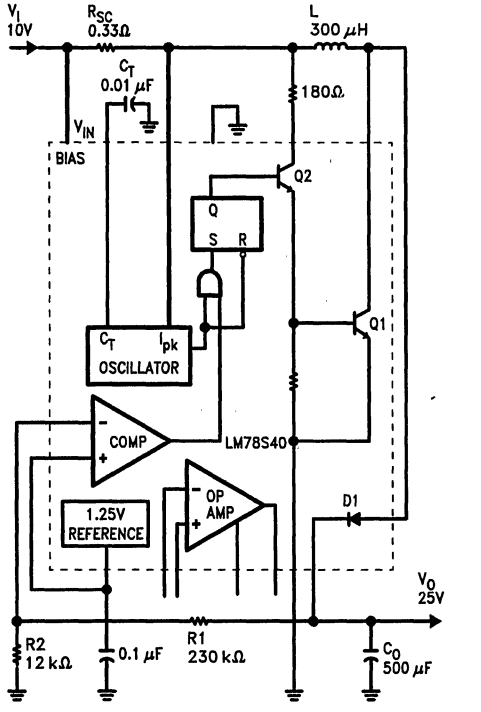

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FIGURE 2. Typical Step-Up Operational Performance (T_A = 25°C)

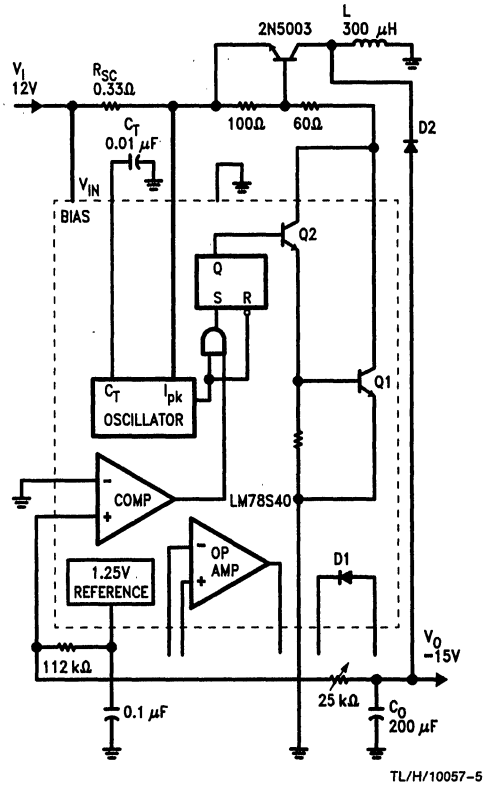

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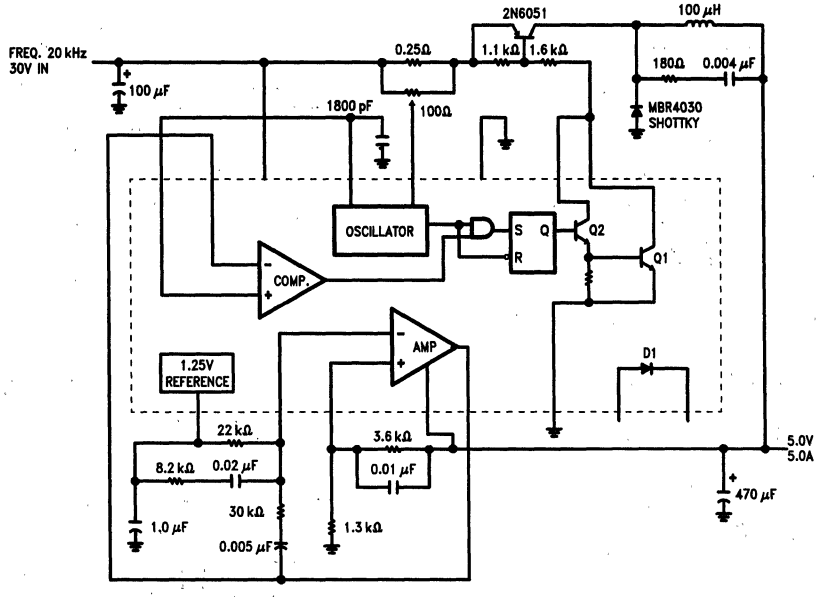
FIGURE 3. Typical Inversion Operational Performance (T_A = 25°C)

Characteristic	Condition	Typical Value
Output Voltage	I_O = 50 mA	25V
Line Regulation	5.0V ≤ V_I ≤ 15V	4.0 mV
Load Regulation	5.0 mA ≤ I_O I_O ≤ 100 mA	2.0 mV
Max Output Current	V_O = 23.75V	160 mA
Output Ripple	I_O = 50 mA	30 mV
Efficiency	I_O = 50 mA	79%
Standby Current	I_O = 50 mA	2.6 mA

Characteristic	Condition	Typical Value
Output Voltage	I_O = 100 mA	−15V
Line Regulation	8.0V ≤ V_I ≤ 18V	5.0 mV
Load Regulation	5.0 mA ≤ I_O I_O ≤ 150 mA	3.0 mV
Max Output Current	V_O = 14.25V	160 mA
Output Ripple	I_O = 100 mA	20 mV
Efficiency	I_O = 100 mA	70%
Standby Current	I_O = 100 mA	2.3 mA

Typical Applications (Continued)



TL/H/10057–10

FIGURE 4. Pulse Width Modulator

National Semiconductor

LMC7660 Switched Capacitor Voltage Converter

General Description

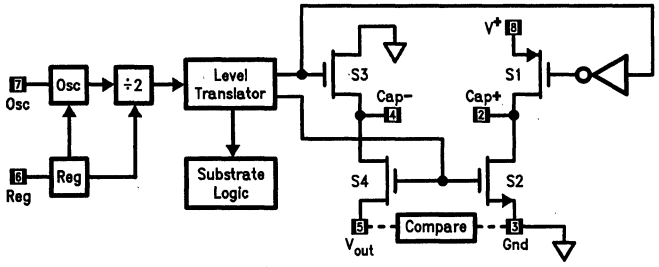
The LMC7660 is a CMOS voltage converter capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage of −1.5V to −10V. The LMC7660 is a pin-for-pin replacement for the industry-standard 7660. The converter features: operation over full temperature and voltage range without need for an external diode, low quiescent current, and high power efficiency.

The LMC7660 uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolytic capacitors.

Features

- Operation over full temperature and voltage range without an external diode
- Low supply current, 200 μA max
- Pin-for-pin replacement for the 7660
- Wide operating range 1.5V to 10V
- 97% Voltage Conversion Efficiency
- 95% Power Conversion Efficiency
- Easy to use, only 2 external components
- Extended temperature range

Block Diagram



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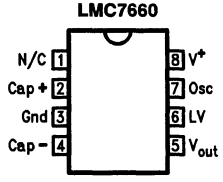
Pin Configuration



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Ordering Information

LMC7660MJ $-55°C \leq T_A \leq +125°C$

LMC7660IN $-40°C \leq T_A \leq +85°C$

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	10.5V
Input Voltage on Pin 6, 7 (Note 2)	−0.3V to (V^+ + 0.3V) for V^+ < 5.5V (V^+ − 5.5V) to (V^+ + 0.3V) for V^+ > 5.5V
Current into Pin 6 (Note 2)	20 μA
Output Short Circuit Duration ($V^+ \leq 5.5V$)	Continuous

	Package J	Package N
Power Dissipation (Note 3)	0.9W	1.4W
T_j Max (Note 3)	150°C	150°C
θ_{ja} (Note 3)	140°C/W	90°C/W
Storage Temp. Range	−65°C ≤ T ≤ 150°C	
Lead Temp. (Soldering, 5 sec)	260°C	260°C
ESD Tolerance (Note 8)		±2000V

Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Typ	LMC7660MJ Tested Limit (Note 5)	LMC7660IN Tested Limit (Note 5)	LMC7660IN Design Limit (Note 6)	Units Limits
I_s	Supply Current	$R_L = \infty$	120	200 **400**	200	**400**	μA max
V^+_H	Supply Voltage Range High (Note 7)	R_L = 10 kΩ, Pin 6 Open Voltage Efficiency ≥ 90%	3 to 10	**3 to 10**	3 to 10	**3 to 10**	V
V^+_L	Supply Voltage Range Low	R_L = 10 kΩ, Pin 6 to Gnd. Voltage Efficiency ≥ 90%	1.5 to 3.5	**1.5 to 3.5**	1.5 to 3.5	**1.5 to 3.5**	V
R_{out}	Output Source Resistance	I_L = 20 mA	55	100 **150**	100	**120**	Ω max
		V = 2V, I_L = 3 mA Pin 6 Short to Gnd.	110	200 **300**	200	**300**	Ω max
F_{osc}	Oscillator Frequency		10				kHz
P_{eff}	Power Efficiency	R_L = 5 kΩ	97	95 **90**	95	**90**	% min
$V_{o\,eff}$	Voltage Conversion Efficiency	$R_L = \infty$	99.9	97 **95**	97	**95**	% min
I_{osc}	Oscillator Sink or Source Current	Pin 7 = Gnd. or V^+	3				μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 4 for conditions.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power-up" of the LMC7660.

Note 3: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{ja} and T_j max, $T_j = T_A + \theta_{ja} P_D$.

Note 4: Boldface numbers apply at temperature extremes. All other numbers apply at T_A = 25°C, V^+ = 5V, C_{osc} = 0, and apply for the LMC7660 unless otherwise specified. Test circuit is shown in *Figure 1*.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed over the operating temperature range (but not 100% tested). These limits are not used to calculate outgoing quality levels.

Note 7: The LMC7660 can operate without an external diode over the full temperature and voltage range. The LMC7660 can also be used with the external diode Dx, when replacing previous 7660 designs.

Note 8: The test circuit consists of the human body model of 100 pF in series with 1500Ω.

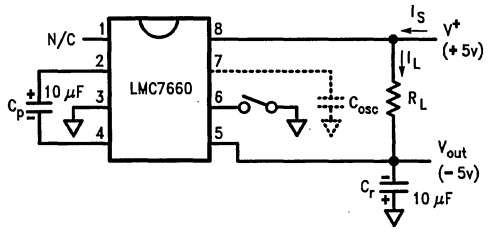

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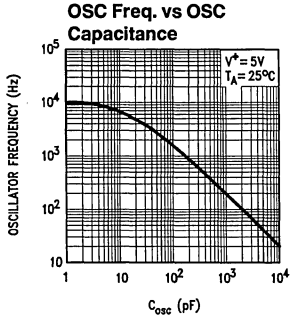
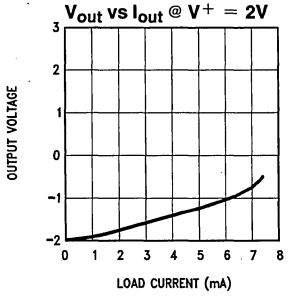
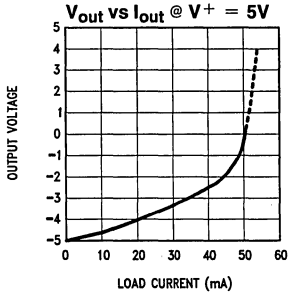
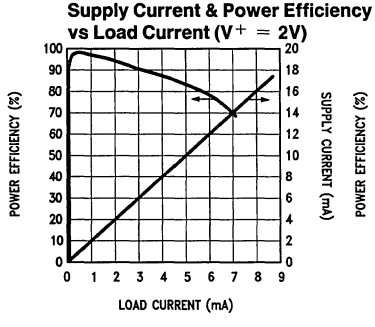
FIGURE 1. LMC7660 Test Circuit

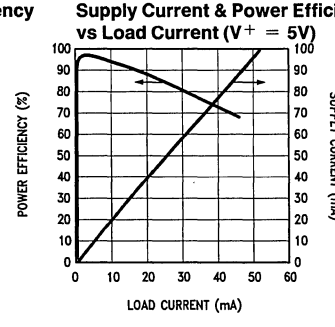
Typical Performance Characteristics

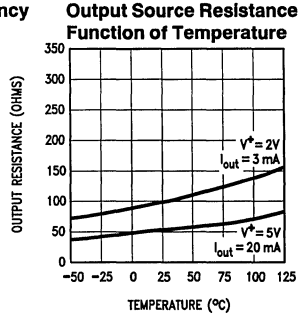


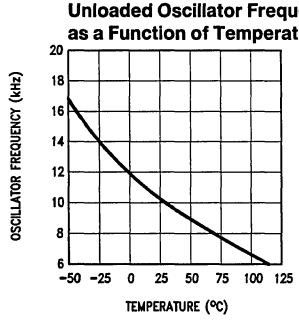


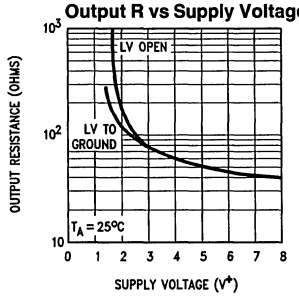


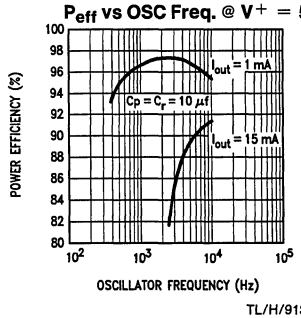












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CIRCUIT DESCRIPTION

The LMC7660 contains four large CMOS switches which are switched in a sequence to provide supply inversion $V_{out} = -V_{in}$. Energy transfer and storage are provided by two inexpensive electrolytic capacitors. *Figure 2* shows how the LMC7660 can be used to generate $-V^+$ from V^+. When switches S1 and S3 are closed, C_p charges to the supply voltage V^+. During this time interval, switches S2 and S4 are open. After C_p charges to V^+, S1 and S3 are opened, S2 and S4 are then closed. By connecting S2 to ground, C_p develops a voltage $-V^+/2$ on C_r. After a number of cycles C_r will be pumped to exactly $-V^+$. This transfer will be exact assuming no load on C_r, and no loss in the switches.

In the circuit of *Figure 2*, S1 is a P-channel device and S2, S3, and S4 are N-channel devices. Because the output is biased below ground, it is important that the p^- wells of S3 and S4 never become forward biased with respect to either their sources or drains. A substrate logic circuit guarantees that these p^- wells are always held at the proper voltage. Under all conditions S4 p^- well must be at the lowest potential in the circuit. To switch off S4, a level translator generates $V_{GS4} = 0V$, and this is accomplished by biasing the level translator from the S4 p^- well.

An internal RC oscillator and ÷ 2 circuit provide timing signals to the level translator. The built-in regulator biases the oscillator and divider to reduce power dissipation on high supply voltage. The regulator becomes active at about $V^+ = 6.5V$. Low voltage operation can be improved if the LV pin is shorted to ground for $V^+ \leq 3.5V$. For $V^+ \geq 3.5V$, the LV pin must be left open to prevent damage to the part.

POWER EFFICIENCY AND RIPPLE

It is theoretically possible to approach 100% efficiency if the following conditions are met:

1) The drive circuitry consumes little power.
2) The power switches are matched and have low R_{on}.
3) The impedance of the reservoir and pump capacitors are negligibly small at the pumping frequency.

The LMC7660 closely approaches 1 and 2 above. By using a large pump capacitor C_p, the charge removed while supplying the reservoir capacitor is small compared to C_p's total charge. Small removed charge means small changes in the pump capacitor voltage, and thus small energy loss and high efficiency. The energy loss by C_p is:

$$E = \tfrac{1}{2}C_p (V1^2 - V2^2)$$

By using a large reservoir capacitor, the output ripple can be reduced to an acceptable level. For example, if the load current is 5 mA and the accepted ripple is 200 mV, then the reservoir capacitor can omit approximately be calculated from:

$$Is = C_r \frac{dv}{dt}$$

$$\sim C_r \times \frac{V_{ripple\ p\text{-}p}}{4/F_{osc}} \qquad C_r = \frac{0.5\ mA}{0.5V/ms} = 10\ \mu F$$

PRECAUTIONS

1) Do not exceed the maximum supply voltage or junction temperature.
2) Do not short pin 6 (LV terminal) to ground for supply voltages greater than 3.5V.
3) Do not short circuit the output to V^+.
4) External electrolytic capacitors C_r and C_p should have their polarities connected as shown in *Figure 1*.

REPLACING PREVIOUS 7660 DESIGNS

To prevent destructive latchup, previous 7660 designs require a diode in series with the output when operated at elevated temperature or supply voltage. Although this prevented the latchup problem of these designs, it lowered the available output voltage and increased the output series resistance.

The National LMC7660 has been designed to solve the inherent latch problem. The LCM7660 can operate over the

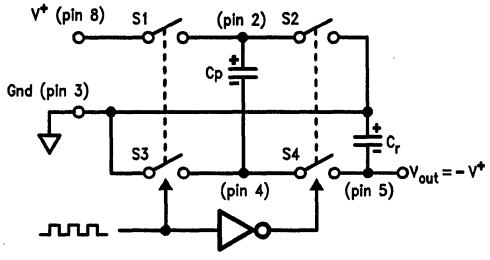

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FIGURE 2. Idealized Voltage Converter

entire supply voltage and temperature range without the need for an output diode. When replacing existing designs, the LMC7660 can be operated with diode Dx.

Typical Applications

Changing Oscillator Frequency

It is possible to dramatically reduce the quiescent operating current of the LMC7660 by lowering the oscillator frequency. The oscillator frequency can be lowered from a nominal 10 kHz to several hundred hertz, by adding a slow-down capacitor C_{osc} *(Figure 3)*. As shown in the Typical Performance Curves the supply current can be lowered to the 10 μA range. This low current drain can be extremely useful when used in μPower and battery back-up equipment. It must be understood that the lower operating frequency and supply current cause an increased impedance of C_r and C_p. The increased impedance, due to a lower switching rate, can be offset by raising C_r and C_p until ripple and load current requirements are met.

Synchronizing to an External Clock

Figure 4 shows an LMC7660 synchronized to an external clock. The CMOS gate overrides the internal oscillator when it is necessary to switch faster or reduce power supply interference. The external clock still passes through the ÷2 circuit in the 7660, so the pumping frequency will be ½ the external clock frequency.

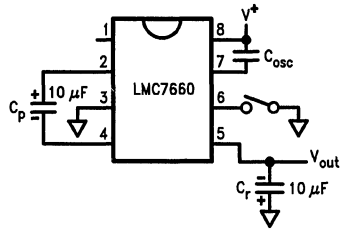

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FIGURE 3. Reduce Supply Current by Lowering Oscillator Frequency

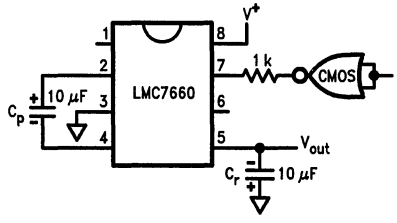

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FIGURE 4. Synchronizing to an External Clock

Typical Applications (Continued)

Lowering Output Impedance

Paralleling two or more LMC7660's lowers output impedance. Each device must have it's own pumping capacitor C_p, but the reservoir capacitor C_r is shared as depicted in *Figure 5*. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of one LMC7660}}{\text{Number of devices}}$$

Increasing Output Voltage

Stacking the LMC7660s is an easy way to produce a greater negative voltage. It should be noted that the input current required for each stage is twice the load current on that stage as shown in *Figure 6A*. The effective output resistance is approximately the sum of the individual R_{out} values, and so only a few levels of multiplication can be used.

It is possible to generate −15V from +5V by connecting the second 7660's pin 8 to +5V instead of ground as shown in *Figure 6B*. Note that the second 7660 sees a full 20V and the input supply should not be increased beyond +5V.

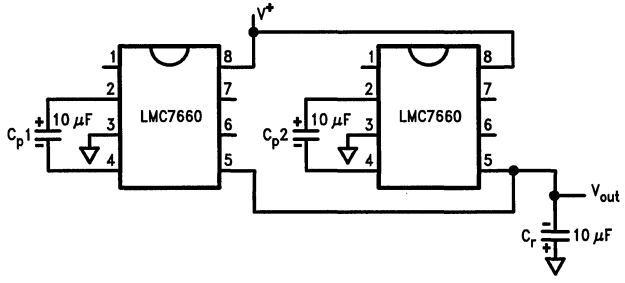

FIGURE 5. Lowering Output Resistance by Paralleling Devices

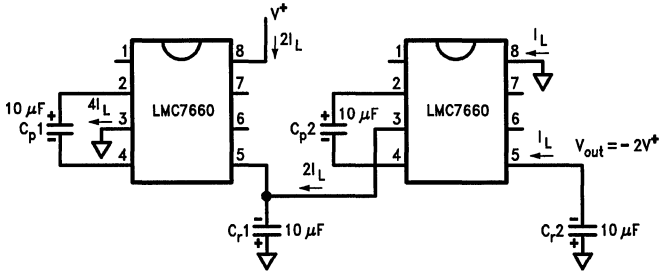

FIGURE 6A. Higher Voltage by Cascade

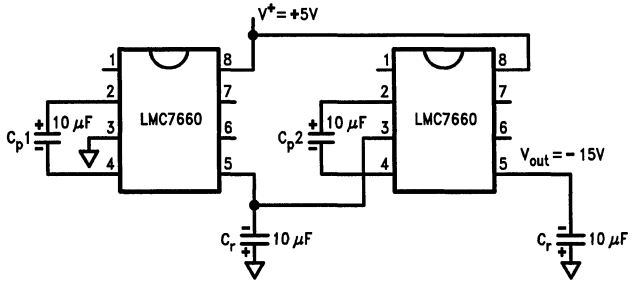

FIGURE 6B. Getting −15V from +5V

Typical Applications (Continued)

Split V^+ In Half

Figure 7 is one of the more interesting applications for the LMC7660. The circuit can be used as a precision voltage divider (for very light loads), alternately it is used to generate a ½ supply point in battery applications. In the ½ cycle when S1 and S3 are closed, the supply voltage divides across the capacitors in a conventional way proportional to their value. In the ½ cycle when S2 and S4 are closed, the capacitors switch from a series connection to a parallel connection. This forces the capacitors to have the same voltage; the charge redistributes to maintain precisely $V^+/2$, across C_p and C_r. In this application all devices are only $V^+/2$, and the supply voltage can be raised to 20V giving exactly 10V at V_{out}.

Getting Up . . . and Down

The LMC7660 can also be used as a positive voltage multiplier. This application, shown in *Figure 8*, requires 2 additional diodes. During the first ½ cycle S2 charges C_p1 through D1; D2 is reverse biased. In the next ½ cycle S2 is open and S1 is closed. Since C_p1 is charged to $V^+ - V_{D1}$ and is referenced to V^+ through S1, the junction of D1 and D2 is at $V^+ + (V^+ - V_{D1})$. D1 is reverse biased in this interval. This application uses only two of the four switches in the 7660. The other two switches can be put to use in performing a negative conversion at the same time as shown in *Figure 9*. In the ½ cycle that D1 is charging C_p1, C_p2 is connected from ground to $-V_{out}$ via S2 and S4, and C_r2 is storing C_p2's charge. In the interval that S1 and S3 are closed, C_p1 pumps the junction of D1 and D2 above V^+, while C_p2 is refreshed from V^+.

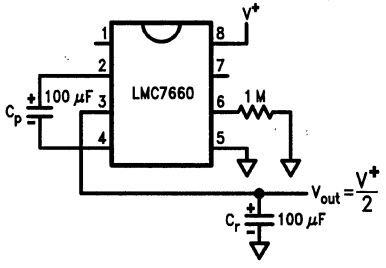

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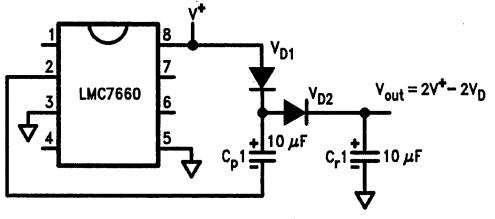
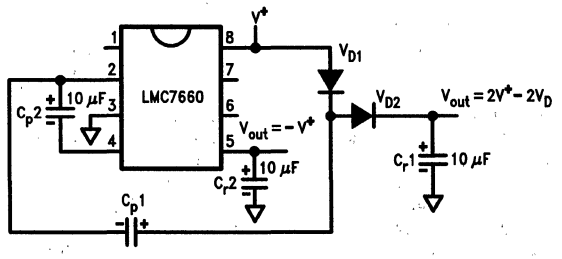
FIGURE 7. Split V^+ in Half



TL/H/9136–13

FIGURE 8. Positive Voltage Multiplier

Typical Applications (Continued)



TL/H/9136–14

FIGURE 9. Combined Negative Converter and Positive Multiplier

Thermometer Spans 180°C

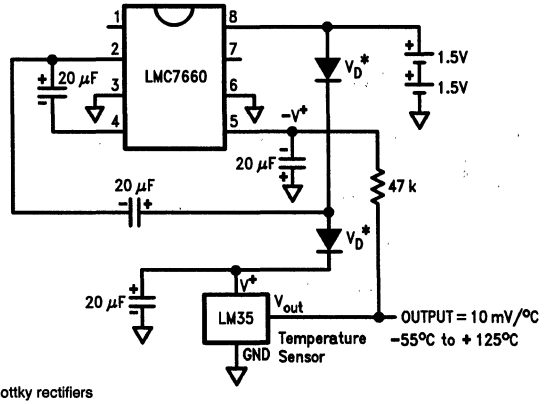
Using the combined negative and positive multiplier of *Figure 10* with an LM35 it is possible to make a µPower thermometer that spans a 180°C temperature range. The LM35 temperature sensor has an output sensitivity of 10 mV/°C, while drawing only 50 µA of quiescent current. In order for the LM35 to measure negative temperatures, a pull down to a negative voltage is required. *Figure 10* shows a thermometer circuit for measuring temperatures from −55°C to +125°C and requiring only two 1.5V cells. End of battery life can be extended by replacing the up converter diodes with Schottky's.

Regulating $-V_{out}$

It is possible to regulate the output of the LMC7660 and still maintain µPower performance. This is done by enclosing the LMC7660 in a loop with a LP2951. The circuit of *Figure 11* will regulate V_{out} to −5V for I_L = 10 mA, and V_{in} = 6V. For V_{in} > 7V, the output stays in regulation up to I_L = 25 mA. The error flag on pin 5 of the LP2951 sets low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high; the LMC7660 can be shutdown by shorting pin 7 and pin 8.

The LP2951 can be reconfigured to an adjustable type regulator, which means the LMC7660 can give a regulated output from −2.0V to −10V dependent on the resistor ratios R1 and R2, as shown in *Figure 12*, V_{ref} = 1.235V:

$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$



*For lower voltage operation, use Schottky rectifiers

TL/H/9136–15

FIGURE 10. µPower Thermometer Spans 180°C, and Pulls Only 150 µA

Typical Applications (Continued)

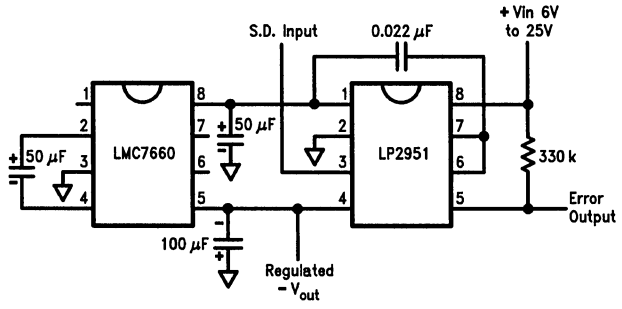


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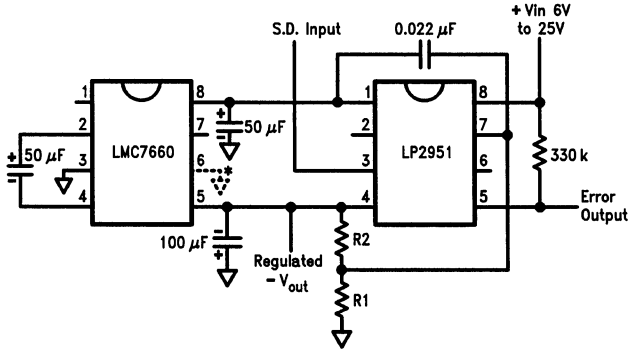
FIGURE 11. Regulated −5V with 200 μA Standby Current



$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$

$V_{ref} = 1.235V$

*Low voltage operation

TL/H/9136–17

FIGURE 12. LMC7660 and LP2951 Make a Negative Adjustable Regulator

Section 3

Operational Amplifiers

Section 3 Contents

Section 3 Contents (Continued)

Section 3 Contents (Continued)

National Semiconductor

Operational Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

General Purpose Operational Amplifier Selection Guide

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage Min V	Supply Voltage Max V	Special Features
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (Note 1)								
LH0044A	0.025	15	0.4	0.06	3	±2	±20	Low Noise
LM607A	0.025	2	1.8	0.7	1.5	±3	±18	Improved OP-07
LH0044	0.05	30	0.4	0.06	4	±2	±20	Low Noise
LM607B	0.06	3	1.8	0.7	1.5	±3	±18	Improved OP-07
LM11	0.3	0.05	0.8	0.3	0.6	±2.5	±20	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LH2108A	0.5	2	1	0.3	1.2	±2	±20	Dual LM108A
LM108A	0.5	2	1	0.3	0.4	±2	±20	
LH0052	0.5	0.003	1	3	3.5	±5	±22	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LH0004	1	100	10	*	0.15	±5	±45	
LM604A	1	40	7	2	8	4	36	Multiplexed Op Amp
LH2101A	2	75	1	0.5	5	±3	±22	Dual LM101A
LF155A	2	0.05	2.5	5	4	±5	±22	
LF156A	2	0.05	5	12	7	±5	±22	
LF157A	2	0.05	25	50	7	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±18	
LMC660A	2	0.02	1.5	1.7	2.2	5	15	Quad CMOS
LM10	2	20	0.09	0.1	0.4	±0.6	±22.5	Op Amp + Reference
LM101A	2	75	1	0.5	3	±3	±22	
LM107	2	75	1	0.5	3	±3	±22	Compensated LM101A
LM108	2	2	1	0.3	0.4	±2	±20	
LM112	2	2	1	0.2	0.6	±2	±20	Compensated LM108
LM124A	2	50	1	0.5	3	3	32	Quad
LM158A	2	50	1	0.5	1.2	3	32	Dual
LP124	2	4	0.1	0.05	0.13	3	32	Quad
LH0020	2.5	250	*	*	5	±5	±22	
LF412	3	0.2	4	15	6.8	±6	±18	Dual
LM741A	3	80	1.5	0.7	2.8	±3	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (continued)								
LH0022	4	0.01	1	3	2.5	±5	±22	
LF155	5	0.1	2.5	5	4	±5	±22	
LF156	5	0.1	5	12	7	±5	±22	
LF157	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LF147	5	0.2	4	13	11	±6	±22	Quad
LF442	5	0.1	1	1	0.5	±6	±18	Dual
LF444A	5	0.1	1	1	0.80	±6	±22	Quad
LH0086	5	0.5	3	10	15.5	±8	±18	Programmable Gain OA
LM124	5	150	1	0.5	3	3	32	Quad
LM143	5	20	1	2.5	4	±4	±40	
LM144	5	20	1	2.5	4	±4	±40	Minimum Gain of 10
LM146	5	100	1.2	0.4	2	±1.5	±22	(Note 5)
LM148	5	100	1	0.5	3.6	±5	±22	Quad
LM149	5	100	4	2	3.6	±5	±22	Minimum Gain of 5, Quad
LM158	5	150	1	0.5	1.2	3	32	Dual
LM192	5	150	1	0.5	2	3	32	Comparator + Op Amp
LM741	5	500	1	0.5	2.8	±3	±22	
LM1558	5	500	*	*	5	±3	±22	Dual
LM4250	5	50	0.2	0.2	0.1	±1	±18	(Note 5)
LH0042	20	0.025	1	3	3.5	±5	±22	

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Automotive Temperature Range (−40°C to +85°C)								
LM604	3	60	7	3	9	4	36	Multiplexed Op Amp
LMC660A	3	0.02	1.4	1.1	2.2	5	15	Quad CMOS
LMC662A	3	0.02	1.4	1.1	1.3	5	15	Dual CMOS
LP2902	4	20	0.1	0.05	0.15	3	26	Quad
LM2902	7	250	1	0.5	3	3	26	Quad
LM2904	7	250	1	0.5	2	3	26	Dual
LM2924	7	250	1	0.5	2	3	26	Comparator + Op Amp

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Industrial Temperature Range (−25°C to +85°C) (Note 1)								
LM637A	0.025	10	65	14	4.5	±3.5	±18	Improved OP-37
LM627A	0.025	10	14	4.5	4.5	±3.5	±18	Improved OP-27
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LH0044B	0.05	30	0.4	0.06	4	±2	±20	
LH0044C	0.05	30	0.4	0.06	4	±2	±20	
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM637	0.1	25	65	14	4.8	±3.5	±18	Improved OP-37
LM627	0.1	25	14	4.5	4.8			Improved OP-27
LM208A	0.5	2	1	0.3	0.6	±2	±20	
LH0052C	2	0.005	1	3	3.8	±5	±22	
LM10B(L)	2	20	0.09	0.1	0.4	(Note 4)		Op Amp + Reference
LM201A	2	75	1	0.5	3	±3	±22	
LM207	2	75	1	0.5	3	±3	±22	Compensated LM201A
LM208	2	2	1	0.3	0.6	±2	±20	
LM212	2	2	1	0.3	0.6	±2	±20	Compensated LM208
LM224A	3	80	1	0.5	2	3	32	Quad
LM258A	3	80	1	0.5	1.2	3	32	Dual
LF255	5	0.1	2.5	5	4	±5	±22	
LF256	5	0.1	5	12	7	±5	±22	
LF257	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LM224	5	150	1	0.5	2	3	32	Quad
LM258	5	150	1	0.5	1.2	3	32	Dual
LM292	5	250	1	0.5	2	3	32	Comparator and Op Amp
LH0020C	6	500	*	*	6	±5	±22	
LH0022C	6	0.025	1	3	2.8	±5	±22	
LM246	6	250	0.5	0.4	2.5	±2	±18	(Note 5)
LM248	6	200	1	0.5	4.5	±5	±18	Quad
LM249	6	200	4	2	4.5	±5	±18	Minimum Gain of 5, Quad
LH0086C	10	0.5	3	10	15.5	±8	±18	Programmable Gain 1 to 200
LH0042C	20	0.05	1	3	4	±5	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2)								
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LM607A	0.025	2	1.8	0.7	1.5	±3	±18	Improved OP-07
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM607B	0.06	3	1.8	0.7	1.5	±3	±18	Improved OP-07
LM607	0.15	10	1.8	0.7	1.8	±3	±18	Improved OP-07
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LM308A	0.5	7	1	0.3	0.8	±2	±20	
LM11C	0.6	0.1	0.8	0.3	0.8	±2.5	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LM604A	1	40	5	3	9	4	36	Multiplexed Op Amp
LF355A	2	0.05	2.5	5	4	±5	±22	
LF356A	2	0.05	5	12	10	±5	±22	
LF357A	2	0.05	20	50	10	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±22	
LF412	3	0.2	4	15	6.8	±6	±22	Dual
LM324A	3	100	1	0.5	3	3	32	Quad
LM358A	3	100	1	0.5	2	3	32	Dual
LM604	3	60	5	7	9	4	36	Multiplexed Op Amp
LM741E	3	80	1.5	0.7	2.8	±3	±22	
LM10C(L)	4	30	0.09	0.1	0.5	(Note 4)		Op Amp + Reference
LP324	4	10	0.1	0.05	0.15	3	32	
LF347B	5	0.2	4	13	11	±6	±22	Quad
LF355B	5	0.1	2.5	5	4	±5	±22	
LF356B	5	0.1	5	12	4	±5	±22	
LF357B	5	0.1	20	50	7	±5	±22	
LF441	5	0.1	1	1	0.25	±6	±22	
LF442	5	0.1	1	1	0.5	±6	±22	Dual
LM11CL	5	0.2	0.8	0.3	0.8	±2.5	±20	
LF451	5	0.2	4	13	3.4	10	32	SO Pkg
LF453	5	0.2	4	13	6.5	10	32	SO Pkg Dual
LM611	5	35	1.4	0.7	0.3	3	36	Op Amp + Ref
LM613	5	35	0.8	0.7	1	3	36	2 Op Amps + 2 Comparators + Ref

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage Min V	Supply Voltage Max V	Special Features
Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2)								
LM614	5	35	0.8	0.7	1	3	36	Quad Op Amp + Ref
LM392	5	250	1	0.5	2	3	32	
LM833	5	1000	10	5	8	±5	±18	Dual Low Noise
LMC660	6	0.002	1.4	1.1	2.7	5	15	Quad CMOS
LMC662	6	0.002	1.4	1.1	1.6	5	15	Dual CMOS
LM346	6	250	0.5	0.4	2.5	±1.5	±22	(Note 5)
LM348	6	200	1	0.5	4.5	±5	±18	
LM349	6	200	4	2	4.5	±5	±18	
LM741C	6	500	1.5	0.5	2.8	±3	±18	
LM1458	6	500	*	*	5.6	±3	±18	
LM4250C	6	75	0.2	0.2	0.1	±1	±18	(Note 5)
LM324	7	250	1	0.5	3	3	32	
LM358	7	250	1	0.5	2	3	32	
LM301A	7.5	250	1	0.5	3	±3	±18	
LM307	7.5	250	1	0.5	3	±3	±18	Compensated LM301A
LM308	7.5	7	1	0.3	0.8	±2	±18	
LM312	7.5	7	1	0.2	0.8	±2	±18	Compensated LM308
LM343	8	40	1	2.5	5	±4	±34	
LM344	8	40	1	2.5	5	±4	±34	Minimum Gain of 10
LF347 N.C	10	0.2	4	13	11	±6	±18	Quad
LF351 NC	10	0.2	4	13	3.4	±6	±18	
LF353 NC	10	0.2	4	13	6.8	±6	±18	Dual
LF355	10	0.2	2.5	5	4	±5	±18	
LF356	10	0.2	5	12	10	±5	±18	
LF357	10	0.2	20	50	10	±5	±18	Minimum Gain of 5
LF444	10	0.1	1	1	1	±6	±18	Quad
LF13741	15	0.2	1	0.5	4	*	±18	
TL081C	15	0.2	4	13	2.8	±6	±18	
TL082C	15	0.2	4	13	5.6	±6	±18	Dual

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is for all amplifiers in a package.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

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Low I_{BIAS} Selection Guide

≤5 pA	≤20 pA	≤50 pA	≤100 pA	≤200 pA	≤500 pA	≤ 1 nA
T_A = 25°C						
LH0022	LMC668	LH0032A	LH0032	LF401A	LH4101	
	LMC660	LF155A/156A/	LF155/156/	LF401	LH0032C	
	LMC662	LF157A	LF157	LF400A		
	LH0022C	LF355A/356A/	LF255/256/	LF400		
LH0052	LH0042	LF357A	LF257	TL081	LH4004	
LH0052C	LH0042C	LF441A	LF355B/356B/	LH0032AC		
LH0062	LH0062C	LF442A	LF357B	LF351		
		LF444A	LF441	LF411A/411		
		LM11	LF442	LF355/356/		
			LF444	LF357		
			LM11C	LF147/347B/347		
				LF353		
			LH0101	LF412A/412		
			LH0086	LF13741		
			LH0086C	LM11CL		
				LH0084		
				LH0084C		
				LH4104		
				LH4104C		
				LH4105		
				LH4105C		
				LH4117		
				LH4117C		

Note: Datasheet should be referred to for conditions and more detailed information.

National Semiconductor

High Speed Operational Amplifier Selection Guide

Part #	Slew Rate V/μs (Typ)	GBW MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max) (Note 1)	Notes
GBW ≥ 4 MHz, T_A = 25°C					
LH4117	2500	400	20	±45	FET Input, Current Feedback
LH4118A	2400	300	2	±25	Low V_{OS}, Current Feedback
LH4004	600	200	15	±40	FET Input, Current Feedback
LH0024	500	70	4	±15	
LH0032	500	70	5	±20	FET Input
LH4124	400	70	8	±15	Low Cost LH0024
LH4161A	300	50	1	±6.5	Trimmed LM6161
LH4162A	300	50	2	±13	Dual LH4161A
LM6161	300	50	7	6.8	Unity Gain Stable, VIP™
LM6164	300	175	4	6.8	Min Gain of 5, VIP
LM6165	300	725	3	6.8	Min Gain of 25, VIP
LH4101	250	40	15	±40	Medium Power JFET
LH4106	170	34	20	±20	Drives 50Ω Loads
LM6313	250	35	20	23	Hi Speed Hi Power
LM6218	140	17	3	7	Fast Settling Dual, VIP
LF400	70	16	0.5	12	Fast Settling JFET
LF401	70	16	0.2	12	Precision Fast Settling JFET
LH0003	70	30	3	±3	
LH0062	70	15	5	±8	FET Input
LM118	70	15	4	7	
LF157	50	20	2	7	Min Gain of 5, JFET
LH4104	40	18	10	±25	Medium Power Fast Settling JFET
LH4105	40	18	2	±25	Trimmed LH4104
LM359	30	30	*	22	Dual Current Mode (Norton) Amp
LF411	15	4	0.5	2.8	JFET
LF412	15	4	1.0	5.6	Dual JFET
LF147	13	4	5	11	Quad JFET
LF451	13	4	5	3.4	SO Pkg
LF453	13	4	5	6.5	SO Pkg Dual
LF351	13	4	10	3.4	JFET
LF353	13	4	10	6.8	Dual JFET
LF156	12	4.5	2	7	JFET
LM833	7	15	5	8	Dual Low Noise

*Not specified.

Note 1: Supply current is for all amplifiers in a package.

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Medium and High Power Operational Amplifier Selection Guide ($\geq$ 0.1A Output) (T_A = 25°C, Note 1)

Part #	I_{OUT} A (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Slew Rate V/μS (Typ)	PBW (Typ)
LH4104	0.1	10	±25	40	600 kHz
LH4101	0.1	15	±40	250	8 MHz
LH4105	0.1	2	±25	40	600 kHz
LH4118	0.1	2	±25	2400	55 MHz
LH0041	0.2	3	±3.5	3	20 kHz
LH4141	0.2	6	±4	3	20 kHz
LH4117	0.2	20	±45	2500	40 MHz
LH0061	0.6	4	±10	70	1 MHz
LH0021	1.2	3	±3.5	3	20 kHz
LH0101A	2.2	3	±35	10	300 kHz
LH0101	2.2	10	±35	10	300 kHz
LM675	3	10	50	8	*
LM12(L)	(Note 2)	7	80	9	60 kHz
LM12C(L)	(Note 2)	15	120	9	60 kHz

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

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Special Amplifier Selection Guide

Amplifiers with Added Functions

Featuring the new Super-Block™ family, these amplifiers have additional special functions within their packages which help minimize the number of components required in an application. These devices are often used in control circuits, power supplies, and automatic test systems.

LH0045	Two-Wire Transmitter
LM10	Op Amp and Adjustable Voltage Reference
LM392	Op Amp and Comparator
LM604	Super-Block Multiplexed Op Amp (4 Inputs, 1 Output)
LM611	Super-Block Op Amp and Adjustable Voltage Reference
LM613	Super-Block Dual Op Amp, Dual Comparator, and Adjustable Voltage Reference
LM614	Super-Block Quad Op Amp and Adjustable Voltage Reference

Transconductance Amplifiers (Voltage In, Current Out)

These amplifiers provide a transconductance (g_m) proportional to their bias current, which is controlled externally. This programmable gain makes the amplifiers useful in applications such as voltage-controlled amplifiers, current-controlled amplifiers, AGC circuits, and voltage multipliers.

LM3080	Operational Transconductance Amplifier
LM13600	Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
LM13700	Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers

Transimpedance Amplifiers (Current In, Voltage Out)

Transimpedance amplifiers are widely used to amplify photo-diode signals, and to ground-reference differential voltage signals which have high common-mode voltages. The LH0082 was designed to receive and amplify analog and digital signals transmitted by fiber optics. Like the LM359, the LH0082 can also be used as a video amplifier. The LM2900 series has found popularity in filter applications, as well as general-purpose amplifiers.

LH0082	20 MHz Transimpedance Amplifier/Comparator
LM359	Dual Current Mode (Norton) Amplifier
LM2900 LM3900 LM3301 LM3401	Quad Current Mode (Norton) Amplifier

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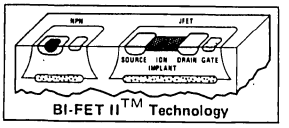


LF147/LF347/LF347B Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

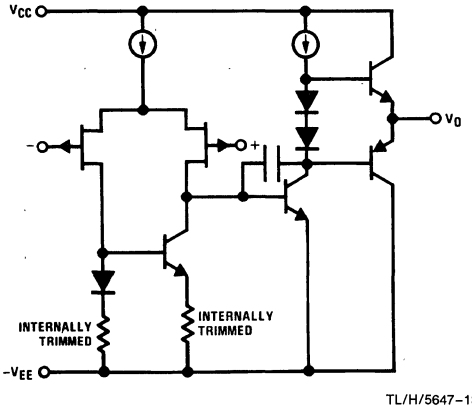
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	5 mV max
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Simplified Schematic

¼ Quad



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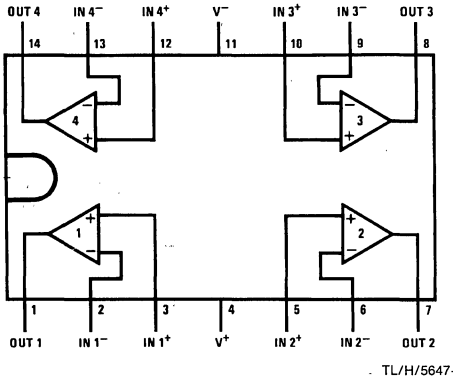
Connection Diagram

Dual-In-Line Package



TL/H/5647–1

Top View

Order Number LF147D, LF347D, LF147J, LF347BJ, LF347J, LF347M, LF347WM, LF347BN or LF347N
See NS Package Number D14E, J14A, M14A, M14B or N14A

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Cavity DIP (D) Package		80°C/W
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		1	5 8		3	5 7		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		25	100 25		25	100 4		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		50	200 50		50	200 8		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	50 25	100		50 25	100		25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz − 20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available In the military temperature range $-55°C \leq T_A \leq 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \leq T_A \leq 70°C$. Junction temperature can rise to T_j max = 150°C.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

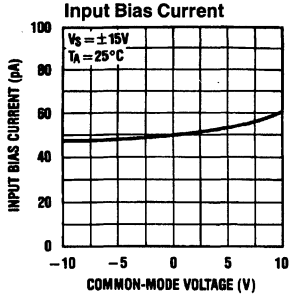
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

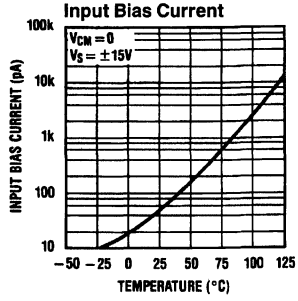
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

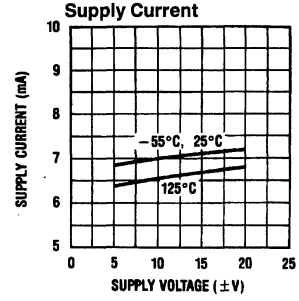
Input Bias Current



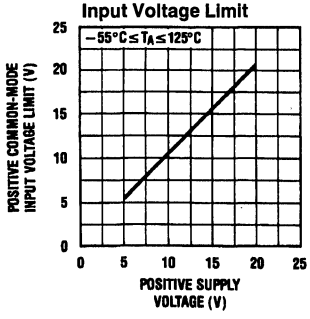
Input Bias Current



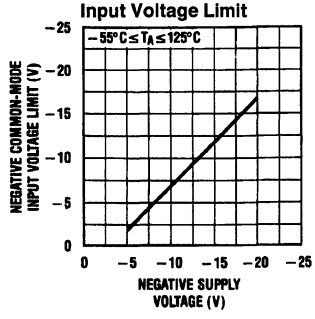
Supply Current



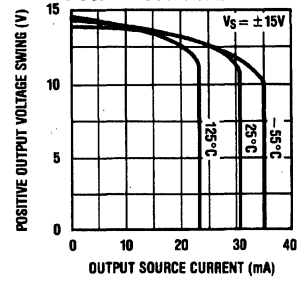
Positive Common-Mode Input Voltage Limit



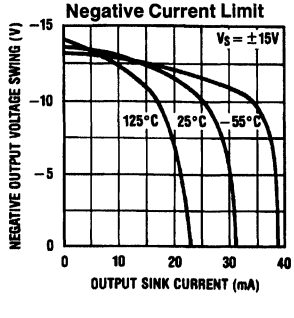
Negative Common-Mode Input Voltage Limit



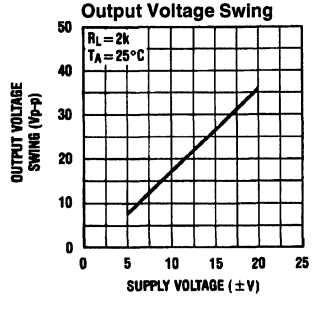
Positive Current Limit



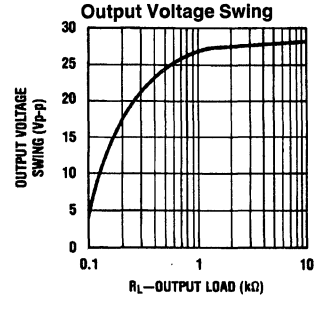
Negative Current Limit



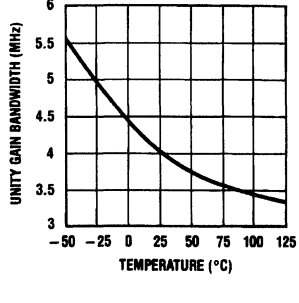
Output Voltage Swing



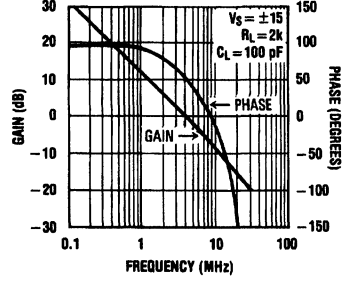
Output Voltage Swing



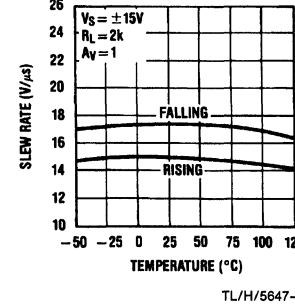
Gain Bandwidth



Bode Plot



Slew Rate



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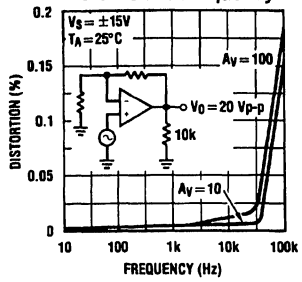
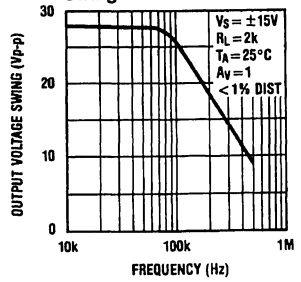
Typical Performance Characteristics (Continued)

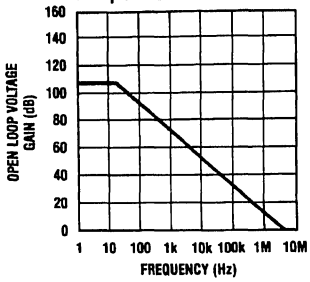
Distortion vs Frequency



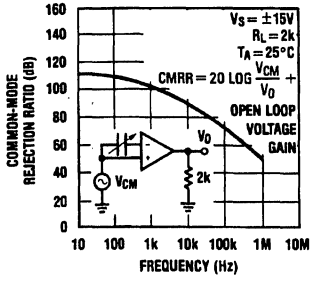
Undistorted Output Voltage Swing



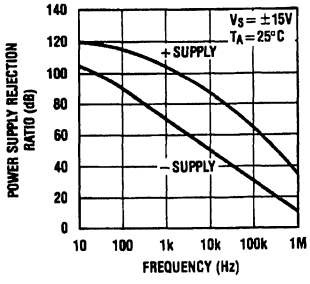
Open Loop Frequency Response



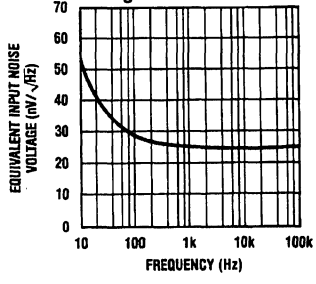
Common-Mode Rejection Ratio



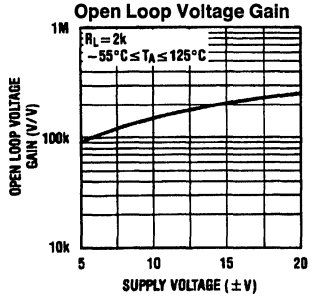
Power Supply Rejection Ratio



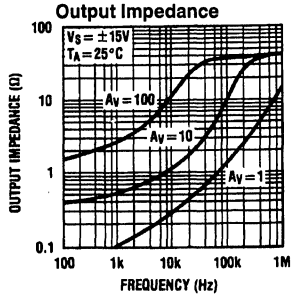
Equivalent Input Noise Voltage



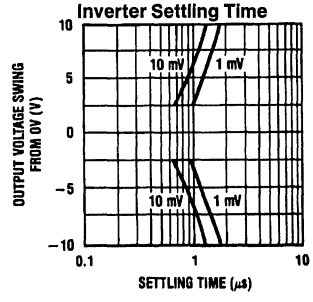
Open Loop Voltage Gain



Output Impedance



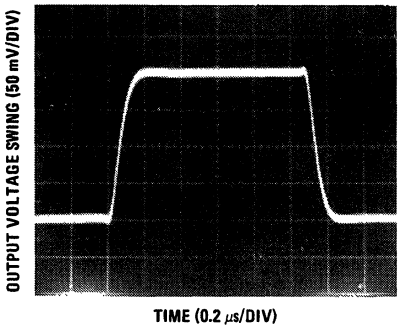
Inverter Settling Time



TL/H/5647–3

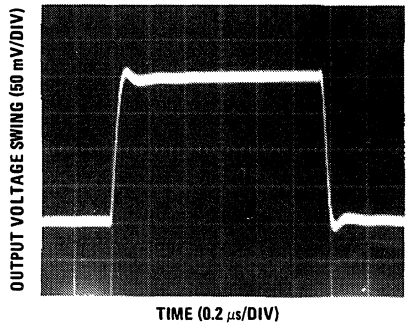
Pulse Response $R_L = 2\,k\Omega$, $C_L = 10\,pF$

Small Signal Inverting



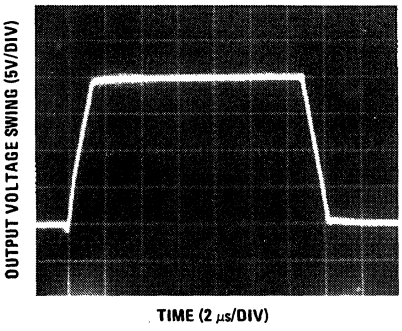
TL/H/5647–4

Small Signal Non-Inverting



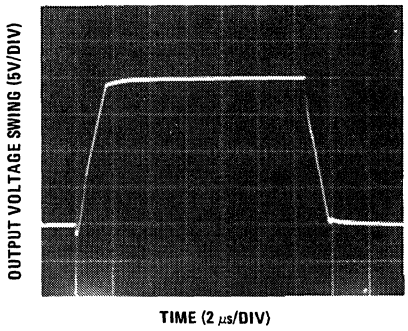
TL/H/5647–5

Large Signal Inverting



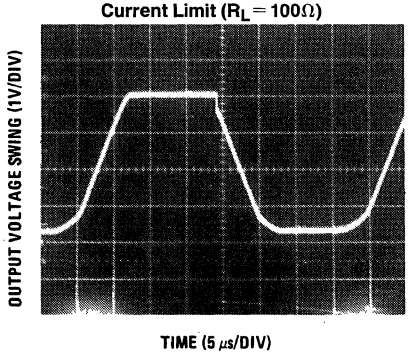
TL/H/5647–6

Large Signal Non-Inverting



TL/H/5647–7

Current Limit ($R_L = 100\Omega$)



TL/H/5647–8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

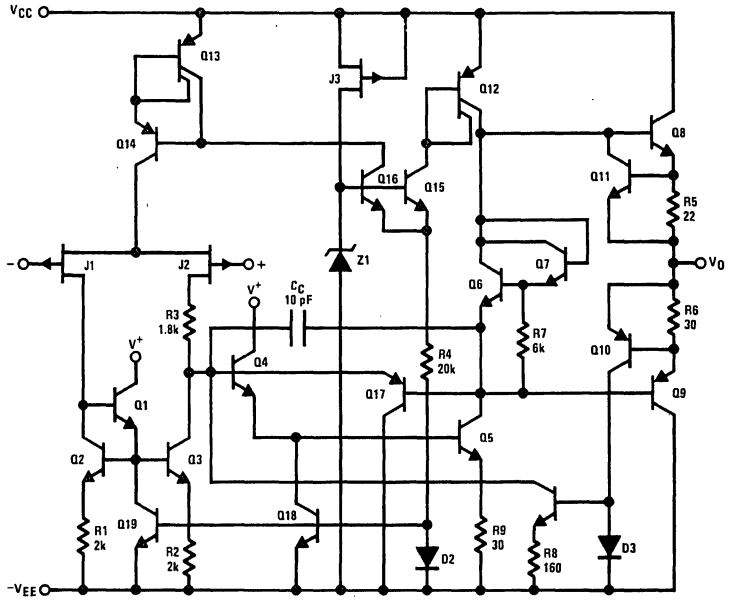
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

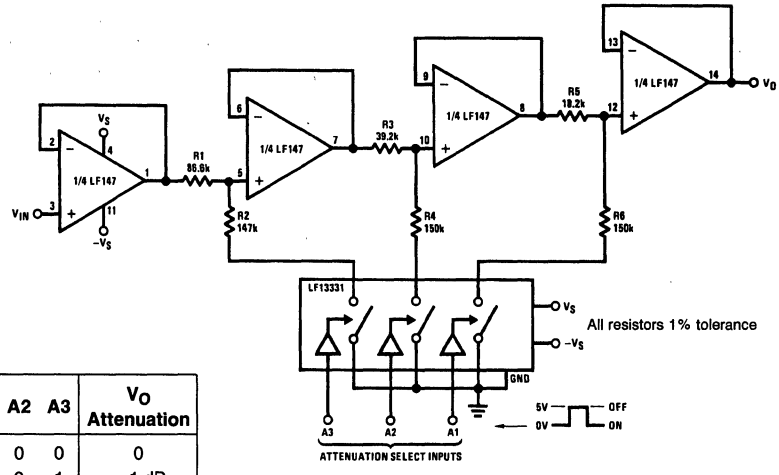
Detailed Schematic



TL/H/5647–9

Typical Applications

Digitally Selectable Precision Attenuator

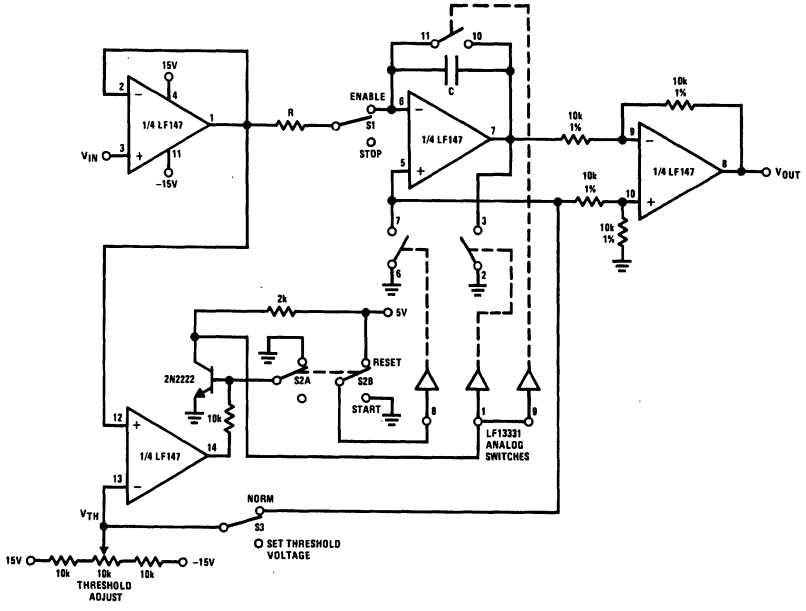


A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

TL/H/5647–10

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



TL/H/5647–11

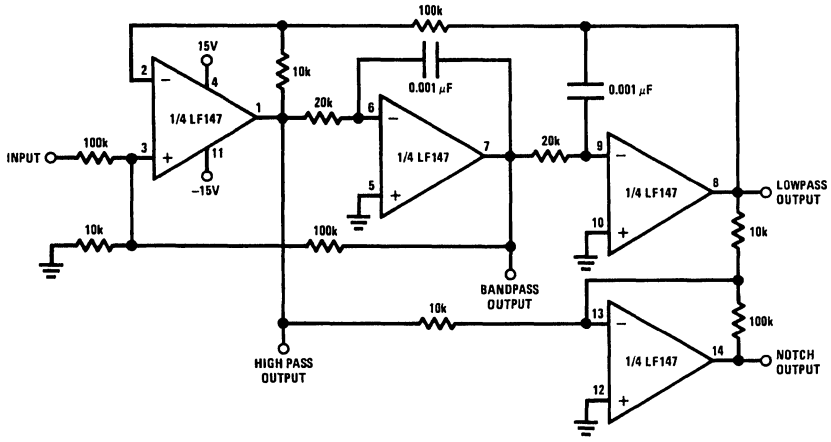
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT}=\frac{1}{RC}\int_0^t (V_{IN}-V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



TL/H/5647–12

For circuit shown:

$f_o = 3$ kHz, $f_{NOTCH} = 9.5$ kHz

$Q = 3.4$

Passband gain:

Highpass—0.1

Bandpass—1

Lowpass—1

Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

National Semiconductor

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155/LF155A/LF255/LF355/LF355A/ LF355B Low Supply Current LF156/LF156A/LF256/LF356/LF356A/ LF356B Wide Band LF157/LF157A/LF257/LF357/LF357A/ LF357B Wide Band Decompensated ($A_{VMIN} = 5$)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

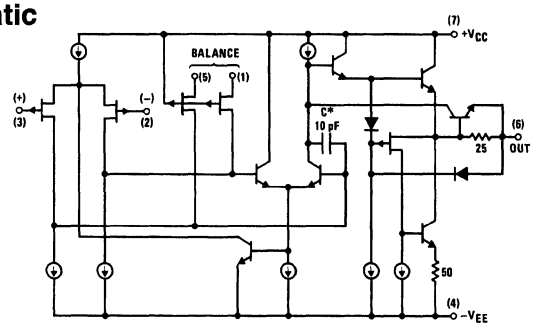
(LF155A, LF156A, LF157A)

- Low input bias current: 30 pA
- Low Input Offset Current: 3 pA
- High input impedance: $10^{12}\Omega$
- Low input offset voltage: 1 mV
- Low input offset voltage temp. drift: 3 μV/°C
- Low input noise current: 0.01 pA/$\sqrt{\text{Hz}}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V = 5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/$\sqrt{\text{Hz}}$

Simplified Schematic



*3 pF in LF157 series.

TL/H/5646–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
J-Package		150°C	115°C	115°C
M-Package			100°C	100°C
Power Dissipation at T_A = 25°C (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
J-Package		1260 mW	900 mW	900 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
J-Package		100°C/W	100°C/W	100°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance (100 pF discharged through 1.5 kΩ)	1200V	1200V	1200V	1200V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 50Ω, T_A = 25°C Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 50Ω		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S = 50Ω, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2k Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10k V_S = ±15V, R_L = 2k	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		 40	 50		V/μs V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 25 25			 15 12			 15 12		 nV/√Hz nV/√Hz
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01			0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25°C, V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/μs V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz	 25 20		 15 12		 15 12	 nV/√Hz nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz	0.01 0.01		0.01 0.01		0.01 0.01	pA/√Hz pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

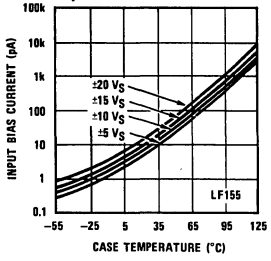
Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETSF156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

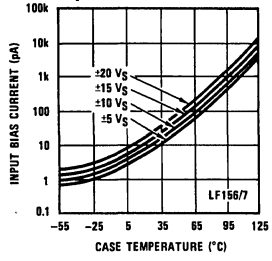
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

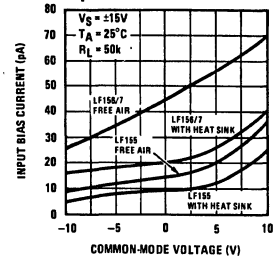
Input Bias Current



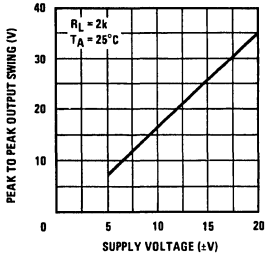
Input Bias Current



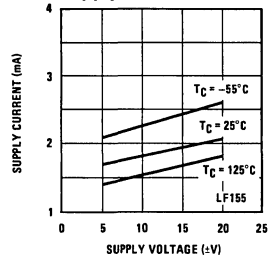
Input Bias Current



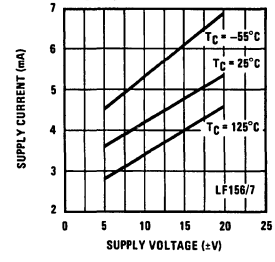
Voltage Swing



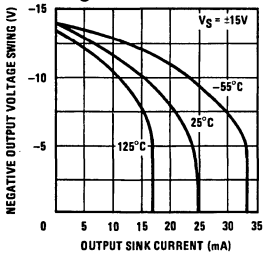
Supply Current



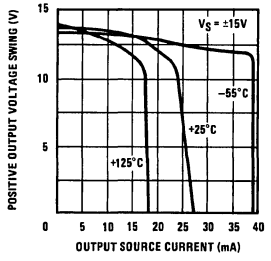
Supply Current



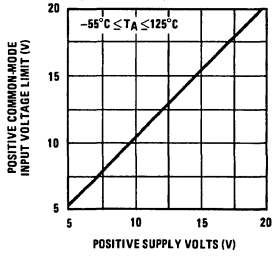
Negative Current Limit



Positive Current Limit

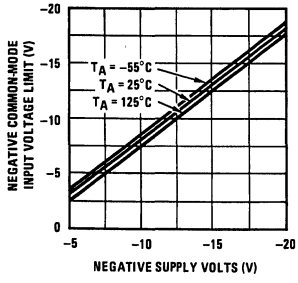


Positive Common-Mode Input Voltage Limit

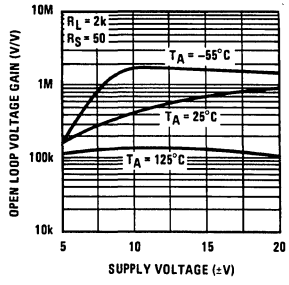


TL/H/5646–2

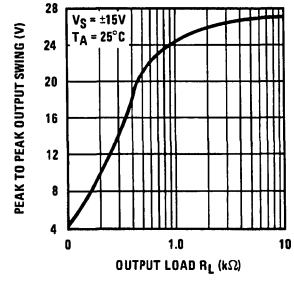
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



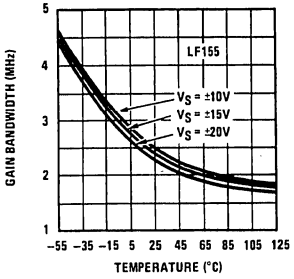
Output Voltage Swing



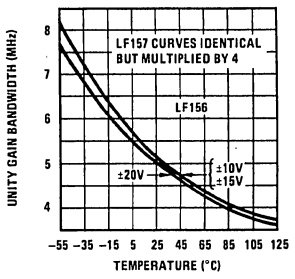
TL/H/5646–3

Typical AC Performance Characteristics

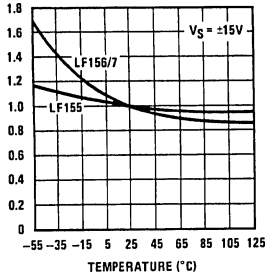
Gain Bandwidth



Gain Bandwidth

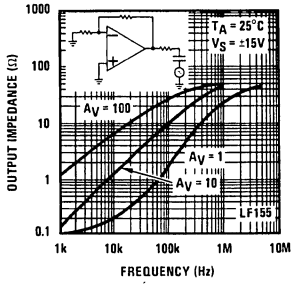


Normalized Slew Rate

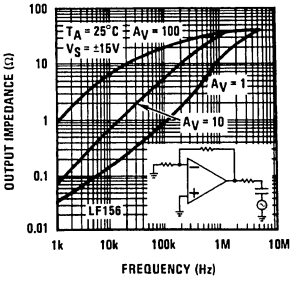


TL/H/5646-4

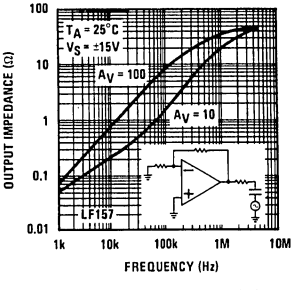
Output Impedance



Output Impedance

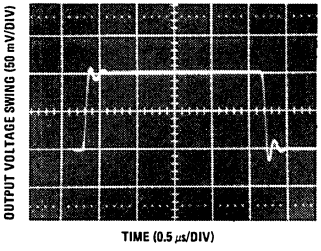


Output Impedance



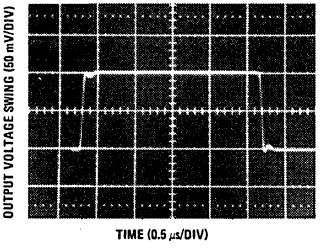
TL/H/5646-12

LF155 Small Signal Pulse Response, $A_V = +1$



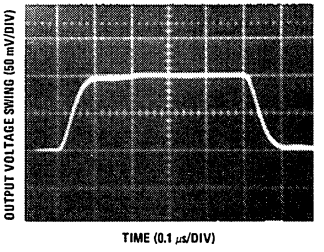
TL/H/5646-5

LF156 Small Signal Pulse Response, $A_V = +1$



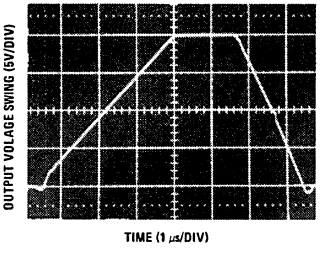
TL/H/5646-6

Small Signal Pulse Response, $A_V = +5$



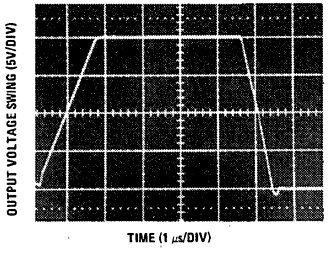
TL/H/5646-7

LF155 Large Signal Pulse Response, $A_V = +1$



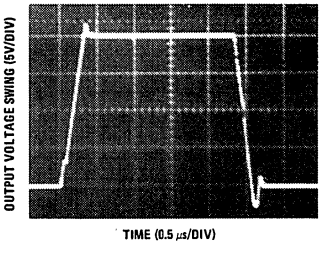
TL/H/5646-8

LF156 Large Signal Pulse Response, $A_V = +1$



TL/H/5646-9

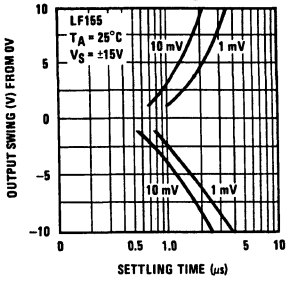
LF157 Large Signal Pulse Response, $A_V = +5$



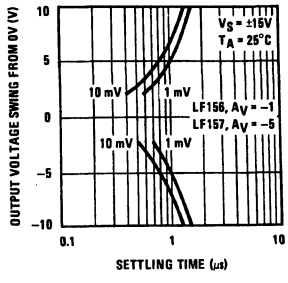
TL/H/5646-10

Typical AC Performance Characteristics (Continued)

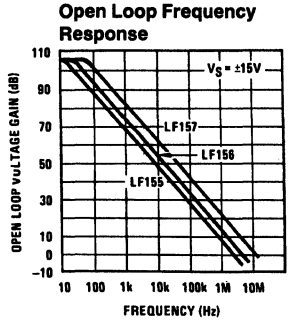
Inverter Settling Time



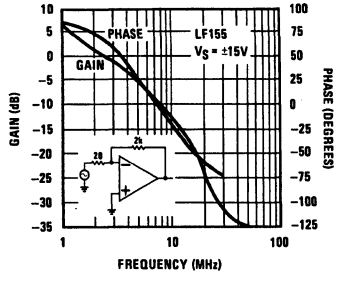
Inverter Settling Time



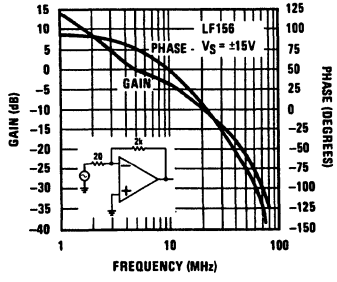
Open Loop Frequency Response



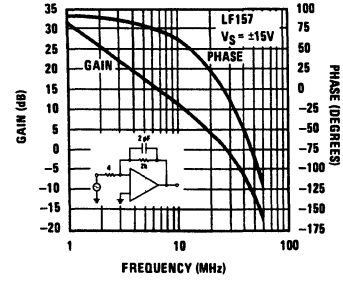
Bode Plot



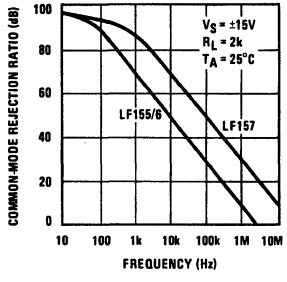
Bode Plot



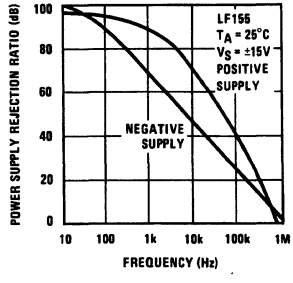
Bode Plot



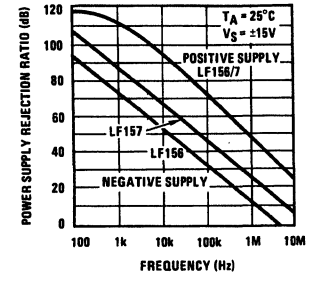
Common-Mode Rejection Ratio



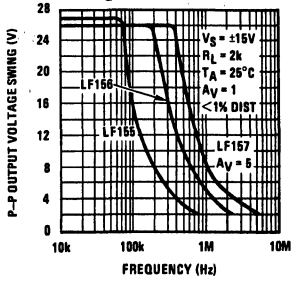
Power Supply Rejection Ratio



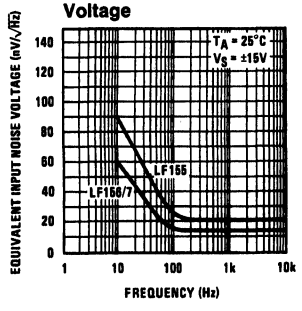
Power Supply Rejection Ratio



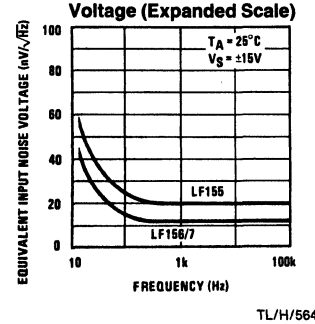
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

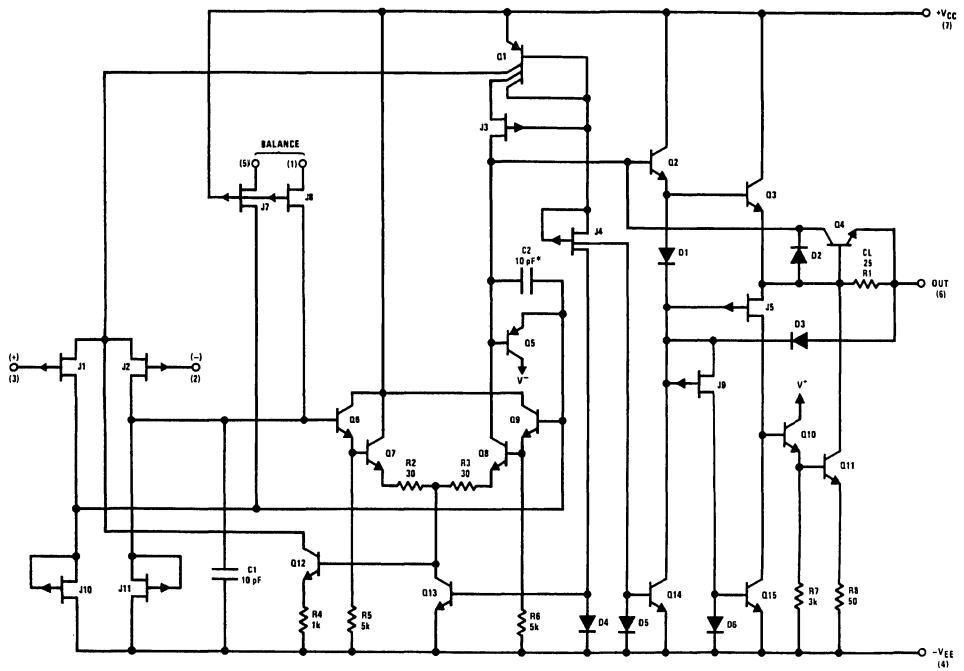


Equivalent Input Noise Voltage (Expanded Scale)



TL/H/5646–11

Detailed Schematic

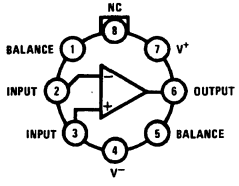


*C = 3 pF in LF157 series.

TL/H/5646–13

Connection Diagrams (Top Views)

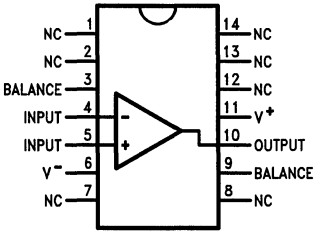
Metal Can Package (H)



TL/H/5646–14

Order Number
LF155AH, LF156AH, LF157AH, LF155H, LF156H, LF157H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF355BH, LF356BH, LF357BH, LF355H, LF356H or LF357H
See NS Package Number H08C

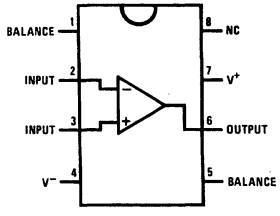
Dual-In-Line Package (J)



TL/H/5646–30

Order Number
LF155J, LF156J, LF157J, LF355J, LF356J, LF357J, LF355BJ, LF356BJ or LF357BJ
See NS Package Number J14A

Dual-In-Line Package (M and N)



TL/H/5646–29

Order Number
LF355M, LF356M, LF357M, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N
See NS Package Number M08A or N08E

3

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

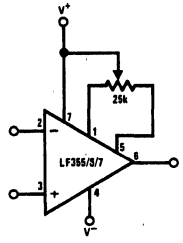
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

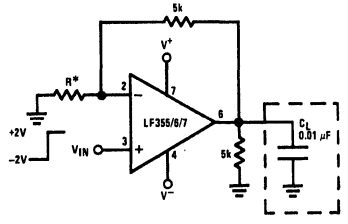
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



*LF155/6 R = 5k

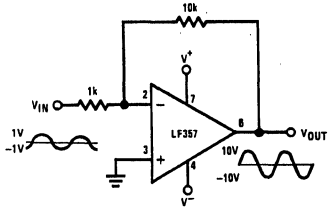
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01$ μF.

Overshoot ≤ 20%

Settling time (t_s) ≅ 5 μs

LF157. A Large Power BW Amplifier

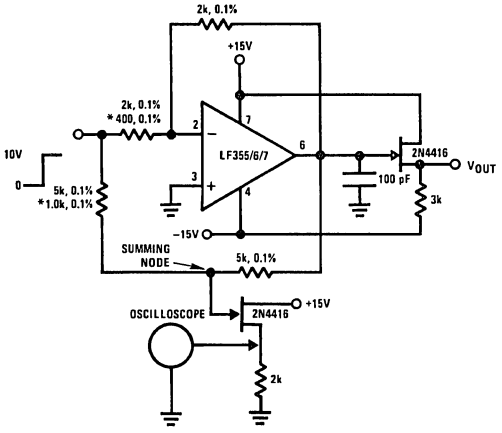


TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

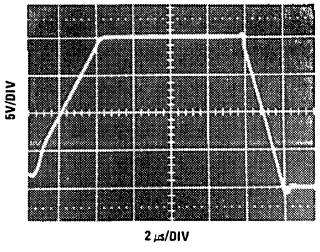


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

TL/H/5646–16

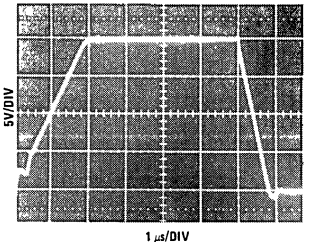
Large Signal inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



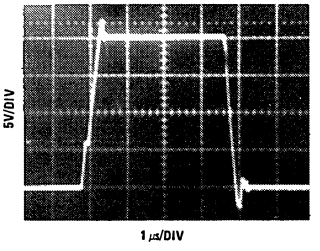
TL/H/5646–17

LF356



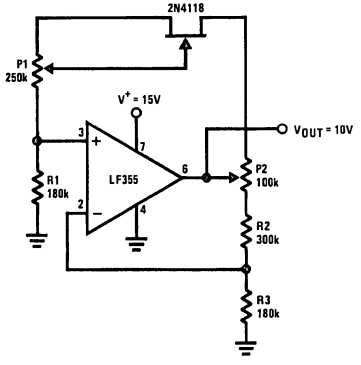
TL/H/5646–18

LF357



TL/H/5646–19

Low Drift Adjustable Voltage Reference

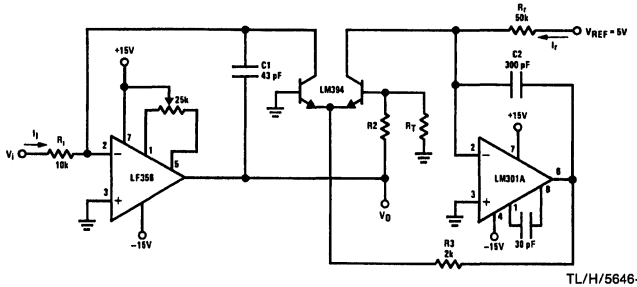


- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

TL/H/5646–20

Typical Applications (Continued)

Fast Logarithmic Converter

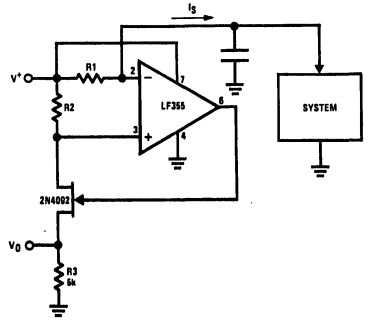


TL/H/5646–21

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q}\ln V_i\left[\frac{R_r}{V_{REF}\,R_i}\right] = \log V_i \frac{1}{R_i I_r} R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)}$$

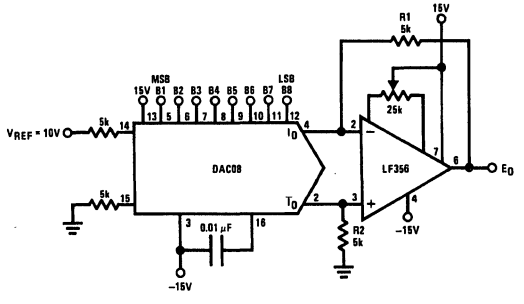
Precision Current Monitor



TL/H/5646–31

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



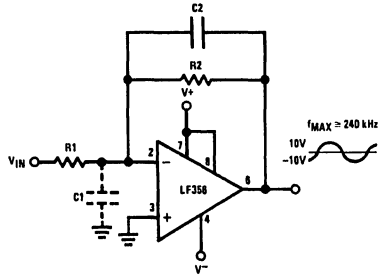
TL/H/5646–32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

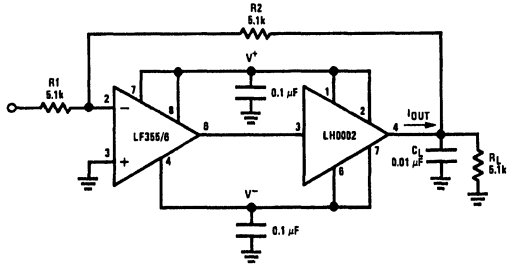
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



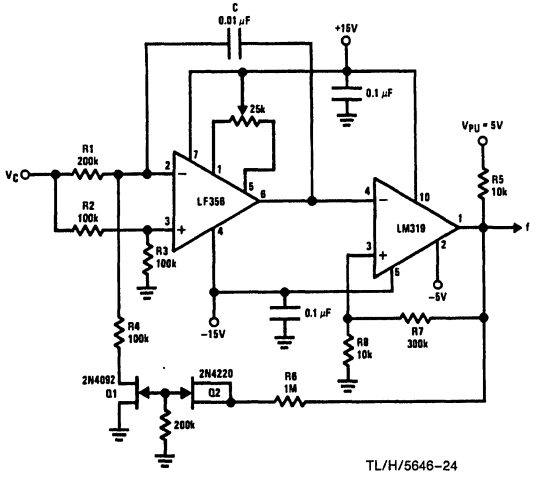
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2≅ R1C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10-2}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

3 Decades VCO

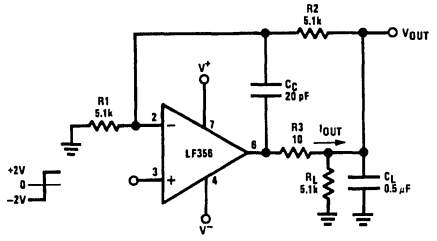


TL/H/5646-24

$f = \frac{V_C (R8+R7)}{(8\ V_{PU}\ R8\ R1)\ C}$, $0 \leq V_C \leq 30V$, $10\ Hz \leq f \leq 10$ kHz

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads

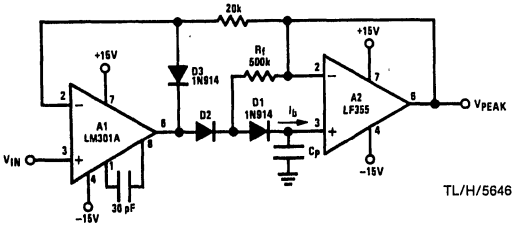


TL/H/5646-22

- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}$ V/µs = 0.04 V/µs (with C_L shown)

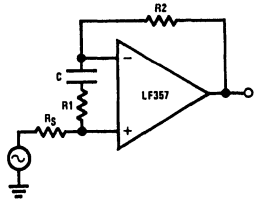
Low Drift Peak Detector



TL/H/5646

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially *Ib* (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



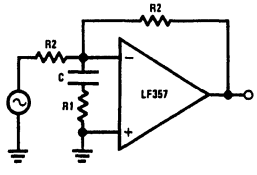
$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3\ dB} \cong 5$ MHz

Inverting Unity Gain for LF157



$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$

$R1 = \frac{R2}{4}$

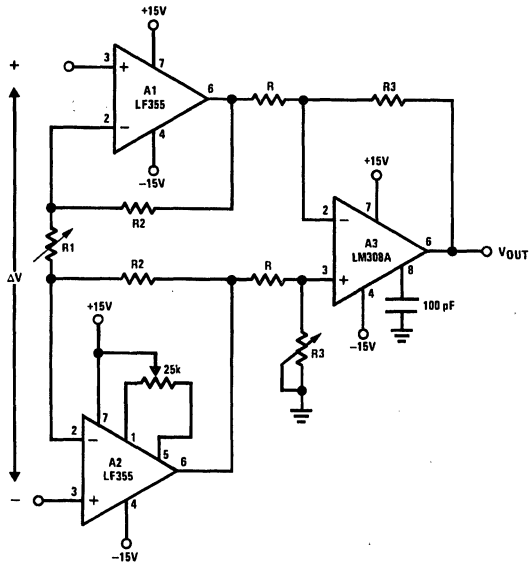
$A_{V(DC)} = -1$

$f_{-3\ dB} \cong 5$ MHz

TL/H/5646-25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier

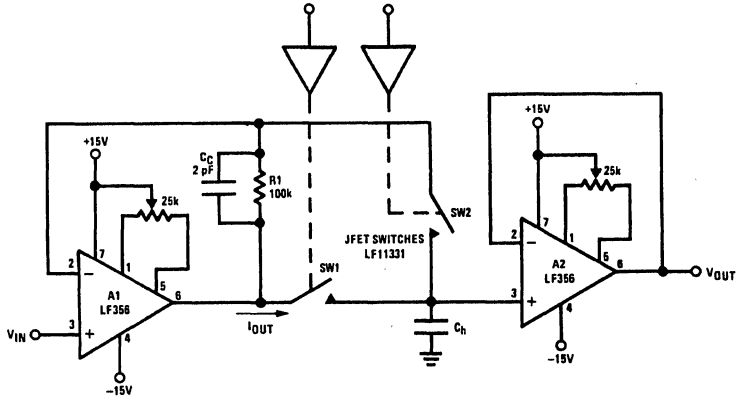


TL/H/5646–26

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold



TL/H/5646–33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

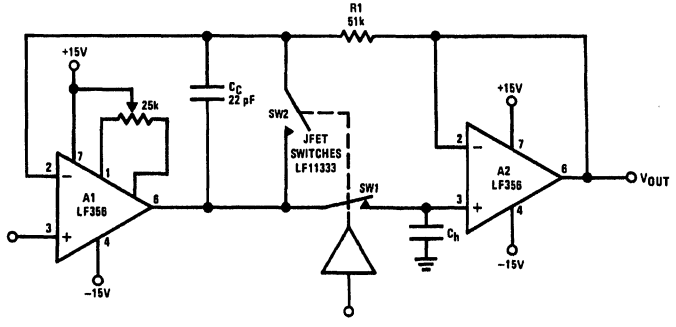
$$T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right] \text{ ½ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN}\, C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN}\, C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

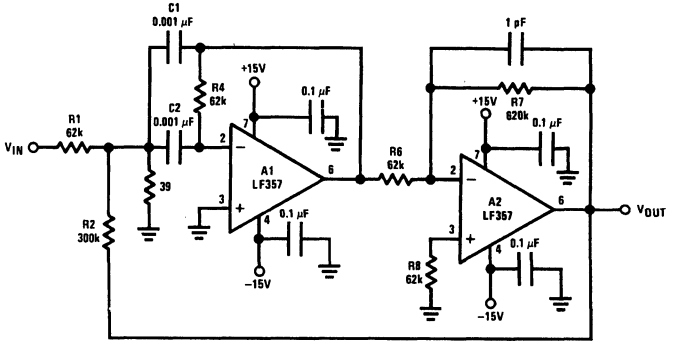


TL/H/5646–27

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

Typical Applications (Continued)

High Q Band Pass Filter



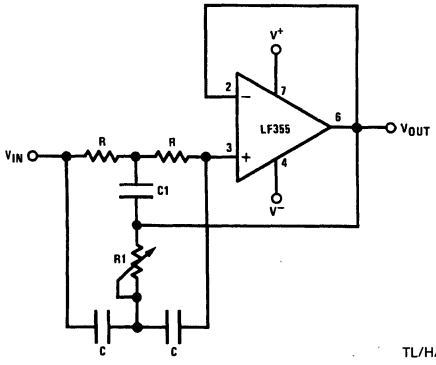
TL/H/5646–28

- By adding positive feedback (R2) Q increases to 40
- $f_{BP} = 100$ kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

High Q Notch Filter



TL/H/5646–34

- $2R1 = R = 10\ M\Omega$
  $2C = C1 = 300$ pF
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120$ Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

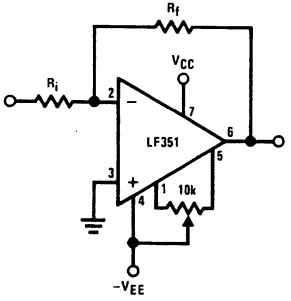
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

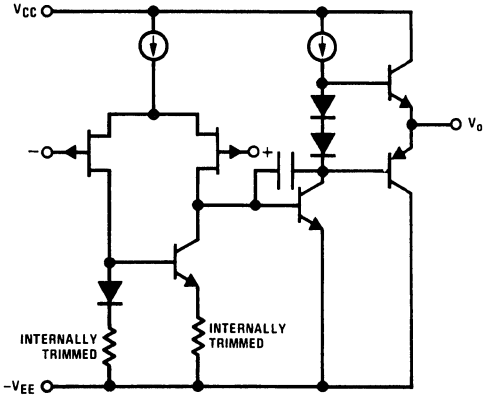
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

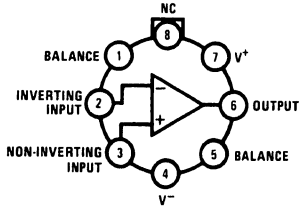


Simplified Schematic



Connection Diagrams (Top Views)

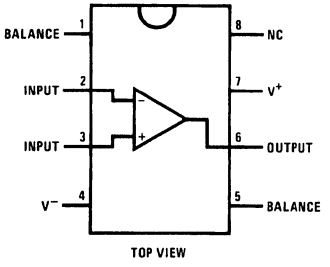
Metal Can Package



Note. Pin 4 connected to case.

Order Number LF351H
See NS Package Number H08C

Dual-In-Line Package



TOP VIEW

Order Number LF351J, LF351M or LF351N
See NS Package Number J08A, M08A or N08E

TL/H/5648–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

	H Package	N Package
θ_{jA}	164°C/W (Still Air)	120°C/W
	66°C/W	
	(400 LF/min Air Flow)	
θ_{jC}	21°C/W	

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ ±70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		$V/\mu s$
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

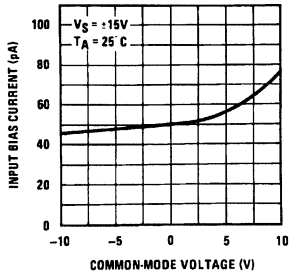
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From $\pm 15V$ to $\pm 5V$.

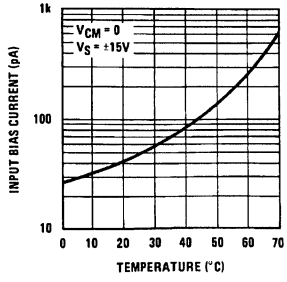
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

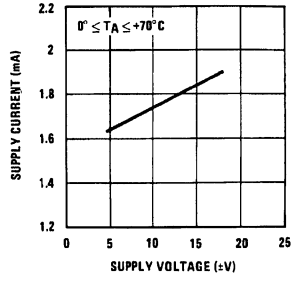
Input Bias Current



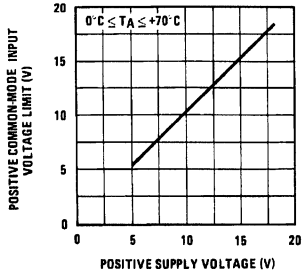
Input Bias Current



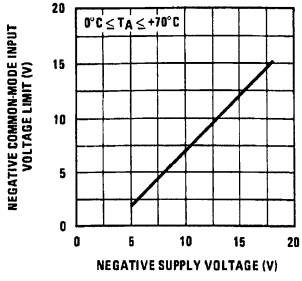
Supply Current



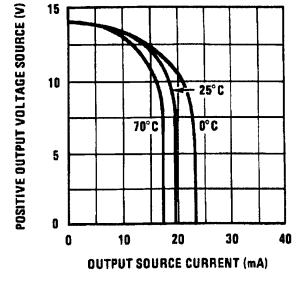
Positive Common-Mode Input Voltage Limit



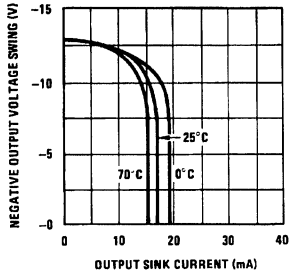
Negative Common-Mode Input Voltage Limit



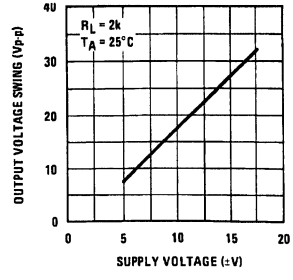
Positive Current Limit



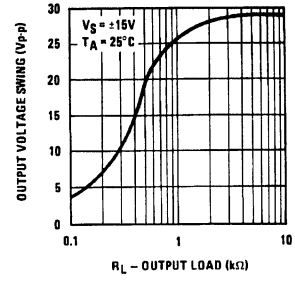
Negative Current Limit



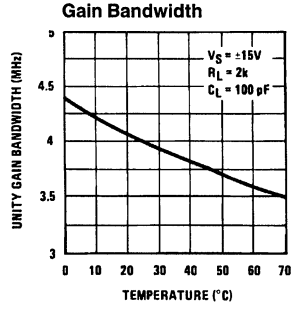
Voltage Swing



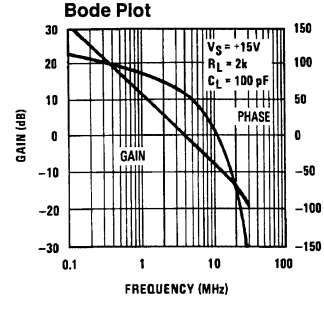
Output Voltage Swing



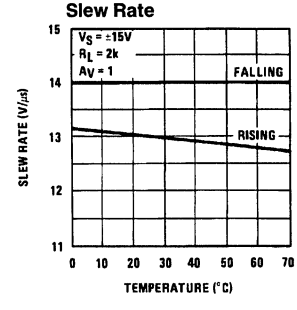
Gain Bandwidth



Bode Plot



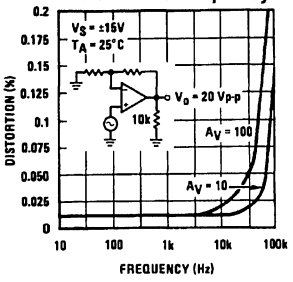
Slew Rate



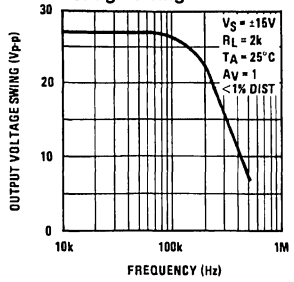
TL/H/5648–2

Typical Performance Characteristics (Continued)

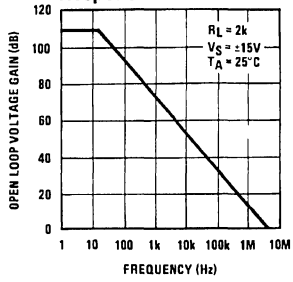
Distortion vs Frequency



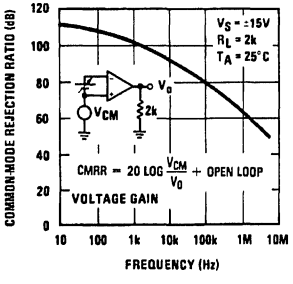
Undistorted Output Voltage Swing



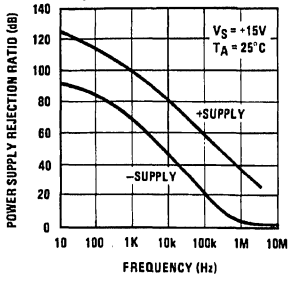
Open Loop Frequency Response



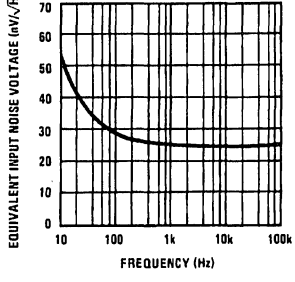
Common-Mode Rejection Ratio



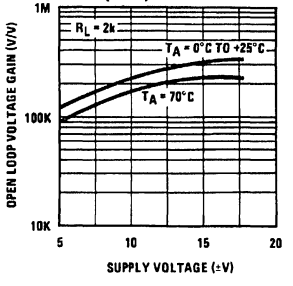
Power Supply Rejection Ratio



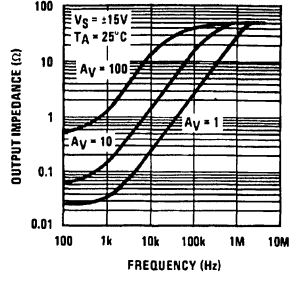
Equivalent Input Noise Voltage



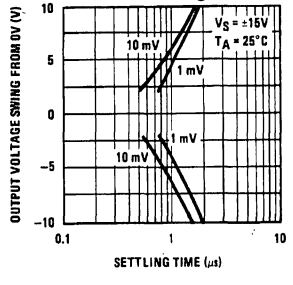
Open Loop Voltage Gain (V/V)



Output Impedance



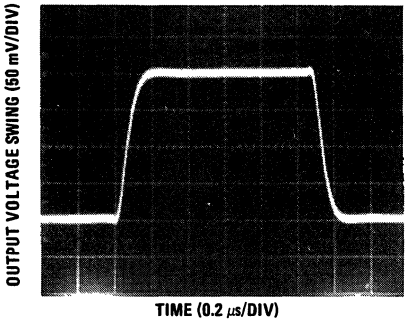
Inverter Settling Time



TL/H/5648–3

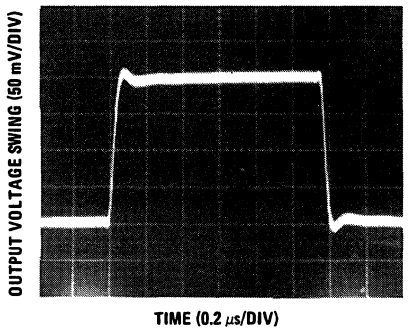
Pulse Response

Small Signal Inverting



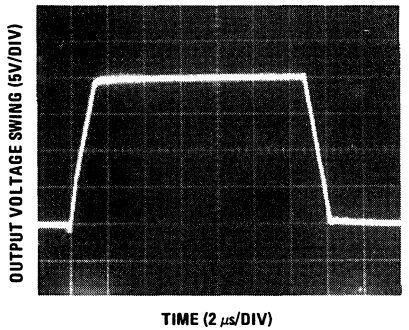
TL/H/5648–4

Small Signal Non-Inverting



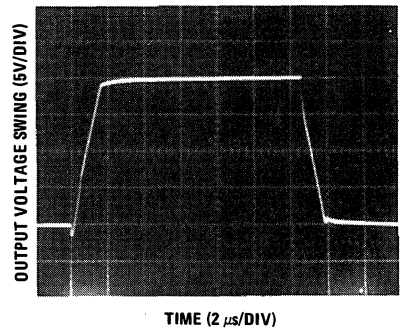
TL/H/5648–5

Large Signal Inverting



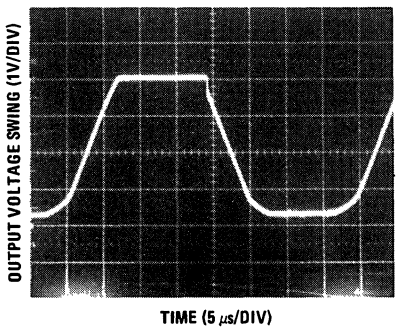
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit ($R_L = 100\Omega$)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

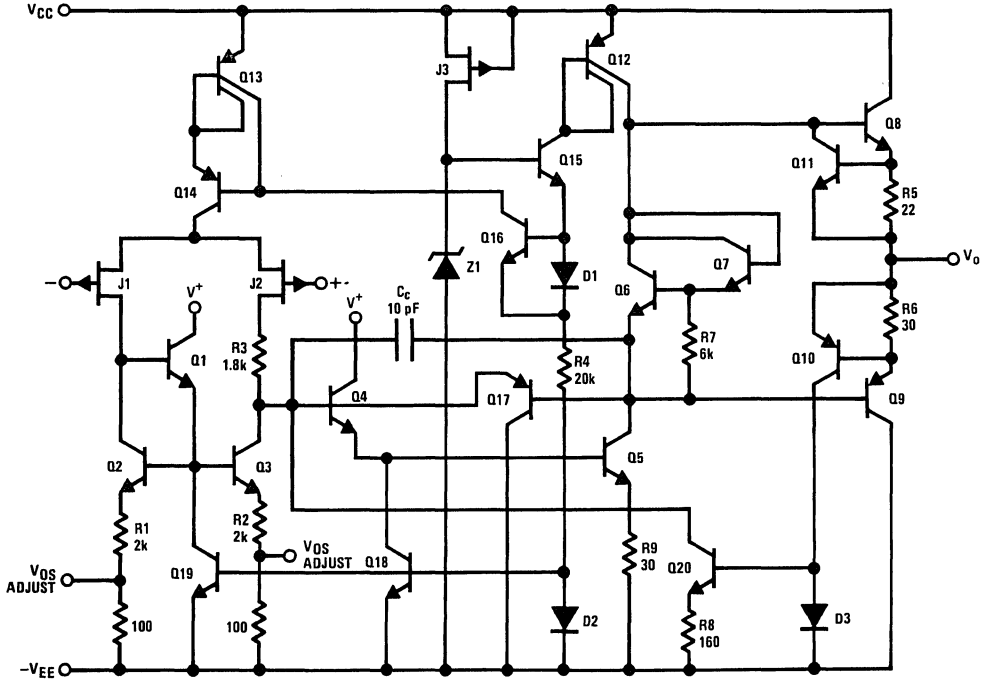
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

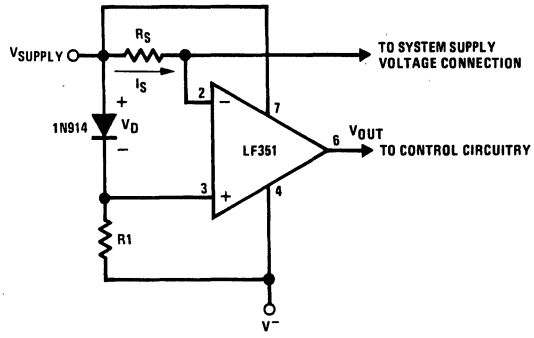
Detailed Schematic



TL/H/5648–9

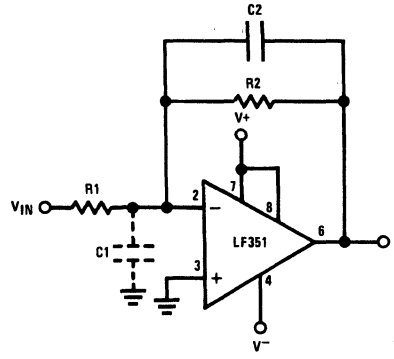
Typical Applications

Supply Current Indicator/Limiter



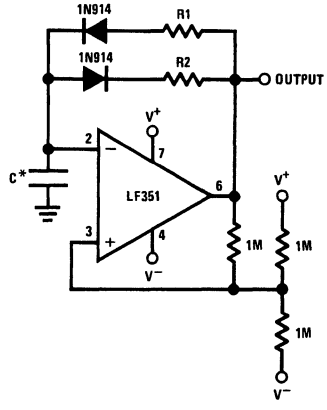
• V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



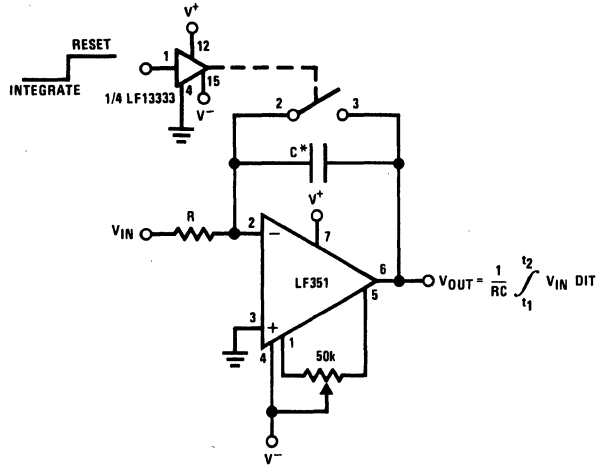
• $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$

• $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

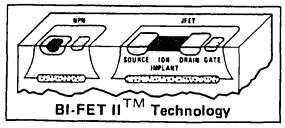


TL/H/5648–10

*Low leakage capacitor

• 50k pot used for less sensitive V_{OS} adjust

National Semiconductor



LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

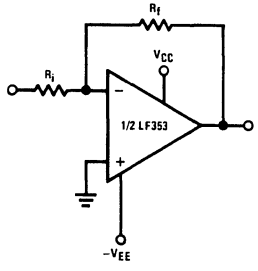
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

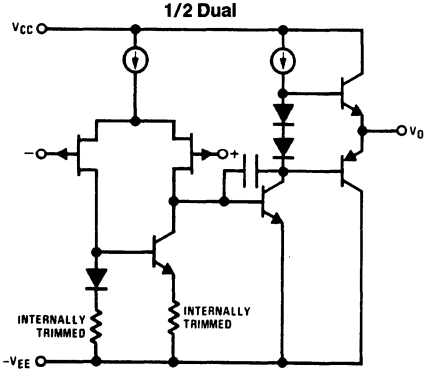
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50pA
■ Low input noise voltage	16 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V=10$, $R_L=10k$, $V_O=20Vp-p$, BW=20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

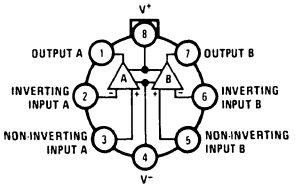


Simplified Schematic



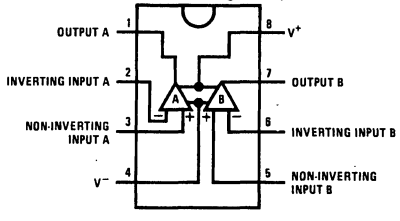
Connection Diagrams

Metal Can Package (Top View)



Order Number LF353H
See NS Package Number H08C

Dual-In-Line Package (Top View)



Order Number LF353J, LF353M or LF353N
See NS Package Number J08A, M08A or N08E

TL/H/5649–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 4, 5) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	T_j=25°C, (Notes 4, 5) $T_j \leq 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C V_O=±10V, R_L=2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz−20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/μs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1000 Hz		25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 158°C/W typ junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

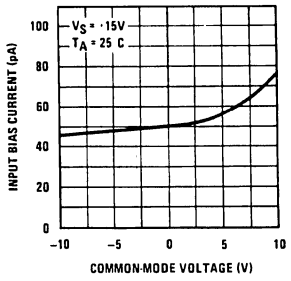
Note 4: These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM}=0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+\theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

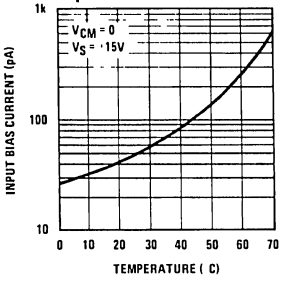
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Typical Performance Characteristics

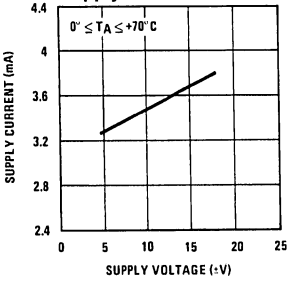
Input Bias Current



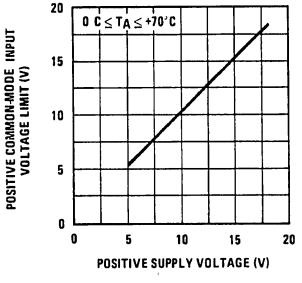
Input Bias Current



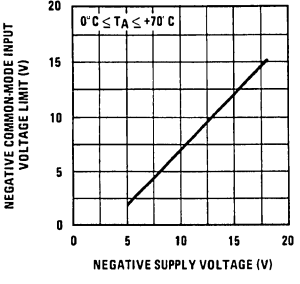
Supply Current



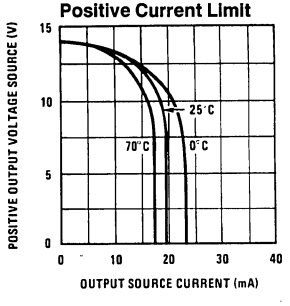
Positive Common-Mode Input Voltage Limit



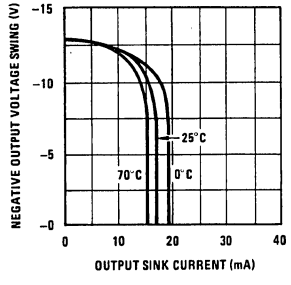
Negative Common-Mode Input Voltage Limit



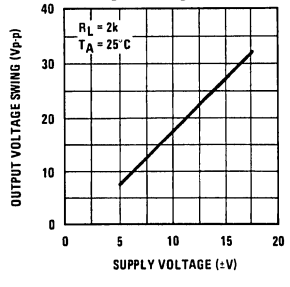
Positive Current Limit



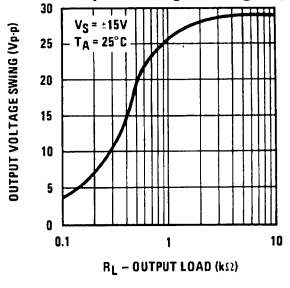
Negative Current Limit



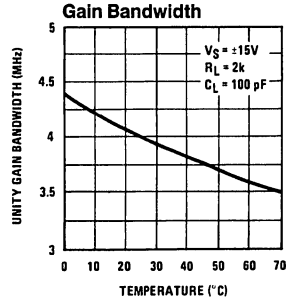
Voltage Swing



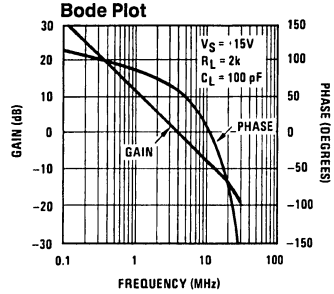
Output Voltage Swing



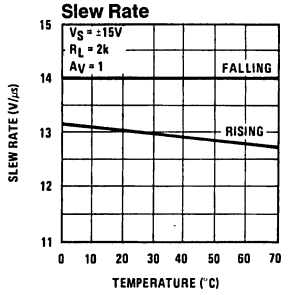
Gain Bandwidth



Bode Plot



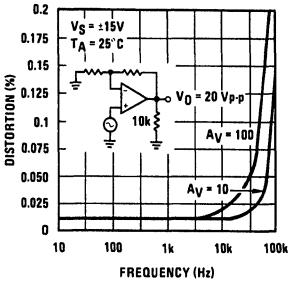
Slew Rate



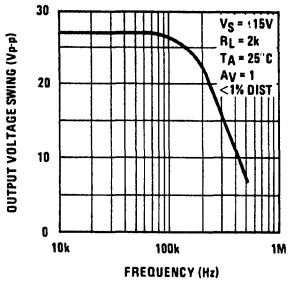
TL/H/5649–2

Typical Performance Characteristics (Continued)

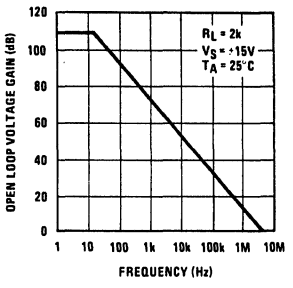
Distortion vs Frequency



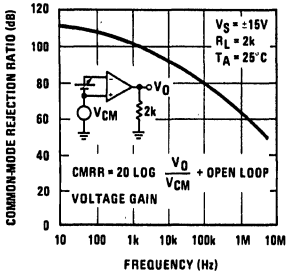
Undistorted Output Voltage Swing



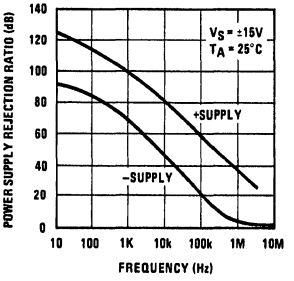
Open Loop Frequency Response



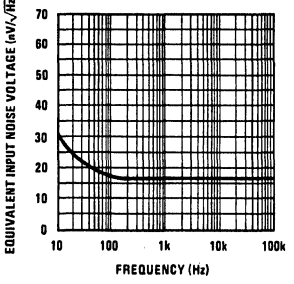
Common-Mode Rejection Ratio



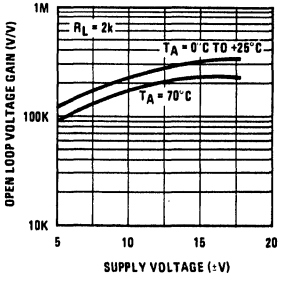
Power Supply Rejection Ratio



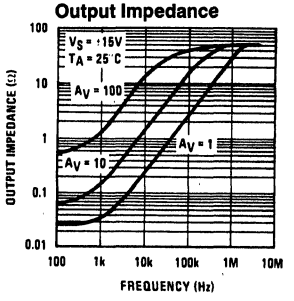
Equivalent Input Noise Voltage



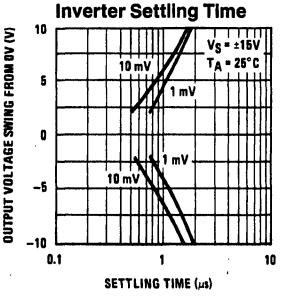
Open Loop Voltage Gain (V/V)



Output Impedance



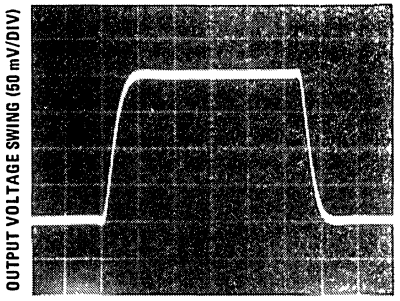
Inverter Settling Time



TL/H/5649–3

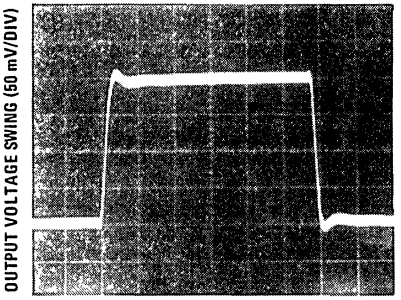
Pulse Response

Small Signaling Inverting



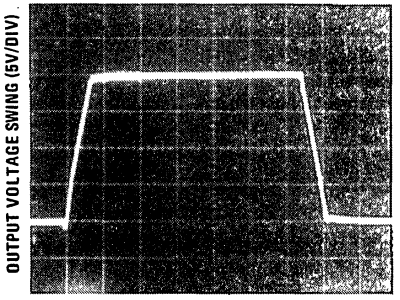
TL/H/5649–4

Small Signal Non-Inverting



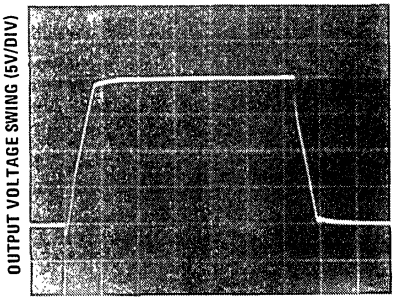
TL/H/5649–5

Large Signal Inverting



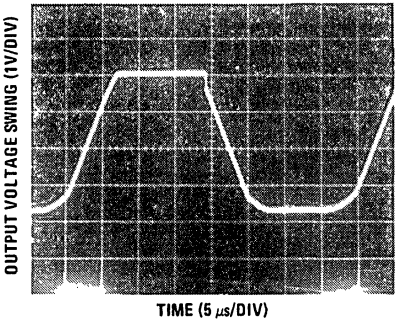
TL/H/5649–6

Large Signal Non-Inverting



TL/H/5649–7

Current Limit (R_L = 100Ω)



TL/H/5649–8

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

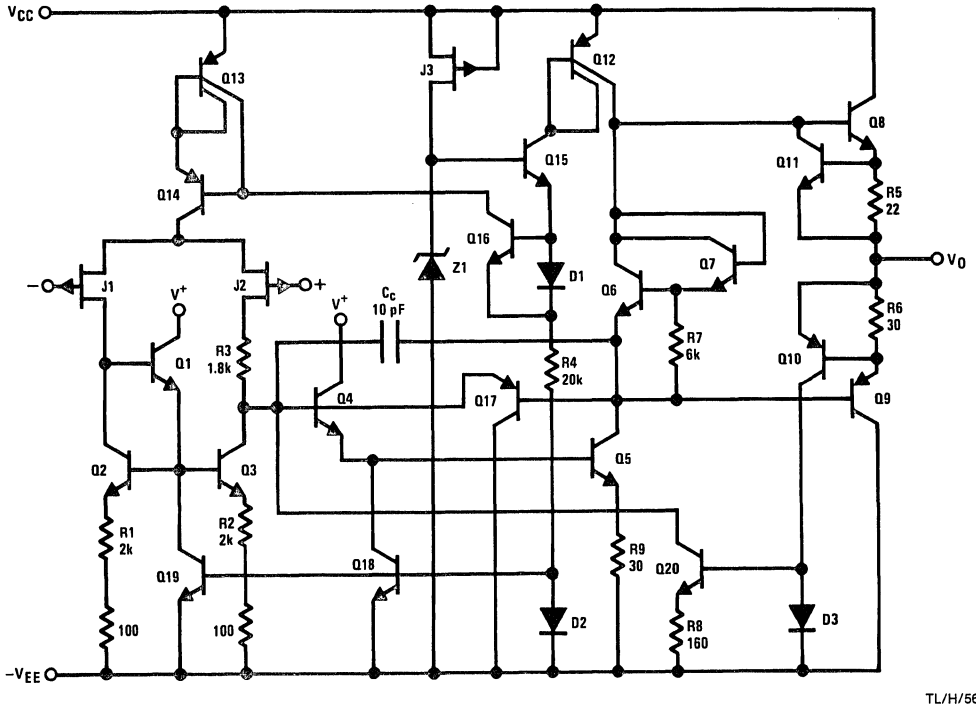
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through theresulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

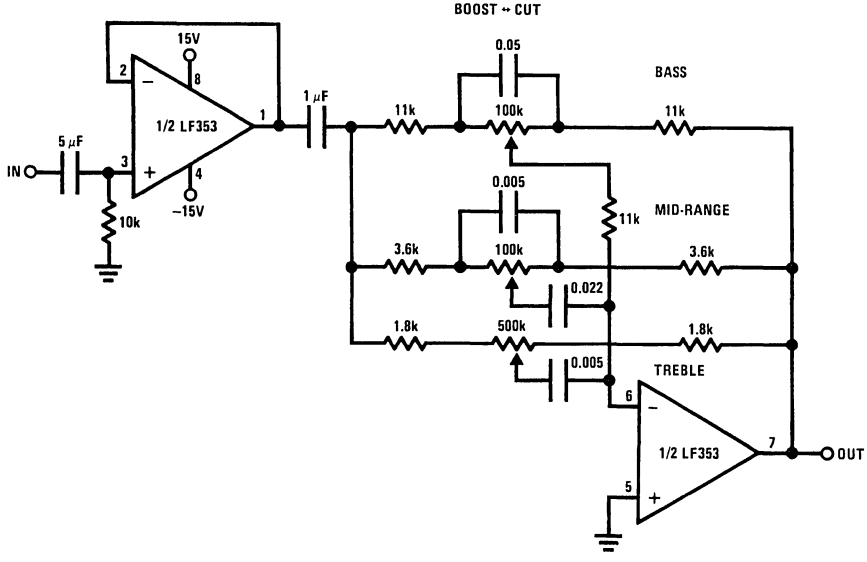
Detailed Schematic

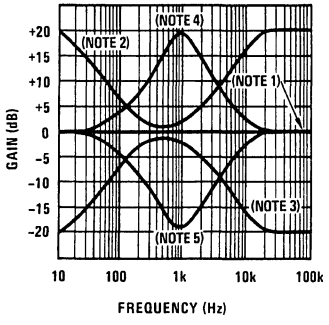


TL/H/5649–9

Typical Applications

Three-Band Active Tone Control





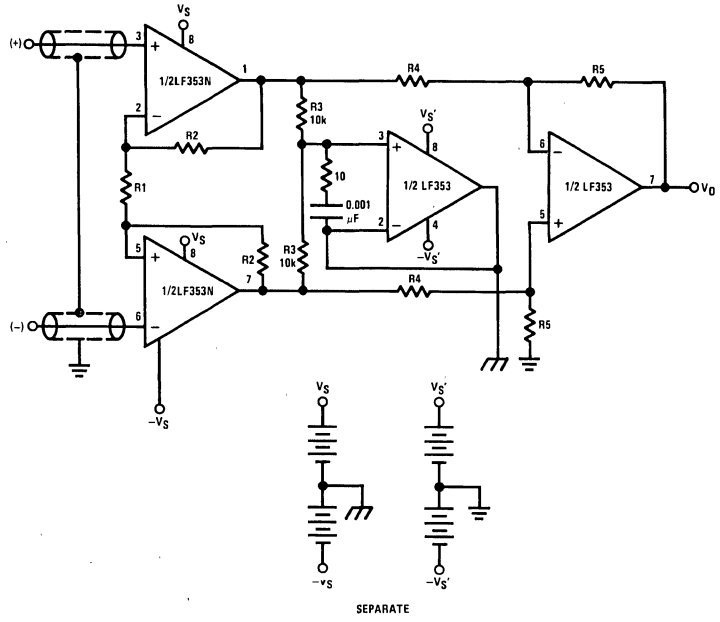
TL/H/5649–10

Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

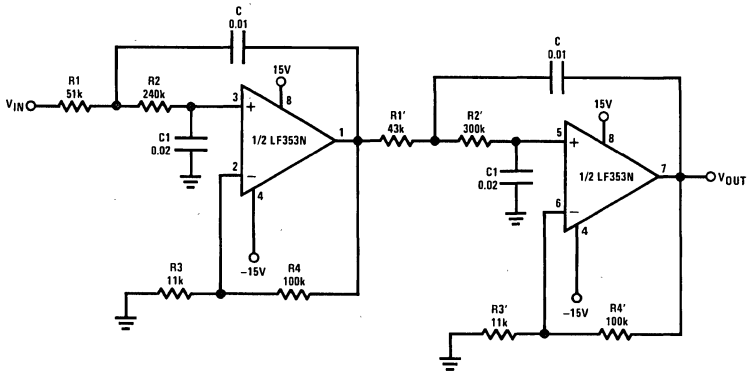
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

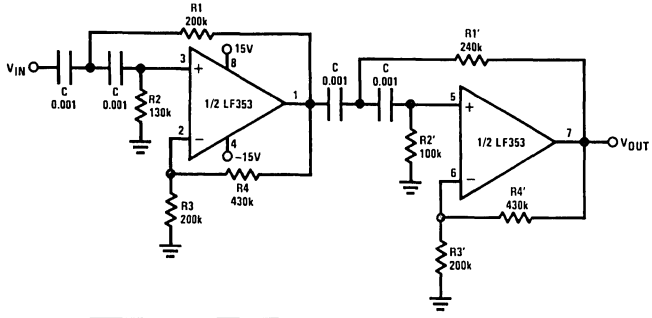


- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

TL/H/5649–11

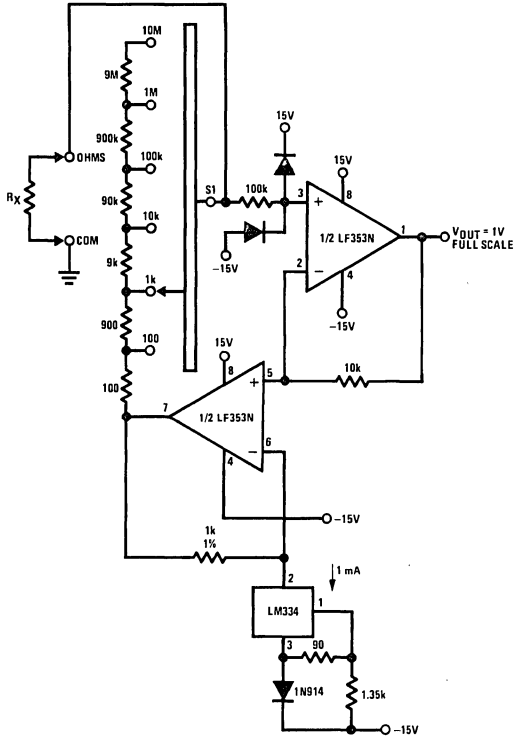
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency $(f_c) = \sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain $(H_O = (1 + R4/R3)\ (1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Ohms to Volts Converter

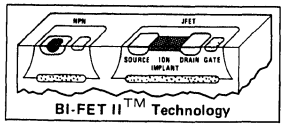


TL/H/5649–13

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

National Semiconductor



LF400A/LF400
Fast-Settling JFET-Input Operational Amplifier

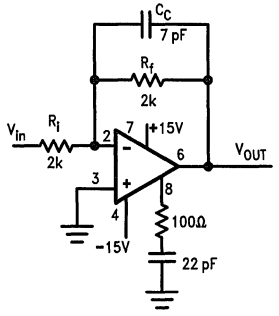
General Description

The LF400 is a fast-settling (under 400 ns to 0.01% for a 10V output step) Bi-FET operational amplifier. Features include 16 MHz bandwidth, 60V/μs inverting slew rate, low input offset voltage (0.5 mV for the LF400A at 25°C), and adjustable output current limit, enabling the amplifier to drive 600Ω loads.

Applications

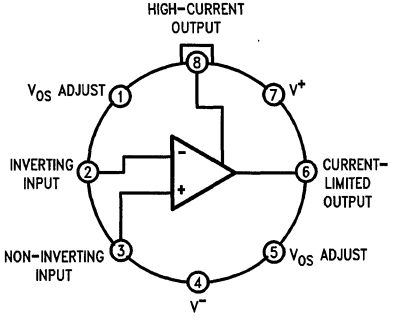
- DAC output amplifiers
- High speed ramp generators
- Fast buffers
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

Typical Connection



TL/H/9414–1

Connection Diagram

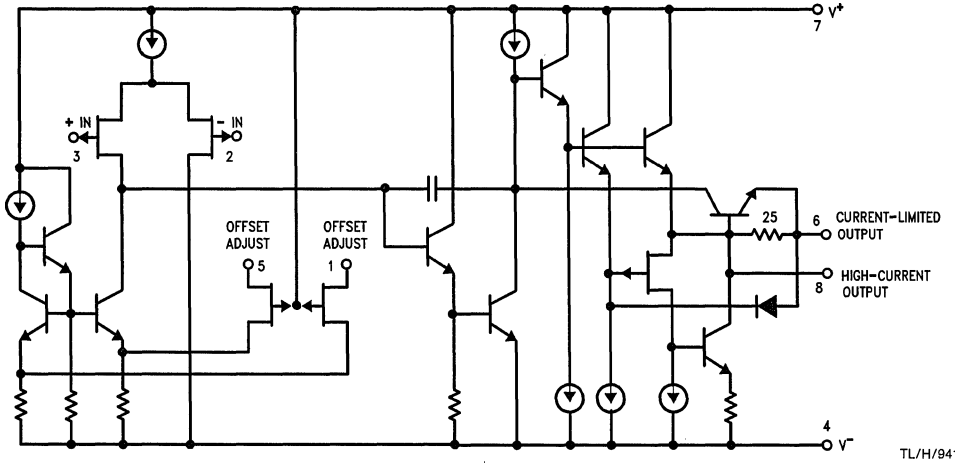


Note: Pin 4 connected to case. TL/H/9414–2

Top View

Order Number LF400ACH, LF400CH, LF400AMH or LF400MH
See NS Package Number H08B

Simplified Schematic



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±32V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration (Pin 6)	Continuous
Power Dissipation (Note 4) H package	500 mW
Junction Temperature (T_{JMAX})	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Susceptibility (Note 9)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF400AMH, LF400MH	$-55°C \le T_A \le +125°C$
LF400ACH, LF400CH	$0°C \le T_A \le +70°C$
Positive Supply Voltage	+10V to +16V
Negative Supply Voltage	−10V to −16V

AC Electrical Characteristics (LF400ACH, LF400CH)

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified.
Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX}; other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter	Conditions	LF400ACH			LF400CH			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Settling Time to 0.01% to 0.10%	See *Figure 1* See *Figure 1*	365 200			365 200			ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, $C_L = 10$ pF	16	14		16	14		MHz
SR	Minimum Slew Rate	$A_V = +1$, $C_L = 10$ pF	30	27		30	27		V/μs
		$A_V = -1$, $C_L = 10$ pF	60			60			V/μs
ϕ	Phase Margin	$A_V = +1$, $C_L = 10$ pF	60			60			Degrees
e_n	Input Noise Voltage	f = 1 kHz, $R_S = 100\Omega$ Broadband, $R_S = 100\Omega$, 10 Hz to 10 kHz	23 2.3			23 2.3			nV/√Hz μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 1.0			0.01 1.0			pA/√Hz pA rms
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -1$, $R_L = 10k$	0.002			0.002			%
C_{IN}	Input Capacitance		7			7			pF

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DC Electrical Characteristics (LF400ACH, LF400CH)

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified.
Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX}; other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter		Conditions		LF400ACH Typical (Note 6)	LF400ACH Tested Limit (Note 7)	LF400ACH Design Limit (Note 8)	LF400CH Typical (Note 6)	LF400CH Tested Limit (Note 7)	LF400CH Design Limit (Note 8)	Units
V_{OS}	Maximum Input Offset Voltage		V_{CM} = 0V,	T_J = 25°C		±0.5			±3.0		mV
			R_S = 0, R_L = ∞	T_J = 70°C		±2.0			±5.0		mV
I_{OS}	Maximum Input Offset Current		V_{CM} = 0V (Note 5)		±50	±100 **±2.5**		±50	±100 **±2.5**		pA nA
I_B	Maximum Input Bias Current		V_{CM} = 0V (Note 5)		100	200 **26**		100	200 **26**		pA nA
R_{IN}	Input Resistance				10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range				−12 to +14	±11		−12 to +14	±11		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 6	V_O = ±10V, R_L = 2 kΩ		300	100		300	100		V/mV
		Using Pin 8	V_O = ±10V, R_L = 600Ω		280	100		280	100		V/mV
V_O	Minimum Output Voltage Swing	Using Pin 6	R_L = 2 kΩ		±12.5	±12.0		±12.5	±12.0		V
		Using Pin 8	R_L = 600Ω		±12.0	±11.0		±12.0	±11.0		V
I_{SC}	Output Short Circuit Current		Pulse Test		25			25			mA
		MIN Using Pin 6				15			15		mA
		MAX Using Pin 6				45			45		mA
		MIN Using Pin 8				100			100		mA
R_O	Output Resistance	Using Pin 6	Open Loop, DC		75			75			Ω
		Using Pin 8	Open Loop, DC		50			50			Ω
CMRR	Minimum DC Common Mode Rejection Ratio		$-11V \le V_{IN} \le +11V$		100	90		100	80		dB
PSRR	Minimum DC Power Supply Rejection Ratio		$+10V \le V^+ \le +15V$, $-15V \le V^- \le -10V$, V_{CM} = 0V		100	90		100	80		dB
I_S	Maximum Supply Current		V_O = 0V, R_L = ∞		11.0	13.0		11.0	13.0		mA

AC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$

Symbol	Parameter	Conditions	LF400AMH			LF400MH			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Settling Time to 0.01% to 0.10%	See *Figure 1* See *Figure 1*	365 200			365 200			ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, $C_L = 10$ pF	16	14 **10**		16	14 **10**		MHz MHz
SR	Minimum Slew Rate	$A_V = +1$, $C_L = 10$ pF	30	**27**		30	**27**		V/μs
		$A_V = -1$, $C_L = 10$ pF	60			60			V/μs
ϕ	Phase Margin	$A_V = +1$, $C_L = 10$ pF	60			60			Degrees
e_n	Input Noise Voltage	f = 1 kHz, $R_S = 100\Omega$ Broadband, $R_S = 100\Omega$, 10 Hz to 10 kHz	23 2.3			23 2.3			nV/√Hz μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 1.0			0.01 1.0			pA/√Hz pA rms
THD	Total Harmonic Distortion	f = 1 kHz, $A_V = -1$, $R_L = 10k$	0.002			0.002			%
C_{IN}	Input Capacitance		7			7			pF

DC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$.

Symbol	Parameter		Conditions		LF400AMH			LF400MH			Unit
					Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage		$V_{CM} = 0V$, $R_S = 0$, $R_L = \infty$	$T_J = 25°C$		±0.5			±3.0		mV
						±2.0			**±5.0**		mV
I_{OS}	Maximum Input Offset Current		$V_{CM} = 0V$ (Note 5)		±50	±100 **±15**		±50	±100 **±25**		pA nA
I_B	Maximum Input Bias Current		$V_{CM} = 0V$ (Note 5)		100	200 **35**		100	200 **50**		pA nA
R_{IN}	Input Resistance				10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range				−12 to +14	**±11**		−12 to +14	**±11**		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 6	$V_O = \pm 10V$, $R_L = 2\ k\Omega$		300	**100**		300	**50**		V/mV
		Using Pin 8	$V_O = \pm 10V$, $R_L = 600\Omega$		280	**100**		280	**50**		V/mV

DC Electrical Characteristics (LF400AMH, LF400MH)

The following specifications apply for $V^+ = +15V$, $V^- = -15V$, and $T_J = 25°C$ unless otherwise specified.
Tested Limits in Boldface apply for $T_J = -55°C$ to $+125°C$. (Continued)

Symbol	Parameter		Conditions	LF400AMH			LF400MH			Units
				Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_O	Minimum Output Voltage Swing	Using Pin 6	$R_L = 2k\Omega$		±12.0			±12.0		V
				±12.5	**±11.5**		±12.5	**±11.5**		V
		Using Pin 8	$R_L = 600\Omega$	±12.0	**±11.0**		±12.0	**±11.0**		V
I_{SC}	Output Short Circuit Current		Pulse Test	25			25			mA
		MIN Using Pin 6			**15**			**15**		mA
		MAX Using Pin 6			**45**			**45**		mA
		MIN Using Pin 8			**100**			**100**		mA
R_O	Output Resistance	Using Pin 6	Open Loop, DC	75			75			Ω
		Using Pin 8	Open Loop, DC	50			50			Ω
CMRR	Minimum DC Common Mode Rejection Ratio		$-11V \le V_{IN} \le +11V$	100	90		100	80		dB
					80			**75**		dB
PSRR	Minimum DC Power Supply Rejection Ratio		$+10V \le V^+ \le +15V$, $-15V \le V^- \le -10V$, $V_{CM} = 0V$	100	90		100	80		dB
					85			**75**		dB
I_S	Maximum Supply Current		$V_O = 0V$, $R_L = \infty$	11.0	13.0		11.0	13.0		mA
					13.0			**15.0**		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to ground.

Note 3: Unless otherwise specified, the Absolute Minimum Input Voltage is equal to the negative power supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures as is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. θ_{JA} for the LF400H is 150°C/W in free air, so a heat sink will generally be required when T_A is greater than about 70°C. θ_{JC} for the LF400H is 17°C/W, which dictates the use of a heat sink with θ_{CA} less than about 35°C/W when $T_A = +125°C$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, input bias currents are measured at $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation P_D. Use of a heat sink is recommended when input bias current must be minimized.

Note 6: Typicals represent the most likely parametric norm.

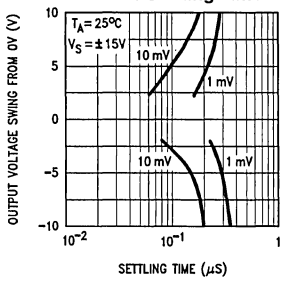
Note 7: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

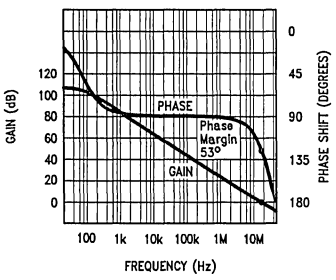
Note 9: Human body model, 100 pF discharged through a 1500Ω resistor.

Typical Performance Characteristics

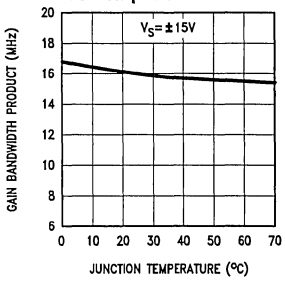
Inverter Settling Time



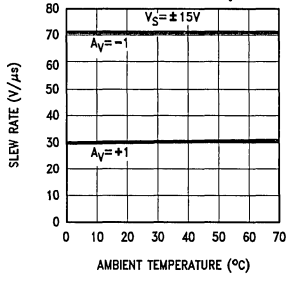
Bode Plot



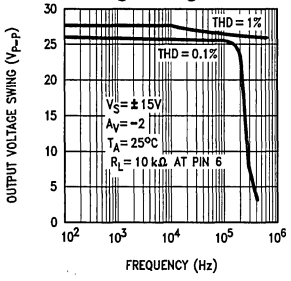
Gain Bandwidth vs Temperature



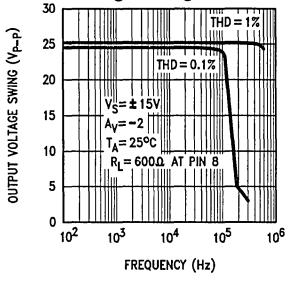
Slew Rate vs Temperature



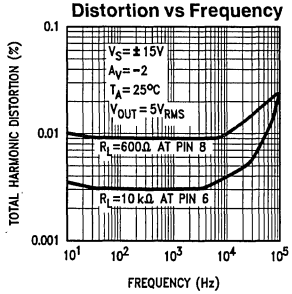
Undistorted Output Voltage Swing



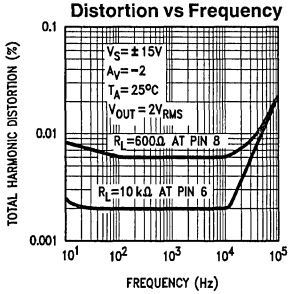
Undistorted Output Voltage Swing



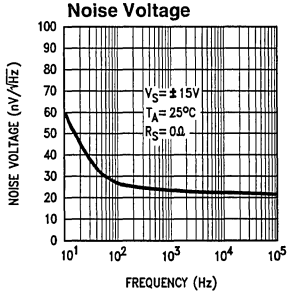
Distortion vs Frequency



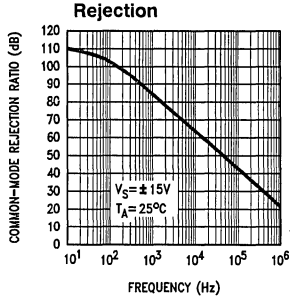
Distortion vs Frequency



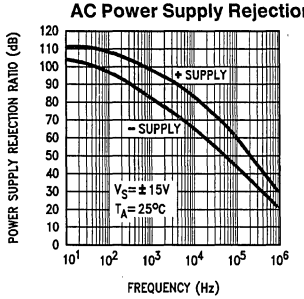
Equivalent Input Noise Voltage



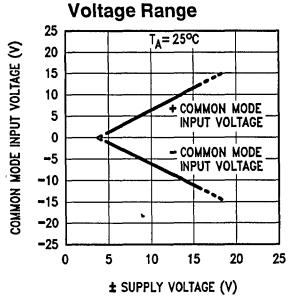
AC Common-Mode Rejection



AC Power Supply Rejection



Common-Mode Input Voltage Range



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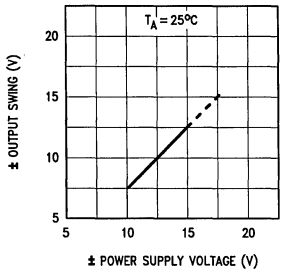
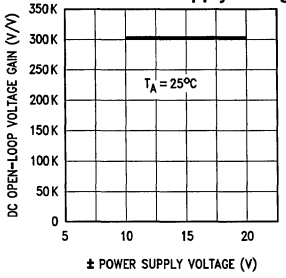
Typical Performance Characteristics (Continued)

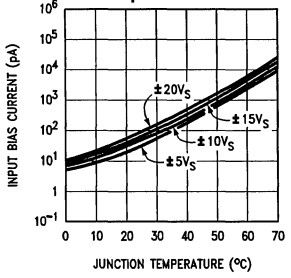
Output Voltage Swing vs Supply Voltage



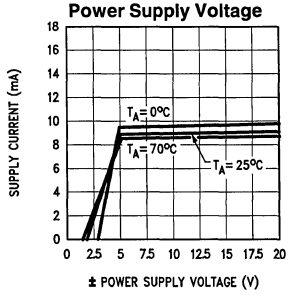
DC Gain vs Supply Voltage



Input Bias Current vs Temperature



Power Supply Current vs Power Supply Voltage



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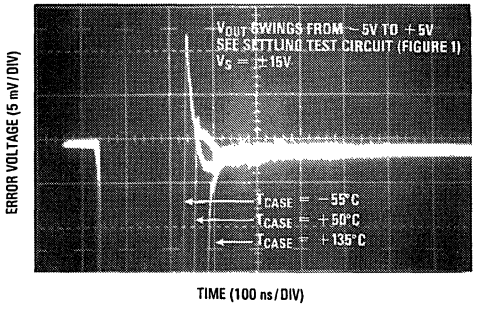
Settling Time—Positive Output Swing



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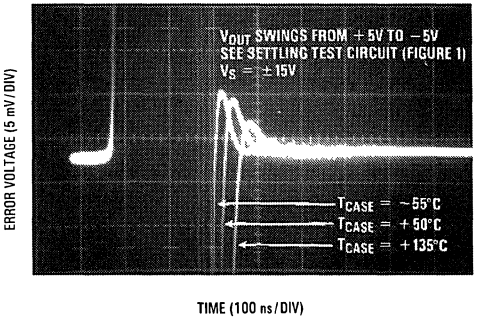
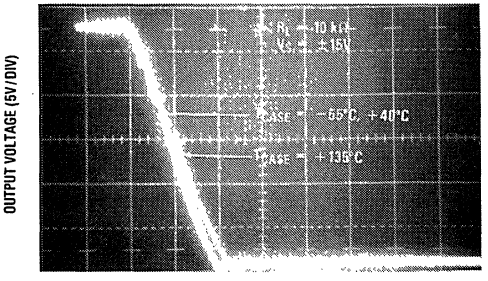
Settling Time—Negative Output Swing



TL/H/9414–13

Step Response



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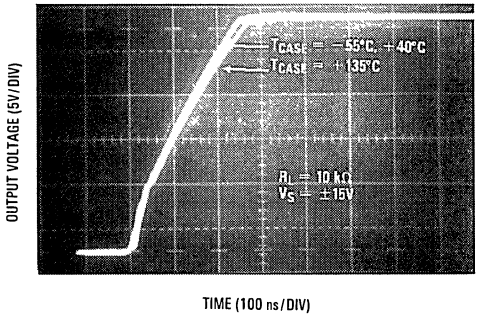
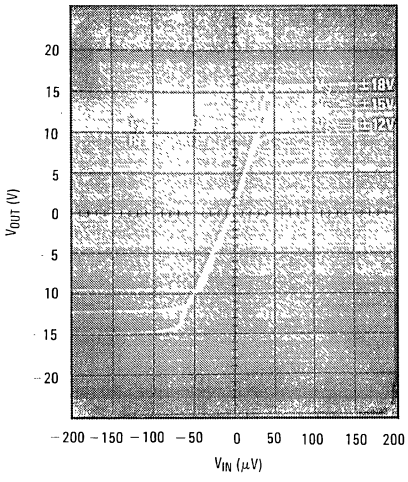
Typical Performance Characteristics (Continued)

Step Response



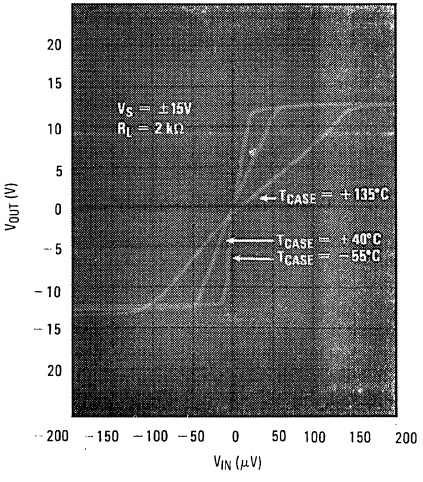
TL/H/9414–15

Voltage Transfer Characteristic

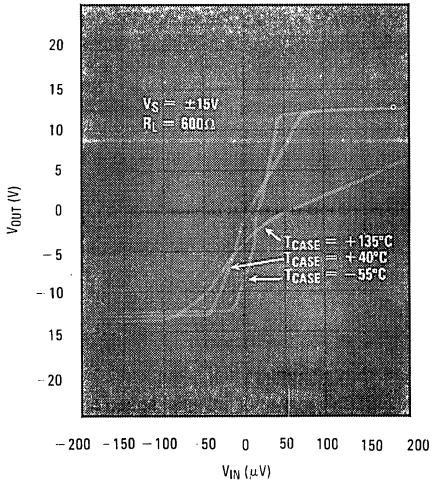


TL/H/9414–16

Voltage Transfer Characteristic



TL/H/9414–17

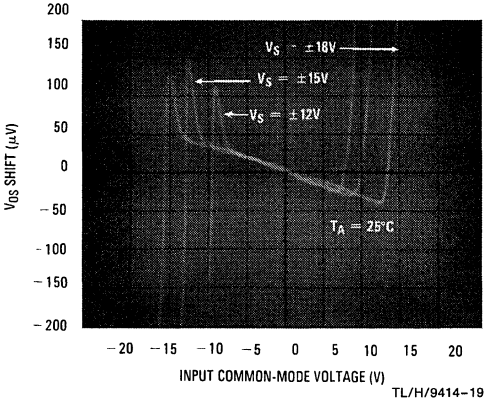


TL/H/9414–18

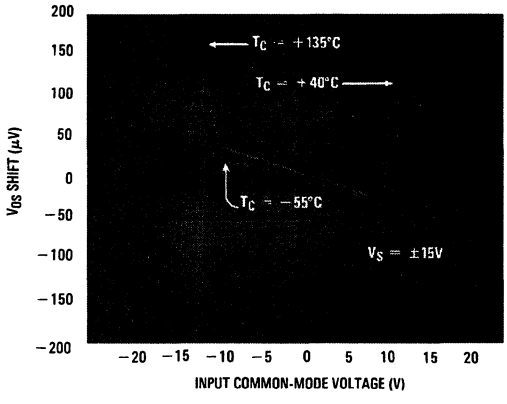
3

Typical Performance Characteristics (Continued)

Common—Mode Voltage Transfer Characteristic



TL/H/9414–19



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Application Hints

The LF400 is a high-speed, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the common-mode input range will not damage the device as long as the Absolute Maximum Ratings are not violated, but it will result in a high output voltage. Latching will not occur, however, and when the offending signal is removed the LF400 will recover quickly.

The nominal power supply voltage is ±15V, but the LF400 will operate satisfactorily from ±10V to ±16V. The LF400 is functional down to ±5V, but performance will be degraded. (See Typical Performance curves.)

Settling Time Considerations

The settling performance of any high-speed operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor C_C between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF400 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF400's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time—Positive Output Swing" and "Settling Time—Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than ½ mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF400's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for set-

Application Hints (Continued)

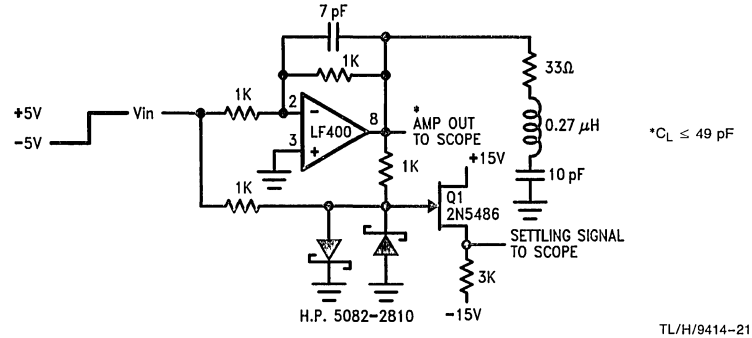

FIGURE 1. Simplified Settling Time Test Circuit (see Text)

tling time testing must be able to drive 50Ω with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

Output Compensation

When operating at very low temperatures, a compensation network should be added to the LF400's output. The 100Ω/22 pF network shown on the first page of this data sheet should be used when the junction temperature might reach 25°C (roughly 0°C ambient when the LF400 is "warmed up"). In applications where the device will be operating with a junction temperature near 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.

Supply Bypassing

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 μF tantalum, a 2.2 μF ceramic, and a 0.47 μF ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.

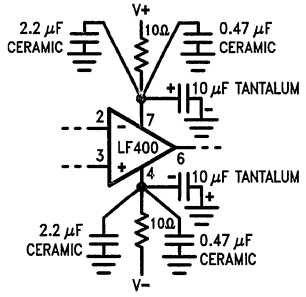

FIGURE 2. Power Supply Bypassing (see Text)

Output Drive and Current Limit

The LF400 can drive heavier resistive loads than most operational amplifiers. The output at pin 6 is internally current-limited when the voltage drop across the 25Ω output resistor reaches about 0.55V (I_{OUT} = 22 mA). When more output current is needed, pin 8 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 8 to pin 6, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 6 and 8 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF400, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.

The effective load impedance (including feedback resistance) should be kept above 500Ω for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1 kΩ to 2 kΩ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

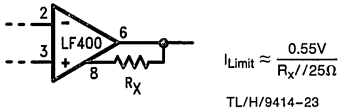

FIGURE 3. Increasing the current limit using pin 8. Current limit is now determined by R_X in parallel with the internal 25Ω sense resistor.

V_{OS} Adjustment

Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 5 as shown in *Figure 4a*. Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 5 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V^-.

Application Hints (Continued)

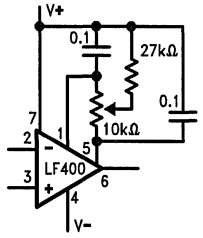

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FIGURE 4a. V_{OS} Adjust Circuit

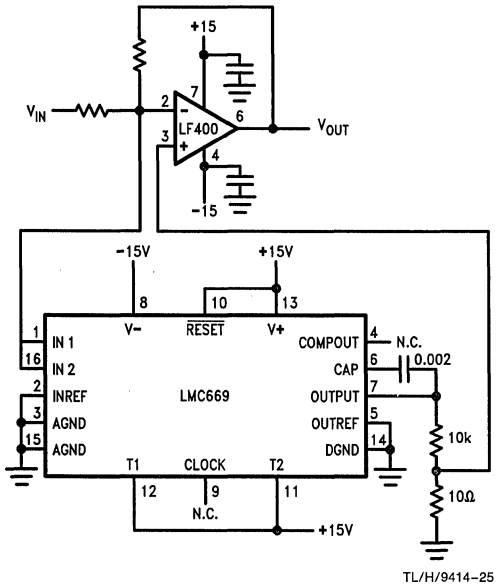

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FIGURE 4b. Automatic Offset Adjustment Using LMC669

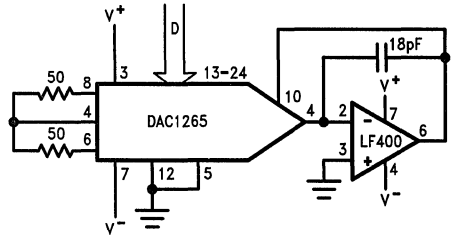
In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF400 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

Input Bias Current

The JFET input stage of the LF400 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF400. "Press on" heat sinks from manufacturers such as Thermalloy and AAVID can reduce junction temperature by roughly 10°C to 40°C.

Typical Applications

High-Speed DAC with Voltage Output



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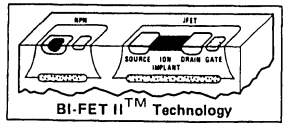
National Semiconductor



LF401/LF401A Precision Fast Settling JFET Input Operational Amplifier

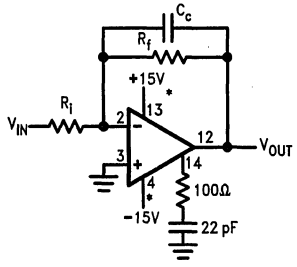
General Description

The LF401A is a fast settling (guaranteed under 400 ns to 0.01% for a 10V output step) BI-FET operational amplifier. The input offset voltage of the LF401A is guaranteed less than 200 μV maximum at 25°C. The LF401 also features 16 MHz bandwidth, 70 V/μs inverting slew rate and adjustable short circuit current limit, enabling it to drive 600Ω loads easily.

Applications

- DAC output amplifiers
- Fast buffers
- High speed ramp generators
- Sample-and-holds
- Fast integrators
- Piezoelectric transducer signal conditioners

Typical Connection



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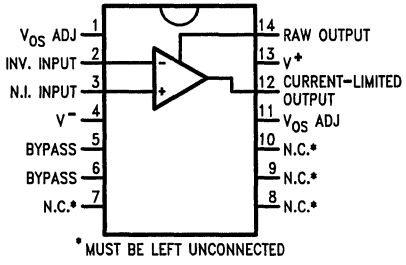
*See *Figure 2* for Power Supply Bypassing.

Connection Diagram

Dual-In-Line Package

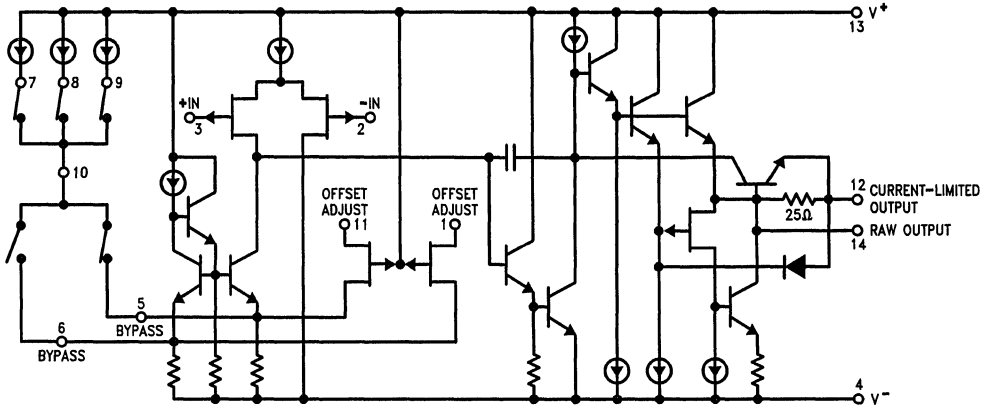


*MUST BE LEFT UNCONNECTED

TL/H/8839–2

Order Number LF401ACD or LF401CD
See NS Package Number D14E

Simplified Schematic



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V
Differential Input Voltage	±32V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration (Pin 12)	Continuous
Power Dissipation (Note 4) D package	500 mW
Junction Temperature (T_{JMAX})	115°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Susceptibility (Note 10)	500V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF401ACD, LF401CD	$0°C \le T_A \le +70°C$
Positive Supply Voltage	+10V to +16V
Negative Supply Voltage	−10V to −16V
Total Supply Voltage ($V^+ - V^-$)	20V to 32V

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX};** other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter	Conditions	LF401ACD			LF401CD			Unit
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
t_s	Maximum Settling Time to 0.01% to 0.10%	See *Figure 1*, $C_L \le 50$ pF See *Figure 1*, $C_L \le 50$ pF	335 200	400		335 200	500		ns ns
GBW	Minimum Gain Bandwidth Product	$A_V = +1$, $C_L = 10$ pF, f = 100 kHz	16	14		16	14		MHz
SR	Minimum Slew Rate	$A_V = +1$, $C_L = 10$ pF		27			27		V/μs
		$A_V = -1$, $C_L = 10$ pF	70			70			V/μs
ϕ	Minimum Phase Margin	$A_{VOL} = +1$, $C_L = 10$ pF	60			60			°
e_n	Input Noise Voltage	f = 1 KHz, Rs = 100Ω Broadband, Rs = 100Ω, 10 Hz to 10 kHz	23 2.3			23 2.3			nV/√Hz μV rms
i_n	Input Noise Current	f = 1 kHz Broadband 10 Hz to 10 kHz	0.01 2.0			0.01 2.0			pA/√Hz pA rms
THD	Total Harmonic Distortion (Max)	f = 1 kHz, Av = −1, R_L = 10k	0.002			0.002			%
CIN	Input Capacitance	Differential	7			7			pF

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$ unless otherwise specified. **Tested Limits in Boldface apply for T_J = 25°C to 95°C. Design Limits in Boldface apply for $T_A = T_{MIN}$ to T_{MAX};** other Design Limits are for T_A = 25°C; all other limits for T_J = 25°C.

Symbol	Parameter		Conditions		LF401ACD Typical (Note 6)	LF401ACD Tested Limit (Note 7)	LF401ACD Design Limit (Note 8)	LF401CD Typical (Note 6)	LF401CD Tested Limit (Note 7)	LF401CD Design Limit (Note 8)	Unit
V_{OS}	Maximum Input Offset Voltage (Note 9)		V_{CM} = 0V, R_S = 0, R_L = ∞	T_A = 25°C T_A = 70°C		±200 ±600			±500 ±1500		μV μV
I_{OS}	Maximum Input Offset Current		V_{CM} = 0V, (Note 5)			±100	±400 **±2.5**		±100	±400 **±2.5**	pA nA
I_B	Maximum Input Bias Current		V_{CM} = 0V, (Note 5)			200	 **26**		200	 **26**	pA nA
R_{IN}	Input Resistance		T_J = 25°C		10^{11}			10^{11}			Ω
V_{CM}	Input Common-Mode Voltage Range				+14/−12	±11		+14/−12	±11		V
A_{VOL}	Minimum Large Signal Voltage Gain	Using Pin 12 Using Pin 14	V_o = ±10V, R_L = 2 kΩ V_o = ±10V, R_L = 600Ω		300 300	100 100		300 300	100 100		V/mV V/mV
V_o	Minimum Output Voltage Swing	Using Pin 12 Using Pin 14	R_L = 2 kΩ R_L = 600Ω		±12.5 ±12	±12 ±11		±12.5 ±12	±12 ±11		V V
I_{SC}	Output Short Circuit Current	MIN Using Pin 12 MAX Using Pin 12 MIN Using Pin 14	Pulse Test			15 45 100			15 45 100		mA mA mA
R_O	Output Resistance	Using Pin 12 Using Pin 14	Open Loop, DC Open Loop, DC		75 50			75 50			Ω Ω
CMRR	Minimum DC Common Mode Rejection Ratio		−11V ≤ V_{IN} ≤ +11V		100	90		100	80		dB
PSRR	Minimum DC Power Supply Rejection Ratio		+10V ≤ V^+ < +15V, −15V ≤ V^- < −10V, V_{CM} = 0V		100	90		100	80		dB
I_S	Maximum Supply Current		V_o = 0V, R_L = ∞		9	12		9	12		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to ground.

Note 3: Unless otherwise specified, the Absolute Maximum Negative Input Voltage is equal to the negative power supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or 500 mW, whichever is less. θ_{JA} for the LF401D is typically 87°C/W.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, input bias currents are measured at T_J = 25°C. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation P_D. Use of a heat sink is recommended when input bias current must be minimized.

Note 6: Typicals represent the most likely parametric norm.

Note 7: Guaranteed to National's AOQL (Average Outgoing Quality Level).

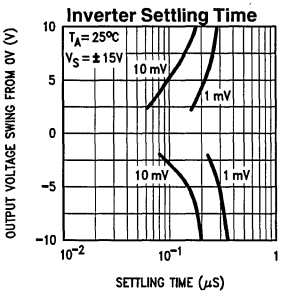
Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 9: Tested and correlated to a 10 minute warm up period.

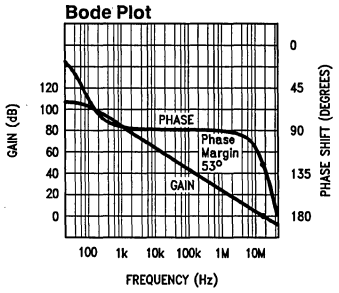
Note 10: Human body model, 100 pF discharged through a 1500Ω resistor.

Typical Performance Characteristics

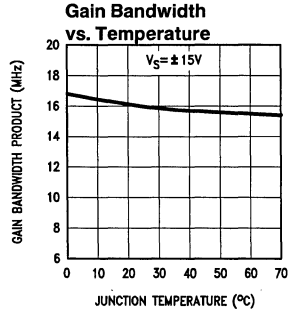
Inverter Settling Time



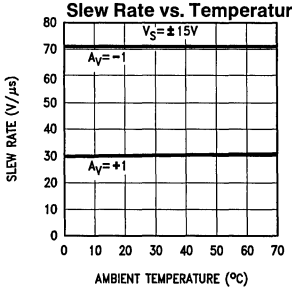
Bode Plot



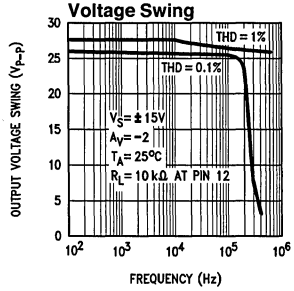
Gain Bandwidth vs. Temperature



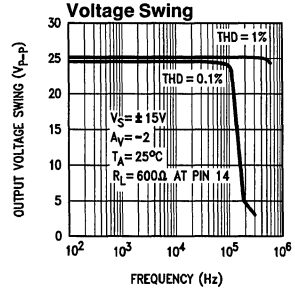
Slew Rate vs. Temperature



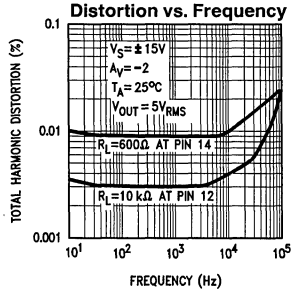
Undistorted Output Voltage Swing



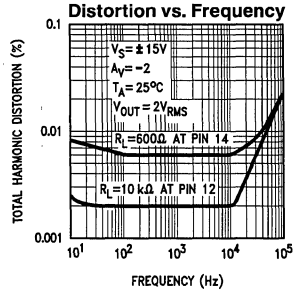
Undistorted Output Voltage Swing



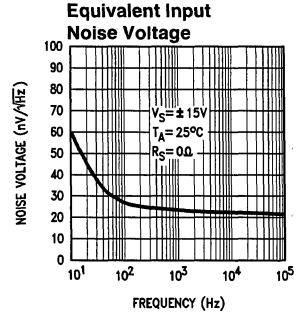
Distortion vs. Frequency



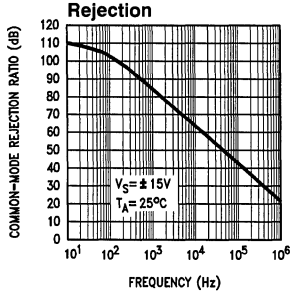
Distortion vs. Frequency



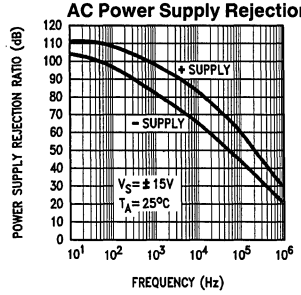
Equivalent Input Noise Voltage



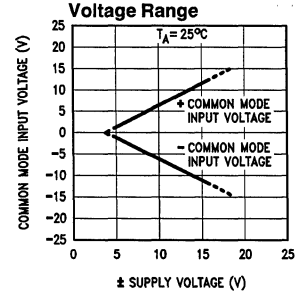
AC Common-Mode Rejection



AC Power Supply Rejection



Common-Mode Input Voltage Range



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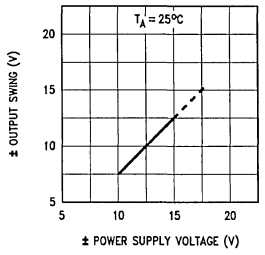
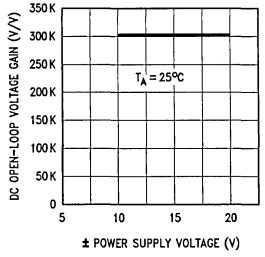
Typical Performance Characteristics (Continued)

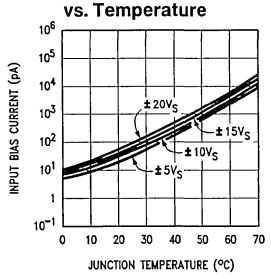
Output Voltage Swing vs. Supply Voltage



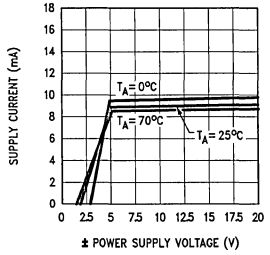
DC Gain vs. Supply Voltage



Input Bias Current vs. Temperature

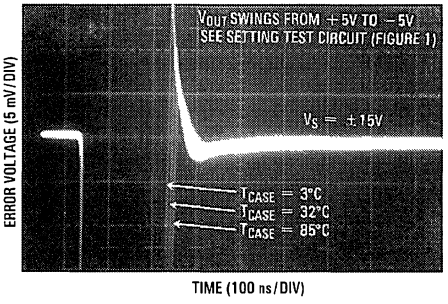


Power Supply Current vs. Power Supply Voltage



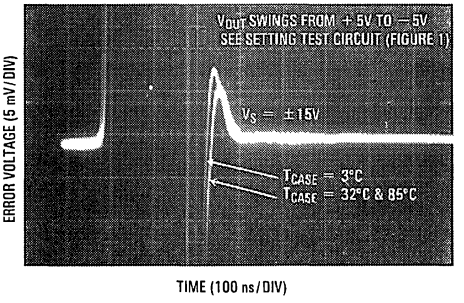
TL/H/8839–5

Settling Time—Positive Output Swing



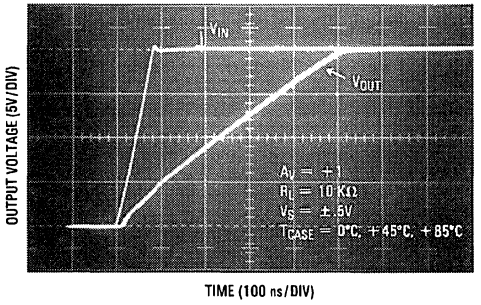
TL/H/8839–6

Settling Time—Negative Output Swing



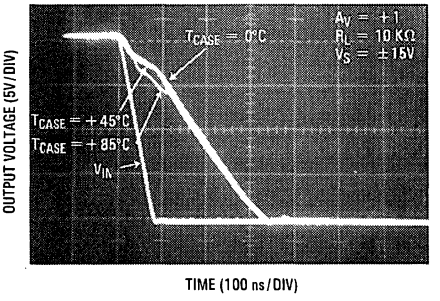
TL/H/8839–7

Step Response



TL/H/8839–22

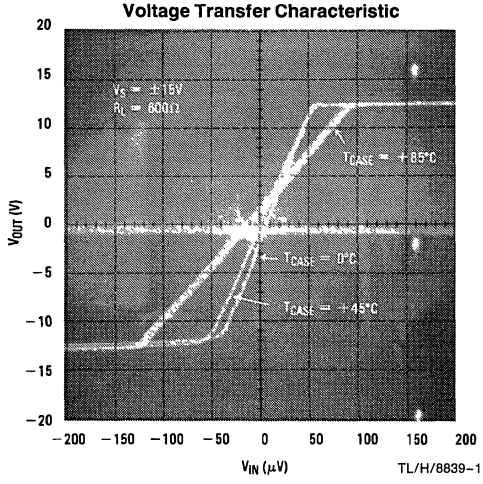
Step Response



TL/H/8839–9

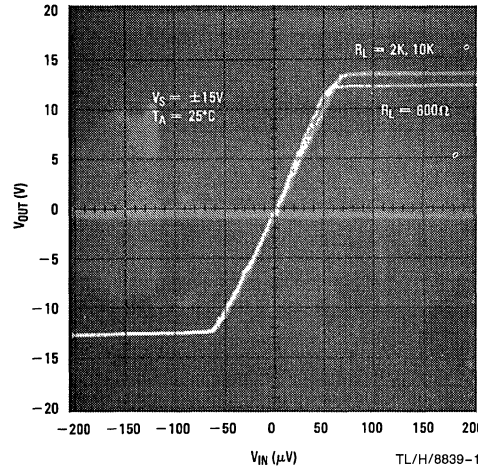
Typical Performance Characteristics (Continued)

Voltage Transfer Characteristic



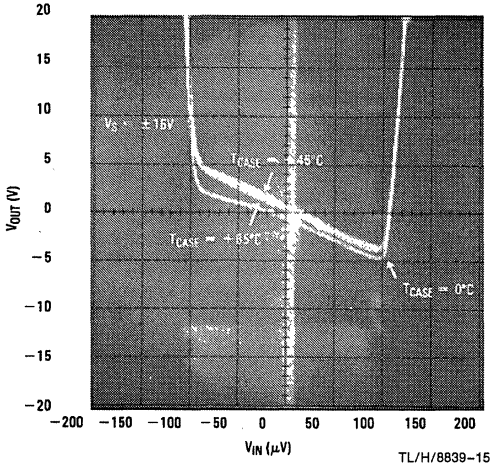
TL/H/8839–11

Voltage Transfer Characteristic



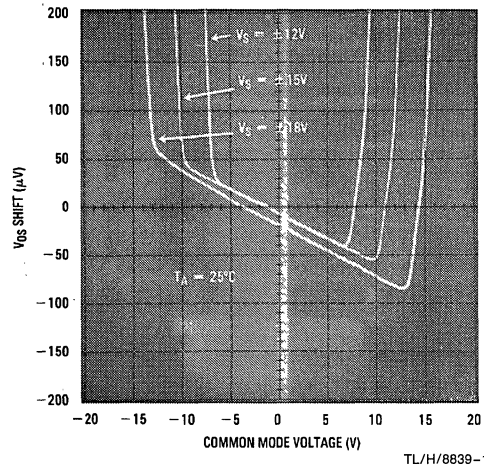
TL/H/8839–12

Common Mode Voltage Transfer Characteristic



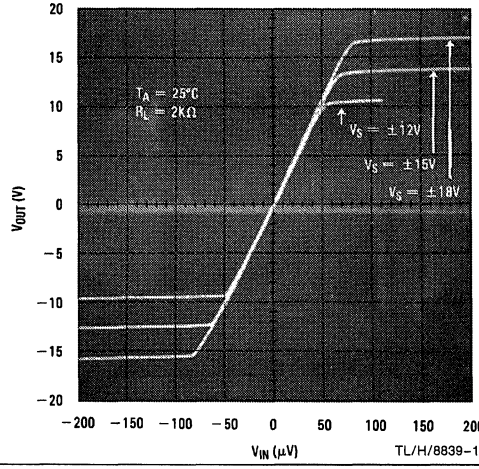
TL/H/8839–15

Common Mode Voltage Transfer Characteristic



TL/H/8839–14

Voltage Transfer Characteristic



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Application Hints

The LF401 is a high-speed, low offset, low input bias current Bi-FET operational amplifier capable of settling to 0.01% of a 10V output swing in less than 400 ns. Input offset voltage at room temperature is less than 200 μV for LF401A. The rugged JFET inputs allow differential input voltages as high as 32V without a large increase in input current. However, the inputs should never be driven to voltages lower than the negative supply, as this can result in input currents large enough to damage the device. To prevent this from occurring when power is first applied, always turn the positive and negative power supplies on simultaneously, or turn the negative supply on first.

Exceeding the positive common-mode input range will not damage the device as long as the Absolute Maximum ratings are not violated, but if both inputs exceed the positive common-mode range the output voltage will go high. Latching will not occur, however, and when the offending signal is removed the LF401 will recover quickly.

The nominal power supply voltage is ±15V, but the LF401 will operate satisfactorily from ±10V to ±16V. The LF401 is functional down to ±5V, but performance will be degraded at low supply voltages. (See Typical Performance curves.)

SETTLING TIME CONSIDERATIONS

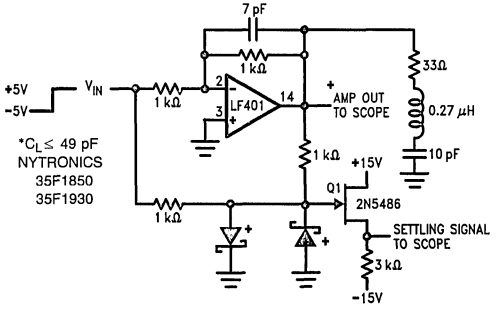
The settling performance of any fast operational amplifier is highly dependent on the external components and circuit board layout. Capacitance between the amplifier summing junction and ground affects the closed-loop transfer function and should be minimized. The compensation capacitor C_C between the output and the inverting input should be carefully chosen to counteract the effect of the input capacitance. Since input capacitance is made up of several stray capacitances that are difficult to predict, the compensation capacitor will generally have to be determined empirically for best settling time. A good starting point is around 10 pF for $A_V = -1$.

Settling time may be verified using a circuit similar to the one in *Figure 1*. The LF401 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LF401's output voltage is equal to the input voltage, the voltage on the gate of Q1 will be zero. Any voltage appearing at this point will represent an error. The FET source follower output is observed on an oscilloscope, and the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (see oscilloscope photos of "Settling Time — Positive Output Swing" and "Settling Time — Negative Output Swing"). For a 10V input signal, settling time to 0.01% (1 mV) will occur when the displayed error is less than 1/2 mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LF401's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier will be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. Very few oscilloscopes are suitable for this sort of measurement. The signal generator used for settling time testing must be able to drive 50Ω with a very clean ±5V square wave. For more information on measuring settling time, see Application Note AN-428.

OUTPUT COMPENSATION

When operating at very low temperatures, a compensation network should be connected to the LF401's "raw" output pin. The 100Ω/22 pF network shown on the first page of this data sheet should be connected to pin 14 in applications where the junction temperature might go as low as 25°C (roughly 0°C ambient when the LF401 is "warmed up"). In applications where the device will be operating with a junction temperature down to 0°C, the output RLC network in *Figure 1* should be used. This network will provide a small (about 20 ns) improvement in settling time at higher temperatures, as well.



TL/H/8839–16

+H.P. 5082-2810

FIGURE 1. Simplified Settling Time Test Circuit (See Text)

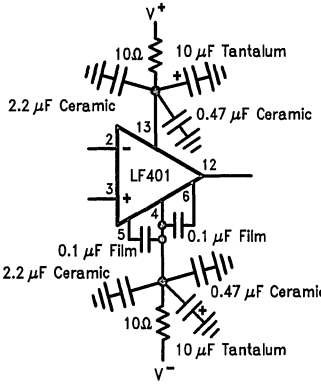


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FIGURE 2. Power Supply Bypassing (See Text)

SUPPLY BYPASSING

Power supply bypassing is extremely important for good high-speed performance. Ideally, multiple bypass capacitors as in *Figure 2* should be used. A 10 μF tanatalum, a 2.2 μF

Application Hints (Continued)

ceramic, and a 0.47 μF ceramic work well. All bypass capacitor leads should be very short. For best results, the ground leads of the capacitors should be separated to reduce the inductance to ground. A ground plane layout approach will give the best results. For simplicity, bypass capacitors have been omitted from some of the schematics in this data sheet, but they should always be used.

Pins 5 through 10 are used to trim the LF401's input offset voltage during the manufacturing process. Always leave pins 7 through 10 open, as signals applied to these pins will affect the amplifier output and can permanently degrade V_{OS}. For fastest settling time to 0.01%, pins 5 and 6 should be bypassed to pin 4 with 0.1 μF capacitors; otherwise, the LF401 may take an additional 600 ns to settle. The bypass capacitors should be low-leakage film types; otherwise the offset voltage can be increased. Settling time to 0.1% will be unaffected by bypassing these pins, so they may be left unconnected in applications requiring less precision.

OUTPUT DRIVE AND CURRENT LIMIT

The LF401 can drive heavier resistive loads than most operational amplifiers. The output at pin 12 is internally current-limited when the voltage drop across the 25Ω output resistor reaches about 0.55V (I_{out} = 22 mA). When more output current is needed, pin 14 provides a means of increasing the maximum output current up to about 100 mA. A resistor may be connected from pin 12 to pin 14, paralleling the internal sense resistor and increasing the current limit threshold (*Figure 3*). Pins 12 and 14 may be shorted together to completely bypass the current limiting circuit. To avoid damaging the LF401, observe the power dissipation limitations mentioned in the Absolute Maximum Ratings and in Note 4.

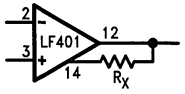

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FIGURE 3. Increasing the current limit using pin 14. Current limit is now determined by R_X in parallel with the internal 25Ω sense resistor.

The effective load impedance (including feedback resistance) should be kept above 500Ω for fastest settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1k to 2 kΩ range wherever practical. Avoid the use of inductive feedback resistors (some wirewounds for example) as these will degrade settling time.

V_{OS} ADJUSTMENT

Offset voltage can be nulled using a 27k resistor and a 10k potentiometer connected to pins 1 and 11 as shown in *Figure 4a*. Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 1 and 11 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V^-.

In very critical applications where a manual adjustment is impractical, the LMC669 Auto Zero circuit may be used to reduce the effective input offset voltage to around 5 μV as in *Figure 4b*. The LF401 will perform better than slower amplifiers in an auto zero loop, because its fast settling capability keeps its summing node voltage more stable. Therefore, the LMC669 is able to more accurately sample the summing node voltage before making an offset correction.

INPUT BIAS CURRENT

The JFET input stage of the LF401 ensures low input bias current (200 pA maximum) when the die is at room temperature, but this current approximately doubles for every 10°C increase in temperature. In applications that demand the lowest possible input bias current, a heat sink should be used with the LF401. "Slide on" heat sinks such as the AAVID 5602B can reduce the junction temperature by about 10°C.

Application Hints (Continued)

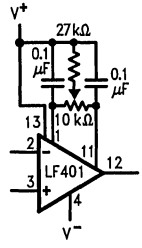

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FIGURE 4a. V_{OS} Adjust Circuit

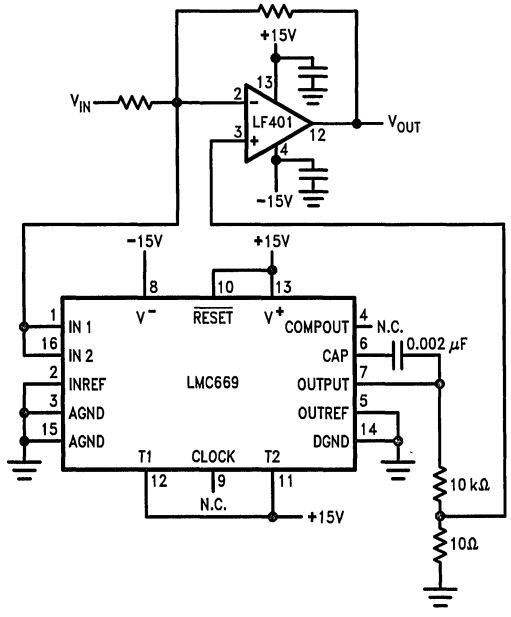

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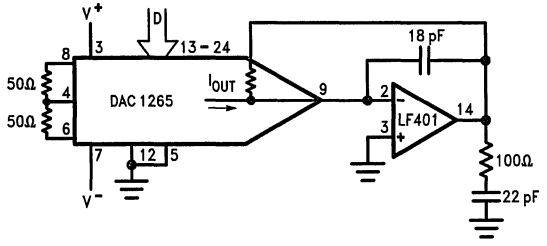
FIGURE 4b. Automatic Offset Adjustment Using LMC669

Typical Applications

High-Speed DAC with Voltage Output
(See *Figure 2* for Recommended Bypass Components)



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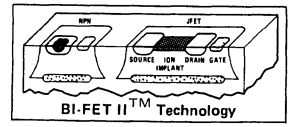
National Semiconductor



LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

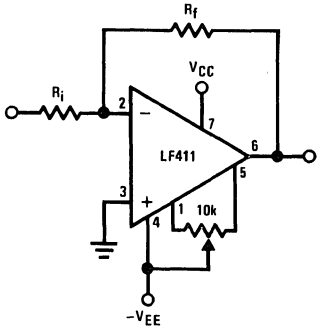
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

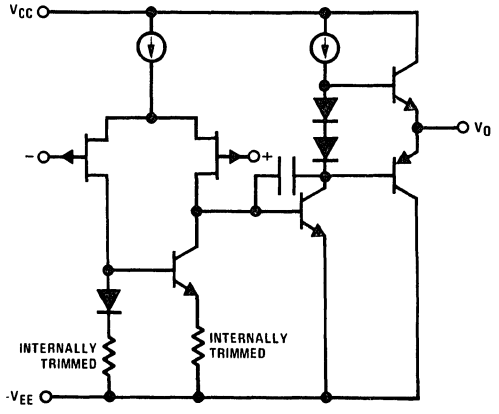
■ Internally trimmed offset voltage	0.5 mV(max)
■ Input offset voltage drift	10 μV/°C(max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz(min)
■ High slew rate	10V/μs(min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5655–1

Simplified Schematic



TL/H/5655–6

Ordering Information

LF411XYZ

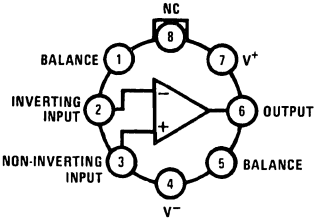
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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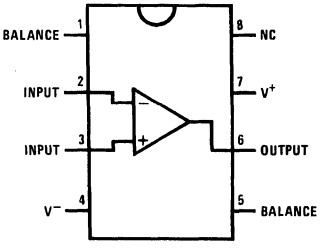
Top View

Note: Pin 4 connected to case.

Order Number LF411AMH, LF411MH, LF411ACH or LF411CH

See NS Package Number H08B

Dual-In-Line Package



TL/H/5655–7

Top View

Order Number LF411ACN or LF411CN

See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 3)	(Note 3)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		7	20 (Note 5)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

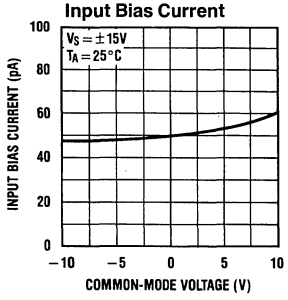
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15V$ to $\pm 5V$ for the LF411 and from $\pm 20V$ to $\pm 5V$ for the LF411A.

Note 8: Refer to RETS 411AX for LF411AMH military specifications and to RETS 411X for LF411MH military specifications.

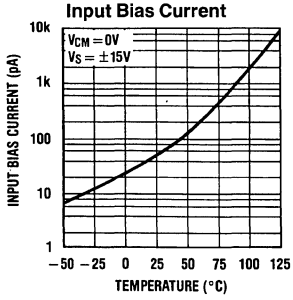
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

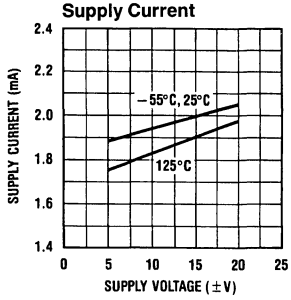
Input Bias Current



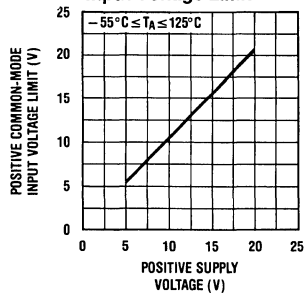
Input Bias Current



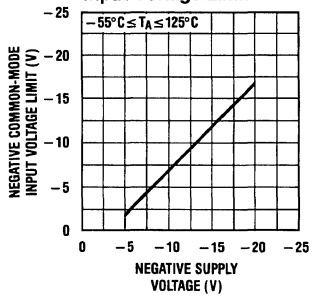
Supply Current



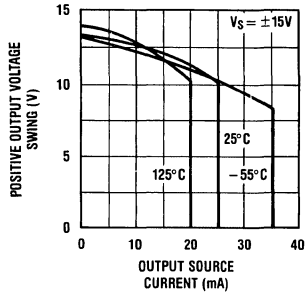
Positive Common-Mode Input Voltage Limit



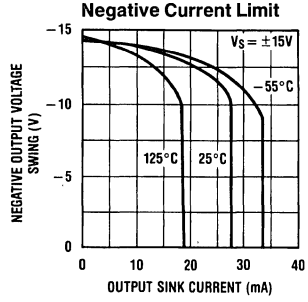
Negative Common-Mode Input Voltage Limit



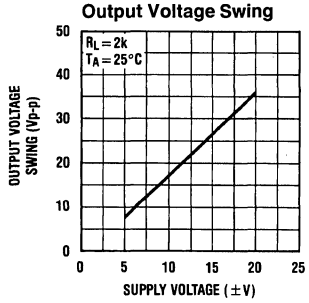
Positive Current Limit



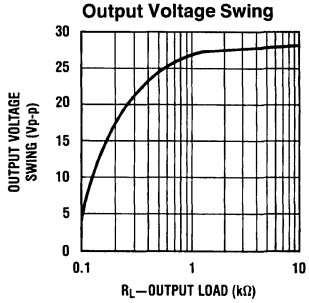
Negative Current Limit



Output Voltage Swing



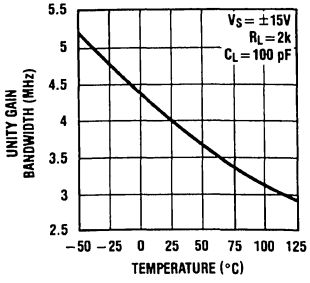
Output Voltage Swing



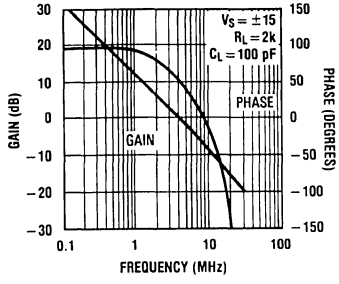
TL/H/5655–2

Typical Performance Characteristics (Continued)

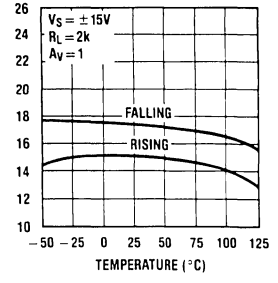
Gain Bandwidth



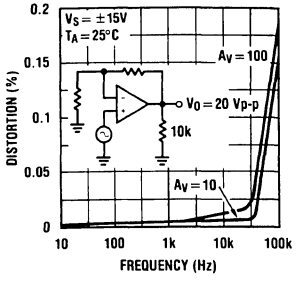
Bode Plot



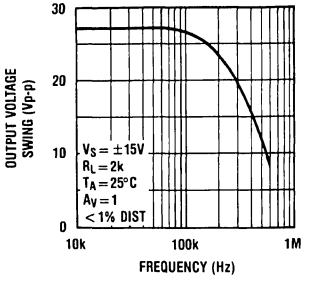
Slew Rate



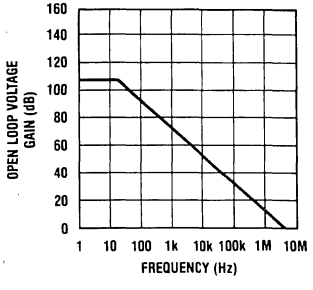
Distortion vs Frequency



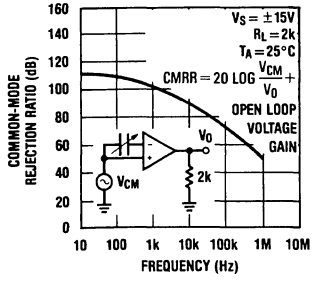
Undistorted Output Voltage Swing



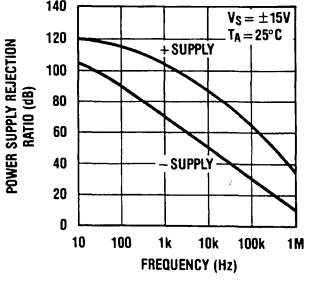
Open Loop Frequency Response



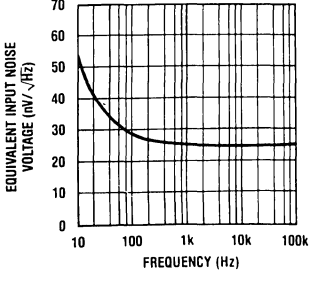
Common-Mode Rejection Ratio



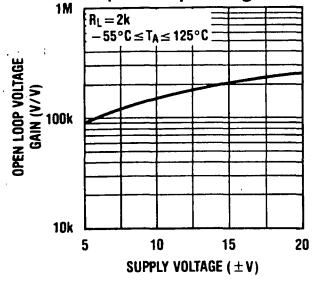
Power Supply Rejection Ratio



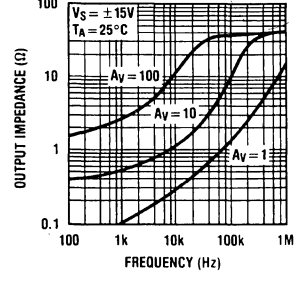
Equivalent Input Noise Voltage



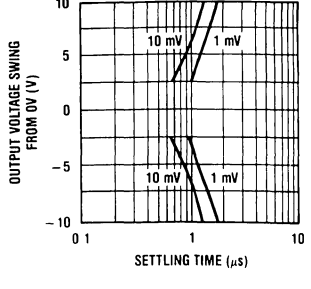
Open Loop Voltage Gain



Output Impedance



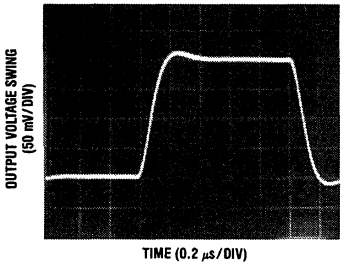
Inverter Settling Time



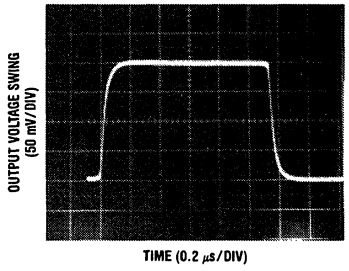
TL/H/5655–3

Pulse Response $R_L = 2\,k\Omega$, C_L 10 pF

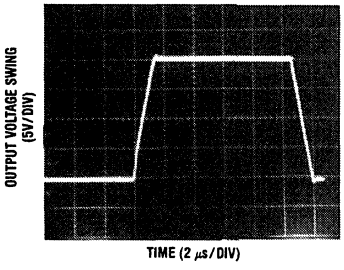
Small Signal Inverting



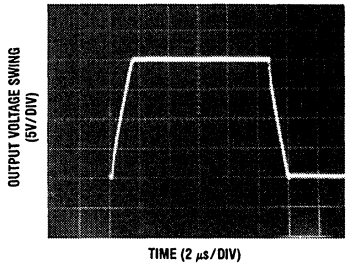
Small Signal Non-Inverting



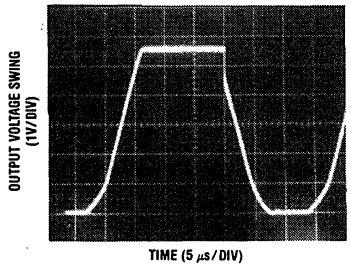
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655–4

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

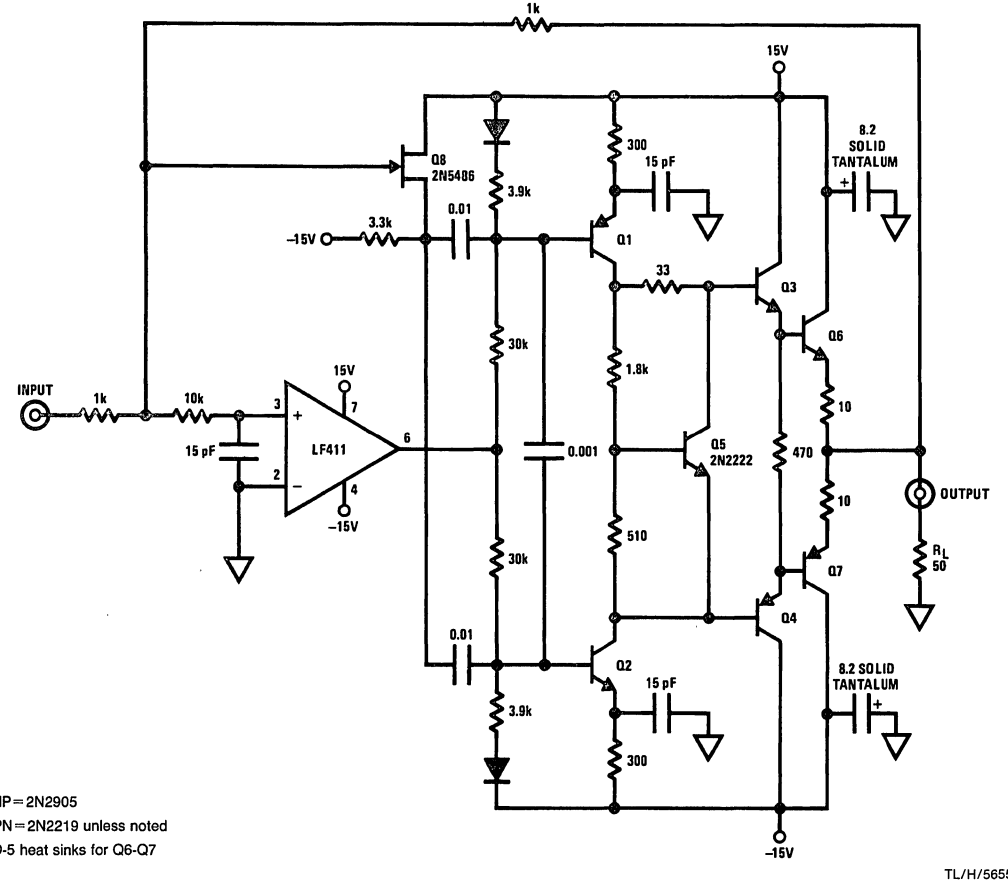
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Ultra High Speed Current Booster

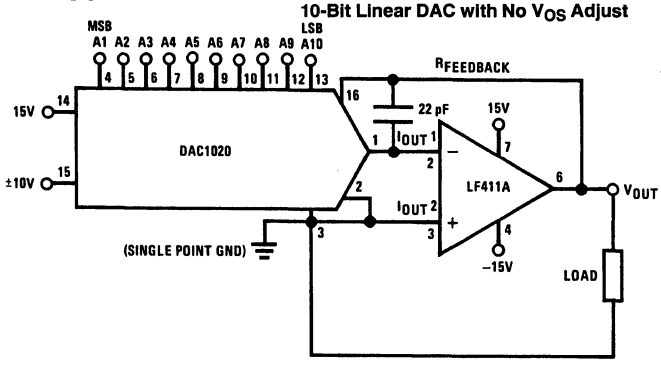


PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

TL/H/5655–9

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

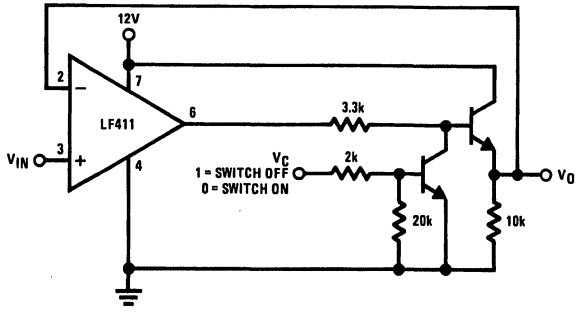
$-10V \le V_{REF} \le 10V$

$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$

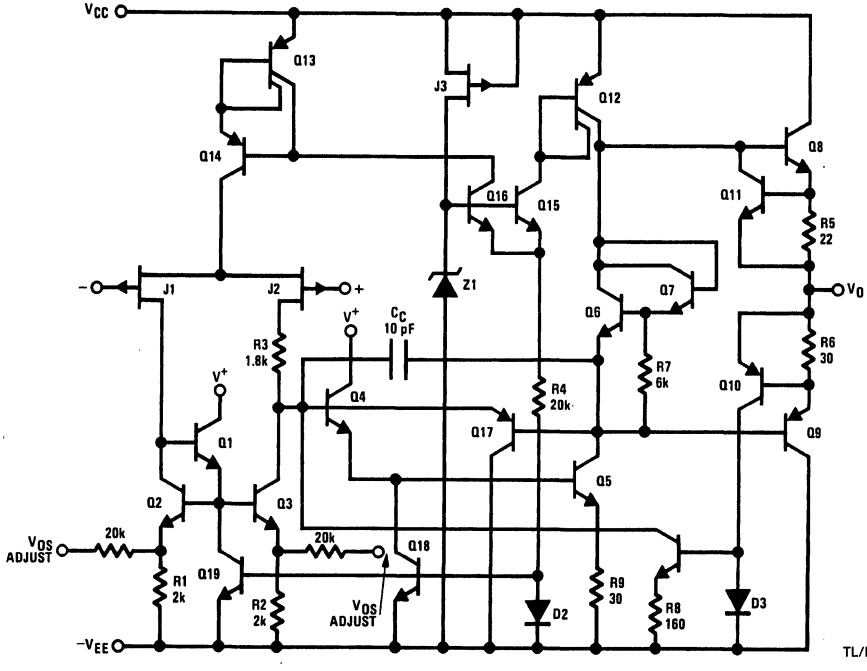
where $A_N = 1$ if the A_N digital input is high

$A_N = 0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output



Detailed Schematic



TL/H/5655–10

National Semiconductor

LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

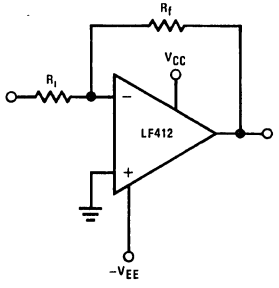
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	≤0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF412XYZ

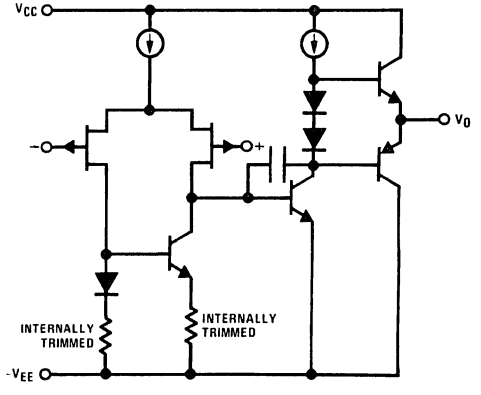
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

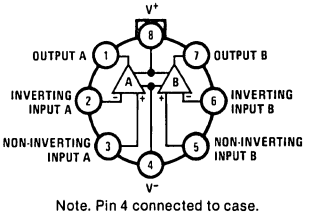
Simplified Schematic

1/2 Dual



Connection Diagrams

Metal Can Package

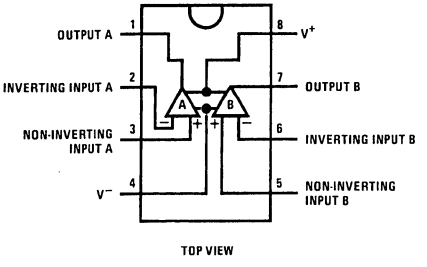


Note. Pin 4 connected to case.

TOP VIEW

Order Number LF412AMH, LF412MH, LF412ACH or LF412CH
See NS Package Number H08B

Dual-In-Line Package



TOP VIEW

TL/H/5656–1

Order Number LF412ACJ, LF412CJ, LF412ACN or LF412CN
See NS Package Number J08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 9)

	LF412A	LF412
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 10)	(Note 3)	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	152°C/W	115°C/W
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A			LF412			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 6)			7	10		7	20 (Note 6)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current	$V_O = 0V$, $R_L = \infty$			3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

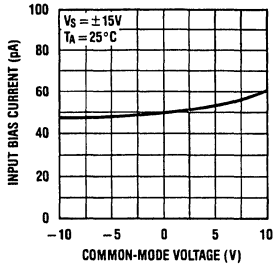
Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

Note 9: Refer to RETS412AX for LF412AMH military specifications and to RETS412X for LF412MH military specifications.

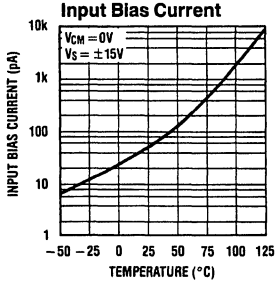
Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

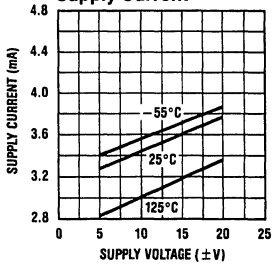
Input Bias Current



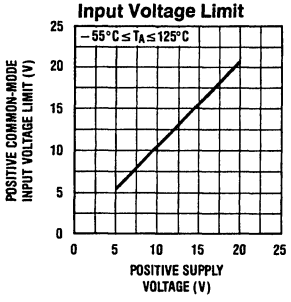
Input Bias Current



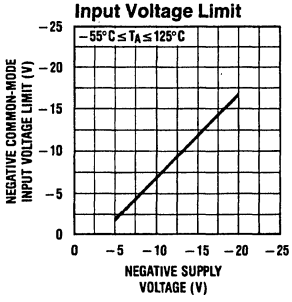
Supply Current



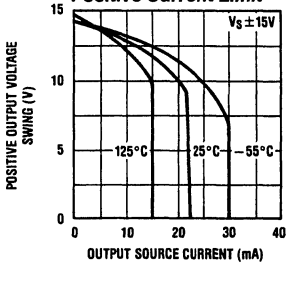
Positive Common-Mode Input Voltage Limit



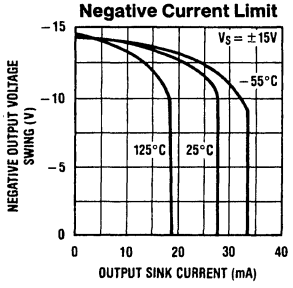
Negative Common-Mode Input Voltage Limit



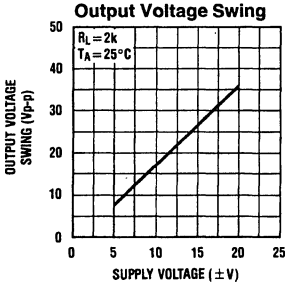
Positive Current Limit



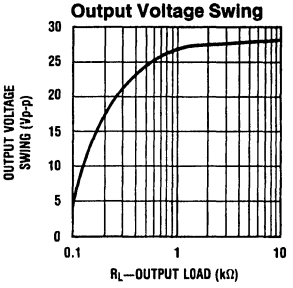
Negative Current Limit



Output Voltage Swing



Output Voltage Swing



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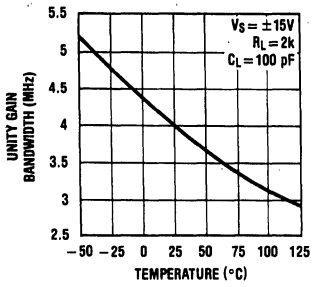
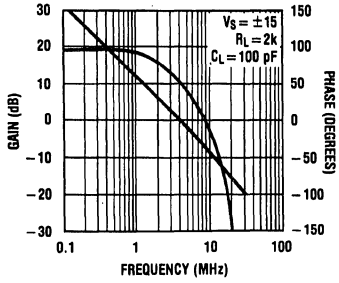
Typical Performance Characteristics (Continued)

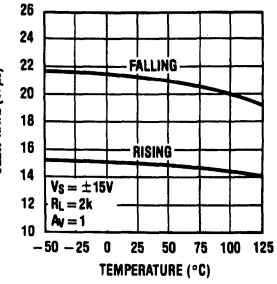
Gain Bandwidth



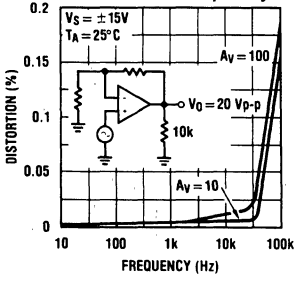
Bode Plot



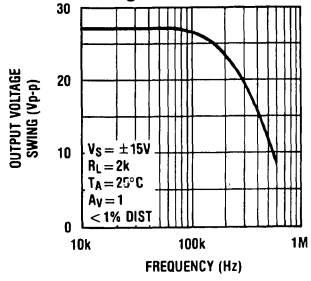
Slew Rate



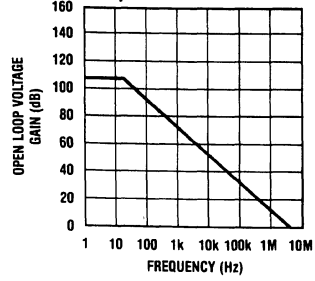
Distortion vs Frequency



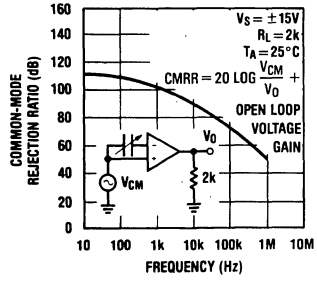
Undistorted Output Voltage Swing



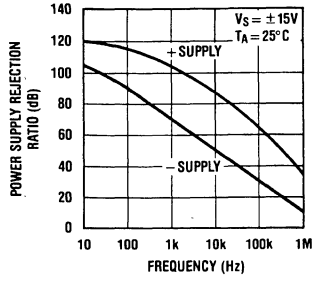
Open Loop Frequency Response



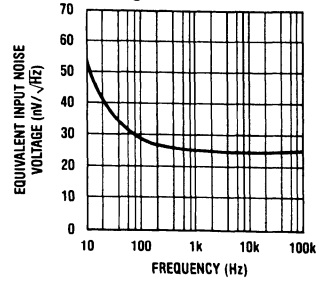
Common-Mode Rejection Ratio



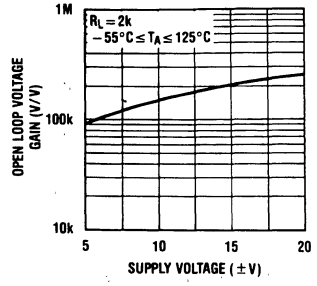
Power Supply Rejection Ratio



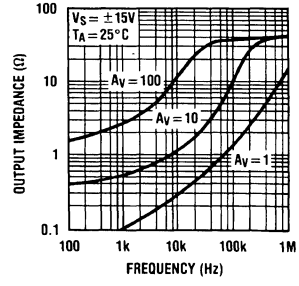
Equivalent Input Noise Voltage



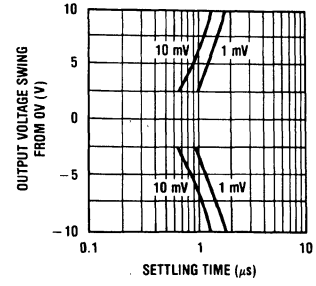
Open Loop Voltage Gain



Output Impedance



Inverter Settling Time



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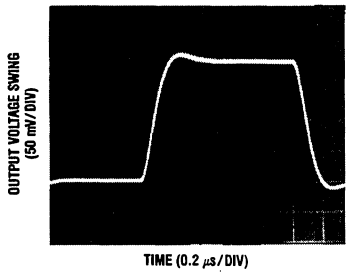
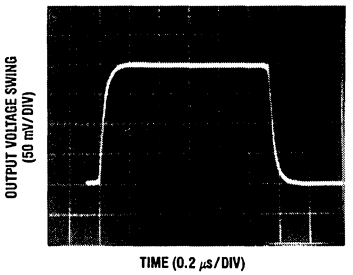
Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

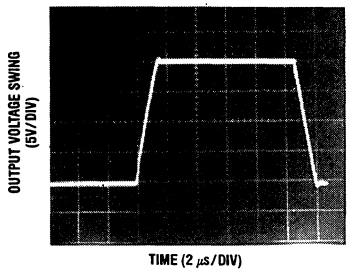
Small Signal Inverting



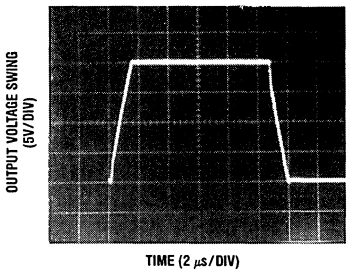
Small Signal Non-Inverting



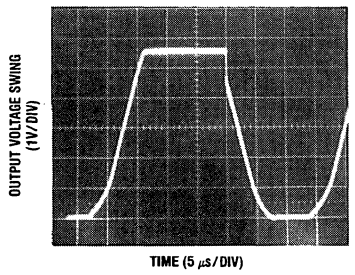
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5656–4

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

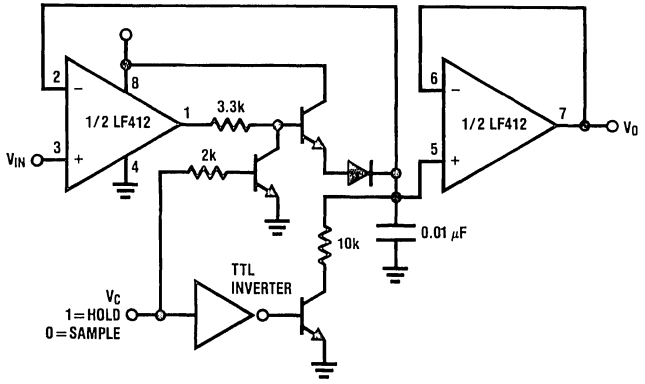
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

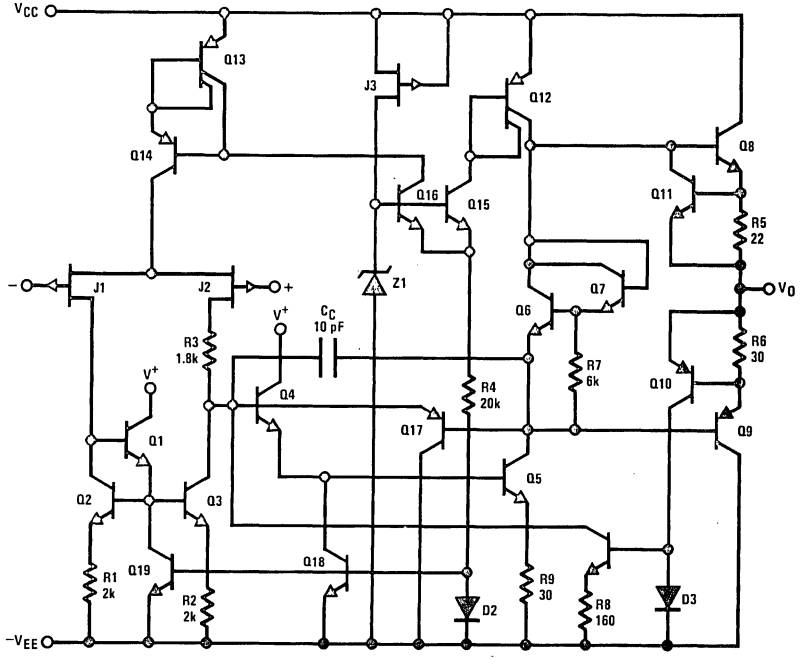
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold



Detailed Schematic



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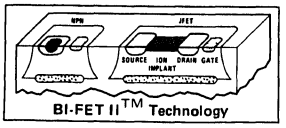
National Semiconductor



LF441A/LF441 Low Power JFET Input Operational Amplifier

General Description

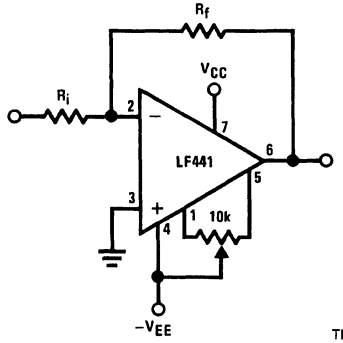
The LF441A/441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441A/441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441A/441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441A/441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441A/441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM741	200 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	0.5 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



TL/H/9297–1

Ordering Information

LF441XYZ

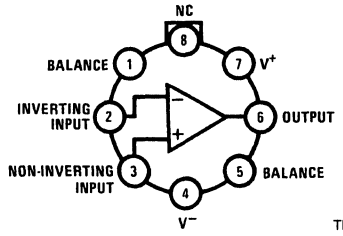
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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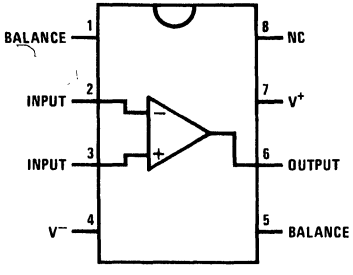
Top View

Note: Pin 4 connected to case.

Order Number LF441AMH or LF441CH
See NS Package Number H08B

Dual-In-Line Package



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Top View

Order Number LF441ACN, LF441CJ, LF441CM or LF441CN
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF441A	LF441
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	J Package	N Package	M Package
Power Dissipation (Notes 2 and 9)	670 mW		670 mW	
$T_{j\,max}$	150°C		115°C	
θ_{jA}(Typical)			130°C/W	185°C/W
Board Mount in still air	165°C/W			
Board Mount in 400 LF/min air flow	65°C/W			
θ_{jC}	25°C/W			
Operating Temp. Range	(Note 3)		(Note 3)	
Storage Temp. Range	$-65°C \le T_A \le 150°C$		$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	260°C	
θ_{jC}	25°C			

	LF441A	LF441
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF441A			LF441			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$			0.3	0.5		1	5	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$ (Note 5)			7	10		10		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\,k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18, −17		±11	+14, −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$		80	100		70	95		dB

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		70	90		dB
I_S	Supply Current			150	200		150	250	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: The LF441A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF441A/441 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF441A and for $V_S = \pm 15V$ for the LF441. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF441A is 100% tested to this specification.

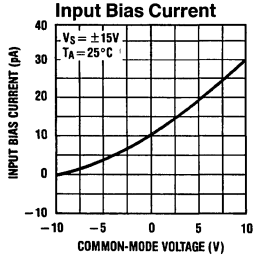
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

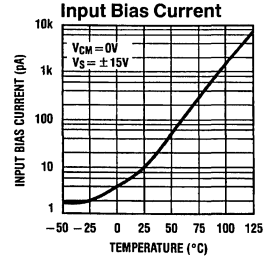
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

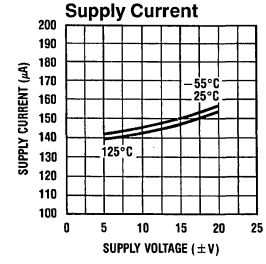
Note 8: Refer to RETS441AX for LF441AMH military specifications.

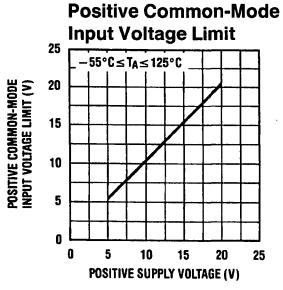
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

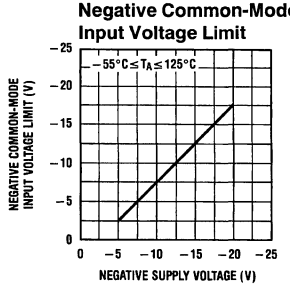
Typical Performance Characteristics

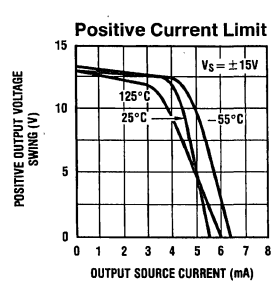








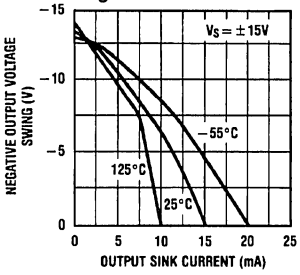




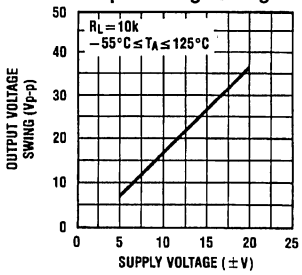
TL/H/9297–5

Typical Performance Characteristics (Continued)

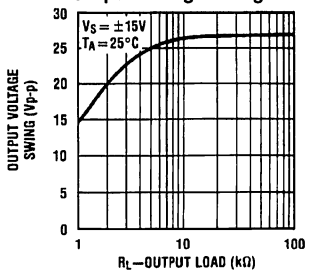
Negative Current Limit



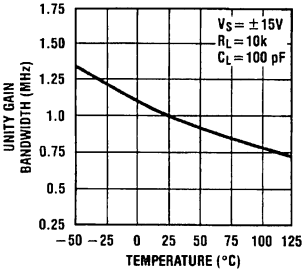
Output Voltage Swing



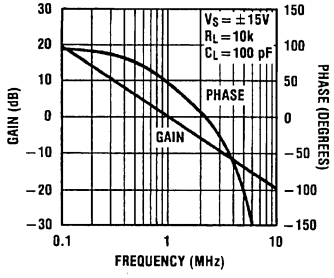
Output Voltage Swing



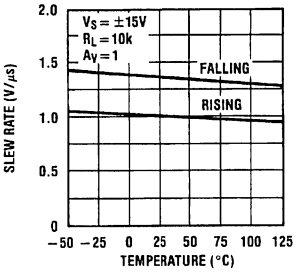
Gain Bandwidth



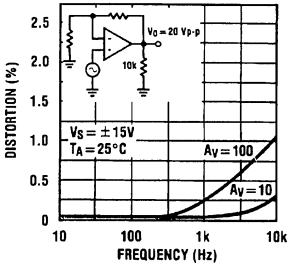
Bode Plot



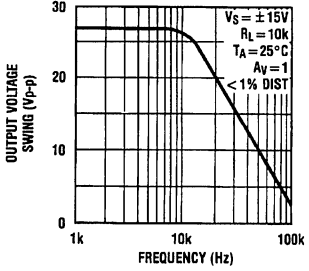
Slew Rate



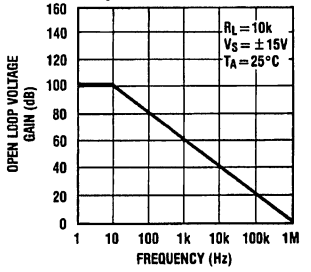
Distortion vs Frequency



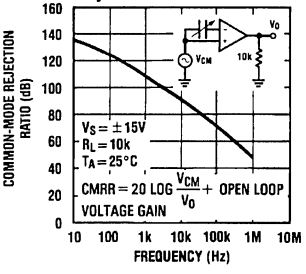
Undistorted Output Voltage Swing



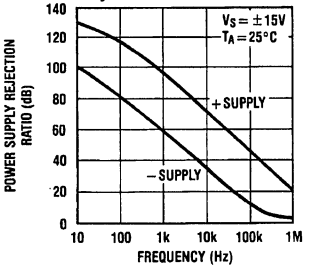
Open Loop Frequency Response



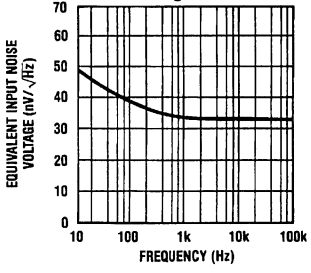
Common-Mode Rejection Ratio



Power Supply Rejection Ratio

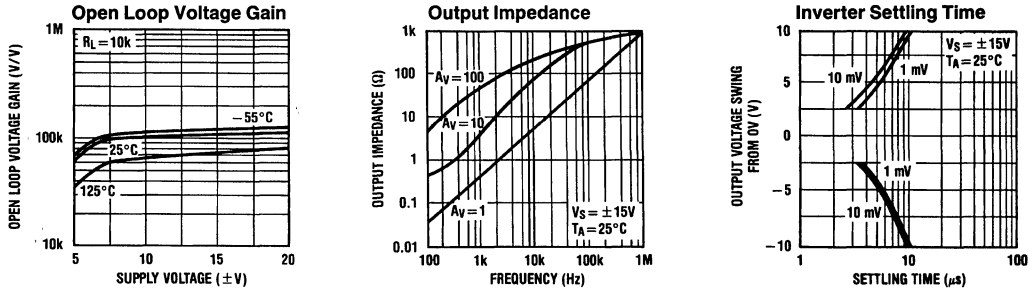


Equivalent Input Noise Voltage



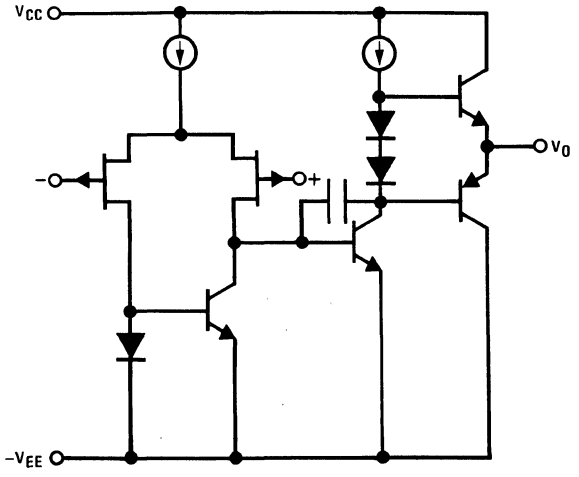
TL/H/9297–6

Typical Performance Characteristics (Continued)



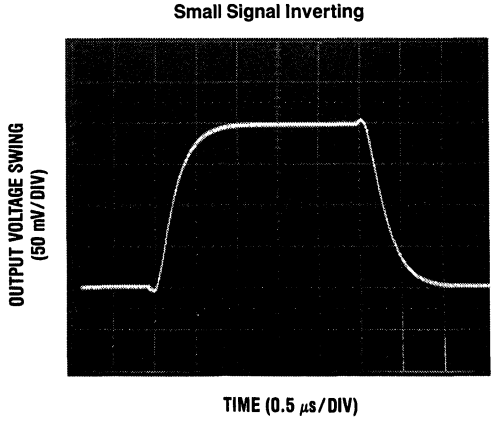
TL/H/9297–7

Simplified Schematic



TL/H/9297–3

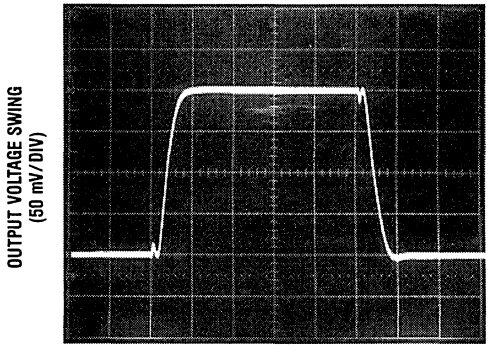
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$



TL/H/9297–8

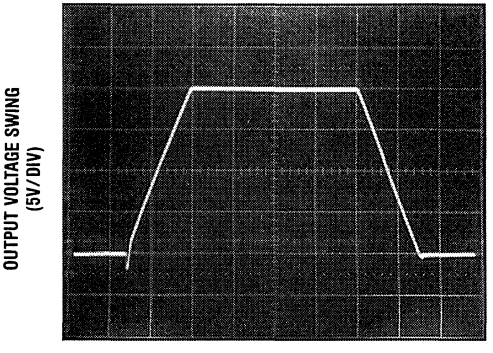
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$ (Continued)

Small Signal Non-Inverting



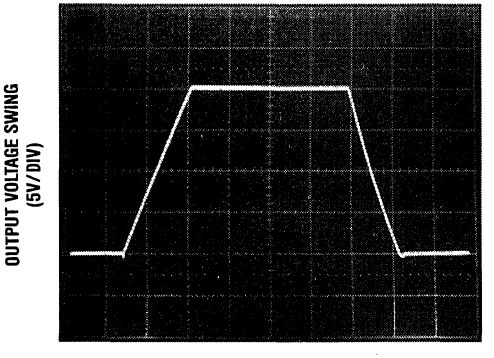
TL/H/9297–9

Large Signal Inverting



TL/H/9297–10

Large Signal Non-Inverting



TL/H/9297–11

Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of ±3V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifier will drive a 10 kΩ load resistance to ±10V over the full temperature range.

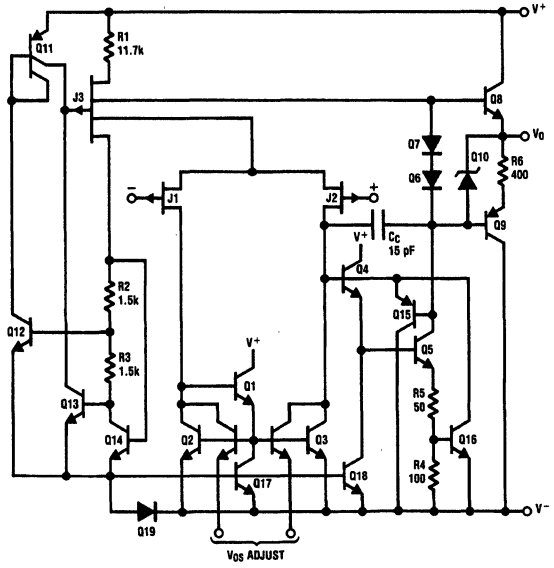
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because this amplifier is a JFET rather than MOSFET input op amp it does not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

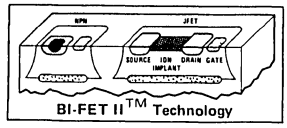
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



TL/H/9297–13

National Semiconductor



LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

General Description

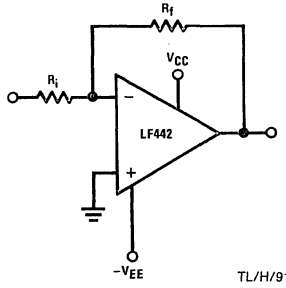
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



TL/H/9155-1

Ordering Information

LF442XYZ

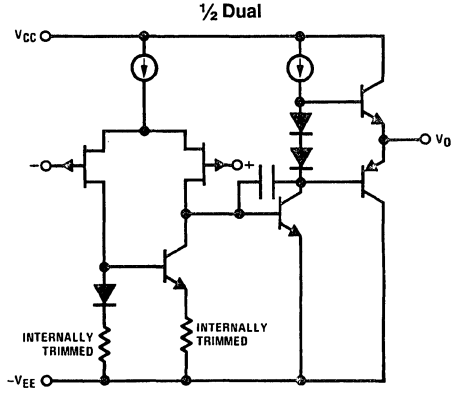
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Simplified Schematic

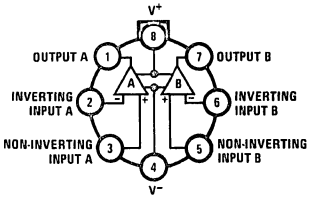
½ Dual



TL/H/9155-3

Connection Diagrams

Metal Can Package



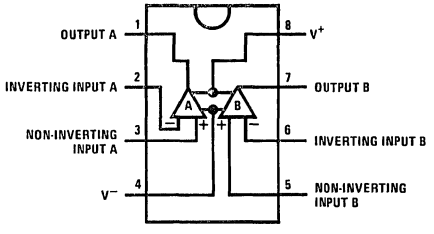
TL/H/9155-2

Top View

Note: Pin 4 connected to case

Order Number LF442AMH, LF442ACH or LF442CH
See NS Package Number H08B

Dual-In-Line Package



TL/H/9155-4

Top View

Order Number LF442CJ, LF442ACN or LF442CN
See NS Package Number J08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LF442A	LF442
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
T_j max	150°C	115°C
θ_{JA} (Typical) (Note 3)	65°C/W	114°C/W
θ_{JA} (Typical) (Note 4)	165°C/W	152°C/W
θ_{JC} (Typical)	21°C/W	
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions		LF442A			LF442			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			7	10		7		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	LF442A			LF442			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The value given is in 400 linear feet/min air flow.

Note 4: The value given is in static air.

Note 5: These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 6: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

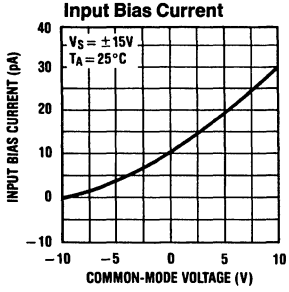
Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

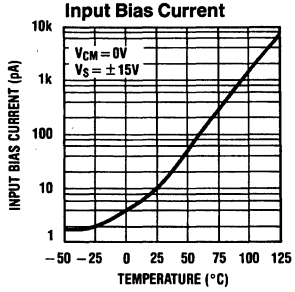
Note 9: Refer to RETS442AX for LF442AMH military specifications and to RETS442X for LF442MH military specifications.

Typical Performance Characteristics

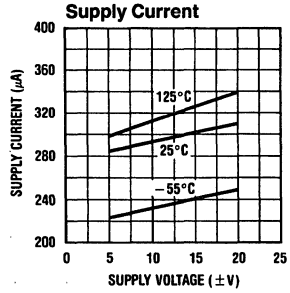
Input Bias Current



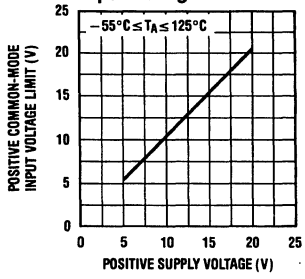
Input Bias Current



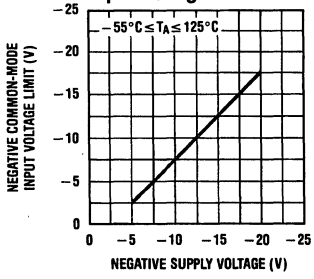
Supply Current



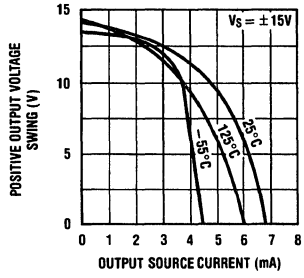
Positive Common-Mode Input Voltage Limit



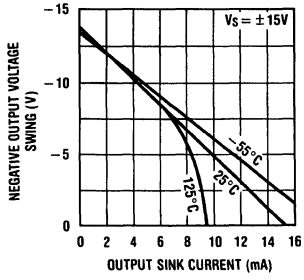
Negative Common-Mode Input Voltage Limit



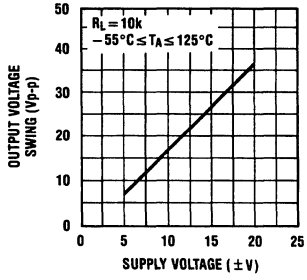
Positive Current Limit



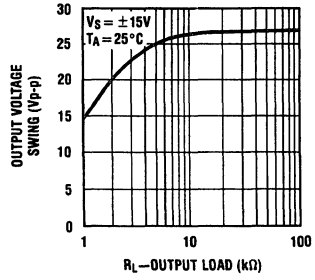
Negative Current Limit



Output Voltage Swing



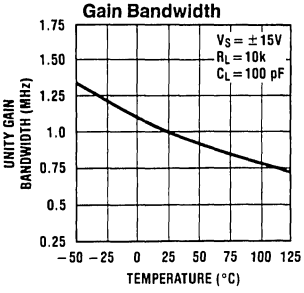
Output Voltage Swing



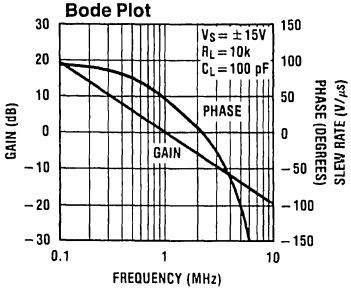
TL/H/9155–5

Typical Performance Characteristics (Continued)

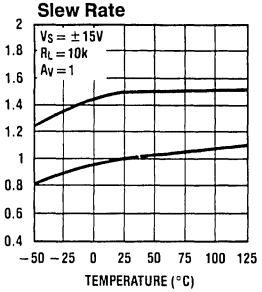
Gain Bandwidth



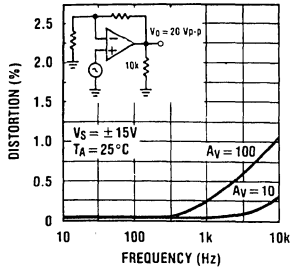
Bode Plot



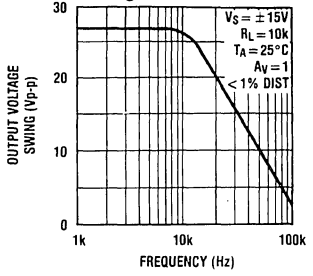
Slew Rate



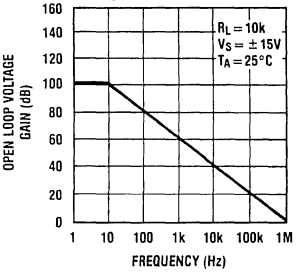
Distortion vs Frequency



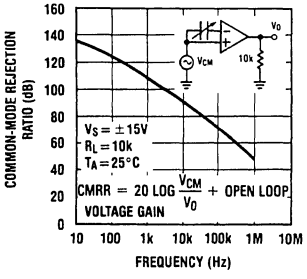
Undistorted Output Voltage Swing



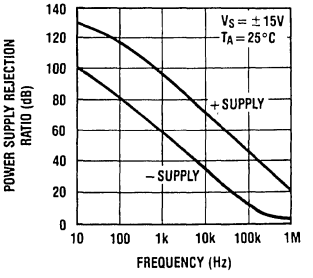
Open Loop Frequency Response



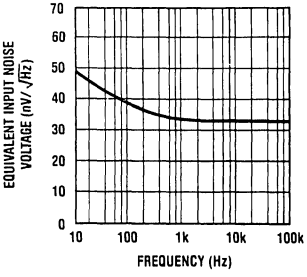
Common-Mode Rejection Ratio



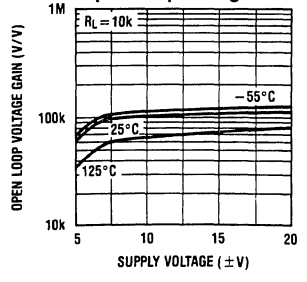
Power Supply Rejection Ratio



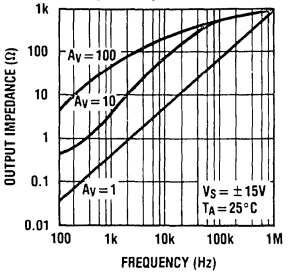
Equivalent Input Noise Voltage



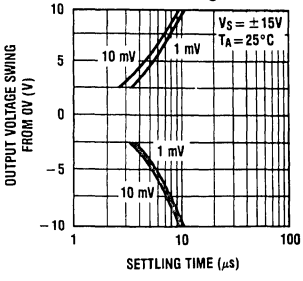
Open Loop Voltage Gain



Output Impedance



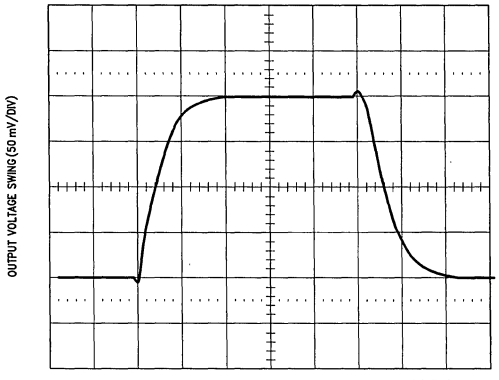
Inverter Settling Time



TL/H/9155–6

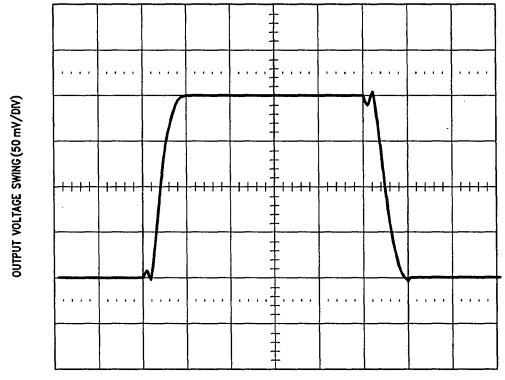
Pulse Response $R_L = 10\ k\Omega, C_L = 10\ pF$

Small Signal Inverting



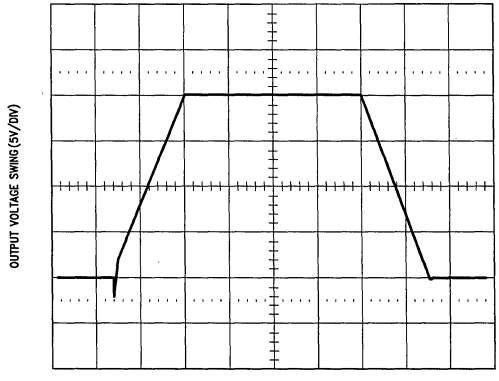
TL/H/9155–7

Small Signal Non-Inverting



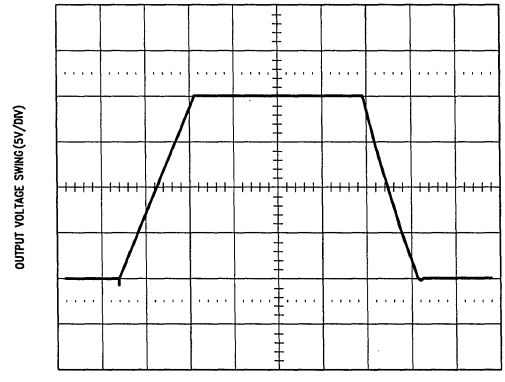
TL/H/9155–8

Large Signal Inverting



TL/H/9155–9

Large Signal Non-Inverting



TL/H/9155–10

Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

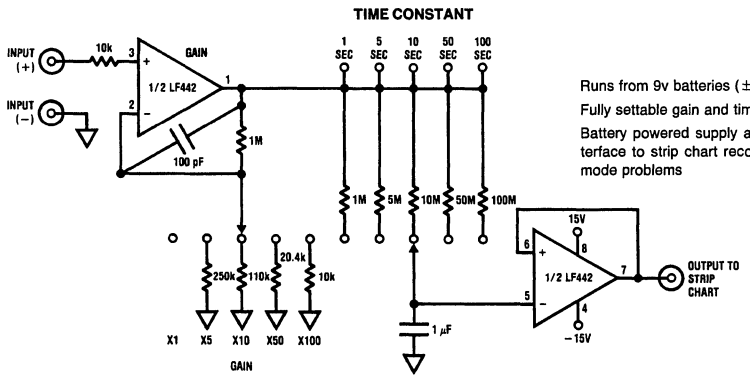
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Battery Powered Strip Chart Preamplifier



Runs from 9v batteries (±9V supplies)

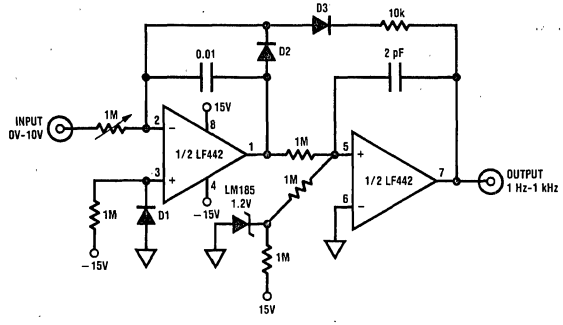
Fully settable gain and time constant

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

TL/H/9155–11

Typical Applications (Continued)

"No FET" Low Power V → F Converter

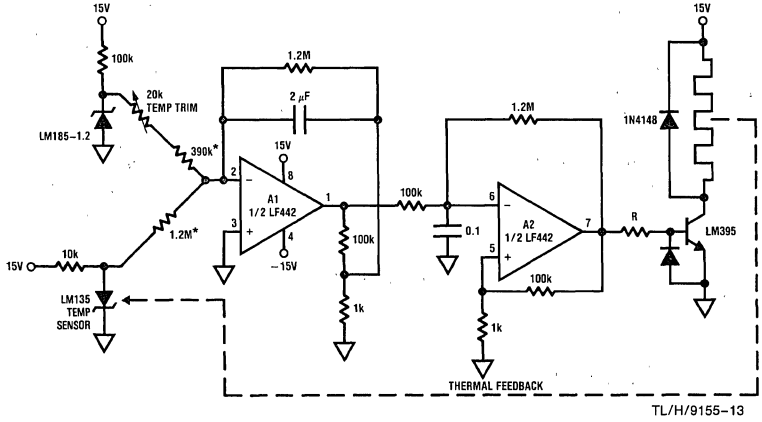


Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

TL/H/9155–12

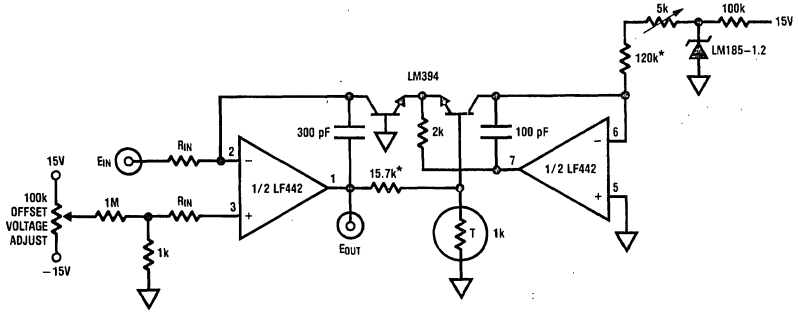
High Efficiency Crystal Oven Controller

- $T_{control}$ = 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor



TL/H/9155–13

Conventional Log Amplifier



TL/H/9155–14

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81

Trim 5k for 10 μA through the 5k–120k combination

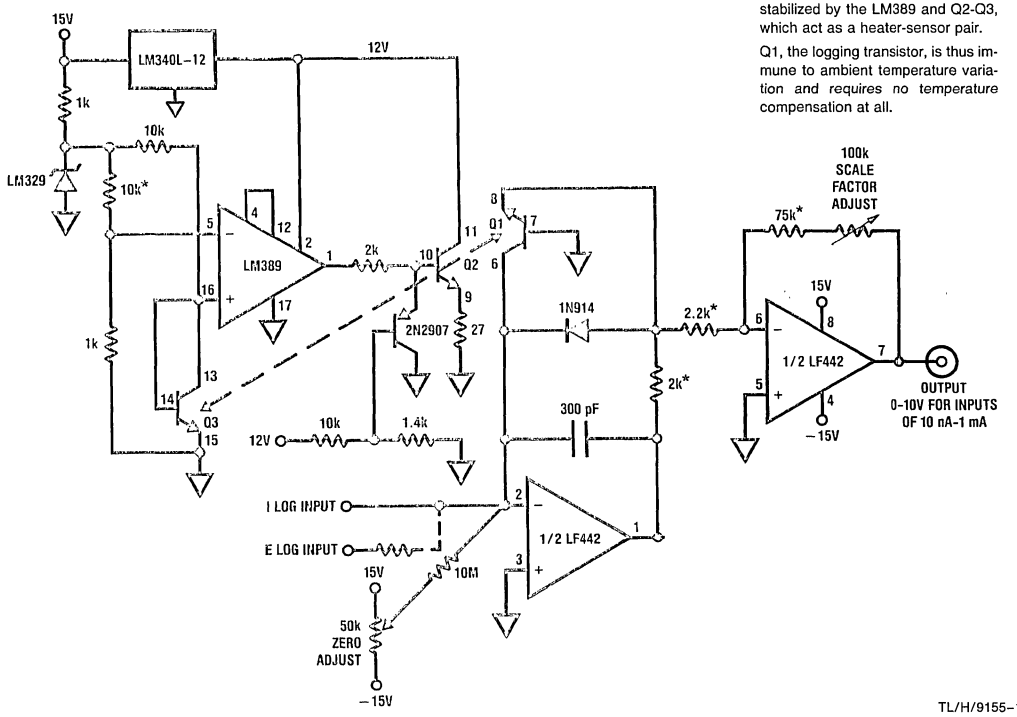
*1% film resistor

Typical Applications (Continued)

Unconventional Log Amplifier

Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.

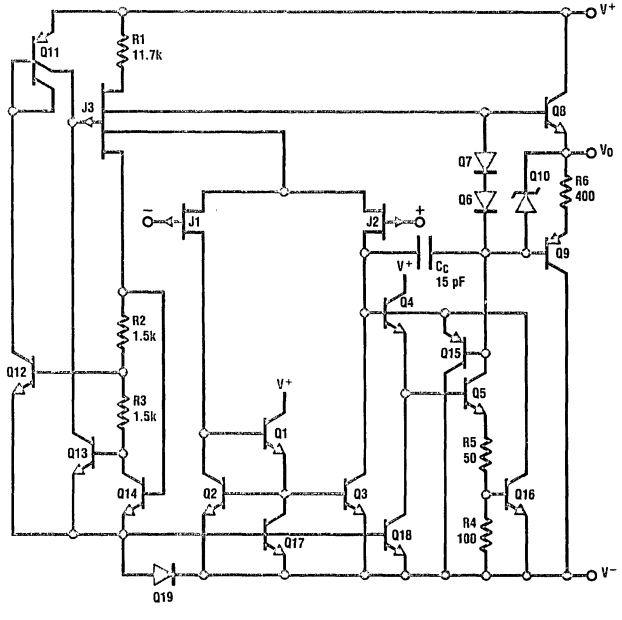
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.



TL/H/9155–15

Detailed Schematic

½ Dual



TL/H/9155–16

National Semiconductor

LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

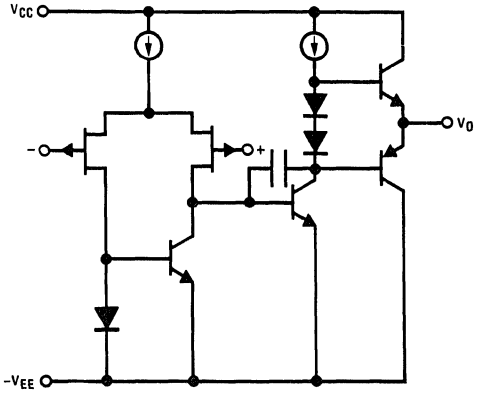
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ ¼ supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Simplified Schematic

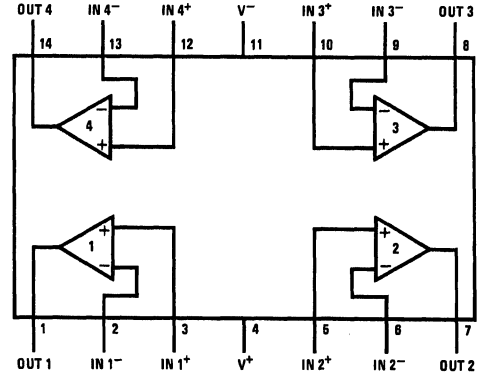
¼ Quad



TL/H/9156-1

Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



TL/H/9156-2

Top View

Order Number LF444AMD, LF444CD, LF444CJ, LF444CM, LF444CWM, LF444ACN or LF444CN
See NS Package Number D14E, J14A, M14A, M14B or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	D Package	N, WM Packages
Power Dissipation (Notes 3 and 9)	900 mW	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	100°C/W	85°C/W

	LF444A/LF444 (Note 4)
Operating Temperature Range	
Storage Temperature Range	$-65°C \le T_A \le 150°C$

ESD rating to be determined.

Soldering Information

Dual-In-Line Packages (Soldering, 10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10k, T_A = 25°C$			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		$\mu V/°C$
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 10\ k\Omega, T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.8	1.0	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/√Hz
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

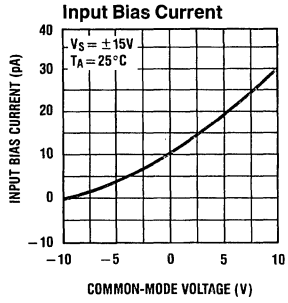
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

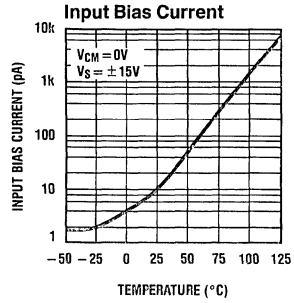
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

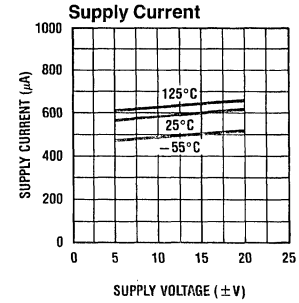
Note 8: Refer to RETS444AX for LF444AMD military specifications.

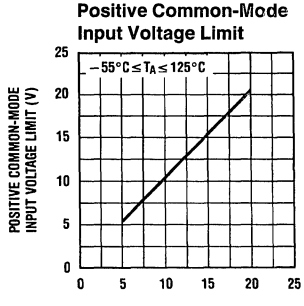
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

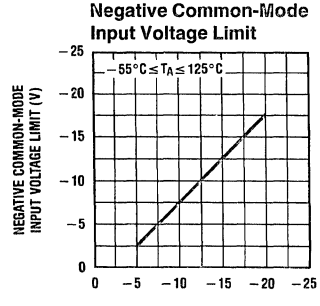
Typical Performance Characteristics

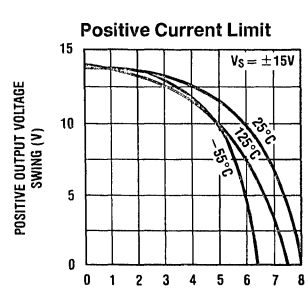








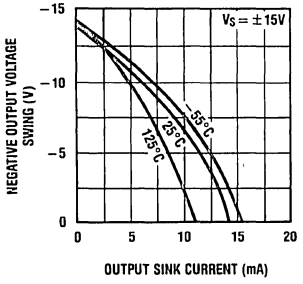




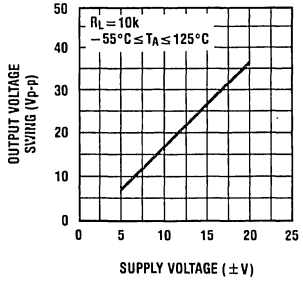
TL/H/9156–3

Typical Performance Characteristics (Continued)

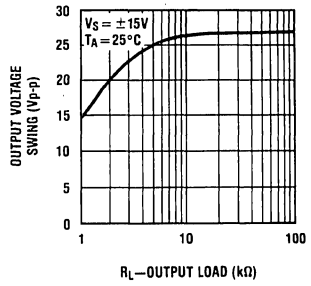
Negative Current Limit



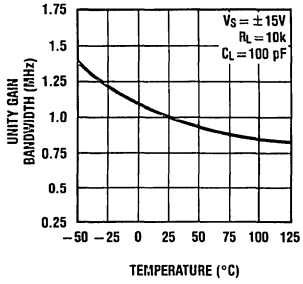
Output Voltage Swing



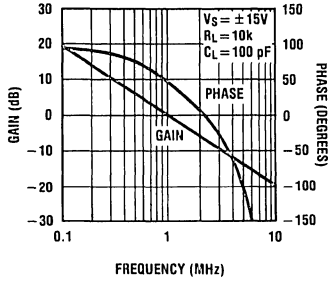
Output Voltage Swing



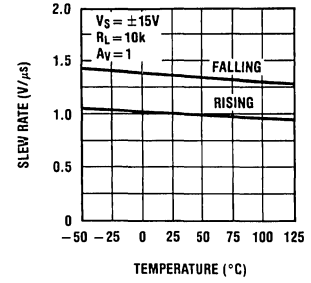
Gain Bandwidth



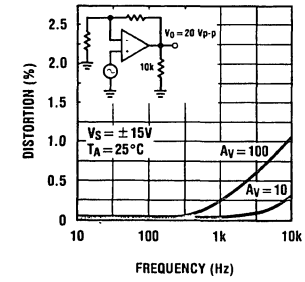
Bode Plot



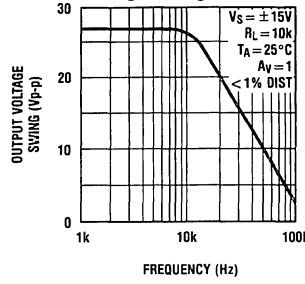
Slew Rate



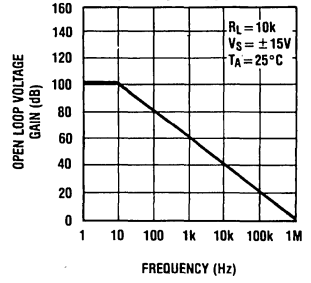
Distortion vs Frequency



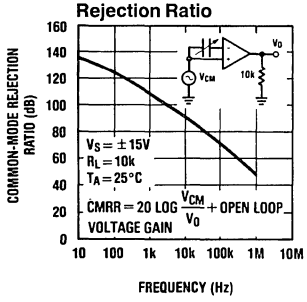
Undistorted Output Voltage Swing



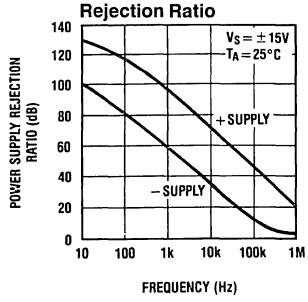
Open Loop Frequency Response



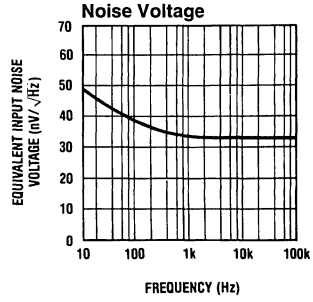
Common-Mode Rejection Ratio



Power Supply Rejection Ratio



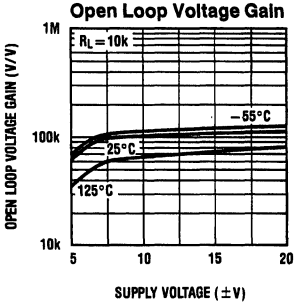
Equivalent Input Noise Voltage



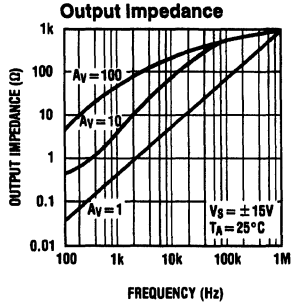
TL/H/9156–4

Typical Performance Characteristics (Continued)

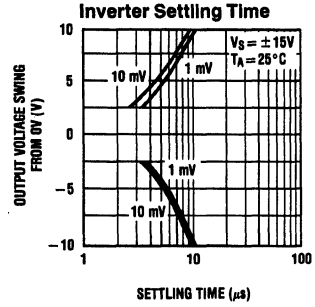
Open Loop Voltage Gain



Output Impedance



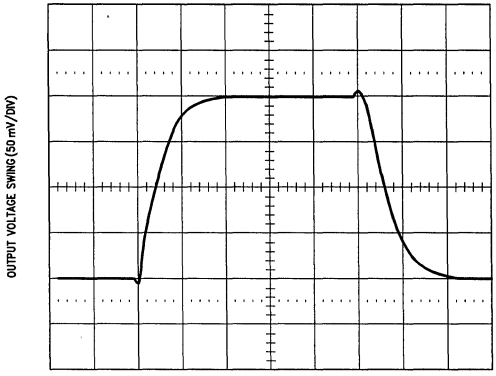
Inverter Settling Time



TL/H/9156-5

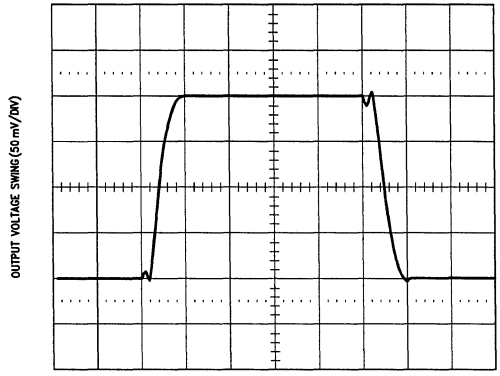
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



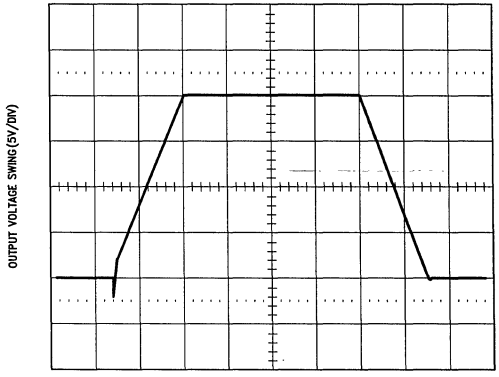
TL/H/9156-6

Small Signal Non-Inverting



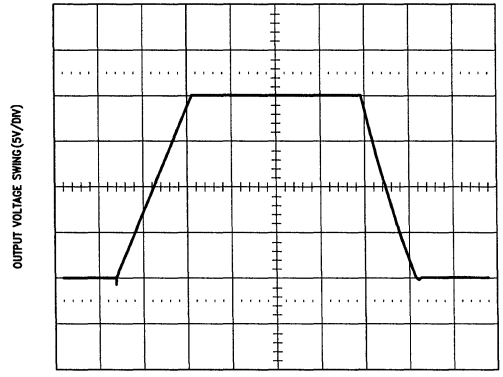
TL/H/9156-7

Large Signal Inverting



TL/H/9156-8

Large Signal Non-Inverting



TL/H/9156-9

Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

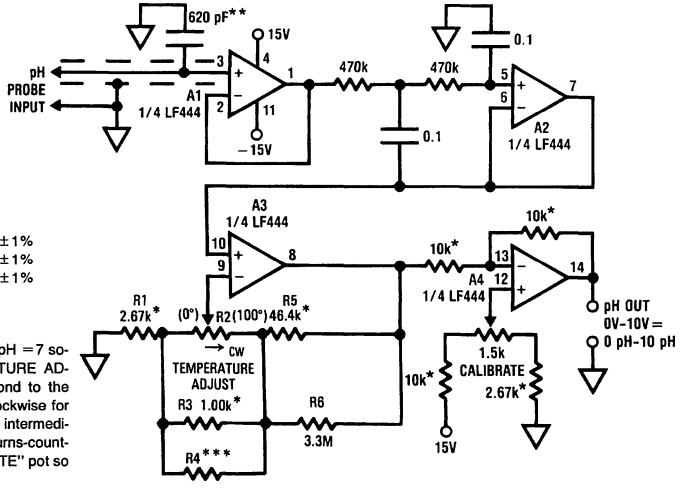
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%

**Polystyrene

*Film resistor type RN60C

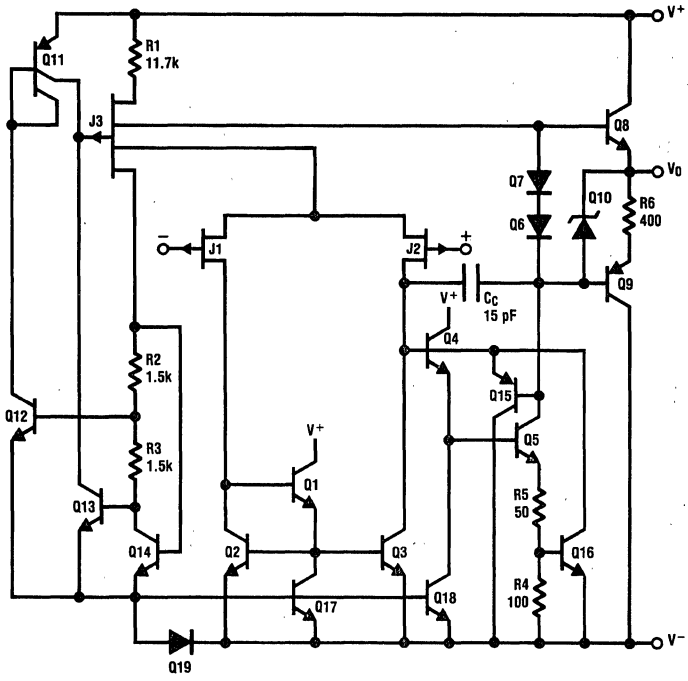
To calibrate, insert probe in pH = 7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set "CALIBRATE" pot so output reads 7V.

Typical probe = Ingold Electrodes #465-35

TL/H/9156–10

Detailed Schematic

¼ Quad



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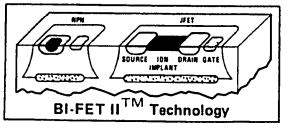
National Semiconductor



LF451 Wide-Bandwidth JFET-Input Operational Amplifier

General Description

The LF451 is a low-cost high-speed JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF451 is pin compatible with the standard LM741, allowing designers to upgrade the overall performance of existing designs.

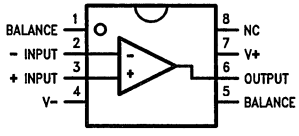
The LF451 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 5.0 mV (max)
- Low input bias current 50 pA (typ)
- Low input noise current 0.01 pA/$\sqrt{Hz}$ (typ)
- Wide gain bandwidth 4 MHz (typ)
- High slew rate 13 V/μs (typ)
- Low supply current 3.4 mA (max)
- High input impedance $10^{12}\Omega$ (typ)
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 V_{p-p}, f = 20 Hz–20 kHz <0.02% (typ)
- Low 1/f noise corner 50 Hz (typ)
- Fast settling time to 0.01% 2 μs (typ)

Connection Diagram

S.O. Package

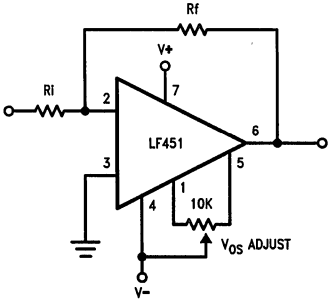


TL/H/9660–2

Top View

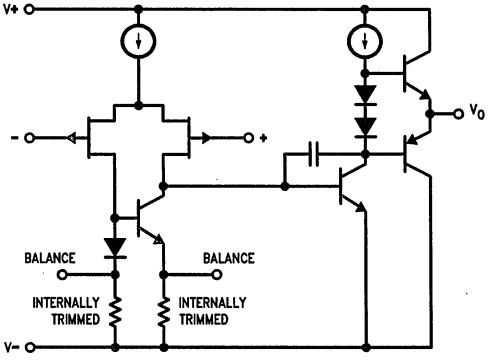
Order Number LF451CM
See NS Package Number M08A

Typical Connection



TL/H/9660–1

Simplified Schematic



TL/H/9660–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Susceptibility (Note 4)	2000V
Soldering Information (Note 5)	
SO Package: Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF451CM	$0°C \le T_A \le +70°C$
Junction Temperature ($T_{J\,max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\,k\Omega$, (Note 10)	0.3	5		mV
I_{OS}	Maximum Input Offset Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\,k\Omega$ (Note 10)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 11)	100	80	**80**	dB
I_S	Maximum Supply Current			3.4	**3.4**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ MAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\,max} = 125°C$. The typical thermal resistance (θ_{JA}) of the LF451CM when board-mounted is 170°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

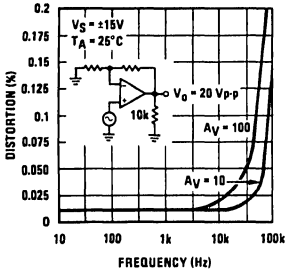
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 10: V_{OS}, I_B, AVOL, and I_{OS} are measured at $V_{CM} = 0V$.

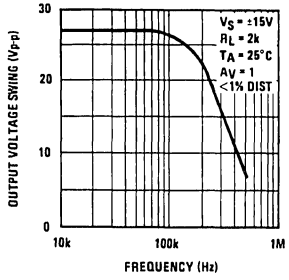
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

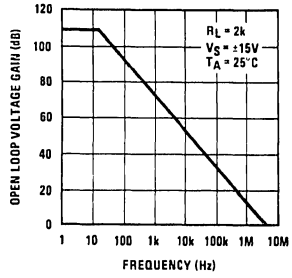
Distortion vs Frequency



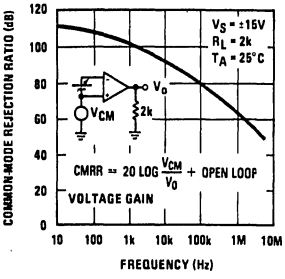
Undistorted Output Voltage Swing



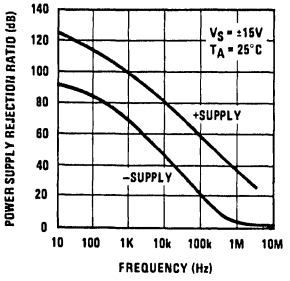
Open Loop Frequency Response



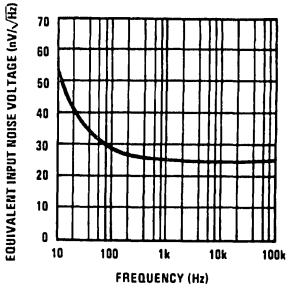
Common-Mode Rejection Ratio



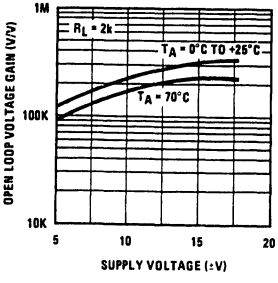
Power Supply Rejection Ratio



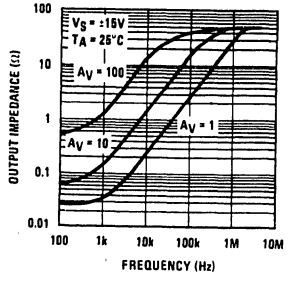
Equivalent Input Noise Voltage



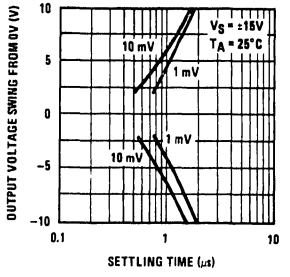
Open Loop Voltage Gain (V/V)



Output Impedance



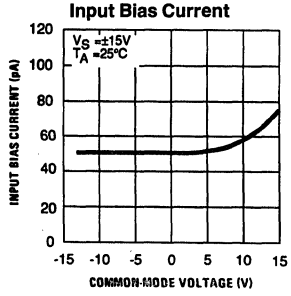
Inverter Settling Time



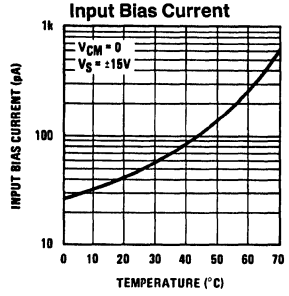
TL/H/9660–5

Typical Performance Characteristics (Continued)

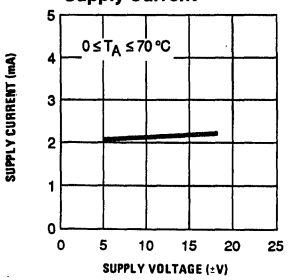
Input Bias Current



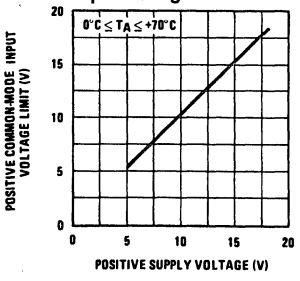
Input Bias Current



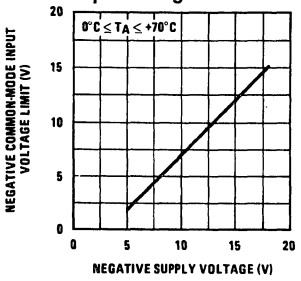
Supply Current



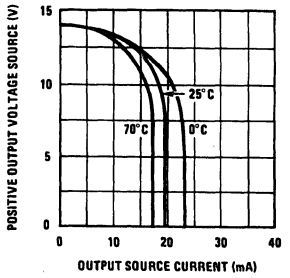
Positive Common-Mode Input Voltage Limit



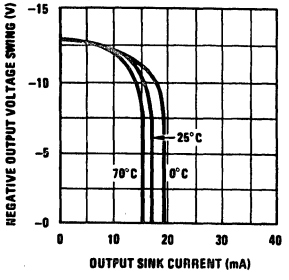
Negative Common-Mode Input Voltage Limit



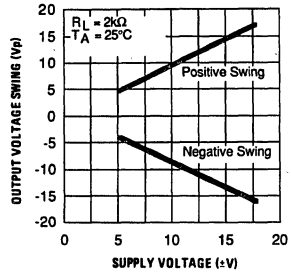
Positive Current Limit



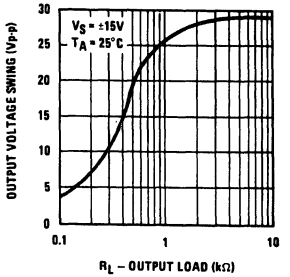
Negative Current Limit



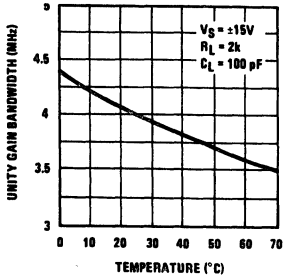
Voltage Swing



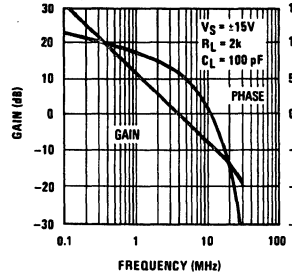
Output Voltage Swing



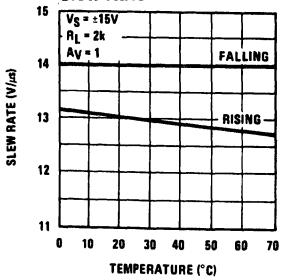
Gain Bandwidth



Bode Plot



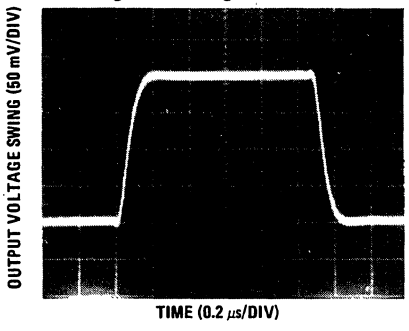
Slew Rate



TL/H/9660–4

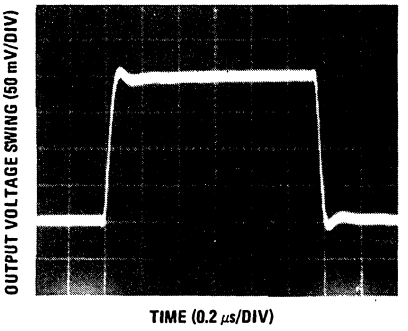
Pulse Response

Small Signal Inverting



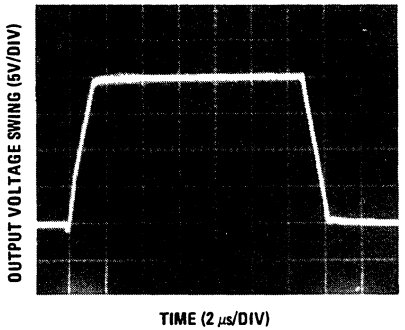
TL/H/9660–6

Small Signal Non-Inverting



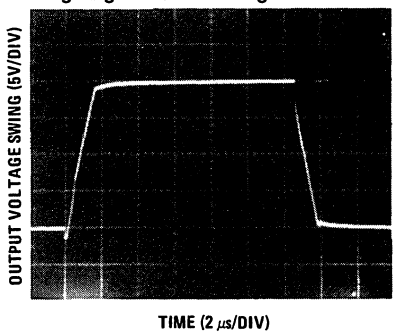
TL/H/9660–7

Large Signal Inverting



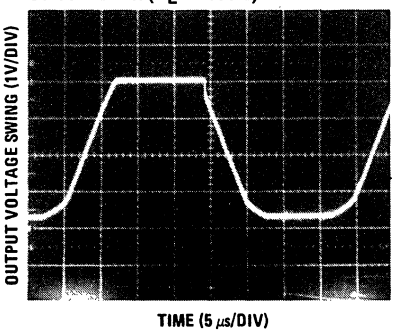
TL/H/9660–8

Large Signal Non-Inverting



TL/H/9660–9

Current Limit (R_L = 100Ω)



TL/H/9660–10

Application Hints

The LF451CM is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output.

In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF451 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF451 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

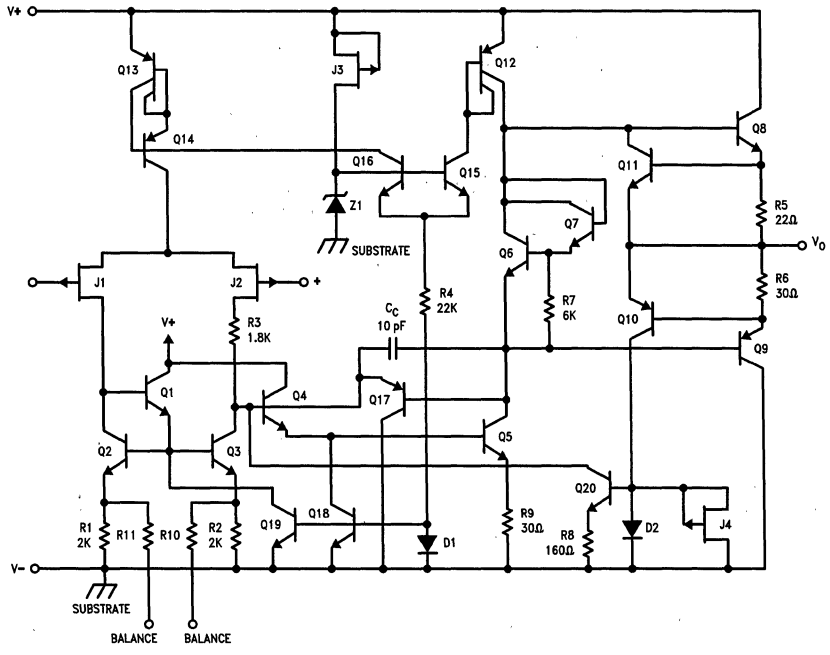
Because these amplifiers are JFET rather than MOSFET input op amps they are more resistant to ESD (see Absolute Maximum Ratings).

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the S.O. package results from its very small size. It follows, however, that the die inside the S.O. package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the S.O. Therefore, not following certain precautions when board mounting the LF451CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF451CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF451CM surface mounting refer to Application Note AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" and to Section 6 "Surface Mount" found in any Rev. 1 Linear Databook volume.

Detailed Schematic



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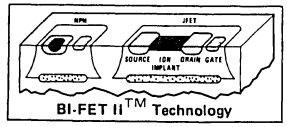
National Semiconductor



LF453 Wide-Bandwidth Dual JFET-Input Operational Amplifiers

General Description

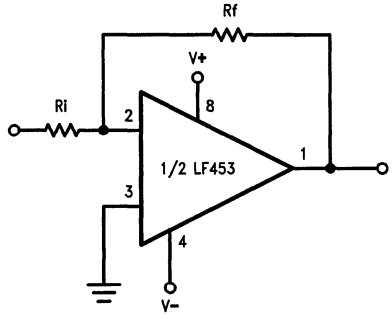
The LF453 is a low-cost, high-speed, dual JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II technology). The device requires a low supply current and yet the amplifiers maintain a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF453 is pin compatible with the standard LM1558, allowing designers to upgrade the overall performance of existing designs.

The LF453 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	5.0 mV (max)
■ Low input bias current	50 pA (typ)
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$ (typ)
■ Wide gain bandwidth	4 MHz (typ)
■ High slew rate	13 V/μs (typ)
■ Low supply current	6.5 mA (max)
■ High input impedance	$10^{12}\Omega$ (typ)
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 V_{p-p}, f = 20 Hz–20 kHz	<0.02% (typ)
■ Low 1/f noise corner	50 Hz (typ)
■ Fast settling time to 0.01%	2 μs (typ)

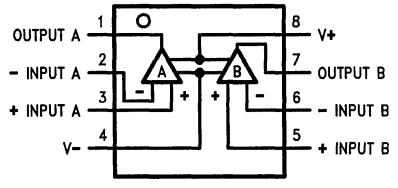
Typical Connection



TL/H/9710–1

Connection Diagram

SO Package

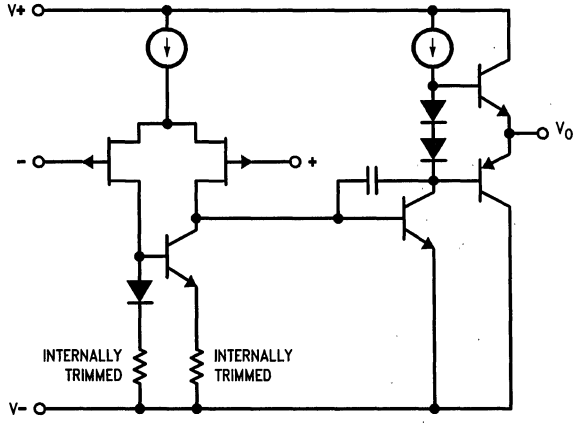


TL/H/9710–2

Top View

Order Number LF453CM
See NS Package Number M08A

Simplified Schematic



TL/H/9710–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V^+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Susceptability (Note 4)	2000V
Soldering Information (Note 5)	
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF453CM	$0°C \le T_A + 70°C$
Junction Temperature ($T_{J\,max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\,k\Omega$, (Note 10)		5		mV
I_{OS}	Maximum Input Offset Current	(Notes 9, 10) $T_J = 25°C$	25	100		pA
		$T_J = 70°C$			**2**	nA
I_B	Maximum Input Bias Current	(Notes 9, 10) $T_J = 25°C$	50	200		pA
		$T_J = 70°C$			**4**	nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\,k\Omega$ (Note 10)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5	+11	**+11**	V
			−11.5	−11	**−11**	V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 11)	100	80	**80**	dB
I_S	Maximum Supply Current			6.5	**6.5**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. Limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\,MAX - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\,max} = 125°C$. The typical thermal resistance (Θ_{JA}) of the LF453CM when board-mounted is 160°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (section titled "Surface Mount") for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

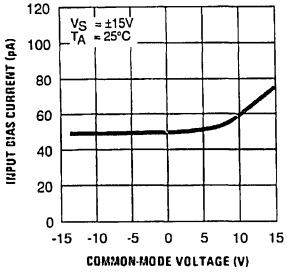
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient.

Note 10: V_{OS}, I_B, AVOL and I_{OS} are measured at $V_{CM} = 0V$.

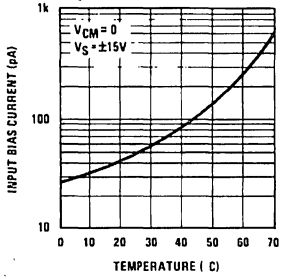
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

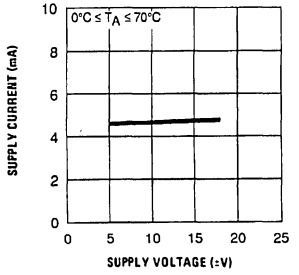
Input Bias Current



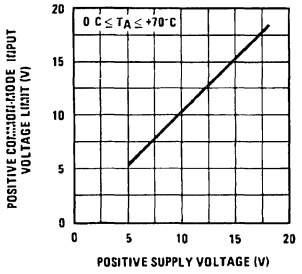
Input Bias Current



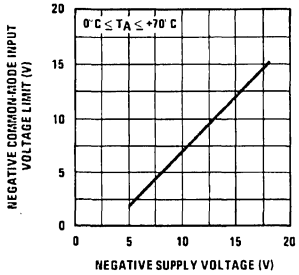
Supply Current



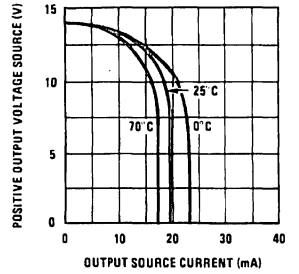
Positive Common-Mode Input Voltage Limit



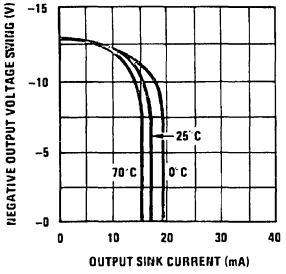
Negative Common-Mode Input Voltage Limit



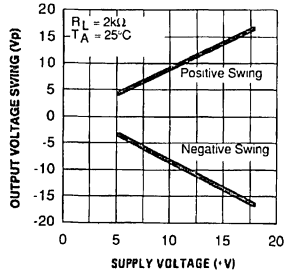
Positive Current Limit



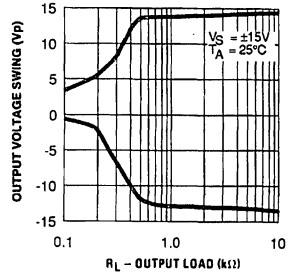
Negative Current Limit



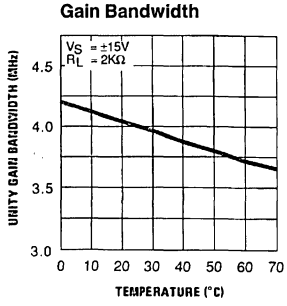
Voltage Swing



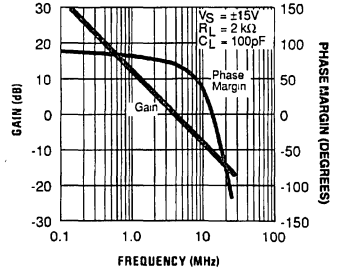
Output Voltage Swing



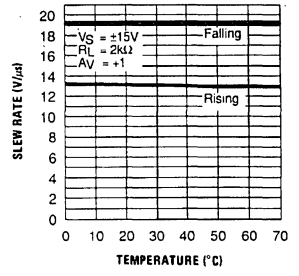
Gain Bandwidth



Bode Plot



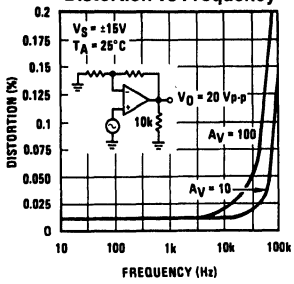
Slew Rate



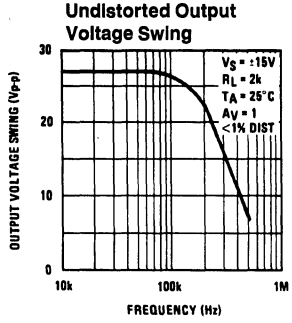
TL/H/9710–4

Typical Performance Characteristics (Continued)

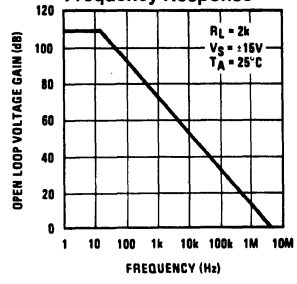
Distortion vs Frequency



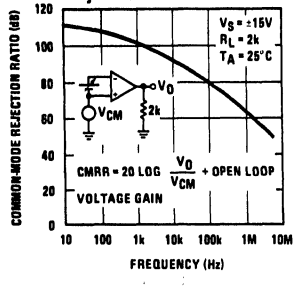
Undistorted Output Voltage Swing



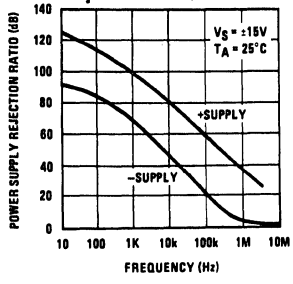
Open Loop Frequency Response



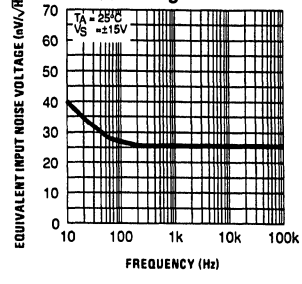
Common-Mode Rejection Ratio



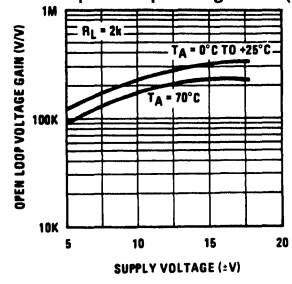
Power Supply Rejection Ratio



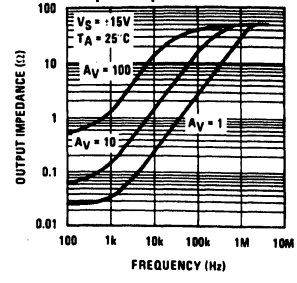
Equivalent Input Noise Voltage



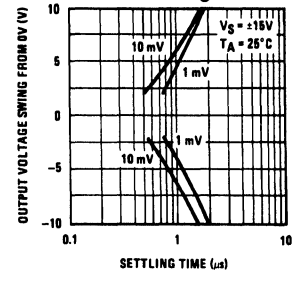
Open Loop Voltage Gain (V/V)



Output Impedance



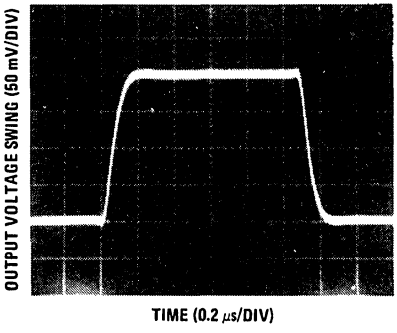
Inverter Settling Time



TL/H/9710–5

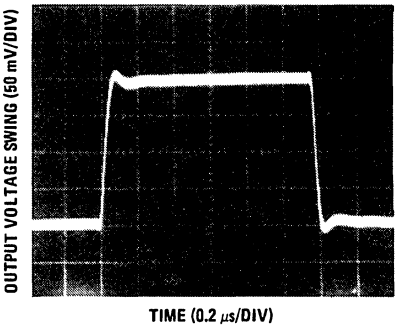
Pulse Response

Small Signal Inverting



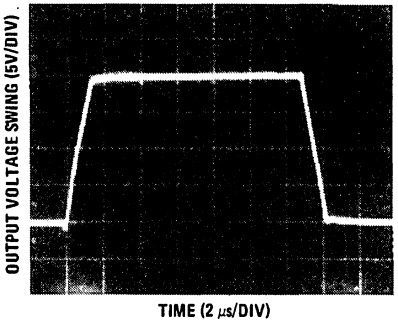
TL/H/9710–6

Small Signal Non-Inverting



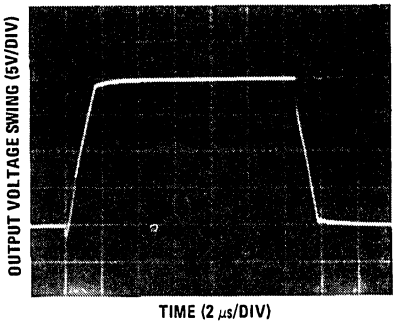
TL/H/9710–7

Large Signal Inverting



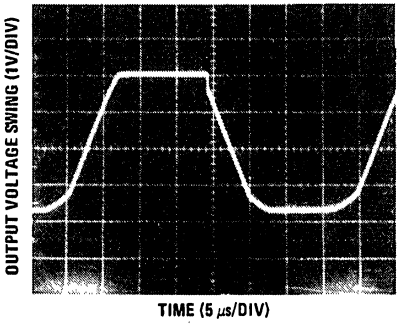
TL/H/9710–8

Large Signal Non-Inverting



TL/H/9710–9

Current Limit (R_L = 100 Ω)



TL/H/9710–10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ± 5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ± 10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

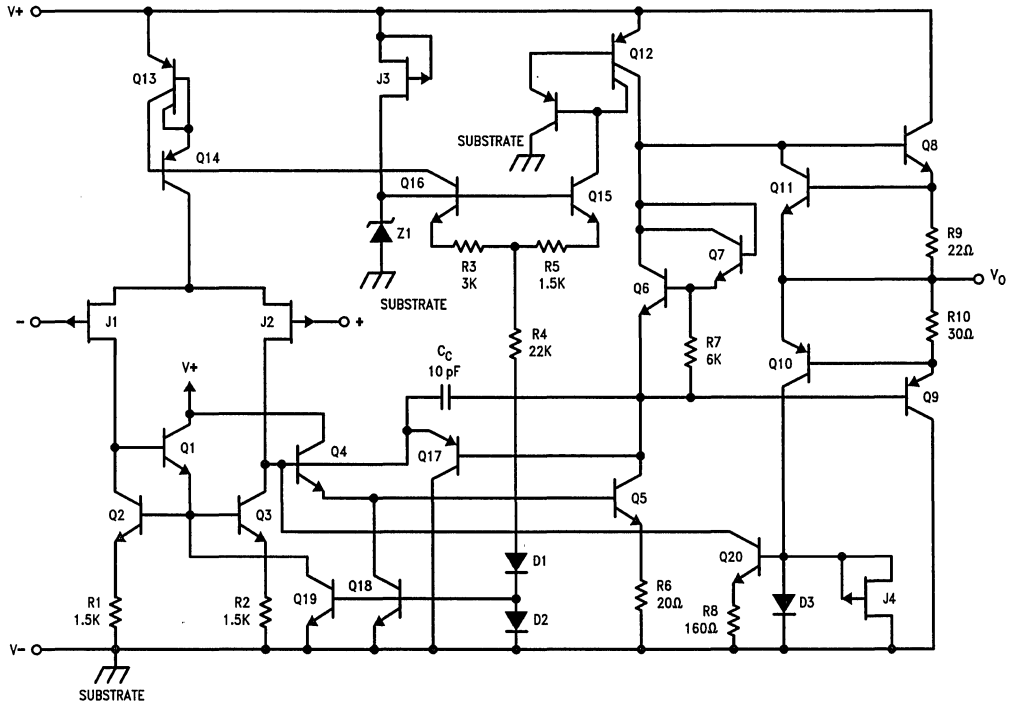
Because these amplifiers are JFET rather than MOSFET input op amps they are more resistant to ESD (see Absolute Maximum Ratings).

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive.The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

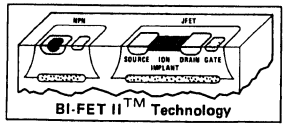
The benefit of the SO package results from its very small size. It follows, however, that the die inside the SO package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the SO. Therefore, not following certain precautions when board mounting the LF453CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF453CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF453CM surface mounting refer to Application Note AN450 "Surface Mounting Methods and Their Effect on Product Reliability" and to the section titled "Surface Mount" found in any Rev 1. Linear Databook volume.

Detailed Schematic



TL/H/9710–11

National Semiconductor



LF13741
Monolithic JFET Input Operational Amplifier

General Description

The LF13741 is a 741 with BI-FET™ input followers on the same die. Familiar operating characteristics—those of a 741—with the added advantage of low input bias current make the LF13741 easy to use. Monolithic fabrication makes this "drop-in-replacement" operational amplifier very economical.

Applications in which the LF13741 excels are those which require low bias current, moderate speed and low cost. A few examples include high impedance transducer amplifiers, photocell amplifiers, buffers for high impedance, slow to moderate speed sources and buffers in sample-and-hold type systems where leakage from the hold capacitor node must be kept to a minimum.

Systems designers can take full advantage of their knowledge of the 741 when designing with the LF13741 to achieve extremely rapid "design times." The LF13741 can also be used in existing sockets to make the "error budget" for input bias and/or offset currents negligible and in many cases eliminate trimming. For higher speed and lower noise use the LF155, LF156, LF157 series of BI-FET operational amplifiers.

Features

- Low input bias current 50 pA
- Input common-mode range to positive supply voltage
- Low input noise current 0.01 pA/$\sqrt{\text{Hz}}$
- High input impedance $5 \times 10^{11}\Omega$
- Familiar operating characteristics

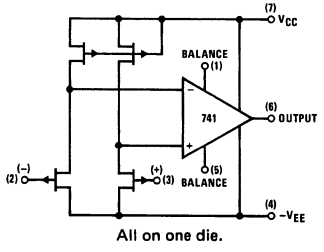
Advantages

- FET inputs—741 operating characteristics
- Low cost
- Ease of use
- Standard supplies
- Standard pin outs
- Non-rectifying input for RF environment
- Rapid "design time"

Applications

- Smoke detectors
- I to V converters
- High impedance buffers
- Low drift sample and hold circuits
- High input impedance, slow comparators
- Long time timers
- Low drift peak detectors
- Supply current monitors
- Low error budget systems

Simplified Schematic

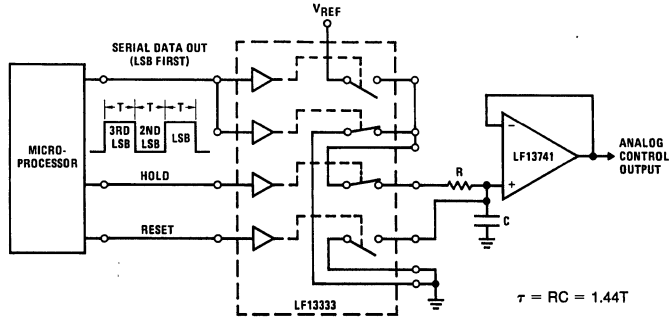


All on one die.

TL/H/9296–1

Typical Applications

Inexpensive Microprocessor D/A



TL/H/9296–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	100°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±16V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C

	H Package	N Package
θ_{jA} (Typical)		
(Note 1)	70°C/W	163°C/W
(Note 2)	175°C/W	218°C/W
θ_{jC} (Typical)	25°C/W	

Metal Package Lead Temperature (Soldering, 10 sec.) 300°C

Plastic Package (Soldering, 4 sec.) 260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	
	Voltage Offset Adjustment Range		10			mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C (Notes 4, 5)		10	50	pA
		$T_j \leq 70°C$			2	nA
I_B	Input Bias Current	T_j = 25°C (Notes 4, 5)		50	200	pA
		$T_j \leq 70°C$		1.6	8	nA
R_{IN}	Input Resistance	T_j = 25°C		5×10^{11}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ	25	100		V/mV
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15.1 −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	77	96		dB
I_S	Supply Current			2	4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	$V_S = \pm 15V, T_A = 25°C$		0.5		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V, T_A = 25°C$		1.0		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C, R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 50 37		 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$ f = 100 Hz f = 1000 Hz		 0.01 0.01		 $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$

Note 1: The value given is in 400 Linear Feet/Min air flow.

Note 2: The value given is in static air.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

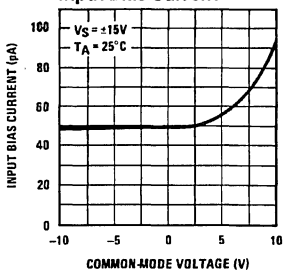
Note 4: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

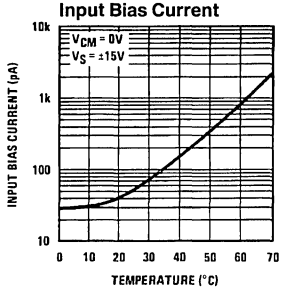
Note 6: Supply Voltage Rejection Ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 10V$ to $\pm 15V$.

Typical Performance Characteristics

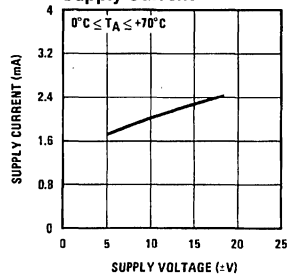
Input Bias Current



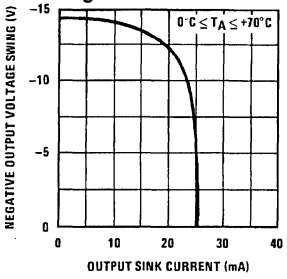
Input Bias Current



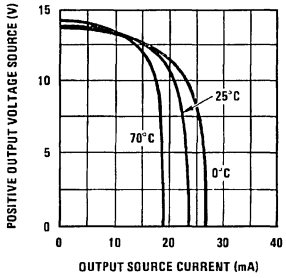
Supply Current



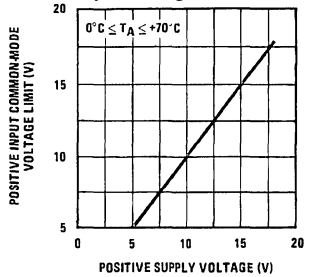
Negative Current Limit



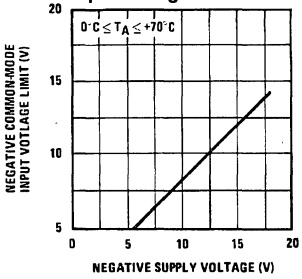
Positive Current Limit



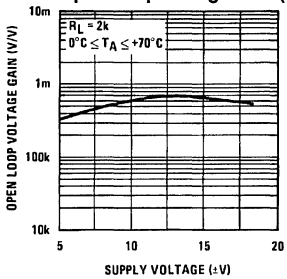
Positive Common-Mode Input Voltage Limit



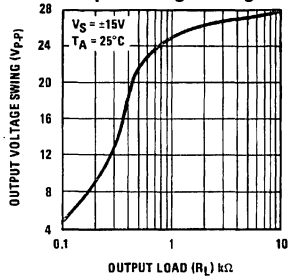
Negative Common-Mode Input Voltage Limit



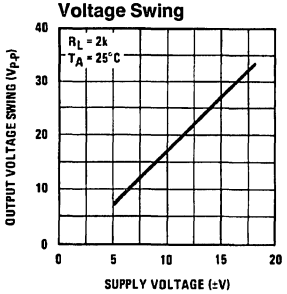
Open Loop Voltage Gain (V/V)



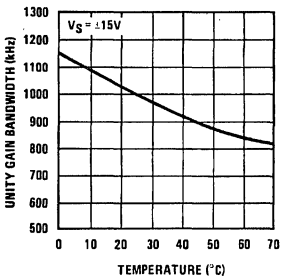
Output Voltage Swing



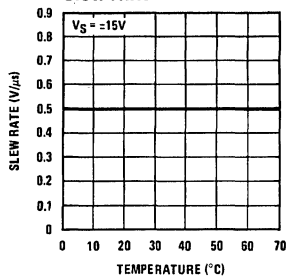
Voltage Swing



Gain Bandwidth



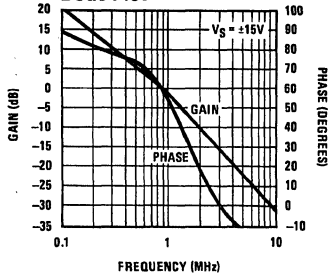
Slew Rate



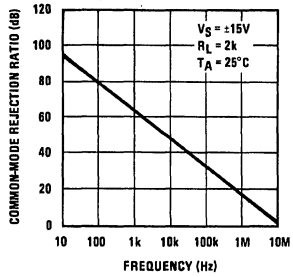
TL/H/9296–3

Typical Performance Characteristics (Continued)

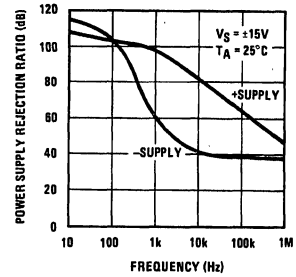
Bode Plot



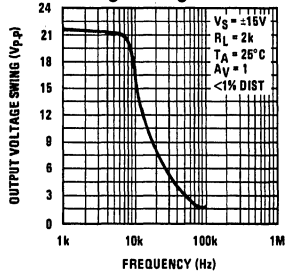
Common-Mode Rejection Ratio



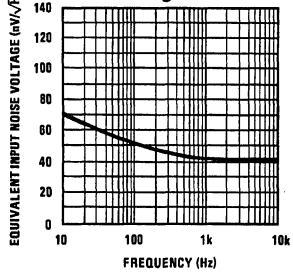
Power Supply Rejection Ratio



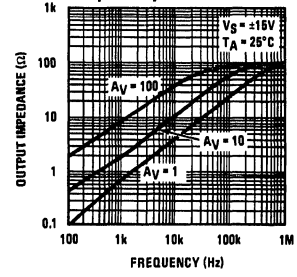
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage



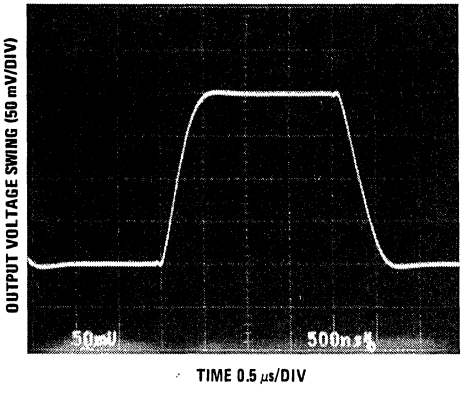
Output Impedance



TL/H/9296–4

LF13741 Pulse Responses

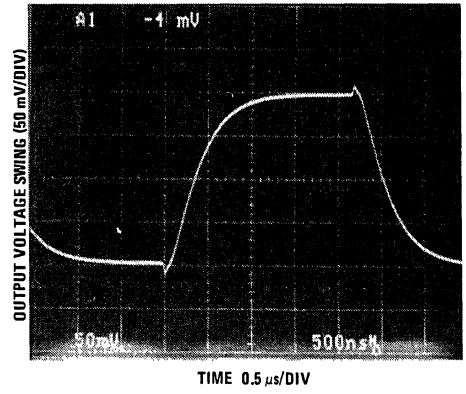
Small Signal Non-Inverting Pulse Response



TL/H/9296–5

A_V = +1(Follower)

Small Signal Inverting Pulse Response



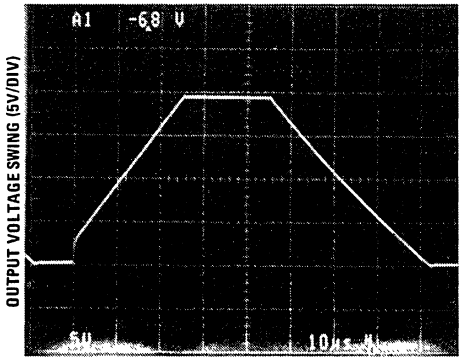
TL/H/9296–6

A_V = −1(Inverter)

Typical Performance Characteristics (Continued)

LF13741 Pulse Responses (Continued)

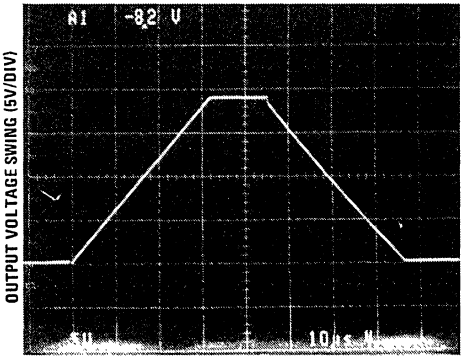
Large Signal Non-Inverting Pulse Response



TIME 10 μs/DIV

TL/H/9296-7

Large Signal Inverting Pulse Response



TIME 10 μs/DIV

TL/H/9296-8

Application Hints

GENERAL CHARACTERISTICS

The LF13741 makes the job of converting from a bipolar to an FET input op amp easy. As a systems designer you are probably very familiar with the operating characteristics of a 741 op amp. In fact, many of you have used 741s with FET input followers—that's just what the LF13741 is, but it's all on a single die.

When you need a low cost, reliable, well known op amp with low input currents and moderate speed, use an LF13741.

DIFFERENTIAL INPUTS

You don't have to use clamps across the inputs for differential input voltages of less than 40V. The input JFETs of the LF13741, in addition to being well matched, have large reverse breakdown voltages from gate to source and drain.

POSITIVE INPUT COMMON-MODE VOLTAGE LIMIT

With the LF13741 (unlike the normal 741) you can take both inputs above the positive supply voltage by more than 0.1V before the amplifier ceases to function. This feature enables you to use the LF13741 to monitor and/or limit the current from the same supply used to power it (see typical applications).

If you exceed the positive common-mode voltage limit on only one input, the output phase will remain correct. When you exceed the limit on both inputs, the output phase is unpredictable.

NEGATIVE INPUT COMMON-MODE VOLTAGE LIMIT

There are two negative input voltage ranges of interest:

1. The range between the negative common-mode voltage limit and the negative supply voltage.
2. Voltages which are more negative than the negative supply voltage.

If you take only one of the inputs of the LF13741 into the first range, the output phase will remain correct. When you take both inputs into this range the output will go toward the positive supply voltage.

If you force either or both of the inputs into the second range, an internal diode will be turned "ON." Unless you externally limit the diode current to about 1 mA, the device will be destroyed. In either case, limited or unlimited input current, you cannot predict the output.

HANDLING

You do not have to take any special precautions in handling the LF13741. It has JFET, as opposed to fragile MOSFET, inputs.

APPLYING POWER

You should never: reverse the power supplies to the LF13741; plug a part in backwards in a powered socket or board; make the negative supply voltage more positive than an input voltage.

Any one of these supply conditions will forward bias an internal diode. If you have not externally limited the resulting current, the device will be destroyed.

LAYOUT

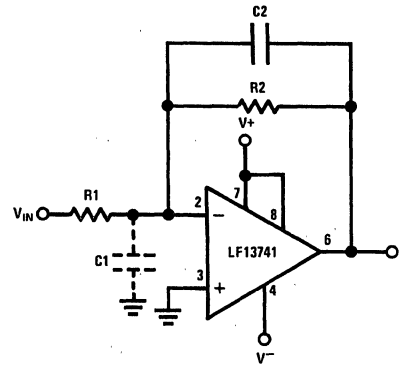
To ensure stability of response you should take care with lead dress, component placement and power supply decoupling. For example, the body of feedback resistors (from output to input pins) should be placed close to the inverting input pin. Noise "pickup" and capacitance to ground from the input pin will be minimized—effects which are usually desirable.

Because of the very low input bias currents of the LF13741, special care should be taken in printed circuit board layouts to prevent unnecessary leakage from the input nodes, (see Typical Applications).

Application Hints (Continued)

FEEDBACK POLE

You create a feedback pole when you place resistive feedback around an amplifier. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency (a distinct possibility when using FET op amps), you should place a lead capacitor from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant *(Figure 1).*



TL/H/9296–9

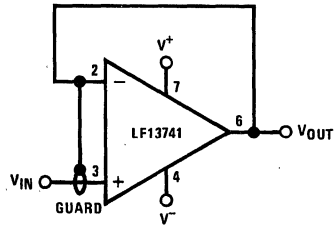
Parasitic input capacitance C1 ≅ (3 pF for LF13741 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

FIGURE 1

Typical Applications (Continued)

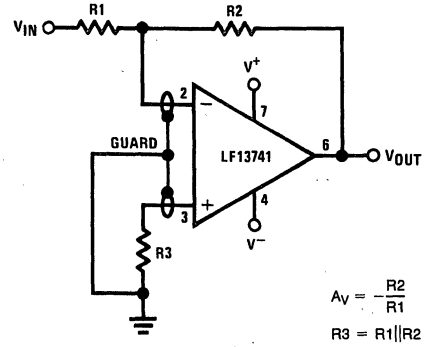
Circuits Using Guard Rings to Prevent Leakage Currents Between Inputs and V⁻

Guarded Voltage Follower



TL/H/9296–10

Guarded Inverting Amplifier

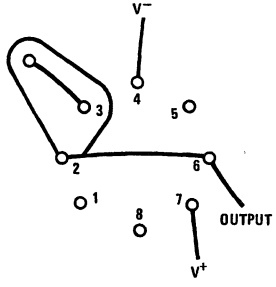


$$A_V = -\frac{R2}{R1}$$

$$R3 = R1 \| R2$$

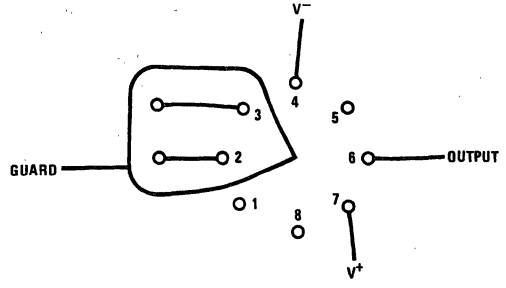
TL/H/9296–11

PC Layout



TL/H/9296–12

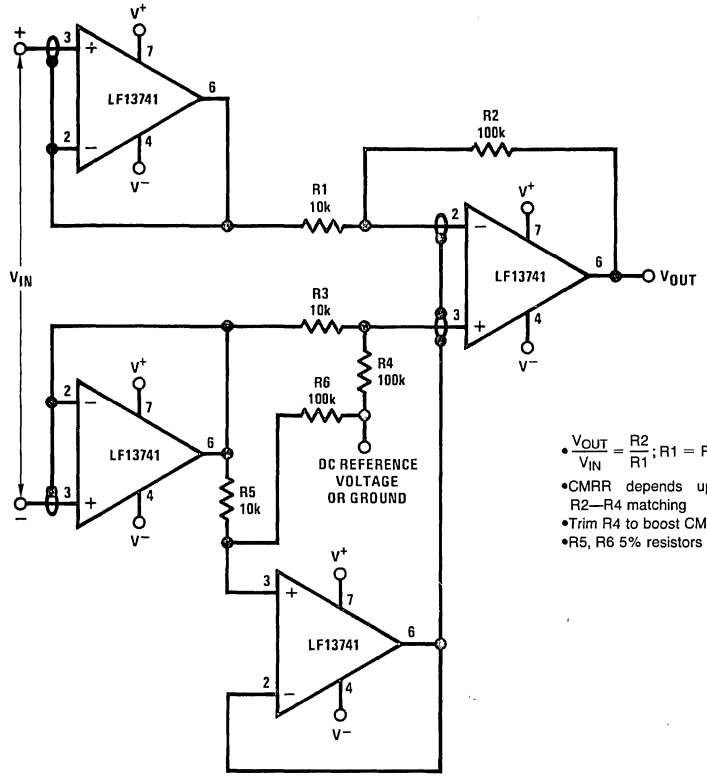
PC Layout



TL/H/9296–13

Typical Applications (Continued)

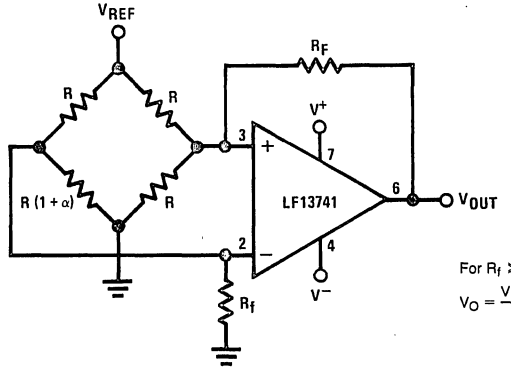
Guarded Instrumentation Amplifier



- $\frac{V_{OUT}}{V_{IN}} = \frac{R2}{R1}$; R1 = R3, R2 = R4
- CMRR depends upon R1—R3, R2—R4 matching
- Trim R4 to boost CMRR
- R5, R6 5% resistors

TL/H/9296–14

Bridge Amplifier



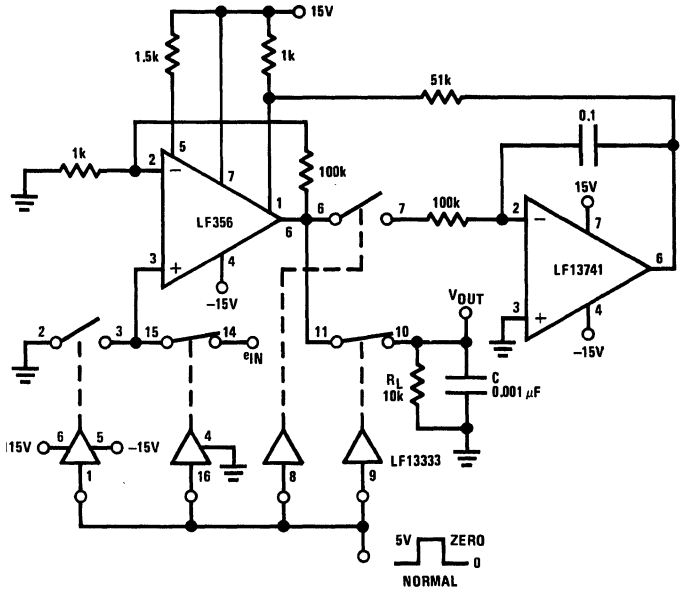
For $R_f \gg R$

$$V_O = \frac{V_{REF}}{2}\left(\frac{R_F}{R}\right)\left(\frac{\alpha}{1+\alpha}\right)$$

TL/H/9296–15

Typical Applications (Continued)

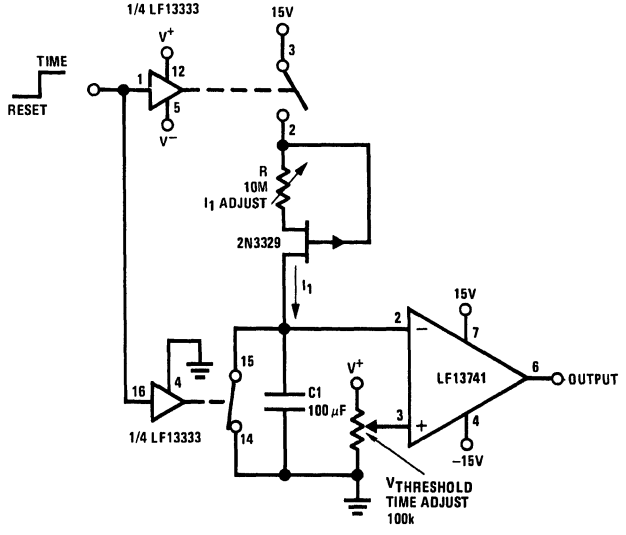
Auto Zero Circuit for LF356



TL/H/9296–16

- With the output having a 10k load resistor minimum pulse width to zero ≈800 μs
- The capacitor on the output reduces the output switch glitch

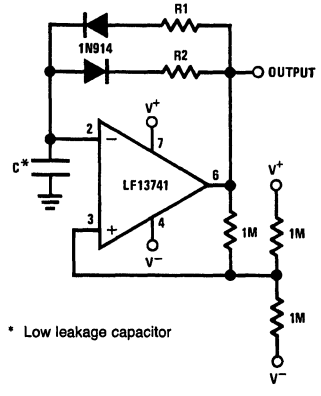
Long Time Timer



TL/H/9296–17

- Time = $\frac{C1}{I_1} V_{THRESHOLD}$
- Output goes high on time out
- Reverse op amp inputs for output low on time out
- C1 low leakage capacitor

Ultra-Low (or High) Duty Cycle Pulse Generator



* Low leakage capacitor

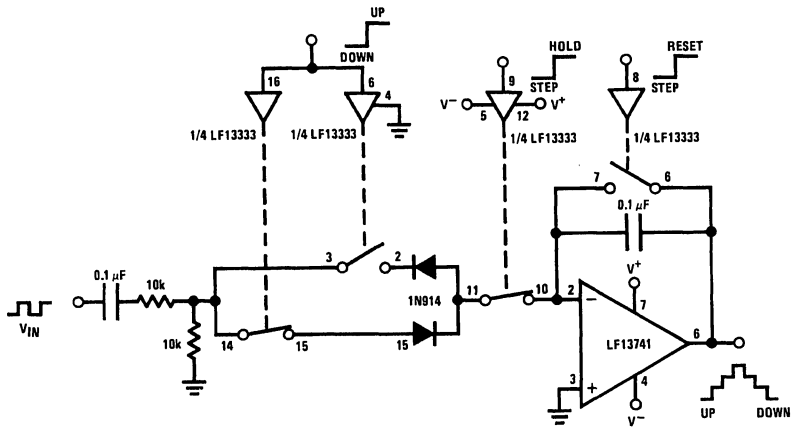
TL/H/9296–18

- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

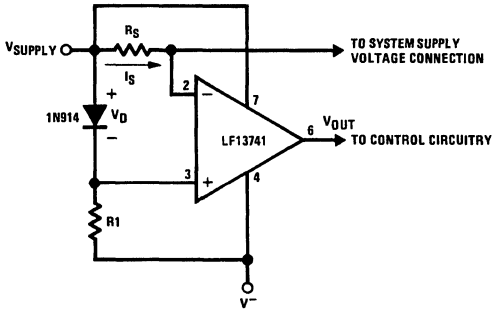
Typical Applications (Continued)

Up/Down Staircase Generator/Step and Hold



TL/H/9296-19

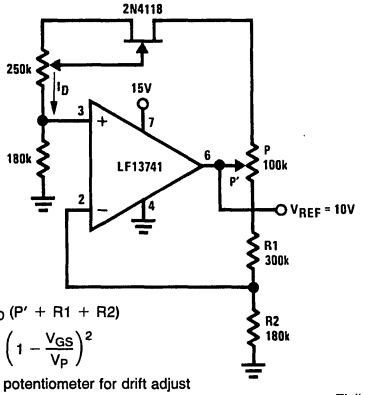
Supply Current Indicator/Limiter



TL/H/9296-20

- V_{OUT} switches high when $R_S I_S > V_D$

Low Drift Adjustable Voltage Reference



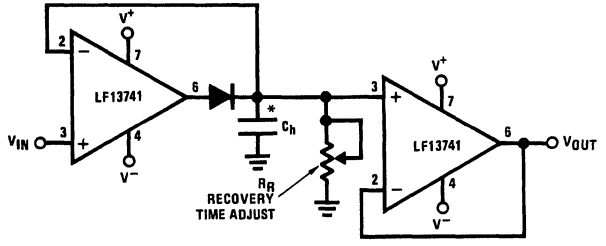
- $V_{REF} = I_D (P' + R1 + R2)$

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- Trim 250k potentiometer for drift adjust
- Trim 100k potentiometer for V_{REF} adjust

TL/H/9296-21

Low Drift Peak Detector

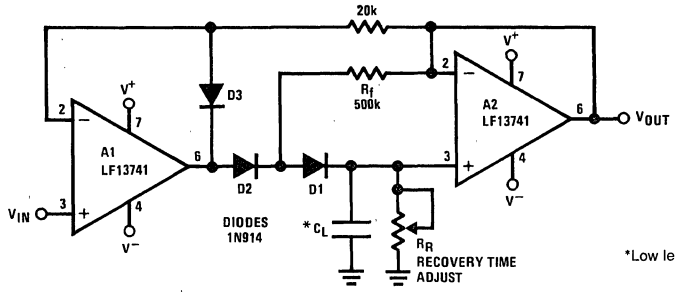


TL/H/9296-23

*Low leakage capacitor

Typical Applications (Continued)

Ultra-Low Drift Peak Detector

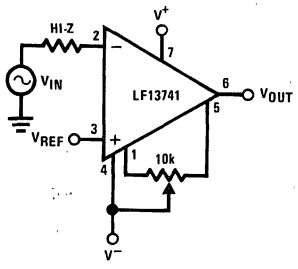


*Low leakage capacitor

TL/H/9296–24

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is I_B plus leakage of C_h.
- D3 clamps V_{OUT} A1 to $V_{IN} - V_{D3}$ to improve speed and to limit the reverse bias of D2.
- Maximum input frequency should be $\ll \frac{1}{2\pi} R_f C_{D2}$, where C_{D2} is the shunt capacitance of D2.

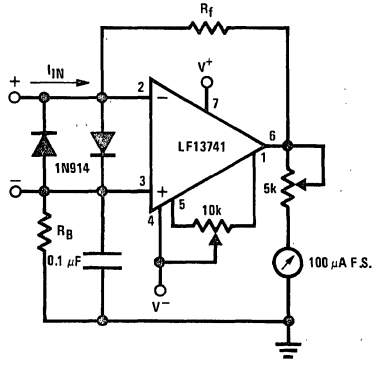
Comparator with Offset Adjust for Hi-Z Inputs



TL/H/9296–25

$V^- + 3V \leq V_{IN} \leq V^+ + 0.1V$

Low Current Ammeter

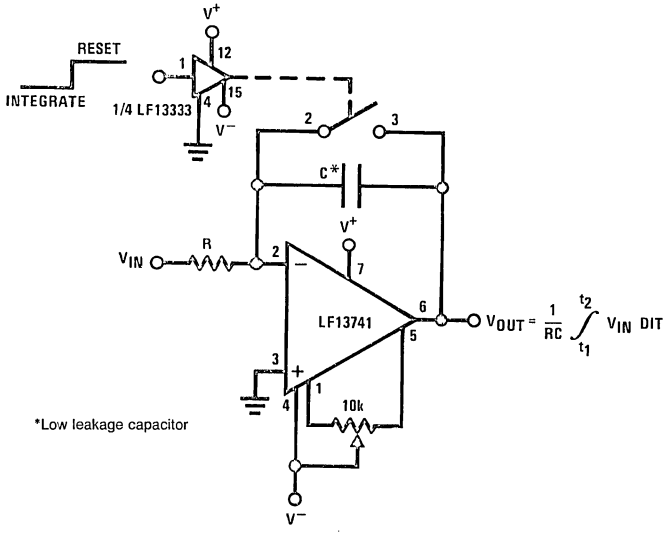


TL/H/9296–26

$I_{FULL\ SCALE}$	R_F	R_B
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

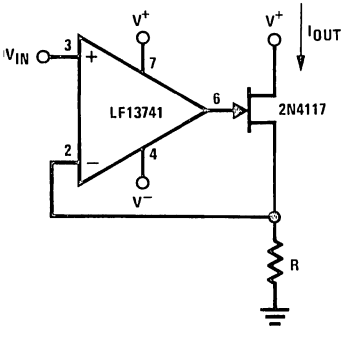
Typical Applications (Continued)

Long Time Integrator



TL/H/9296–27

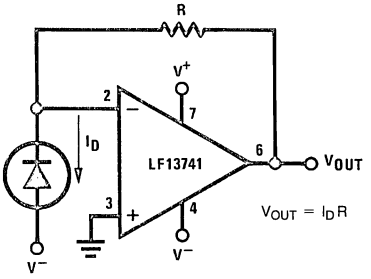
Precision Current Sink



TL/H/9296–28

$I_{OUT} = \frac{V_{IN}}{R}$, where $I_{OUT} \leq I_{DSS}$

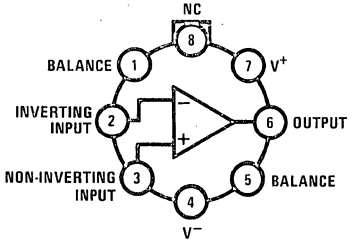
Photo Cell Amplifier (I to V Converter)



TL/H/9296–29

Connection Diagrams (Top Views)

TO-99 Metal Can Package

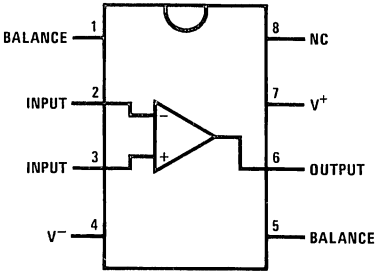


TL/H/9296–30

Note: Pin 4 connected to case.

Order Number LF13741H
See NS Package Number H08C

Dual-In-Line Package



TL/H/9296–31

Order Number LF13741N
See NS Package Number N08E

National Semiconductor

PRELIMINARY

LH0003/LH0003C
Wide Bandwidth Operational Amplifier

General Description

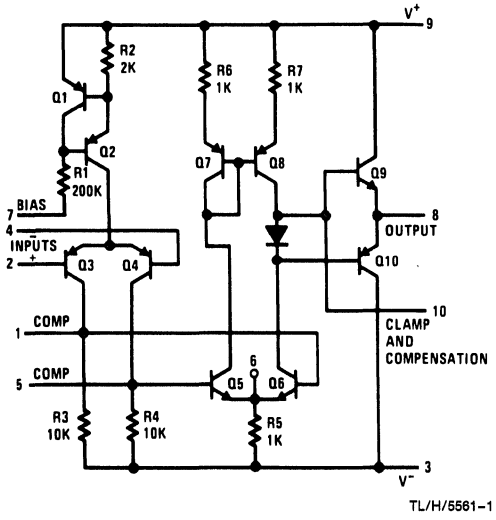
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 V/μs, a gain bandwidth of up to 30 MHz, and high output currents.

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

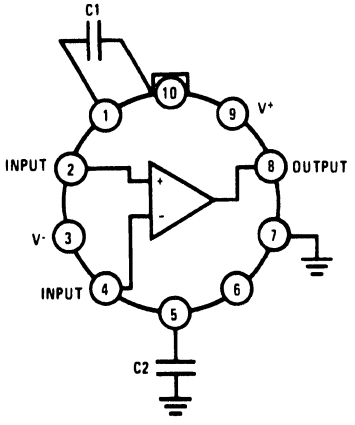
Features

■ Very low offset voltage	Typically 0.4 mV
■ Large output swing	> ±10V into 100Ω load
■ High CMRR	Typically >90 dB
■ Good large signal frequency response	50 kHz to 400 kHz depending on compensation

Schematic and Connection Diagrams



TL/H/5561–1



TL/H/5561–2

Top View

Order Number LH0003H or LH0003CH
See NS Package Number H10G

Typical Compensation

Circuit Gain	C_1 pF	C_2 pF	Slew Rate R_L > 200Ω, V/μsec	Full Output Frequency R_L > 200Ω V_{OUT} = ±10V
≥40	0	0	70	400
≥10	5	30	30	350
≥ 5	15	30	15	250 kHz
≥ 2	50	50	5	100
≥ 1	90	90	2	50

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Supply Voltage	±20V
Power Dissipation	See Curve
Differential Input Voltage	±7V
Input Voltage	Equal to Supply
Load Current	120 mA
Operating Temperature Range	
LH0003	−55°C to +125°C
LH0003C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Notes 1 & 2)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S < 100\Omega$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	$V_S = \pm 20V$		1.2	3	mA
Voltage Gain	$R_L = 100k, V_S = \pm 15V, V_{OUT} = \pm 10V$	20	70		V/mV
	$R_L = 2k, V_S = \pm 15V, V_{OUT} = \pm 10V$	15	40		V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 100\Omega$	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S \leq 100\Omega$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 100\Omega, V_S = \pm 15V, V_{IN} = \pm 10V$	70	90		dB
PSRR	$R_S < 100\Omega, V_S = \pm 15V, \Delta V = 5V$ to 20V	70	90		dB
Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 10 kHz to 100 kHz $V_S = \pm 15V$ dc		1.8		μVrms

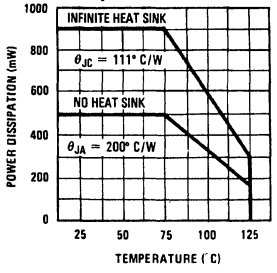
Note 1: These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor C_1 = 90 pF from Pin 1 to Pin 10 and C_2 = 90 pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

Note 2: Typical values are for T_A = 25°C unless otherwise specified.

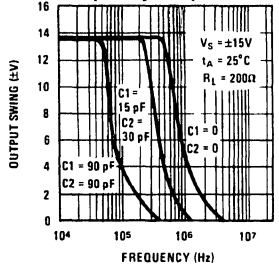
Note 3: Refer to RETS0003X for LH0003H military specifications.

Typical Performance Characteristics

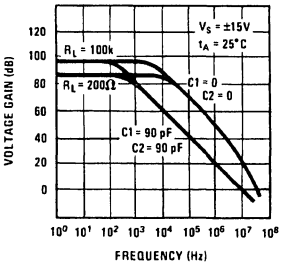
Maximum Power Dissipation



Large Signal Frequency Response



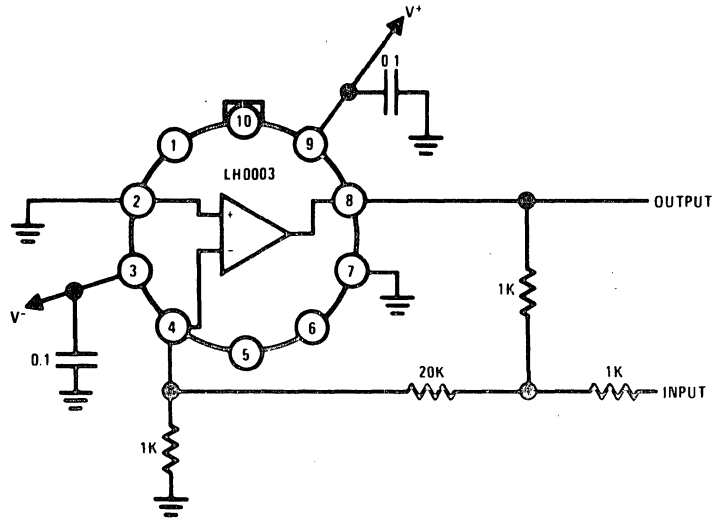
Open Loop Frequency Response



TL/H/5561–5

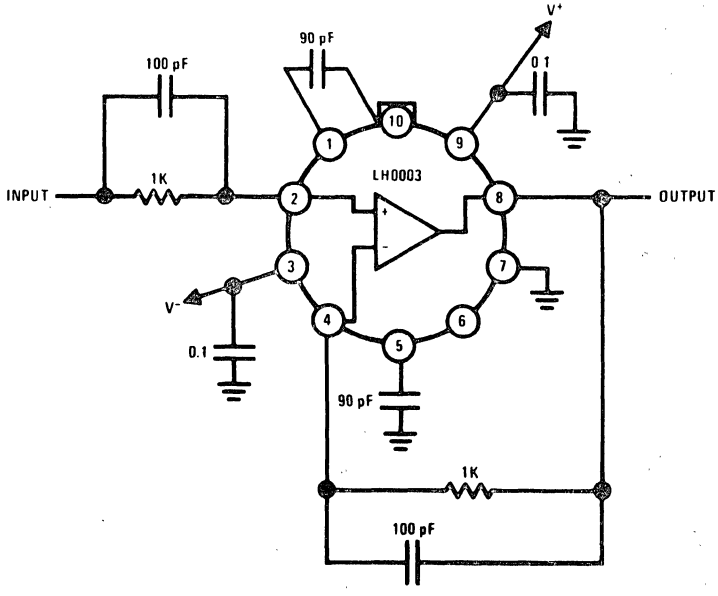
Typical Applications

High Slew Rate Unity Gain Inverting Amplifier



TL/H/5561–3

Unity Gain Follower



TL/H/5561–4

National Semiconductor

LH0004/LH0004C High Voltage Operational Amplifier

General Description

The LH0004/LH0004C is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V.

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

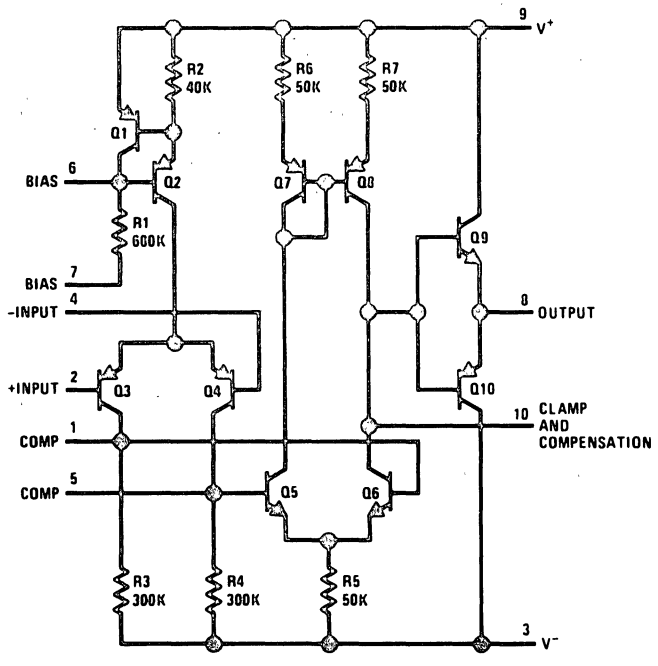
Features

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 kΩ load with ±40V supplies
- Low input offset current typically 20 nA for the LH0004 and 45 nA for the LH0004C
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

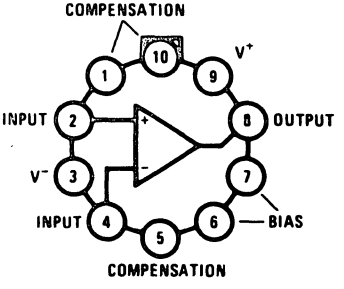
Applications

- Precision high voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams



TL/H/5559–1



TL/H/5559–2

Note: Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 kΩ per volt of potential between Pin 3 and Pin 9.

Order Number LH0004H or LH0004CH
See NS Package Number H10G

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage, Continuous	±45V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to Supply
Short Circuit Duration	3 sec
Operating Temperature Range	
LH0004	−55°C to +125°C
LH0004C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

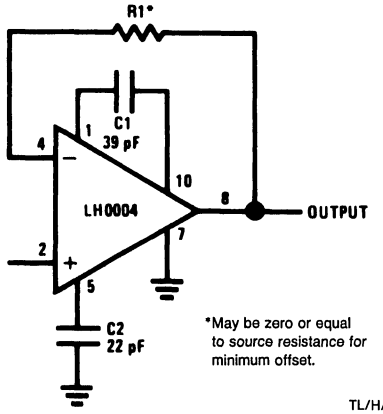
Parameter	Conditions	LH0004			LH0004C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		0.3	1.0 2.0		0.3	1.5 3.0	mV
Input Bias Current	$T_A = 25°C$		20	100 300		30	120 300	nA
Input Offset Current	$T_A = 25°C$		3	20 100		10	45 150	nA
Positive Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		110	150 175		110	150 175	μA
Negative Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		80	100 135		80	100 135	μA
Voltage Gain	$V_S = \pm 40V$, $R_L = 100k$, $T_A = 25°C$ $V_{OUT} = \pm 30V$	30	60		30	60		V/mV
	$V_S = \pm 40V$, $R_L = 100k$ $V_{OUT} = \pm 30V$	10			10			V/mV
Output Voltage	$V_S = \pm 40V$, $R_L = 10k$		±35	±30		±33	±30	V
CMRR	$V_S = \pm 40V$, $R_S \leq 5k$ $V_{IN} = \pm 33V$	70	90		70	90		dB
PSRR	$V_S = \pm 40V$, $R_S \leq 5k$ $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 100\Omega$		4.0			4.0		μV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		nA/°C
Equivalent Input Noise Voltage	$R_S = 100\Omega$, $V_S = \pm 40V$ $f = 500$ Hz to 5 kHz, $T_A = 25°C$		3.0			3.0		μVrms

Note 1: These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

Note 2: Refer to RETS0004X for LH0004H military specifications.

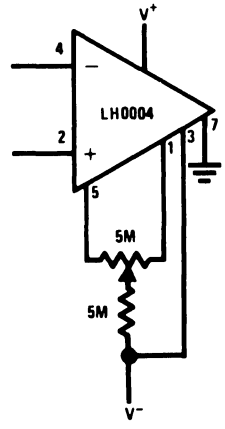
Typical Applications

Voltage Follower



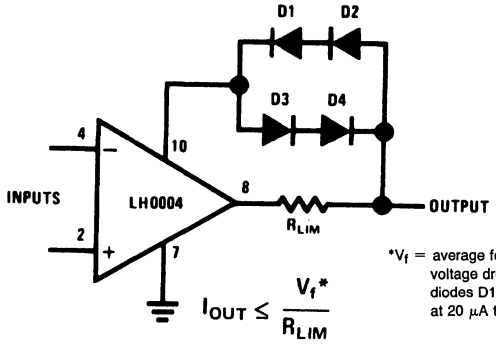
TL/H/5559–3

Input Offset Voltage Adjust



TL/H/5559–4

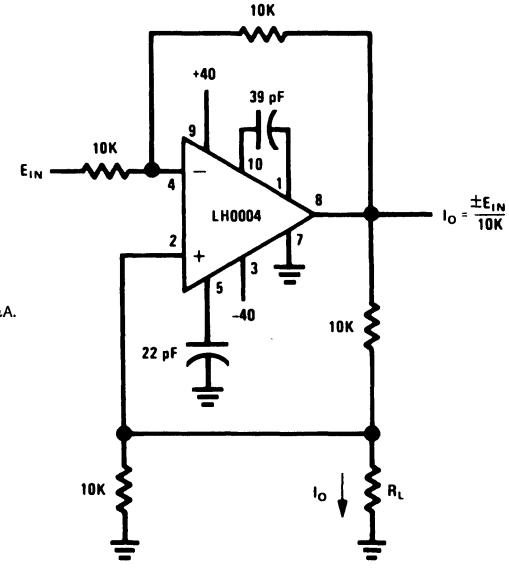
External Current Limiting Method



*V_f = average forward voltage drop of diodes D1 to D4 at 20 μA to 50 μA.

TL/H/5559–5

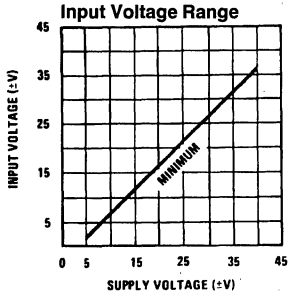
High Compliance Current Source



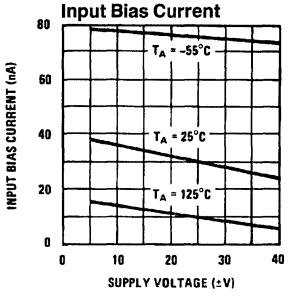
TL/H/5559–6

Typical Performance Characteristics

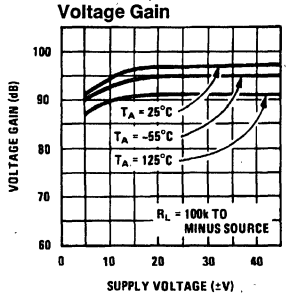
Input Voltage Range



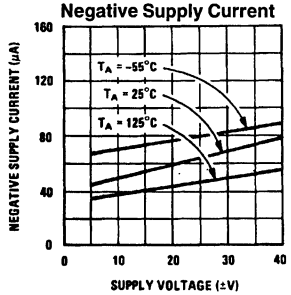
Input Bias Current



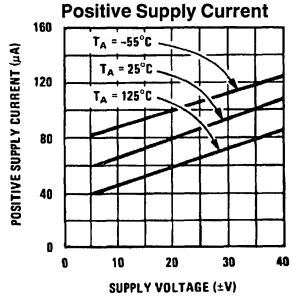
Voltage Gain



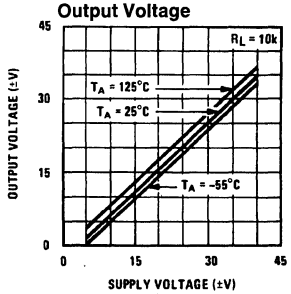
Negative Supply Current



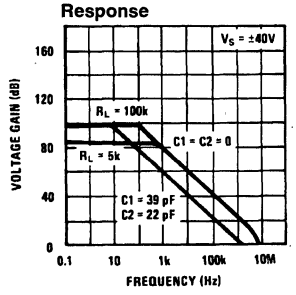
Positive Supply Current



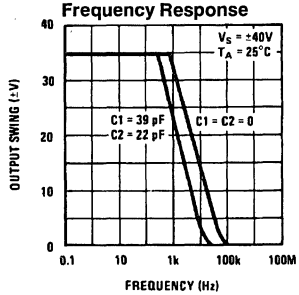
Output Voltage



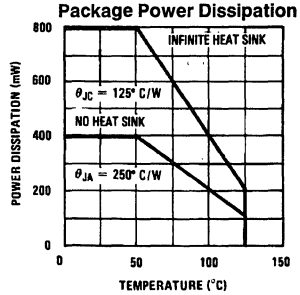
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



TL/H/5559–7

National Semiconductor

LH0020/LH0020C High Gain Operational Amplifier

General Description

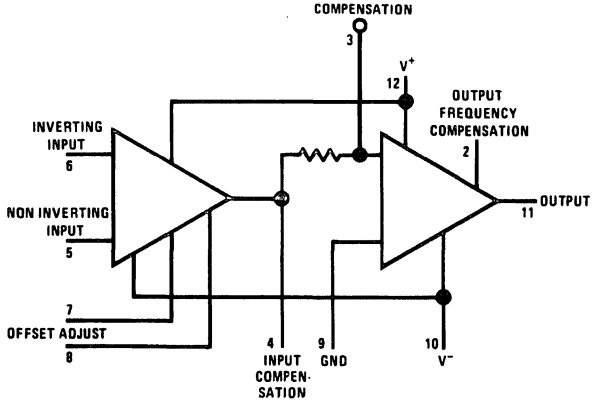
The LH0020/LH0020C is a general purpose operational amplifier designed to source and sink 50 mA output currents. In addition to its high output capability, the LH0020/LH0020C exhibits excellent open loop gain, typically in excess of 100 dB. The parameters of the LH0020 are guaranteed over the temperature range of −55°C to +125°C and $\pm 5V \leq V_S \leq \pm 22V$, while those of the LH0020C are guaranteed over the temperature range of 0°C to +85°C and $\pm 5V \leq V_S \leq \pm 18V$.

Output current capability, excellent input characteristics, and large open loop gain make the LH0020/LH0020C suitable for application in a wide variety of applications from precision DC power supplies to precision medium power comparator.

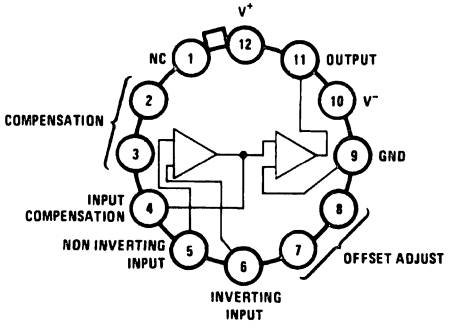
Features

- Low offset voltage typically 1.0 mV at 25°C over the entire common-mode voltage range
- Low offset current typically 10 nA at 25°C for the LH0020 and 30 nA for the LH0020C
- Offset voltage is adjustable to zero with a single potentiometer
- ±14V, 50 mA output capability

Schematic and Connection Diagrams



TL/H/5554–1



TL/H/5554–2

Top View

Order Number LH0020G or LH0020CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Supply Voltage	±22V
Power Dissipation	1.5W
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0020	−55°C to +125°C
LH0020C	0°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 2) $T_{min} \le T_A \le T_{max}$ unless otherwise specified

Parameter	Conditions	LH0020			LH0020C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 100\Omega$, $T_A = 25°C$ Over Temp.		1.0 2.0	2.5 4.0		1.0 3.0	6.0 7.5	mV mV
Input Offset Current	$T_A = 25°C$ Over Temp.		10	50 100		30	200 300	nA nA
Input Bias Current	$T_A = 25°C$ Over Temp.		60	250 500		200	500 800	nA nA
Supply Current	$V_S = \pm 15V$, $T_A = 25°C$		3.5	5.0		3.6	6.0	mA
Input Resistance	$T_A = 25°C$	0.6	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$, $T_A = 25°C$ $V_S = \pm 15V$, $R_L = 300\Omega$, $V_O = \pm 10V$, $T_A = 25°C$	100 50	300		50 30	150		V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 300\Omega$, $T_A = 25°C$ Over Temp.	14.2 14.0	14.5		14.0 13.5	14.2		V V
Output Short Circuit Current	$V_S = \pm 15V$, $R_L = 0\Omega$, $T_A = 25°C$		100	130	25	120	140	mA
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common-Mode Rejection Ratio	$R_S \le 100\Omega$	90	96		90	96		dB
Power Supply Rejection Ratio	$R_S \le 100\Omega$	90	96		90	96		dB

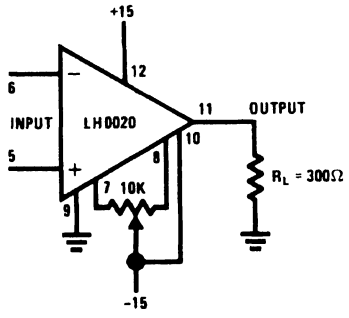
Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: These specifications apply for $\pm 5V \le V_S \le \pm 22V$ for the LH0020, $\pm 5V \le V_S \le \pm 18V$ for the LH0020C, pin 9 grounded, and a 5000 pF capacitor between pins 2 and 3, unless otherwise specified.

Note 3: Refer to RETS0020G for LH0020G military specifications.

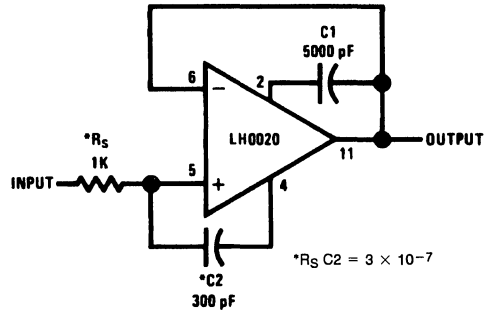
Typical Applications

Offset Adjustment



TL/H/5554–3

Unity Gain Frequency Compensation



TL/H/5554–4

National Semiconductor

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 wil provide output currents in excess of one ampere at voltage levels of ±12V; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

Features

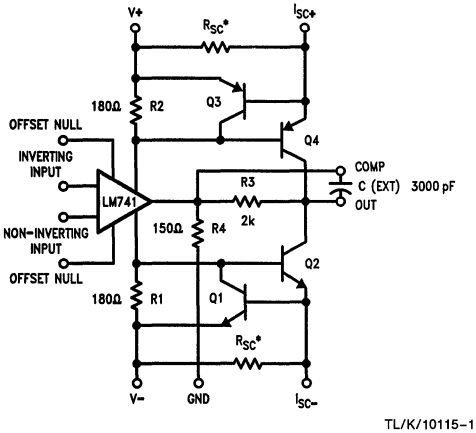
- Output current — 1.0 Amp (LH0021), 0.2 Amp (LH0041)
- Output voltage swing — ±12V into 10Ω (LH0021), ±14V into 100Ω (LH0041)
- Wide full power bandwidth — 15 kHz
- Low input offset voltage and current — 1mV and 20 nA
- Low standby power — 100 mW at ±15V
- High slew rate — 3.0V/μs
- High open loop gain — 100 dB

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

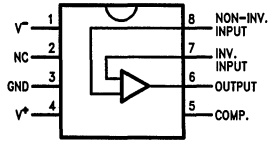
The LH0021 is supplied in a 8-pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both 12-pin TO-8 (2.5 watts with clip on heatsink) and a power 8-pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of −55°C to +125°C while the LH0021C and LH0041C are guaranteed from −25°C to +85°C.

Schematic and Connection Diagrams



TL/K/10115-1

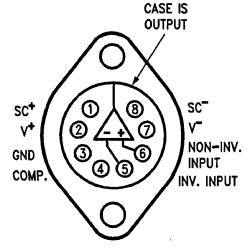
*R_{SC} external on "G" and "K" packages. R_{SC} internal on "J" package. Offset Null connections available only on "G" package.



TL/K/10115-22

Top View

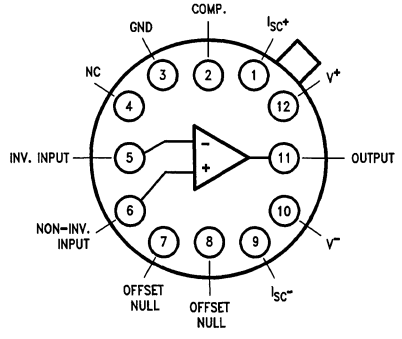
Order Number LH0041CJ
See NS Package Number HY08A



TL/K/10115-2

Top View

Order Number LH0021K or LH0021CK
See NS Package Number K08A



TL/K/10115-3

Order Number LH0041G or LH0041CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	See curves
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Peak Output Current (Note 2)	
LH0021/LH0021C	2.0 Amps
LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	
LH0021/LH0041	−55°C to +125°C
LH0021C/LH0041C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

Parameter	Conditions	Limits						Units
		LH0021			LH0021C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_C = 25°C$ $R_S \leq 100\Omega$		1.0	3.0 5.0		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		3	25		5	30	µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			5	15		5	20	µV/watt
Input Offset Current	$T_C = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_C = 25°C$		100	300 1.0		200	500 1.0	nA µA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_C = 25°C$, $V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	100 25	200		100 20	200		V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$ $V_S = \pm 15V$, $R_L = 10\Omega$, $T_C = 25°C$	±13.5 ±11.0	±14 ±12		±13 ±10	±14 ±12		V V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 0.5\Omega$	0.8	1.2	1.6	0.8	1.2	1.6	Amps
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	0.8	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

DC Electrical Characteristics for LH0041/LH0041C (Note 4)

Parameter	Conditions	Limits						Units
		LH0041			LH0041C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		1.0	3.0 5.0		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		3			5		µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			15			15		µV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Offset Current Drift with Time			2			2		nA/week
Input Bias Current	$T_A = 25°C$		100	300 1.0		200	500 1.0	nA µA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	100 25	200		100 20	200		V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	±14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000$ pF)

Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.5	3.0		1.0	3.0		V/µs
Power Bandwidth	$R_L = 100\Omega$		20			20		kHz
Small Signal Transient Response			0.3	1.0		0.3	1.5	µs
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4			4		µs
Overload Recovery Time			3			3		µs
Harmonic Distortion	$f = 1$ kHz, $P_O = 0.5W$		0.2			0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5			5		µV/rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power rating is not exceeded.

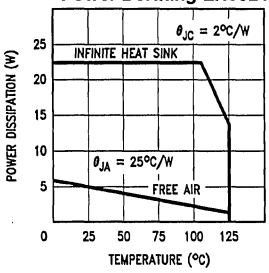
Note 4: Specifications apply for $V_S = \pm 5V$ to $\pm 18V$, and $-55°C \leq T_C \leq +125°C$ for LH0021K and LH0041G, and $-25°C \leq T_C \leq +85°C$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

Note 5: TO-8 "G" packages only.

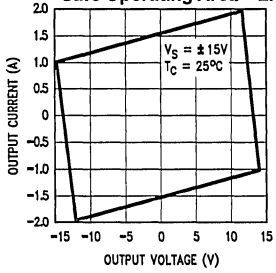
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{SC} = 3.3\Omega$.

Typical Performance Characteristics

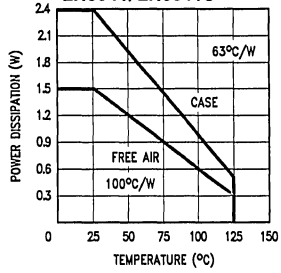
Power Derating-LH0021



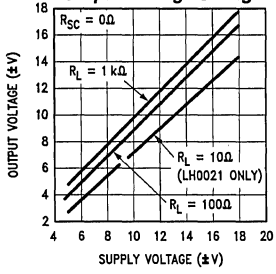
Safe Operating Area—LH0021



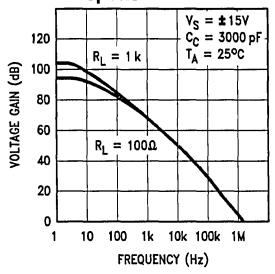
Package Power Dissipation LH0041/LH0041C



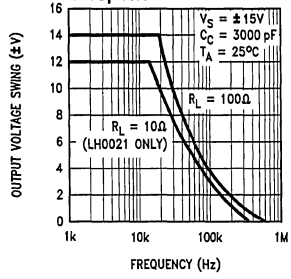
Output Voltage Swing



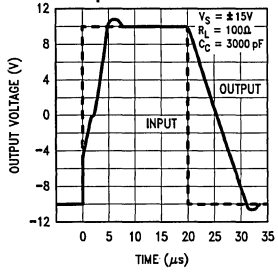
Open Loop Frequency Response



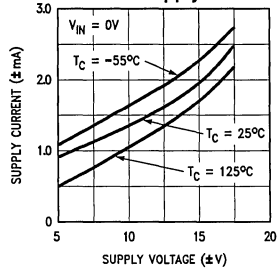
Large Signal Frequency Response



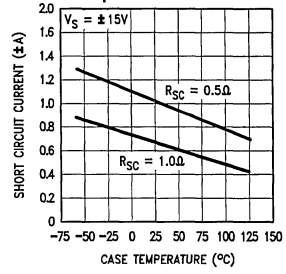
Voltage Follower Pulse Response



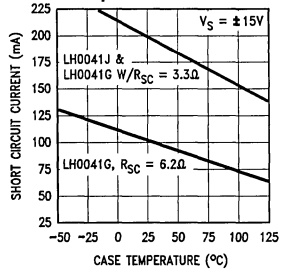
No Load Supply Current



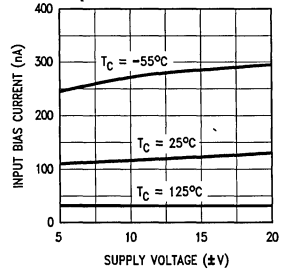
Short Circuit Current vs Temperature LH0021/LH0021C



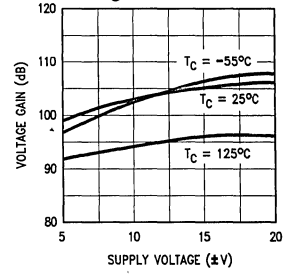
Short Circuit vs Temperature LH0041/LH0041C



Input Bias Current



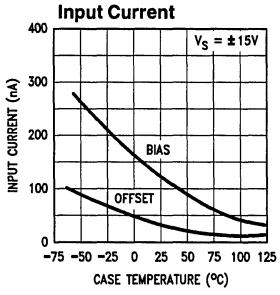
Voltage Gain

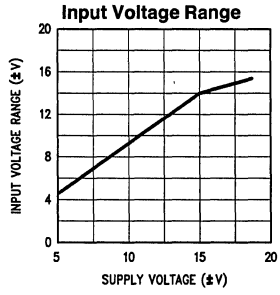


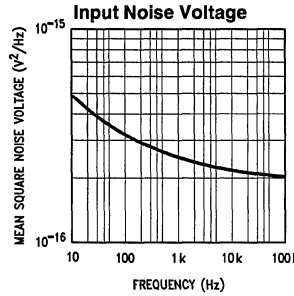
TL/K/10115–4

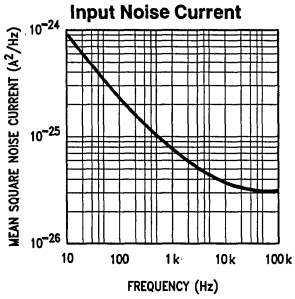
3

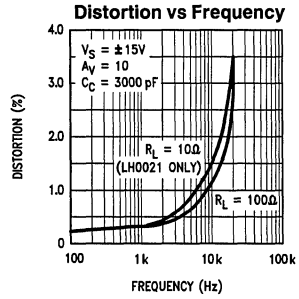
Typical Performance Characteristics (Continued)







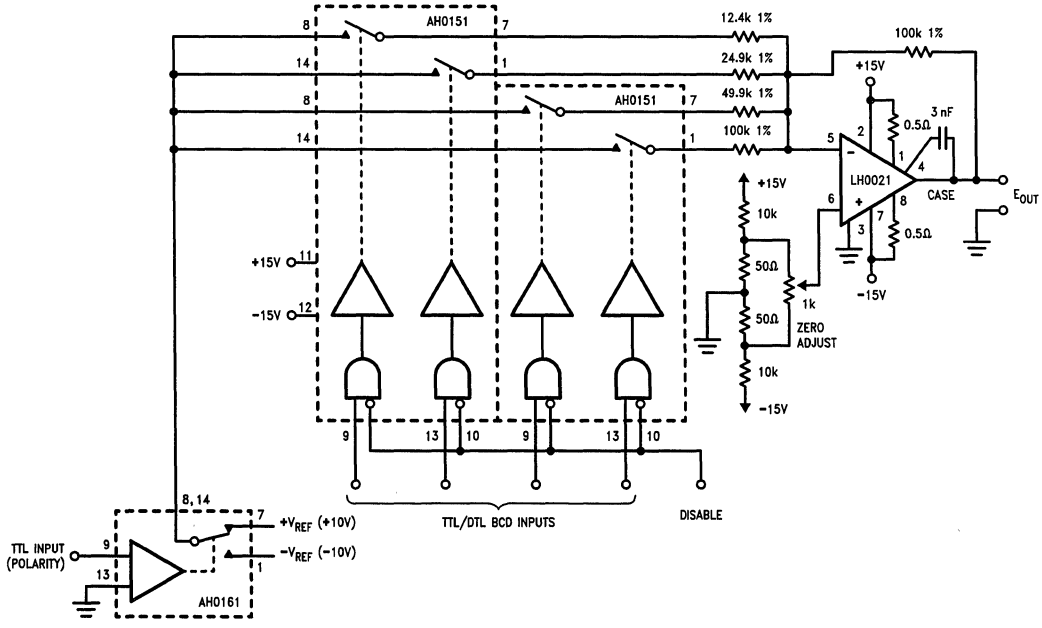




TL/K/10115–5

Typical Applications

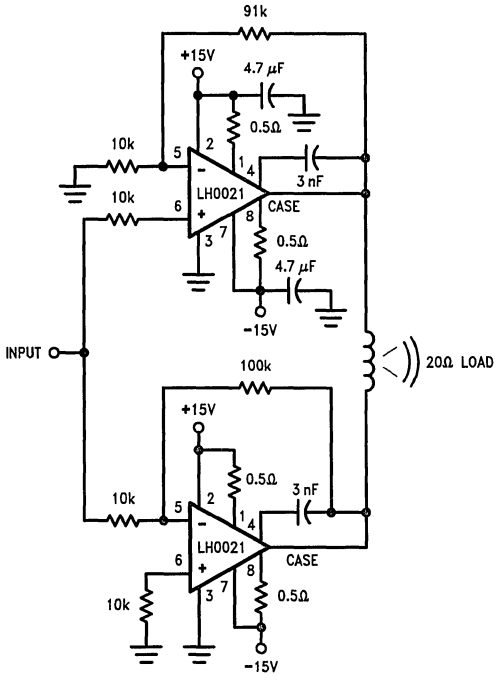
Programmable One Amp Power Supply



TL/K/10115–6

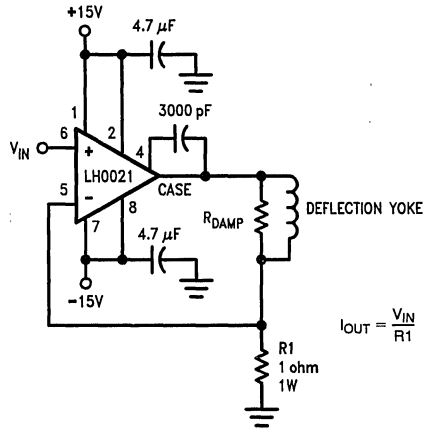
Typical Applications (Continued)

10 WATT (rms) Audio Amplifier



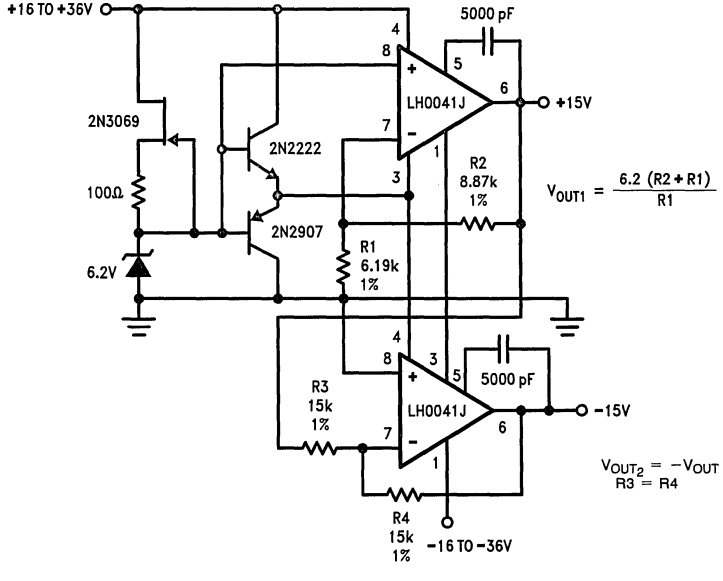
TL/K/10115–7

CRT Deflection Yoke Driver



TL/K/10115–9

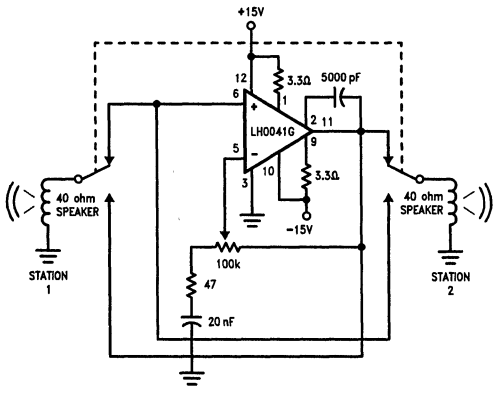
Dual Tracking One Amp Power Supply



TL/K/10115–8

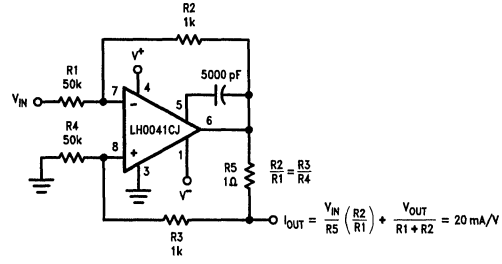
Typical Applications (Continued)

Two Way Intercom



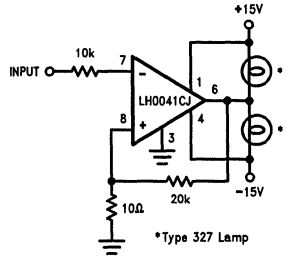
TL/K/10115–10

Programmable High Current Source/Sink



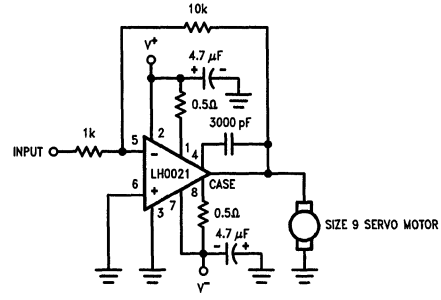
TL/K/10115–11

Power Comparator



TL/K/10115–12

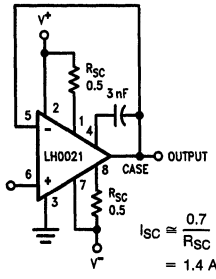
DC Servo Amplifier



TL/K/10115–13

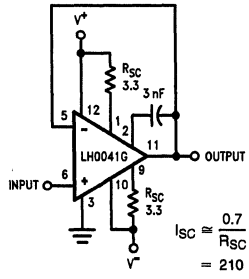
Auxiliary Circuits

LH0021 Unity Gain Circuit with Short Circuit Limiting



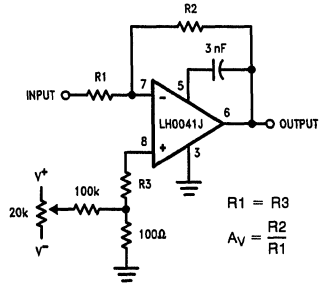
TL/K/10115–14

LH0041G Unity Gain with Short Circuit Limiting



TL/K/10115–15

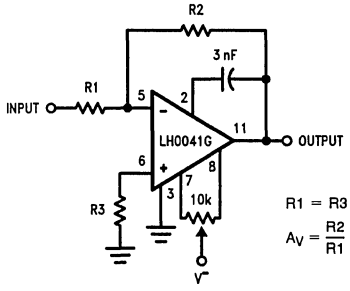
LH0041/LH0021 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*



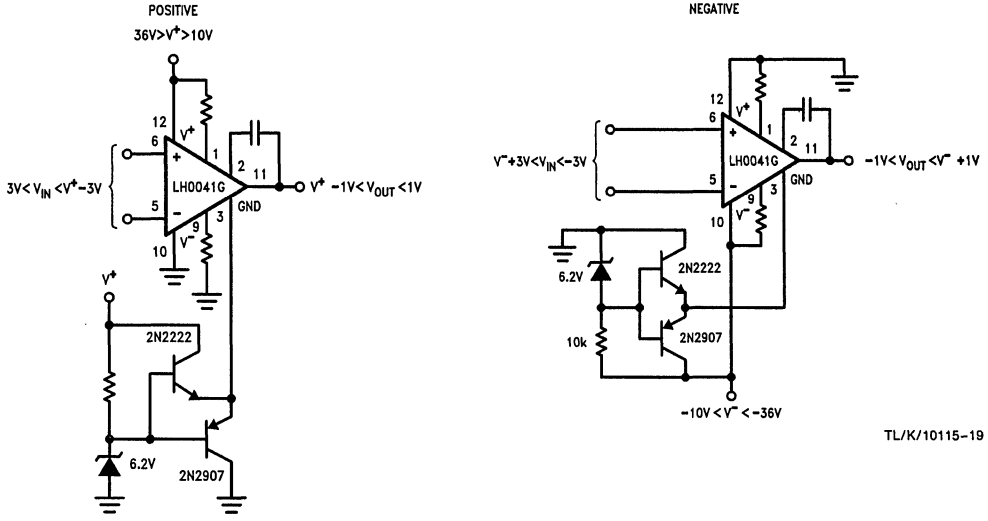
TL/K/10115–16

Auxiliary Circuits (Continued)

LH0041G Offset Voltage Null Circuit*



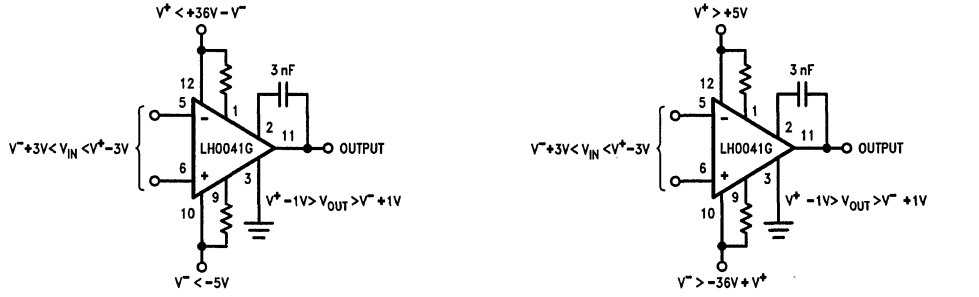
TL/K/10115–17



TL/K/10115–19

TL/K/10115–18

Operation from Single Supplies



TL/K/10115–20

TL/K/10115–21

Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

LH0022/LH0022C High Performance FET Op Amp
LH0042/LH0042C Low Cost FET Op Amp
LH0052/LH0052C Precision FET Op Amp

General Description

The LH0022/LH0042/LH0052 are a family of FET input operational amplifiers with very closely matched input characteristics, very high input impedance, and ultra-low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The internally laser nulled LH0052 offers 500 μV maximum offset and 2 μV/°C offset drift. Input offset current is less than 500 femtoamps at room temperature and 500 pA maximum at 125°C. The LH0022 and LH0042 are not internally nulled but offer comparable matching characteristics. All devices in the family are internally compensated and are free of latch-up and unusual oscillation problems. The devices may be offset nulled with a single 10k trimpot with negligible effect in CMRR.

The LH0022, LH0042 and LH0052 are specified for operation over the −55°C to +125°C military temperature range. The LH0022C, LH0042C and LH0052C are specified for operation over the −25°C to +85°C temperature range.

The LH0022/LH0042/LH0052 family of IC op amps are intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0052 is particularly suited for long term high accuracy integrators and high accuracy sample and hold buffer amplifiers. The LH0022 and LH0042 provide low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

Special electrical parameter selection is available on special request.

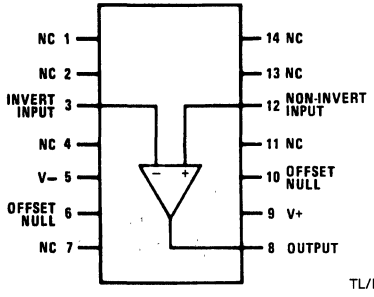
For additional application information and information on other National operational amplifiers, see *Available Linear Applications Literature.*

Features

- Low input offset current—500 femtoamps max (LH0052)
- Low input offset drift—2 μV/°C typ (LH0052)
- Low input offset voltage—100 μV typ
- High open loop gain—100 dB typ
- Excellent slew rate—3.0 V/μs typ
- Internal 6 dB/octave frequency compensation
- Pin compatible with standard IC op amps (TO-5 package)

Connection Diagrams

Dual-In-Line Package

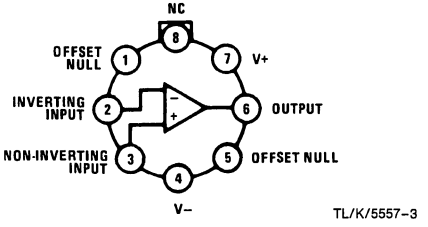


Top View

Order Number LH0022D, LH0022CD, LH0042D, LH0042CD, LH0052D or LH0052CD
See NS Package Number D14E

Order Number LH0042E
See NS Package Number E20A

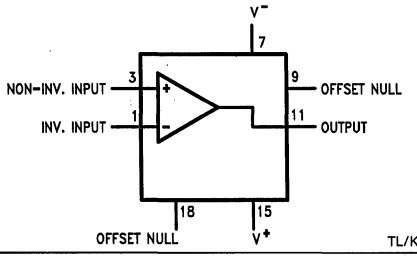
Metal Can Package



Top View

Order Number LH0022H, LH0022CH, LH0042H, LH0042CH, LH0052H or LH0052CH
See NS Package Number H08D

Leadless Chip Carrier



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (see Graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3) $T_A = T_J(Max)$

Parameter	Conditions	Limits						Units
		LH0022			LH0022C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		10			15		μV/°C
Offset Voltage Drift with Time			3			4		μV/week
Input Offset Current	(Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles Every 10°C			Doubles Every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $T_A = 25°C$, $V_S = \pm 15V$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		10			15		μV/°C
Offset Voltage Drift with Time			7.0			10		μV/week
Input Offset Current	(Note 4)		1.0	5.0		2.0	10	pA
Temperature Coefficient of Input Offset Current		Doubles Every 10°C			Doubles Every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	(Note 4)		10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	86		dB
Large Signal Voltage Gain	$R_S \leq 2\ k\Omega$, $V_{OUT} = \pm 10V$	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

DC Electrical Characteristics for LH0052/LH0052C (Note 3)

Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S < 100\ k\Omega$, $V_S = +15V$ $T_A = 25°C$		0.1	1.0		0.4	2.0	mV
	$R_S < 100\ k\Omega$, $V_S = \pm 15V$			2.0			3.0	mV
Temperature Coefficient of Input Offset Voltage	$V_S = 100\ k\Omega$, $V_S = \pm 15V$		2.0			5.0		μV/°C
Offset Voltage Drift with Time			2.0			4.0		μV/week
Input Offset Current	(Note 4)		0.01	5.0		0.02	1.0	pA
				500			100	pA
Temperature Coefficient of Input Offset Current		Doubles Every 10°C			Doubles Every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week

DC Electrical Characteristics for LH0052/LH0052C (Note 3) (Continued)

Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	(Note 4)		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$, $T_A = 25°C$	100	200		75	160		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	50			50			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		3.0	3.5		3.0	3.8	mA
Power Consumption	$V_S = \pm 15V$			105			114	mW

AC Electrical Characteristics for all amplifiers ($T_A = 25°C$, $V_S = \pm 15V$)

Parameter	Conditions	Limits						Units
		LH0022/42/52			LH0022C/42C/52C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs

AC Electrical Characteristics for all amplifiers (T_A = 25°C, V_S = ±15V) (Continued)

Parameter	Conditions	Limits						Units
		LH0022/42/52			LH0022C/42C/52C			
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
	BW = 10 Hz to 10kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10kHz		<0.1			<0.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

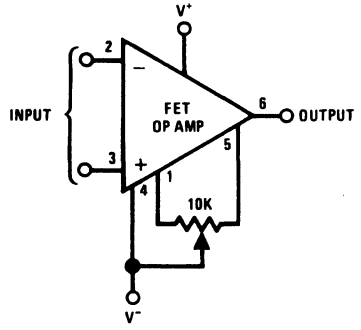
Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ +20V and −55°C ≤ T_A ≤ +125°C for the LH0022/42/52 and −25°C ≤ T_A ≤ +85°C for the LH0022C/42C/52C. Typical values are given for T_A = 25°C.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature T_j = 25°C. Self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

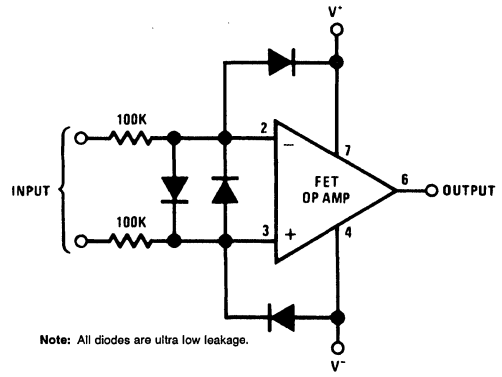
Auxiliary Circuits (Shown for TO-5 pin out)

Offset Null



TL/K/5557–5

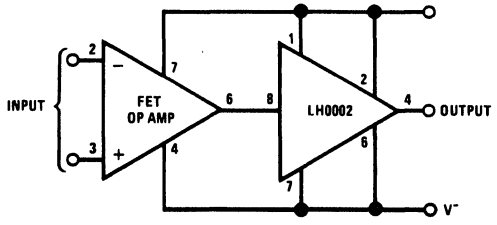
Protecting Inputs from ±150V Transients



Note: All diodes are ultra low leakage.

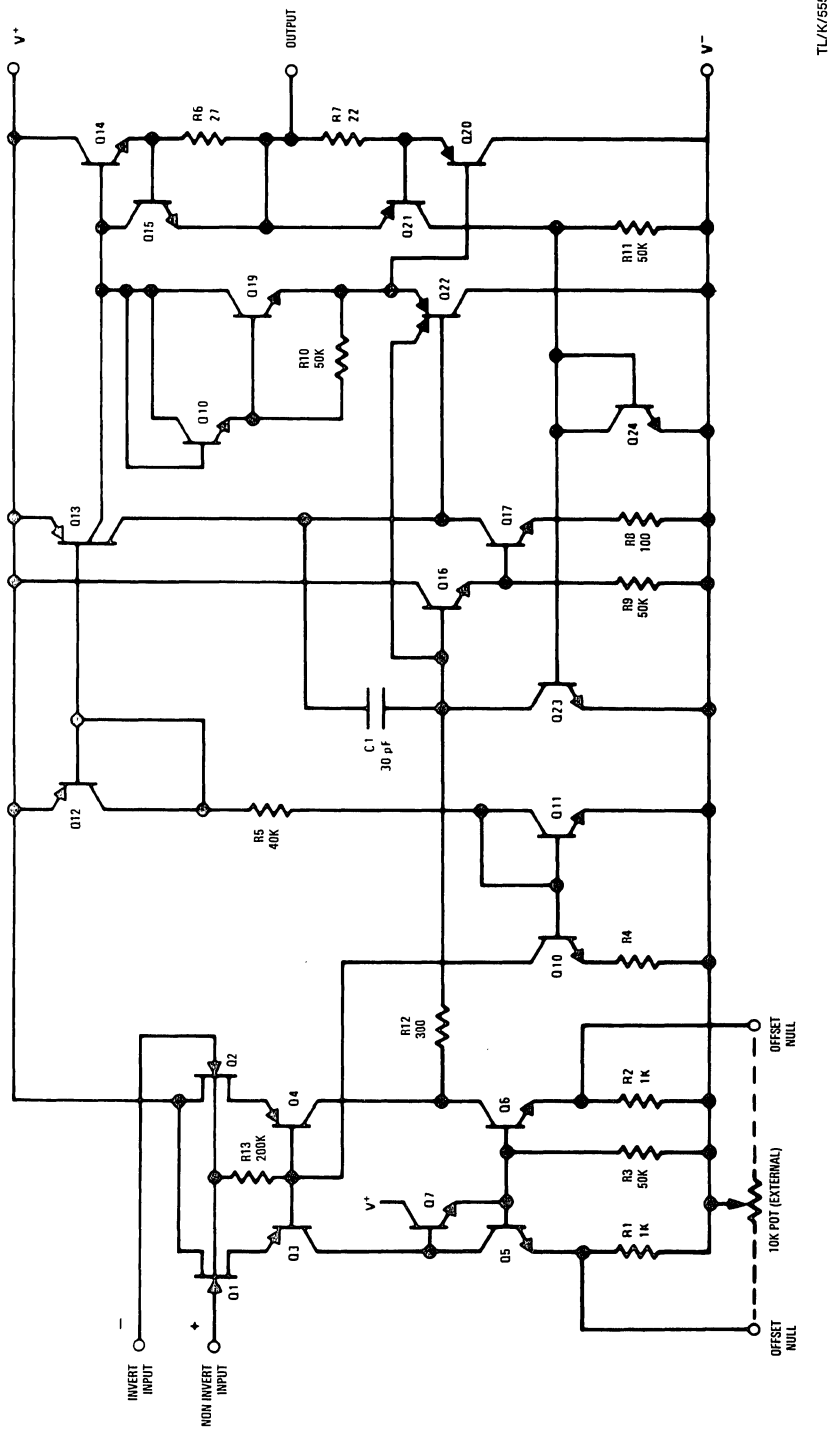
TL/K/5557–6

Boosting Output Drive to ±100 mA



TL/K/5557–7

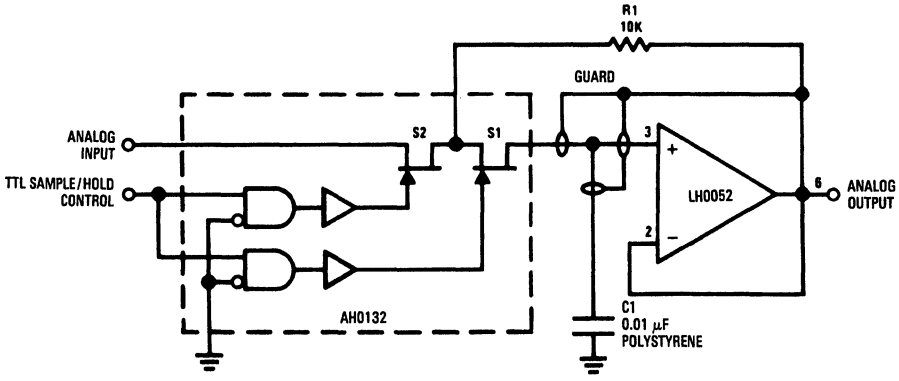
Schematic Diagram



3

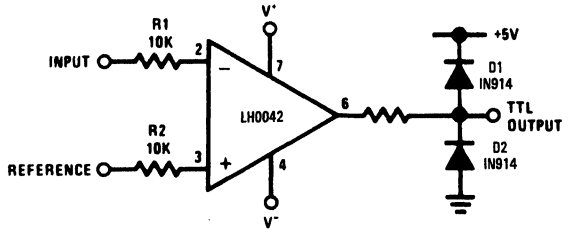
Typical Applications

Low Drift Sample and Hold



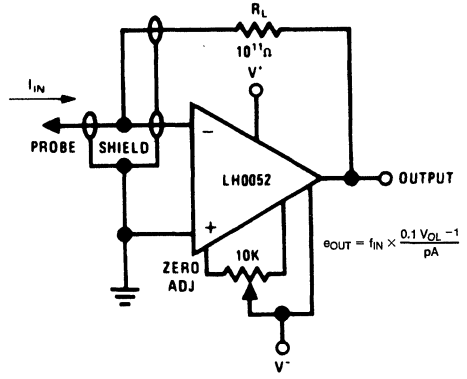
TL/K/5557–8

Precision Voltage Comparator



TL/K/5557–9

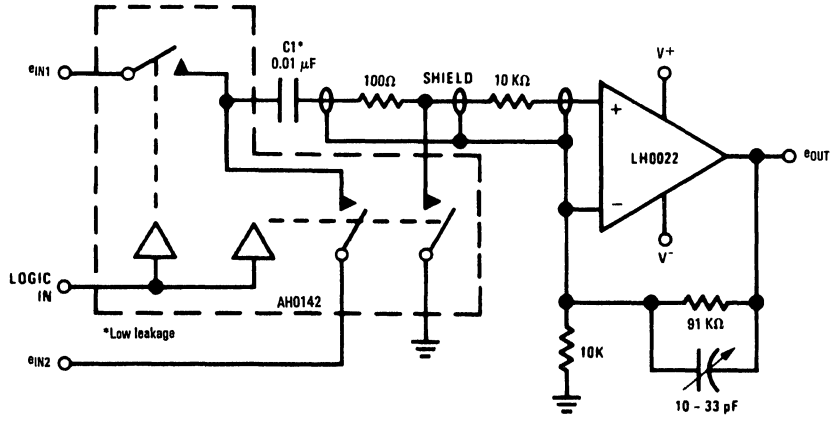
Picoamp Amplifier for pH Meters and Radiation Detectors



TL/K/5557–10

Typical Applications (Continued)

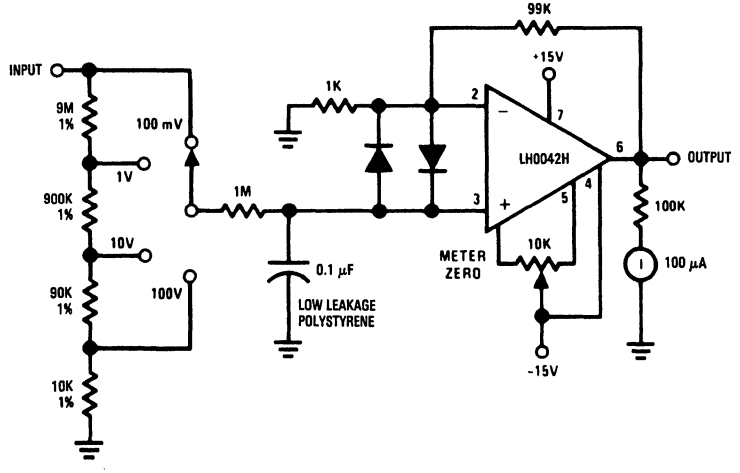
Precision Subtractor for Automatic Test Gear



TL/K/5557–11

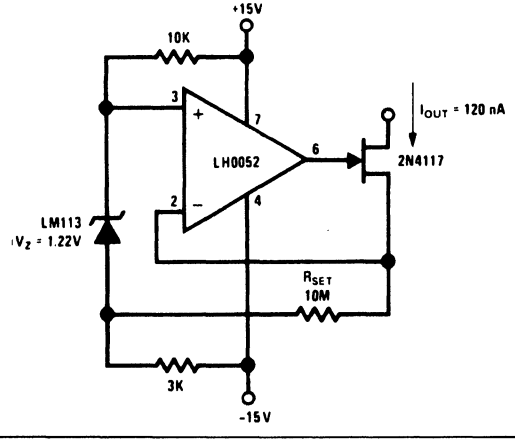
$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

Sensitive Low Cost "VTVM"



TL/K/5777–12

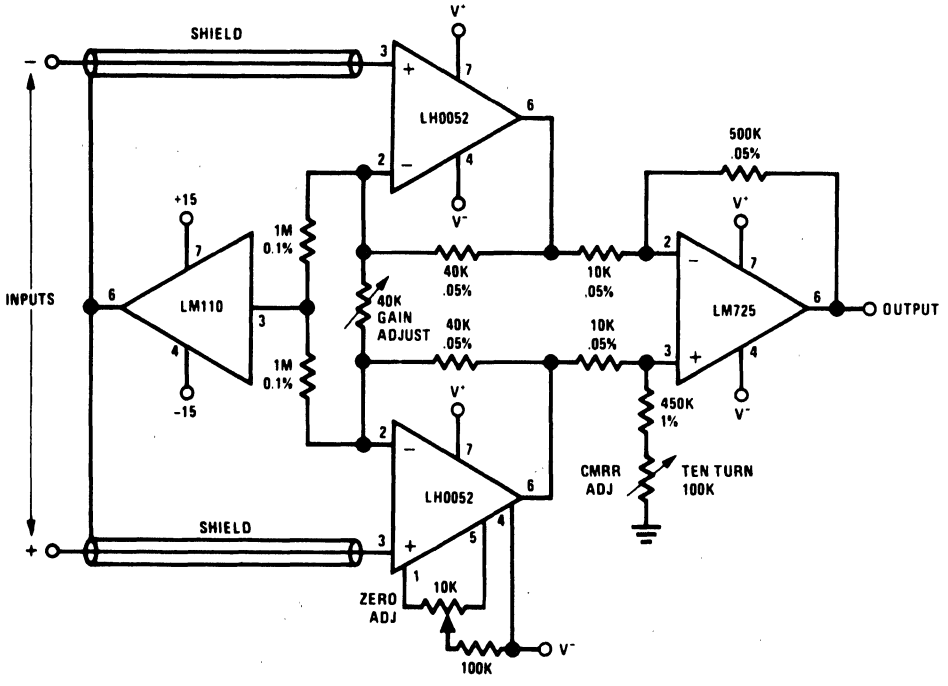
Ultra Low Level Current Source



TL/K/5557–13

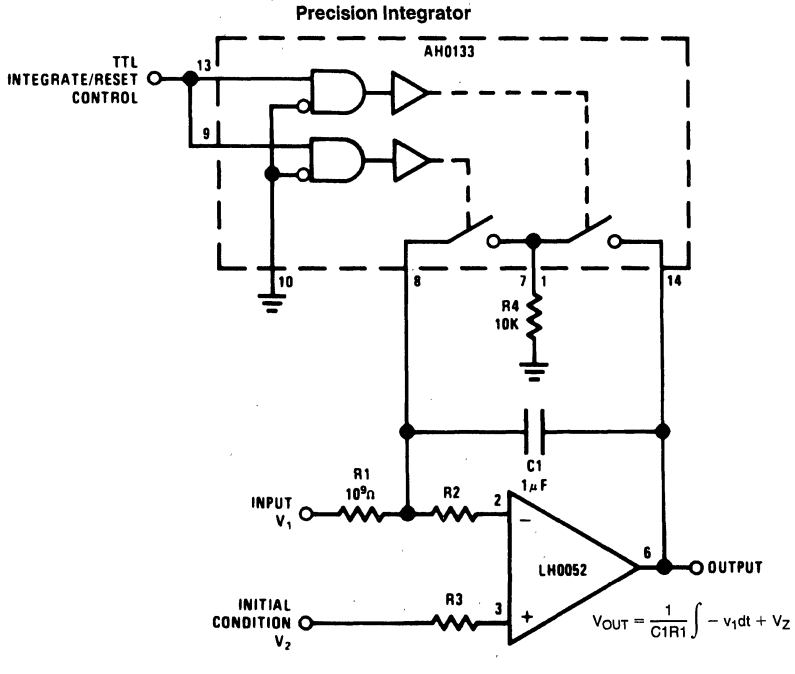
Typical Applications (Continued)

True Instrumentation Amplifier



TL/K/5557–14

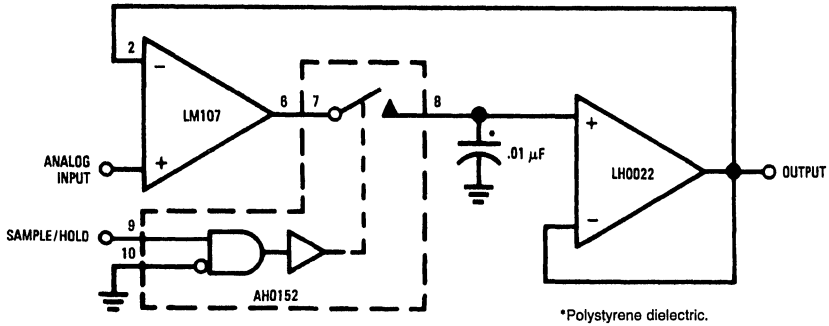
Precision Integrator



TL/K/5557–15

Typical Applications (Continued)

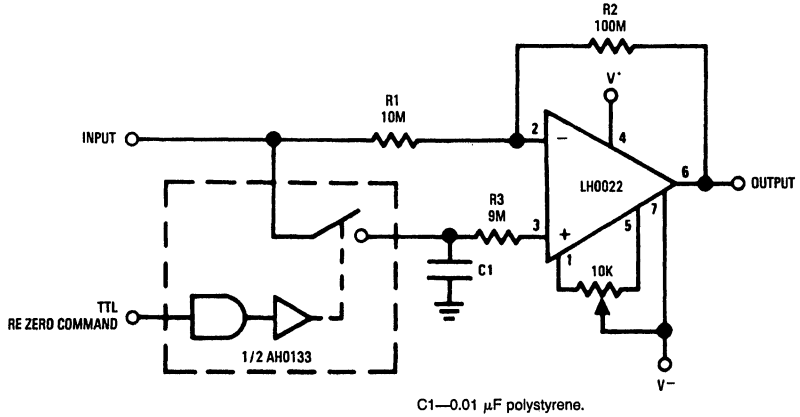
Precision Sample and Hold



*Polystyrene dielectric.

TL/K/5557–16

Re-Zeroing Amplifier

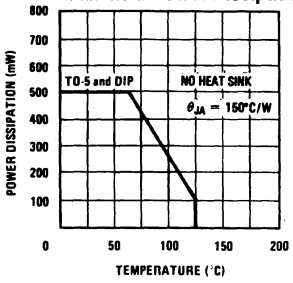


C1—0.01 μF polystyrene.

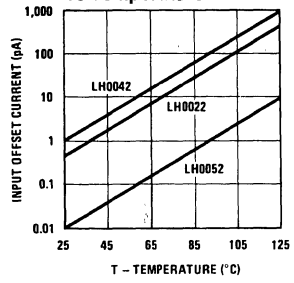
TL/K/5557–17

Typical Performance Characteristics

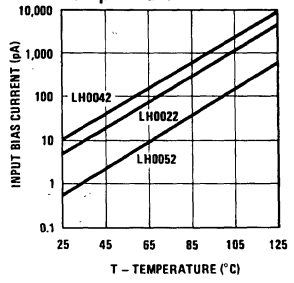
Maximum Power Dissipation



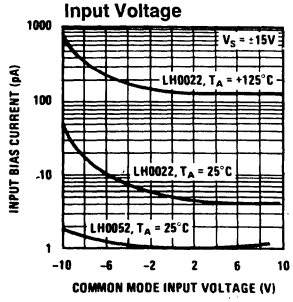
Input Offset Current vs Temperature



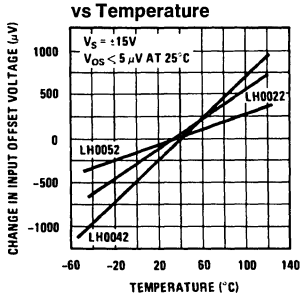
Input Bias Current vs Temperature



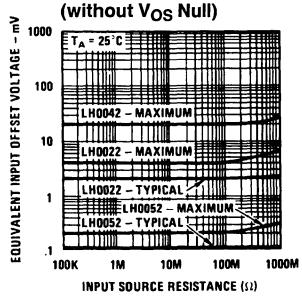
Input Bias Current vs Input Voltage



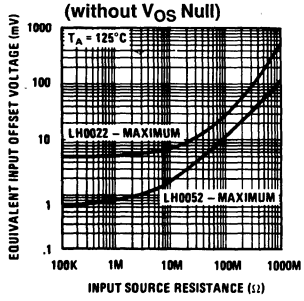
Input Offset Voltage vs Temperature



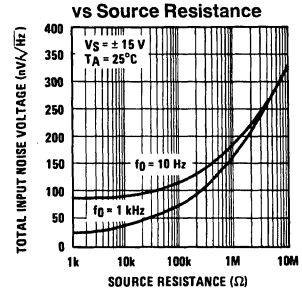
Offset Error (without V_{OS} Null)



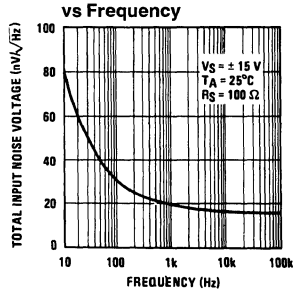
Offset Error (without V_{OS} Null)



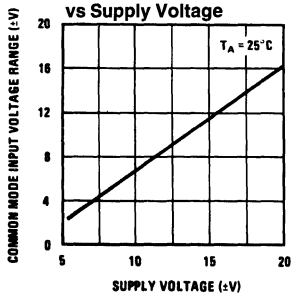
Total Input Noise Voltage* vs Source Resistance



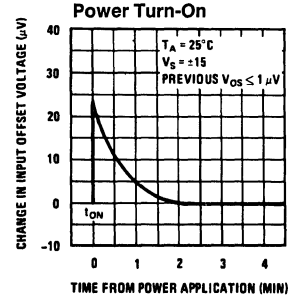
Total Input Noise Voltage* vs Frequency



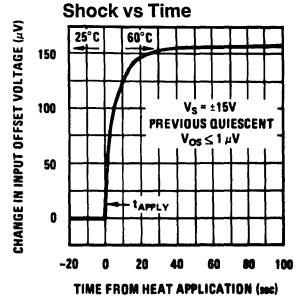
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



Change in Input Offset Voltage Due to Thermal Shock vs Time

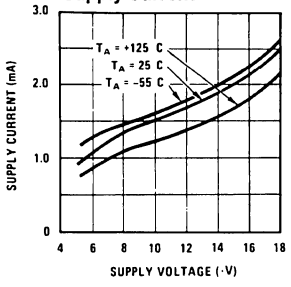


TL/K/5557–18

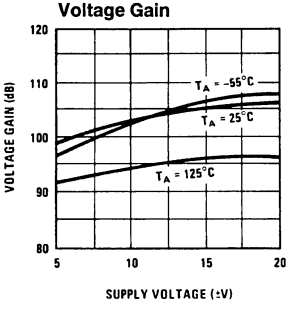
*Noise voltage includes contribution from source resistance.

Typical Performance Characteristics (Continued)

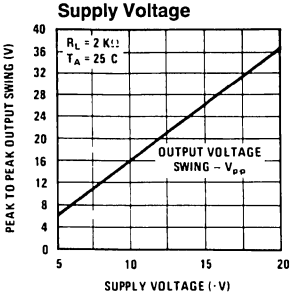
Supply Voltage vs Supply Current



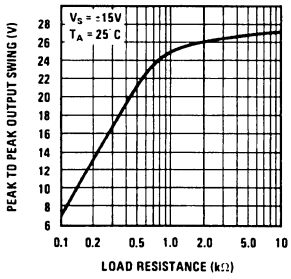
Voltage Gain



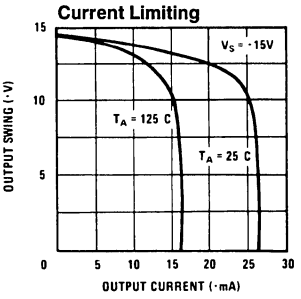
Output Swing vs Supply Voltage



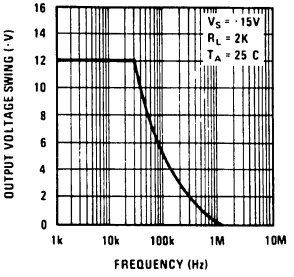
Output Voltage Swing vs Load Resistance



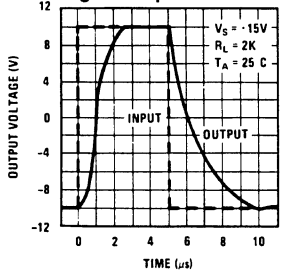
Current Limiting



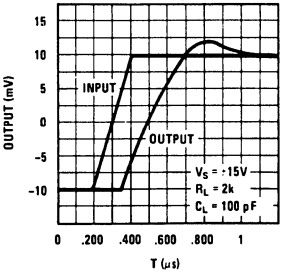
Output Voltage Swing vs Frequency



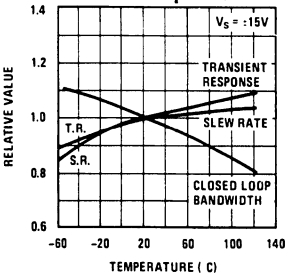
Voltage Follower Large Signal Response



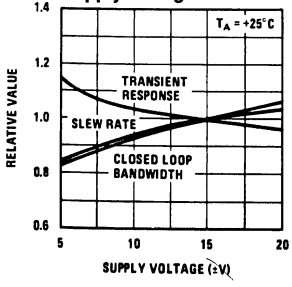
Transient Response



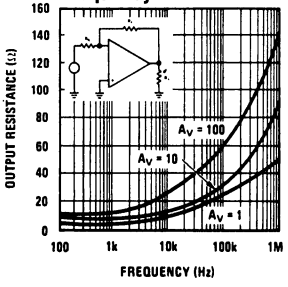
Frequency Characteristics vs Ambient Temperature



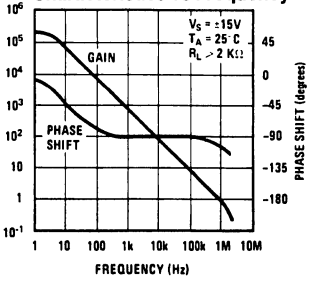
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



TL/K/5557–19

3

National Semiconductor

LH0024/LH0024C High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

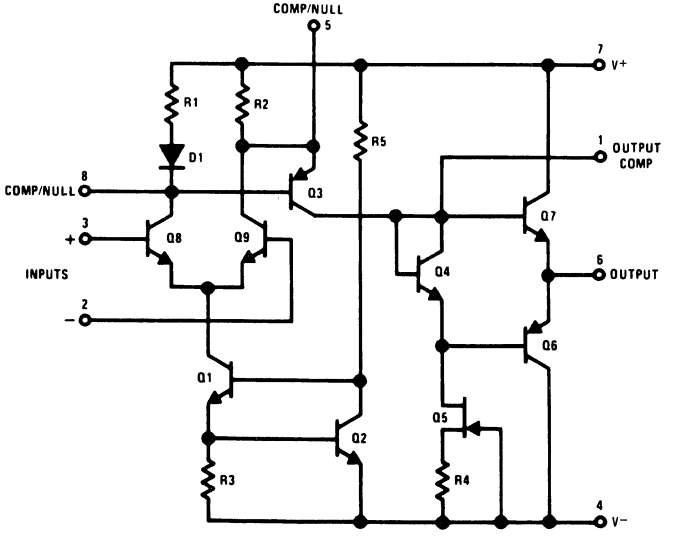
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range −55°C to +125°C, whereas the LH0024C is guaranteed −25°C to +85°C.

Features

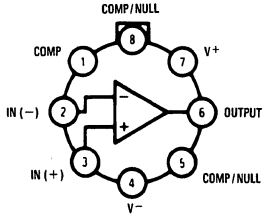
- Very high slew rate—500 V/μs at $A_V = +1$
- Wide small signal bandwidth—70 MHz
- Wide large signal bandwidth—15 MHz
- High output swing—±12V into 1k
- Offset null with single pot
- Low input offset—2 mV
- Pin compatible with standard IC op amps

Schematic and Connection Diagrams



TL/K/5552–1

Metal Can Package



TL/K/5552–2

Top View

Note: For heat sink use Thermalloy 2230-5 series.

Order Number LH0024H or LH0024CH
See NS Package Number H08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±18V
Input Voltage	Equal to Supply
Differential Input Voltage	±5V
Power Dissipation	600 mW

Operating Temperature Range	
LH0024	−55°C to +125°C
LH0024C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 1)

Parameter	Conditions	LH0024			LH0024C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ $R_S = 50\Omega$		2.0	4.0 6.0		5.0	8.0 10.0	mV mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 50\Omega$ −55°C to 125°C		−20			−25		µV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0 10.0		4.0	15.0 20.0	µA µA
Input Bias Current	$T_A = 25°C$		15	30 40		18	40 50	µA µA
Supply Current			12.5	15		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm15V$, $R_L = 1k$	4 3	5		3 2.5	4		V/mV V/mV
Input Voltage Range	$V_S = \pm15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm15V$, $R_L = 1k$	±12 ±10	±13		±10 ±10	±13		V V
Slew Rate	$V_S = \pm15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF, $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/µs
Common-Mode Rejection Ratio	$V_S = \pm15V$, $\Delta V_{IN} = \pm10V$, $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm5V \le V_S \le \pm18V$, $R_S = 50\Omega$		60			60		dB

Note 1: These specifications apply for $V_S = \pm15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

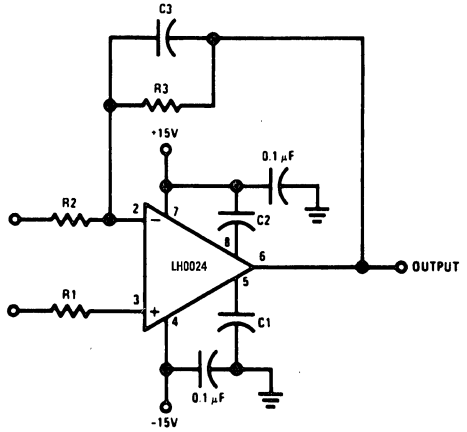
Note 2: Refer to RETS0024H for LH0024H military specifications.

Frequency Compensation

TABLE I

Closed Loop Gain	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

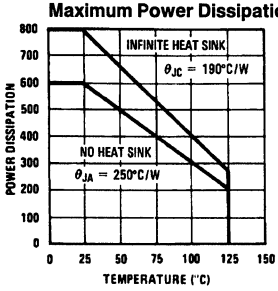
Frequency Compensation Circuit



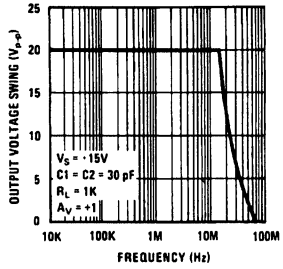
TL/K/5552–6

Typical Performance Characteristics

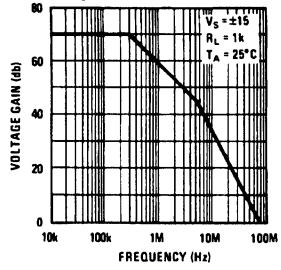
Maximum Power Dissipation



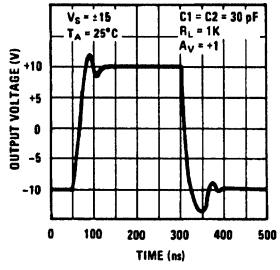
Large Signal Frequency Response



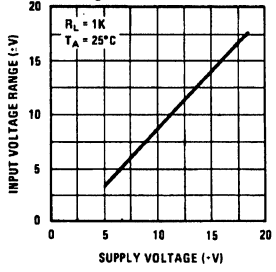
Open Loop Frequency Response



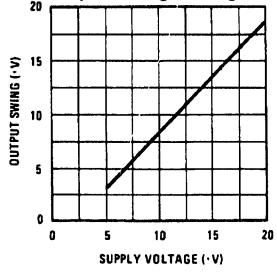
Voltage Follower Pulse Response



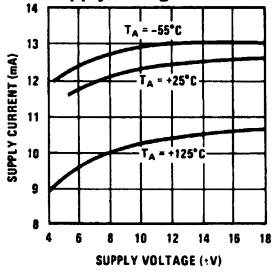
Input Voltage vs Supply Voltage



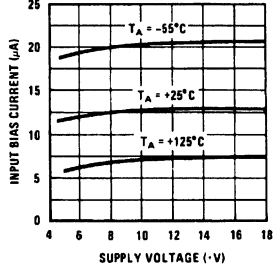
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



TL/K/5552–7

Applications Information

LAYOUT CONSIDERATIONS

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least 0.01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1 kΩ.

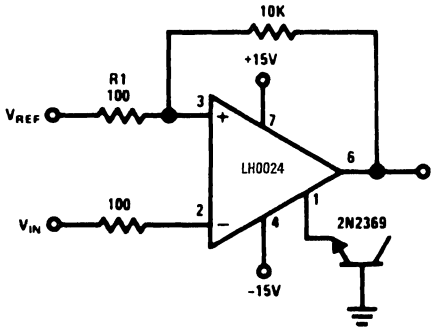
The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

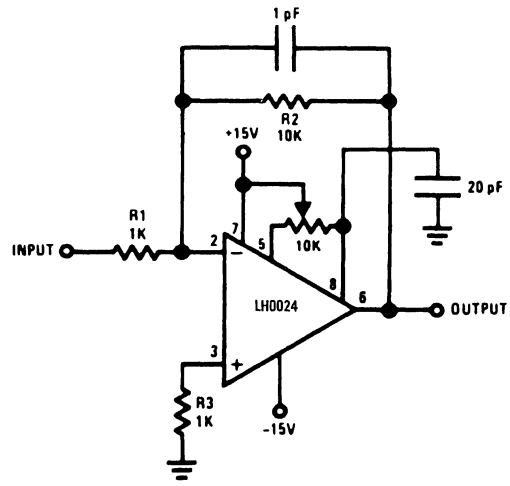
Typical Applications

TTL Compatible Comparator



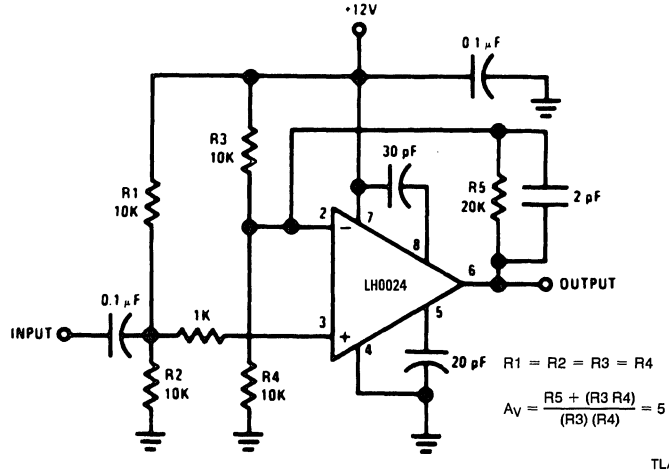
TL/K/5552–3

Offset Null



TL/K/5552–4

Video Amplifier



$R1 = R2 = R3 = R4$

$$A_V = \frac{R5 + (R3\,R4)}{(R3)\,(R4)} = 5$$

TL/K/5552–5

National Semiconductor

LH0032/LH0032A/LH0032C/LH0032AC
Ultra Fast FET-Input Operational Amplifier

General Description

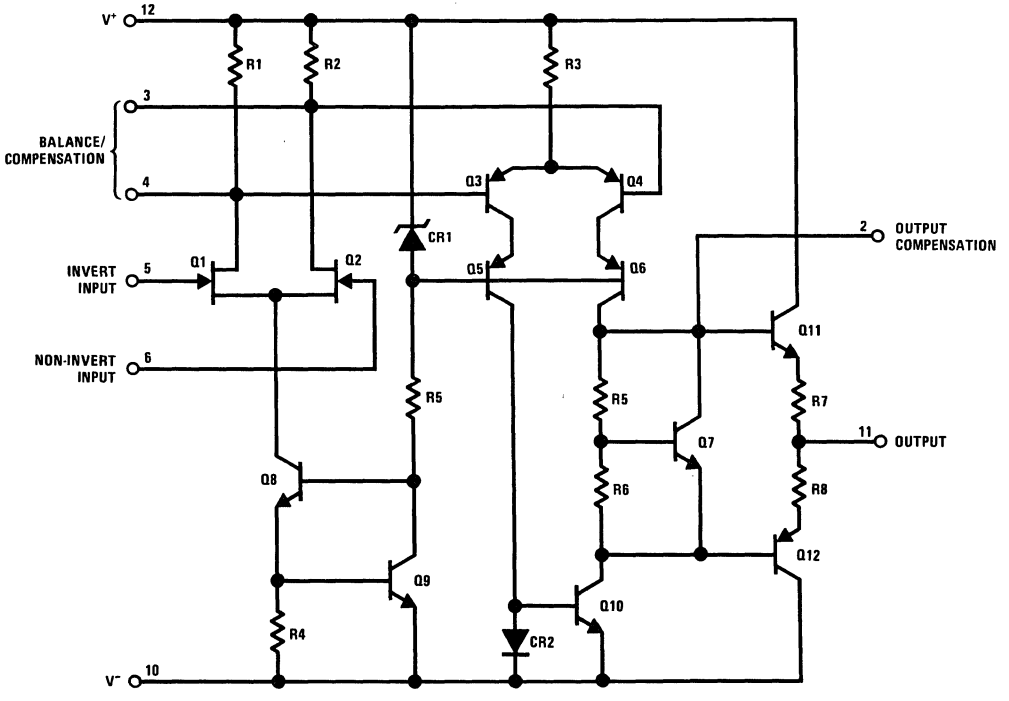
The LH0032/LH0032A is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 and LH0032A are guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C and LH0032AC are guaranteed for −25°C to +85°C.

Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

Block Diagram



TL/K/5265–1

Absolute Maximum Ratings

Supply Voltage, V_S	±18V	Operating Temperature Range, T_A	
Input Voltage, V_{IN}	$\pm V_S$	LH0032G/AG/E	−55°C to +125°C
Differential Input Voltage	±30V or $\pm 2V_S$	LH0032CG/ACG	−25°C to +85°C
Power Dissipation, P_D		Operating Junction Temperature, T_J	175°C
T_A = 25°C	1.5W, derate 100°C/W to 125°C (Note 1)	Storage Temperature Range	−65°C to +150°C
T_C = 25°C	2.2W, derate 70°C/W to 125°C (Note 1)	Lead Temp. (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_j$)

Symbol	Parameter	Test Conditions		LH0032A			LH0032AC			LH0032			LH0032C			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$V_{IN}=0$	$T_A=T_J=25°C$ (Note 3)		1	2 5		2	5 7		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift		(Note 4)		15	30		15	30		15	50		15	50	µV/°C
I_{OS}	Input Offset Current		$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5)			10 250 10			30 500 3			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5)			50 1 25			150 5 10			100 1 50			500 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN}=\pm 10V$		50	60		50	60		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O=\pm 10V$, f=1 kHz R_L = 1 kΩ (Note 6)	$T_J=25°C$	60	70		60	70		60	70		60	70		dB
				57			57			57			57			
V_O	Output Voltage Swing	R_L = 1 kΩ		±10	±13.5		±10	±13		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_A=25°C$, $I_O=0$ (Note 5)			18	20		20	22		18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S=10V$ (±5 to ±15V)		50	60		50	60		50	60		50	60		dB

AC Electrical Characteristics

V_S = ±15V, R_L = 1kΩ, T_J = 25°C (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	A_V = +1	ΔV_{IN} = 20V	350	500		V/µs
t_s	Settling Time to 1% of Final Value	A_V = −1,			100		
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V			8	20	
t_D	Small Signal Delay Time				10	25	

Note 1. In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2. LH0032AG/G are 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032ACG/CG are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3. Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25 C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4. LH0032AG/G are 100% production tested for this parameter. LH0032ACG/CG are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

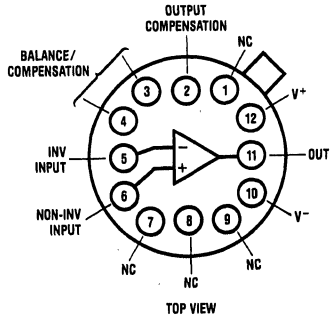
Note 5. Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 6. Guaranteed thru correlated automatic pulse testing at T_J = 25°C.

Note 7. Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

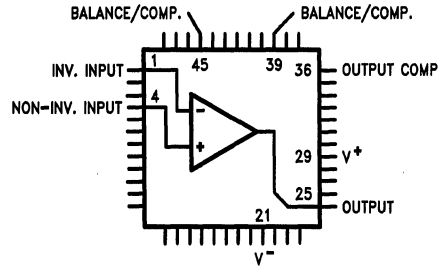
*Guaranteed by CMRR test condition.

Connection Diagrams



TL/K/5265-23

Order Number LH0032G, LH0032AG, LH0032CG or LH0032ACG
See NS Package Number G12B

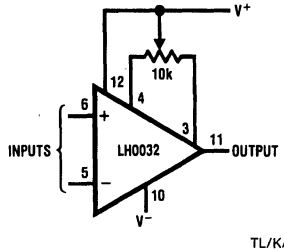


TL/K/5265-25

Order Number LH0032E
See NS Package Number E48B

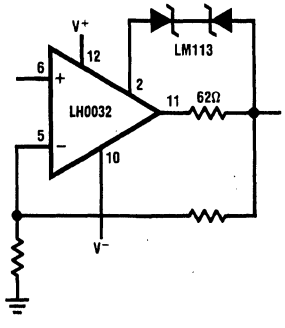
Auxiliary Circuits

Offset Null



TL/K/5265-15

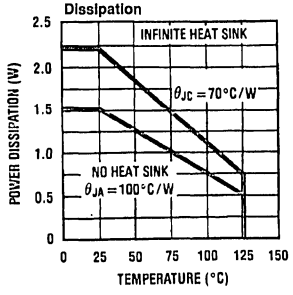
Output Short Circuit Protection



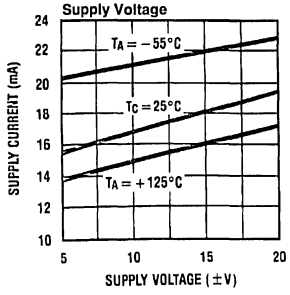
TL/K/5265-16

Typical Performance Characteristics

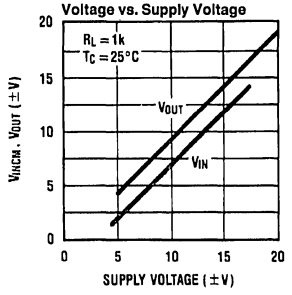
Maximum Power Dissipation



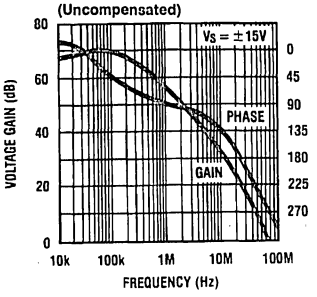
Supply Current vs. Supply Voltage



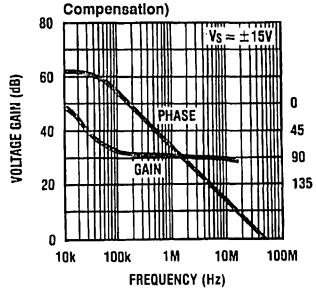
Input Voltage Range and Output Voltage vs. Supply Voltage



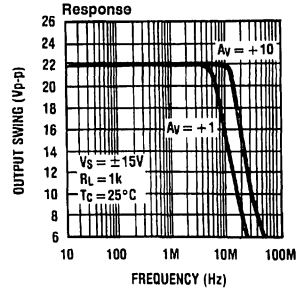
Bode Plot (Uncompensated)



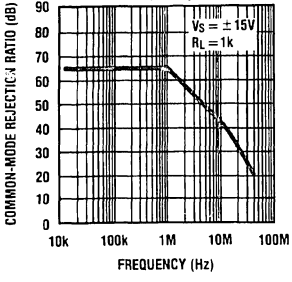
Bode Plot (Unity Gain Compensation)



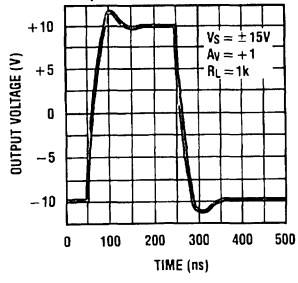
Large Signal Frequency Response



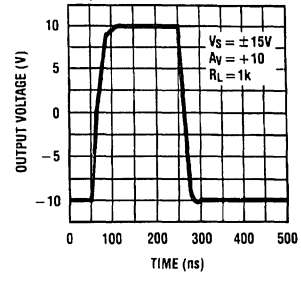
Common Mode Rejection Ratio vs. Frequency



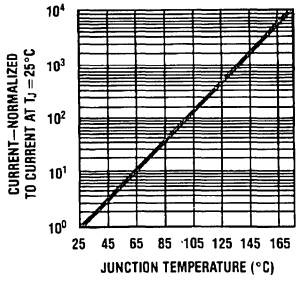
Large Signal Pulse Response



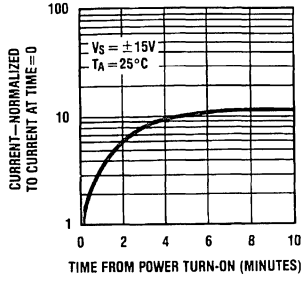
Large Signal Pulse Response



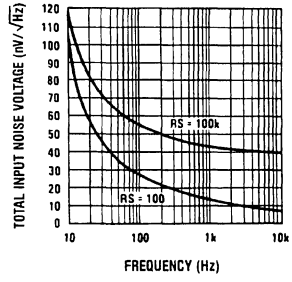
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Total Input Noise Voltage vs. Frequency*

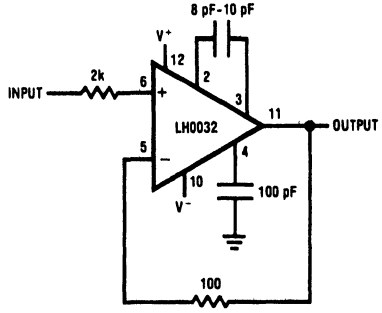


TL/K/5265–2

*Noise voltage includes contribution from source resistance.

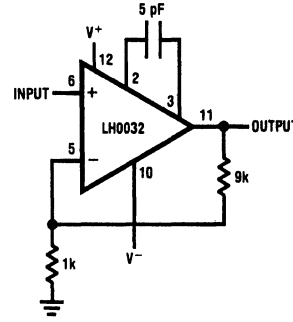
Typical Applications

Unity Gain Amplifier



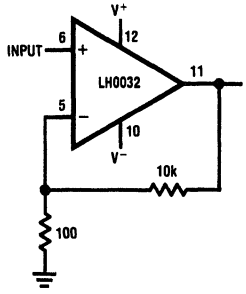
TL/K/5265–17

10X Buffer Amplifier



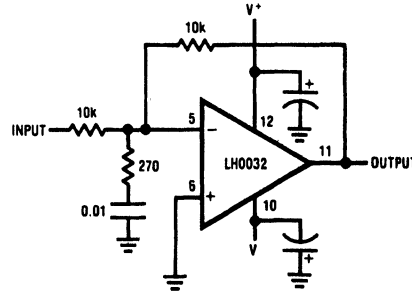
TL/K/5265–18

100X Buffer Amplifier



TL/K/5265–19

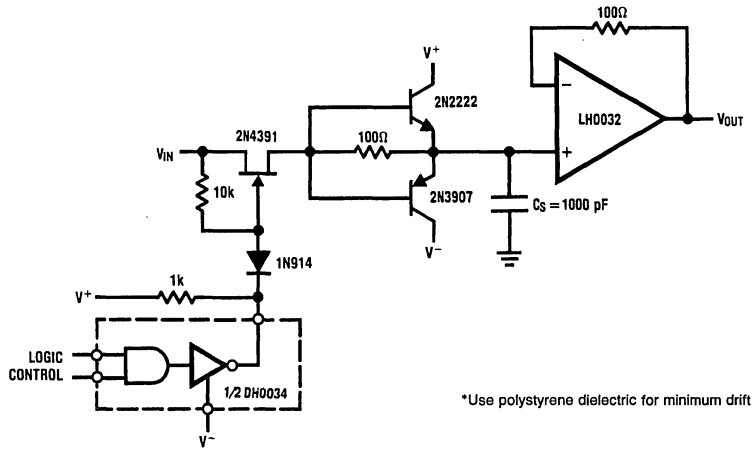
Non-Compensated Unity Gain Inverter



TL/K/5265–20

Typical Applications (Continued)

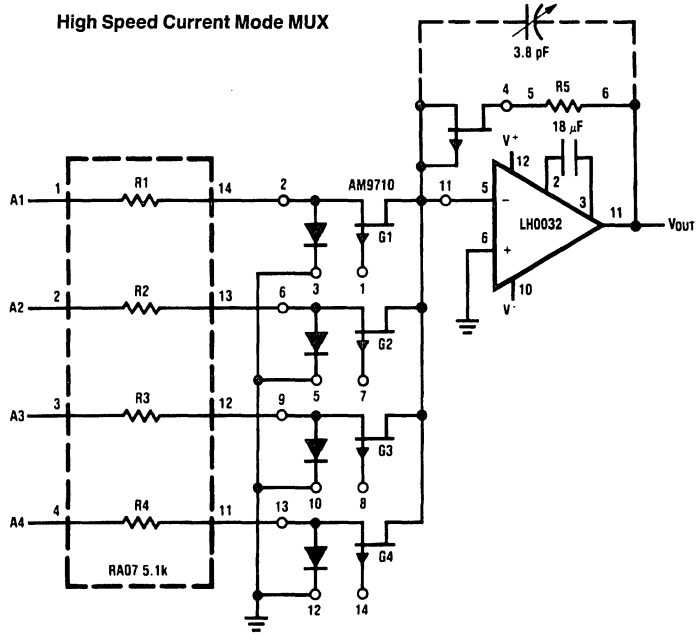
High Speed Sample and Hold



*Use polystyrene dielectric for minimum drift

TL/K/5265–21

High Speed Current Mode MUX



TL/K/5265–22

Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

National Semiconductor

LH0044 Series Precision Low Noise Operational Amplifiers

General Description

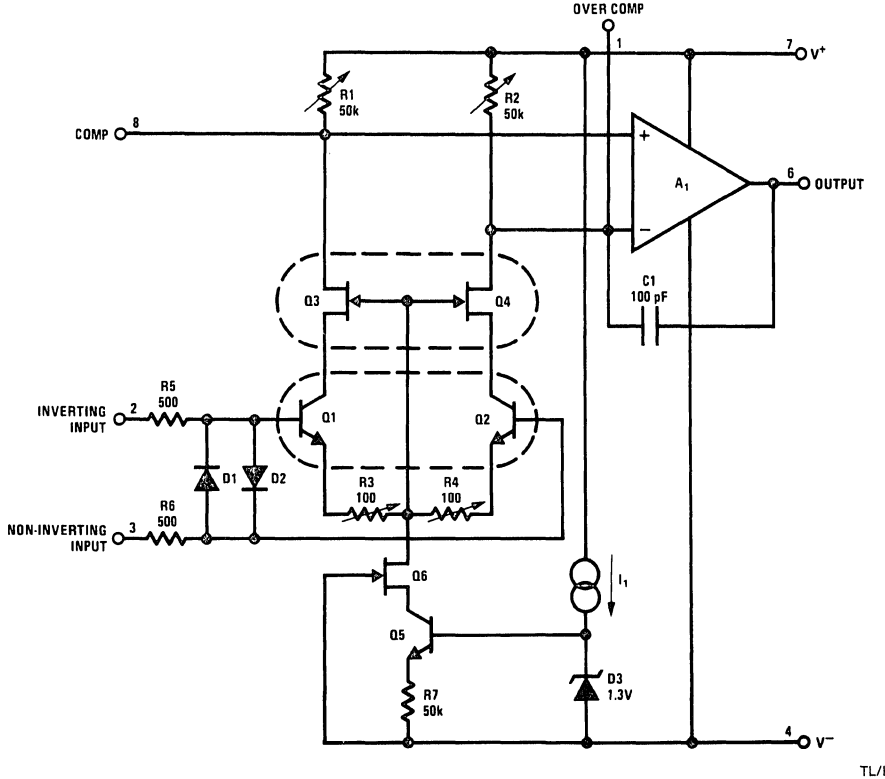
The LH0044 Series is a low noise, ultra-stable, high gain, precision operational amplifier family intended to replace either chopper-stabilized monolithic or modular amplifiers. The devices are particularly suited for differential mode, inverting, and non-inverting mode applications requiring very low initial offset, low offset drift, very high gain, high CMRR, and high PSRR. In addition, the LH0044 Series' low initial offset and offset drift eliminate costly and time consuming null adjustments at the systems level. The superior performance afforded by the LH0044 Series is made possible by advanced processing and testing techniques, as well as active laser trim of critical metal film resistors to minimize offset voltage and drift. Unique construction eliminates thermal feedback effects.

The LH0044 Series is an excellent choice for a wide range of precision applications including strain gauge bridges, thermocouple amplifiers, and ultrastable reference amplifiers. The LH0044 is guaranteed over the temperature range of −55°C to +125°C, and the LH0044AC, LH0044B, and LH0044C are guaranteed from −25°C to +85°C. The device is available in standard TO-5 op amp pin out and is compatible with LM108A, LM725, and LM741 type amplifiers.

Features

Low input offset voltage	25μV max
Excellent long-term stability	±1μV/month max
Low offset drift	0.5μV/°C max
Very low noise	0.7μVp-p max 0.1 Hz to 10 Hz
High CMRR and PSRR	120 dB min
High open loop gain	120 dB min
Wide common-mode range	±13V min
Wide supply voltage range	±2V to ±20V

Equivalent Circuit



TL/K/5551–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±20V
Power Dissipation	600 mW
Differential Input Voltage (Note 4)	±1V
Input Voltage (Note 5)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH0044	−55°C to +125°C
LH0044AC, LH0044B, LH0044C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 1)

Parameter	Conditions	Limits						Units
		LH0044AC			LH0044/ LH0044B/LH0044C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A=25°C, R_S=50Ω, V_{CM}=0V LH0044C Only		8	25		12	50 100	μV μV
Input Offset Voltage	R_S = 50Ω, V_{CM} = 0V LH0044A and LH0044B Only			55 75			180 80	μV μV
Average Input Offset Voltage Drift	$T_{Min} \le T_A \le T_{Max}$ LH0044B Only		0.1	0.5		0.2	1.3 0.5	μV/°C μV/°C
Long-Term Stability	(Note 2)		0.2	1		0.3	2	μV/month
Input Noise Voltage (Note 3)	BW=0.1 Hz to 10 Hz, R_S=50Ω R_S= 10 kΩ Imbalance		0.35 0.50	0.7 0.9		0.35 0.50	0.8 1.0	μVp-p μVp-p
Thermal Feedback Coefficient			0.005			0.005		μV/mW
Open Loop Voltage Gain	R_L = 10 kΩ	120	145		114	140		dB
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	120	145		114	140		dB
Power Supply Rejection Ratio	$\pm 3V \le V_S \le \pm 18V$	120	145		114	140		dB
Input Voltage Range		±13	±13.8		±12	±13.5		V
Output Voltage Swing	R_L = 10 kΩ	±13	±13.7		±12	±13.5		V
Input Offset Current	25°C ≤ $T_A \le T_{Max}$ $T_{Min} \le T_A$ < 25°C		1.0	2.5 5.0		1.5	5.0 10.0	nA nA
Average Input Offset Current Drift			5	40		15	80	pA/°C
Input Bias Current	25°C ≤ $T_A \le T_{Max}$ $T_{Min} \le T_A$ < 25°C		8.5	15 50		10	30 100	nA nA
Average Input Bias Current Drift			50	300		100	600	pA/°C
Differential Input Impedance		5	10		2.5	8		MΩ
Common Mode Input Impedance			2×10^{11}			2×10^{11}		Ω
Supply Current	I_L = 0		0.9	3.0		1.0	4.0	mA
Power Dissipation			27	90		30	120	mW

AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Parameter	Conditions	Typ	Units
Input Noise Voltage	$R_S = 1\ k\Omega, f_O = 10\ Hz$ $R_S = 1\ k\Omega, f_O = 1\ kHz$	11 9	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Slew Rate	$A_V = +1, R_L = 10\ k\Omega, V_{IN} = \pm 10V$	0.06	$V/\mu s$
Large Signal Bandwidth	$A_V = +1, R_L = 10\ k\Omega, V_{IN} = \pm 10V$	1	kHz
Overload Recovery Time	$A_V = +100, V_{IN} = -100\ mV, \Delta V_{IN} = 200\ mV$	5	μs
Small Signal Bandwidth	$A_V = +1, R_L = 10\ k\Omega$	400	kHz
Small Signal Rise Time	$A_V = +1, R_L = 10\ k\Omega, V_{IN} = 10\ mV$	2.5	μs
Overshoot	$A_V = +1, R_L = 10\ k\Omega, V_{IN} = 10\ mV, C_L = 100\ pF$	10	%

Note 1: All specifications apply for all device grades, at $V_S = \pm 15V$, and from T_{Min} to T_{Max} unless otherwise specified. T_{Min} is $-55°C$ and T_{Max} is $+125°C$ for the LH0044. T_{Min} is $-25°C$ and T_{Max} is $+85°C$ for the LH0044AC, LH0044B and LH0044C. Typicals are given for $T_A = 25°C$.

Note 2: This parameter is not 100% tested; however, 90% of the devices are guaranteed to meet this specification after one month of operation and after initial turn-on stabilization.

Note 3: Noise is 100% tested on the LH0044AC and LH0044B only. 90% of the LH0044 and LH0044C devices are guaranteed to meet this specification.

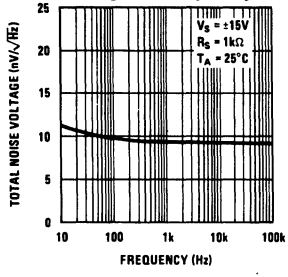
Note 4: The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow for differential input voltages in excess of 1V. Input current should be limited to less than 1 mA.

Note 5: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

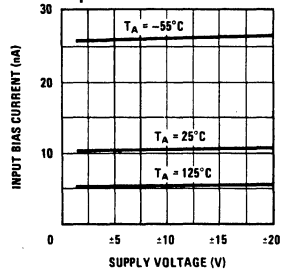
Note 6: Refer to RETS0044AH for LH0044AH military specifications and RETS0044H for LH0044H military specfifications.

Typical Performance Characteristics

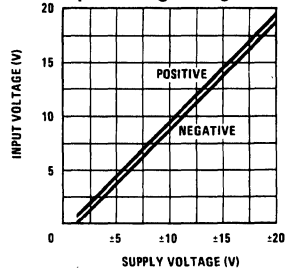
Total Input Noise Voltage vs Frequency



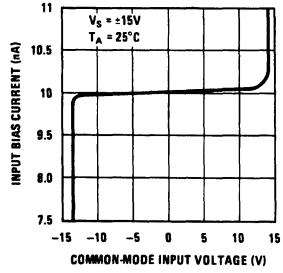
Input Bias Current



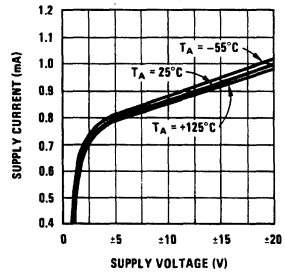
Input Voltage Range



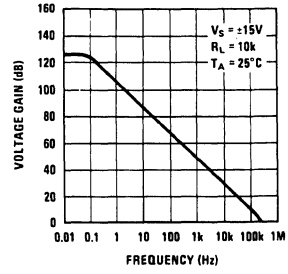
Input Bias Current vs Common-Mode Input Voltage



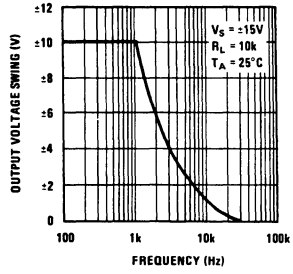
Supply Current vs Supply Voltage



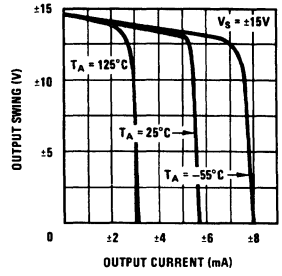
Open Loop Frequency Response



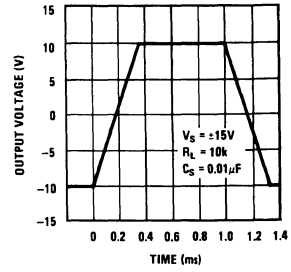
Large Signal Voltage Response



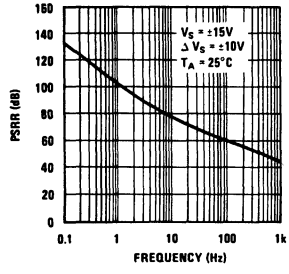
Output Swing



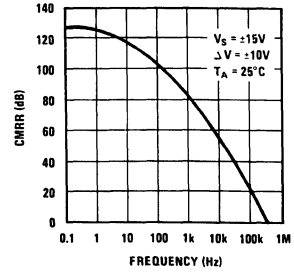
Large Signal Pulse Response



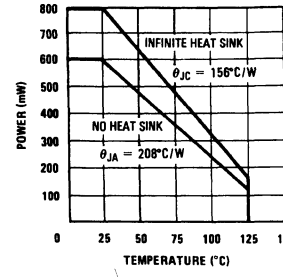
Power Supply Rejection Ratio vs Frequency



CMRR vs Frequency



Maximum Power Dissipation



TL/K/5551–3

Applications Information

LOW DRIFT CONSIDERATIONS

Achieving ultra-low drift in practical applications requires strict attention to board layout, thermocouple effects, and input guarding. For specific recommendations refer to AN-63 and AN-79.

A point worth stressing with regard to low drift specifications is testing of the LH0044. Simply stated—it is virtually impossible to test the device using a thermoprobe or other form of local heating. A one degree centigrade temperature gradient can account for tens of microvolts of virtual offset (or drift). The test circuit of *Figure 1* is recommended for use in a stabilized oven or continuously stirred oil bath with the entire circuit inside the oven or bath. Isothermal layout of the resistors is advised in order to minimize thermocouple induced EMF's.

OVER COMPENSATION

The LH0044 may be overcompensated in order to minimize noise bandwidth by paralleling the internal 100 pF capacitor with an external capacitor connected between pins 1 and 6. Unity gain frequency may be predicted by:

$$f = \frac{4 \times 10^{-5}}{100\ \text{pF} + C_{ext}\ \text{pF}}\ (\text{Hz})$$

COMPENSATION

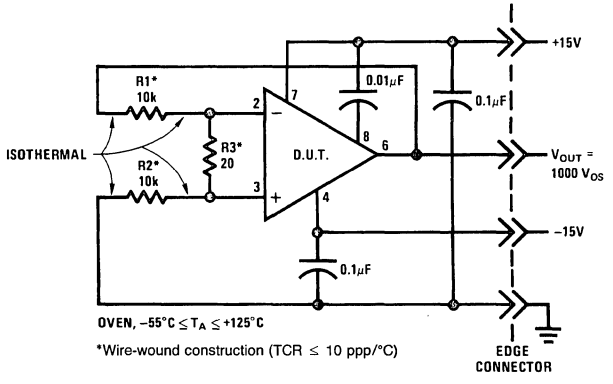
For closed loop gains in excess of 10, no external components are required for frequency stability. However, for gains of 10 or less, a 0.01μF disc capacitor is recommended between pin 7 (V^+) and pin 8 (Comp). An improvement in ac PSRR will also be realized by use of the 0.01μF capacitor.

OFFSET NULL

In general, further nulling of LH0044 is neither necessary nor recommended. For most applications the specified initial offset is sufficient.

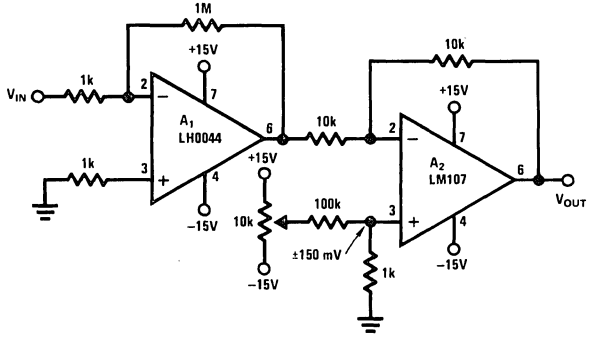
However, for those applications requiring additional null, an obvious temptation might be to place a pot between pins 1 and 8 with the wiper returned to V^+. This technique will usually result in reduced gain and increased offset drift due to mismatch in the TCR of the pot and R1 and R2. The technique is, therefore, not generally recommended.

The recommended technique for offset nulling the LH0044 is shown in *Figure 2*. Null is accomplished in A_2 and all errors are divided by the closed loop gain of the LH0044. Additional offset and drift incurred due to the use of A_2 is less than 1μV/V for V^+ and V^- changes and 0.01μV/°C drift for the values shown in *Figure 2*.



TL/K/5551–4

FIGURE 1. LH0044 Temperature Test Circuit

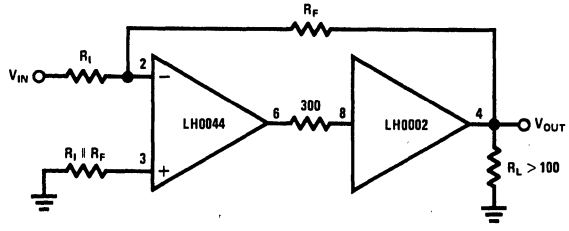


TL/K/5551–5

FIGURE 2. LH0044 Null Technique

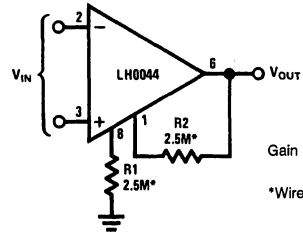
Typical Applications

Buffered Output for Heavy Loads



TL/K/5551–6

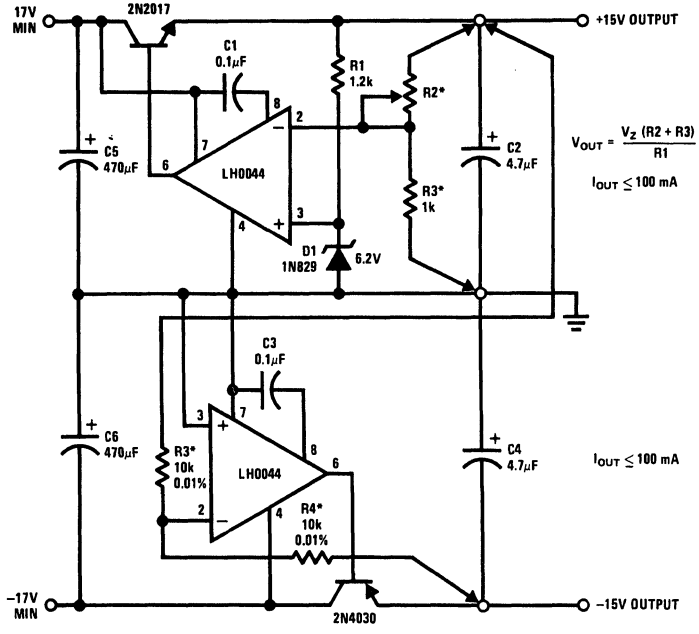
X1000 Instrumentation Amp



Gain = $g_m R_L$
$\geq 0.2 \times 10^3$ (R1 + R2) for $V_{IN} \leq 10$ mV
*Wire-wound resistors

TL/K/5551–7

Precision Dual Tracking Regulator

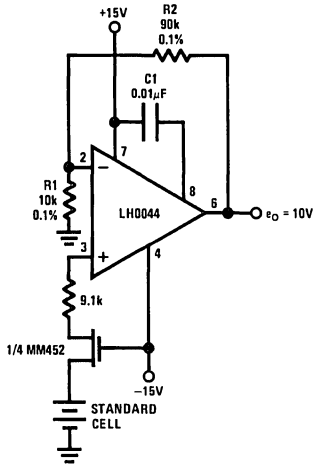


TL/K/5551–8

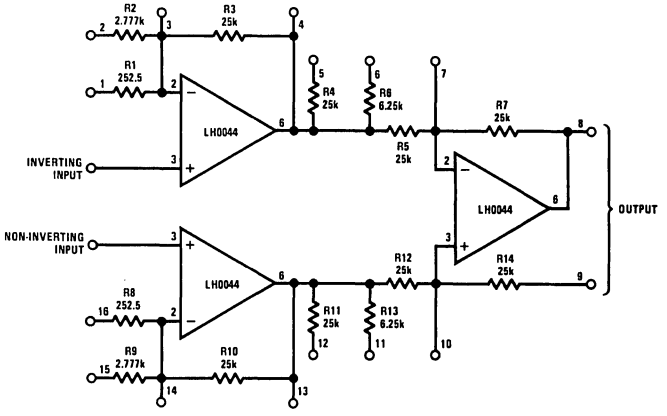
*Wire-wound for minimum drift.
Line and load regulation ≤ 0.005%

Typical Applications (Continued)

10V Reference Supply



TL/K/5551–9

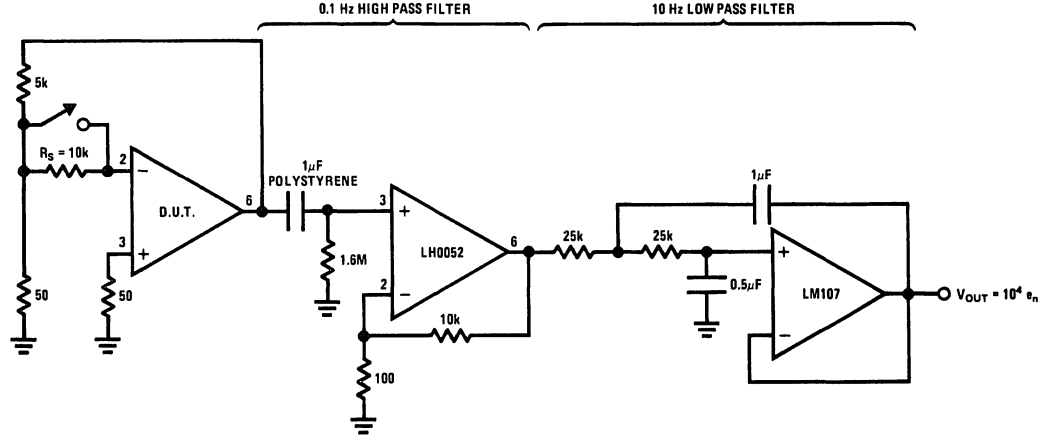


TL/K/5551–10

Precision Instrumentation Amplifier

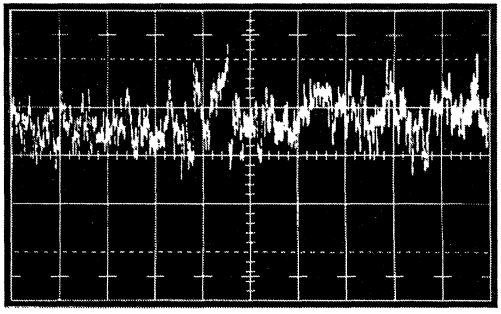
Overall Gain	Input Stage Gain	Output Stage Gain
X1	X1	X1
X2	X1	X2
X5	X1	X5
X10	X10	X1
X20	X10	X2
X50	X10	X5
X100	X100	X1
X200	X100	X2
X500	X100	X5
X995	X199	X5

Noise Test Circuit



TL/K/5551–11

Noise Test Circuit (Continued)

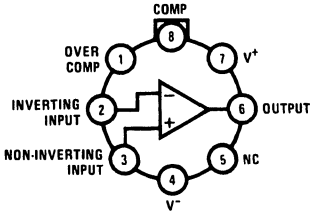


VERT: 200 nV/DIV
HORIZ: 5 SEC/DIV

TL/K/5551–12

Connection Diagram

Metal Can Package



TL/K/5551–2

Top View

Case is electrically isolated

Note: Compensation is not normally required. However, for maximum stability, a 0.01μF capacitor should be placed between pins 7 and 8 when device is used below closed loop gains of 10.

Order Number LH0044H, LH0044CH, LH0044ACH or LH0044BH
See NS Package Number H08B

National Semiconductor

LH0045/LH0045C Two Wire Transmitter

General Description

The LH0045/LH0045C Two Wire Transmitters are linear integrated circuits designed to convert the voltage from a sensor to a current, and send it through to a receiver, utilizing the same simple twisted pair as the supply voltage.

The LH0045 and LH0045C contain an internal reference designed to power the sensor bridge, a sensitive input amplifier, and an output current source. The output current scale can be adjusted to match the industry standards of 4.0 mA to 20 mA or 10 mA to 50 mA.

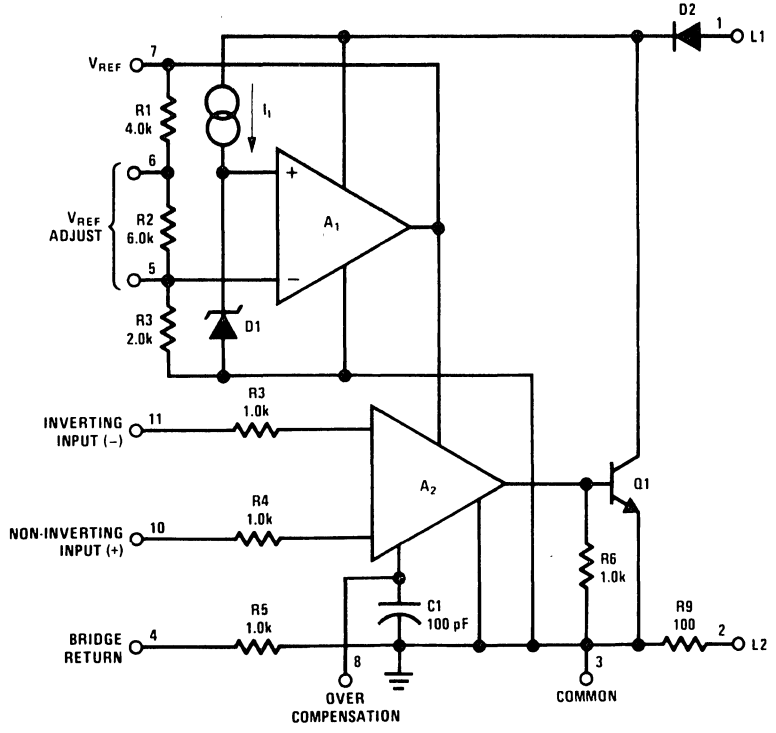
Designed for use with various sensors, the LH0045/LH0045C will interface with thermocouples, strain gauges, or thermistors. The use of the power supply leads as the signal output eliminates two or three extra wires in remote signal applications. Also, current output minimizes susceptibility to voltage noise spikes and eliminates line drop problems.

The LH0045/LH0045C is intended to fulfill a wide variety of process control, instrumentation, and data acquisition applications. The LH0045 is guaranteed over the temperature range of −55°C to +125°C; whereas the LH0045C is guaranteed from −25°C to +85°C.

Features

■ High sensitivity	> 10 μA/μV
■ Low input offset voltage	1.0 mV
■ Low input bias current	2.0 nA
■ Single supply operation	10V to 50V
■ Programmable bridge reference (LH0045G)	5.0V to 30V
■ Non-interactive span and null adjust	
■ Over compensation capability	
■ Supply reversal protection	

Equivalent Schematic



*Note: Pins shown are for the 12 pin to 8 ("G") package.

TL/K/5556–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage (L1 to common)	+50V
Input Current	+20 mA
Input Voltage (Either Input to Common)	0V to V_{REF}
Differential Input Voltage	±20V
Output Current (Either L1 or L2)	50 mA
Reference Output Current	5.0 mA
Power Dissipation	
LH0045G	1.5W
Operating Temperature Range	
LH0045	−55°C to +125°C
LH0045C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

Parameter	Conditions	Limits						Units
		LH0045			LH0045C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})	I_S = 4.0 mA, T_A = 25°C I_S = 4.0 mA		0.7	2.0 3.0		2.0	7.5 10	mV mV
Offset Voltage Temperature Coefficient ($\Delta V_{OS}/\Delta T$)	I_S = 4.0 mA		3.0			6.0		µV/°C
Input Bias Current (I_B)	T_A = 25°C		0.8	2.0 3.0		1.5	7.0 10	nA nA
Input Offset Current (I_{OS})	T_A = 25°C		0.05	0.2 0.4		0.2	1.0 1.5	nA nA
Open Loop Transconductance (g_{MOL})	ΔI_S = 4.0 mA to 20 mA ΔI_S = 10 mA to 50 mA	10^6 2×10^6	10^7 2×10^7		10^6 2×10^6	10^7 2×10^7		µΩ µΩ
Supply Voltage Range (V_S)	LH0045G Pins 5 and 6 Open	9.0 15		50 50	9.0 15		50 50	V V
Input Voltage Range (V_{IN})	LH0045G Pins 5 and 6 Open	1.0 1.0		3.3 7.6	1.0 1.0		3.3 7.6	V V
Open Loop Output Impedance (R_{OUT})	V_S=10V to 45V, I_S=4.0 mA, T_A = 25°C		1.0			1.0		MΩ
Common Mode Rejection Ratio (CMRR)	ΔV_{IN} = 1.0V to 3.3V, I_S = 12 mA	0.1	0.05		0.1	0.05		mV/V
Power Supply Rejection Ratio (PSRR)	ΔV_S = 10V to 45V, I_S = 12 mA	0.1	0.01		0.1	0.01		mV/V
Open Loop Supply Current (I_{SOL})	V_S = 50V		2.0	3.0		2.0	3.0	mA
Reference Voltage Load Regulation ($\Delta V_{REF}/\Delta I_{REF}$)	ΔI_{REF} = 0 mA to 2.0 mA, T_A = 25°C,		0.05	0.2		0.05	0.2	%
Reference Voltage Line Regulation ($\Delta V_{REF}/\Delta V_S$)	ΔV_S = 10V to 45V, T_A = 25°C		0.3	0.5		0.3	0.7	mV/V
Reference Voltage Temperature Coefficient ($\Delta V_{REF}/\Delta T$)	I_{REF} = 2.0 mA		0.004			0.004		%/°C
Reference Voltage (V_{REF})	I_{REF} = 2.0 mA, T_A = 25°C I_{REF} = 2.0 mA, T_A = 25°C, LH0045G Pins 5 and 6 Open	4.3 8.6	5.1 10.3	5.9 12	4.3 8.6	5.1 10.3	5.9 12	V V

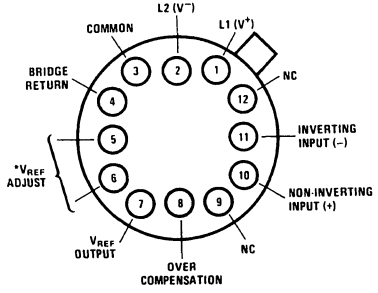
Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions	Limits						Units
		LH0045			LH0045C			
		Min	Typ	Max	Min	Typ	Max	
Resistor R9	I_S = 12 mA, T_A = 25°C	95	100	105	95	100	105	Ω
Average Temperature Coefficient of R9 (TCR_9)	I_S = 12 mA		50	300		50	300	PPM/°C
Resistor R5	I_S = 1.0 mA, T_A = 25°C	950	1000	1050	950	1000	1050	Ω
Average Temperature Coefficient of R5 (TCR_5)	I_S = 1.0 mA		50	300		50	300	PPM/°C
Input Resistance (R_{IN})	T_A = 25°C		50			50		MΩ

Note 1: Unless otherwise specified, these specifications apply for +10V ≤ V_S ≤ +50V, pin 5 shorted to pin 6 on the LH0045G, over the temperature range −55°C to +125°C for the LH0045 and −25°C to +85°C for the LH0045C.

Note 2: Refer to RETS 0045G for LH0045G military specifications.

Connection Diagram



TL/K/5556–2

Top View

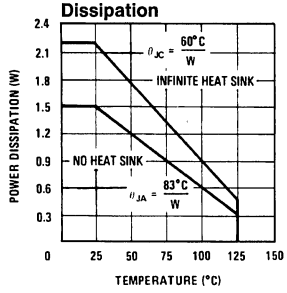
***Note:** Pin 5 is shorted to Pin 6 to obtain a Nominal +5.1V, V_{REF}. Left open V_{REF} = +10V.

The case is isolated from the circuit for both to 3 and to 8.

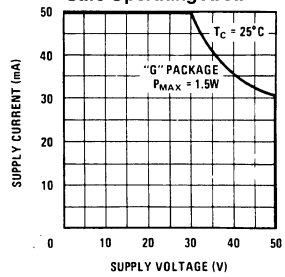
Order Number LH0045G or LH0045CG
See NS Package Number G12B

Typical Performance Characteristics

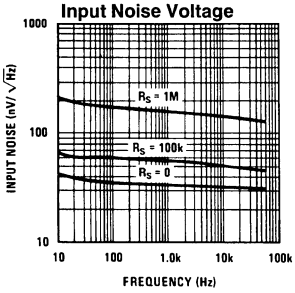
LH0045G Maximum Power Dissipation



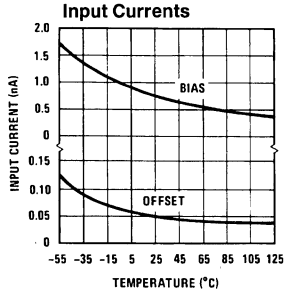
Safe Operating Area



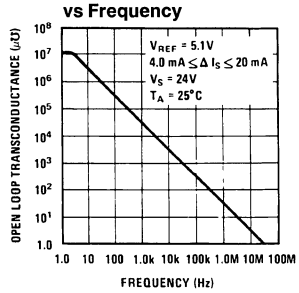
Input Noise Voltage



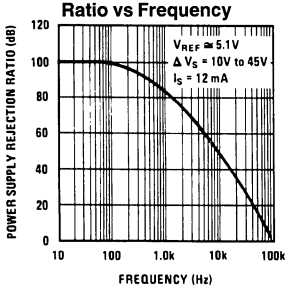
Input Currents



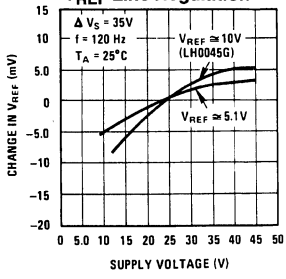
Open Loop Transconductance vs Frequency



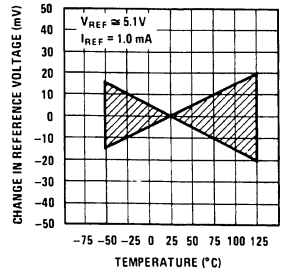
Power Supply Rejection Ratio vs Frequency



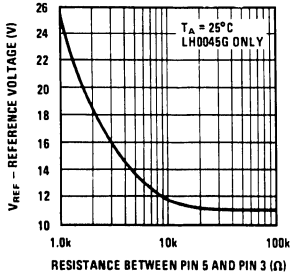
V_{REF} Line Regulation



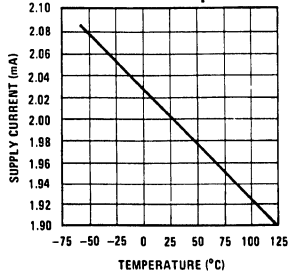
Variation of V_{REF} with Temperature Normalized to 25°C



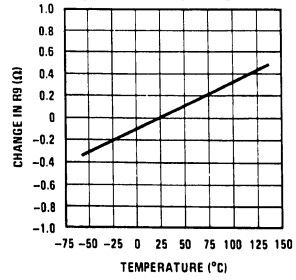
V_{REF} vs Resistance Between Pin 5 and Pin 3



Open Loop Supply Current vs Temperature



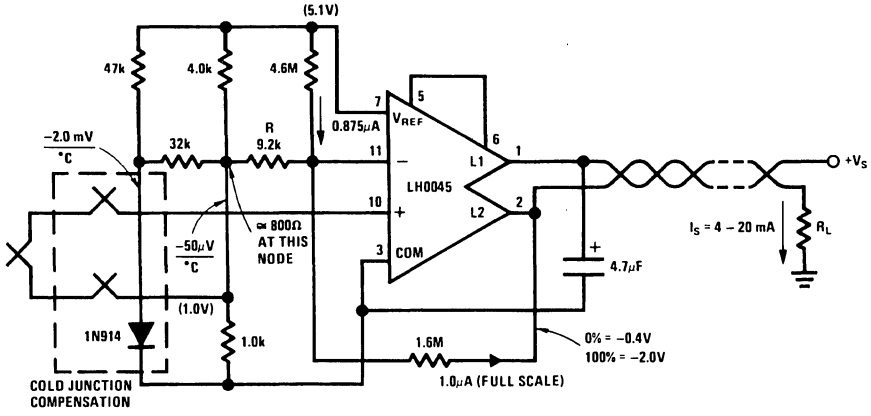
Change in R9 with Temperature Normalized to 25°C



TL/K/5556–3

Typical Applications

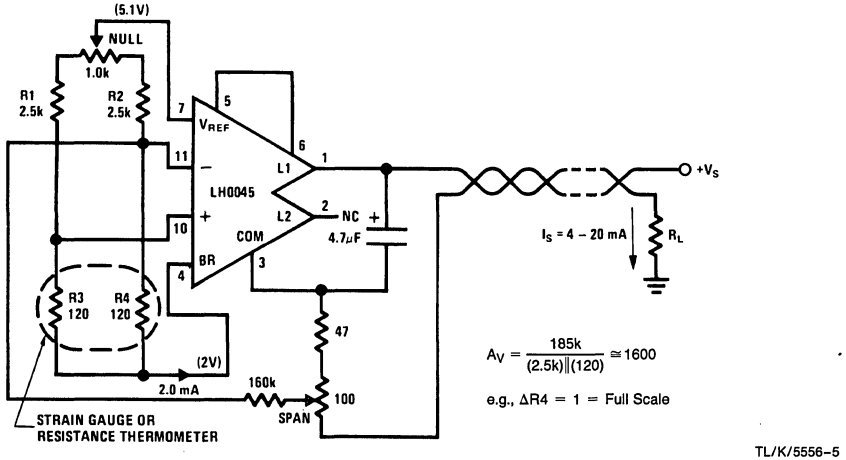
Thermocouple Input Transmitter



TL/K/5556–4

For 1 μA Full Scale, $R_{IN} = V_{IN}/1\ \mu A$ = Source Impedance @ Pin 11
e.g., V_{IN} (Full Scale) = 10 mV, R_{IN} = 10k
Bridge Impedance = 0.8k, R = 10k − 0.8k = 9.2k

Resistance Bridge Input Transmitter



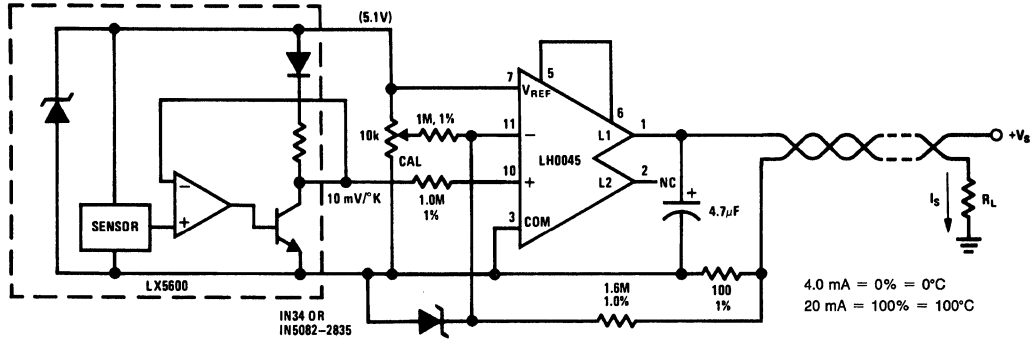
$$A_V = \frac{185k}{(2.5k)\|(120)} \cong 1600$$

e.g., ΔR4 = 1 = Full Scale

TL/K/5556–5

Typical Applications (Continued)

Electronic Temperature Sensor



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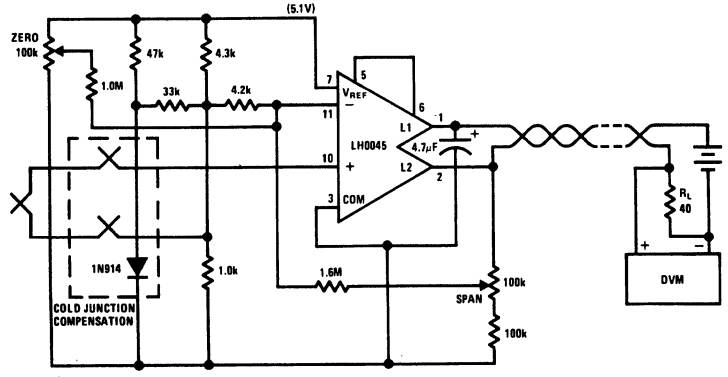
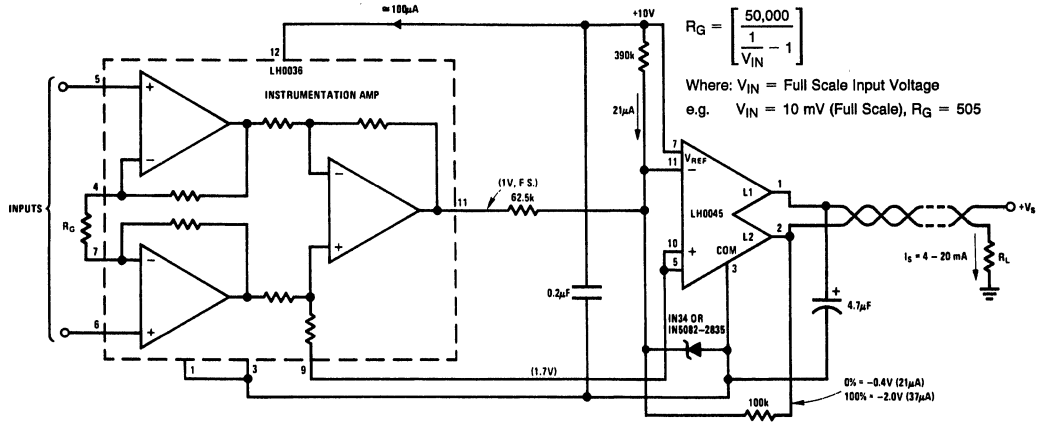
Remote Sensing Digital Thermometer



TL/K/5556–7

*All voltages indicated by ( ) are measured with respect to common, pin 3.

Instrumentation Amplifier Transmitter



TL/K/5556–8

*All voltages indicated by ( ) are measured with respect to common, pin 3.

Applications Information

CIRCUIT DESCRIPTION AND OPERATION

A simplified schematic of the LH0045/LH0045C is shown in *Figure 1*. Differential amplifier, A_2 converts very low level signals to an output current via transistor Q1. Reference voltage diode D1 is used to supply voltage for operation of A_2 and to bias an external bridge. Current source I_1 minimizes fluctuation in the bridge reference voltage due to changes in V_S.

In normal operation, the LH0045/LH0045C is used in conjunction with an external bridge comprised of R_{B1} through R_{B4}. The bridge resistors in conjunction with bridge return resistor, R5, bias A_2 in its linear region and sense the input signal; e.g. R_{B4} might be a strain sensitive resistor in a strain gauge bridge. R_T is adjusted to purposely unbalance the bridge for 4.0 mA output (null) for zero signal input. This is accomplished by forcing 2.5 μA more through R_{B3} than R_{B4}.

The 2.5 μA imbalance causes a voltage rise of (2.5 μA) $\times$ (100Ω) or 250 μV at the top of R_{B3}. Terminal L2 may be viewed as the output of an op amp whose closed loop gain is approximately $R_F/R_{B3} = 1600$.

The 250 μV rise at the top of R_{B3} causes a voltage drop of (1600) $\times$ (250 μV) or -0.4V across R9. An output current, I_S, equal to 0.4V/R9 or 4.0 mA is thus established in Q1. If R_{B4} is now decreased by 1.0Ω (due to application of a strain force), a -1.0 mV change in input voltage will result. This causes L2 to drop to -2.0V. The output current would then be 2.0V/100Ω or 20 mA (Full Scale). If R_{B3} is a resistor of the same material as R_{B4} but not subjected to the strain, temperature drift effects will be equal in the two legs and will cancel.

In actual practice the loading effects of R_{B2} on the gain (span) and R_F on output current must be taken into account.

THERMAL CONSIDERATIONS

The power output transistor of the LH0045 is thermally isolated from the signal amplifier, A_2. Nevertheless, a change in the power dissipation will cause a change in the temperature of the package and thus may cause amplifier drift. These temperature excursions may be minimized by careful heat sinking to hold the case temperature equal to the ambient. With the TO-8 (G) package this is best accomplished by a clip-on heat sink such as the Thermalloy #2240A or the Wakefield #215-CB. The case is electrically isolated from the circuit.

In addition, the power change can be minimized by operating the device from relatively high supply voltages in series with a relatively high load resistance. When the signal forces the supply current higher, the voltage across the device will be reduced and the internal power dissipation kept nearly equal to the low current, high voltage condition.

For example, take the case of a 4.0 mA to 20 mA transmitter with a 24V supply and a 100Ω load resistance. The power at 4.0 mA is (23.6V) $\times$ (4.0 mA) = 94.4 mW while at full scale the power is (22V) $\times$ (20 mA) = 440 mW. The net change in power is 345 mW. This change in power will cause a change in temperature and thus a change in offset voltage of A_2.

If the optimum load resistance of 800Ω (from *Figure 2*) is used, the power at null is [24V $-$ (4.0 mA) $\times$ (800Ω)] (4.0 mA) = 83 mW. The power at full scale is [24V $-$ (20 mA) $\times$ (800Ω)] (20 mA) = 160 mW. The net change is 77 mW. This change is significantly less than without the resistor.

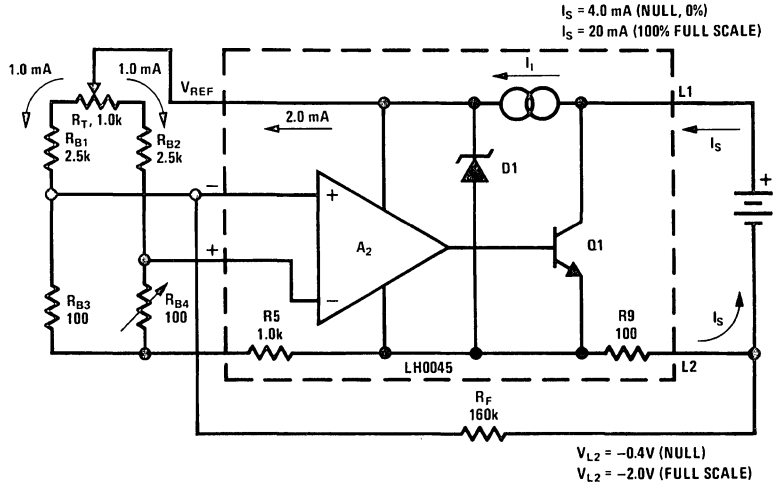


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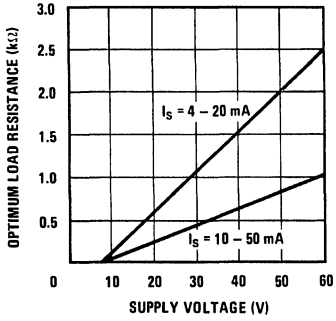
FIGURE 1. LH0045 Simplified Schematic

Applications Information (Continued)

If the supply voltage is increased to 48V and the load resistance chosen to be the optimum value from *Figure 2* (1.95k), then the power at null is [48V − (4.0 mA) × (1.95k)] (4.0 mA) = 160.8 mW and the power at full scale is [48 − (20) × (1.95k)] (20 mA) = 180 mW for a net change of 19.2 mW.



TL/K/5556–10

FIGURE 2. Optimum Load Resistance vs Supply Voltage

Note that the optimized load resistance is actually the sum of the line resistance, receiver resistances and added external load resistance. However, in many applications the line resistance and receiver resistances are negligible compared to the added external load resistance and thus may be omitted in calculations.

AUXILIARY PINS

The LH0045 has several auxiliary pins designed to provide the user with enhanced flexibility and performance. The following is a discussion of possible uses for these pins.

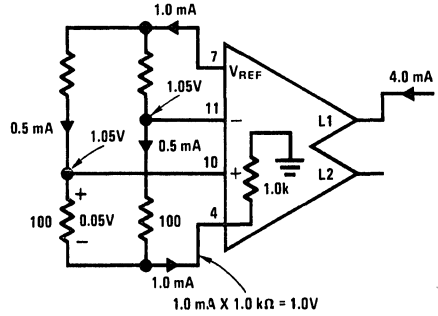
Programmable V_{REF}—Pins 5 and 6

The LH0045G provides pins 5 and 6 to allow the user to program the value of the reference voltage. The factory trimmed 10V value is obtained by leaving 5 and 6 open. A short between 5 and 6 will program the reference to a nominal 5.1V.

A resistor or pot may be placed between pin 5 and common (pin 3) to obtain reference voltages between 10V and 30V or between pin 5 and pin 7 for reference voltages below 10V. Increased reference voltage might be useful to extend the positive common mode range or to accommodate transducers requiring higher supply voltage. A plot of resistance between pin 5 and pin 3 versus V_{REF} is given in the typical electrical characteristics section. V_{REF} may be adjusted about its nominal value by arranging a pot from V_{REF} to common and feeding a resistor from the wiper into pin 5 so that it may either inject or extract current. Lastly, pin 5 may be used as a nominal 1.7V reference point, if care is taken not to unduly load it with either DC current or capacitance. Obviously, higher supply voltages must be used to obtain the higher reference values. The minimum supply voltage to reference voltage differential is about 4.0V.

Bridge Return

An applications resistor is provided in the LH0045 with a nominal value of 1.0 kΩ. The primary application for the resistor is to maintain the minimum common mode input voltage (1.0V) required by the signal amplifier, A_2. A typical input application might utilize a strain gauge or thermistor bridge where the resistance of the sensor is 100Ω. Since only 1.0 mA may be drawn from V_{REF}, the 1.0 kΩ bridge return resistor is used to bias A_2 in its linear region as shown in *Figure 3*.



TL/K/5556–11

FIGURE 3. Use of Bridge Return

Over Compensation—Pin 8

Over compensation of the signal amplifier, A_2, may be desirable in DC applications where the noise-bandwidth must be minimized. A capacitor should be placed between pin 8 and pin 3, common.

Typically,

$$f_{3\,db} = \frac{1}{2\pi R (C_1 + C_{EXT})}$$

where:

R = 400 MΩ
C1 = Internal Compensation Capacitor = 100 pF
C_{EXT} = External (overcompensation) Capacitor

Input Guard—Pins 9 and 12

Pins 9 and 12 have no internal connection whatever and thus need not be used. In some critical low current applications there may be an advantage to running a guard conductor between the inputs and the adjacent pins to intercept stray leakage currents. Pins 9 and 12 may be connected to this guard to simplify the PC board layout and allow the guard to continue under the device. (See AN-63 for further discussion of guarding techniques.)

NULL AND SPAN ADJUSTMENTS

Most applications of the LH0045 will require potentiometers to trim the initial tolerances of the sensor, the external resistors and the LH0045 itself. The preferred adjustment proce-

Applications Information (Continued)

dure is to stimulate the sensor, alternating between two known values, such as zero and full scale. The span and null are adjusted by monitoring the output current on a chart recorder, meter, or oscilloscope. A full scale stimulus is applied to the sensor and the span potentiometer adjusted for the desired full scale. Then, to adjust the null, apply a zero percent signal to the sensor and adjust the null potentiometer for the desired zero percent current indication.

If it is impractical to cycle the sensor during the calibration procedure, the signal may be simulated electrically with two cautions: 1) the calibration signal must be floating and 2) the calibration thus achieved does not account for sensor inaccuracies and/or errors in the signal generator.

SENSOR SELECTION

Generally it is easiest to use an insulated sensor. If it is necessary to use a grounded sensor, the power supply must be isolated from chassis ground to avoid extraneous circulating currents.

DESIGN EXAMPLE

There are numerous circuit configurations that may be utilized with the LH0045. The following is intended as a general design example which may be extended to specific cases.

Circuit Requirements

Output Characteristics

a. 0% = 4.0 mA (NULL)

b. 100% = 20 mA (SPAN = 16 mA)

c. Supply Voltage = 24V

Input (Sensor) Characteristics

a. V_{IN} = 100 mV (Full Scale)

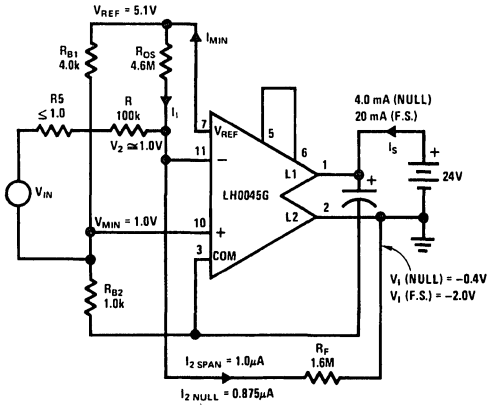
b. V_{IN} = 0 mV (Zero Scale)

c. Source Impedance ≤ 1.0Ω

General Characteristics

a. 0°C ≤ T_A ≤ +75°C

b. Overall Accuracy ≤ 0.5%



TL/K/5556–12

FIGURE 4. Design Example Circuit

Selection of R_F

Input bias current to the LH0045C is guaranteed less than 10 nA. Furthermore, the change in I_B over the temperature range of interest is typically under 1.0 nA. If $I_{2\ SPAN}$ is selected to be 1.0 μA (1000 ΔI_B) errors due to $\Delta I_B/\Delta T$ will be less than 0.1%. For SPAN = 16 mA.

$$V_{SPAN} = \Delta V_1 = -(16\ mA)(R9) = -1.6V$$

where R9 = Internal Current Set Resistor = 100Ω.

For $I_{2\ SPAN}$ = 1.0 μA,

$$R_F = \frac{V_{SPAN}}{I_{2\ SPAN}} = \frac{-1.6V}{1.0\ \mu A} = 1.6M$$

$$R_F = 1.6\ M\Omega$$

Note: For applications with DC gain (ratio of feedback and input resistance) less than 8, it is recommended that a Schottky barrier diode be connected between pin 11 (cathode) and pin 3 (anode). This prevents the possibility of latch up resulting from the inverting input being forced beyond the amplifier supply voltage during power up.

Selection of R_{B1} and R_{B2}

The minimum input common mode voltage, V_{MIN} required at the pin 10 input of A_2 is 1.0V. Furthermore, the maximum open loop supply current (I_{SOL}) drawn by the LH0045 is 3.0 mA. That leaves I_{MIN} = 4.0 mA − 3.0 mA = 1.0 mA left to bias the bridge at null. Hence:

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}} = \frac{1.0V}{1.0\ mA} = 1.0\ k\Omega$$

And,

$$\frac{V_{REF}\ R_{B2}}{R_{B1} + R_{B2}} = 1.0V$$

$$R_{B1} = R_{B2}\frac{V_{REF} - 1.0V}{1.0V}$$

$$= 1.0k\ (5.1 - 1.0)$$

$$R_{B1} \cong 4.0\ k\Omega$$

Alternatively, an LM113, 1.22V reference diode, or an op amp such as the LM108 may be used to bias the signal amplifier, A_2, as shown in *Figure 5.* These techniques have the advantage of lowering the impedance seen at pin 10.

Selection of R_{OS}

R_{OS} is selected to provide the null current of 4.0 mA, $V_{1\ NULL}$ = 4.0 mA × 100Ω = 0.4V. From previous calculations we know that V_{MIN} = 1.0V. The voltage pin 11, V_2 is:

$$V_2 = V_{MIN} + V_{OS} \cong V_{MIN}$$

for V_{IN} = OV

Hence, the current required to generate the null voltage, $I_{2\ NULL}$ is:

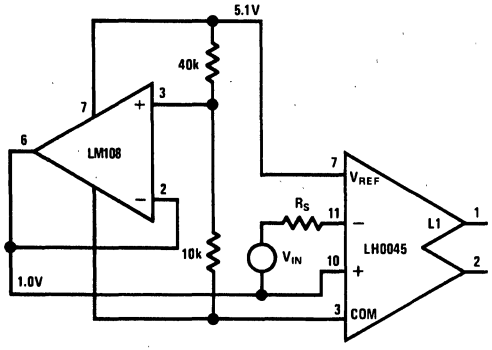
$$I_{2\ NULL} = \frac{V_{MIN} - V_{1\ NULL}}{R_F}$$

$$= \frac{1.0V - (-0.4V)}{1.6\ M\Omega} = 0.875\ \mu A$$

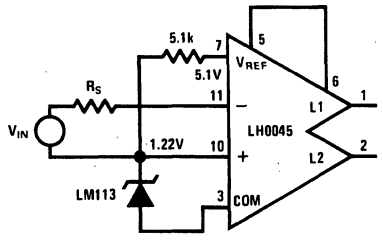
This current must be provided by R_{OS} from V_{REF}; hence:

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

Applications Information (Continued)



TL/K/5556–13



TL/K/5556–14

FIGURE 5. Alternate Biasing Techniques

The nominal value for V_{REF} is 5.1V, therefore the nominal value for R_{OS} is:

$$\frac{5.1V - 1.0V}{0.875\ \mu A} \text{ or}$$

$$R_{OS} = 4.6\ M\Omega$$

It should be noted however, that the variation of V_{REF} may be as high as 5.9V or as low as 4.3V. Furthermore, the tolerances of R9 (100Ω), R_{B1}. R_{B2}, and the input V_{OS} of A_2 would predict values for R_{OS} as low as 3.98M and as high as 5.43M. The implication is that in the specific case, R_{OS} should be implemented with a pot, of appropriate value, in order to accommodate the tolerances of V_{REF}, R9, V_{OS}, R_{B1}, R_{B2}, etc.

Selection of R

SPAN is required to be 16 mA. From feedback theory and the gain equation we know:

$$I_{SPAN} = V_{IN} \frac{R_F}{R} \times \frac{1}{R9}$$

where:

R = Total impedance in signal path between pin 10 and pin 11

R9 = Current setting resistor = 100Ω

V_{IN} = Full scale input voltage = 100 mV

$$\therefore R = \frac{(V_{IN})\ (R_F)}{(I_{SPAN}\ (R9)}$$

$$R = \frac{(100\ mV)\ (1.6\ M\Omega)}{(16\ mA)\ (100\Omega)}$$

$$R = 100\ k\Omega$$

As before, uncertainties in device parameters might dictate that R_F be made a pot of appropriate value.

Summary of the Steps to Determine External Resistor Values

1. Select $I_{FULL\ SCALE} = I_{NULL} + I_{SPAN}$ for the desired application. (I_{NULL} is frequently 4.0 mA and $I_{FULL\ SCALE}$ is frequently 20 mA.)
2. Select $I_{2\ SPAN}$ so that it is large compared to ΔI_B. 1000 ΔI_B is a good value.
3. Determine $V_{SPAN} = \Delta V_2 = (I_{SPAN})\ (R9)$.
4. Determine $R_F = (V_{SPAN}/I_{2\ SPAN})$
5. Select

$$R_{B2} \geq \frac{V_{MIN}}{I_{MIN}}$$

$$R_{B2} \geq \frac{1V}{I_{NULL} - I_{SOL}}$$

Where:

V_{MIN} = minimum common mode input voltage

I_{MIN} = minimum available bridge current

I_{SOL} = maximum open loop supply current

6. Determine

$$R_{B1} = R_{B2} \frac{V_{REF} - V_{MIN}}{V_{MIN}}$$

7. Determine $V_{2\ NULL} = I_{NULL}\ R9$
8. Determine

$$I_{2\ NULL} = \frac{V_{MIN} - V_{2\ NULL}}{R_F}$$

9. Determine

$$R_{OS} = \frac{V_{REF} - V_{MIN}}{I_{2\ NULL}}$$

10. Determine

$$R = \frac{(V_{IN})\ (R_F)}{(I_{SPAN})\ (R9)}$$

Where:

V_{IN} = Sensor full scale output voltage

Applications Information (Continued)

ERROR BUDGET ANALYSIS

Errors Due to Change in V_{REF} (ΔV_{REF})

There are several factors which could cause a change in V_{REF}. First, as the ambient temperature changes, a V_{REF} drift of ±0.2 mV/°C might be expected. Secondly, supply voltage variations could cause a 0.5 mV/V change in V_{REF}. Lastly, self-heating due to power dissipation variations can cause drift of the reference.

An overall expression for change in V_{REF} is:

$$\Delta V_{REF} = \underbrace{[(\theta)(\Delta P_{DISS}) + \Delta T_A]\frac{\Delta V_{REF}}{\Delta T}}_{\text{Thermal Effects}} + \underbrace{\frac{\Delta V_{REF}}{\Delta V_S}(\Delta V_S)}_{\text{Supply Voltage Effects}}$$

Where:

θ = Thermal resistance, either junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in avg. power dissipation

ΔT_A = Change in ambient temperature

$\frac{\Delta V_{REF}}{\Delta T}$ = Reference voltage drift (in mV/°C)

$\frac{\Delta V_{REF}}{\Delta V_S}$ = Line regulation of V_{REF}

Several steps may be taken to minimize the bracketed terms in the equation above. For example, operating the LH0045G with a heat sink reduces the thermal resistance from θ_{jA} = 83°C/W to θ_{jC} = 60°C/W. The ΔP_{DISS} term may be significantly reduced using the power minimization technique described under "Thermal Considerations". For the design example, ΔP_{DISS} is reduced from 384 mW to 77 mW (R_L = 800Ω). Evaluating the LH0045G with a heat sink and R_L = 800Ω yields.

$$\Delta V_{REF} = \left(\frac{60°C}{W}(0.077W) + 75°C\right)\left(\frac{0.2\ mV}{°C}\right) + \frac{0.5\ mV}{V}(16V)$$

$$\Delta V_{REF} = 24\ mV$$

An expression for error in the output current due to ΔV_{REF} is:

$$\frac{\Delta I_S}{I_{SPAN}}(\%) = 100\frac{(K)(R_{OS})(\Delta V_{REF}) - (1-K)(\Delta V_{REF})(RF)}{(R9)(R_{OS})(I_{SPAN}}$$

Where:

ΔV_{REF} = Total change in V_{REF}

$K = \frac{R_{B2}}{R_{B1} + R_{B2}}$

R9 = Current set resistor

I_{SPAN} = Change in output current from 0% to 100%

For example, ΔV_{REF} = 24 mV, K = 0.2, R9 = 100Ω, I_{SPAN} = 16 mA. Hence, a 0.12% worst case error might be expected in output currents due to ΔV_{REF} effects.

Error Due to V_{OS} Drift

One of the primary causes of error in I_S is caused by V_{OS} drift. Drift may be induced either by self heating of the device or ambient temperature changes. The input offset voltage drift, $\Delta V_{OS}/\Delta T$, is nominally 3.3 μV/°C per millivolt of initial offset. An expression for the total temperature dependent drift is:

$$\Delta V_{OS} = [(\theta)(\Delta P_{DISS}) + \Delta T_A]\frac{\Delta V_{OS}}{\Delta T}$$

Where:

θ = Thermal resistance either junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

ΔT_A = Change in ambient temperature

The bracketed term may be minimized by heat sinking and using the power minimization technique described under "Thermal Considerations". For the LH0045G design example, ΔV_{OS} = 0.352 mV under ambient conditions and 0.263 mV using a heat sink and R_L = 800Ω.

The error in output current due to ΔV_{OS} is:

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in }\%) = 100 \times \frac{\Delta V_{OS}}{V_{IN\ (FULL\ SCALE)}} = 100 \times \frac{R_F}{(R)(R9)(I_{SPAN})}$$

For the design example, ΔV_{OS} = 0.263 mV, V_{IN} (Full Scale) = 100 mV. Hence, 0.26 mV ÷ 100 mV or 0.26% worst case error could be expected in output current effects.

Errors Due to Changes in R9

The temperature coefficient of R9 (TCR) will produce errors in the output current. Changes in R9 may be caused by self-heating of the device or by ambient temperature changes.

$$\frac{\Delta I_S}{I_{SPAN}}(\text{in }\%) = 100\frac{\Delta R9}{\Delta T}(\theta\ P_{DISS} + \Delta T_A)$$

Where:

θ = Thermal resistance either from junction-to-ambient or junction-to-case

ΔP_{DISS} = Change in average power dissipation

3

Applications Information (Continued)

ΔT_A = Change in ambient temperature

$\frac{\Delta R9}{\Delta T}$ = TCR of R9

Using the LH0045G design example, $\Delta R9/\Delta T$ = 0.03%/°C, hence a 3.2% worst case error in output current might be expected for operation without a heat sink over the temperature range.

Heat sinking the device and using R_L = 800Ω, reduces $\Delta I_S/I_{SPAN}$ to 2.3%.

The error analysis indicates that the internal current set resistor, R9, is inadequate to satisfy high accuracy design criterion. In these instances, an external 100Ω resistor should be substituted for R9.

Obviously, the TCR of the resistor should be low. Metal film or wire-wound resistors are the best choice offering TCR's less than 10 ppm/°C versus 50 ppm/°C typical drift for R9.

External Causes of Error

The components external to the LH0045 are also critical in determining errors. Specifically, the composition of resistors R_{B1}, R_{OS}, R_F, R, etc. in the design example will influence both drift and long term stability.

In particular, resistors and potentiometers of wire wound construction are recommended. Also, metal-film resistors with low TCR (≤ 10 ppm/°C) may be used for fixed resistor applications.

Error Analysis Summary

The overall errors attributable to the LH0045 may be minimized using heat sinking, and utilization of an external load resistor. Although R_L reduces the compliance of the circuit, its use is generally advisable in precision applications. External components should be selected for low TCR and long term stability.

The design example errors, using an external 100Ω wire wound resistor for R9 equal:

$$\frac{\Delta I_S}{I_{SPAN}} = \underbrace{0.12\%}_{\Delta V_{REF}} + \underbrace{0.26\%}_{\Delta V_{OS}} + \underbrace{0.08\%}_{\Delta R9} = 0.46\%$$

SOCKETS AND HEAT SINKS

Mounting sockets, test sockets and heat sinks are available for the G package.

The following or their equivalents are recommended:

Sockets:

G — 12-Lead TO-8: Barnes Corp. #MGX-12
Textool #212-100-323

Heat Sinks:

G — 12-Lead TO-8: Thermalloy #2240A
Wakefield #215-CB

Definition of Terms

Input Offset Voltage, V_{OS}: The voltage which must be applied between the input terminals through equal resistances to obtain 4.0 mA of supply (output) current.

Input Bias Current, I_B: The average of the two input currents.

Input Offset Current, I_{OS}: The difference in the current into the two input terminals when the supply (output) current is 4.0 mA.

Input Resistance, R_{IN}: The ratio of the change in input voltage to the change in input current at either input with the other input connected to 1.0 V_{DC}.

Open Loop Transconductance, g_{MOL}: The ratio of the supply (output) current SPAN to the input voltage required to produce that SPAN.

Open Loop Output Resistance, R_{OUT}: The ratio of a specified supply (output) voltage change to the resulting change in supply (output) current at the specified current level.

Common Mode Rejection Ratio, CMRR: The ratio of the change in input offset voltage to the peak-to-peak input voltage range.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in supply (output) voltage producing it.

Input Voltage Range, V_{IN}: The range of voltages on the input terminals for which the device operates within specifications.

Open Loop Supply Current, I_S: The supply current required with the signal amplifier A_2 biased off (inverting input positive, non-inverting input negative) and no load on the V_{REF} terminal.

This represents a measure of the minimum low end signal current.

Reference Voltage Line Regulation, $\Delta V_{REF}/\Delta V_S$: The ratio of the change in V_{REF} to the peak-to-peak change in supply (output) voltage producing it.

Reference Voltage Load Regulaion, $\Delta V_{REF}/\Delta I_{REF}$: The change in V_{REF} for a stipulated change in I_{REF}.

National Semiconductor

LH0061/LH0061C 0.5 Amp Wide Band Operational Amplifier

General Description

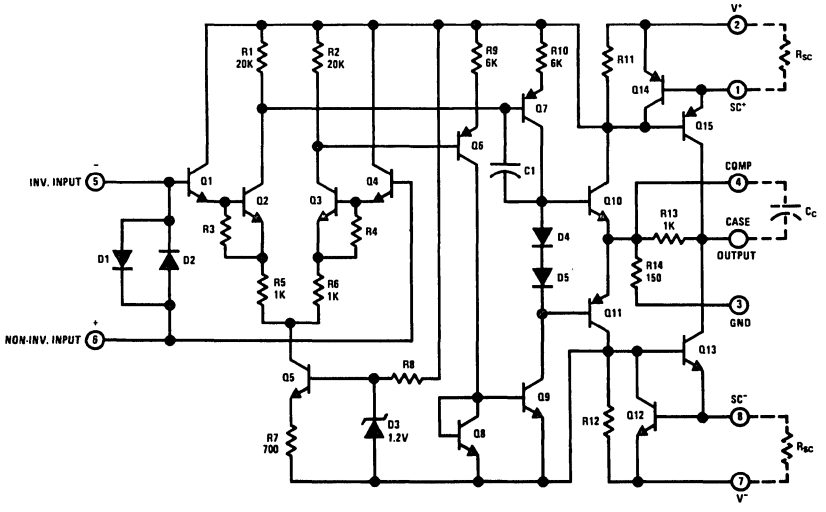
The LH0061/LH0061C is a wide band, high speed, operational amplifier capable of supplying currents in excess of 0.5 ampere at voltage levels of ±12V. Output short circuit protection is set by external resistors, and compensation is accomplished with a single external capacitor. With a suitable heat sink the device is rated at 20W.

The wide bandwidth and high output power capabilities of the LH0061/LH0061C make it ideal for such applications as AC servos, deflection yoke drivers, capstan drivers, and audio amplifiers. The LH0061 is guaranteed over the temperature range −55°C to +125°C; whereas, the LH0061C is guaranteed from −25°C to +85°C.

Features

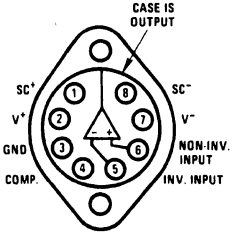
■ Output current	0.5A
■ Wide large signal bandwidth	1 MHz
■ High slew rate	70V/μs
■ Low standby power	240 mW
■ Low input current	300 nA Max

Schematic and Connection Diagrams



TL/K/6861–1

TO-3 Package



TL/K/6861–2

Top View

Order Number LH0061CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage	±18V
Power Dissipation	See Curve
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Peak Output Current	2A
Output Short Circuit Duration (Note 4)	Continuous
Operating Temperature Range	
LH0061	−55°C to +125°C
LH0061C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD rating to be determined.	

DC Electrical Characteristics (Note 1)

Parameter	Conditions	Limits						Units
		LH0061			LH0061C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \le 10\,k\Omega$, $T_C = 25°C$, $V_S = \pm 15V$ $R_S \le 10\,k\Omega$, $V_S = \pm 15V$		1.0	4.0 6.0		3.0	10 15	mV mV
Voltage Drift with Temperature	$R_S \le 10\,k\Omega$		5			5		μV/°C
Offset Voltage Change with Output Power			5			5		μV/watt
Input Offset Current	$T_C = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			1			1		nA/°C
Input Bias Current	$T_C = 25°C$		100	300 1.0		200	500 1.0	nA μA
Input Resistance	$T_C = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \le 10\,k\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		60	80		dB
Input Voltage Range	$V_S = \pm 15V$	±11			±11			V
Power Supply Rejection Ratio	$R_S \le 10\,k\Omega$, $\Delta V_S = \pm 10V$	70	80		50	70		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\,k\Omega$, $T_C = 25°C$ $V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 20\Omega$	50 5	100		25 2.5	50		V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 20\Omega$	±10	±12		±10	±12		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_C = 25°C$, $R_{SC} = 1.0\Omega$		600			600		mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		7	10		10	15	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		210	300		300	450	mW

AC Electrical Characteristics (T_C = 25°C, V_S = ±15V, C_C = 3000 pF)

Parameter	Conditions	Limits						Units
		LH0061			LH0061C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	A_V = +1, R_L = 100Ω	25	70		25	70		V/μs
Power Bandwidth	R_L = 100Ω		1			1		MHz
Small Signal Transient Response			30			30		ns
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	ΔV_{IN} = 10V, A_V = +1		0.8			0.8		μs
Overload Recovery Time			1			1		μs
Harmonic Distortion	f = 1 kHz, P_O = 0.5W		0.2			0.2		%

Note 1: Specifications apply for ±5V ≤ V_S ≤ ±18V, C_C = 3000 pF, and −55°C ≤ T_C ≤ +125°C for the LH0061K and −25°C ≤ T_C ≤ +85°C for the LH0061CK. Typical values are for T_C = 25°C.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Excessive current will flow if a differential voltage in excess of 1V is applied between the inputs without limiting resistors.

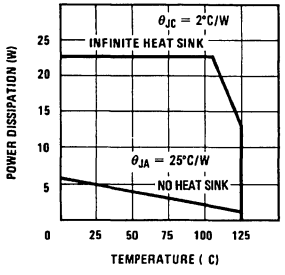
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Rating applies as long as package power rating is not exceeded.

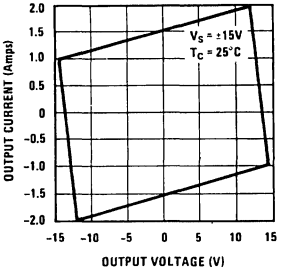
Note 5: Refer to RETS0061K for LH0061K military specifications.

Typical Performance Characteristics

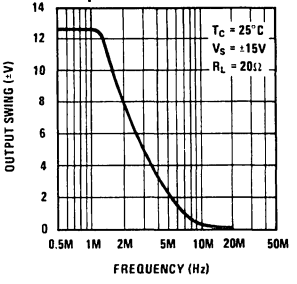
Power Derating



Safe Operating Area



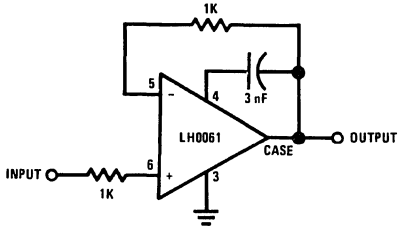
Large Signal Frequency Response



TL/K/6861–3

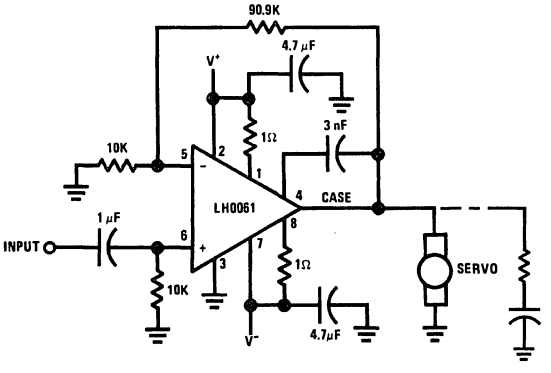
Typical Applications

Unity Gain Driver



TL/K/6861–4

AC Servo Amplifier



TL/K/6861–5

National Semiconductor

LH0062/LH0062C High Speed FET Operational Amplifier

General Description

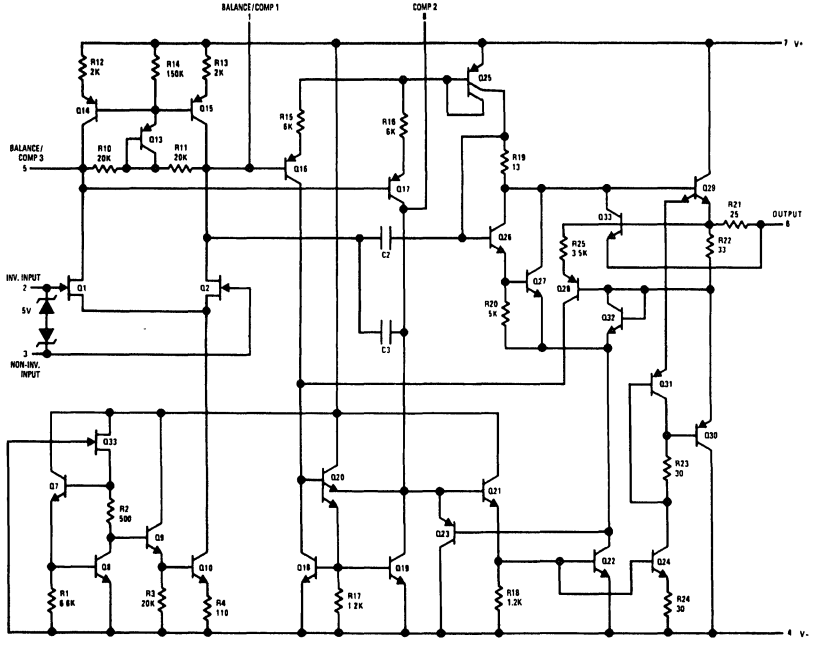
The LH0062/LH0062C is a precision, high speed FET input operational amplifier with more than an order of magnitude improvement in slew rate and bandwidth over conventional FET IC op amps. In addition it features very closely matched input characteristics, very high input impedance, and ultra low input currents with no compromise in noise, common mode rejection ratio or open loop gain. The device has internal unity gain frequency compensation, thus assuring stability in all normal applications. This considerably simplifies its application, since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 120 V/μs and almost double the bandwidth. (See LB-2, LB-14, and LB-17 for discussions of the application of feed-forward techniques). Over-compensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs. In addition it is free of latch-up and may be simply offset nulled with negligible effect on offset drift or CMRR.

The LH0062 is designed for applications requiring wide bandwidth, high slew rate and fast settling time while at the same time demanding the high input impedance and low input currents characteristic of FET inputs. Thus it is particularly suited for such applications as video amplifiers, sample/hold circuits, high speed integrators, and buffers for A/D conversion and multiplex system. The LH0062 is specified for the full military temperature range of −55° to +125°C while the LH0062C is specified to operate over a −25°C to +85°C temperature range.

Features

- High slew rate 70 V/μs
- Wide bandwidth 15 MHz
- Settling time (0.1%) 1 μs
- Low input offset voltage 2 mV
- Low input offset current 1 pA
- Wide supply range ±5V to ±20V
- Internal 6 dB/octave frequency compensation
- Pin compatible with std IC op amps (TO-5 pkg)

Schematic Diagram



TL/K/6862–1

*Pin Numbers Shown for TO-5 Package

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage	±20V
Power Dissipation (see graph)	500 mW
Input Voltage (Note 1)	±5V
Differential Input Voltage (Note 2)	±30V
Short Circuit Duration	Continuous
Operating Temperature	
LH0062	−55°C to +125°C
LH0062C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Limits						Units
		LH0062			LH0062C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\ k\Omega$, $T_A = 25°C$, $R_S \leq 100\ k\Omega$		2	5 7		10	15 20	mV mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		25			25		µV/°C
Offset Voltage Drift with Time			4			5		µV/week
Input Offset Current	$T_A = 25°C$		0.2	2 2		1	5 0.2	pA nA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$ (Note 4)		5	10 10		10	65 2	pA nA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4			4		pF
Input Voltage Range	$V_S = \pm 15V$	±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	80	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	80	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$, $V_S = \pm 15V$ $R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$, $V_S = \pm 15V$	50 25	200		25 25	160		V/mV V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, $V_S = \pm 15V$ $R_L = 2\ k\Omega$, $V_S = \pm 15V$	±12 ±10	±13		±12 ±10	13		V V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current	$T_A = 25°C$		25			25		mA
Supply Current	$V_S = \pm 15V$		5	8		7	12	mA
Power Consumption	$V_S = \pm 15V$			240			360	mW

3

AC Electrical Characteristics (T_A = 25°C, V_S = ±15V)

Parameter	Conditions	Limits						Units
		LH0062			LH0062C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	Voltage Follower	50	70		50	70		V/μs
Large Signal Bandwidth	Voltage Follower		2			2		MHz
Small Signal Bandwidth			15			15		MHz
Rise Time			25			25		ns
Overshoot			10			15		%
Settling Time (0.1%)	ΔV_{IN} = 10V		1			1		μs
Overload Recovery			0.9			0.9		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<0.1			<0.1		pArms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Inputs are protected from excessive voltages by back-to-back diodes. Input currents should be limited to 1 mA.

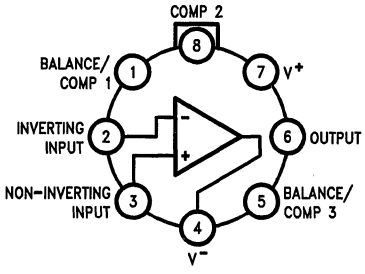
Note 3: Unless otherwise specified, these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ for the LH0062 and $-25°C \leq T_A \leq +85°C$ for the LH0062C. Typical values are given for T_A = 25°C. Power supplies should be bypassed with 0.1 μF ceramic capacitors.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature T = 25°C , self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

Note 5: Refer to RETS0062X for LH0062D and LH0062H military specifications.

Connection Diagrams

Metal Can Package

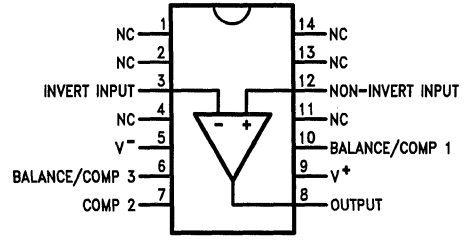


TL/K/6862–2

Top View

Order Number LH0062H or LH0062CH
See NS Package Number H08D

Dual-In-Line Package



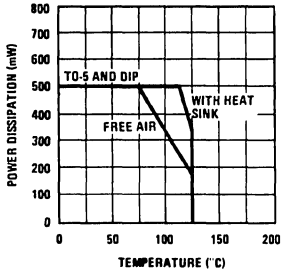
TL/K/6862–3

Top View

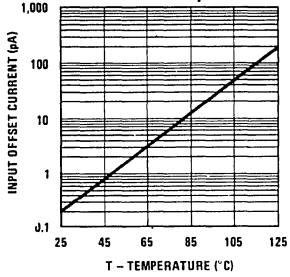
Order Number LH0062D or LH0062CD
See NS Package Number D14E

Typical Performance Characteristics

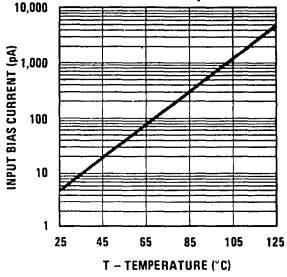
Maximum Power Dissipation



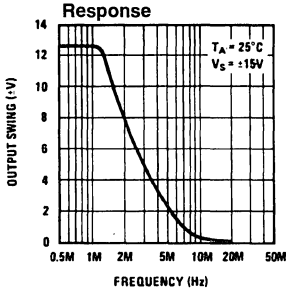
Input Offset Current vs Temperature



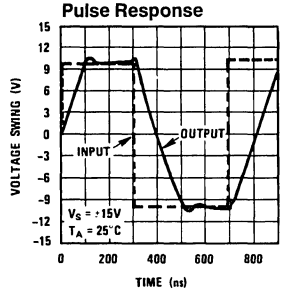
Input Bias Current vs Temperature



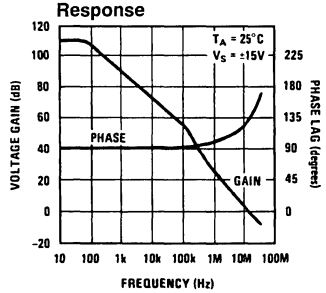
Large Signal Frequency Response



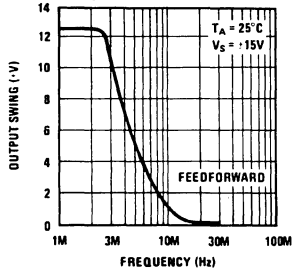
Voltage Follower Pulse Response



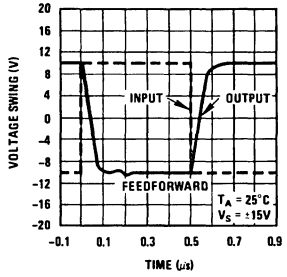
Open Loop Frequency Response



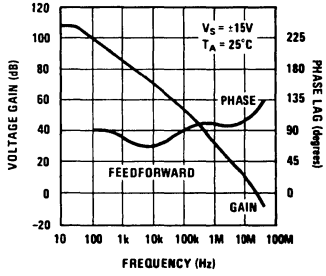
Large Signal Frequency Response



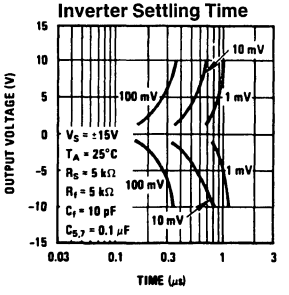
Inverter Pulse Response



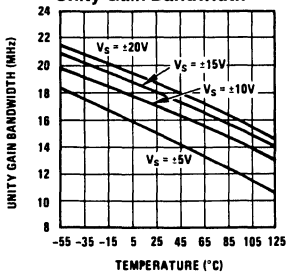
Open Loop Frequency Response



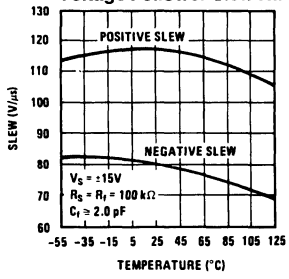
Inverter Settling Time



Unity Gain Bandwidth



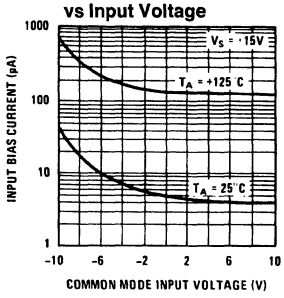
Voltage Follower Slew Rate



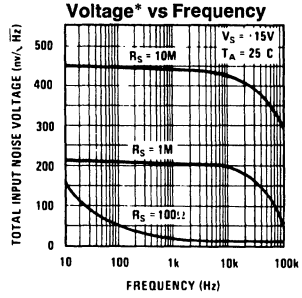
TL/K/6862–4

Typical Performance Characteristics (Continued)

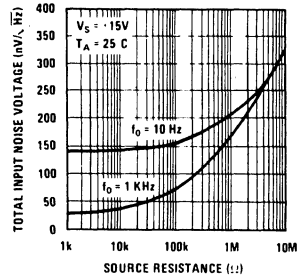
Input Bias Current vs Input Voltage



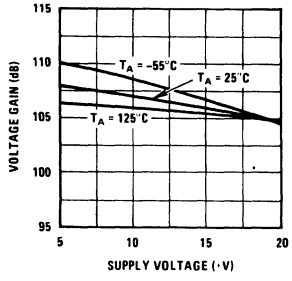
Total Input Noise Voltage* vs Frequency



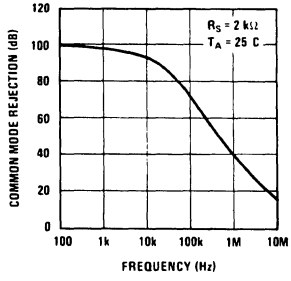
Total Input Noise Voltage* vs Source Resistance



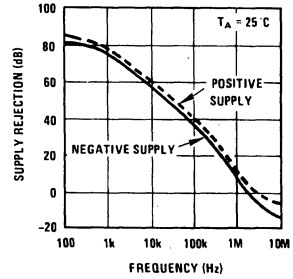
Voltage Gain



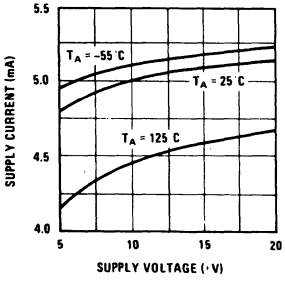
Common Mode Rejection



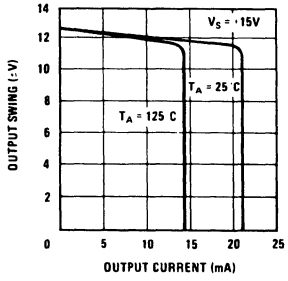
Power Supply Rejection



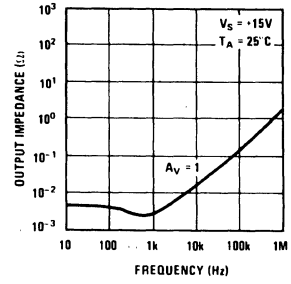
Supply Current



Current Limiting



Closed Loop Output Impedance

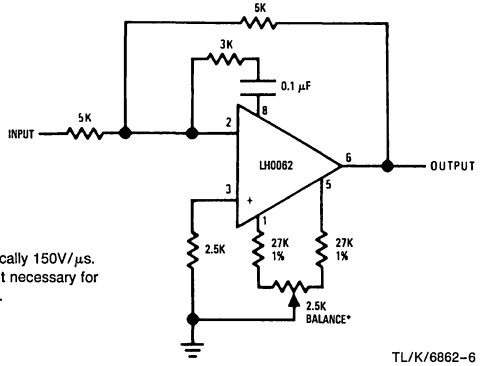


TL/K/6862–5

*Noise Voltage Includes Contribution from Source Resistance

Auxiliary Circuits

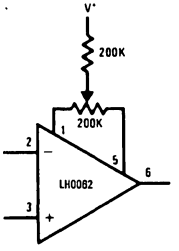
Feedforward Compensation for Greater Inverting Slew Rate†



†Slew rate typically 150V/μs.
*Balance circuit necessary for increased slew.

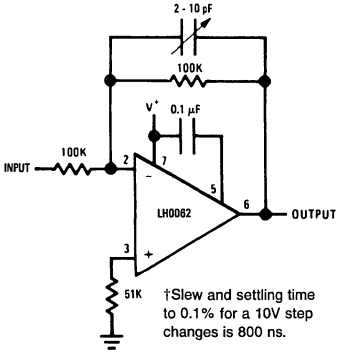
TL/K/6862-6

Offset Balancing



TL/K/6862-7

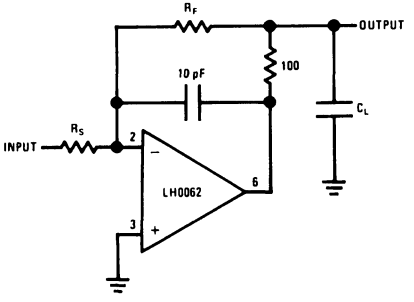
Compensation for Minimum Settling† Time



†Slew and settling time to 0.1% for a 10V step changes is 800 ns.

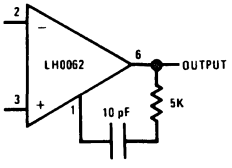
TL/K/6862-8

Isolating Large Capacitive Loads



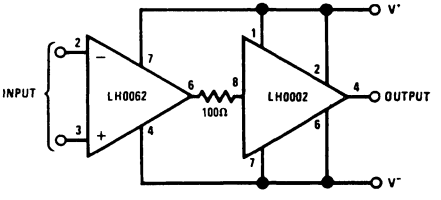
TL/K/6862-9

Overcompensation



TL/K/6862-10

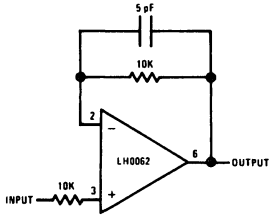
Boosting Output Drive to ±100 mA



TL/K/6862-11

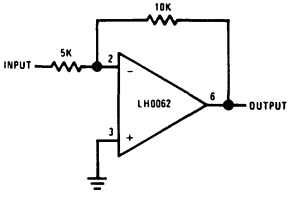
Typical Applications*

Fast Voltage Follower



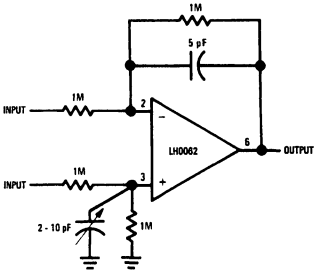
TL/K/6862-12

Fast Summing Amplifier



TL/K/6862-13

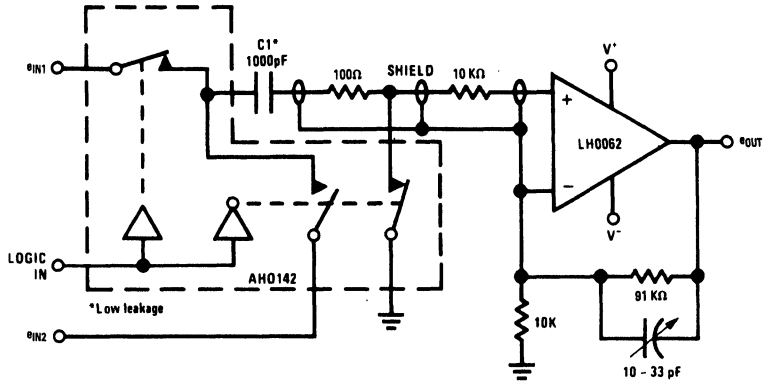
Differential Amplifier



TL/K/6862-14

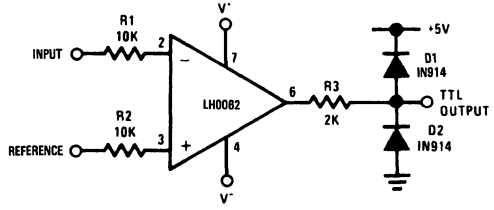
Typical Applications* (Continued)

High Speed Subtractor



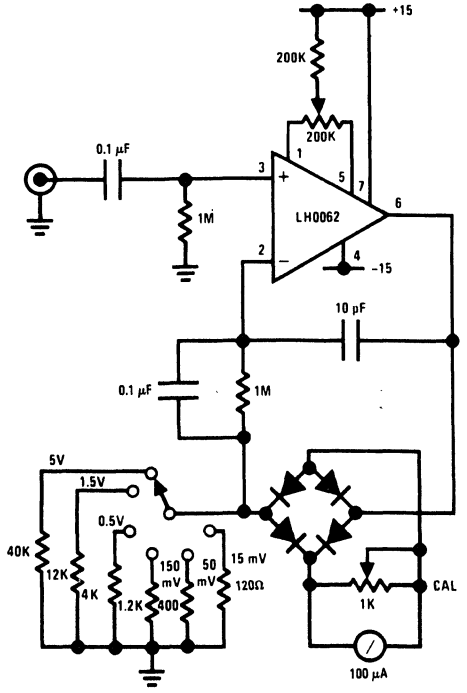
TL/K/6862–15

Fast Precision Voltage Comparator



TL/K/6862–16

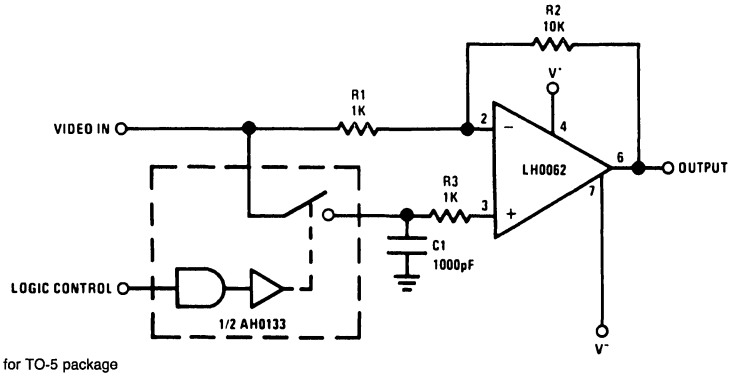
Wide Range AC Voltmeter



TL/K/6862–17

Typical Applications* (Continued)

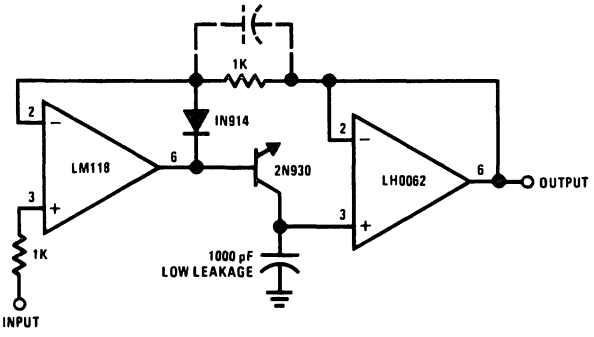
Video DC Restoring Amplifier



*Pin numbers shown for TO-5 package

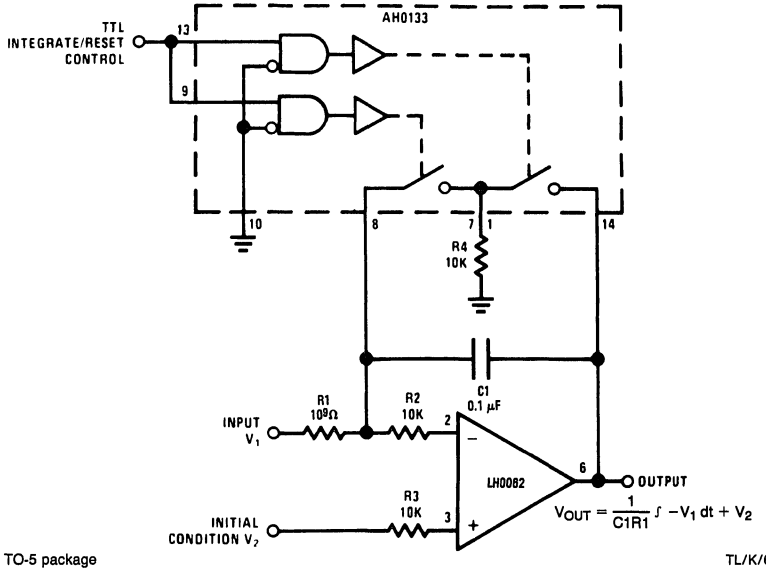
TL/K/6862–18

High Speed Positive Peak Detector



TL/K/6862–19

Precision Integrator

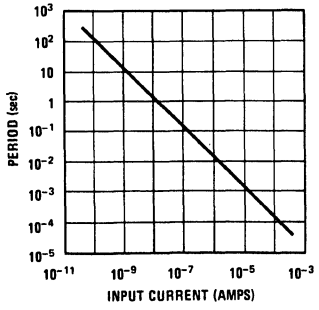


*Pin numbers shown for TO-5 package

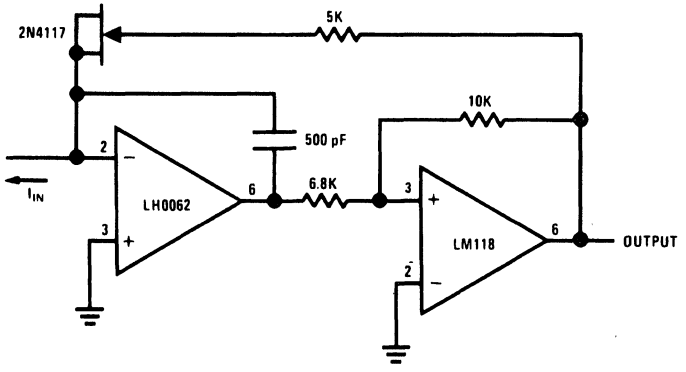
TL/K/6862–20

Typical Applications* (Continued)

Precision Wide Range Current to Period Converter



TL/K/6862–21



TL/K/6862–22

National Semiconductor

LH0082 Optical Communication Receiver/Amplifier

General Description

The LH0082 is a general purpose, low-noise, fiber-optic receiver, which may also be used as a fast current to voltage converter, or as a high speed voltage amplifier. The circuit includes a wide-bandwidth FET-input amplifier, a 2.4V reference, a comparator with hysteresis, and all the necessary resistors and capacitors for feedback and coupling, all integrated in a hermetic dual-in-line package. The large gain-bandwidth of the preamp enables fast response even with high capacitance photodiodes. A separate analog output permits the reception of analog signals to 20 MHz via a fiber-optic link. The internal comparator converts a low level analog signal to a CMOS/TTL compatible logic signal at data rates up to 5 Mbits/s NRZ. The LH0082 can be used with an external comparator at data rates to 40 Mbits/s.

Features

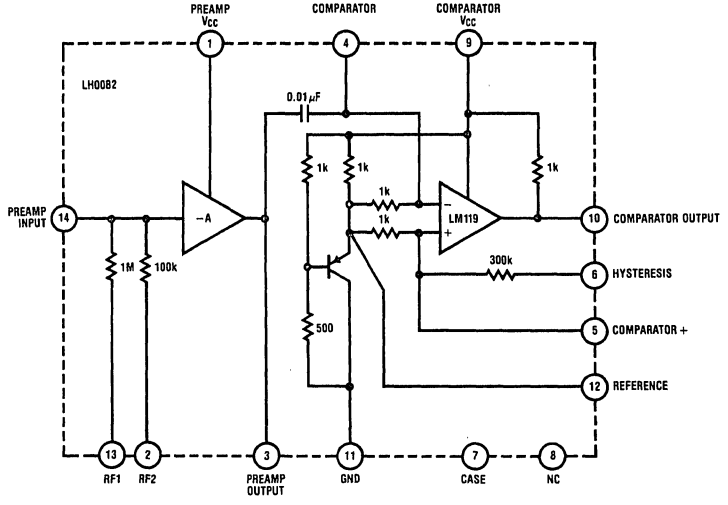
- Single 4.5V to 12V supply
- 600 MHz unity gain bandwidth
- Low noise
- Low edge jitter
- $<10^{-9}$ bit error rate
- Low input bias current
- Pin selectable sensitivity: −45 dBm/−35 dBm*
- CMOS/TTL compatibility
- Can be used with photodiodes, PIN photodiodes, phototransistors, avalanche photodiodes, and photomultipliers
- Hermetic dual-in-line metal package
- Highly versatile building block
- >21 dB dynamic range

Applications

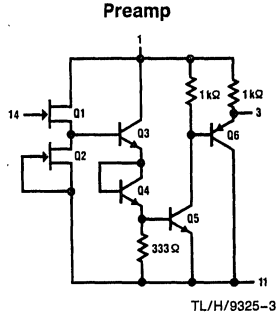
- Data terminals
- Secure communication
- Peripheral control/communication
- Video transmission
- Wideband amplifier
- High speed current to voltage converter
- Fiber-optic repeater
- Video amplifier
- Industrial machine control

*Assumes 0.5 A/W PIN diode input

Schematic Diagrams



TL/H/9325-1



TL/H/9325-3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 1)

Supply Voltage	+15V
Power Dissipation, T_A = 25°C	0.5W
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Operating Temperature Range (Note 2) LH0082CD	−25°C to +85°C
Lead Temperature (Soldering, 10 sec.)	260°C
Input Current	±10 mA
ESD Susceptibility	TBD

Electrical Characteristics Preamplifier: Power supply voltage = +5 V_{DC}, T_A = 25°C, see *Figure 1*

Symbol	Parameter	Min	Typ	Max	Units
I_B	Input Bias Current		100	250	pA
C_{IN}	Input Capacitance			5	pF
A_V	Voltage Gain	50	90		V/V
$f_{3\,dB}$	−3 dB Frequency		18		MHz
V_Q	Output Quiescent Voltage	1.9	2.1	2.6	V
$\Delta V_Q/\Delta T$	Output Quiescent Voltage Drift with Temperature		−6		mV/°C
Z_O	Open Loop Output Impedance at 1 MHz		30		Ω
	Output Noise (10 Hz to 10 MHz)		300		μV RMS
V_O	Output Swing (No Load)	3.5	4.0		V_{P-P}
	Transimpedance:				
	Low Sensitivity	90	100	110	kΩ
	High Sensitivity	0.9	1	1.1	MΩ
I_S	Supply Current		22	30	mA

Electrical Characteristics Comparator/Reference: Power supply voltage = +5 V_{DC}, T_A = 25°C, see *Figure 2*

Symbol	Parameter	Min	Typ	Max	Units
R_{IN}	Comparator Input Resistance (to Reference)	0.90	1	1.10	kΩ
V_{HYST}	Hysteresis Voltage				
	Positive	7	8.7	11.4	mV
	Negative	5	6.9	8.8	mV
R_O	Output Pull-up Resistor	0.90	1	1.10	kΩ
V_R	Reference Voltage	2.2	2.4	2.6	V
$\Delta V_R/\Delta T$	Reference Voltage Drift with Temperature		−2		mV/°C
R_O (V_{REF})	Reference Voltage Output Resistance		15		Ω
V_{OL}	(I_{OL} = 3.2 mA)		0.3	0.5	V
V_{OH}	(I_{OH} = −1 mA)	3.8	4		V
T_{PD}	(V_{IN} = 30 mV, V_{OD} = 15 mV)		160		ns
T_R	(C_L = 3 pF)		80		ns
T_F	(C_L = 3 pF)		60		ns
I_S	Supply Current:				
	Output High	4.5	8	17	mA
	Output Low	9.5	13	22	mA

Electrical Characteristics

Fiber-Optic Receiver: Photodiode responsivity is assumed to be 0.5 A/W, capacitance of 10 pF at 2.5V reverse bias, V_{CC} = 5V, T_A = 25°C, C_L = 15 pF

Symbol	Parameter	Min	Typ	Max	Units
	High Sensitivity: R_F = 1 MΩ, (see *Figure 3*) Input Power for 10^{-9} BER (Bit Rate = 500 kbit NRZ)		200		nW
t_r, t_f	Analog Output Rise or Fall Time		1.5		μs
	Maximum Data Rate, NRZ, Digital Output		650		kbit/s
P_N	Noise Equivalent Power		1		nW
i_N	Equivalent Input Noise Current (10 Hz to 10 MHz)		300		pA RMS
	Low Sensitivity: R_F = 100 kΩ, (see *Figure 4*) Input Power for 10^{-9} BER (Bit Rate = 2 Mbit NRZ)		800		nW
t_r, t_f	Analog Output Rise or Fall Time		50		ns
	Maximum Data Rate, NRZ, Digital Output		5		Mbit/s
P_N	Noise Equivalent Power		10		nW
i_N	Equivalent Input Noise Current (10 Hz to 10 MHz)		3		nA RMS
I_S	Total Supply Current (High or Low Sensitivity)		35		mA

Note 1: Refer to RETS0082D for LH0082D/883 and LH0082D-MIL specifications.

Note 2: For military temperature range, see RETS0082D.

DIGITAL EDGE JITTER

A potential problem in digital transmission systems is "edge jitter". Jitter is related to the system rise time and receiver noise and can be approximated by the following equation:

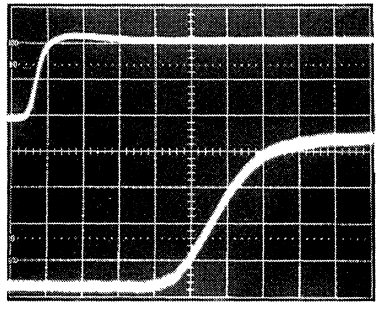
$$\text{RMS edge jitter} = \frac{\text{System rise time (10\%–90\%)}}{\text{(p/p signal voltage} \div \text{RMS noise voltage in receiver)}}$$

For a 5 Mbits/s NRZ operation using a 0.5 A/W PIN diode, the LH0082 requires a 2 μW peak optical power. This translates to 120 mV peak-to-peak signal voltage. Following through this equation the RMS edge jitter of the LH0082 is inconsequential at approximately 0.1 μs.

Fiber-Optic Receiver Preamp Response

R_F = 100 kΩ

Photodiode capacitance = 10 pF, V_{CC} = 5V



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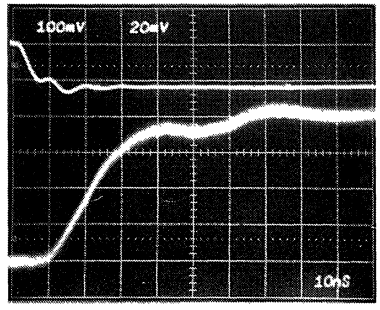
Preamp Voltage Mode Pulse Response

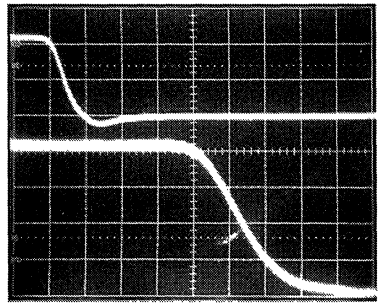


Input
(1 mV/div)

Output
(20 mV/div)

Small Signal

TL/H/9325–5

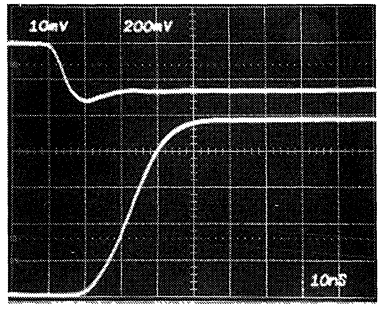


Optical Input

Preamp output
(20 mV/div)

Time (10 ns/div)

TL/H/9325–6



Input
(10 mV/div)

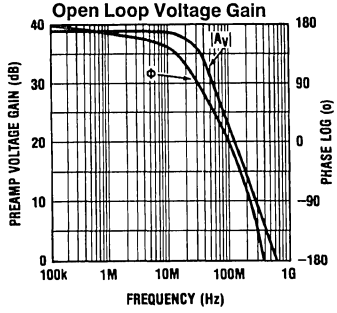
Output
(200 mV/div)

Large Signal

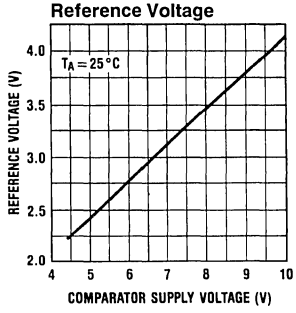
TL/H/9325–7

Typical Performance Characteristics

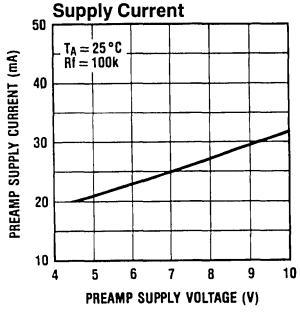
Open Loop Voltage Gain



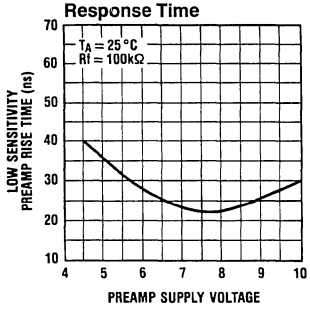
Reference Voltage



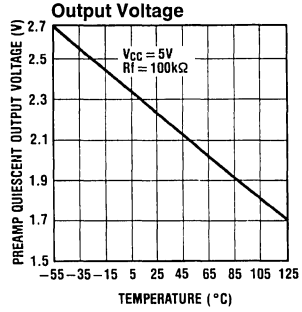
Supply Current



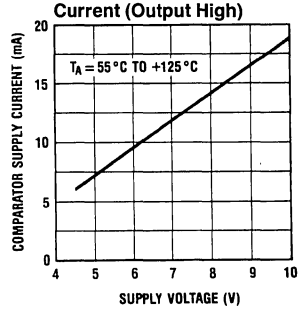
Response Time



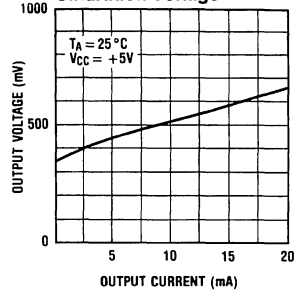
Output Voltage



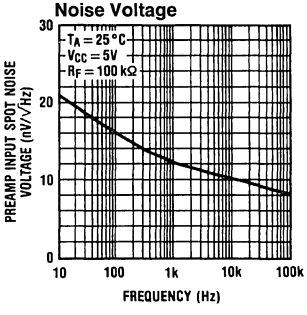
Comparator Supply Current (Output High)



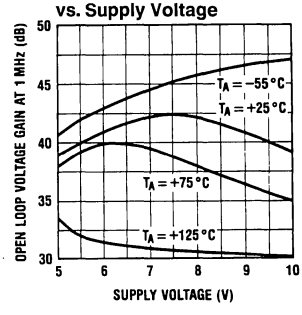
Comparator Output Saturation Voltage



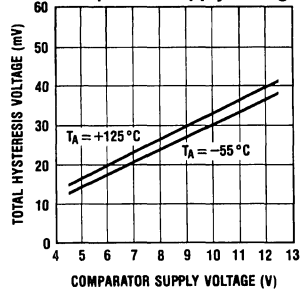
Preamp Input Spot Noise Voltage



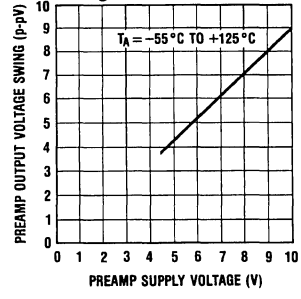
Preamp Open Loop Voltage vs. Supply Voltage



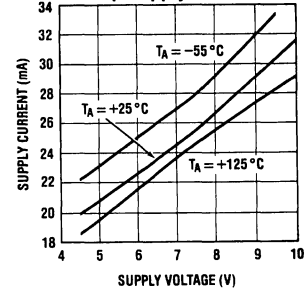
Hysteresis Voltage vs. Comparator Supply Voltage



Preamp Output Voltage Swing



Preamp Supply Current



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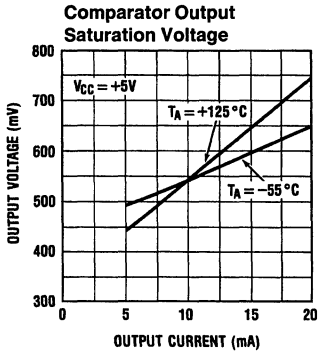
Typical Performance Characteristics (Continued)



TL/H/9325-9

Applications Information

The gain-bandwidth of the LH0082 preamp is nearly 2 GHz, thus good bypassing of the supply voltage is necessary; a 3.3 μF tantalum capacitor in parallel with a 0.01 μF ceramic disc is recommended, placed as close as possible to the device pins.

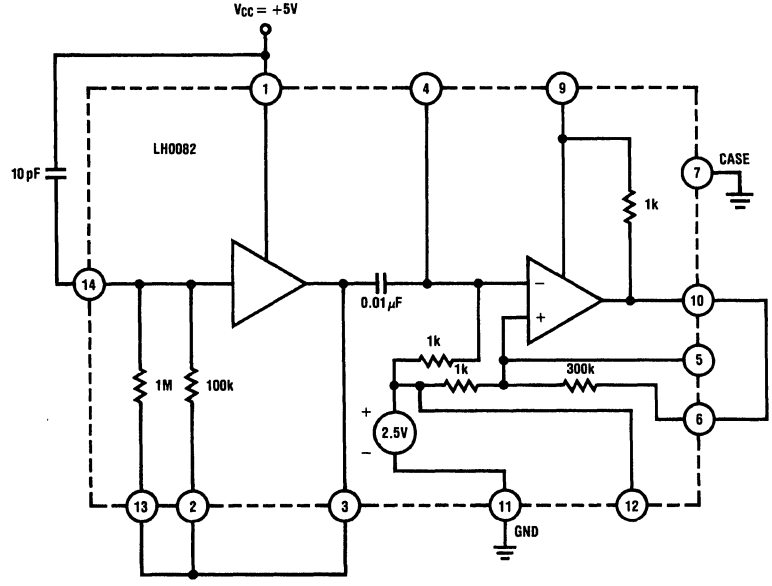
Careful shielding of pins 2, 13 and 14 is necessary if the LH0082 is used in a high noise environment. Minimize stray capacitance to pin 14 from ground, V_{CC} or pin 3 to avoid slowing overall circuit response. Choose the lowest capacitance photodiode possible for the application. When using phototransistors, only the collector-base junction should be used for fastest response. Additional sensitivity may be gained by using a phototransistor in the transistor mode, although this will result in slower circuit response, and poor DC stability due to beta multiplication of the dark current of the phototransistor. Avoid capacitive loading at the output of the comparator to achieve maximum data rates.

Avalanche photodiodes can be used for improved sensitivity and speed. Overall speed is limited by the internal comparator. Use of an external comparator such as the LM160 will enable the full speed capability to be realized. This requires the use of an additional power supply, see *Figure 5*.

For operations at higher data rates, *Figure 5* shows the use of an external comparator to enable speeds to 50 Mbit NRZ. *Figure 6, 7* and *8* demonstrate interfacing techniques to avalanche photodiodes and phototransistors.

With a few additional components, the LH0082 can be used as a repeater as shown in *Figure 9*. Interfacing to a microcomputer-bus, (*Figure 10*), is also easy when the LH0082 is teamed with an INS8250 Asynchronous Communications Element. This provides a full duplex link capable of bit rates to 56 kbits/s NRZ.

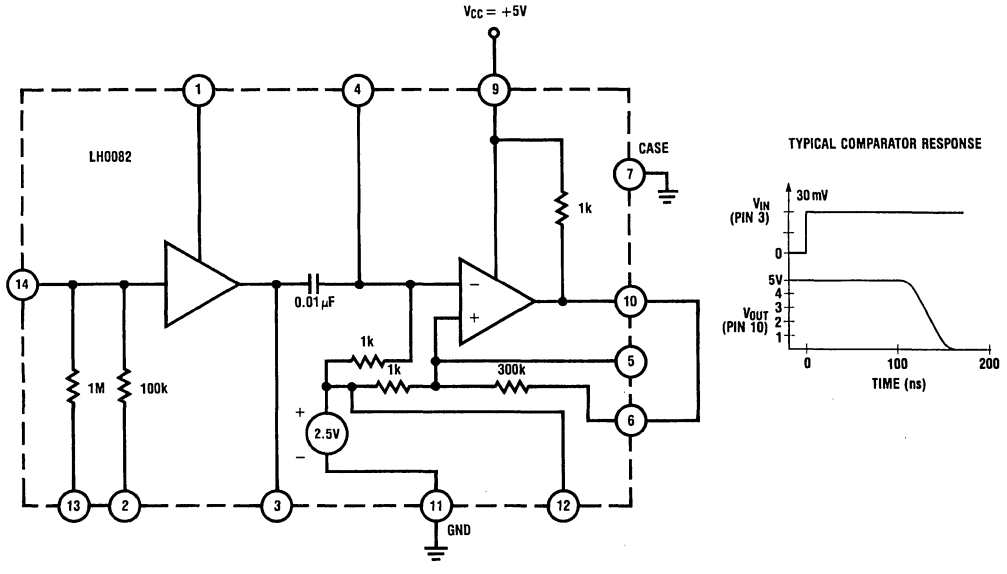
Analog data can be sent along a fiber-optic cable via digital means, (*Figure 11*). Low temperature drift can be obtained in the analog mode, by using the circuit shown in *Figure 12*.



TL/H/9325-10

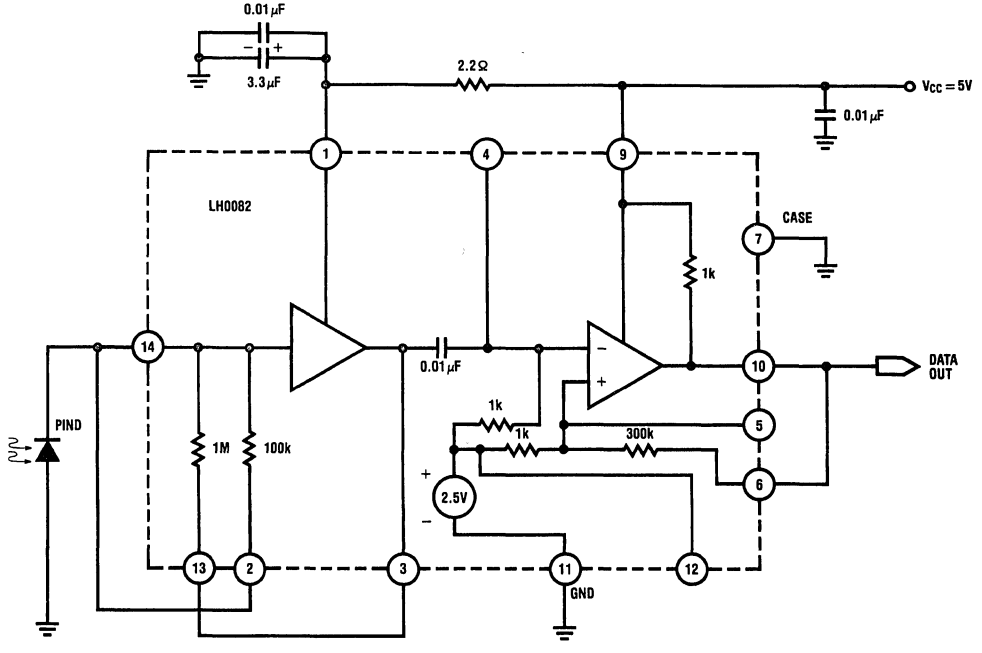
FIGURE 1. Preamp Test Circuit

Applications Information (Continued)



TL/H/9325–11

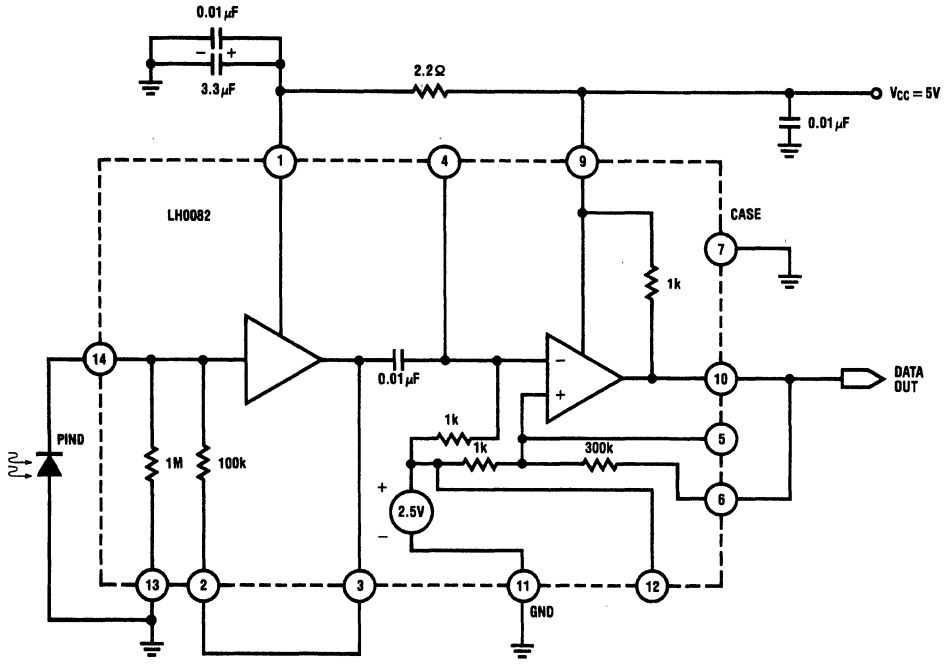
FIGURE 2. Comparator Test Circuit



TL/H/9325–12

FIGURE 3. Fiber-Optic Receiver, Basic High Sensitivity: 150 nW, 400 kbps NRZ

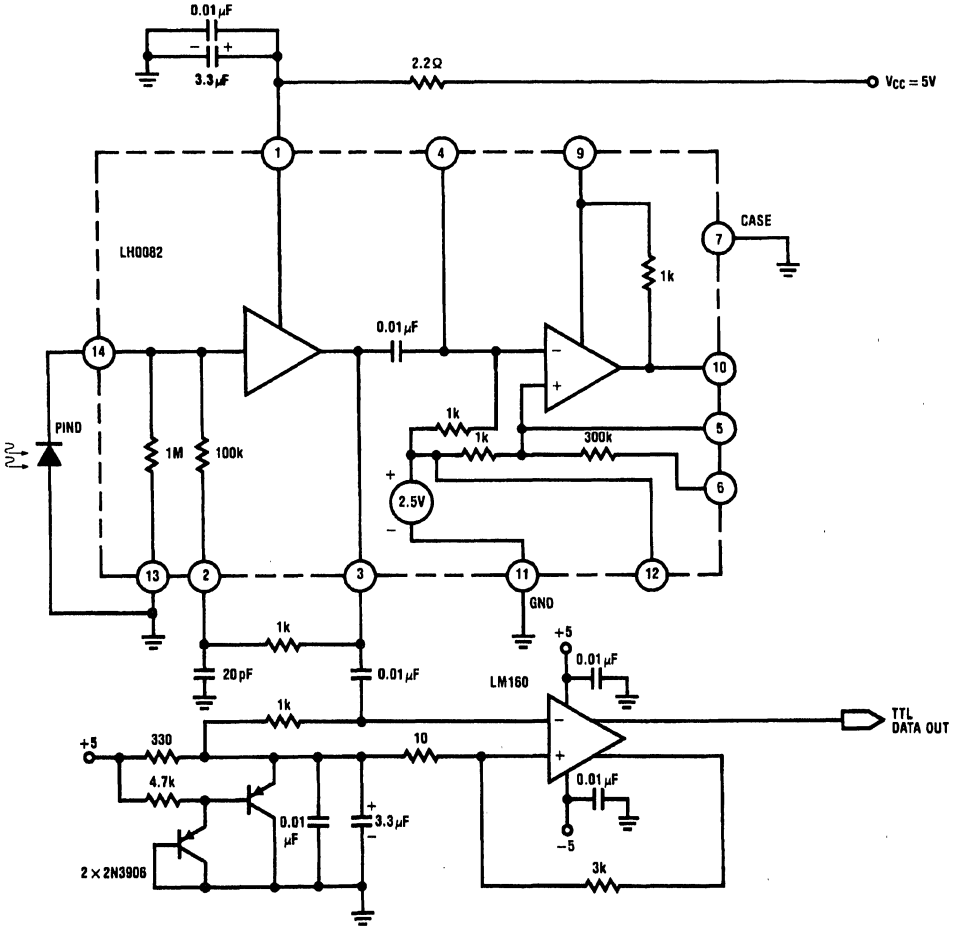
Applications Information (Continued)



TL/H/9325–13

FIGURE 4. Fiber-Optic Receiver, Basic Low Sensitivity: 2 μW, 5 Mbit, NRZ

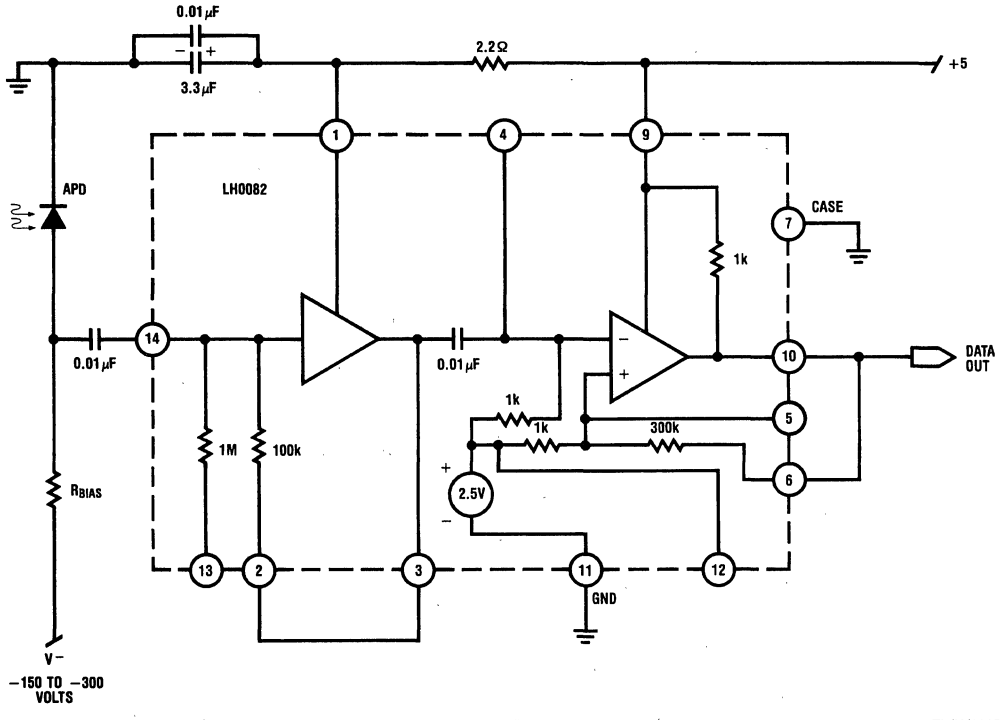
Applications Information (Continued)



TL/H/9325–14

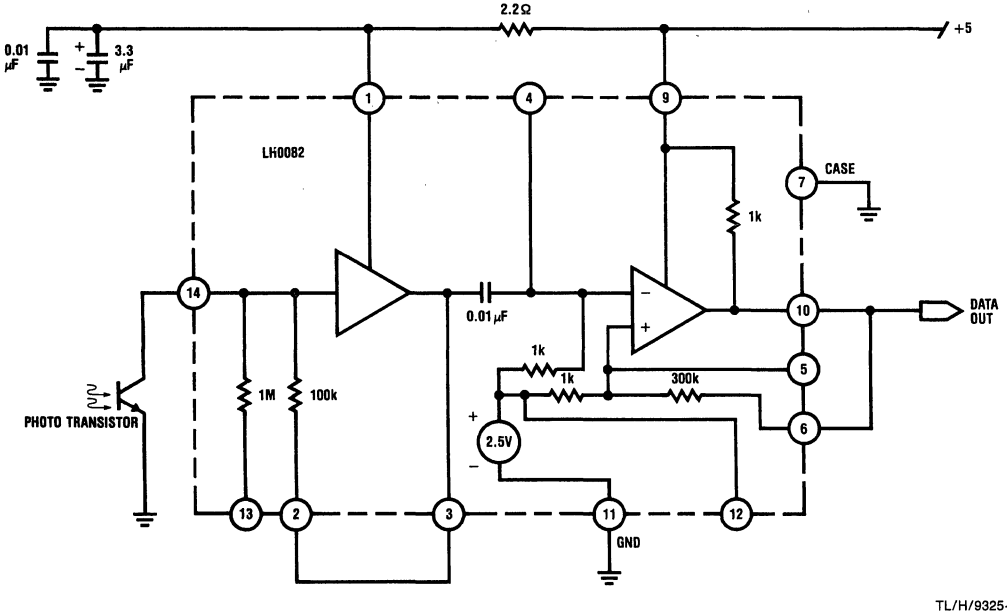
FIGURE 5. High Speed—Low Sensitivity Receiver

Applications Information (Continued)



TL/H/9325–15

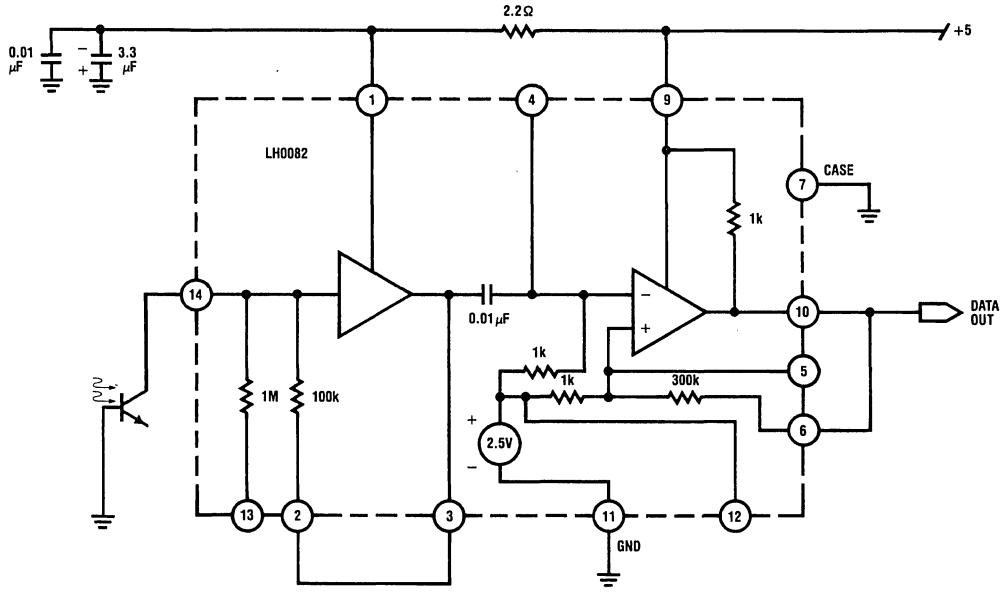
FIGURE 6. Connection to Avalanche Photodiode



TL/H/9325–16

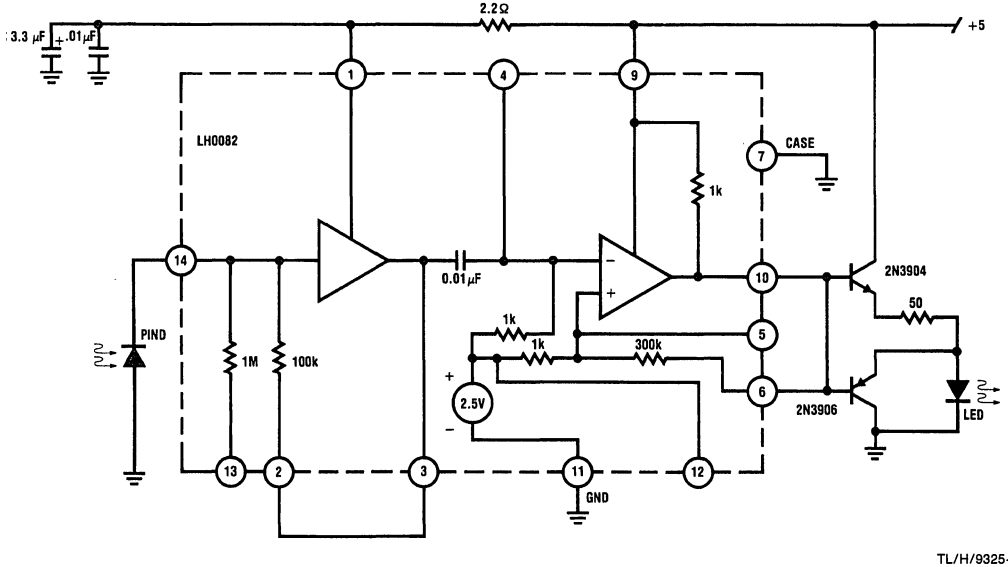
FIGURE 7. Connection to Phototransistor—High Sensitivity, Low Speed

Applications Information (Continued)



TL/H/9325–17

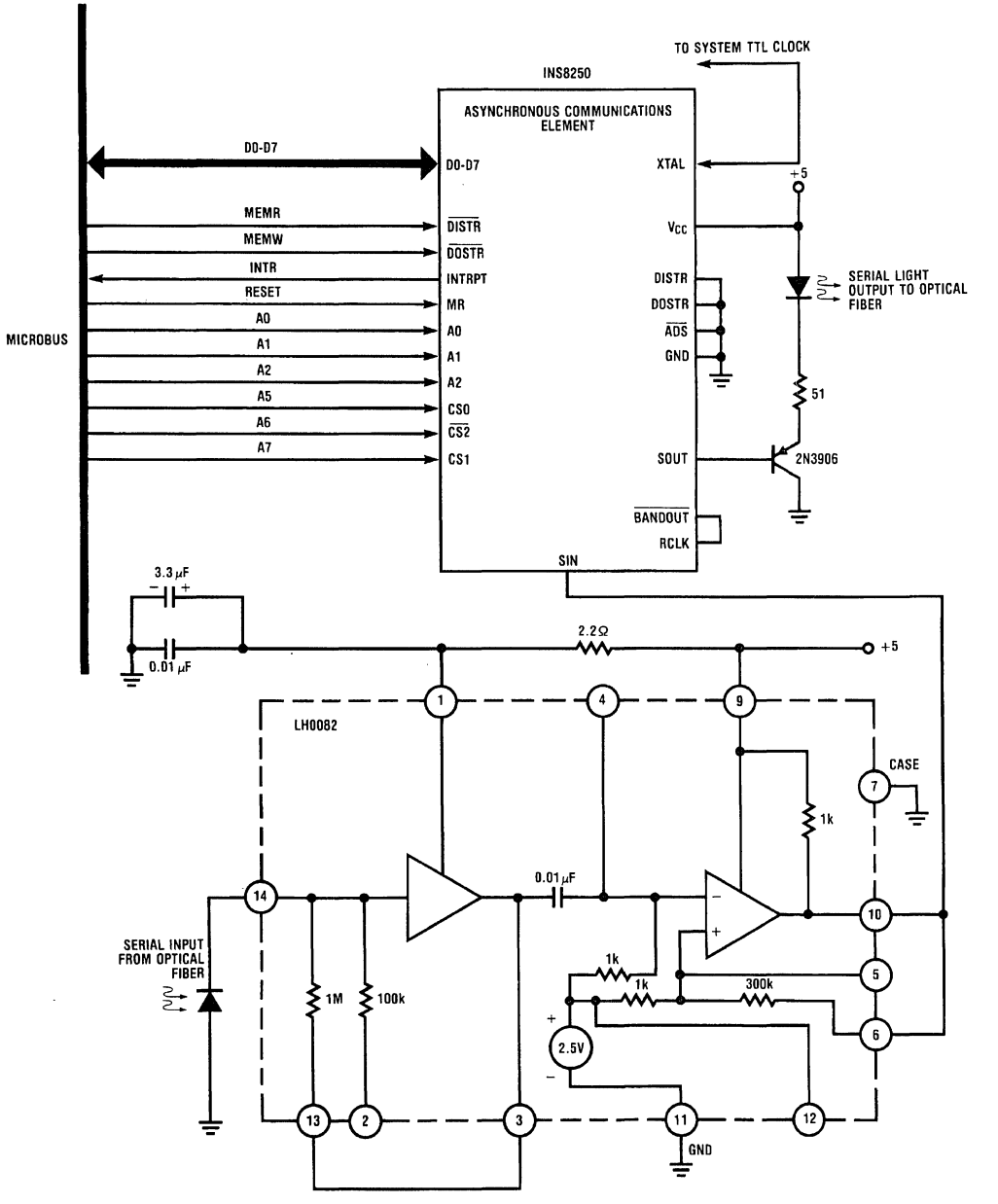
FIGURE 8. Connection to Phototransistor—Low Sensitivity, High Speed Receiver



TL/H/9325–18

FIGURE 9. Fiber-Optic Link Repeater

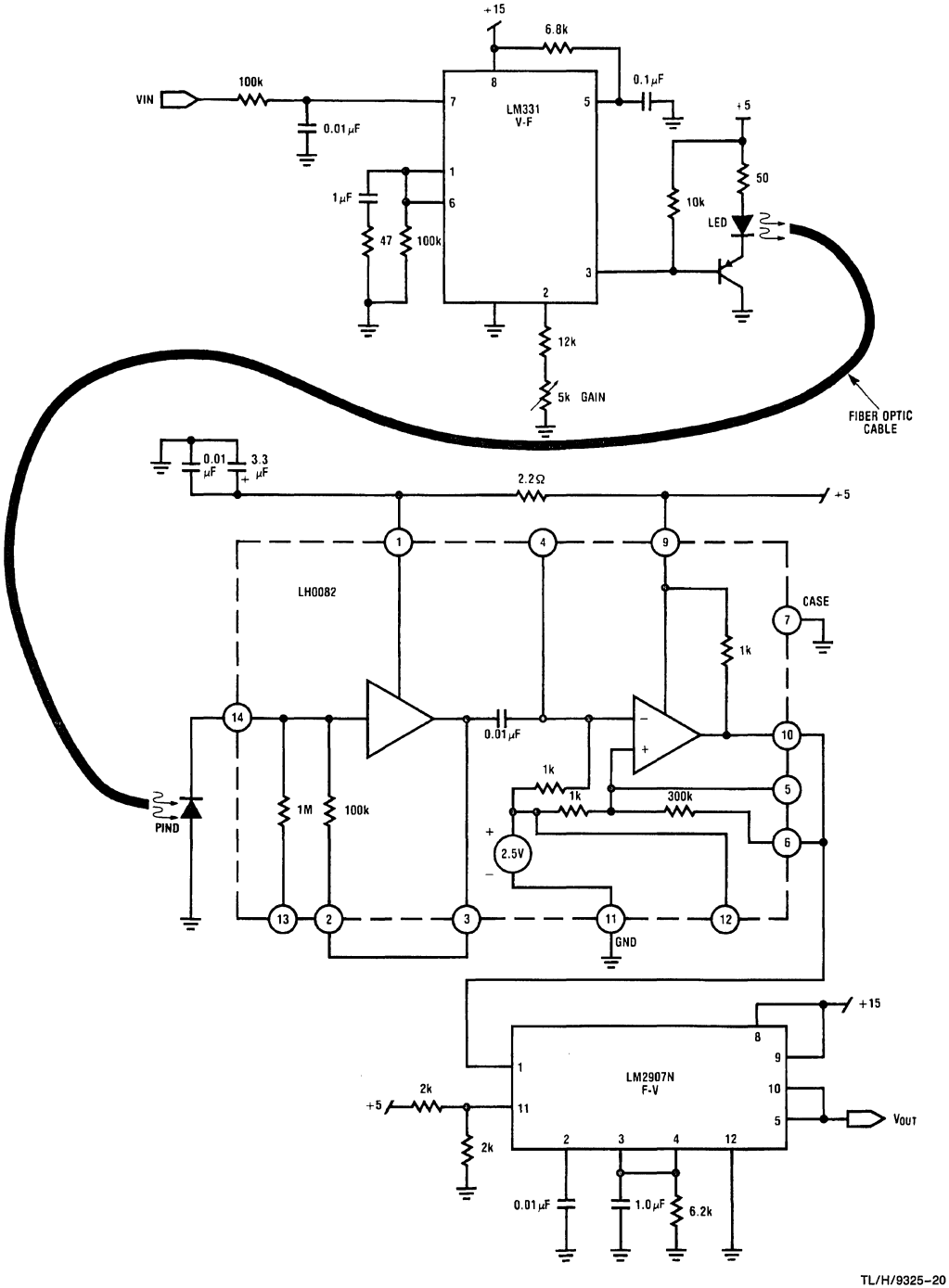
Applications Information (Continued)



TL/H/9325–19

FIGURE 10. Optical Link to Microbus

Applications Information (Continued)

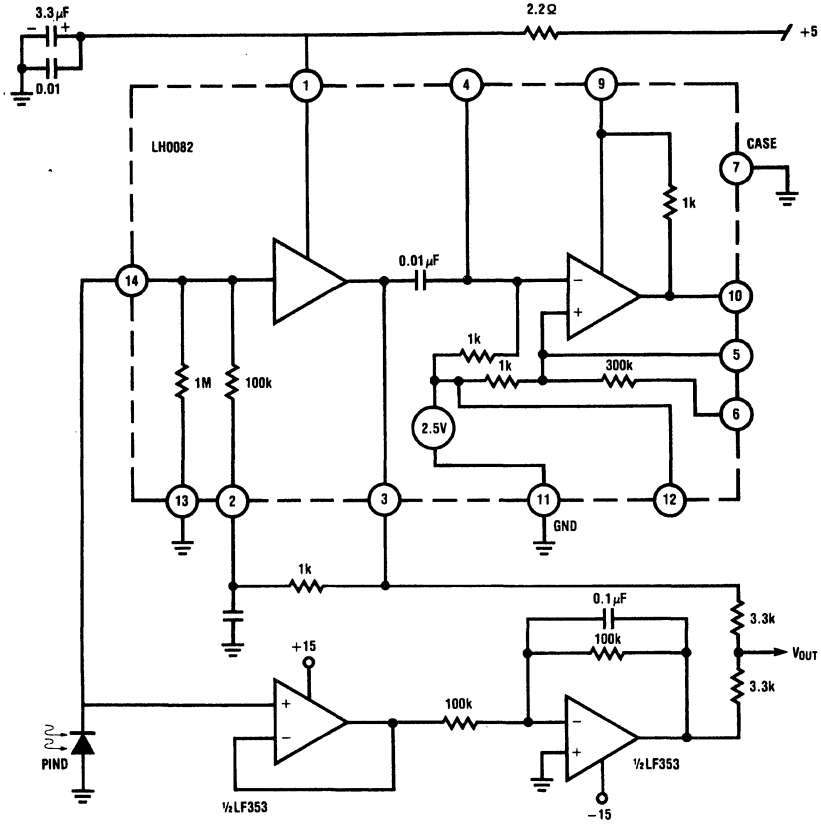


TL/H/9325–20

FIGURE 11. Analog Data Link Using V/F and F/V

3

Applications Information (Continued)

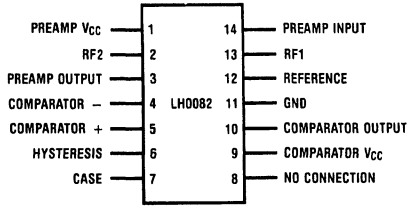


TL/H/9325-21

FIGURE 12. Low Temperature Drift Analog Receiver

Connection Diagram

Dual-In-Line Package



TL/H/9325-2

Top View

Order Number LH0082CD
See NS Package Number D14F

National Semiconductor

LH0086/LH0086C
Digitally-Programmable-Gain Amplifier

General Description

The LH0086 is a self-contained, high-accuracy, digitally-programmable-gain amplifier. It consists of a FET-input operational amplifier, a precision resistor ladder, and a digitally-programmable switch network. A three-bit TTL-compatible digital input selects accurate gain settings of 1, 2, 5, 10, 20, 50, 100, or 200.

The LH0086 exhibits low offset voltage, high input impedance, fast settling, high power supply rejection ratio, and excellent gain accuracy and gain non-linearity.

The LH0086 is specified for operation from −55°C to +125°C. The LH0086C is specified from −25°C to +85°C. Both devices are hermetically sealed in a 14-lead dual-in-line metal package.

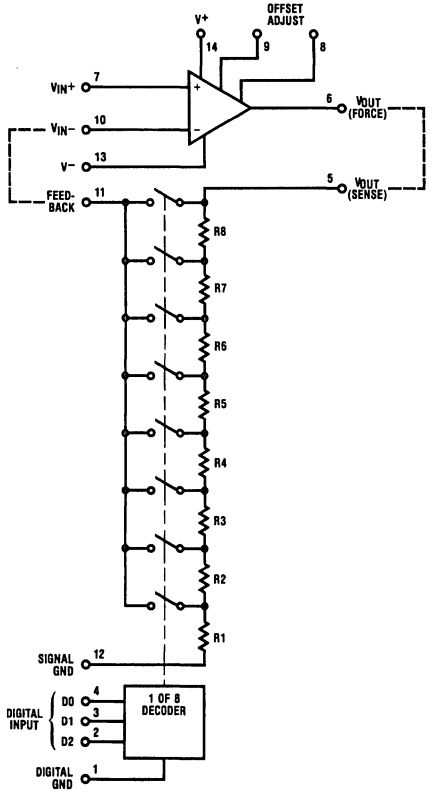
Features

- 0.01% maximum gain accuracy at gain = 1
- 0.005% typical gain non-linearity
- 1 ppm/°C typical gain drift
- $10^{10}\Omega$ input impedance
- 80 dB minimum PSRR.
- TTL-compatible digital inputs
- 2 μs settling to 0.01%

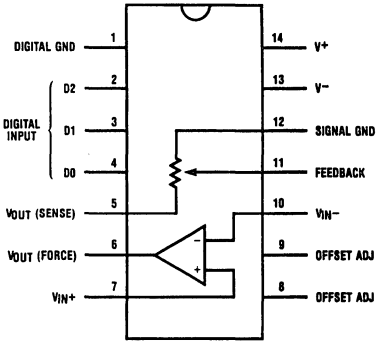
Applications

- Data acquisition systems
- Auto range DVMs
- Adaptive servo loops

Simplified Schematic and Connection Diagrams



Dual-In-Line Package



Top View

CASE IS ELECTRICALLY ISOLATED

Order Number LH0086D or LH0086CD
See NS Package Number D14F

TL/K/5657–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

V_S	Supply Voltage (Note 1)	±18V
V_{IN}	Analog Input Voltage (Note 2)	±15V
$V_{IL(H)}$	Digital Input Voltage	−4V, $+V_S$
P_D	Power Dissipation	500 mW
	Output Short Circuit Duration	Continuous

T_A	Operating Temperature Range:	
	LH0086	−55°C to +125°C
	LH0086C	−25°C to +85°C
T_{STG}	Storage Temperature	−65°C to +150°C
	Lead Temperature (Soldering, 10 seconds)	+300°C

ESD rating to be determined.

DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting)

Symbol	Parameter	Conditions		LH0086			LH0086C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage		$T_J = 25°C$		0.3	5.0		0.3	10	mV
						7.0			13	
$V_{OS}/\Delta T$	Input Offset Voltage Change with Temperature	$V_{IN} = 0V$			10			10		µV/°C
I_B	Input Bias Current	(Notes 3, 4)	$T_J = 25°C$		100	500		100	500	pA
						500			100	nA
R_{IN}	Input Resistance				10			10		GΩ
V_{IN}	Input Voltage Range			±10	±11.5		±10	±11.5		V
A_V	Voltage Gain	See Table 1 for Digital Gain-Control Codes			1.0			1.0		V/V
					2.0			2.0		
					5.0			5.0		
					10			10		
					20			20		
					50			50		
					100			100		
					200			200		
	Gain Error	$A_V = 1$ $A_V = 2,5$ $A_V = 10,20$ $A_V = 50,100,200$	$T_A = 25°C$		0.003 0.03 0.05 0.1	0.01 0.05 0.1 0.3		0.003 0.05 0.1 0.15	0.03 0.1 0.2 0.4	%
		$A_V = 1$ $A_V = 2,5$ $A_V = 10,20$ $A_V = 50,100,200$			0.003 0.03 0.1 0.15	0.02 0.1 0.2 0.4		0.003 0.05 0.1 0.15	0.06 0.2 0.3 0.5	
	Gain Non-Linearity	$A_V = 1$	$T_A = 25°C$		0.002			0.002		%
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient	$A_V = 1$			1.0			1.0		ppm/°C
PSRR	Power Supply Rejection Ratio	$\pm 8V \leq V_S \leq \pm 18V$		80	90		70	90		dB
V_O	Output Voltage Swing	$R_L \geq 10\ k\Omega$		±10	±12		±10	±12		V

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection Section under Applications Information.

Note 2: for supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: Due to short production test time, these parameters are specified at junction temperature, $T_J = 25°C$. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of the internal power dissipation, PD. $T_J = T_A + \theta_{JA} \times PD$ where θ_{JA} is the thermal resistance from junction to ambient (typically 65°C/W).

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

Note 5: Refer to RETS0086D for LH0086D military specifications.

DC Electrical Characteristics (Continued)

$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-inverting).

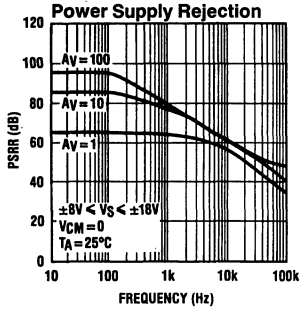
Symbol	Parameter	Conditions		LH0086			LH0086C			Units
				Min	Typ	Max	Min	Typ	Max	
I_{SC}	Output Short-Circuit Current		$T_A = 25°C$	±5	±18	±40	±5	±18	±40	mA
				±2		±40	±2		±40	
R_O	Output Resistance	$A_{VCL} = 1$			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage					0.7			0.7	V
V_{IH}	Digital "1" Input Voltage			2.0			2.0			
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$			1.5	4.0		1.5	4.0	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$			0.01			0.01		
V_S	Supply Voltage Range			±8.0		±18	±8.0		±18	V
$I_S(+)$	Positive Supply Current	$V_S = \pm 18V$			8.5	15.5		8.5	15.5	mA
$I_S(-)$	Negative Supply Current				−4.5	−8.5		−4.5	−8.5	

AC Electrical Characteristics

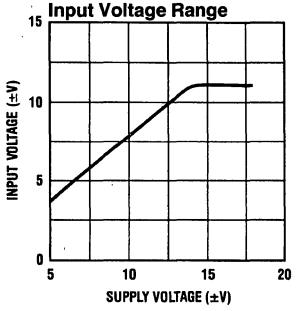
$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$, Pin 10 connected to Pin 11, Pin 5 connected to Pin 6 (Non-Inverting)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
BW	Small Signal Bandwidth	−3 dB	$A_V = 1$		3000		kHz
			$A_V = 50$		60		
			$A_V = 200$		15		
		−1%	$A_V = 1$		425		
			$A_V = 50$		8.5		
			$A_V = 200$		2		
PBW	Power Bandwidth	$V_O = \pm 10V$			159		kHz
SR	Slew Rate				10		V/μs
t_S	Settling Time (*Figure 7*) 0.01%	$\Delta V_O = 20V$	$A_V = 1$		2.5		μs
			$A_V = 50$		20		μs
			$A_V = 200$		75		μs
t_S	Settling Time After Gain Change				10		
$\bar{e}_N$	Equivalent Input Noise Voltage (*Figure 6*)	$R_S = 100\Omega$ $A_V = 100$	BW = 0.1-10 Hz		3		μVp-p
			f = 1 kHz		25		$nV/\sqrt{Hz}$
$\bar{i}_N$	Equivalent Input Noise Current				0.01		$pA/\sqrt{Hz}$

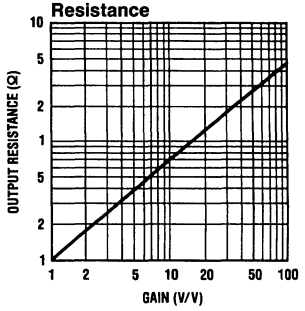
Power Supply Rejection



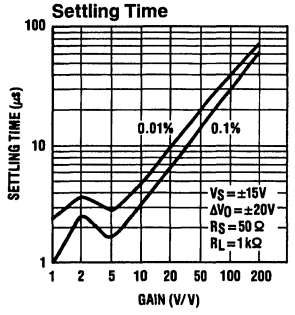
Input Voltage Range



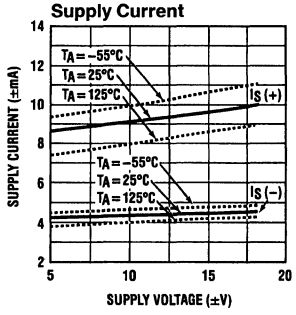
Closed Loop Output Resistance



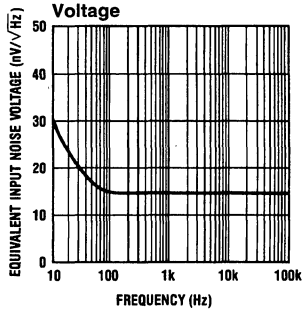
Settling Time



Supply Current

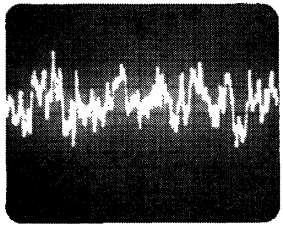


Equivalent Input Noise Voltage



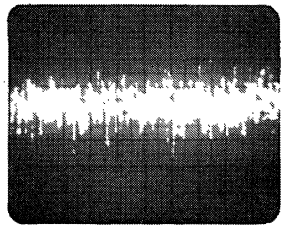
TL/K/5657–2

Wideband Noise



TL/K/5657–3

R_S = 50Ω. Bandwidth = 0.1 Hz to 10 Hz
1 μV/division Vertical, 5 seconds/division Horizontal



TL/K/5657–4

R_S = 50Ω. Bandwidth = 10 Hz to 10 kHz
5 μV/division Vertical, 1 ms/division Horizontal

Applications Information

Theory of Operation

The LH0086 is a digitally programmable gain amplifier with 3-bit digital gain control. It contains a FET-input operational amplifier, a precision resistor ladder, and a digitally programmable switch network.

The LH0086 was designed for use in a non-inverting configuration, thus the following discussion covers the LH0086 as used as a non-inverting amplifier. The gain of the LH0086 is given by the familiar gain equation of a non-inverting amplifier.

$$A_V = 1 + \frac{R_F}{R_S}$$

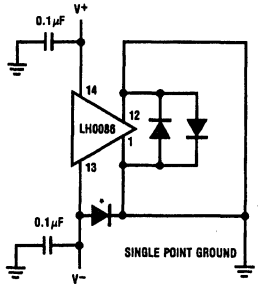
Each gain step is set by the ratio of the ladder resistors. The resistor ladder is constructed with high stability, low temperature-coefficient resistors precision laser-trimmed to the required values. FET switches are used to select the desired ratio. Since the FET switches are in series with the operational amplifier input, their "on resistance" and temperature drift do not degrade amplifier accuracy. The FET switches are selected by a 1 of 8 decoder, by applying the proper logic levels at digital inputs D0, D1, and D2. The gains are set as given in Table I.

TABLE I. Gain-Control Codes

Gain	D2	D1	D0
1	0	0	0
2	0	0	1
5	0	1	0
10	0	1	1
20	1	0	0
50	1	0	1
100	1	1	0
200	1	1	1

Power Supply Connection

Proper power supply connections are shown in *Figure 1*. The power supplies should be bypassed to ground as close as possible to device supply pins. For most applications, the bypass capacitor should be 0.1 μF.



*GERMANIUM OR SCHOTTKY

FIGURE 1. Power Supply and Ground Connections

Care must be taken in the power-on sequence. The LH0086 may suffer irreversible damage if the V^+ supply is applied prior to the powering on of the V^- supply. In most applications using dual-tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V^- pin as shown in *Figure 1*.

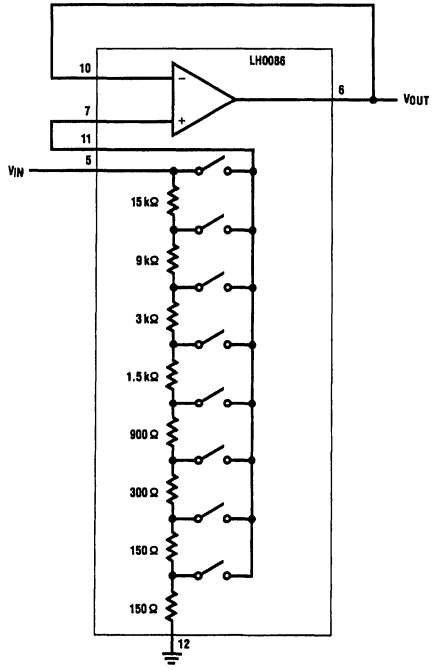
Grounding Considerations

Care should be taken in the connection of digital and analog grounds. Digital switching currents can introduce noise on the analog ground pin. If possible, both grounds should go to a ground plane beneath the device, otherwise each ground should be run separately to a single point ground. The idea is to keep digital current from passing through the analog ground line. If long ground leads are used, diode clamps should be placed as close to the device as possible (*Figure 1*).

Programmable Attenuator

The LH0086 may be used as a programmable attenuator when connected as in *Figure 2*. The accuracy of this attenuator will be typically 0.1%.

Note: Max. $V_{IN} = \pm 11$ Volts.



TL/K/5657–5

FIGURE 2. Programmable Attenuator

Applications Information (Continued)

TABLE II. Attenuator Codes

D2	D1	D0	Attenuation
0	0	0	1
0	0	1	2
0	1	0	5
0	1	1	10
1	0	0	20
1	0	1	50
1	1	0	100
1	1	1	200

TABLE III. Inverting Gain Chart

D2	D1	D0	Gain	R_{IN} (Ω)
0	0	0	$A_V=0$	30k
0	0	1	$A_V=1$	15k
0	1	0	$A_V=4$	6k
0	1	1	$A_V=9$	3k
1	0	0	$A_V=19$	1.5k
1	0	1	$A_V=49$	600
1	1	0	$A_V=99$	300
1	1	1	$A_V=199$	150

Inverting Mode

The LH0086 may be used in the inverting mode, however, there are several design considerations.

1. Input resistance is low at high gains (see gain chart for input resistance at each gain).
2. Each gain step gets a one subtracted from the non-inverting gain. (See inverting gain chart for available gains.)
3. The first gain step (digital code of 000) cannot be used because the output will remain at virtual ground regardless of the input.

Remote Output Sense

The V_{OUT} sense pin of the LH0086 should be connected at the load in order to eliminate errors due to lead resistance. In any case the output sense and output force must be tied together at some point. See *Figure 4*.

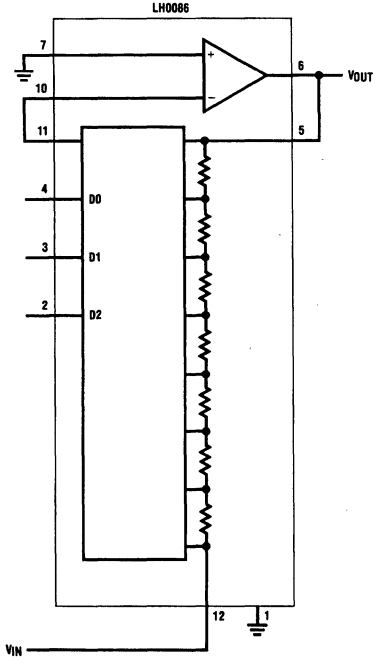


FIGURE 3. LH0086 Inverting Gain Configuration

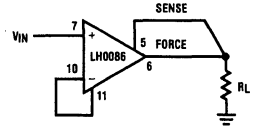


FIGURE 4. Remote Output Sense

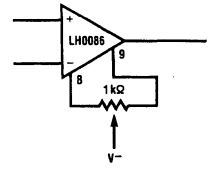


FIGURE 5. Offset Adjustment

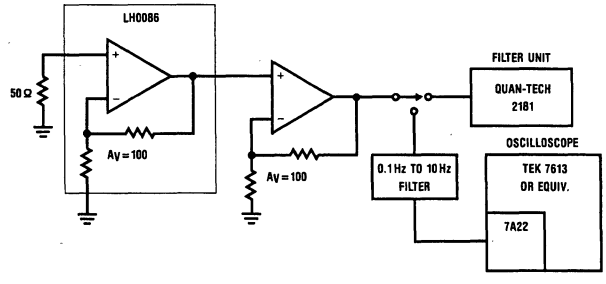
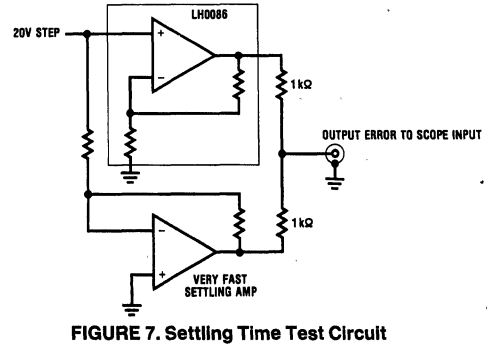


FIGURE 6. Noise Measurement Circuit



TL/K/5657–6

FIGURE 7. Settling Time Test Circuit

Definition of Terms

V_{OS} **Offset Voltage:** The voltage that must be applied to force the output to 0 volts.

I_B **Input Bias Current:** The current into Pin 7 with the device connected in the non-inverting configuration.

R_{IN} **Input Resistance:** The ratio of the change in input voltage to the change in input current on either input with the other grounded.

V_{IN} **Input Voltage Range:** The voltage range for which the device is operational.

PSRR **Power Supply Rejection Ratio:** The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

A_V **Voltage Gain:** The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full scale (10V for operation with ±15V supplies). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

V_O **Output Voltage Swing:** The peak output voltage swing referenced to ground into specified load.

$I_{O(SC)}$ **Output Short-Circuit Current:** The current supplied by the device with the output connected directly to ground.

R_O **Closed Loop Output Resistance:** The ratio of change in output voltage to change to output current at a specific gain.

V_S **Supply Voltage Range:** The supply voltage range for which the device is operational.

I_S **Supply Current:** The current required from the supply to operate the device with no load and with the analog as well as the digital inputs at 0V.

P_D **Power Dissipation:** The power dissipated in the device with no load and with the analog as well as the digital inputs at 0V.

V_{IH} **Digital "1" Input Voltage:** Minimum voltage required at the digital input to guarantee a high logic state.

V_{IL} **Digital "0" Input Voltage:** The current into a digital input at specified logic level.

$\Delta V_{OS}/\Delta T$ **Average Input Offset Voltage Drift:** The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

$\Delta A_V/\Delta T$ **Average Gain Temperature Coefficient:** The ratio in gain from 25°C to either temperature extreme divided by the temperature range.

BW **Bandwidth:** The frequency at which the voltage gain is reduced to 3 dB below the low frequency value.

PBW **Power Bandwidth:** Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

SR **Slew Rate:** The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

t_S **Settling Time:** The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

e_N **Equivalent Input Noise Voltage:** The rms or peak noise voltage referred to the input (RTI) over a specified frequency band.

i_N **Equivalent Input Noise Current:** The rms or peak noise current referred to the input (RTI) over a specified frequency band.

National Semiconductor

LH0101/LH0101C, LH0101A/LH0101AC Power Operational Amplifier

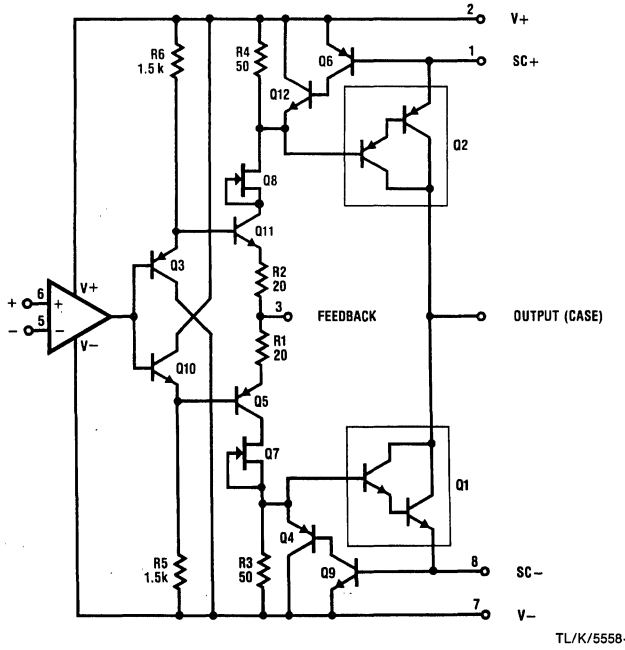
General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 60 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μs slew rate
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams



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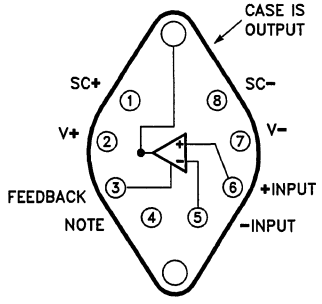


TL/K/5558-2

Top View

Order Numbers LH0101K, LH0101CK, LH0101AK or LH0101ACK
See NS Package Number K08A

Note: Electrically connected internally, no connection should be made to pin.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage, V_S ±22V

Power Dissipation at $T_A = 25°C$, P_D 5W
Derate linearly at 25°C/W to zero at 150°C,

Power Dissipation at $T_C = 25°C$ 62W
Derate linearly at 2°C/W to zero at 150°C

Differential Input Voltage, V_{IN} ±40V but < $\pm V_S$

Input Voltage Range, V_{CM} ±20V but < $\pm V_S$

Thermal Resistance—
See Typical Performance Characteristics

Peak Output Current (50 ms pulse), $I_{O(PK)}$ 5A

Output Short Circuit Duration
(within rated power dissipation,
$R_{SC} = 0.35\Omega$, $T_A = 25°C$) Continuous

Operating Temperature Range, T_A
LH0101AC, LH0101C −25°C to +85°C
LH0101A, LH0101 −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_J 150°C

Lead Temperature (Soldering <10 sec.) 260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions			LH0101AC LH0101A			LH0101C LH0101			Units
					Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage					1	3		5	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$					7			15	
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with Dissipated Power	(Note 2)				150			300		µV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with Temperature	$V_{CM} = 0$				10			10		µV/°C
I_B	Input Bias Current						300			1000	pA
			$T_A \le T_{MAX}$	LH0101C/AC			60			60	nA
				LH0101/A			300			1000	
I_{OS}	Input Offset Current						75			250	pA
			$T_A \le T_{MAX}$	LH0101C/AC			15			15	nA
				LH0101/A			75			250	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 10\Omega$			50	200		50	200		V/mV
V_O	Output Voltage Swing	$R_{SC} = 0$	$R_L = 100\Omega$		±12	±12.5		±12	±12.5		V
		$A_V = +1$	$R_L = 10\Omega$		±11.25	±11.6		±11.25	±11.6		
		Note 3	$R_L = 5\Omega$		±10.5	±11		±10.5	±11		
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$			85	100		85	100		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 5V$ to $\pm 15V$			85	100		85	100		
I_S	Quiescent Supply Current					28	35		28	35	mA

3

AC Electrical Characteristics (Note 1), $V_S = \pm 15V$, $T_A = 25°C$

Symbol	Parameter	Conditions		LH0101 LH0101A			LH0101C LH0101AC			Units
				Min	Typ	Max	Min	Typ	Max	
e_n	Equivalent Input Noise Voltage	f = 1 kHz			25			25		$nV\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 1 MHz			3.0			3.0		pF
	Power Bandwidth, −3 dB	$R_L = 10\Omega$	$A_V = +1$		300			300		kHz
SR	Slew Rate			7.5 (Note 4)	10			10		V/μs
t_r, t_f	Small Signal Rise or Fall Time				200			200		ns
	Small Signal Overshoot				10			10		%
GBW	Gain-Bandwidth Product	$R_L = \infty$		4.0 (Note 4)	5.0			5.0		MHz
t_s	Large Signal Settling Time to 0.01%				2.0			2.0		μs
THD	Total Harmonic Distortion	$P_O = 10W$, f = 1 kHz $R_L = 10\Omega$			0.008			0.008		%

Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

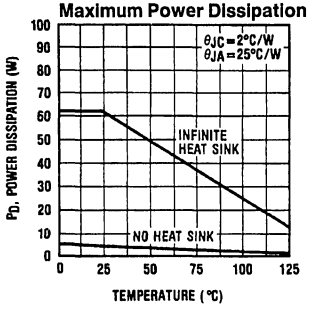
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

Note 4: These parameters are sample tested to 10% LTPD.

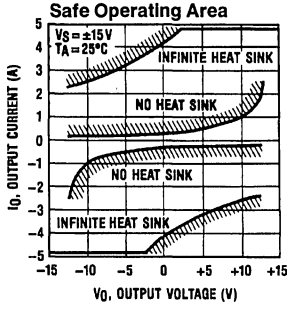
Note 5: Refer to RETS0101AK for the LH0101AK military specifications and RETS0101K for the LH0101K military specifications.

Typical Performance Characteristics

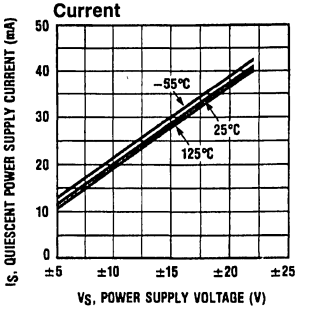
Maximum Power Dissipation



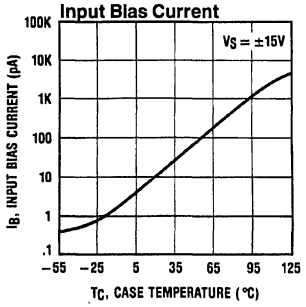
Safe Operating Area



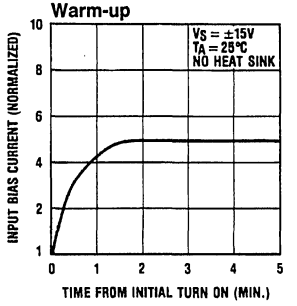
Quiescent Power Supply Current



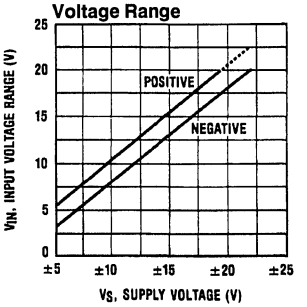
Input Bias Current



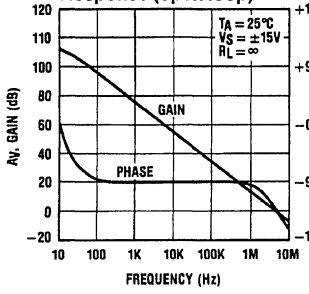
Input Bias Current after Warm-up



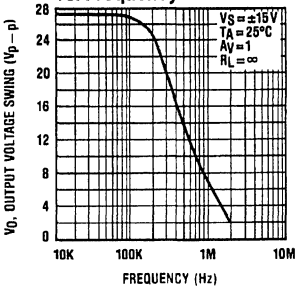
Input Common-Mode Voltage Range



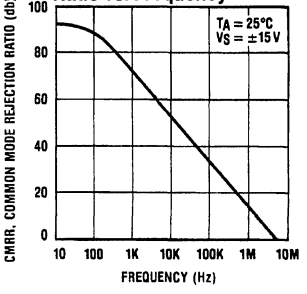
Small Signal Frequency Response (open loop)



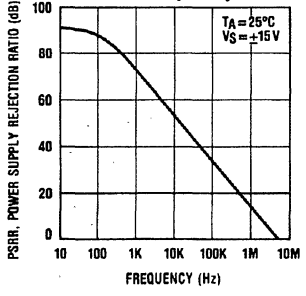
Output Voltage Swing vs. Frequency



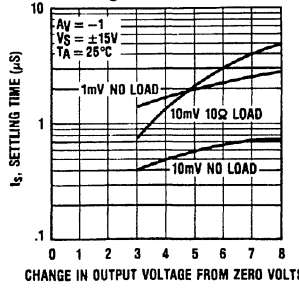
Common-Mode Rejection Ratio vs. Frequency



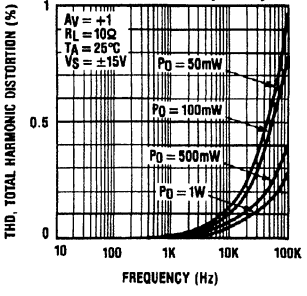
Power Supply Rejection Ratio vs. Frequency



Settling Time



Total Harmonic Distortion vs. Frequency



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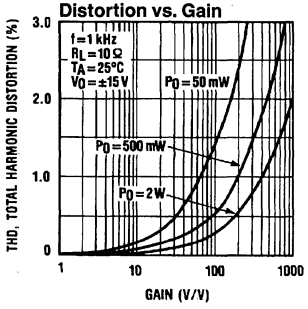
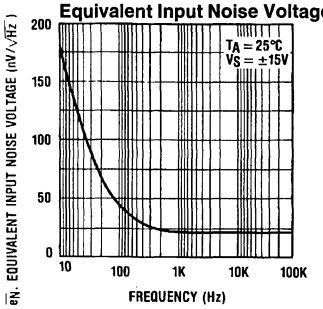
3

Typical Performance Characteristics (Continued)

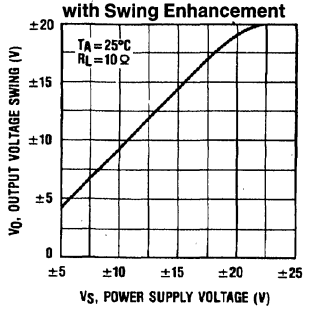
Total Harmonic Distortion vs. Gain



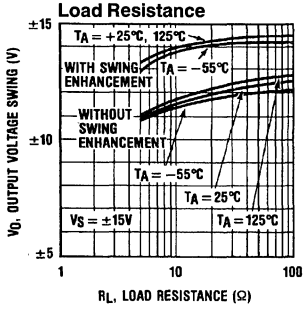
Equivalent Input Noise Voltage



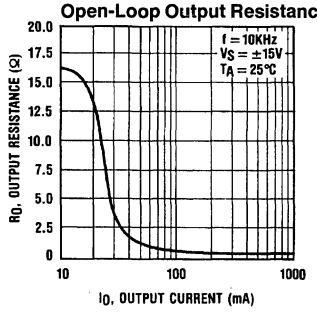
Output Voltage Swing with Swing Enhancement



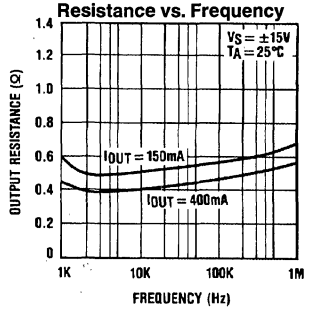
Output Voltage Swing vs. Load Resistance



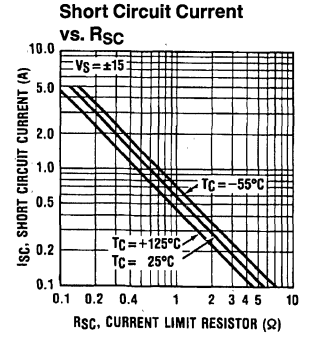
Open-Loop Output Resistance



Open-Loop Output Resistance vs. Frequency



Short Circuit Current vs. R_{SC}



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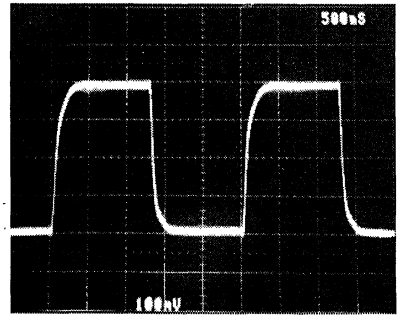
Small Signal Pulse Response (No Load)



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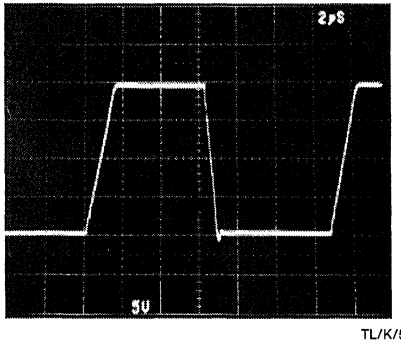
Large Signal Pulse Response (R_L = 10Ω)



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Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

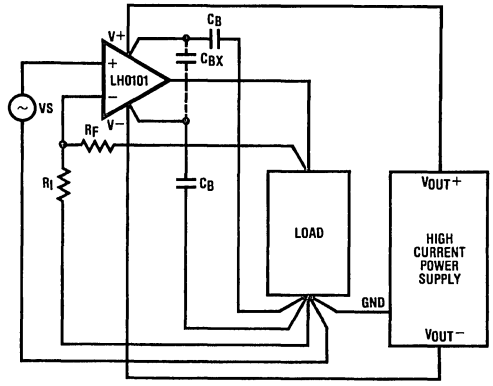
The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



TL/K/5558–7

FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately .3%.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

Application Hints (Continued)

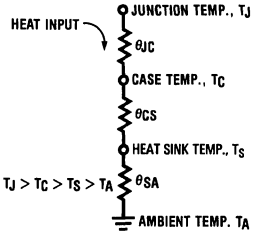
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} °C/W$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J, T_C and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.



TL/K/5558–8

FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions.

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} °C/W$$

$$T_J = T_A + P_D\theta_{JA} °C$$

Where: P_D $(V_S - V_{OUT})I_{OUT} + |V+ - (V-)|I_Q$ for a DC Signal

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and V_S = Supply Voltage

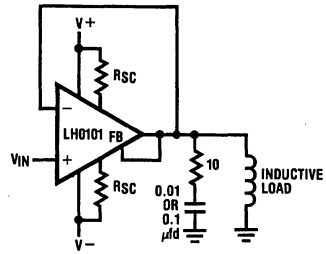
θ_{JC} for the LH0101 is about 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

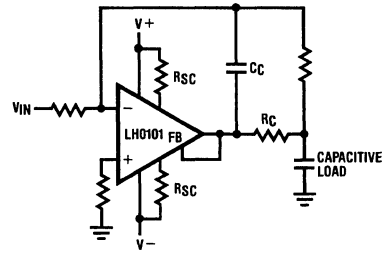
Some inductive loads may cause output stage oscillation. A .01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.



TL/K/5558–9

FIGURE 3. Driving Inductive Loads

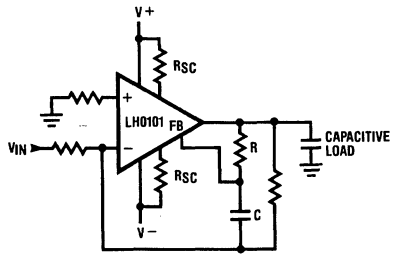
Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):



TL/K/5558–10

FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:



TL/K/5558–11

FIGURE 5. Alternate Compensation for Capacitive Load

Application Hints (Continued)

Output Swing Enhancement

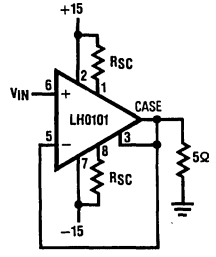
When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under on Ω for load currents exceeding 100 mA.

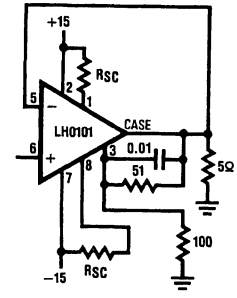
Typical Applications

See AN261 for more information.



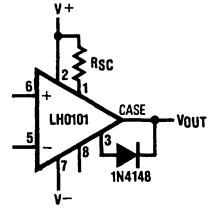
TL/K/5558–12

FIGURE 6. High Power Voltage Follower



TL/K/5558–13

FIGURE 7. High Power Voltage Follower with Swing Enhancement



TL/K/5558–14

FIGURE 8. Restricting Outputs to Positive Voltages Only

Following is a partial list of sockets and heat dissipators for use with the LH0101. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS

Keystone 4626 or 4627
Robinson Nugent 0002011
Azimuth 6028 (test socket)

HEAT SINKS

Thermalloy 2266B (35°C/W)
IERC LAIC3B4CB
IERC HP1-TO3-33CB (7°C/W)
AAVID 5791B

MICA WASHERS

Keystone 4658

AAVID Engineering
30 Cook Court
Laconla, New Hampshire 03246

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92572

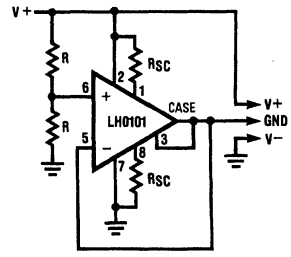
IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150

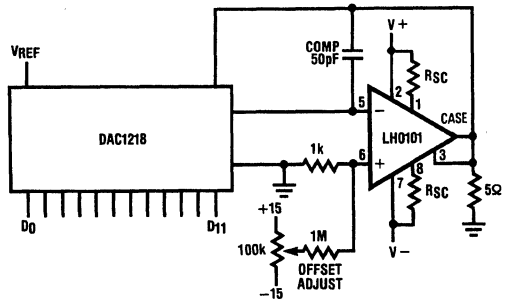
Thermalloy
P.O. Box 34829
Dallas, TX 75234

Typical Applications (Continued)



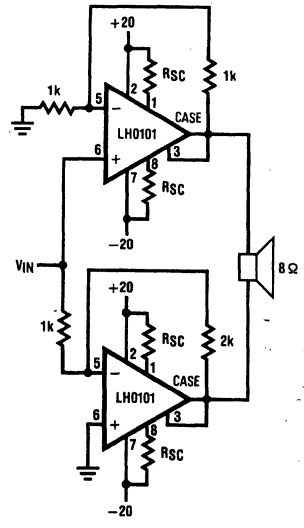
TL/K/5558–15

FIGURE 9. Generating a Split Supply from a Single Voltage Supply



TL/K/5558–16

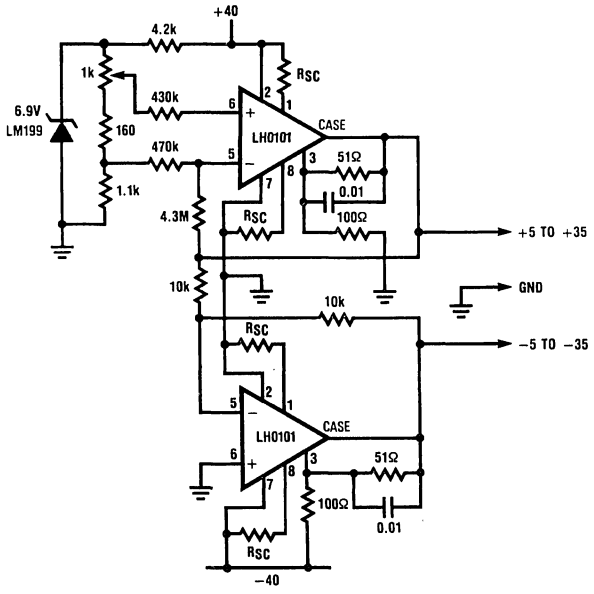
FIGURE 10. Power DAC



TL/K/5558–17

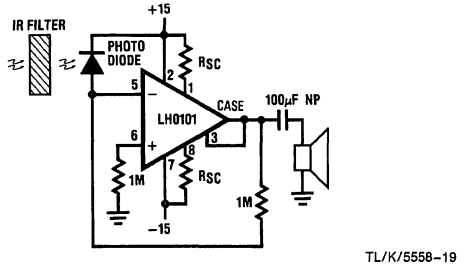
FIGURE 11. Bridge Audio Amplifier

Typical Applications (Continued)



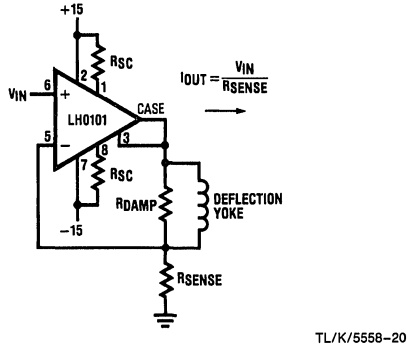
TL/K/5558–18

FIGURE 12. ±5 to ±35 Power Source or Sink



TL/K/5558–19

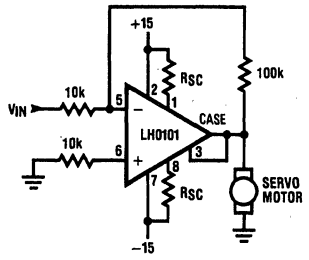
FIGURE 13. Remote Loudspeaker via Infrared Link



TL/K/5558–20

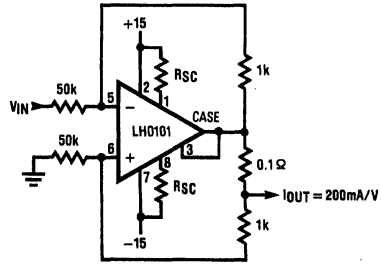
FIGURE 14. CRT Deflection Yoke Driver

Typical Applications (Continued)



TL/K/5558–21

FIGURE 15. DC Servo Amplifier



TL/K/5558–22

FIGURE 16. High Current Source/Sink

National Semiconductor

LH2101A/LH2201A/LH2301A
Dual High Performance Operational Amplifiers

General Description

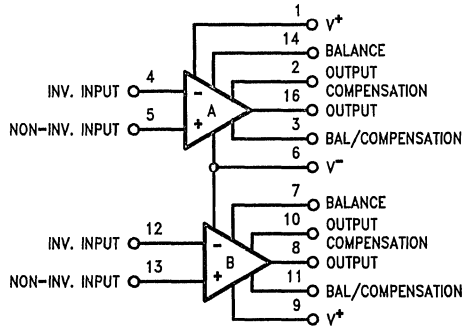
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles. For additional information, see the LM101A data sheet and National's Linear Application Handbook.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10 V/μs as a summing amplifier

Connection Diagram



TL/K/10118–1

Order Number LH2101AD, LH2201AD or LH2301AD
See NS Package Number D16C

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LH2101A	−55°C to +125°C
LH2201A	−25°C to +85°C
LH2301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	300°C

Electrical Characteristics Each Side (Note 3)

Parameter	Conditions	Limits			Units
		LH2101A	LH2201A	LH2301A	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50\ k\Omega$	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Curent	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±12 ±10	±12 ±10	V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S < 50\ k\Omega$	80	80	70	dB Min

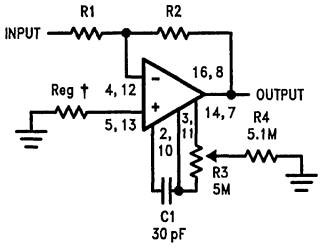
Note 1: The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures of devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq +70°C$, and $\pm 5V \leq V_S \leq +15V$. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

Auxiliary Circuits

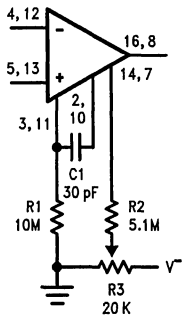
Inverting Amplifier with Balancing Circuit



TL/K/10118–2

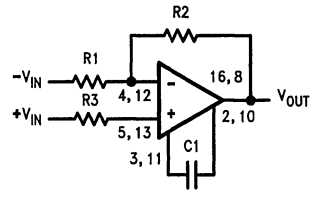
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Alternate Balancing Circuit



TL/K/10118–3

Single Pole Compensation

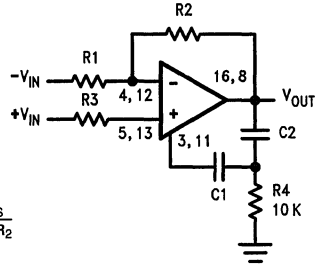


TL/K/10118–4

$$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$$

C_S = 30 pF

Two Pole Compensation



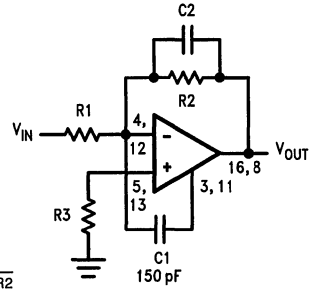
$$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$$

C_S = 30 pF

C2 = 10 C1

TL/K/10118–5

Feedforward Compensation



$$C2 = \frac{1}{2\pi f_o R2}$$

f_o = 3 MHz

TL/K/10118–6

National Semiconductor

LH2108/LH2208/LH2308, LH2108A/LH2208A/LH2308A Dual Super Beta Operational Amplifiers

General Description

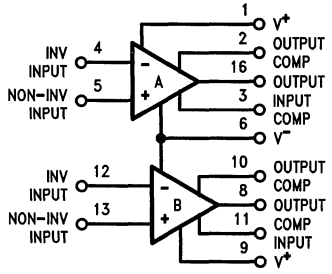
The LH2108A/LH2208A/LH2308A and LH2108/LH2208/LH2308 series of dual operational amplifiers are two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two single devices. For additional information see the LM108A or LM108 data sheet and National's Linear Application Handbook.

The LH2108A/LH2108 is specified for operation over the −55°C to +125°C military temperature range. The LH2208A/LH2208 is specified for operation over the −25°C to +85°C temperature range. The LH2308A/LH2308 is specified for operation over the 0°C to +70°C temperature range.

Features

- Low offset current 50 pA
- Low offset voltage 0.7 mV
- Low offset voltage LH2108A 0.3 mV
  LH2108 0.7 mV
- Wide input voltage range ±15V
- Wide operating supply range ±3V to ±20V

Connection Diagram

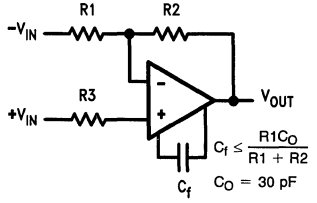


TL/K/10117–1

Order Number LH2108AD, LH2208AD, LH2208AD, LH2308AD, LH2108D, LH2208D, or LH2308D
See NS Package Number D16C

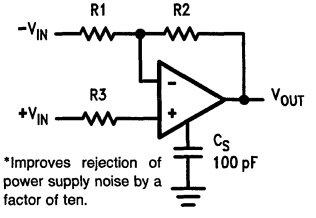
Auxiliary Circuits

Standard Compensation Circuit



TL/K/10117–2

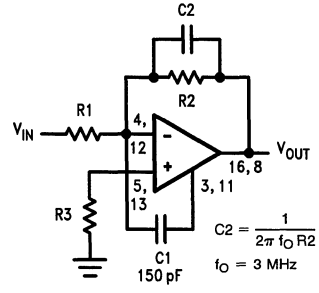
Alternate* Frequency Compensation



*Improves rejection of power supply noise by a factor of ten.

TL/K/10117–3

Feedback Compensation



TL/K/10117–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH2108A/LH2108	−55°C to +125°C
LH2208A/LH2208	−25°C to +85°C
LH2308A/LH2308	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 4)

Parameter	Conditions	Limits			Units
		LH2108	LH2208	LH2308	
Input Offset Voltage	T_A = 25°C	2.0	2.0	7.5	mV Max
Input Offset Current	T_A = 25°C	0.2	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	2.0	7.0	nA Max
Input Resistance	T_A = 25°C	30	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, R_L > 10 kΩ	50	50	25	V/mV Min
Input Offset Voltage		3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Current		15	15	30	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	T_A = +125°C	0.4	0.4		mA Max
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10 kΩ	25	25	15	V/mV Min
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±13	±13	V Min
Input Voltage Range	V_S = ±15V	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		85	85	80	dB Min
Supply Voltage Rejection Ratio		80	80	80	dB Min

Electrical Characteristics Each Side (Note 4)

Parameter	Conditions	Limits			Units
		LH2108A	LH2208A	LH2308A	
Input Offset Voltage	T_A = 25°C	0.5	0.5	0.5	mV Max
Input Offset Current	T_A = 25°C	0.2	0.2	1.0	nA Max
Input Bias Current	T_A = 25°C	2.0	2.0	7.0	nA Max
Input Resistance	T_A = 25°C	30	30	10	MΩ Min
Supply Current	T_A = 25°C	0.6	0.6	0.8	mA Max
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, R_L > 10 kΩ	80	80	80	V/mV Min

Electrical Characteristics Each Side (Note 4) (Continued)

Parameter	Conditions	Limits			Units
		LH2108A	LH2208A	LH2308A	
Input Offset Voltage		1.0	1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	5	μV/°C Max
Input Offset Current		0.4	0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	2.5	10	pA/°C Max
Input Bias Current		3.0	3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	0.4		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L > 10\ k\Omega$	40	40	60	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±13	±13	V Min
Input Voltage Range	$V_S = \pm 15V$	±13.5	±13.5	±14	V Min
Common Mode Rejection Ratio		96	96	96	dB Min
Supply Voltage Rejection Ratio		96	96	96	dB Min

Note 1: The maximum junction temperature of the LH2108A/LH2108 is 150°C, while that of the LH2208A/LH2208 is 100°C and that of the LH2308A/LH2308 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 20V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified. With the LH2208A/LH2208, however, all temperature specifications are limited to $-25°C \le T_A \le 85°C$ and with the LH2308A/LH2308 for $\pm 5V \le V_S \le 15V$ and $0°C \le T_A \le 70°C$.

National Semiconductor

LH4101/LH4101C Wideband High Current Operational Amplifier

General Description

The LH4101 is a high slew rate, FET input, wideband operational amplifier designed for applications that require an op amp to provide up to 200 mA peak and 100 mA continuous output current. This feature eliminates the need for a buffer to provide the additional current drive not available with most wideband op amps.

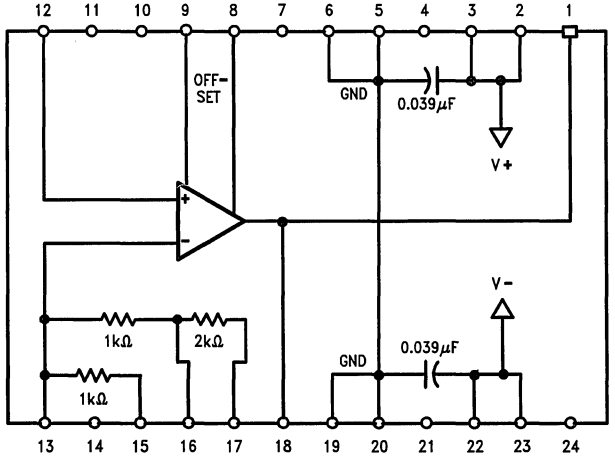
Designed for use with minimum external circuitry, the LH4101 provides internal compensation for unity gain stability and all the gain set resistors for most popular gain settings, as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions. These features are provided in a 24 pin hermetic dual in-line package.

Features

- 45 MHz bandwidth
- $10^{12}\Omega$ input impedance
- Pin strappable gain settings of 1, 2, 3, 4, −1, −2, −3
- Unity gain stable
- Internal supply bypassing
- 100 mA continuous output current
- 24 pin hermetic DIP
- Directly drives 50Ω loads

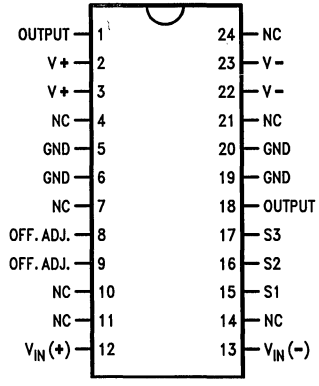
The LH4101's wide bandwidth, programmable gain settings, and high output current make it an ideal choice for fast buffering applications such as video distribution. It is also appropriate for use in summing amplifiers, sample and hold circuits, and high speed integrators.

Block and Connection Diagrams



TL/K/8543–1

Dual In-Line Package



TL/K/8543–2

Order Number LH4101D or LH4101CD
See NS Package Number D24D

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±17V
Power Dissipation, at T_A = 25°C, P_D	2W
Input Voltage Range, V_{CM}	±V_S
Steady State Output Current, I_O	±100 mA
Operating Temperature Range, T_A	
LH4101CD	−25°C to +85°C
LH4101D	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	175°C
Lead Temperature (Soldering <10 sec.)	300°C
ESD rating to be determined	

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	V_{IN} = 0V	$T_A = T_J$ = 25°C (Note 1)			15 25	mV mV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift				25		µV/°C
I_B	Input Bias Current		$T_A = T_J$ = 25°C (Note 1) $T_A = T_J = T_{max}$			500 500	pA nA
I_{OS}	Input Offset Current		$T_A = T_J$ = 25°C (Note 1) $T_A = T_J = T_{max}$			200 200	pA nA
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V		50	60		dB
PSRR	Power Supply Rejection Ratio	ΔV_S = ±10V		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	V_O = ±10V, R_L = 1 kΩ, f = 1 kHz V_O = ±5V, R_L = 50Ω, f = 1 kHz, T_A = 25°C		60 57	65 62		dB dB
V_O	Output Voltage Swing	V_{IN} = ±15V, R_L = 1 kΩ V_{IN} = ±5.5V, R_L = 50Ω, T_J = 25°C (Note 2)		±10 ±5	±13.5		V V
I_S	Supply Current	R_L = 1 kΩ			25	40	mA
e_{-3}	Gain Error A_V = −3	V_{IN} = ±1V, R_L = 50Ω, T_J = 25°C			0.8	2	%
e_{-1}	Gain Error A_V = −1				0.8	2	%

Note 1: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25°C.

Note 2: The output swing is limited by the maximum output current of ±100 mA when R_L = 50Ω. When the LH4101 is operated at elevated temperature (such as 125°C), some form of heatsinking or forced air cooling is required. The quiescent power with V_S of ±15V is 1.2W max, whereas the package can only handle 750 mW without a heatsink at 125°C.

AC Electrical Characteristics A_V = +1, R_L = 50Ω, T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_R	Slew Rate	V_{IN} = ±5V	200	250		V/µs
$f_{-3\,dB}$	Small Signal Bandwidth	V_{IN} = 100 mVrms		45		MHz
t_S	Settling Time to 1% Settling Time to 0.1%	ΔV_{IN} = 10V		140 300		ns ns
t_r	Small Signal Rise Time	V_{IN} = 0V to +100 mV		10		ns

Applications Information

Power Supply Bypassing

The LH4101 will perform well in most circuit boards even without external supply bypassing; however, it is recommended that some bulk bypassing be provided. One 10 μF electrolytic on each supply is recommended. Proximity to the device pins is not critical, but the bypass will be most effective if located within an inch of the part.

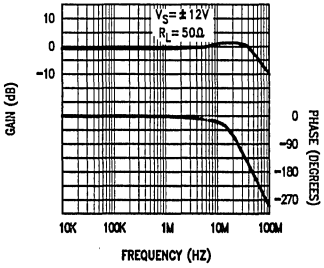
Input Capacitance

The input capacitance to the LH4101 is typically 5 pF and for source impedances greater than 100Ω, the input time constant should be considered.

Gain Settings

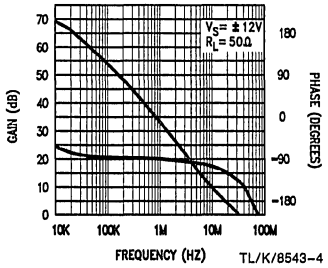
The LH4101 provides internal gain set resistors for most popular gain settings. A chart is provided to assist in determining the proper pins to connect to achieve these gains. The internal gain resistors are trimmed and matched to insure the gain accuracy to 0.8% typically. The LH4101 can operate at other gain settings, but the user must supply additional gain set resistors external to the part.

Frequency Response (A_V = +1 Closed Loop)



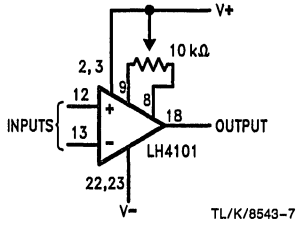
TL/K/8543-3

Frequency Response (Open Loop)



TL/K/8543-4

Offset Null



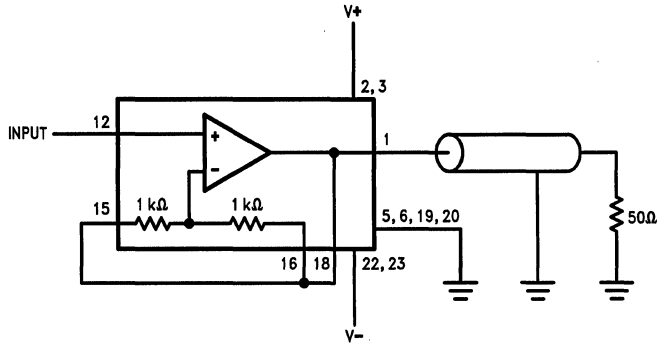
TL/K/8543-7

Gain	Connect	Pin Number	Comment
+1	V_{out} to S1 V_{out} to S2	18 to 15 18 to 16	For all positive gains, the input is $V_{in(+)}$, pin 12.
+2	V_{out} to S2 and S1 to GND	18 to 16 15 to 19	
+3	V_{out} to S3 and S2 to $V_{in(-)}$ and S1 to GND	18 to 17 16 to 13 15 to 19	
+4	V_{out} to S3 and S1 to GND	18 to 17 15 to 19	
−1	S2 to V_{out}	16 to 18	For all negative gains, input is S1, pin 15. Also, $V_{in(+)}$, pin 12, MUST BE CONNECTED TO GROUND.
−2	$V_{in(-)}$ to S2 and S3 to V_{out}	13 to 16 17 to 18	
−3	S3 to V_{out}	17 to 18	

Typical Applications

Unity Gain Follower

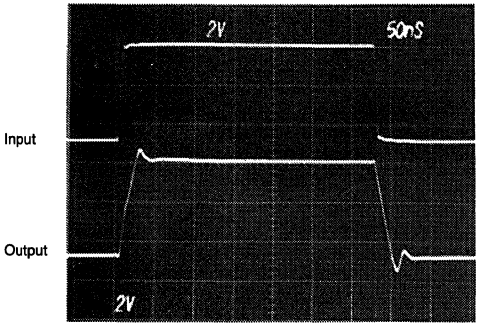
The LH4101 can be used as a unity gain follower to provide output current to drive 50Ω or 75Ω coax cable directly. By shorting pins 15, 16 and 18, a follower circuit is configured as seen in *Figure 1a*. This configuration features a bandwidth greater than 40 MHz with an input signal of 1.0 V_{p-p} and greater than 16 MHz with a 5 V_{p-p} input signal. This is all achieved without any external components. *Figures 1b* and *1c* show the small and large signal pulse responses, respectively.



TL/K/8543–5

FIGURE 1a. Unity Gain Follower

Large Signal Pulse Response

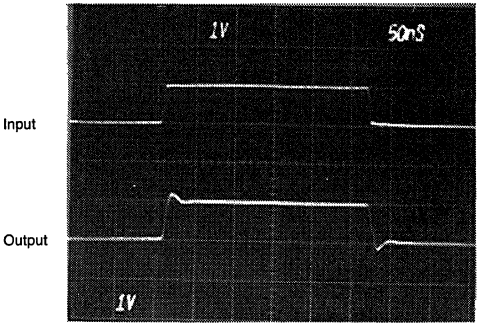


V_S = ±15V
A_V = 1
R_L = 50Ω

TL/K/8543–9

FIGURE 1b

Small Signal Pulse Response

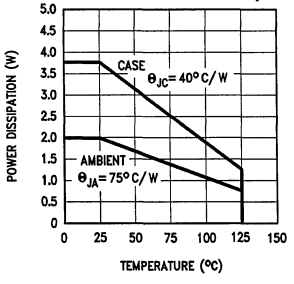


V_S = ±15V
A_V = 1
R_L = 50Ω

TL/K/8543–10

FIGURE 1c

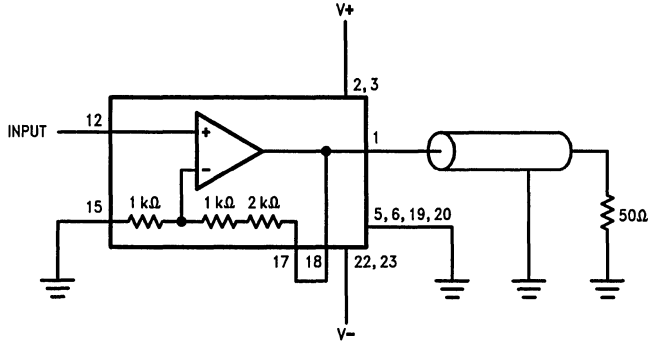
Maximum Power Dissipation



TL/K/8543–13

Non-Inverting Amplifier

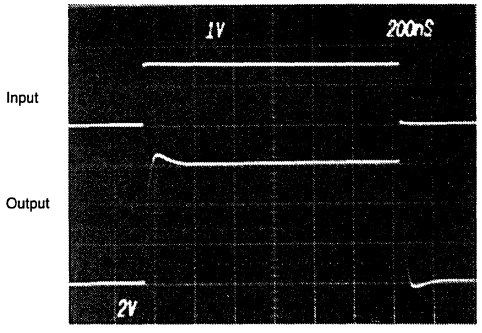
To configure the LH4101 as a non-inverting amplifier with a gain of 4, short pins 17 to 18 and 15 to 19, as shown in *Figure 2a*. Again, no external components are necessary. This configuration provides a bandwidth of 25 MHz with an input sine wave of 1.0 V_{p-p} and a bandwidth of 10 MHz with an input of 5 V_{p-p} while providing 100 mA of output current. This eliminates the need of an additional buffer in the circuit to provide the output current to drive large loads. *Figures 2b* and *2c* show the small and large signal pulse responses, respectively.



TL/K/8543-8

FIGURE 2a. Non-Inverter with Gain of +4

Large Signal Pulse Response

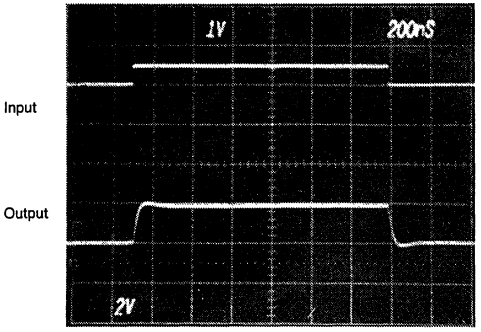


$V_S = \pm 15V$
$A_V = 4$
$R_L = 50\Omega$

TL/K/8543-11

FIGURE 2b

Small Signal Pulse Response



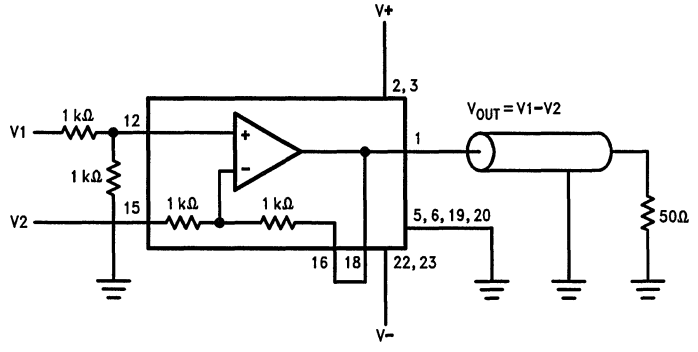
$V_S = \pm 15V$
$A_V = 4$
$R_L = 50\Omega$

TL/K/8543-12

FIGURE 2c

Differential Amplifier

To configure the LH4101 as a differential amplifier, two additional 1 kΩ resistors are required. *Figure 3* shows this configuration, where $V_0 = V_1 - V_2$. The gain accuracy of this circuit is dependent upon the gain accuracy of the additional 1 kΩ resistors.



TL/K/8543-6

FIGURE 3. Wideband Differential Amplifier

National Semiconductor

PRELIMINARY

LH4104/LH4104C Fast Settling High Current Operational Amplifier

General Description

The LH4104 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4104 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

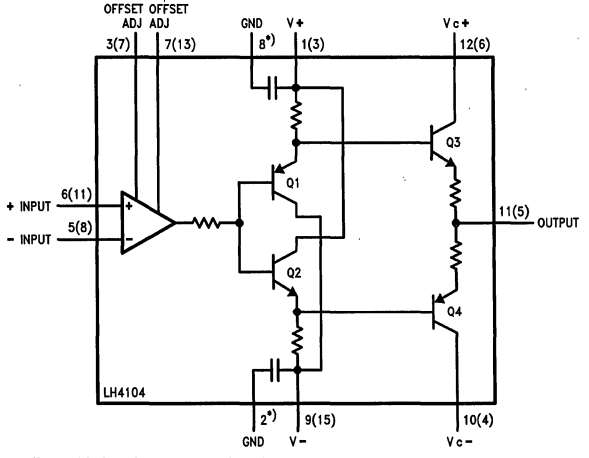
Features

- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- 18 MHz gain bandwidth product
- Internal supply bypassing
- Unity gain stable

Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

Schematic Diagram



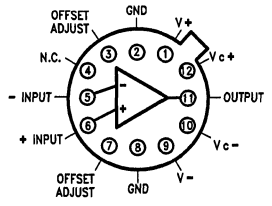
TL/K/8840-1

Pinout shown for metal can package (for molded package in parenthesis)

*On metal can package (G) pins #2 and #8 are internally connected. The case is electrically isolated. The molded package (N) does not have ground connections or bypass capacitors.

Connection Diagrams

Metal Can Package

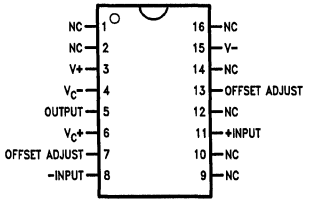


TL/K/8840-2

Top View

Order Number LH4104CG or LH4104G
See NS Package Number H12B

16-Lead Molded Dual-In-Line Package (N)



TL/K/8840-14

Top View

Order Number LH4104CN
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±18V
Steady State Output Current, I_o	100 mA
Power Dissipation (See Curves)	
T_A = 25°C, LH4104G, LH4104CG	1.5W
LH4104CN	1.56W
T_C = 25°C, LH4104G, LH4104CG	2.5W
Differential Input Voltage, V_{IN}	±30V but ≤ $\pm 2V_s$
Input Voltage Range, V_{CM}	±18V but ≤ $\pm V_s$
Operating Temperature Range, T_A	
LH4104	−55°C to +125°C
LH4104C	−25°C to +85°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering < 10 sec.)	300°C

ESD rating is to be determined.

DC Electrical Characteristics V_S = ±15V, T_A = 25°C unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4104C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	R_S = 50Ω	2	5	**10**	mV
$V_{OS}/\Delta T$	Offset Voltage Drift	R_S = 50Ω	20			µV/°C
I_B	Input Bias Current	T_j = 25°C, (Note 4) V_{CM} = 0V	200	600		pA
					250	nA
I_{OS}	Input Offset Current	T_j = 25°C, V_{CM} = 0V	20	400		pA
					200	nA
R_{IN}	Input Resistance	T_j = 25°C	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 100Ω	106	87		dB (Min)
		R_L = 1 kΩ	106	87	**80**	
V_O	Output Voltage Swing	R_L = 100Ω (Note 5)		±10		V (Min)
		R_L = 1 kΩ	±13	±10	**±10**	
V_{CM}	Input Common Mode Range		±12	±11	**±10**	V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} = −11V to +11V	100	80	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	V_{CC} = ±10V to ±15V	100	80	**70**	dB (Min)
I_S	Supply Current		20	25		mA

AC Electrical Characteristics V_{CC} = ±15V, T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	LH4104C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	A_V = −1, V_{IN} = −5V to +5V, R_L = 100Ω	500	800		ns
S_R	Slew Rate	V_{IN} = −10V to +10V, R_L = 100Ω	40		32	V/µs(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	A_V = 1, R_L = 100Ω	10		20	ns

DC Electrical Characteristics $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Notes 1 and 6)

Symbol	Parameter	Conditions	LH4104			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	2	**10**		mV
$V_{OS}/\Delta T$	Offset Voltage Drift	$R_S = 50\Omega$	20			$\mu V/°C$
I_B	Input Bias Current	$T_j = 25°C$, (Note 4) $V_{CM} = 0V$	200	600		pA
				350		nA
I_{OS}	Input Offset Current	$T_j = 25°C$, $V_{CM} = 0V$	20	400		pA
				250		nA
R_{IN}	Input Resistance	$T_j = 25°C$	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$	106	87		dB (Min)
		$R_L = 1\ k\Omega$	106	87		
				80		
V_O	Output Voltage Swing	$R_L = 100\Omega$ (Note 5)		± 10		V (Min)
		$R_L = 1\ k\Omega$	± 13	$\pm$ **10**		
V_{CM}	Input Common Mode Range		± 12	$\pm$ **10**		V (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} -11V$ to $+11V$	100	80		dB (Min)
				70		
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10V$ to $\pm 15V$	100	80		dB (Min)
				70		
I_S	Supply Current		20	25		mA

AC Electrical Characteristics $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH4104			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	$A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$	500	800		ns
S_R	Slew Rate	$V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$	40		32	$V/\mu s$(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	$A_V = 1$, $R_L = 100\Omega$	10		20	ns

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4104C is $-25°C$ to $+85°C$, and LH4104 is $-55°C$ to $+125°C$.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested).

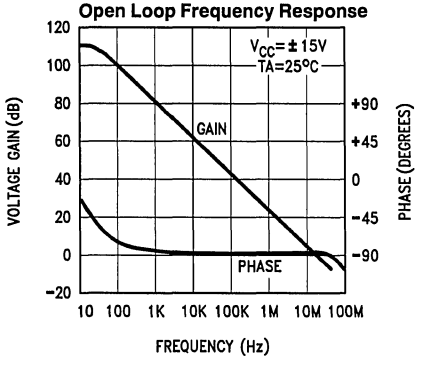
Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

Note 5: The output swing is limited by the maximum output current of ± 100 mA when $R_L = 100\Omega$.

Note 6: When the LH4104 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_{CC} of $\pm 15V$ is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

Typical Performance Characteristics

Open Loop Frequency Response



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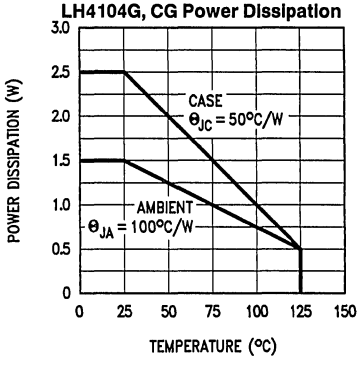
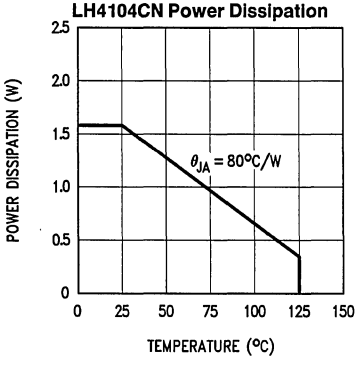
LH4104G, CG Power Dissipation



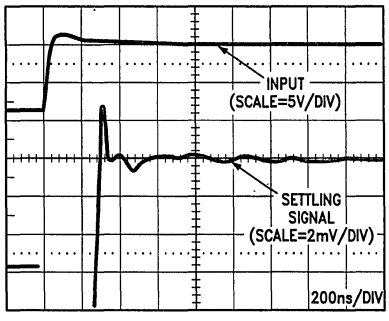
TL/K/8840–5

LH4104CN Power Dissipation



TL/K/8840–15

Settling Signal



TL/K/8840–3

Applications Information

POWER SUPPLY BYPASSING

The LH4104 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 μF disc ceramic capacitor and 1 μF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

COMPENSATION

To minimize the effects of input capacitance at the LH4104's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias (I_B) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. I_B will normally double with each 11°C rise in junction temperature.

LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4104. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4104, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the

Applications Information (Continued)

LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4104. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4104 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4104 without impacting setting time.

PROTECTION SCHEMES FOR THE LH4104

The LH4104 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4104's input stage shares its topology with the LF400.)

NEVER LEAVE AN INPUT UNATTENDED!

If an input to the LH4104 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance (<10 pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4104 is a capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

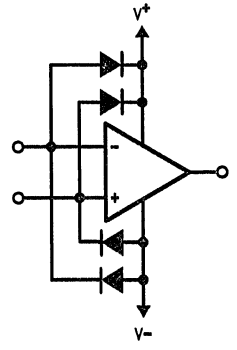
To avoid this condition in circuits where the LH4104 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected" state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor apears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can cause this problem. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.



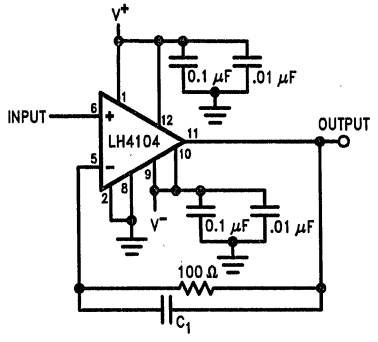
TL/K/8840-13

FIGURE 1. Clamping Inputs of Op Amp

V_{OS} ADJUSTMENT

Offset voltage can be nulled using a 56K resistor and a 25K potentiometer connected to pins 3 and 7 as shown in *Figure 3.* Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 3 and 7 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V^-.

Test Circuit for Pulse Response

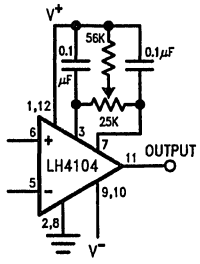


TL/K/8840-6

FIGURE 2*

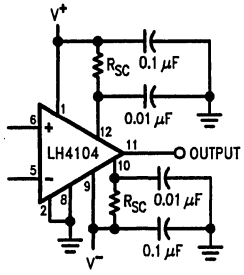
*Pinouts shown are for the metal can package (LH4104G or LH4104CG)

Typical Applications



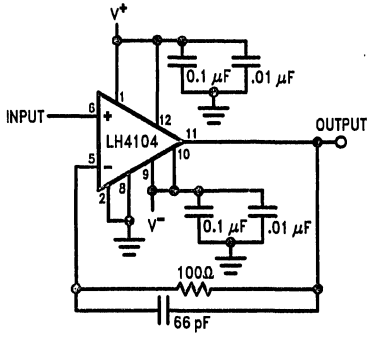
TL/K/8840–8

FIGURE 3. Offset Null*



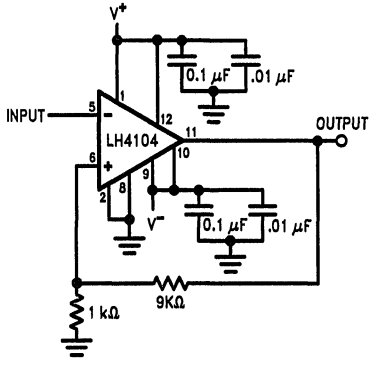
TL/K/8840–9

FIGURE 4. Using Resistor Current Limiting*



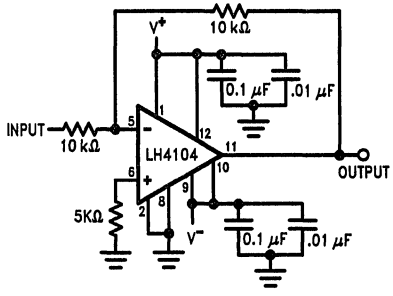
TL/K/8840–10

FIGURE 5. Unity Gain Follower*



TL/K/8840–11

FIGURE 6. 10X Buffer Amplifier*



TL/K/8840–12

FIGURE 7. Unity Gain Inverter*

*Pinouts shown are for the metal can package (LH4104G or LH4104CG)

National Semiconductor

PRELIMINARY

LH4105/LH4105C Precision Fast Settling High Current Operational Amplifier

General Description

The LH4105 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4105 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

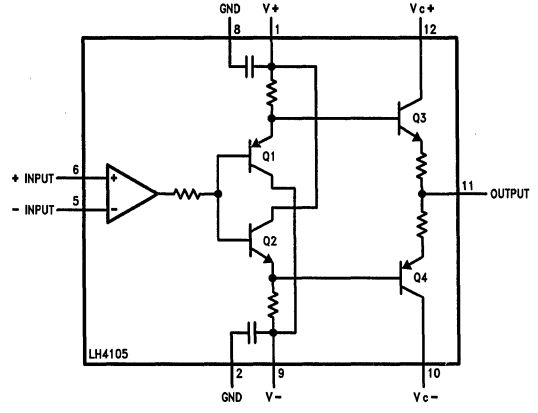
Features

- 500 μV offset voltage
- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- Internal supply bypassing
- Unity gain stable

Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

Schematic Diagram

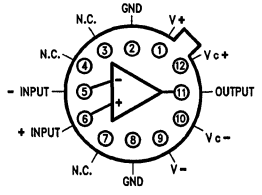


TL/K/9159-1

Pins #2 & #8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally, do not connect to these pins

Connection Diagram

Metal Can Package



TL/K/9159-2

Top View

Note: 2 and 8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally. Do not connect to these pins.

Order Number LH4105G or LH4105CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±18V
Steady State Output Current, I_o	100 mA
Power Dissipation at, P_D	
T_A = 25°C, derate linearly at 100°C/W	2.5W
T_C = 25°C, derate linearly at 50°C/W	1.5W
Differential Input Voltage, V_{IN}	±30V but ≤ $\pm 2V_s$
Input Voltage Range, V_{CM}	±18V but ≤ $\pm V_s$
Operating Temperature Range, T_A	
LH4105	−55°C to +125°C
LH4105C	−25°C to +85°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering < 10 sec.)	300°C

ESD rating is to be determined.

DC Electrical Characteristics V_S = ±15V, T_A = 25°C unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4105C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	R_S = 50Ω	0.2	0.5	**2**	mV
$V_{OS}/\Delta T$	Offset Voltage Drift	R_S = 50Ω	20			μV/°C
I_B	Input Bias Current	T_j = 25°C, (Note 4) V_{CM} = 0V	200	600		pA
					250	nA
I_{OS}	Input Offset Current	T_j = 25°C, V_{CM} = 0V	20	400		pA
					200	nA
R_{IN}	Input Resistance	T_j = 25°C	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 100Ω	106	87		dB (Min)
		R_L = 1 kΩ	106	87	**80**	
V_O	Output Voltage Swing	R_L = 100Ω (Note 5)		±10		V (Min)
		R_L = 1 kΩ	±13	±10	**±10**	
V_{CM}	Input Common Mode Range		±12	±11	**±10**	V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} = −11V to +11V	100	80	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	V_{CC} = ±10V to ±15V	100	80	**70**	dB (Min)
I_S	Supply Current		20	25		mA

AC Electrical Characteristics V_S = ±15V, T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	LH4105C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	A_V = −1, V_{IN} = −5V to +5V, R_L = 100Ω	500	800		ns
S_R	Slew Rate	V_{IN} = −10V to +10V, R_L = 100Ω	40		32	V/μs(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	A_V = 1, R_L = 100Ω	10		20	ns

DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Notes 1 and 6)

Symbol	Parameter	Conditions	LH4105			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	0.2	**2**		mV
$V_{OS}/\Delta T$	Offset Voltage Drift	$R_S = 50\Omega$	20			$\mu V/°C$
I_B	Input Bias Current	$T_j = 25°C$, (Note 4) $V_{CM} = 0V$	200	600		pA
				350		nA
I_{OS}	Input Offset Current	$T_j = 25°C$, $V_{CM} = 0V$	20	400		pA
				250		nA
R_{IN}	Input Resistance	$T_j = 25°C$	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$	106	87		dB (Min)
		$R_L = 1\ k\Omega$	106	87		
				80		
V_O	Output Voltage Swing	$R_L = 100\Omega$ (Note 5)		±10		V (Min)
		$R_L = 1\ k\Omega$	±13	**±10**		
V_{CM}	Input Common Mode Range		±12	**±10**		V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} −11V to +11V	100	80		dB (Min)
				70		
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10V$ to $\pm 15V$	100	80		dB (Min)
				70		
I_S	Supply Current		20	25		mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH4105			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	$A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$	500	800		ns
S_R	Slew Rate	$V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$	40		32	$V/\mu s$(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	$A_V = 1$, $R_L = 100\Omega$	10		20	ns

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4105C is −25°C to +85°C, and LH4105 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested). These limits are not used to calculate outgoing quality levels.

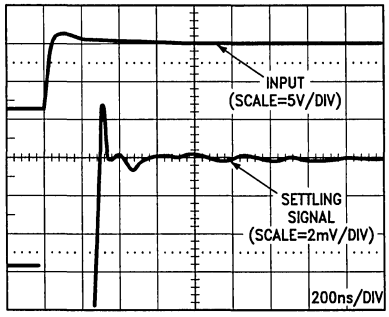
Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

Note 5: The output swing is limited by the maximum output current of ±100 mA when $R_L = 100\Omega$.

Note 6: When the LH4105 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_{CC} of ±15V is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

Typical Performance Characteristics

Settling Signal



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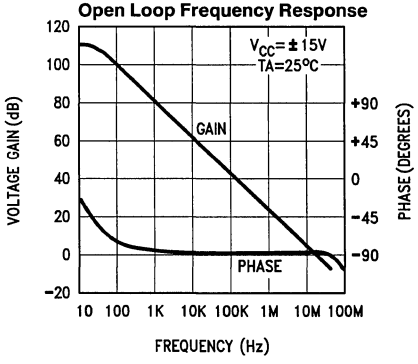
Open Loop Frequency Response



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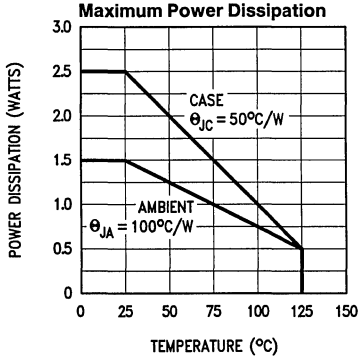
Maximum Power Dissipation



TL/K/9159–5

Applications Information

POWER SUPPLY BYPASSING

The LH4105 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 μF disc ceramic capacitor and 1 μF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

COMPENSATION

To minimize the effects .of input capacitance at the LH4105's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias (I_B) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. I_B will normally double with each 11°C rise in junction temperature.

LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4105. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4105, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4105. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4105 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4105 without impacting settling time. In addition, bypassing offset adjust pins 3 and 7 with 0.1 μF capacitors will minimize noise pickup and preserve the settling time.

PROTECTION SCHEMES FOR THE LH4104

The LH4105 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4105's input stage shares its topology with the LF400.)

NEVER LEAVE AN INPUT UNATTENDED

If an input to the LH4105 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance (<10 pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4105 is capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

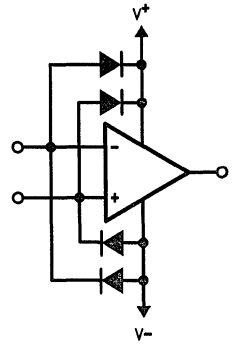
To avoid this condition in circuits where the LH4105 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor appears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can damage the device. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

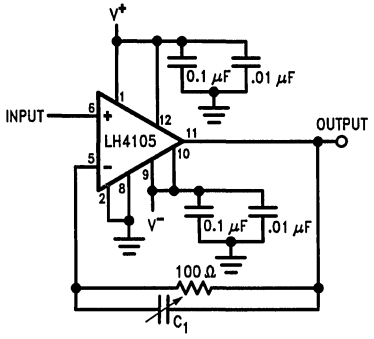
Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.



TL/K/9159–6

FIGURE 1. Clamping Inputs of Op Amp

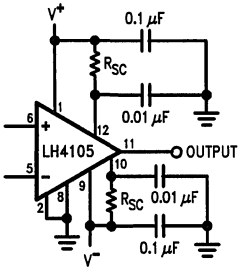
Test Circuit for Pulse Response



TL/K/9159–7

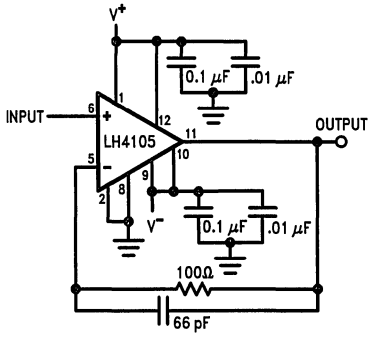
FIGURE 2

Typical Applications



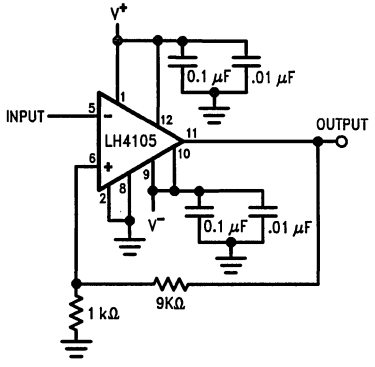
TL/K/9159–8

FIGURE 3. Using Resistor Current Limiting



TL/K/9159–9

FIGURE 4. Unity Gain Follower



TL/K/9159–10

FIGURE 5. 10X Buffer Amplifier

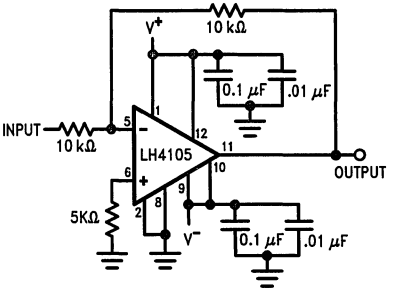


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FIGURE 6. Unity Gain Inverter

National Semiconductor

LH4106/LH4106C ±5V High Speed Operational Amplifier

General Description

The LH4106 is a wideband op amp designed to operate with ±5V power supplies. It features a 30 MHz bandwidth and can drive 50 or 75Ω loads directly at slew rates in excess of 170 V/μs.

It is intended to fulfill a wide range of applications; such as, precision cable drivers, buffers in high speed data acquisition systems, and high speed peak detectors.

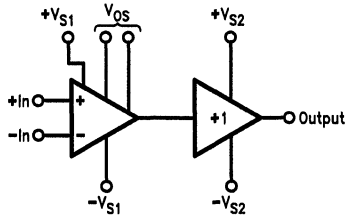
Features

- Operates from V_S of ±5V
- Unity gain stable
- Very high slew rate—170 V/μs
- Wide small signal bandwidth—32 MHz
- Low supply current—16 mA
- Drives 50 or 75Ω directly

Applications

- Flash A/D input buffers
- Video amplifier
- High speed summing amplifiers
- Pulse amplifiers
- Precision cable drivers

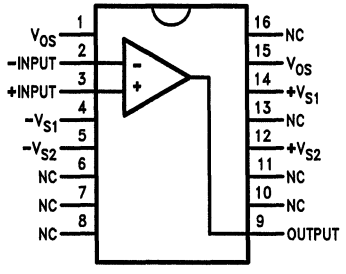
Block Diagram



TL/K/9317-10

Connection Diagrams

LH4106CN



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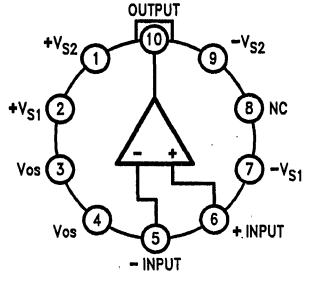
Order Number LH4106CN
See NS Package Number N16A



TL/K/9317-1

Top View

TO-5 Metal Can Package (H)
Order Number LH4106CH or LH4106H
See NS Package Number H10F

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S ±7.5V

Steady State Output Current, I_O 40 mA

Power Dissipation, P_D (See Curve) 600 mW

Differential Input Voltage, V_{IN} $\pm V_S$

Input Voltage Range, V_{CM} (V+ − 0.7V) to (V− − 7V)

Operating Temperature Range, T_A
LH4106 −55°C to +125°C
LH4106C −25°C to +85°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_j 150°C

Lead Temperature (Soldering <10 sec.) 300°C

ESD Rating ±700V
(100 pF in series with 1500 ohms)

DC Electrical Characteristics

V_S = ±5V, T_A = 25°C, R_S = 50Ω, R_L = 100Ω unless otherwise noted (Note 1)

Symbol	Parameter	Conditions		LH4106C Typ	LH4106C Tested Limit (Note 2)	LH4106C Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_{OS}	Input Offset Voltage	V_{IN} = 0V		5	15		mV
$V_{OS/AT}$	Offset Voltage Drift			10			µV/°C
I_B	Input Bias Current	(Note 4)		2	6		µA
I_{OS}	Input Offset Current	(Note 4)		150	1200		nA
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz		1.5			pF
R_{IN}	Input Resistance			325			kΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} ≅ ±2V		65	60		dB (Min)
V_O	Output Voltage Swing	R_L = 100Ω	$+V_o$	+3	+2		V (Min)
			$-V_o$	−2.6	−2		
V_{CM}	Input Common Mode Range	See CMRR			$+V_S$ − 1.5 $-V_S$ + 2.0		V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} = −3V ≤ V_{CM} ≤ + 3.5V R_L = 1 kΩ		90	70		db (Min)
PSRR	Power Supply Rejection Ratio	V_{OC} = ±3V to ±6V, R_L = 1 kΩ		80	70		dB (Min)
I_S	Supply Current	No Load		16	20		mA

DC Electrical Characteristics

V_S = ±5V, T_A = 25°C, R_S = 50Ω, R_L = 100Ω unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4106 Typ	LH4106 Tested Limit (Note 2)	LH4106 Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_{OS}	Input Offset Voltage	V_{IN} = 0V	5	**20**		mV
$V_{OS/AT}$	Offset Voltage Drift		10			µV/°C
I_B	Input Bias Current	(Note 4)	2	**6**		µA
I_{OS}	Input Offset Current	(Note 4)	150	**1500**		nA
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz	1.5			pF
R_{IN}	Input Resistance		325			kΩ
A_{VOL}	Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} ≅ ±2V	65	**60**		dB (Min)

DC Electrical Characteristics

$V_S = \pm 5V$, $T_A = 25°C$, $R_S = 50\Omega$, $R_L = 100\Omega$ unless otherwise noted (Note 1) (Continued)

Symbol	Parameter	Conditions		LH4106 Typ	LH4106 Tested Limit (Note 2)	LH4106 Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_O	Output Voltage Swing	$R_L = 100\Omega$	$+V_O$	+3	**+2**		V (Min)
			$-V_O$	−2.6	**−2**		
V_{CM}	Input Common Mode Range	See CMRR			$+V_S - 1.5$ $-V_S + 2.0$		
CMRR	Common Mode Rejection Ratio	$V_{IN} = -3V \le V_{CM} \le +3.5V$ $R_L = 1\ k\Omega$		90	**70**		db (Min)
PSRR	Power Supply Rejection Ratio	$V_{OC} = \pm 3V$ to $\pm 6V$, $R_L = 1\ k\Omega$		80	**70**		
I_S	Supply Current	No Load		16	20		mA

AC Electrical Characteristics $V_S = \pm 5V$, $T_A = 25°C$, $R_S = R_L = 50\Omega$ unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4106/LH4106C Typ	LH4106/LH4106C Tested Limit (Note 2)	LH4106/LH4106C Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
t_s	Settling Time to 0.1%		120			ns
SR	Slew Rate	$V_O = \pm 2V$	170	120		V/μs (Min)
t_r	Small Signal Rise Time	$A_V = 1$, $V_O = \pm 0.1V$	11			ns
	Power Bandwidth	(Note 6)	7			MHz
	Differential Gain	NTSC, $A_V = +4$	<0.1			%
	Differential Phase	NTSC, $A_V = +4$	0.1			degrees
	GBWP		34			MHz
	Phase Margin		60			degrees
	Input Noise Voltage	f = 10 kHz	15			$nV/\sqrt{Hz}$
	Input Noise Current	f = 10 kHz	1.5			$pa/\sqrt{Hz}$
SSBW	Small Signal Bandwidth	(Note 7)	32			MHz

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4106C is −25°C to +85°C, and LH4106 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature may exceed value at $T_j = 25°C$.

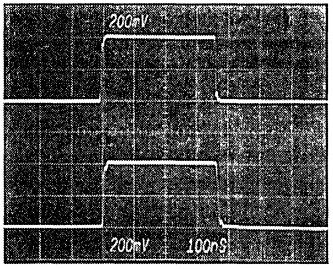
Note 5: When the LH4106 is operated at elevated temperature (such as 125°), some form of heatsinking or forced air cooling is required. The quiescent power with $V_S = \pm 5V$ is 160 mW, whereas, the package is only rated to 170 mW without a heatsink at 125°C.

Note 6: Power bandwidth is calculated from slew rate measurement using BW = Slew Rate/$2\pi V$ Peak.

Note 7: Calculated from t_r using SSBW = $0.35/t_r$.

Typical Performance Characteristics

Small Signal Pulse Response

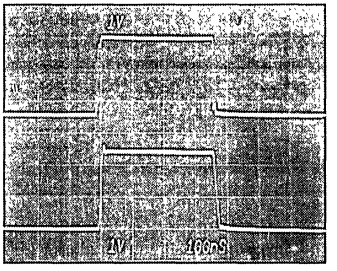


TOP = INPUT

BOTTOM = OUTPUT
$R_S = R_L = 50\Omega$

TL/K/9317–3

Large Signal Pulse Response



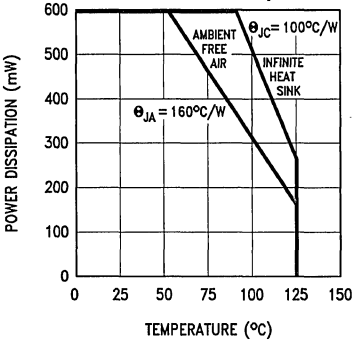
TOP = INPUT

BOTTOM = OUTPUT
$R_S = R_L = 50\Omega$

TL/K/9317–4

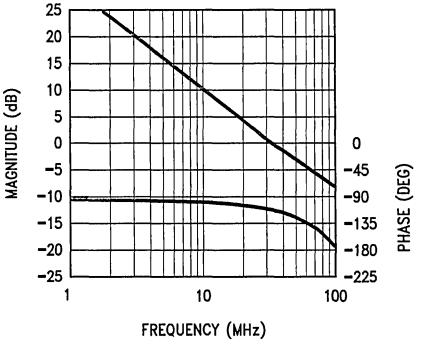
Typical Applications

Maximum Power Dissipation



TL/K/9317–5

Bode Plot LH4106



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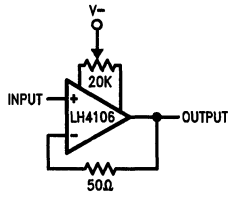
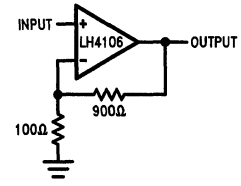
Typical Applications (Continued)



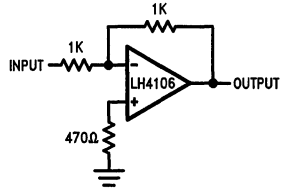
TL/K/9317-7

FIGURE 1. Unity Gain Follower with Offset Adjust



TL/K/9317-8

FIGURE 2. 10X Buffer Amplifier



TL/K/9317-9

FIGURE 3. Unity Gain Inverter

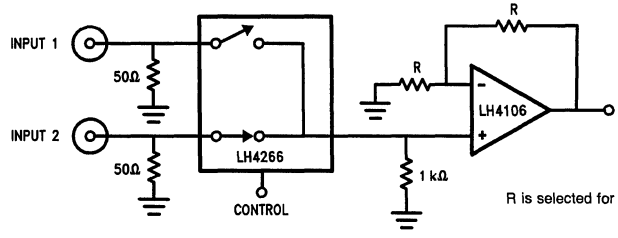


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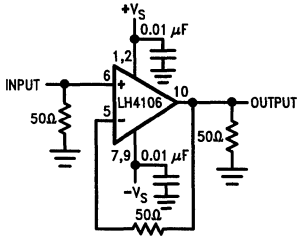
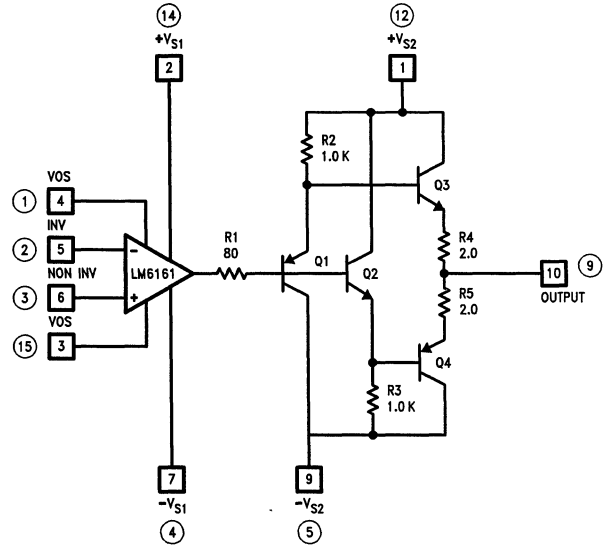
FIGURE 4. Switched Video Amplifier

AC Test Circuit



TL/K/9317-2

Circuit Schematic



TL/K/9317-14

Pin numbers in circle denote pin connections for the dual-in-line package.

National Semiconductor

PRELIMINARY

LH4117/LH4117C Precision RF Amplifier

General Description

The LH4117 is a FET-input wideband amplifier optimized for high speed, low gain applications. It is an ideal alternative to low precision open loop buffers and conventional operational amplifiers. It features a closed loop −3 dB unity gain bandwidth in excess of 150 MHz. Unlike conventional op-amps, the bandwidth is relatively independent of closed loop gain between 1 and 20. A high current output stage is also incorporated, allowing the LH4117 to drive 50Ω terminated lines directly. It is an ideal choice for video distribution, flash converter input buffering and ATE pin drivers.

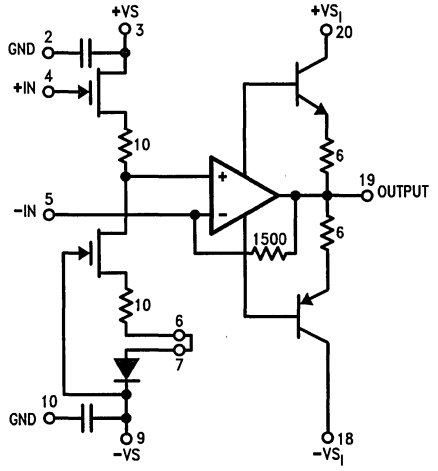
Features

- 150 MHz bandwidth
- 9 ns settling time to 0.2%
- 3.3 ns rise and fall times
- Output current to 200 mA
- FET-input, low bias current
- 2500 V/μS slew rate (100Ω load)
- ±0.3 dB gain flatness (A_V = 20)

Applications

- Unity gain buffers
- Low gain op amp
- High speed peak detectors
- Video amplifier

LH4117 Simplified Schematic



TL/K/9348-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_S)	±18V
Power Dissipation, (P_D) See Graph	2.0W
Input Voltage Range, (V_{CM})	±V_S
Operating Temperature Range, (T_A)	
LH4117CD	−25°C to +85°C
LH4117D	−25°C to +125°C
Storage Temperature Range, (T_{STG})	−65°C to +150°C
Maximum Junction Temperature, (T_j)	175°C
Lead Temperature (Soldering, <10 sec.)	300°C

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117D			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	V_{IN} = 0V, T_A = T_j = 25°C (Note 4)	15	20 **25**		mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift	V_{IN} = 0V	100			µV/°C
I_B	Non-Inverting Input Bias Current	T_A = T_j = 25°C Pin 4 (Note 4)	0.2	2 **5**		nA
V_O	Output Voltage Swing	R_L = 100Ω		±**11**		V (Min)
PSRR	Power Supply Rejection Ratio	ΔV_S = ±10V to ±15V	70	60 **50**		dB (Min)
I_O	Peak Output Current	T_A = T_j = 25°C (Note 5)	200			mA
I_S	Supply Current	T_A = T_j = 25°C		45		mA
P_D	Quiescent Power Dissipation	(Note 5)		1.35		W

DC Electrical Characteristics

V_S = ±15V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117CD			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	V_{IN} = 0V, T_A = T_j = 25°C (Note 4)	15	20	**25**	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift		100			µV/°C
I_B	Non-Inverting Input Bias Current	T_A = T_j = 25°C Pin 4 (Note 4)	0.2	2	**5**	nA
V_O	Output Voltage Swing	R_L = 100Ω		±11	±**11**	V (Min)
PSRR	Power Supply Rejection Ratio	ΔV_S = ±10V to ±15V	70	50		dB (Min)
I_O	Peak Output Current	T_A = T_j = 25°C (Note 5)	200			mA
I_S	Supply Current			45		mA
P_D	Quiescent Power Dissipation	(Note 5)		1.35		W

AC Electrical Characteristics

$V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25°C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions	LH4117D/LH4117CD			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time	$V_O = 5V$, $A_V = +20$ 10%–90%	3			ns
t_s	Settling Time to 0.2%	$V_O = 10V$	9			ns
$f_{-3\ dB}$	Small Signal Bandwidth	$V_O = 4\ V_{PP}$, $A_V = 20$	150	100		MHz (Min)
$f_{-3\ dB}$	Large Signal Bandwidth	$V_O = 20\ V_{PP}$, $A_V = 20$	70	40		MHz
	−1 dB Gain Compression	V_O, f = 50 MHz, $A_V = +20$	20			V_{PP}
SR	Slew Rate	$V_{IN} = \pm 1V$, $A_V = +20$ V_O = 10%–90%, $V_O = \pm 4V$	2500 6000			V/μs V/μs
	Harmonic Distortion	Second Order, $V_O = 4\ V_{PP}$, 20 MHz	−50			dB
	Gain Flatness	$V_{IN} = 100\ mV_{PP}$, $A_V = +20$ f = DC to 50 MHz f = DC to 70 MHz	±0.3 ±0.9			dB
	Differential Gain	(Note 6)	0.01			dB
	Differential Phase	(Note 6)	0.01			deg

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4117C is −25°C to +85°C, and LH4117 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

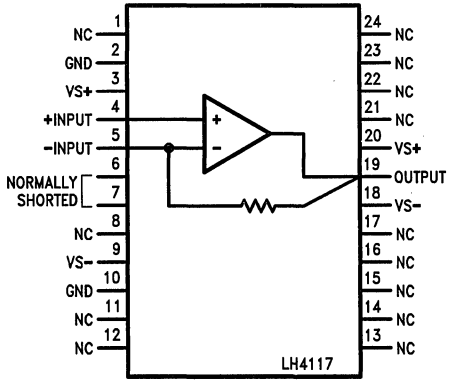
Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

Note 5: When the LH4117 is operated at elevated temperature (such as 125°C), some form of heat sinking of forced air cooling is required. The quiescent power with $V_S = \pm 15V$ is 1.2W, whereas the package can only handle 660 mW without a heatsink at 125°C.

Note 6: Differential gain and phase were measured at video levels (0 mV–750 mV) between 15.7 kHz and 3.58 MHz. The actual values are smaller than 0.01 dB and 0.01 deg, but could not be accurately measured with existing equipment.

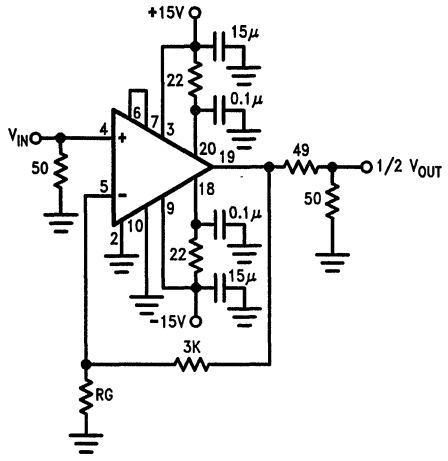
Connection Diagram



TL/K/9348–2

Order Number LH4117D or LH4117CD
See NS Package Number D24J

AC Test Circuit

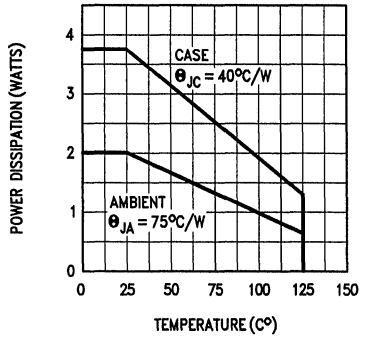


TL/K/9348-3

The 22Ω resistors in the supply line are for limiting the short circuit current.
For a gain of 20 select R_G = 52Ω.
Slew rate measurement is done with R_G = 56Ω, ΔV_{IN} = ±1V Step with 1 ns rise time.

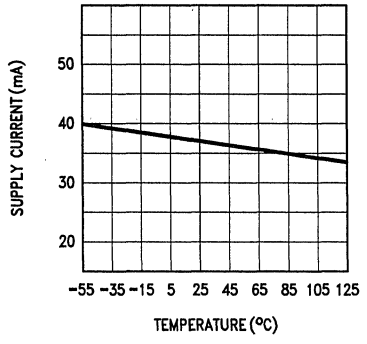
Typical Performance Characteristics

Maximum Power Dissipation



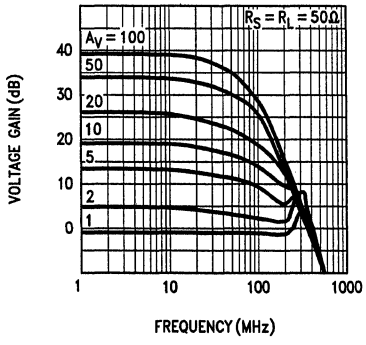
TL/K/9348-4

Supply Current



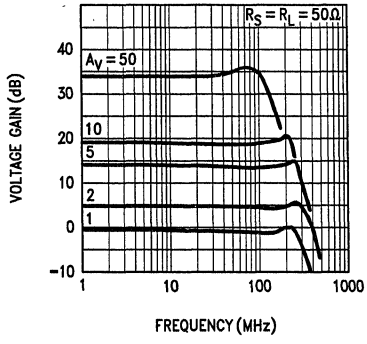
TL/K/9348-5

Closed Loop Response, Uncompensated



TL/K/9348-6

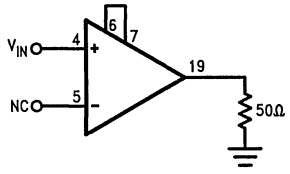
Closed Loop Response, Peaked (+1 dB)



TL/K/9348-7

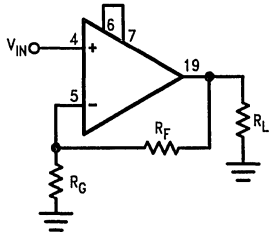
*For details see application section.

Typical Applications



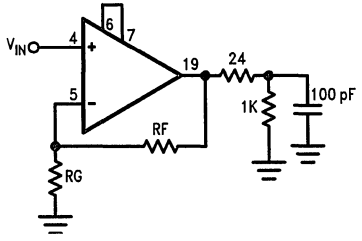
TL/K/9348-8

FIGURE 1. Unity Gain Buffer



TL/K/9348-9

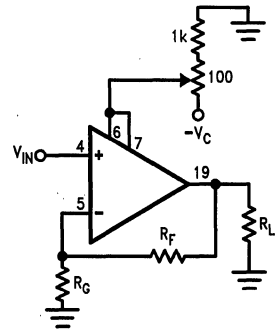
FIGURE 2. Amplifier



TL/K/9348-10

FIGURE 3. Driving Capacitive Loads

Typical Applications (Continued)



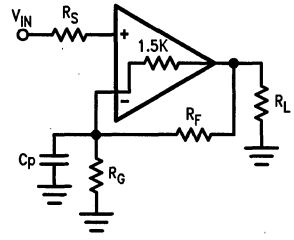
TL/K/9348–11

FIGURE 4. Offset Adjust

Application Hints

The two inputs of the LH4117 are radically different. While the non-inverting input is the gate of a FET, the inverting input is low impedance.

The graph "Closed Loop Response, Uncompensated" shows gain vs. frequency using only the internal feedback resistor. This performance can be considerably improved by choice of RF and peaking (See graph "Closed Loop Response, Peaked")



$$A_V = 1 + \frac{R_F^*}{R_G}$$

$$R_F^* = \frac{1500 \times R_F}{1500 + R_F}$$

TL/K/9348–12

FIGURE 5. LH4117 as Amplifier with Compensation Elements

Guidelines for Compensation

A_V (Nom. Gain)	R_F Ω	R_F^* Ω	R_G Ω	C_P pF	R_S Ω
1	—	1.5k	—	—	140
2	3k	1k	1k	—	—
5	3k	1k	165	1.2	—
10	3k	1k	110	3.9	—
50	3k	1k	20	25	—
100	750	500	5	100	—

The maximum peaking for the above values was +1 dB. For $A_V = 1$, the input resistor R_S corrects for excessive peaking.

National Semiconductor

LH4118/LH4118A/LH4118C
Low Gain Wide Band RF Amplifier

General Description

The LH4118 is a wideband amplifier optimized for high speed, low gain applications. It is an ideal alternative to low precision amplifiers. It features a closed loop −3 dB unity gain bandwidth in excess of 200 MHz. Unlike conventional op-amps, the bandwidth is relatively independent of closed loop gain between 1 and 5. A high current output stage is also incorporated, allowing the LH4118 to drive 50Ω terminated lines directly. It is an ideal choice for video distribution, flash converter input buffering and ATE pin driver.

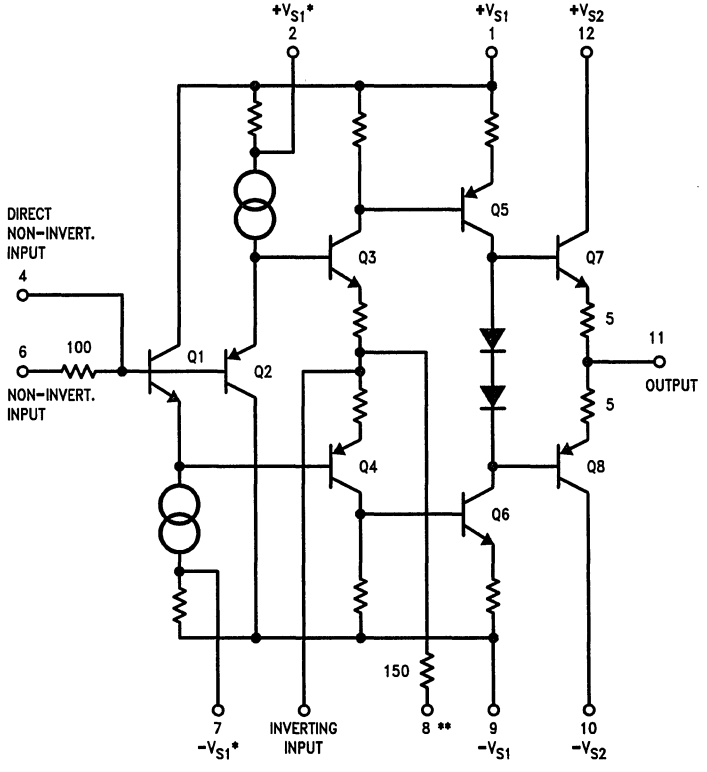
Features

- 250 MHz bandwidth
- 15 ns settling time to 0.1%
- 2.5 ns rise and fall times
- Output current to 100 mA
- 2 mV offset voltage
- 2500 V/μs slew rate (100Ω load)
- ±0.5 dB gain flatness (AV = 5)

Applications

- Unity gain buffers
- Low gain op amp
- High speed peak detectors
- Video amplifier
- Flash converter driver

Simplified Schematic



TL/K/9768–1

*Pins 2 and 7 can also be left disconnected (floating)

**The built-in 150Ω can be used as feedback resistor for A_V = 1. For details see applications section.

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

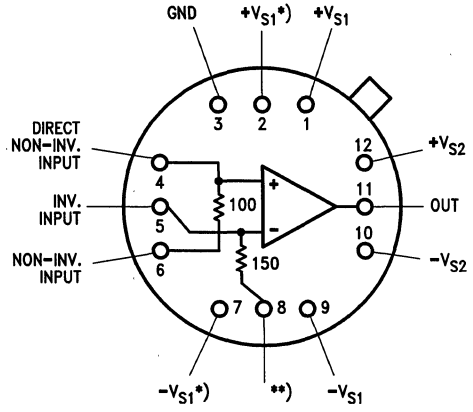
Supply Voltage, V_S	±18V
Power Dissipation, P_D (See Graph)	1.65W
Output Current	125 mA
Non-Inverting Input Voltage Range, V_{CM} (For $V_S \leq +15V$) (Note 1)	$\pm V_S$
Operating Temperature Range, T_A	
LH4118CG	−25°C to +85°C
LH4118G, LH4118AG	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	175°C
Lead Temperature (Soldering, < 10 sec.)	300°C
ESD Tolerance (Note 2)	650V

DC Electrical Characteristics

Unless otherwise noted, $R_S = 50\Omega$, $T_A = T_C = 25°C$, $V_S = \pm 15V$ (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118AG			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Non-Inverting Input Offset Voltage	$V_{IN} = 0V$	±2	±2 **±5**		mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			μV/°C
I_B	Non-Inverting Input Bias Current		±5	±25 **±30**		μA
V_O	Output Voltage Swing	$R_L = 500\Omega$	±13	±11 **±10.5**		V (Min)
V_O	Output Voltage Swing	$R_L = \infty$	±14	±12 **±11.5**		V (Min)
I_O	Output Current Swing	$R_L = 50\Omega$ (Note 7)		**±100**		mA (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11V$ to $+11V$, $V_S = \pm 18V$	54	**50**		dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9V$ to 15V $\Delta V = 6V$	72	**62**		dB (Min)
I_S	Quiescent Supply Current	$V_{IN} = 0V$	20	**25**		mA
P_D	Quiescent Power Dissipation	(Note 7)	600	**750**		mW
C_{IN}	Input Capacitance		1.5			pF

Connection Diagram



TL/K/9768–2

Top View

*Pins 2 and 7 can also be left disconnected (floating)

**The built-in 150Ω can be used as feedback resistor for $A_V = 1$. For details see applications section.

Order Number LH4118G, LH4118AG or LH4118CG
See NS Package Number H12B

DC Electrical Characteristics

Unless otherwise noted, $R_S = 50\Omega$, $T_A = T_C = 25°C$, $V_S = \pm 15V$ (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118G			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Non-Inverting Input Offset Voltage	$V_{IN} = 0V$	±2	**±5**		mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			µV/°C
I_B	Non-Inverting Input Bias Current		±5	±25 **±30**		µA
V_O	Output Voltage Swing	$R_L = 500\Omega$	±13	±11 **±10.5**		V (Min)
V_O	Output Voltage Swing	$R_L = \infty$	±14	±12 **±11.5**		V (Min)
I_O	Output Current Swing	$R_L = 50\Omega$ (Note 7)		**±100**		mA (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11V$ to $+11V$, $V_S = \pm 18V$	54	**50**		dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9V$ to $15V$ $\Delta V = 6V$	72	**62**		dB (Min)
I_S	Quiescent Supply Current	$V_{IN} = 0V$	20	**25**		mA
P_D	Quiescent Power Dissipation	(Note 7)	600	**750**		mW
C_{IN}	Input Capacitance		1.5			pF

DC Electrical Characteristics

Unless otherwise noted, $R_S = 50\Omega$, $T_A = T_C = 25°C$, $V_S = \pm 15V$ (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118CG			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Non-Inverting Input Offset Voltage	$V_{IN} = 0V$	±2	±5	**±5**	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10			µV/°C
I_B	Non-Inverting Input Bias Current		±5	±25	**±30**	µA
V_O	Output Voltage Swing	$R_L = 500\Omega$	±13	±11	**±10.5**	V
V_O	Output Voltage Swing	$R_L = \infty$	±14	±12	**±11.5**	V (Min)
I_O	Output Current Swing	$R_L = 50\Omega$ (Note 7)		±100	**±100**	mA
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11V$ to $+11V$, $V_S = \pm 18V$	54	50	**50**	dB
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9V$ to $15V$ $\Delta V = 6V$	72	62	**62**	dB
I_S	Quiescent Supply Current	$V_{IN} = 0V$	20	25	**25**	mA
P_D	Quiescent Power Dissipation	(Note 7)	600	750	**750**	mW
C_{IN}	Input Capacitance		1.5			pF

3

AC Electrical Characteristics

Unless otherwise noted, Av = +2, R_S = 50Ω, R_L = 100Ω, V_S = ±15V, T_A = 25°C

Symbol	Parameter	Conditions	LH4118CG, LH4118AG and LH4118G			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit	Design Limit	
SSBW −3 dB	Small Signal Bandwidth	V_{OUT} = 0.2 V_{P-P}	250	200		MHz (Min)
PBW −3 dB	Power Bandwidth	V_{OUT} = 10 V_{P-P}	68	55		MHz (Min)
GF	Gain Flatness	V_{OUT} = 0.2 V_{P-P}, 0.5 MHz, −50 MHz	±0.3			dB (Max)
		V_{OUT} = 0.2 V_{P-P}, 0.5 MHz, −100 MHz	−1.0			dB (Max)
SR	Slew Rate LH4118AG LH4118G LH4118CG	V_{OUT} = 15 V_{P-P} 20%–80%		2400 2000 1800		V/μS (Min)
t_r	Rise Time	V_{OUT} = 10 V_{P-P} 10%–90%	2.5			ns
V_{GC}	−1 dB Gain Compression	f = 50 MHz	23.5			dBm
e_n	Input Noise Voltage	A_V = 5, R_S = 50Ω, f = 10 MHz	1.3			nV/√Hz
HD_2	Second Harmonic Distortion	V_{OC} = 1.27 V_{P-P} F_C = 14 MHz	−58			dBc
HD_3	Third Harmonic Distortion	V_{OC} = 1.27 V_{P-P} F_C = 14 MHz	−40			dBc
t_s	Settling Time	A_V = −1 V_{IN} = +5 V_{P-P} to 0.1%	15			ns
LVBW −3 dB	Low Supply Voltage Bandwidth	V_{OUT} = 0.2 V_{P-P} V_S = ±5V	230			MHz
LVSR	Low Supply Voltage Slew Rate	V_S = ±5V, V_{OUT} = 5 V_{P-P} 20%–80%	1400			V/μs
DG	Differential Gain	V_{IN} = ±4 V_{DC} 0.4 V_{P-P} AC f = 4 MHz	<0.01			dB
PL	Phase Linearity	V_{IN} = ±4 V_{DC} 0.4 V_{P-P} AC, f = 4 MHz	<0.1			DEG

Note 1: The input signal should be within the supply rails. Also, the input signal as well as the output signal should not be more than 30V from any supply voltage.

Note 2: The average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 3: **Boldface** limits are guaranteed over full temperature range. Operating ambient temperature range of LH4118CG is −25°C to +85°C, for LH4118G and LH4118AG it is −55°C to 125°C.

Note 4: Specifications are at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_J = 25°C.

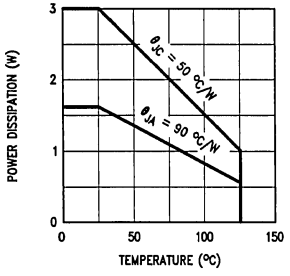
Note 5: Tested limits are guaranteed and 100% production tested.

Note 6: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

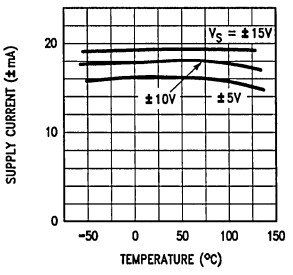
Note 7: When the LH4118 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S = ±15V is 750 mW, whereas the package can only handle 550 mW without a heatsink at 125°C.

Typical Performance Characteristics

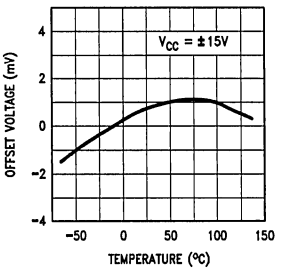
Power Dissipation



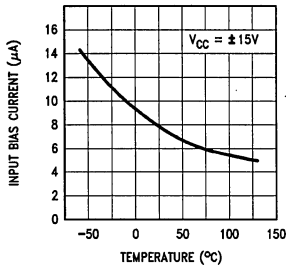
Supply Current vs Temperature



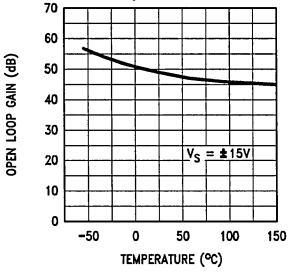
Offset Voltage vs Temperature



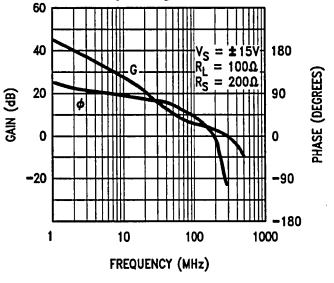
Input Bias Current vs Temperature



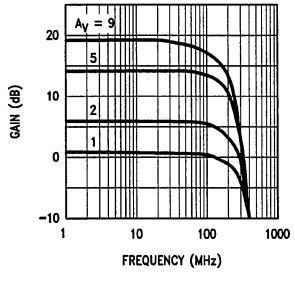
Open Loop Gain vs Temperature



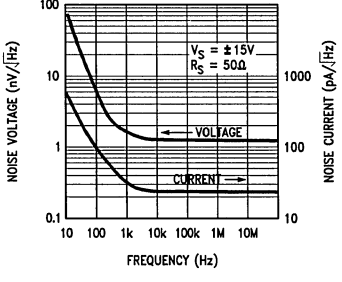
Inverting Open Loop Gain and Phase vs Frequency



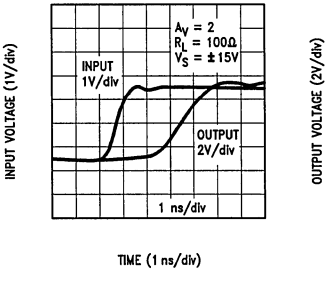
Non-Inverting Closed Loop Gain vs Frequency



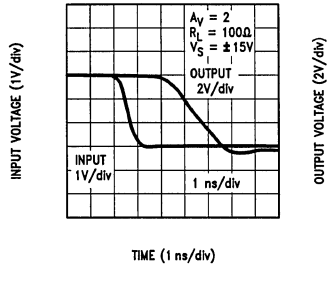
Input Noise vs Frequency



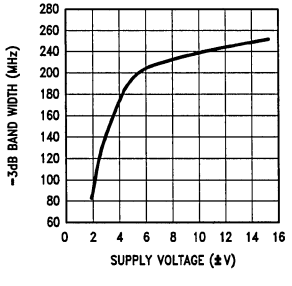
Rise Time



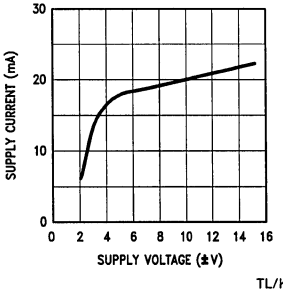
Fall Time



Bandwidth vs Supply Voltage



Supply Current vs Supply Voltage



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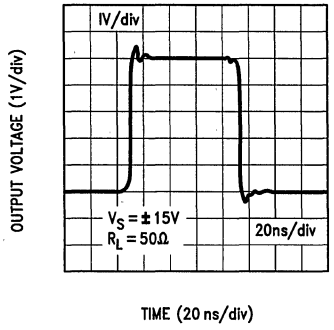
Typical Performance Characteristics (Continued)

Pulse Response



TL/K/9768–4

Applications Information

LAYOUT

Breadboards should have a solid ground plane and short point-to-point wiring. Do not use wirewrap boards or techniques. PC boards should have short connections and as much ground plane as possible.

The inputs (Pins 4, 5 & 6) should have low capacitance and, therefore, the ground plane should be taken out around these pins. The body of RG should be close to Pin 5 for the same reason.

It is best to have a layout without sockets, but sockets with short pins and receptacles do not degrade the performance much.

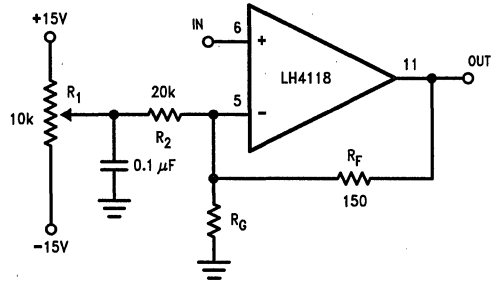
Input and output should be led by coax or microstrip if the distances are more than a few inches to avoid impedance shifts and resulting reflections.

Power supplies need to be bypassed with 0.01 μF to 0.1 μF as close as 0.15″ to the pins and additional 1 μF tantalum a maximum 1″ distant. Please make sure that the return current from the ground end of R_L does not flow across the input: the grounding point of R_L should be close to the grounding points of the power supply bypass capacitors. On the LH4118, this comes almost natural because of the layout of the pins.

The direct non-inverting input on pin 4, if used, should not see impedances of less than 100Ω.

The built-in feedback resistor (pin 8) is limited to a maximum dissipation of 150 mW. It can be used for unity gain and for higher gains at lower amplitudes.

Input-to-Output Offset Zero Adjust

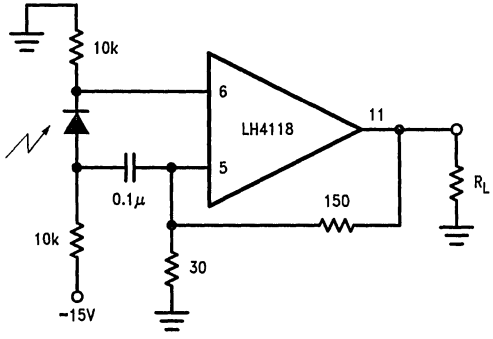


TL/K/9768–5

This circuit lets the V_{OS} between non-inverting input (pin 6) and output (pin 11) be adjusted. For $R_G = 15\Omega$ the range of adjustment is ± 11 mV, for higher R_G proportionately more. For higher R_G it is recommended to increase R_2 to decrease the range and make trimming less sensitive.

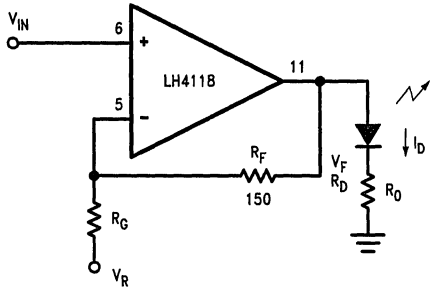
There is also an offset between inverting and non-inverting input which cannot be trimmed out.

Typical Applications



TL/K/9768–6

FIGURE 1. Bootstrapped Fiber Optic Receiver



$$I_D = I_{BIAS} + I_{Signal}$$

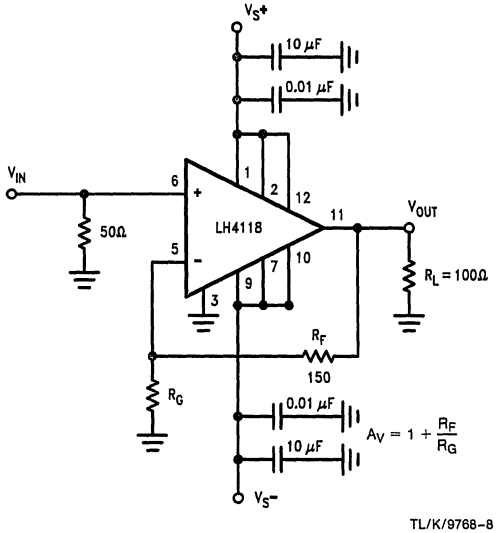
$$I_{BIAS} = \frac{V_R(-R_F/R_G) - V_F}{R_O}$$

$$I_{Signal} = \frac{V_{IN}(1 + R_F/R_G}{R_O + R_D}$$

$$R_D \approx 26\ mV/I_{BIAS}$$

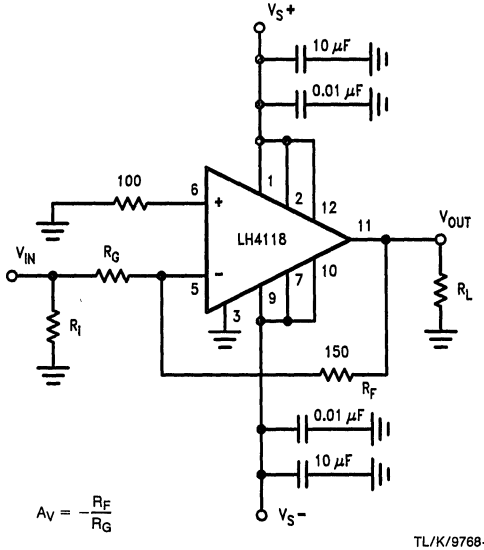
TL/K/9768–7

FIGURE 2. Fiber Optic Transmitter



TL/K/9768–8

FIGURE 3. Non-Inverting Gain Circuit



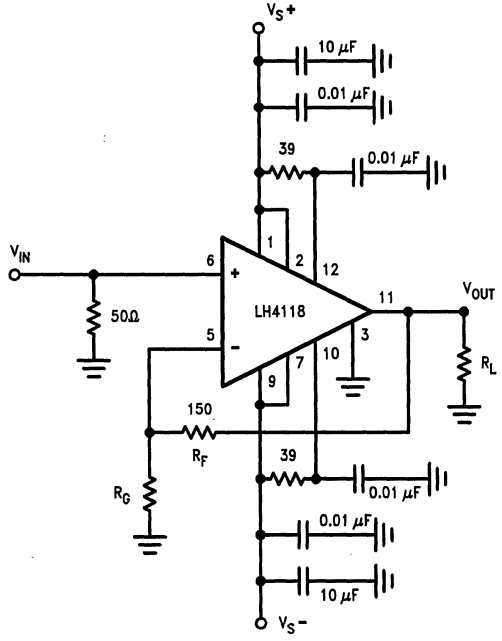
TL/K/9768–9

R_I is selected so that $R_I \parallel R_G$ matches the line impedance (e.g., 50Ω)

FIGURE 4. Inverting Gain Circuit

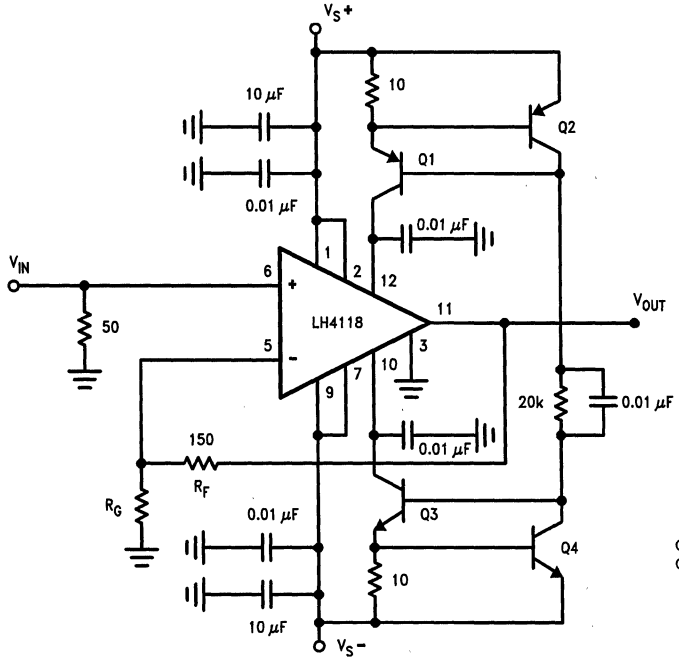
3

Typical Applications (Continued)



TL/K/9768–10

FIGURE 5. Current Limiting Using Resistor



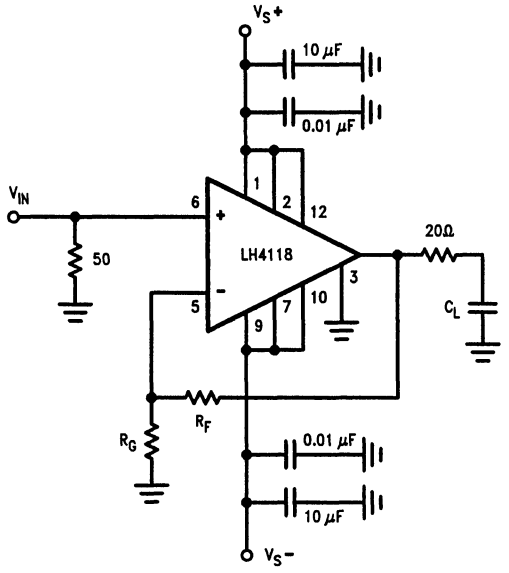
Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

TL/K/9768–11

The current cutoff is set to $I = \frac{VBE}{R} = \frac{600\ mV}{10\Omega} = 60$ mA. Higher current peaks are sustained by the 0.01 μF Capacitors.

FIGURE 6. Current Limiting Using Transistor Current Source

Typical Applications (Continued)

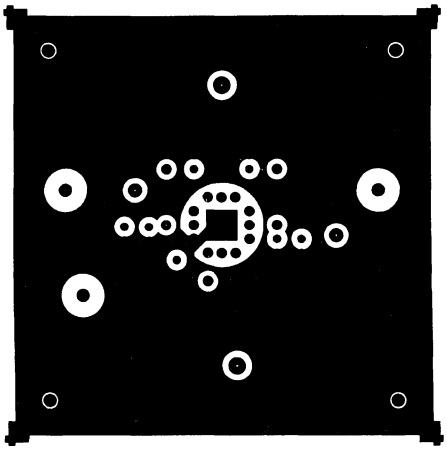


TL/K/9768–12

A series resistor between 5Ω and 50Ω helps to stabilize capacitive loads. There is, however, a corresponding drop in bandwidth.

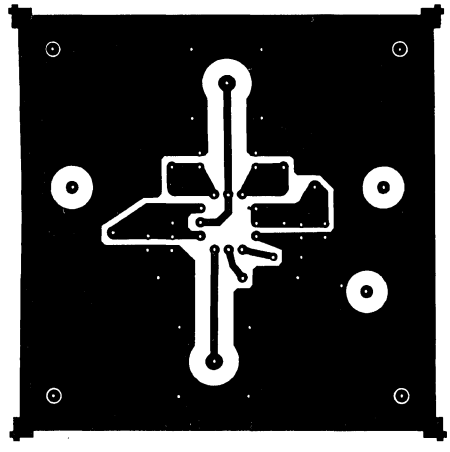
Evaluation Board

(3" x 3", not to scale)



TL/K/9768–13

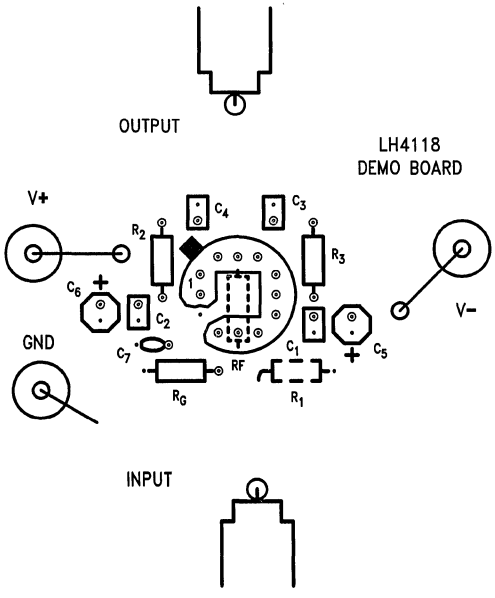
Top



TL/K/9768–14

Bottom

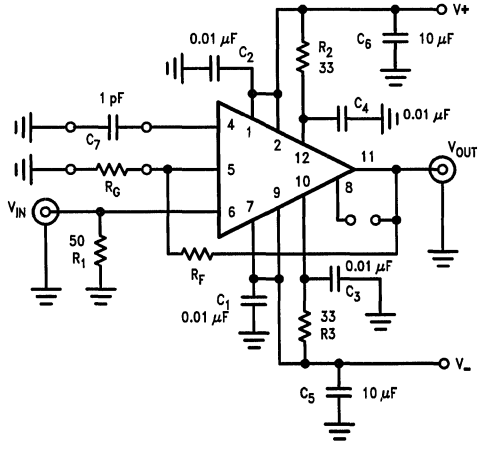
Components



TL/K/9768–15

Top View

Schematic Diagram



TL/K/9768–16

Input and output connections are made through BNC connectors. When the indicated cut-outs are made, the connectors can be placed in-line. As an alternative, Amphenol No. 31-4758 connectors can be used soldered upright into the board.

R1 is the termination resistor of the input line. It is mounted on the bottom of the board, with one side soldered flat to the center of the input strip-line.

The LH4118 can be soldered directly into the board or Hole-tight pins can be used (Augat part No. 8134-HC-5P2). These pins need plated through holes with a finished inner diameter of 41 ±2 Mil. For $A_V = 1$ the built-in R_F (150Ω) can be utilized by bridging the trace between pins 8 and 11. In this case no external R_F should be used.

National Semiconductor

LH4124C High Slew Rate Operational Amplifier

General Description

The LH4124C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers for A/D and D/A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

The LH4124C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH4124C is guaranteed over the temperature range −25°C to +85°C.

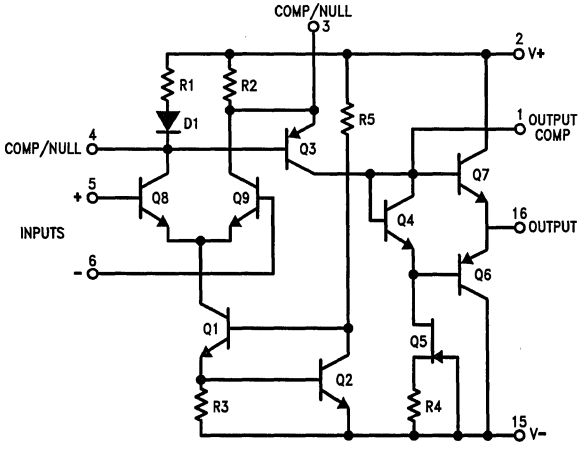
Features

■ Very high slew rate	500 V/μs at Av = +1
■ Wide small signal bandwidth	70 MHz
■ Wide large signal bandwidth	15 MHz
■ High output swing—	±12V into 1k
■ Offset null with single pot	
■ Low input offset	2 mV

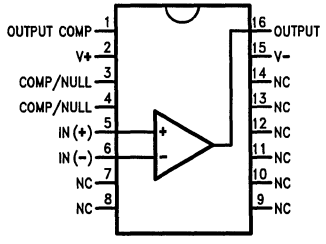
Applications

- Flash A/D input buffer
- Video amplifier
- High frequency oscillator
- Active filter

Schematic and Connection Diagrams



TL/K/10031-1



TL/K/10031-5

Top View

Order Number LH4124CN
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Input Voltage	Equal to Supply
Differential Input Voltage	±5V
Power Dissipation	600 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD	TBD

DC Electrical Characteristics (Notes 1, 2)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ $R_S = 50\Omega$		5.0	8.0 10.0	mV mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm 15V$, $R_S = 50\Omega$ −25°C to +85°C		25		μV/°C
Input Offset Current	$T_A = 25°C$		4.0	15.0 20.0	μA μA
Input Bias Current	$T_A = 25°C$		18	40 50	μA μA
Supply Current	No Load		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm 15V$, $R_L = 1k$	3 2.5	4		V/mV V/mV
Input Voltage Range	$V_S = \pm 15V$	±12	±13		V
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm 15V$, $R_L = 1k$	±10 ±10	±13		V V
Slew Rate	$V_S = \pm 15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF $A_V = +1$, $T_A = 25°C$ (Note 3)	250	400		V/μs
Common Mode Rejection Ratio	$V_S = \pm 15V$, $\Delta V_{IN} = \pm 10V$ $R_S = 50\Omega$		60		dB
Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq \pm 18V$ $R_S = 50\Omega$		60		dB

Note 1: These specifications apply for $V_S = \pm 15V$.

Note 2: LH4124C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing. These limits are not used to calculate outgoing quality level.

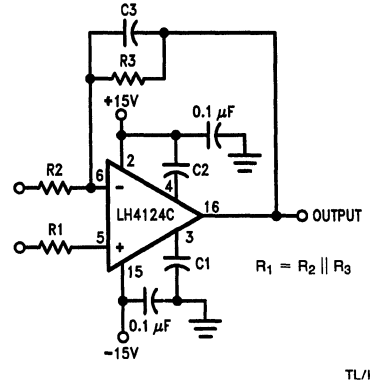
Note 3: Not 100% production tested, verified by sample testing only. Limits are not used to calculate outgoing quality level.

Frequency Compensation

TABLE I

Closed Loop Gain	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

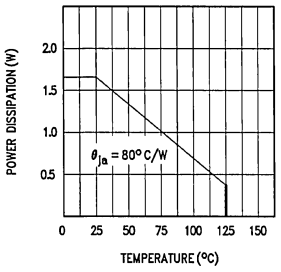
Frequency Compensation Circuit



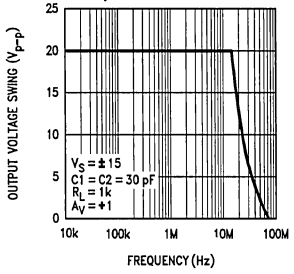
TL/K/10031–6

Typical Performance Characteristics

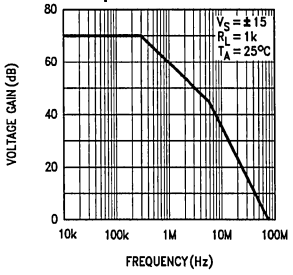
Package Power Dissipation



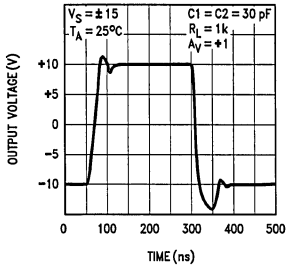
Large Signal Frequency Response



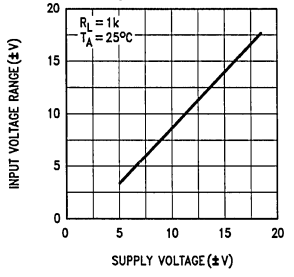
Open Loop Frequency Response



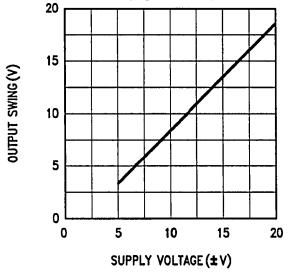
Voltage Follower Pulse Response



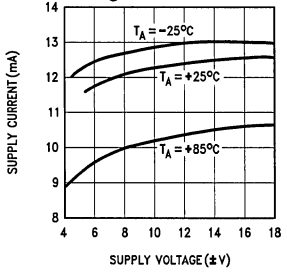
Input Voltage vs Supply Voltage



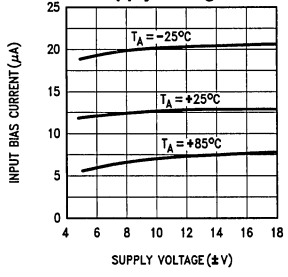
Output Voltage Swing vs Supply Voltage



Supply Current vs Supply Voltage



Input Bias Current vs Supply Voltage



TL/K/10031–7

Applications Information

1.0 Layout Considerations

The LH4124C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be bypassed as close to the device as possible with at least 0.01 μF ceramic capacitor. Compensating capacitors should also be placed as close to the device as possible.

2.0 Compensation Recommendations

Compensation schemes recommended in Table I work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH4124C or cause the device to oscillate. Slight adjustments in the values for C1, C2 and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

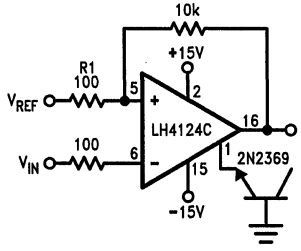
When operating the LH4124C at a gain of +1, the value of R1 should be at least 1 kΩ.

3.0 Heat Sinking

The LH4124C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink.

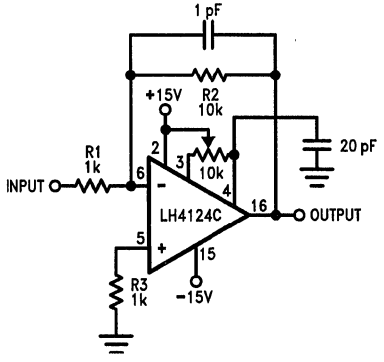
Typical Applications

TTL Compatible Comparator



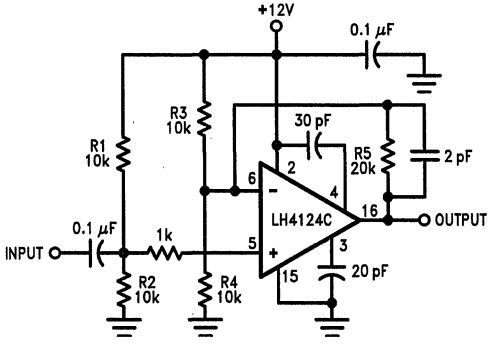
TL/K/10031–2

Offset Null



TL/K/10031–3

Video Amplifier



TL/K/10031–4

National Semiconductor

LH4141C
0.2 Amp Power Operational Amplifier

General Description

The LH4141C is a general purpose operational amplifier capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH4141C delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. The devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

The LH4141C is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

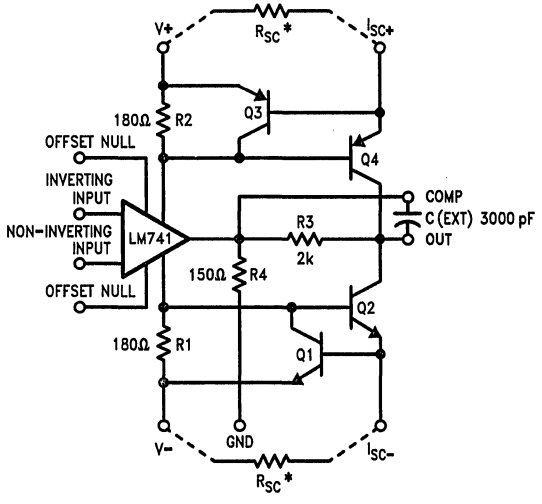
Features

■ Output current	0.2 Amp
■ Output voltage swing	±14V into 100Ω
■ Wide full power bandwidth	15 kHz
■ Low standby power	100 mW at ±15V
■ Low input offset voltage and current	1 mV and 20 nA
■ High slew rate	3.0 V/μs
■ High open loop gain	100 dB

Applications

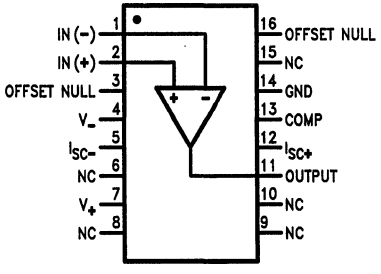
- Yoke driver
- Programmable power supplies
- Cable driver
- Servo amplifier

Schematic and Connection Diagrams



TL/K/10009–1

*R_{SC} is an external short circuit current limiting resistor.



TL/K/10009–2

Order Number LH4141CN
See NS Package Number N16A

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	See Curves
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Peak Output Current (Note 2)	0.5 Amp
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics (Notes 4 & 5)

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		5		μV/°C
Offset Voltage Drift with Time			5		μV/Week
Offset Voltage Change with Output Power			15		μV/W
Offset Voltage Adjustment Range			20		mV
Input Offset Current	$T_A = 25°C$		50	200 500	nA nA
Offset Current Drift with Temperature			0.2	1.0	nA/°C
Offset Current Drift with Time			2		nA/Week
Input Bias Current	$T_A = 25°C$		200	500 1.0	nA μA
Input Resistance	$T_A = 25°C$	0.3	1.0		MΩ
Input Capacitance			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	 100 20	 200 	 	 V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0V$		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0V$		90	120	mW

AC Electrical Characteristics (Note 7), $T_A = 25°C$, $V_S = \pm 15V$, $C_C = 3000\ pF$

Parameter	Conditions	Limits			Units
		Min	Typ	Max	
Slew Rate	$A_V = +1$, $R_L = 100\Omega$	1.0	3.0		V/μs
Power Bandwidth	$R_L = 100\Omega$		20		kHz
Small Signal Transient Response			0.3	1.5	μs
Small Signal Overshoot			10	30	%
Settling Time (0.1%)	$\Delta V_{IN} = 10V$, $A_V = +1$		4		μs
Overload Recovery Time			3		μs
Harmonic Distortion	f = 1 kHz, $P_O = 0.5W$		0.2		%
Input Noise Voltage	$R_S = 50\Omega$, B.W. = 10 Hz to 10 kHz		5		μV(rms)
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05		nA(rms)

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for $R_{SC} = 0\Omega$.

Note 3: Rating applies as long as package power dissipation rating is not exceeded.

Note 4: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$, and $-25°C \leq T_C \leq +85°C$ unless otherwise specified. Typical values are for 25°C only.

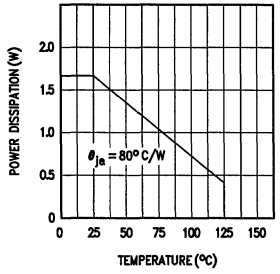
Note 5: LH4141C is 100% production tested at 25°C only, specifications at temperature extremes are verified by sample testing but these limits are not used to calculate outgoing quality level.

Note 6: Rating applies for $R_{SC} = 3.3\Omega$.

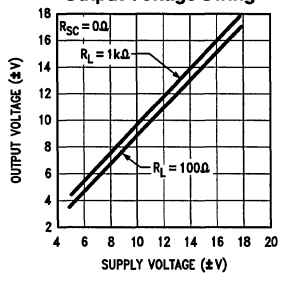
Note 7: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

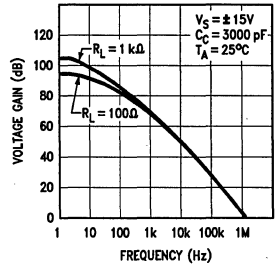
Package Power Dissipation



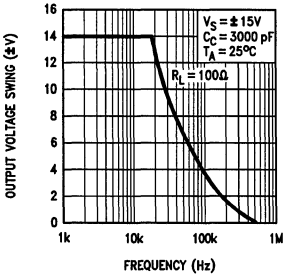
Output Voltage Swing



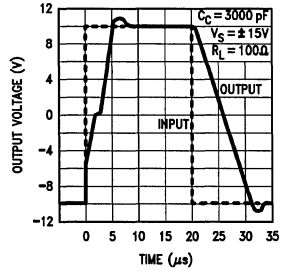
Open Loop Frequency Response



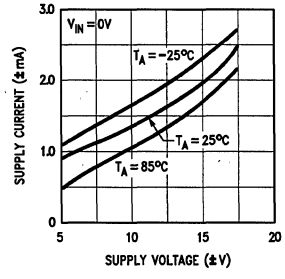
Large Signal Frequency Response



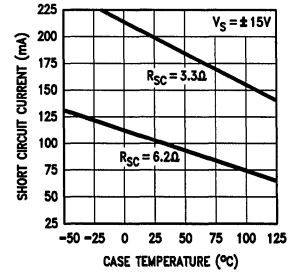
Voltage Follower Pulse Response



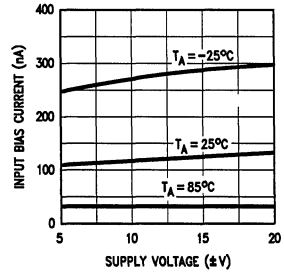
No Load Supply Current



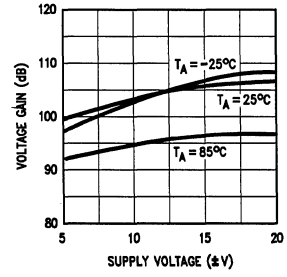
Short Circuit Current vs Temperature



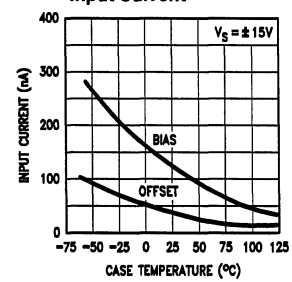
Input Bias Current



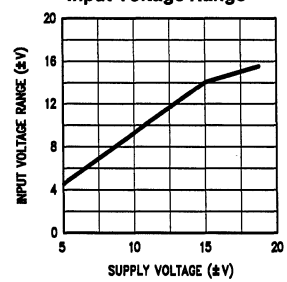
Voltage Gain



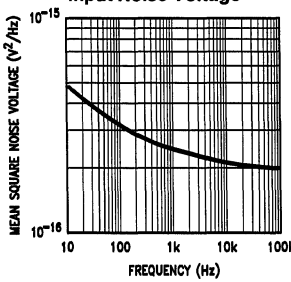
Input Current



Input Voltage Range



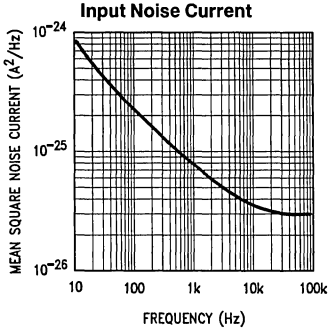
Input Noise Voltage



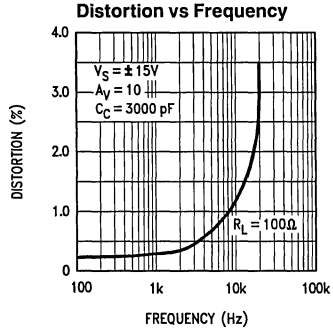
TL/K/10009–3

Typical Performance Characteristics (Continued)

Input Noise Current



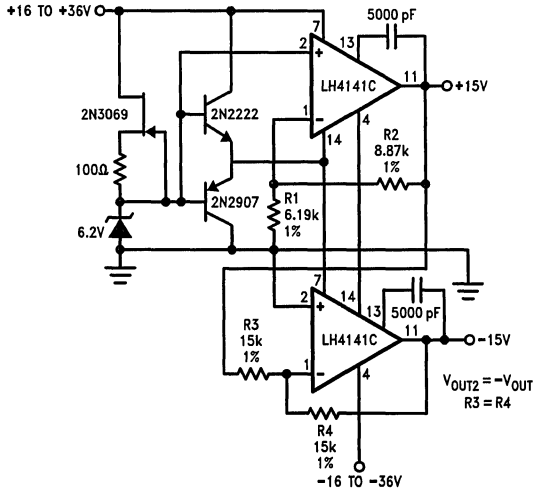
Distortion vs Frequency



TL/K/10009–4

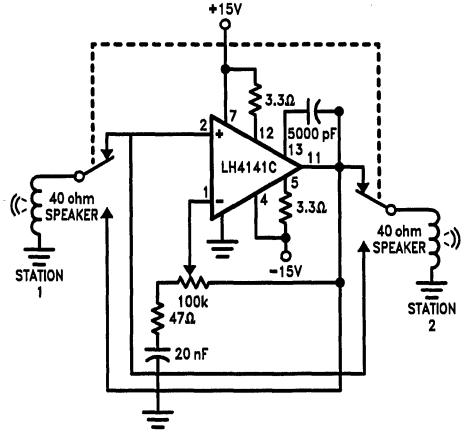
Typical Applications

Dual Tracking One Amp Power Supply



TL/K/10009–5

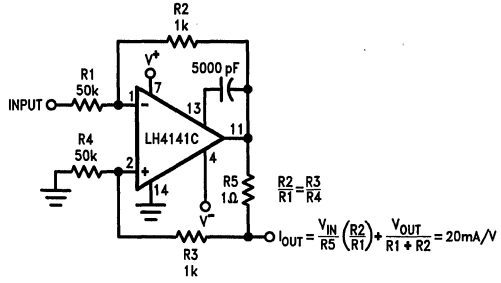
Two Way Intercom



TL/K/10009–6

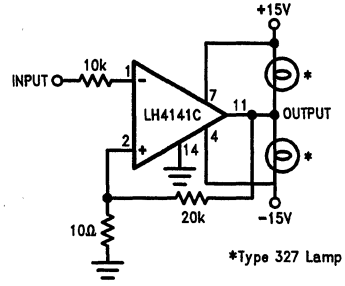
Typical Applications (Continued)

Programmable High Current Source/Sink



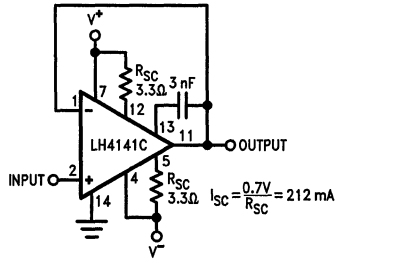
TL/K/10009–7

Power Comparator



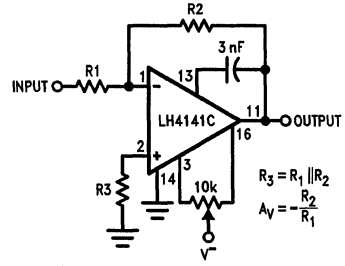
TL/K/10009–8

Unity Gain Circuit with Short Circuit Limiting



TL/K/10009–9

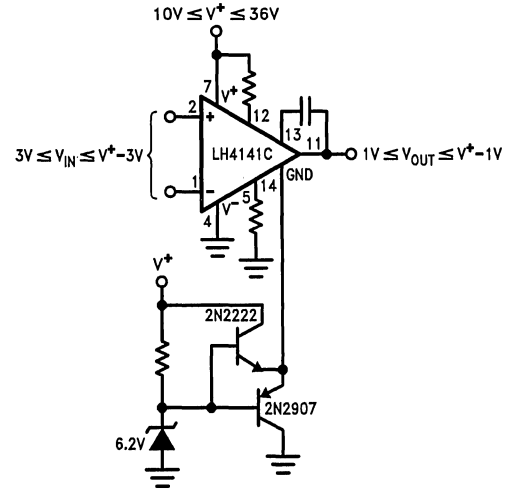
Offset Voltage Null Circuit*



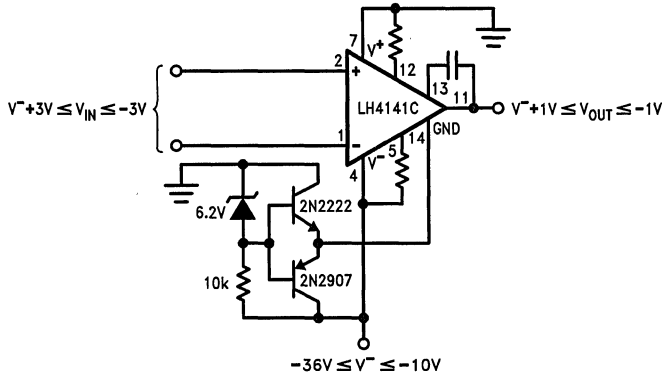
TL/K/10009–10

Typical Applications (Continued)

Operation from Single Supplies

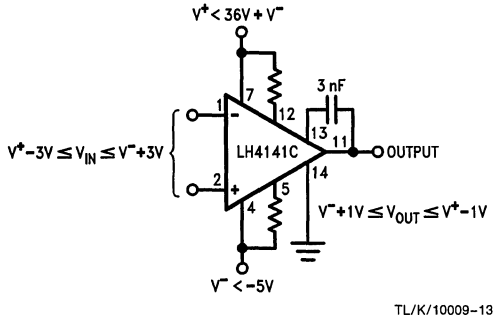


TL/K/10009-11

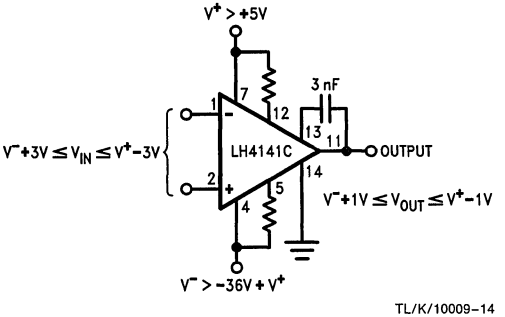


TL/K/10009-12

Operation from Non-Symmetrical Supplies



TL/K/10009-13



TL/K/10009-14

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

PRELIMINARY

LH4161A/LH4161/LH4161C
High Speed Operational Amplifier

General Description

The LH4161 high-speed amplifier exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high-speed performance without the need for complex and expensive dielectric isolation.

In addition, they are precision laser trimmed to guarantee low offset voltage.

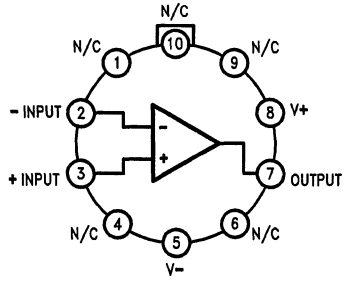
Features

■ High slew rate	300 V/μs
■ High unity gain freq	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved, easy to apply	
■ Low offset voltage	±1 mV
■ Pin compatible with LM6161	

Applications

- Low differential gain and phase amplifier
- Fast pulse amplifier
- High frequency filters and oscillators

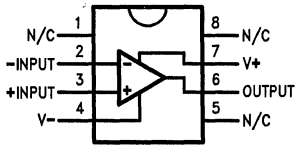
Connection Diagrams



TL/K/9767-1

Top View

Order Number LH4161AH, LH4161H or LH4161CH
See NS Package Number H10F



TL/K/9767-2

Top View

Order Number LH4161AJ, LH4161J or LH4161CJ
See NS Package Number J08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) 36V

Differential Input Voltage (Note 8) ±8V

CM Voltage ($V^+ - 0.7V$) to ($V^- - 7V$)

Output Short Circuit to GND (Note 1) Continuous

Lead Temperature (Soldering, 10 sec.) 260°C

Storage Temperature Range −65°C to +150°C

Operating Temperature Range (Note 2)
LH4161A/LH4161 −55°C to +125°C
LH4161C −25°C to +85°C

Max. Junction Temperature 150°C

ESD Tolerance (Notes 8 and 9) ±700V

Operating Supply Voltage Range 4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LH4161A		LH4161		LH4161C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		0.5	1 **3**		2 **5**		4	**6**	mV Max
Input Offset Voltage Average Drift		10							µV/°C
Input Bias Current		2	3 **6**		3 **6**		5	**6**	µA Max
Input Offset Current		150	350 **800**		350 **800**		1500	**1900**	nA Max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	$A_V = +1$ @ 10 MHz	1.5							pF
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\,k\Omega$ (Note 11)	750	550 **300**		550 **300**		400	**350**	V/V Min
	$R_L = 10\,k\Omega$	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9 **+13.8**		+13.8	**+13.7**	V Min
		−13.2	−12.9 **−12.7**		−12.9 **−12.7**		−12.8	**−12.7**	V Min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9 **3.8**		3.8	**3.7**	V Min
		1.8	2.0 **2.2**		2.0 **2.2**		2.1	**2.2**	V Max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**		80 **74**		72	**70**	dB Min
Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	90	80 **74**		80 **74**		72	**70**	dB Min
Output Voltage Swing	Supply = ±15V and $R_L = 2\,k\Omega$	+14.2	+13.5 **+13.3**		+13.5 **+13.3**		+13.4	**+13.3**	V Min
		−13.4	−13.0 **−12.7**		−13.0 **−12.7**		−12.9	**−12.8**	V Min
	Supply = +5V and $R_L = 2\,k\Omega$ (Note 6)	4.2	3.5 **3.3**		3.5 **3.3**		3.4	**3.3**	V Min
		1.3	1.7 **2.0**		1.7 **2.0**		1.8	**1.9**	V Max
Output Short Circuit Current	Source	65	30 **20**		30 **20**		30	**25**	mA Min
	Sink	65	30 **20**		30 **20**		30	**25**	mA Min
Supply Current		5.0	6.5 **6.8**		6.5 **6.8**		6.8	**6.9**	mA Max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LH4161A		LH4161		LH4161C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@F = 20 MHz	50	40		40		35		MHz
	Supply = ±5V	35							Min
Slew Rate	A_V = +1 (Note 10)	300	225		225		200		V/μs Min
	Supply = ±5V	200							V/μs
Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5							MHz
Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, A_V = +4	<0.1							%
Differential Phase	NTSC, A_V = +4	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							$nV/\sqrt{Hz}$
Input Noise Current	f = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the cerdip (J) package is 125°C/W, and the TO-5 (H) package is 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$ with supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100$ kΩ. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_J$ in the "Absolute Maximum Ratings" section.

Note 4: Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

Note 5: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 6: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V.

Note 7: $C_L \leq 5$ pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS} and Noise).

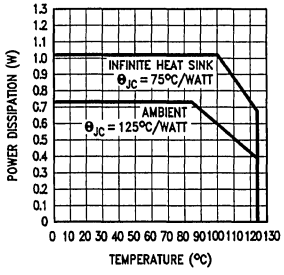
Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 10: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

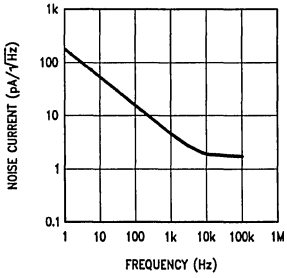
Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Typical Performance Characteristics R_L = 10k and T_A = 25°C unless otherwise specified

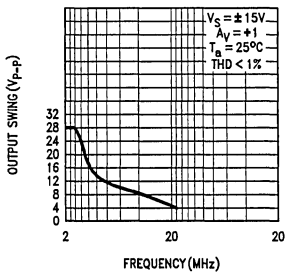
Power Dissipation Curve



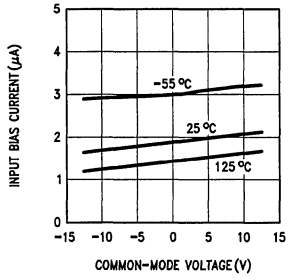
Input Current Noise



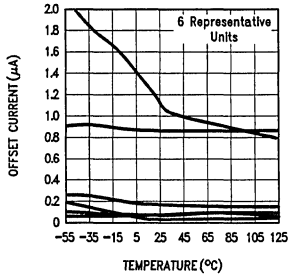
Power Bandwidth



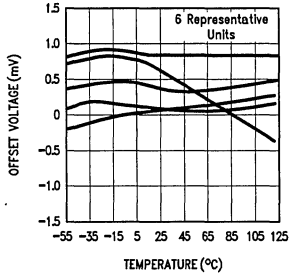
Bias Current vs Common-Mode Voltage



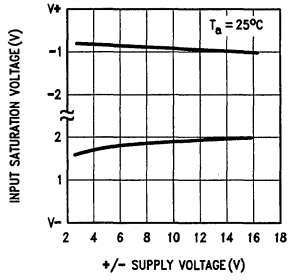
Input Offset Current



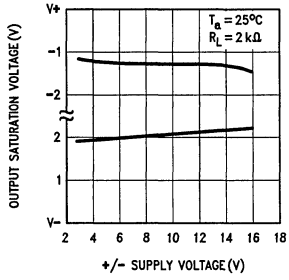
Input Offset Voltage



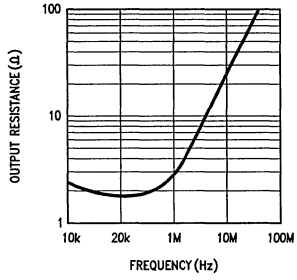
Common-Mode Input Saturation Voltage



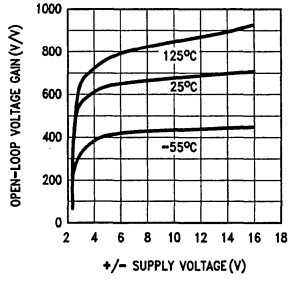
Output Saturation Voltage



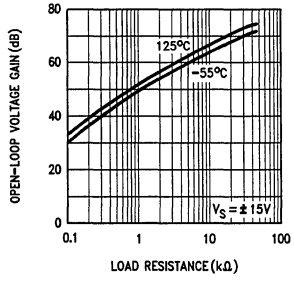
Output Resistance



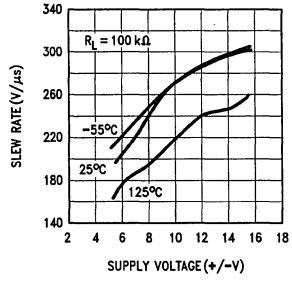
Gain vs Supply Voltage



Voltage Gain vs Load Resistance



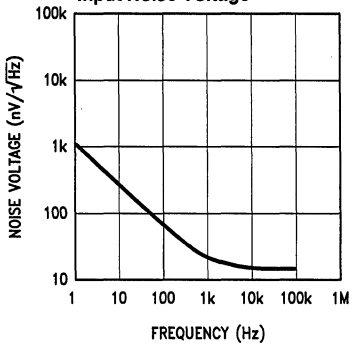
Positive Slew Rate



TL/K/9767–5

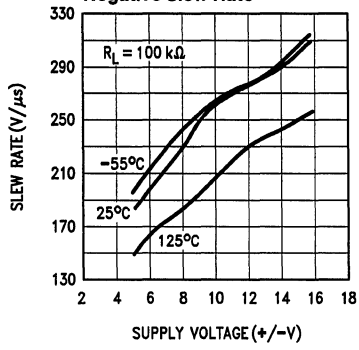
Typical Performance Characteristics (Continued)

Input Noise Voltage



TL/K/9767–4

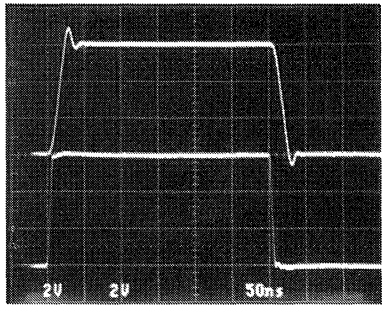
Negative Slew Rate



TL/K/9767–6

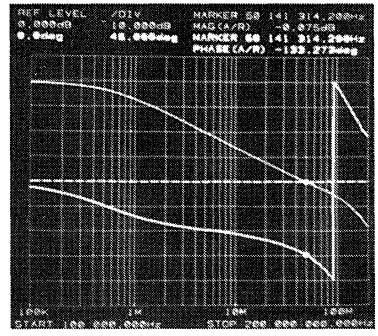
Typical AC Characteristics

Step Response; $A_V = +1$



TL/K/9767–7

Gain & Phase; $A_V = +100$



TL/K/9767–8

Application Hints

The LH4161 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains.

The LH4161 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). However, load capacitance on the LH4161 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth.

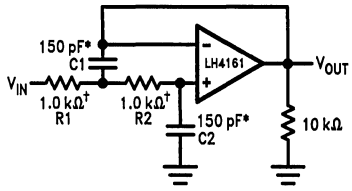
Power supply bypassing is not as critical for the LH4161 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LH4161, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 to 10 μF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

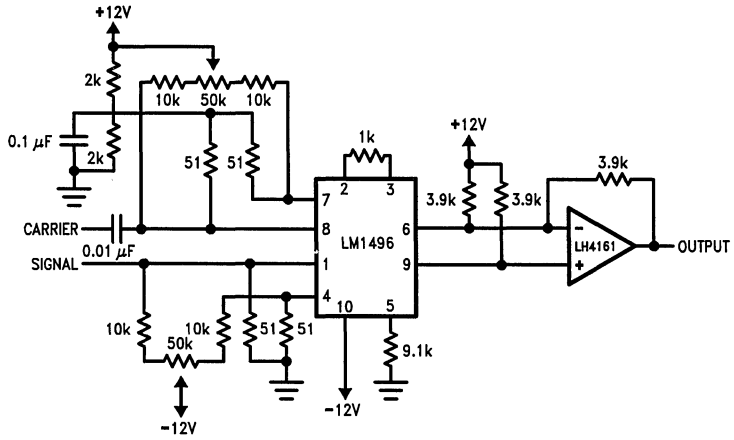
1 MHz Low-Pass Filter
$f_C = 1/2\pi\sqrt{(R_1R_2C_1C_2)}$



TL/K/9767–9

† 1% tolerance
*Matching determines filter precision

Modulator with Differential-to-Single-Ended Converter



TL/K/9767–10

National Semiconductor

PRELIMINARY

LH4162A/LH4162/LH4162C
Dual High Speed Operational Amplifier

General Description

The LH4162 high-speed amplifier exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's new VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high-speed performance without the need for complex and expensive dielectric isolation.

In addition, they are precision laser trimmed to guarantee low offset voltage.

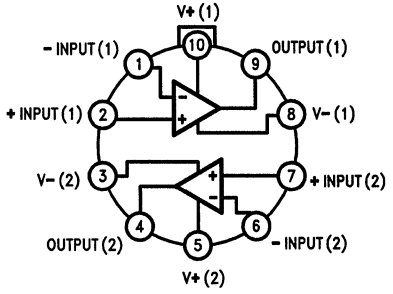
Features

■ High slew rate	300 V/μs
■ High unity gain frequency	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved, easy to apply	
■ Low offset voltage	±1 mV

Applications

- Low differential gain and phase video amplifiers
- Fast pulse amplifiers
- High frequency filters and oscillators

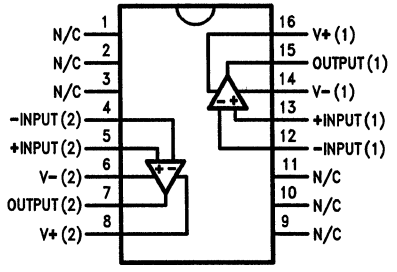
Connection Diagrams



TL/K/9769-1

Top View

Order Number LH4162AH, LH4162H or LH4162CH
See NS Package Number H10F



TL/K/9769-2

Top View

Order Number LH4162AJ, LH4162J or LH4162CJ
See NS Package Number J16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) 36V

Differential Input Voltage (Note 8) ±8V

CM Voltage ($V^+ - 0.7V$) to ($V^- - 7V$)

Output Short Circuit to GND (Note 1) Continuous

Lead Temperature (Soldering, 10 sec.) 260°C

Storage Temperature Range −65°C to +150°C

Operating Temperature Range (Note 2)

LH4162A/LH4162 −55°C to +125°C

LH4162C −25°C to +85°C

Max. Junction Temperature 150°C

ESD Tolerance (Notes 8 and 9) ±700V

Operating Supply Voltage Range 4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LH4162A		LH4162		LH4162C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		0.5	2 **4**		3 **6**		4	**6**	mV Max
Input Offset Voltage Average Drift		10							μV/°C
Input Bias Current		2	3 **6**		3 **6**		5	**6**	μA Max
Input Offset Current		150	350 **800**		350 **800**		1500	**1900**	nA Max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	A_V = +1 @ 10 MHz	1.5							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	750	550 **300**		550 **300**		400	**350**	V/V Min
	R_L = 10 kΩ	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9 **+13.8**		+13.8	**+13.7**	V Min
		−13.2	−12.9 **−12.7**		−12.9 **−12.7**		−12.8	**−12.7**	V Min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9 **3.8**		3.8	**3.7**	V Min
		1.8	2.0 **2.2**		2.0 **2.2**		2.1	**2.2**	V Max
Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	94	80 **74**		80 **74**		72	**70**	dB Min
Power Supply Rejection Ratio	±10V ≤ $V^{\pm}$ ≤ ±16V	90	80 **74**		80 **74**		72	**70**	dB (Min)
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5 **+13.3**		+13.4	**+13.3**	V Min
		−13.4	−13.0 **−12.7**		−13.0 **−12.7**		−12.9	**−12.8**	V Min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5 **3.3**		3.4	**3.3**	V Min
		1.3	1.7 **2.0**		1.7 **2.0**		1.8	**1.9**	V Max
Output Short Circuit Current	Source	65	30 **20**		30 **20**		30	**25**	mA Min
	Sink	65	30 **20**		30 **20**		30	**25**	mA Min
Supply Current	Per Amplifier	5.0	6.5 **6.8**		6.5 **6.8**		6.8	**6.9**	mA Max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LH4162A		LH4162		LH4162C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@F = 20 MHz	50	40		40		35		MHz Min
	$V^+ = \pm 5V$	35							MHz
Slew Rate	$A_V = +1$ (Note 10)	300	225		225		200		V/μs Min
	$V^+ = \pm 5V$	200							V/μs
Power Bandwidth	$V_{OUT} = 20\ V_{PP}$	4.5							MHz
Settling Time	10V Step to 0.1% $A_V = -1$, $R_L = 2\ k\Omega$	120							ns
Phase Margin		45	3						Deg
Differential Gain	NTSC, $A_V = +4$	<0.1							%
Differential Phase	NTSC, $A_V = +4$	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							nV/√Hz
Input Noise Current	f = 10 kHz	1.5							pA/√HZ

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the cerdip (J) package is 85°C/W, and the TO-5 (H) package is 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$ with supply voltage = ±15V, $V_{CM} = 0V$, and $R_L \geq 100\ k\Omega$. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_J$ in the "Absolute Maximum Ratings" section.

Note 4: Guaranteed and 100% production tested. These limits are used to calculate outgoing AQL levels.

Note 5: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 6: For single supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$.

Note 7: $C_L \leq 5$ pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS} and Noise).

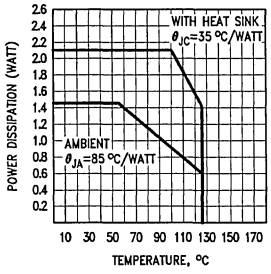
Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 10: $V_{IN} = 8V$ step. For supply = ±5V, $V_{IN} = 5V$ step.

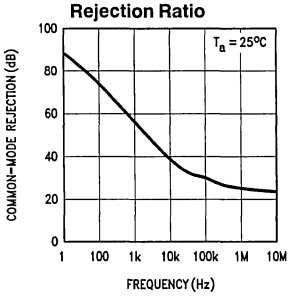
Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Typical Performance Characteristics R_L = 10k and T_A = 25°C unless otherwise specified

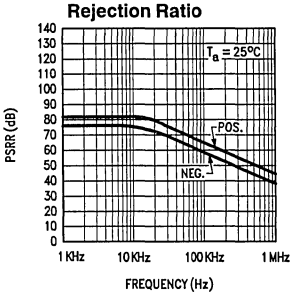
Power Dissipation Curve



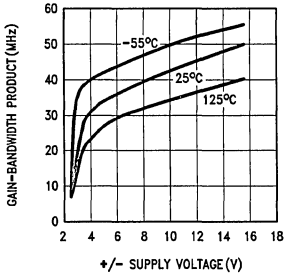
Common-Mode Rejection Ratio



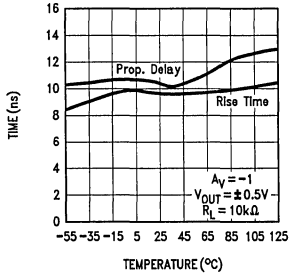
Power Supply Rejection Ratio



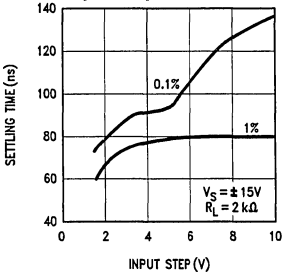
Gain-Bandwidth Product



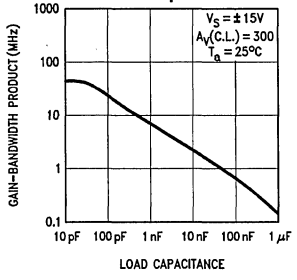
Propagation Delay and Rise Time



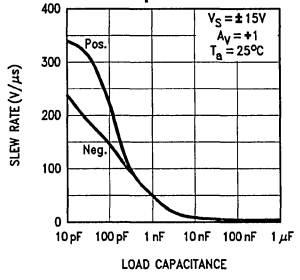
Settling Time vs Input Step



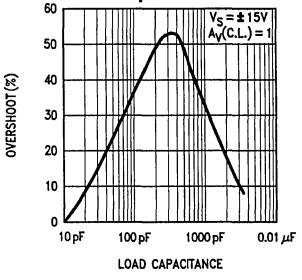
Gain-Bandwidth Product vs Load Capacitance



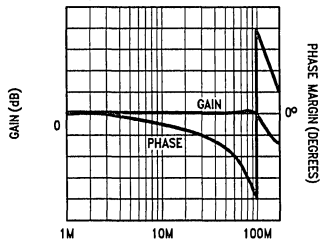
Slew Rate vs Load Capacitance



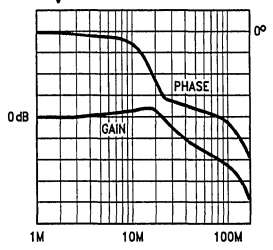
Overshoot vs Load Capacitance



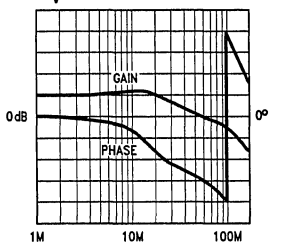
Frequency Response, A_V = +1 (Follower)



Frequency Response, A_V = −1



Frequency Response, A_V = +3



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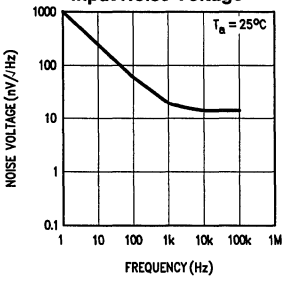
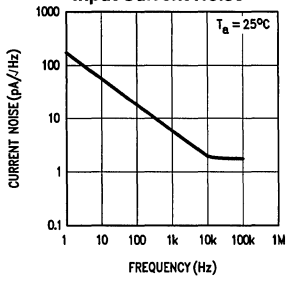
Typical Performance Characteristics (Continued)

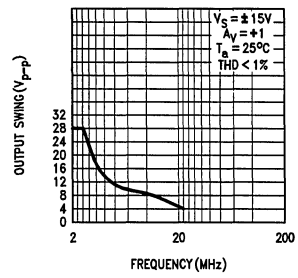
Input Noise Voltage



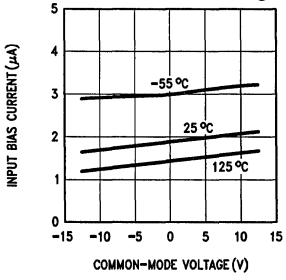
Input Current Noise



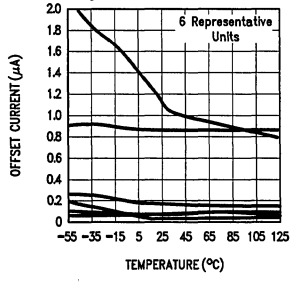
Power Bandwidth



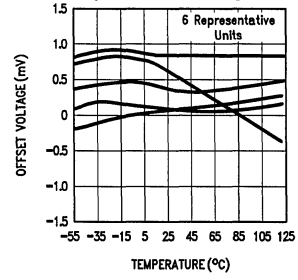
Bias Current vs Common-Mode Voltage



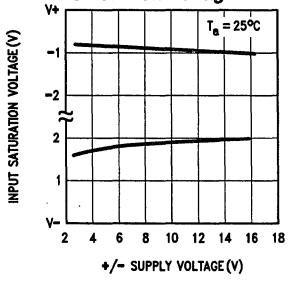
Input Offset Current



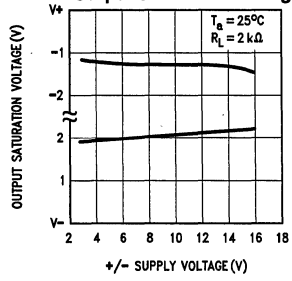
Input Offset Voltage



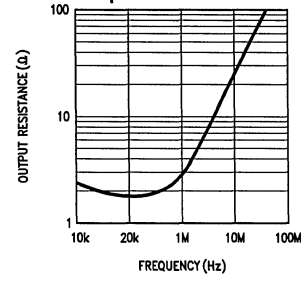
Common-Mode Input Saturation Voltage



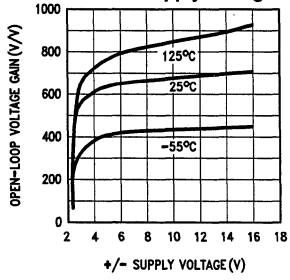
Output Saturation Voltage



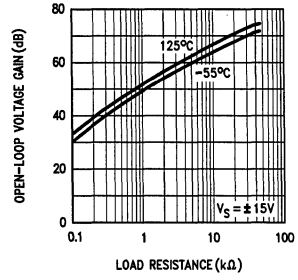
Output Resistance



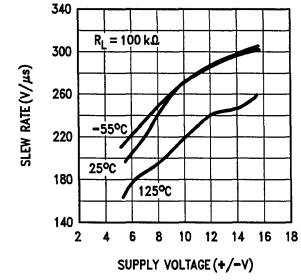
Gain vs Supply Voltage



Voltage Gain vs Load Resistance



Positive Slew Rate



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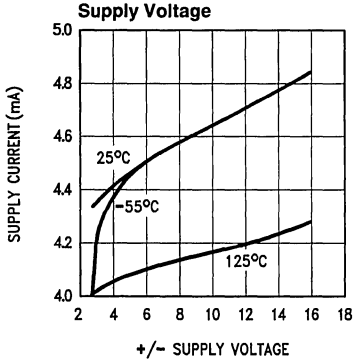
Typical Performance Characteristics (Continued)

Supply Current vs Supply Voltage



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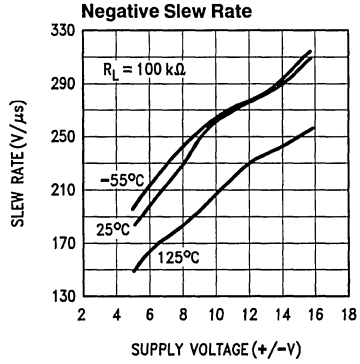
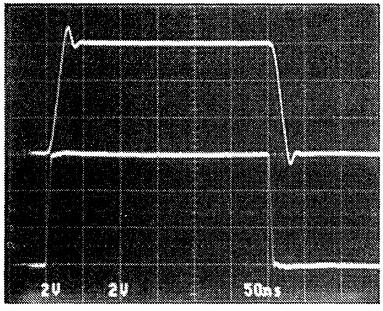
Negative Slew Rate



TL/K/9769-5

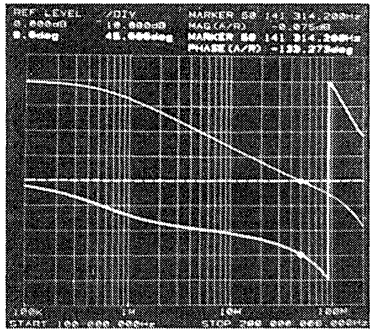
Typical AC Characteristics

Step Response; $A_V = +1$



TL/K/9769-8

Gain & Phase; $A_V = +100$



TL/K/9769-9

Application Hints

The LH4162 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains.

The LH4162 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). However, load capacitance on the LH4162 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth.

Power supply bypassing is not as critical for the LH4162 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LH4162 and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may be required for extra noise reduction.

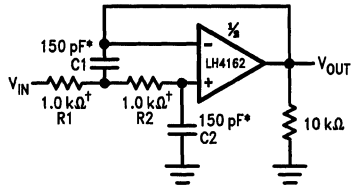
Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

1 MHz Low-Phase Filter

$f_C = 1/2\pi\sqrt{(R_1 R_2 C_1 C_2)}$



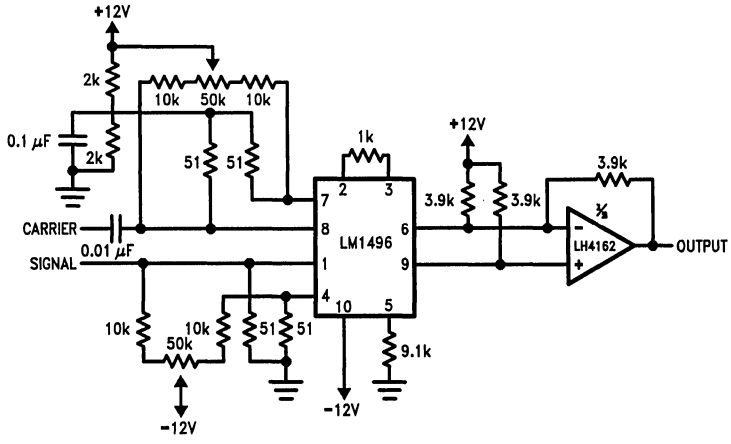
TL/K/9769–10

†1% tolerance

*Matching determines filter precision

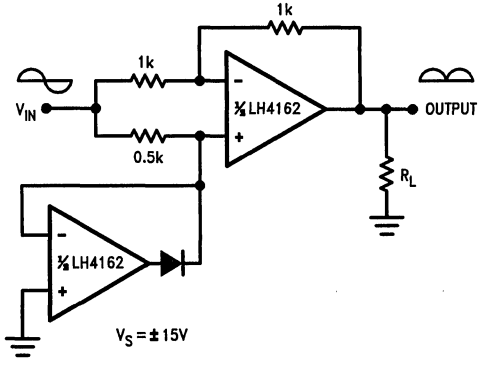
Typical Applications (Continued)

Modulator with Differential-to-Single-Ended Converter



TL/K/9769–11

Full Wave Rectifier



TL/K/9769–12

National Semiconductor

PRELIMINARY

LH4200 General Purpose GaAs FET Amplifier

General Description

This is a general purpose low noise, AC coupled, high frequency amplifier useful for applications from 500 KHz to 1 GHz. It features a Gallium Arsenide input stage for high frequency performance and bipolar second and third stages for low output impedance. Series feedback may be provided for gain stabilization and input impedance improvement. A control input is available to vary the open loop gain of the amplifier making it useful for AGC and mixer applications.

Features

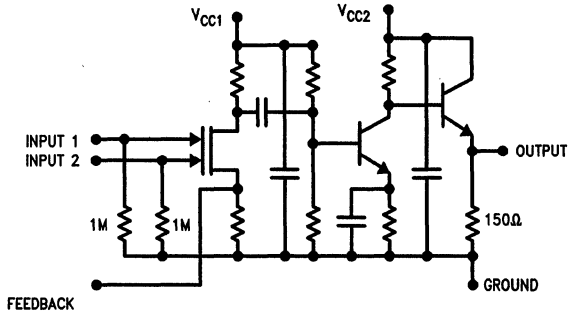
- High gain — 38 dB at 100 MHz
- Wide AGC range — 60 dB at 100 MHz
- High input impedance — 1 MΩ
- Low noise figure — 3 dB, 50Ω

Applications

- Voltage Controlled Amplifiers
- Feedback Stabilized Amplifiers
- Mixer-Amplifiers
- HF-UHF Oscillators
- Video Diode Receivers
- Fiber Optics

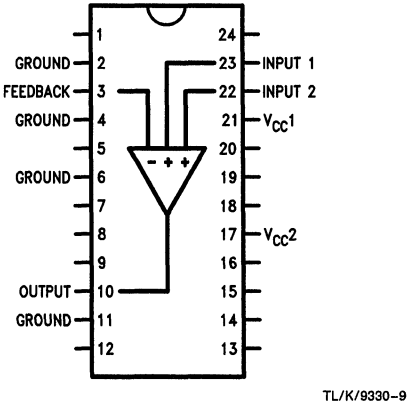
Simplified Schematic

High Frequency Amplifier



TL/K/9330–1

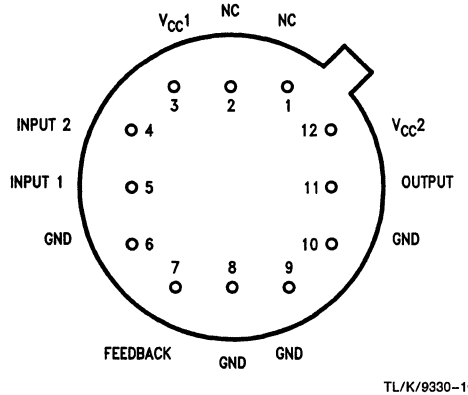
Connection Diagrams



TL/K/9330–9

Top View

Order Number LH4200CD
See NS Package Number D24D



TL/K/9330–10

Top View

Order Number LH4200G
See NS Package Number G12B

Note: Unspecified pins are No Connection.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC1}, V_{CC2})	12V
Power Dissipation (P_D) at T_A = 25°C	980 mW
Output Current (I_O)	40 mA
Voltage	
Input 1	+1.4 to −4V
Input 2	+2.5 to −4V
Operating Temperature Range	
LH4200C	−25°C to +85°C
LH4200G	−55°C to +125°C
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	150°C
Lead Temperature (Soldering < 10 sec.)	300°C
ESD Tolerance (Note 1)	150V

DC Electrical Characteristics

Unless otherwise specified. V_{CC} = V_{CO} = 10V, R_S = 50Ω, R_L = 50Ω, T_A = 25°C (Note 4)

Symbol	Description	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
V_{10}	Output Bias Voltage		5		**4.5**	V (Min)
V_3	FET Source Bias	V_{IN1} = V_{IN2} = 0V	0.6	0.5	**0.4**	V (Min)
V_0	Output Voltage Swing	100 kHz	3			V_{P-P}
I_S	Supply Current		45	70		mA (Max)
Z_{IN}	Input Impedance		1 Meg	200k		Ω (Min)

AC Electrical Characteristics

Unless otherwise specified. V_S = 10V, R_S = 50Ω, R_L = 50Ω, T_A = 25°C (Note 4)

Symbol	Description	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
S21	Power Gain (Note 4)	10 MHz V_{IN1} = 0V, V_{IN2} = +1.5V	50	42		dB
		100 MHz V_{IN1} = 0V, V_{IN2} = +1.5V	37	30		dB
		500 MHz V_{IN1} = 0V, V_{IN2} = +1.5V	18	14		dB
		1000 MHz V_{IN1} = 0V, V_{IN2} = +1.5V	3			dB
P_1	Power Output @1 dB Compression	10 MHz	15	12		dBm
		100 MHz	14	10		dBm
		500 MHz	6	4		dBm
		1000 MHz	1			dBm
	AGC Range	100 MHz, V_{G2} = −2V	60			dB
NF	Noise Figure	10–500 MHz, R_S = 50	3			dB
		R_S = 800	2			dB

Note 1: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Boldface limits are guaranteed over full temperature range.

Note 4: These measurements are taken with the LH4200 open loop.

General Information

The LH4200 is useful for a variety of RF, VHF, and UHF applications including feedback, AGC amplifiers, and signal sources. The amplifier is internally bypassed for good high frequency performance, but should be bypassed externally with a large (10 μF aluminum electrolytic or better) capacitor to prevent low frequency stability (oscillation) problems.

The amplifier has three inputs: Two high impedance gates for signal input, and a low impedance source for series mode Feedback (Pin 3).

Normally, Input 1 is used as the signal input while Input 2 is used to control the gain of the amplifier for those applications using Automatic Gain Control (AGC). Gain control ranges of over 60 dB are possible to 100 MHz. Input 2 is biased at +1.5V for maximum gain and −2V for minimum gain. Input 2 and Feedback (Pin 3) are normally bypassed with 0.01 μF capacitors for maximim gain.

The second gate, Input 2 may be used as a second isolated input for small signal operation. The open loop gain from this input is approximately 6 dB less than from Input 1.

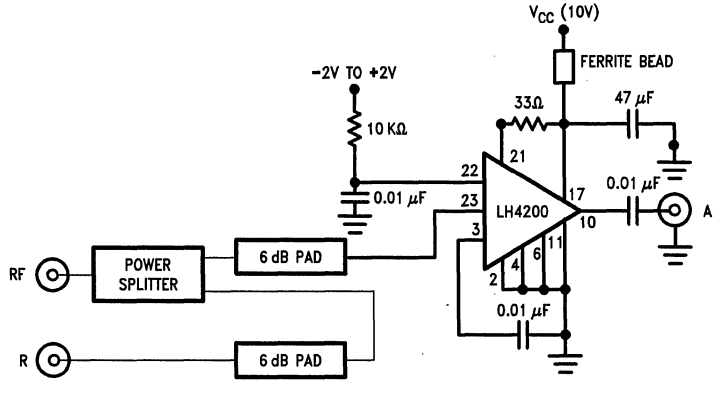
The LH4200 may be used as a feedback amplifier, in which case, the third input, Feedback, is connected to the output with a suitable resistor to set the overall power gain. In this manner, voltage series feedback is used to establish the power gain and increase input impedance. A typical connection is shown along with the feedback components needed to achieve several different gain settings. (See *Figure 5.*)

The performance of the LH4200 degrades from ideal above 250 MHz as indicated by the S parameters. The input impedance decreases and is capacitive while the output impedance increases and is inductive. For maximum performance in the 250 MHz to 900 MHz area, some performance improvement can be obtained with suitable matching networks.

LH4200 TYPICAL S PARAMETERS

$V_{CC1} = V_{CC2} = 10V$, $V_{Input\ 2} = 1.5V$

Frequency	S11		S21		S12	S22	
MHz	Mag	Ang	dB	Ang	dB	Mag	Ang
10	0.96	−0.5	50	−49	−48	0.99	181
100	0.97	−15	36	−130	−45	0.93	152
250	0.86	−32	26	150	−43	0.93	115
500	0.64	−62	18	39	−40	0.82	73
750	0.41	−105	10	70	−33	0.7	52
1000	0.23	168	3.5	−160	−37	0.71	42



TL/K/9330–2

Note: Pinout shown for D24D package.

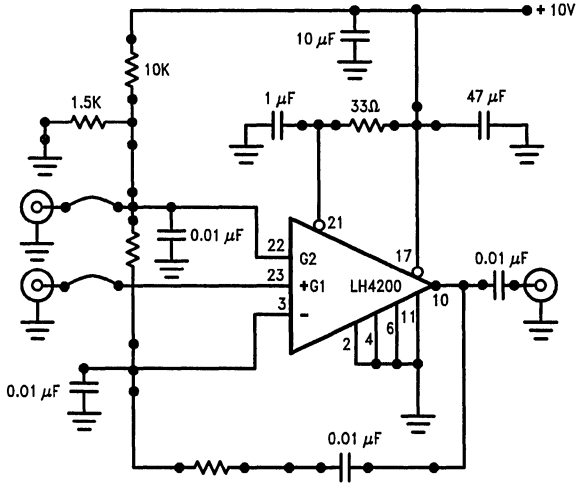
Ferrite Bead

Stackpole 57 0257

RF, R, A: HP8505A Network Analyzer Connections

FIGURE 1. S21 Measurement Circuit

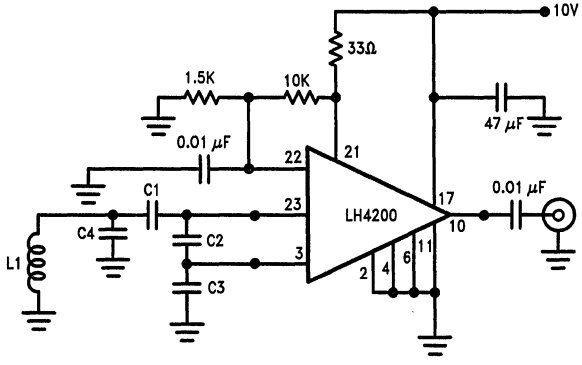
General Information (Continued)



TL/K/9330–3

Note: Pinout shown for D24D package.

FIGURE 2. Applications Board



TL/K/9330–4

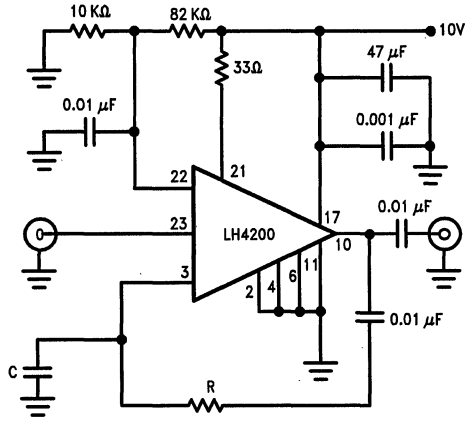
Note: Pinout shown for D24D package.

FIGURE 3. VHF-UHF Oscillator

General Information (Continued)

The LH4200 may be used as a Colpitts Oscillator to above 500 MHz (see *Figure 3*). It is stable and features load isolation and will provide +15 dBm to a 50Ω load. Capacitors C2 and C3 provide feedback from source to gate of the input GaAs FET. The resonator network, L1–C4, is coupled to the active device through C1. Approximate values suitable for beginning design are:

Frequency	C1	C2	C3	L1
MHz	pF	pF	pF	nH
75–150	5	30	60	150
150–300	3	6	10	100
300–500	1.5	3	6	50

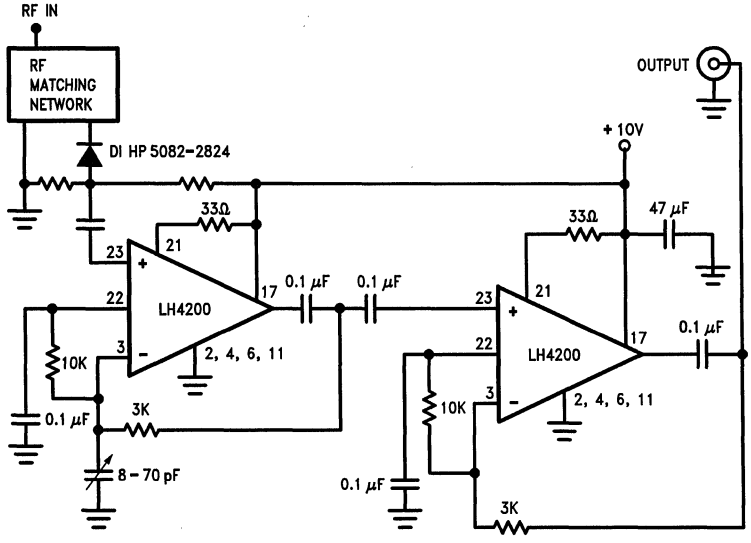


TL/K/9330–5

Note: Pinout shown for D24D package.

FIGURE 5. Feedback Amplifier

Gain	Bandwidth	R	C
30 dB	150 MHz	1.5k	9–30 pF
25 dB	300 MHz	860Ω	2–8 pF
20 dB	500 MHz	430Ω	<1 pF



TL/K/9330–6

Note: Pinout shown for D24D package.

FIGURE 6. Video Diode Receiver (Opto or RF)

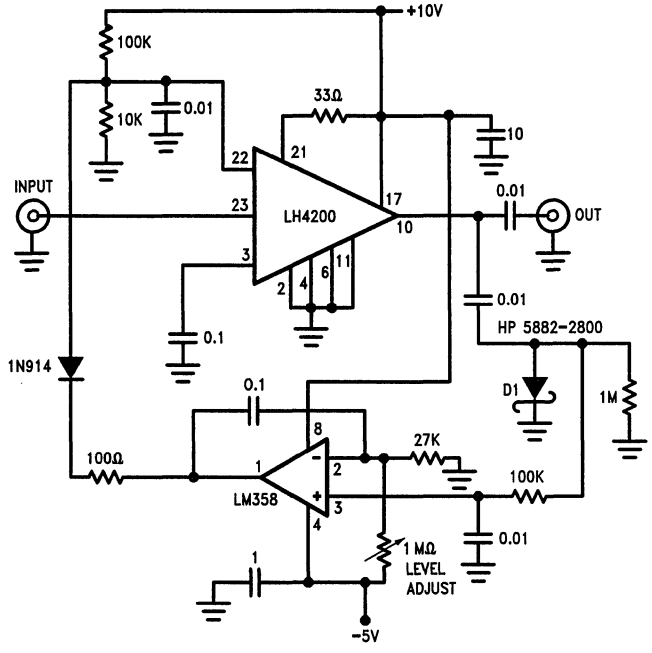
LH4200 Video Diode Receiver

The LH4200 may be used for crystal video receiver applications (see *Figure 6*). Crystal video receivers, although much less sensitive than their superhetrodyne counterparts, offer the advantage of simplicity. Typical applications include receivers for radar beacons, missile guidance, fuze activation and countermeasures; as well as signal monitoring and power leveling detectors.

This circuit shows two LH4200 amplifiers cascaded to provide a gain of 60 dB with a bandwidth of over 100 MHz. Series mode feedback provides high input impedance over the operating frequency range and low noise figure from high source impedances. Measured noise figure is 7 dB from a 50Ω source and less than 4 dB from a 1 kΩ source.

AGC Application

This circuit provides a constant RF output signal level over a broad range of input signal levels (see *Figure 7*). Diode D1 provides a DC signal proportional to the RF output level. This signal is compared to a reference voltage at the input to the LM358, which in turn controls the voltage at Input 2, controlling the gain of the LH4200.



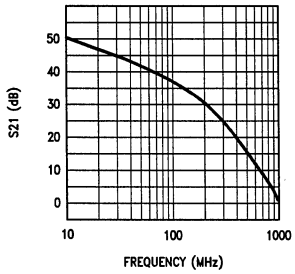
Note 1: Pinout shown for D24D package.

Note 2: All capacitance values are in microfarads.

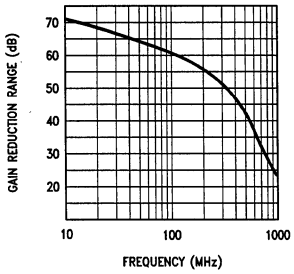
FIGURE 7. AGC Application

LH4200 Performance Characteristics

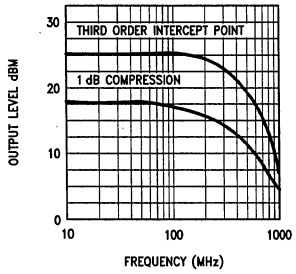
Gain vs. Frequency



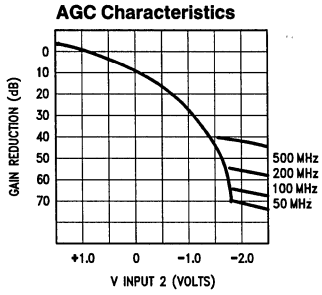
AGC Characteristics



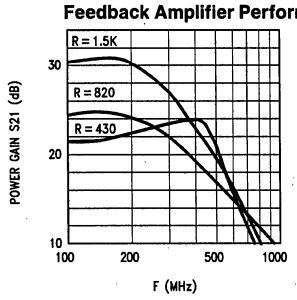
Signal Handling Capabilities



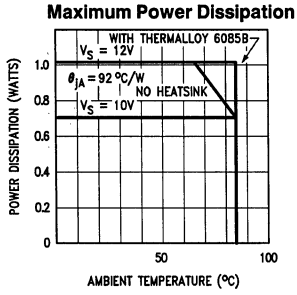
AGC Characteristics



Feedback Amplifier Performance



Maximum Power Dissipation



TL/K/9330–8

National Semiconductor

LM10/LM10B(L)/LM10C(L) Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

- input-offset voltage 2.0 mV (max)
- input-offset current 0.7 nA (max)
- input-bias current 20 nA (max)
- reference regulation 0.1% (max)
- offset-voltage drift 2μV/°C
- reference drift 0.002%/°C

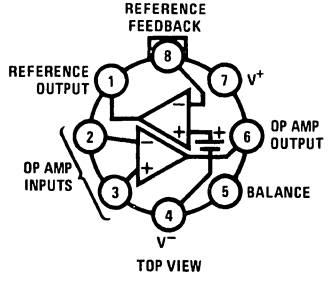
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

Metal Can Package (H)

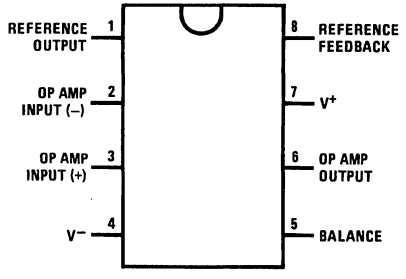


TOP VIEW

TL/H/5652–1

Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH
See NS Package Number H08A

Dual-In-Line Package (N)

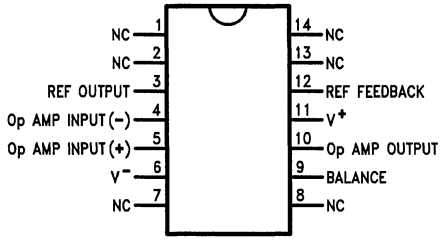


TOP VIEW

TL/H/5652–15

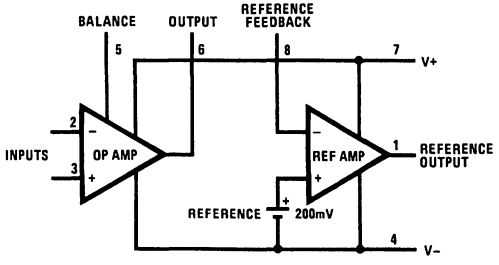
Order Number LM10CN or LM10CLN
See NS Package Number N08E

Small Outline Package (M)



TL/H/5652–17

Order Number LM10CWM or LM10CLWM
See NS Package Number M14B



TL/H/5652–16

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

	LM10/LM10B/LM10C	LM10BL/LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage (note 1)	±40V	±7V
Power Dissipation (note 2)	internally limited	
Output Short-circuit Duration (note 3)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds)		
Metal Can	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (note 4) **(Boldface type refers to limits over temperature range)**

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.25	0.7 **1.5**		0.4	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 20V$, $I_{OUT} = 0$ $V_{OUT} = \pm 19.95V$ $V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$ $I_{OUT} = \pm 20$ mA **(± 15 mA)** $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **(± 0.3V)**, $V_{CM} = -0.4V$	120 **80** 50 **20** 1.5 **0.5**	400 130 3.0 		80 **50** 25 **15** 1.0 **0.75**	400 130 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	1.2V **(1.3V)** ≤ V_{OUT} ≤ 40V, $R_L = 1.1$ kΩ 0.1 mA ≤ I_{OUT} ≤ 5 mA 1.5V ≤ V^+ ≤ 40V, $R_L = 250\Omega$ 0.1 mA ≤ I_{OUT} ≤ 20 mA	14 **6** 8 **4**	33 25 		10 **6** 6 **4**	33 25 		V/mV V/mV V/mV V/mV
Common-mode rejection	−20V ≤ V_{CM} ≤ 19.15V **(19V)** $V_S = \pm 20V$	93 **87**	102		90 **87**	102		dB dB
Supply-voltage rejection	−0.2V ≥ V^- ≥ −39V $V^+ = 1.0V$ **(1.1V)** 1.0V **(1.1V)** ≤ V^+ ≤ 39.8V $V^- = -0.2V$	90 **84** 96 **90**	96 106 		87 **84** 93 **90**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	$T_C < 100°C$		60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤ V_S ≤ 40V 0 ≤ I_{REF} ≤ 1.0 mA, $V_{REF} = 200$ mV		0.001	0.003 **0.006**		0.001	0.008 **0.01**	%/V %/V
Load regulation	0 ≤ I_{REF} ≤ 1.0 mA $V^+ - V_{REF} \ge 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Amplifier gain	$0.2V \le V_{REF} \le 35V$	50 **23**	75		25 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 **500**		300	500 **570**	μA μA
Supply current change	$1.2V$ **(1.3V)** $\le V_S \le 40V$		15	**75**		15	**75**	μA

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.1	0.7 **1.5**		0.2	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$ $V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75$ V $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **($\pm$0.3V)**, $V_{CM} = -0.4V$	60 **40** 10 **4** 1.5 **0.5**	300 25 3.0 		40 **25** 5 **3** 1.0 **0.75**	300 25 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	$1.5V \le V^+ \le 6.5V$, $R_L = 500\Omega$ $0.1\text{ mA} \le I_{OUT} \le 10$ mA	8 **4**	30		6 **4**	30		V/mV V/mV
Common-mode rejection	$-3.25V \le V_{CM} \le 2.4V$ **(2.25V)** $V_S = \pm 3.25V$	89 **83**	102		80 **74**	102		dB dB
Supply-voltage rejection	$-0.2V \ge V^- \ge -5.4V$ $V^+ = 1.0V$ **(1.2V)** 1.0V **(1.1V)** $\le V^+ \le 6.3V$ $V^- = 0.2V$	86 **80** 94 **88**	96 106 		80 **74** 80 **74**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	$1.2V$ **(1.3V)** $\le V_S \le 6.5V$ $0 \le I_{REF} \le 0.5$ mA, $V_{REF} = 200$ mV		0.001	0.01 **0.02**		0.001	0.02 **0.03**	%/V %/V
Load regulation	$0 \le I_{REF} \le 0.5$ mA $V^+ - V_{REF} \ge 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	$0.2V \le V_{REF} \le 5.5V$	30 **20**	70		20 **15**	70		V/mV V/mV

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 **500**		280	500 **570**	μA μA

Note 1: The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \approx 20$ ms), die heating ($\tau_2 \approx 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 7: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

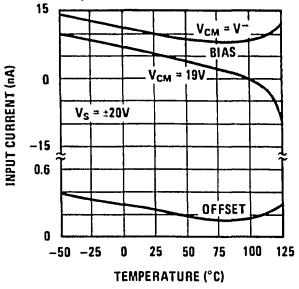
Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

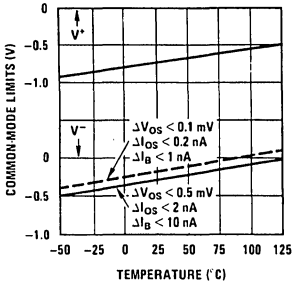
Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

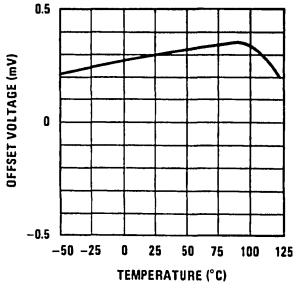
Input Current



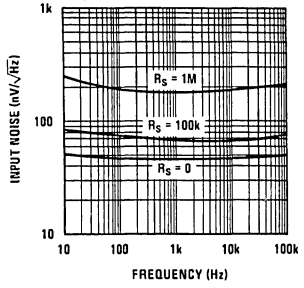
Common Mode Limits



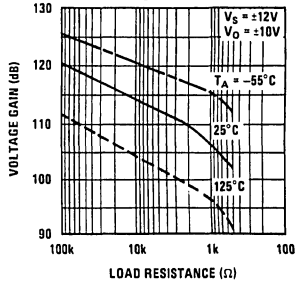
Offset Voltage Drift



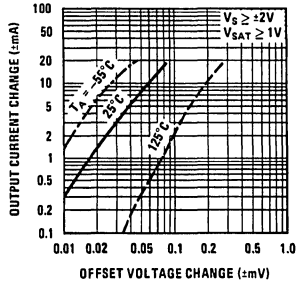
Input Noise Voltage



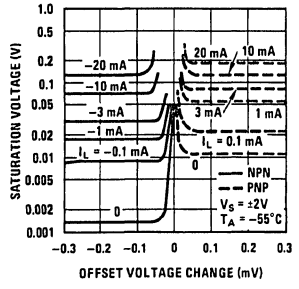
DC Voltage Gain



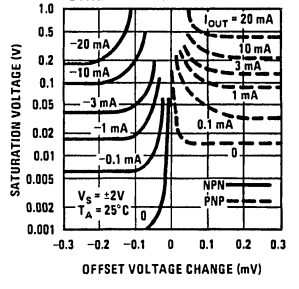
Transconductance



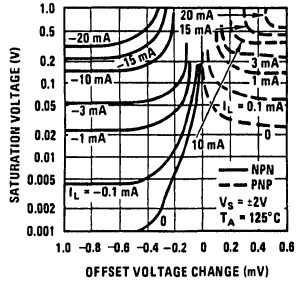
Output Saturation Characteristics



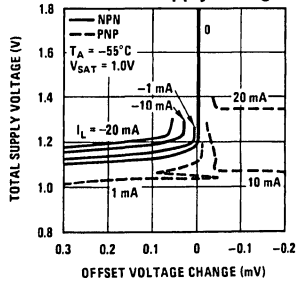
Output Saturation Characteristics



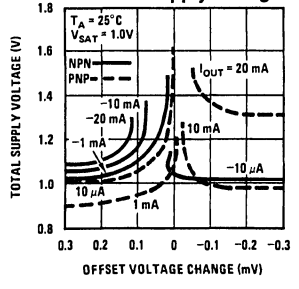
Output Saturation Characteristics



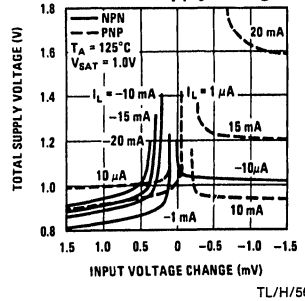
Minimum Supply Voltage



Minimum Supply Voltage



Minimum Supply Voltage



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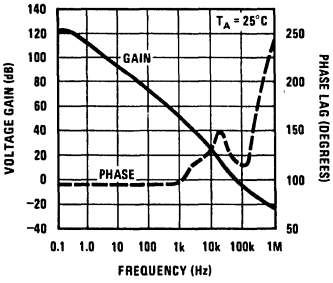
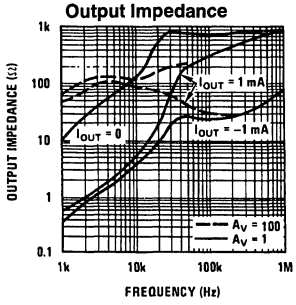
Typical Performance Characteristics (Op Amp) (Continued)

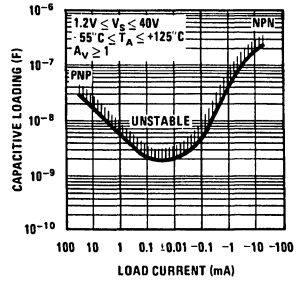
Frequency Response



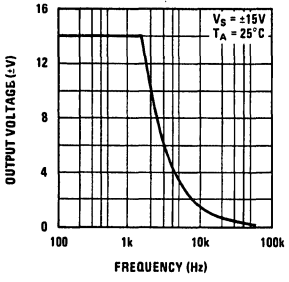
Output Impedance



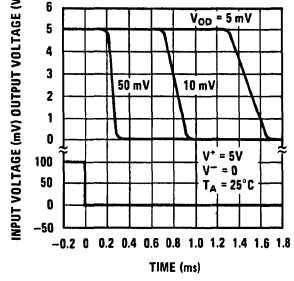
Typical Stability Range



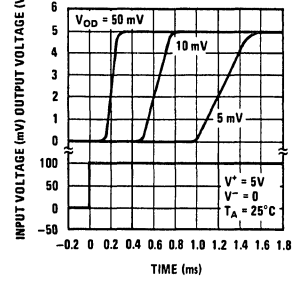
Large Signal Response



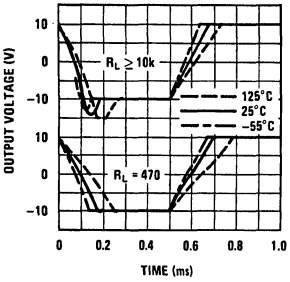
Comparator Response Time For Various Input Overdrives



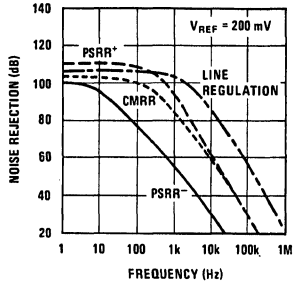
Comparator Response Time For Various Input Overdrives



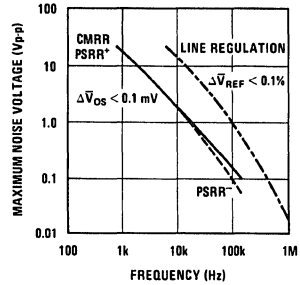
Follower Pulse Response



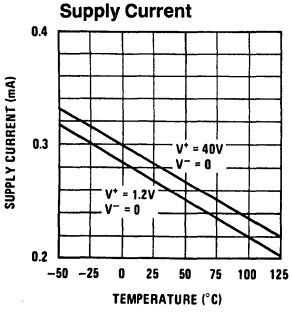
Noise Rejection



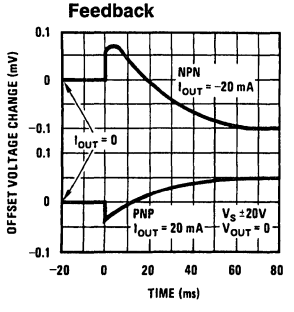
Rejection Slew Limiting



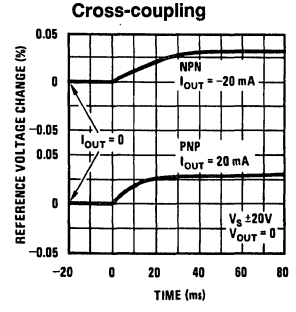
Supply Current



Thermal Gradient Feedback



Thermal Gradient Cross-coupling



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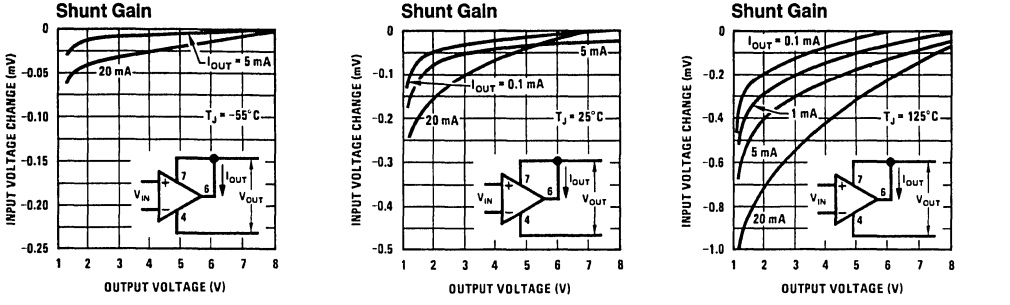
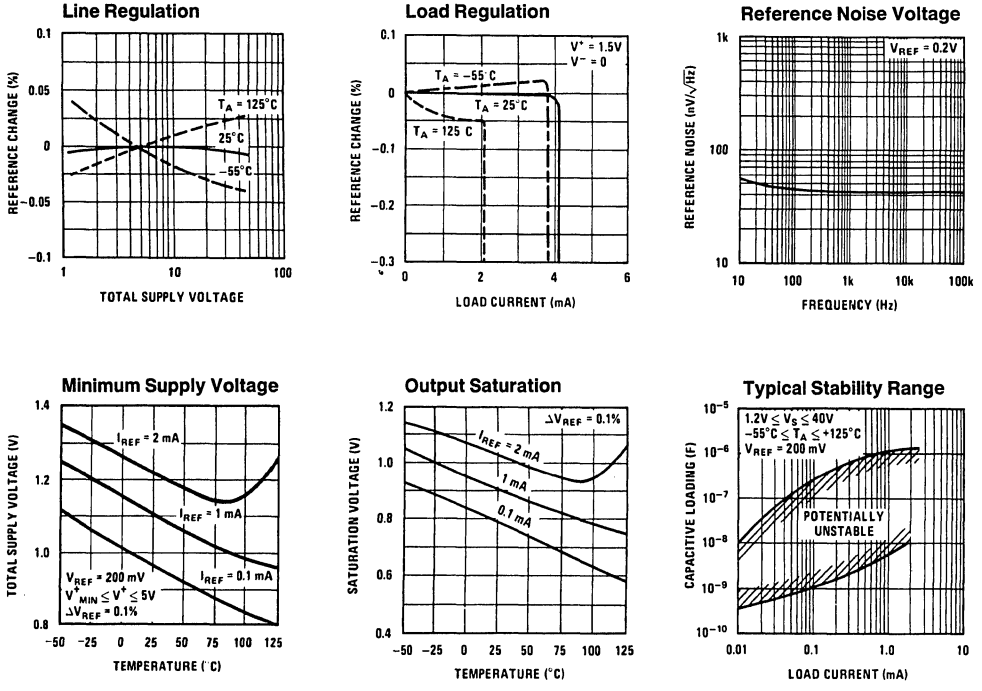
Typical Performance Characteristics (Op Amp) (Continued)



TL/H/5652–4

Typical Performance Characteristics (Reference)



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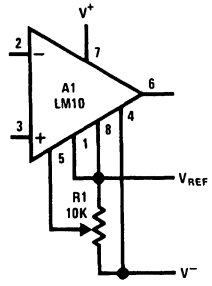
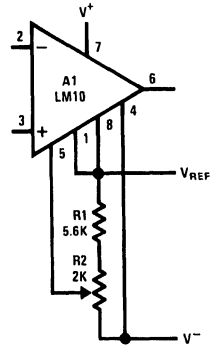
Typical Applications†† (Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment

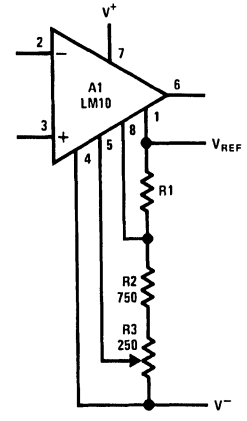
Standard



Limited Range

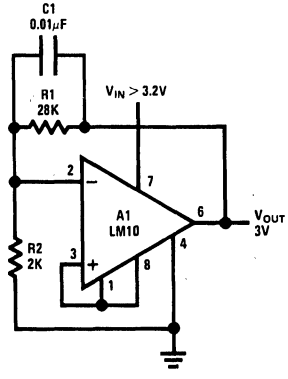


Limited Range With Boosted Reference

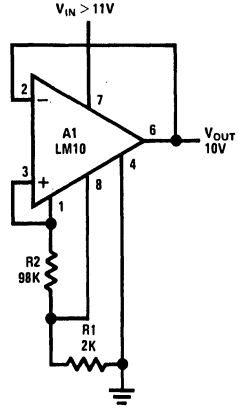


Positive Regulators†

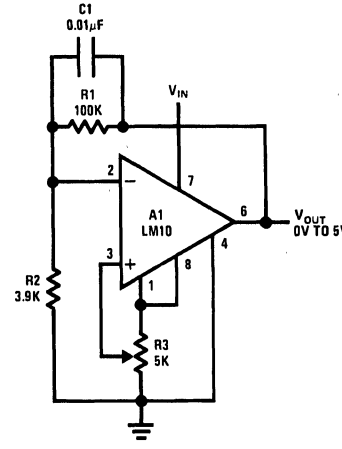
Low Voltage



Best Regulation



Zero Output



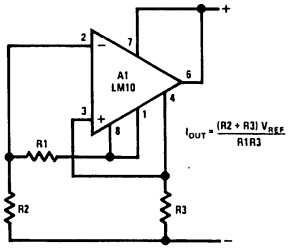
TL/H/5652–6

†Use only electrolytic output capacitors.

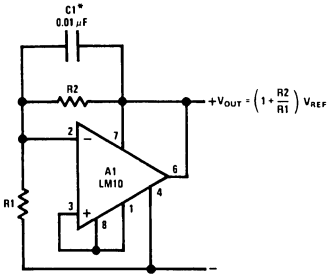
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

Current Regulator

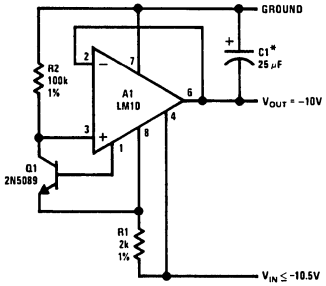


Shunt Regulator



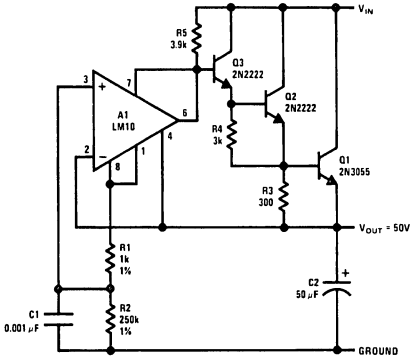
*Required For Capacitive Loading

Negative Regulator

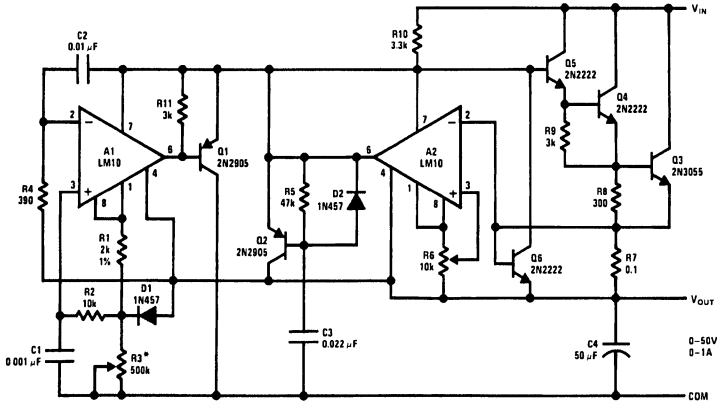


*Electrolytic

Precision Regulator



Laboratory Power Supply



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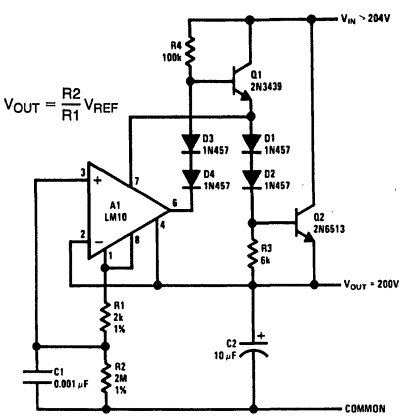
*$V_{OUT} = 10^{-4}$ R3

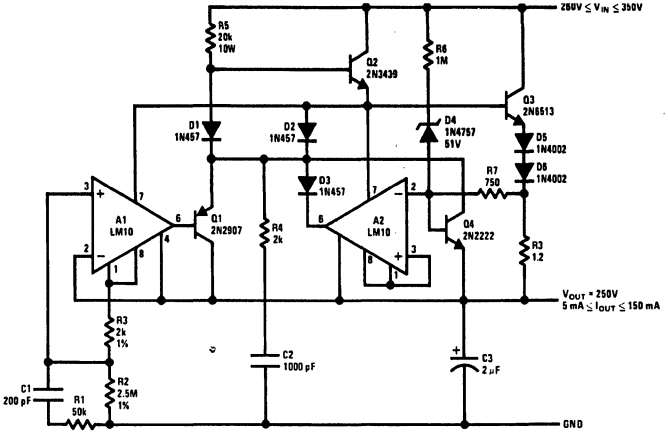
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

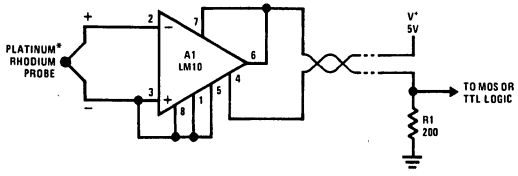
HV Regulator



Protected HV Regulator

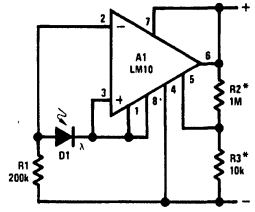


Flame Detector



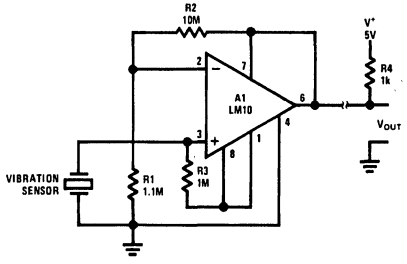
*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Light Level Sensor

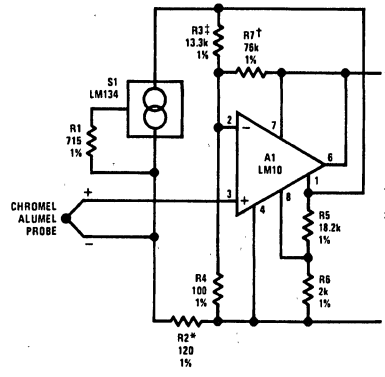


*Provides Hysteresis

Remote Amplifier



Remote Thermocouple Amplifier



$4V \leq V_{OUT} \leq 20V$
$200°C \leq T_P \leq 700°C$
†Span Trim
‡Level-shift Trim
*Cold-junction Trim

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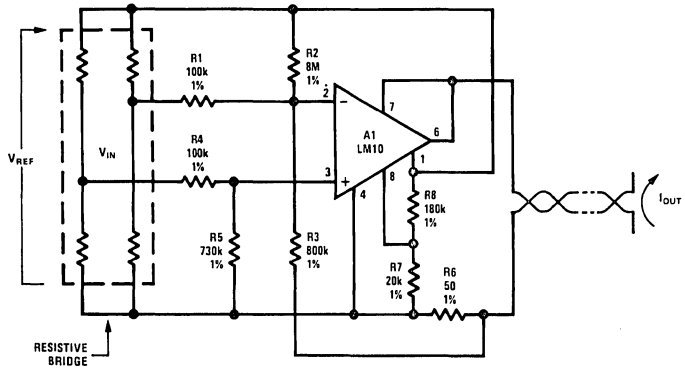
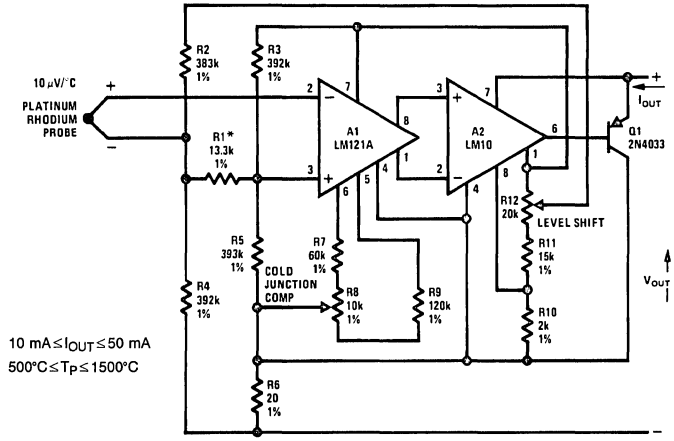
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Transmitter for Bridge Sensor

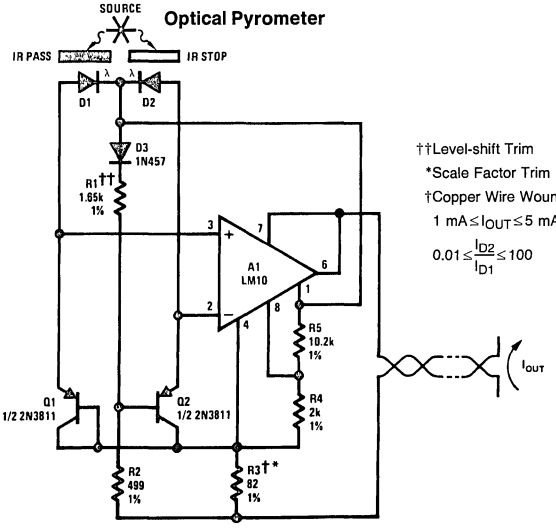


Precision Thermocouple Transmitter



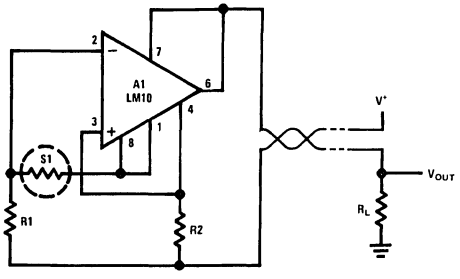
*Gain Trim

Optical Pyrometer



††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound
1 mA ≤ I_{OUT} ≤ 5 mA
$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

Resistance Thermometer Transmitter



††Circuit descriptions available in application note AN-211.

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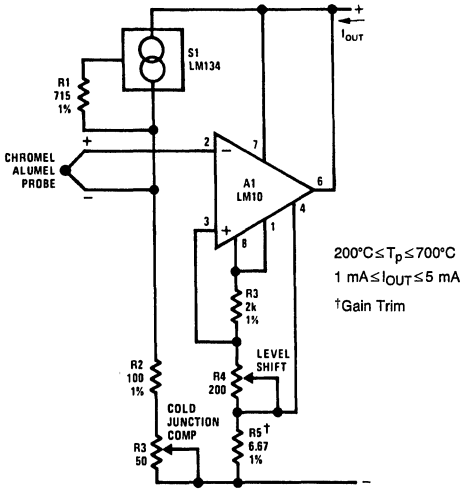
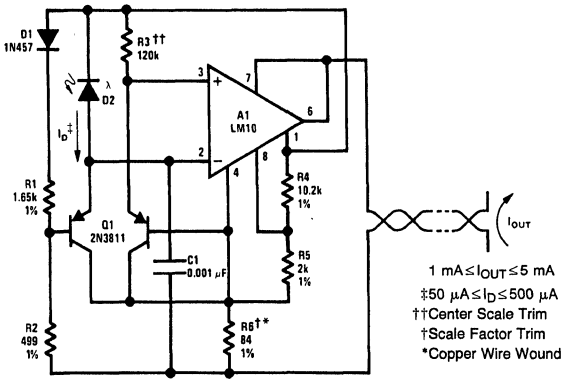
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Thermocouple Transmitter



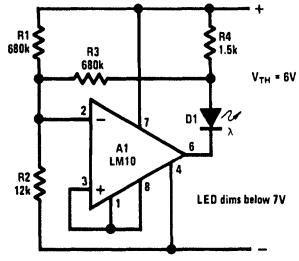
200°C≤T_p≤700°C
1 mA≤I_{OUT}≤5 mA
†Gain Trim

Logarithmic Light Sensor

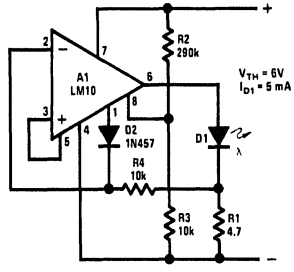


1 mA≤I_{OUT}≤5 mA
‡50 μA≤I_D≤500 μA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

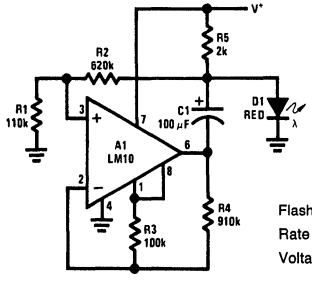
Battery-level Indicator



Battery-threshold Indicator

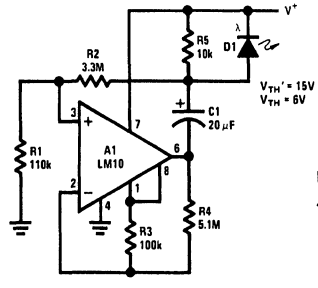


Single-cell Voltage Monitor



Flashes Above 1.2V
Rate Increases With
Voltage

Double-ended Voltage Monitor



Flash Rate Increases
Above 6V and Below 15V

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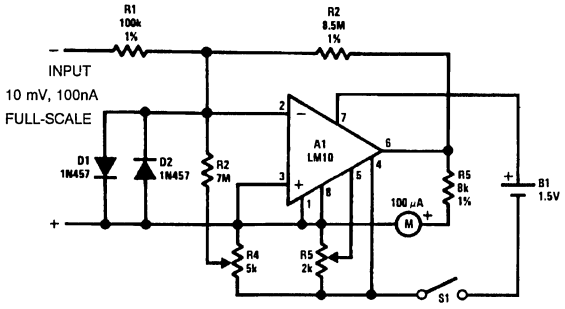
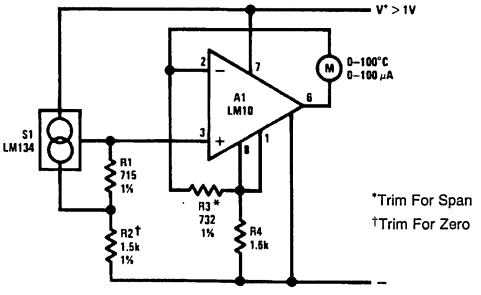
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

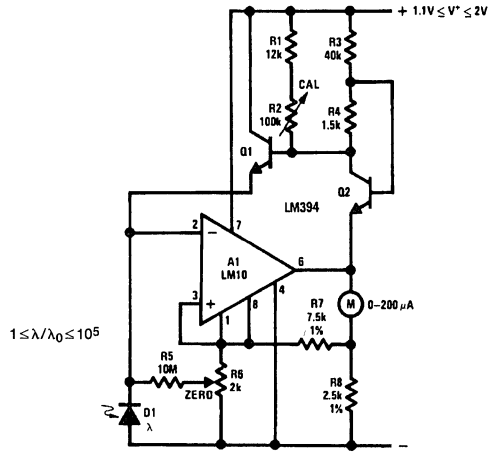
Meter Amplifier



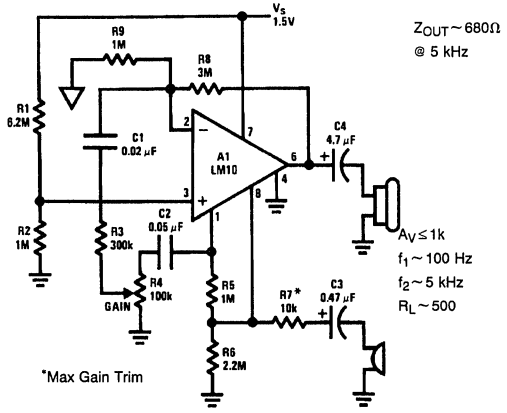
Thermometer



Light Meter



Microphone Amplifier

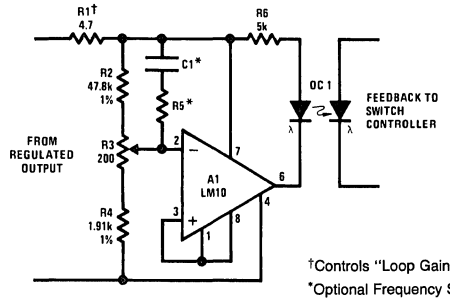


TL/H/5652–11

††Circuit descriptions available in application note AN-211.

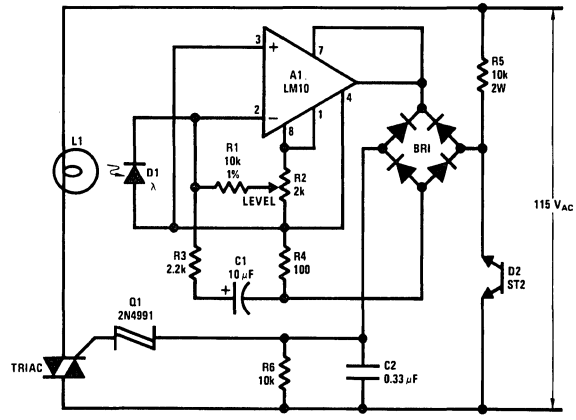
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Isolated Voltage Sensor



†Controls "Loop Gain"
*Optional Frequency Shaping

Light-level Controller



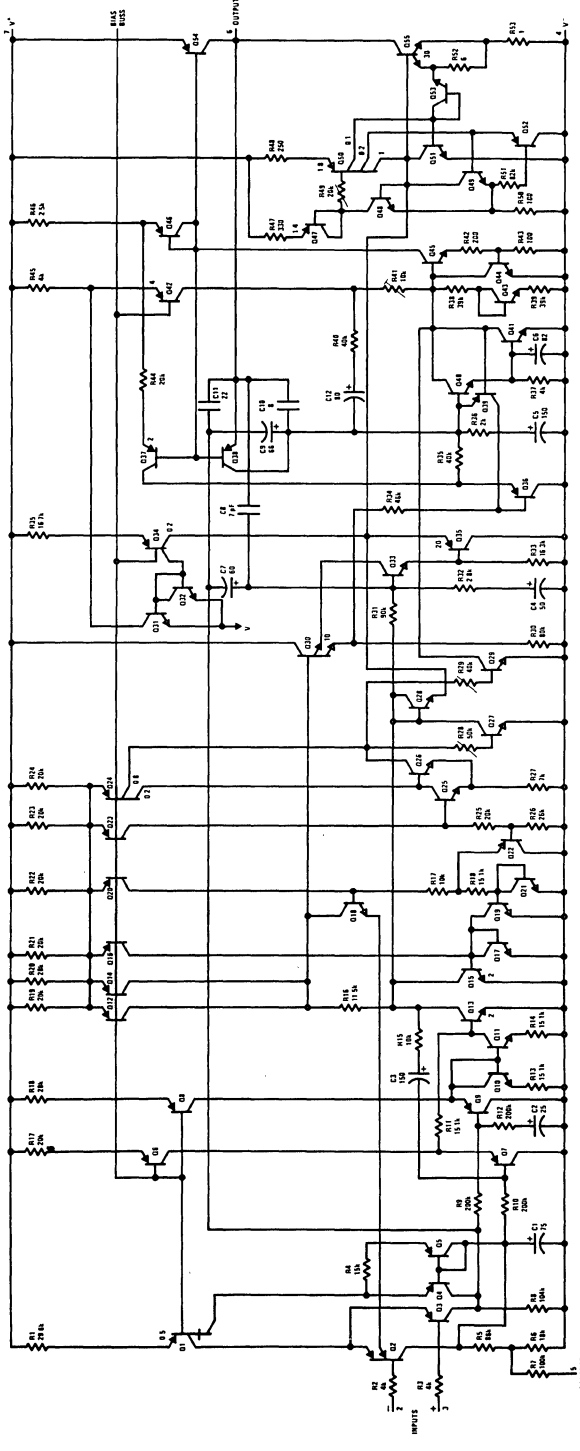
TL/H/5652–12

††Circuit descriptions available in application note AN-211.

Application Hints

With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic (Pin numbers are for 8-pin packages)



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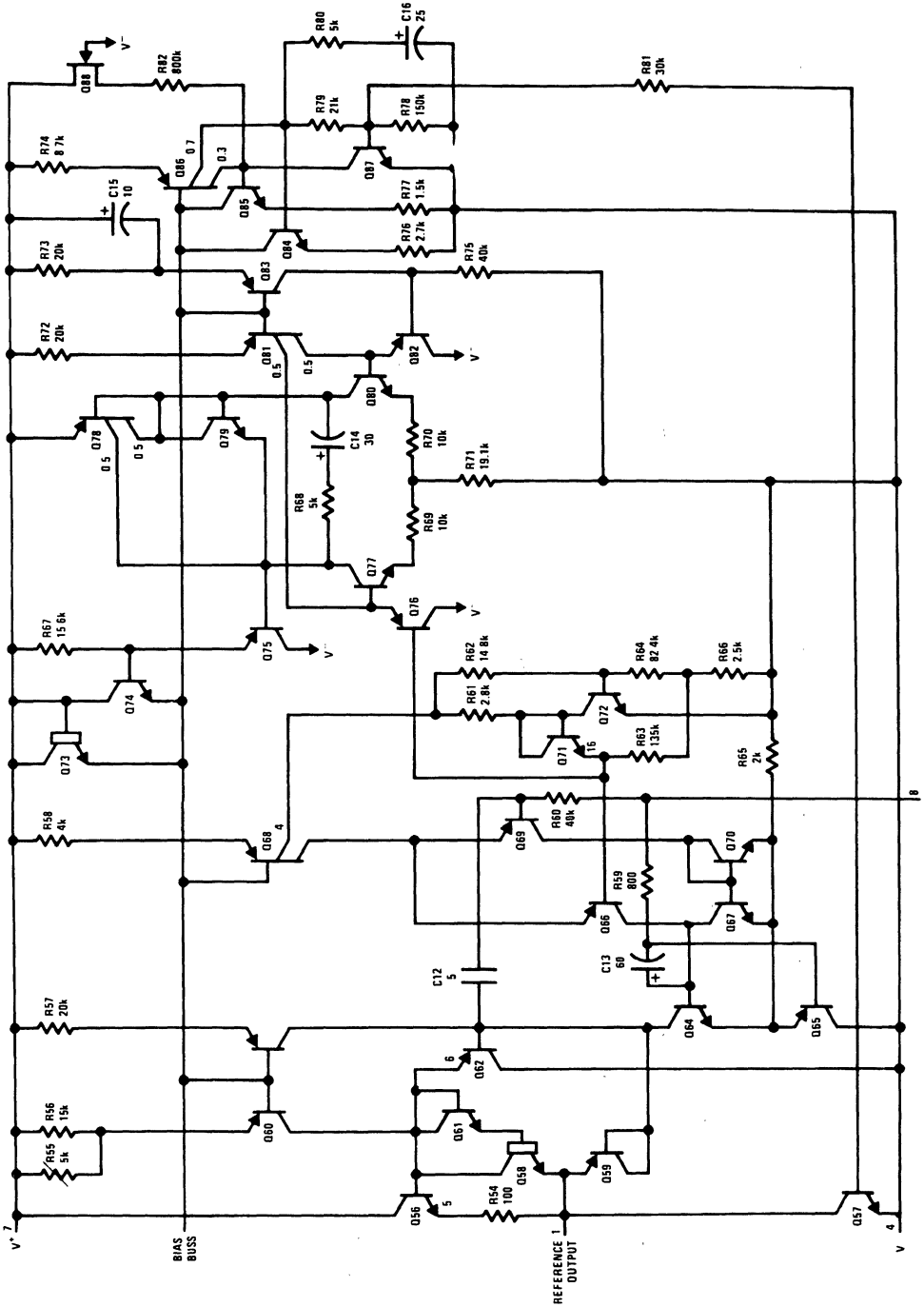
Reference and Internal Regulator (Pin numbers are for 8-pin packages)



National Semiconductor

LM11/LM11C/LM11CL Operational Amplifiers

General Description

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been approved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (**−55°C** to **125°C**) are:

- offset voltage: 100 μV **(200 μV)**
- bias current: 25 pA **(65 pA)**
- offset current: 0.5 pA **(3 pA)**
- temperature drift: **1 μV/°C**
- long-term stability: 10 μV/year

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

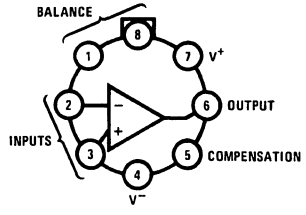
Otherwise, the device is the electrical equivalent of the LM108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obviously applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

Metal Can*



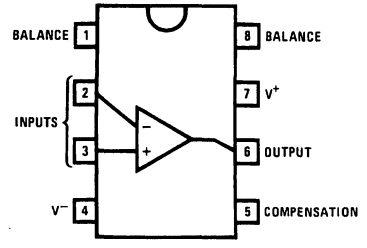
TL/H/5653–1

Top View

Order Number LM11H, LM11CH or LM11CLH
See NS Package H08C

*Case connected to V−

Mini-DIP



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Top View

Order Number LM11CN or LM11CLN
See NS Package N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Total Supply Voltage	40V
Input Current (Note 1)	±10 mA
Power Dissipation (Note 2)	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
(DIP)	260°C
(Metal Can)	300°C
ESD Tolerance	
(R_{ZAP} = 1.5k, C_{ZAP} = 100 pF)	1500V

Electrical Characteristics $T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (Note 4)

(Boldface type refers to limits over temperature range.)

Parameter	Conditions	LM11		LM11C		LM11CL		Units
		Typ	Lim	Typ	Lim	Typ	Lim	
Input Offset Voltage	(Note 4)	0.1	0.3 **0.6**	0.2	0.6 **0.8**	0.5	5 **6**	mV mV
Input Offset Current	(Note 4)	0.5	10 **30**	1	10 **20**	4	25 **50**	pA pA
Input Bias Current	(Note 4)	25	50 **150**	40	100 **150**	70	200 **300**	pA pA
Input Resistance	(Note 4)	10^{11}		10^{11}		10^{11}		Ω
Offset Voltage Drift	(Note 4)	1	**3**	2	**5**	3		µV/°C
Offset Current Drift	(Note 4)	20		10		50		fA/°C
Bias Current Drift	(Note 4)	0.5	**1.5**	0.8	**3**	1.4		pA/°C
Large Signal Voltage Gain	V_S ±15V, I_{OUT} = ±2 mA V_{OUT} = ±12V(±**11.5V**) V_S = ±15V, I_{OUT} = ±0.5 mA V_{OUT} ±12V	300 1200	100 **50** 250 **100**	300 1200	100 **50** 250 **100**	300 800	25 **15** 50 **30**	V/mV V/mV V/mV V/mV
Common-Mode Rejection	−13V (−**12.5V**) ≤ V_{CM} ≤ 14V V_S = ±15V	130	110 **100**	130	110 **100**	110	96 **90**	dB dB
Power Supply Rejection Ratio	±2.5V ≤ V_S ≤ ±20V	118	100 **96**	118	100 **96**	100	84 **80**	dB dB
Supply Current	(Note 4)	0.3	0.6 **0.8**	0.3	0.8 **1**	0.3	0.8 **1**	mA mA
Output Short-Circuit Current	T_J = 150°C		±15					mA

Note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

Note 2: The maximum operating-junction temperature is 150°C for the LM11 and 85°C for the LM11C(L). Devices must be derated at 150°C/W for the metal can and 155°C/W for the plastic DIP. The metal can has a thermal resistance of 45°C/W for the junction to case if a heat sink is used.

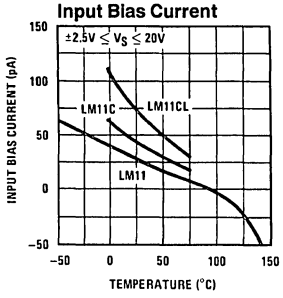
Note 3: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

Note 4: These specifications apply for V^- + 2V (**2.5V**) ≤ V_{CM} ≤ V^+ − 1V and ±2.5V ≤ V_S ≤ ±20V, unless otherwise specified. Normal typeface indicates 25°C limits. **Boldface type indicates limits for full-temperature range operation.** This is −55°C ≤ T_J ≤ 125°C for the LM11 and 0°C ≤ T_J ≤ 70°C for the LM11C(L).

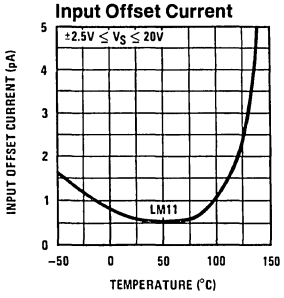
Note 5: Refer to RETS11X for LM11 military specifications.

Typical Characteristics

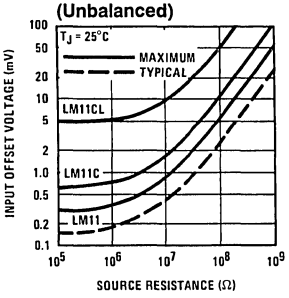
Input Bias Current



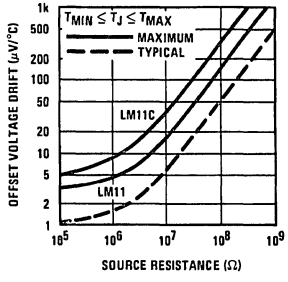
Input Offset Current



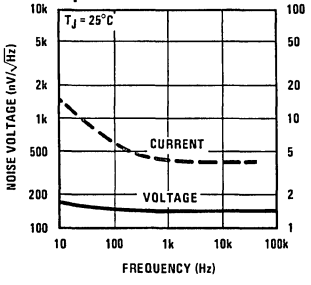
Offset: Single Source Resistor (Unbalanced)



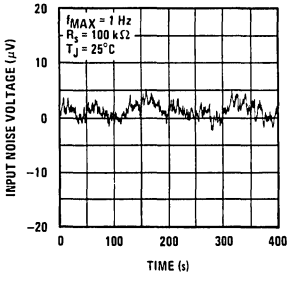
Drift: Single Source Resistor (Unbalanced)



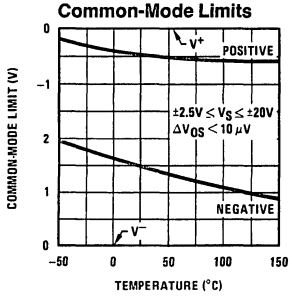
Input Noise



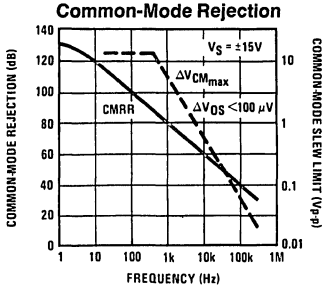
Input Noise



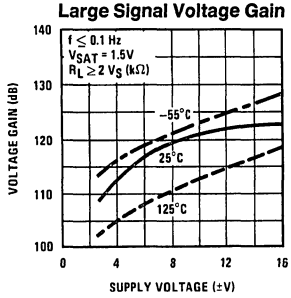
Common-Mode Limits



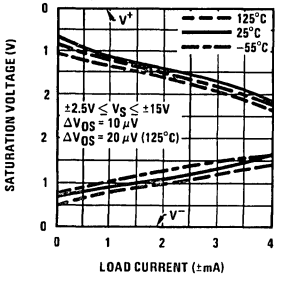
Common-Mode Rejection



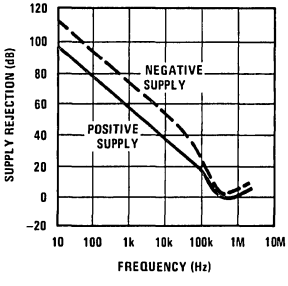
Large Signal Voltage Gain



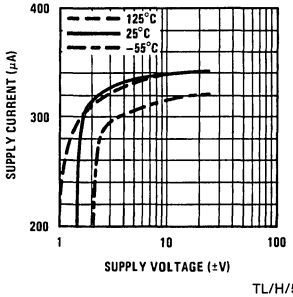
Output Saturation Threshold



Supply Rejection



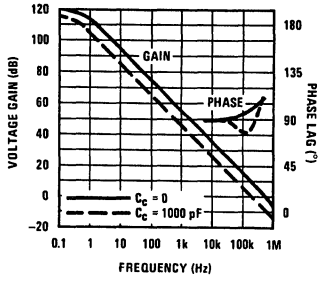
Supply Current



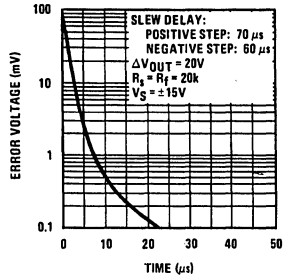
TL/H/5653–2

Typical Characteristics (Continued)

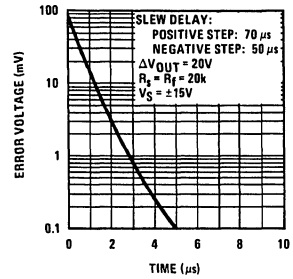
Open Loop Response



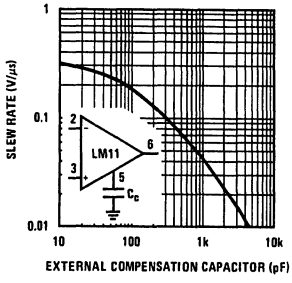
Follower Final Settling Time



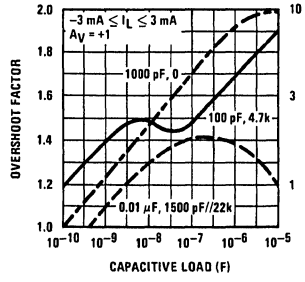
Inverter Final Settling Time



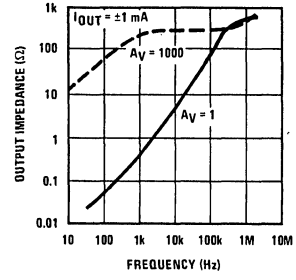
Slew Rate



Stability With Over-Compensation



Closed Loop Output Impedance



TL/H/5653–3

Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

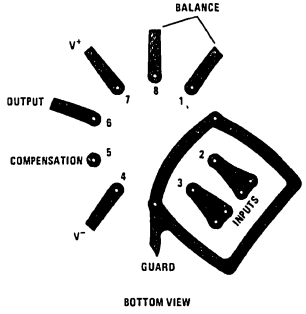
With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the noninverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 µF bypass on the supply buss.

Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

Application Hints (Continued)

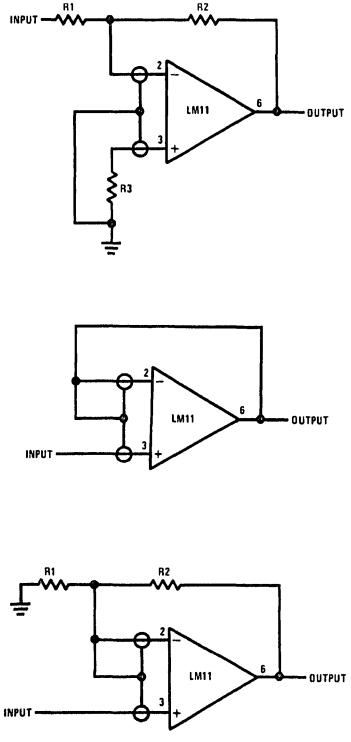
Input Guarding

Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



TL/H/5653–4

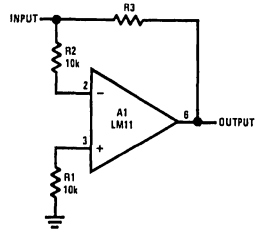
Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are here.



TL/H/5653–7

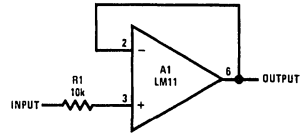
Input Protection

Current is limited by R2 even when input is connected to voltage source outside common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



TL/H/5653–5

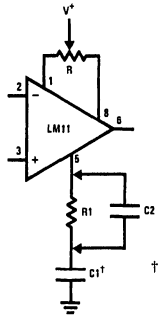
Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



TL/H/5653–6

Balancing And Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.



† See stability with over-compensation curve

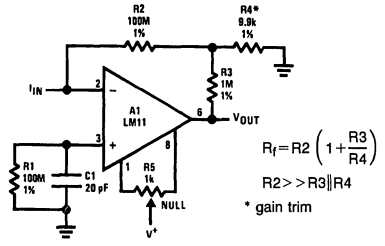
TL/H/5653–8

min. adj range	R
±4 mV	100 kΩ
±2	10k
±0.8	3k
±0.4	1k

Application Hints (Continued)

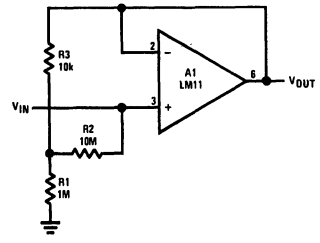
Resistance Multiplication

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.



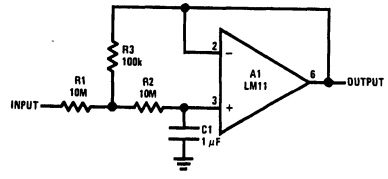
TL/H/5653–9

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.



TL/H/5653–11

This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.

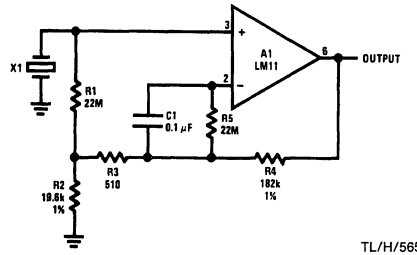


TL/H/5653–13

$$\tau = \frac{R1C}{R3}(R2+R3)$$

$$\Delta V_{OUT} = \frac{R1+R3}{R3}(I_B R2 + V_{OS})$$

A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.

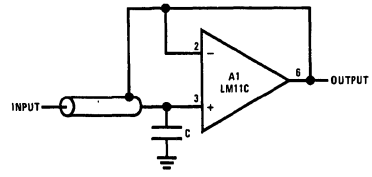


TL/H/5653–10

$$R_{IN} = R1\left(1+\frac{R2}{R3}\right) \quad A_V = \frac{R2+R3+R4}{R2+R3}$$

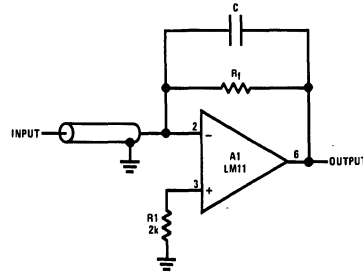
Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



TL/H/5653–12

With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.



TL/H/5653–14

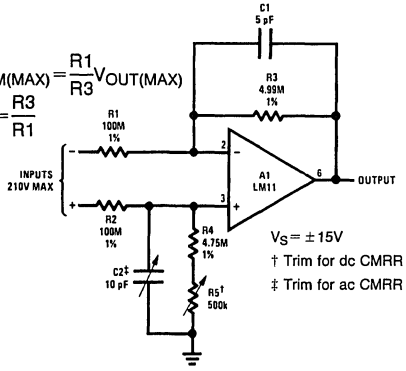
Application Hints (Continued)

Differential Amplifiers

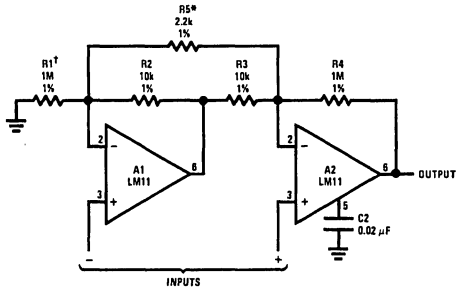
This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

$$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$$

$$A_V = \frac{R3}{R1}$$

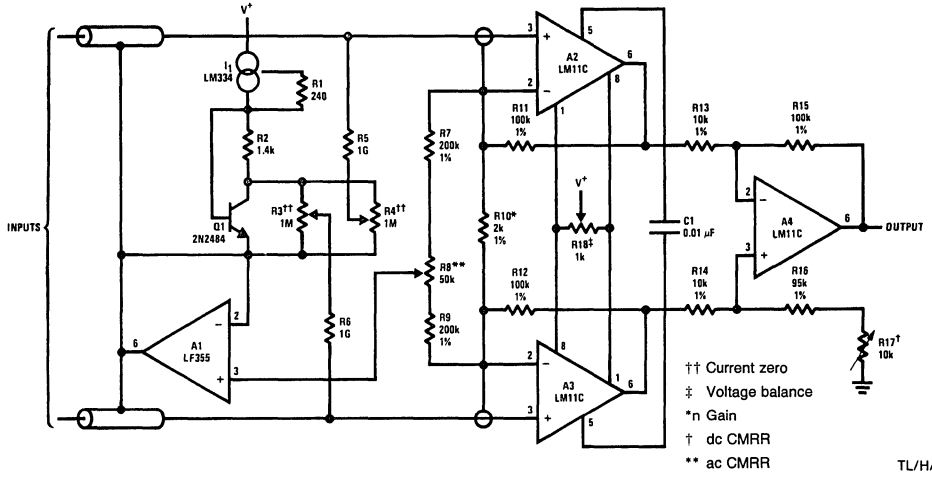


Two op-amp instrumentation amplifier has poor ac common mode rejection. This can be improved at the expense of differential bandwidth with C2.



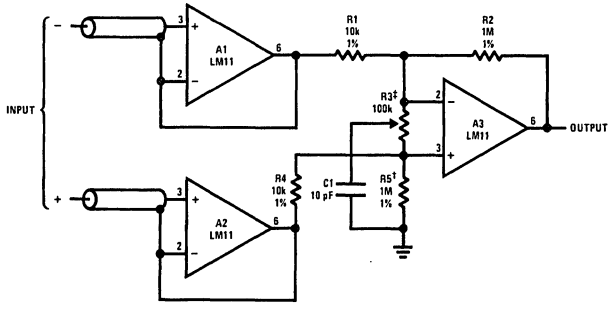
TL/H/5653–15

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



TL/H/5653–16

For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.



R1 = R3; R2 = R4

$$A_V = \frac{R2}{R1}$$

†Trim for dc CMRR

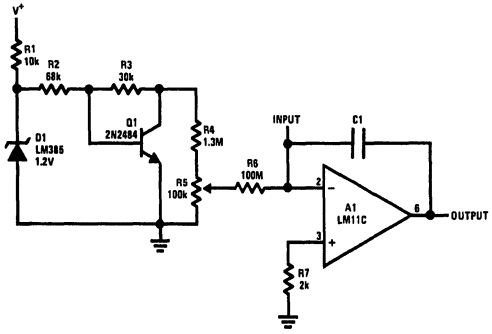
‡Set for ac CMRR

TL/H/5653–17

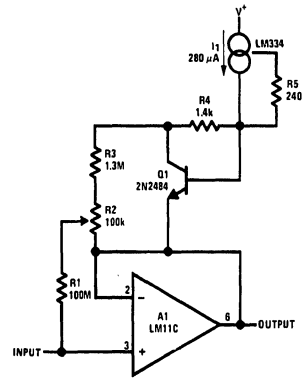
Application Hints (Continued)

Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.



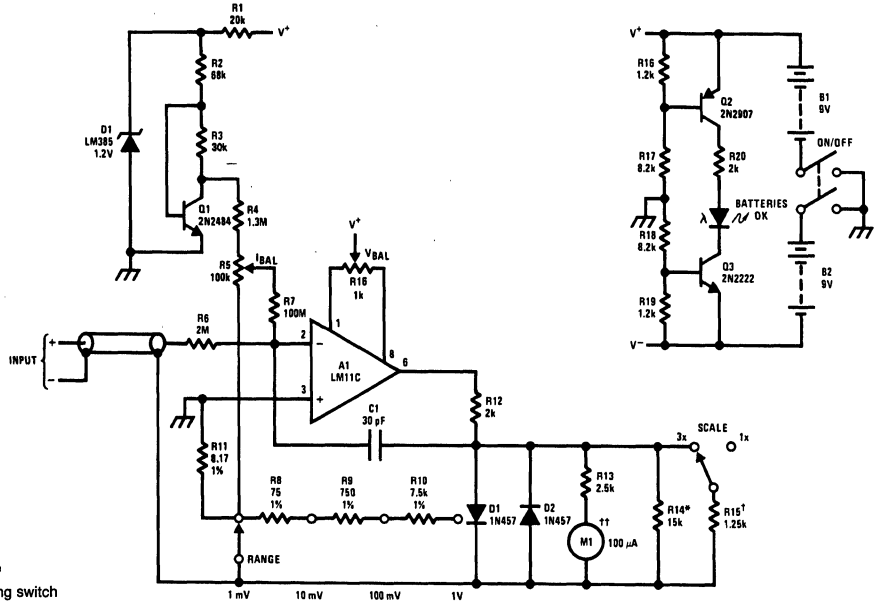
This circuit shows how bias current compensation can be used on a voltage follower.



TL/H/5653–18

Voltmeter

High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.



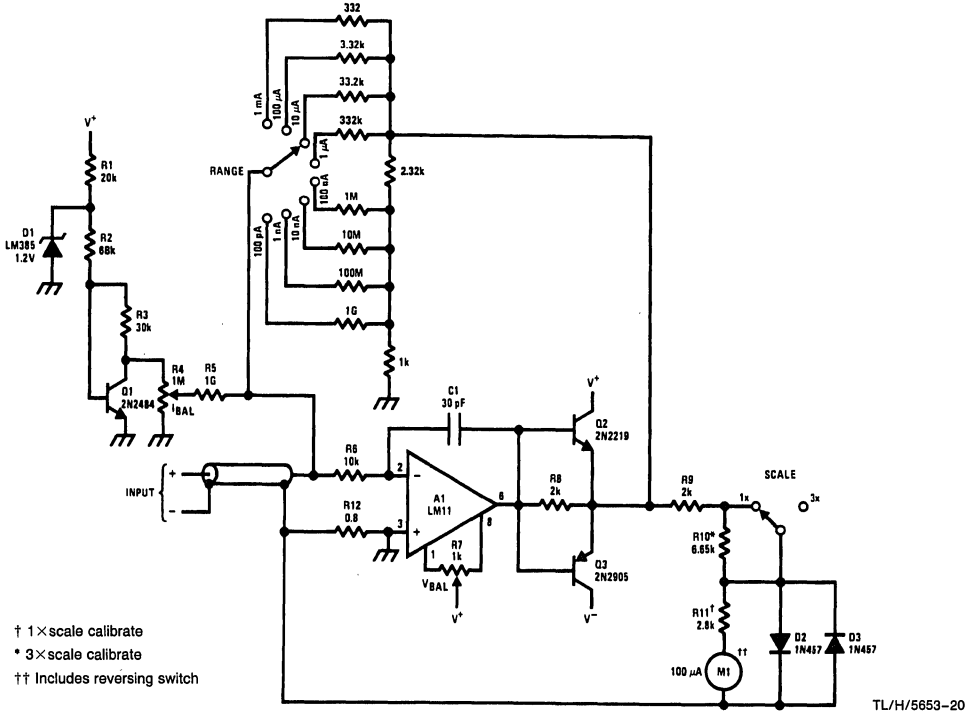
* 1×scale calibrate
† 3×scale calibrate
†† Includes reversing switch

TL/H/5653–19

Application Hints (Continued)

Ammeter

Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.

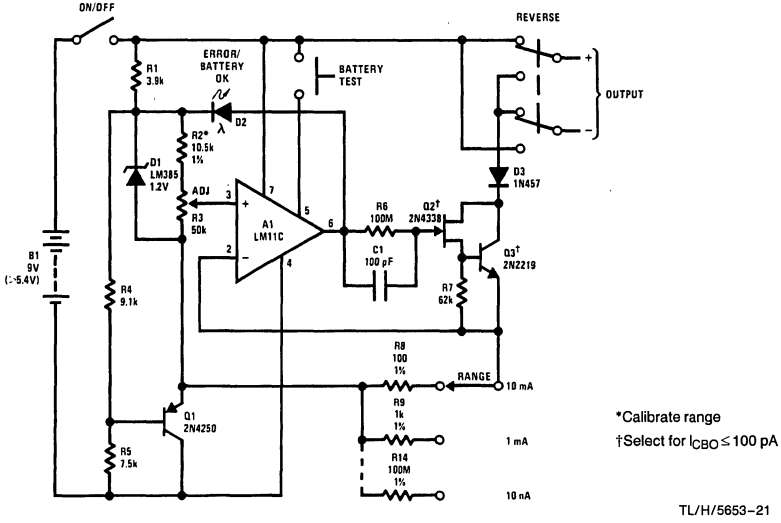


† 1×scale calibrate
* 3×scale calibrate
†† Includes reversing switch

TL/H/5653–20

Current Source

Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.



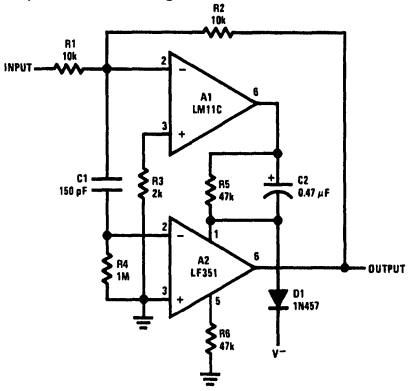
*Calibrate range
†Select for $I_{CBO} \leq 100$ pA

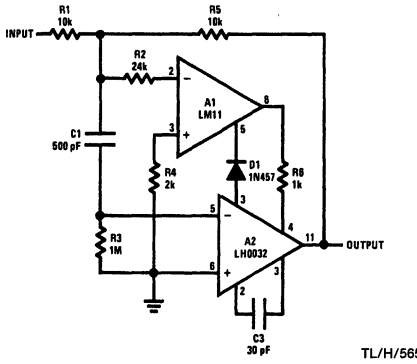
TL/H/5653–21

Application Hints (Continued)

Fast Amplifiers

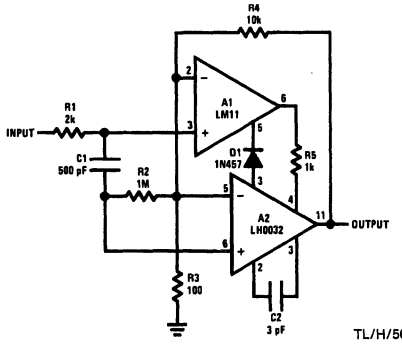
These inverters have bias current and offset voltage of LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μS. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.





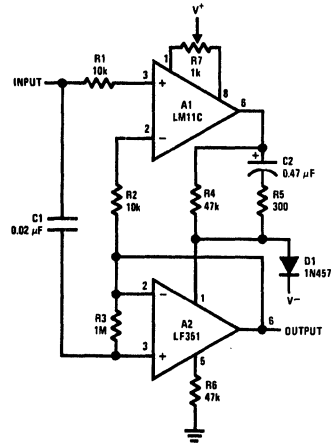
TL/H/5653–22

This 100× amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.



TL/H/5653–24

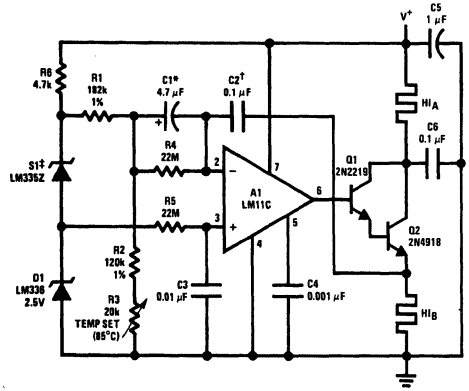
Follower has 10 μS setting to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



TL/H/5653–23

Heater Control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



TL/H/5653–25

* Solid tantalum

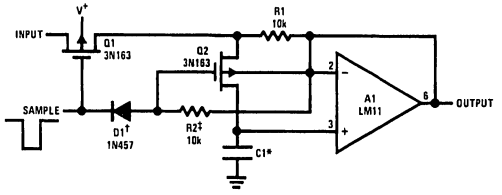
† Mylar

‡ Close thermal coupling between sensor and oven shell is recommended.

Application Hints (Continued)

Leakage Isolation

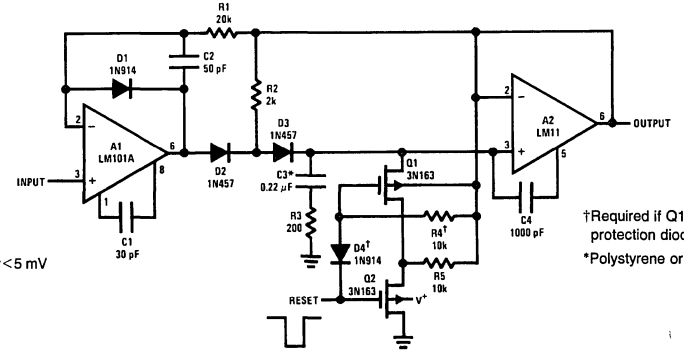
Switch leakage in this sample and hold does not reach storage capacitor.



*Polystyrene or Teflon
†Required if protected-gate switch is used

TL/H/5653–26

A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

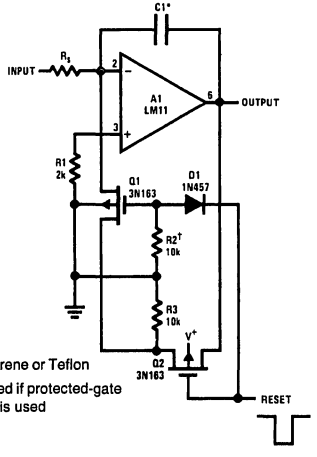


300 μS min single pulse
200 μS min repetitive pulse
300 Hz max sine wave error < 5 mV

†Required if Q1 has gate-protection diode
*Polystyrene or Teflon

TL/H/5653–27

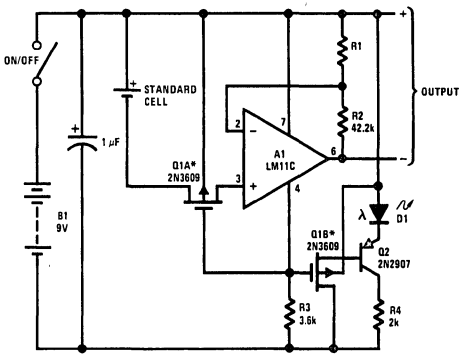
Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



*Polystyrene or Teflon
†Required if protected-gate switch is used

Standard-Cell Buffer

Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



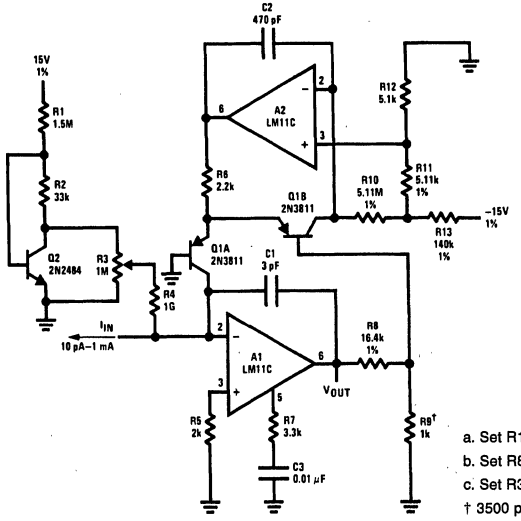
TL/H/5653–28

*Cannot have gate protection diode; $V_{TH} > V_{OUT}$

Application Hints (Continued)

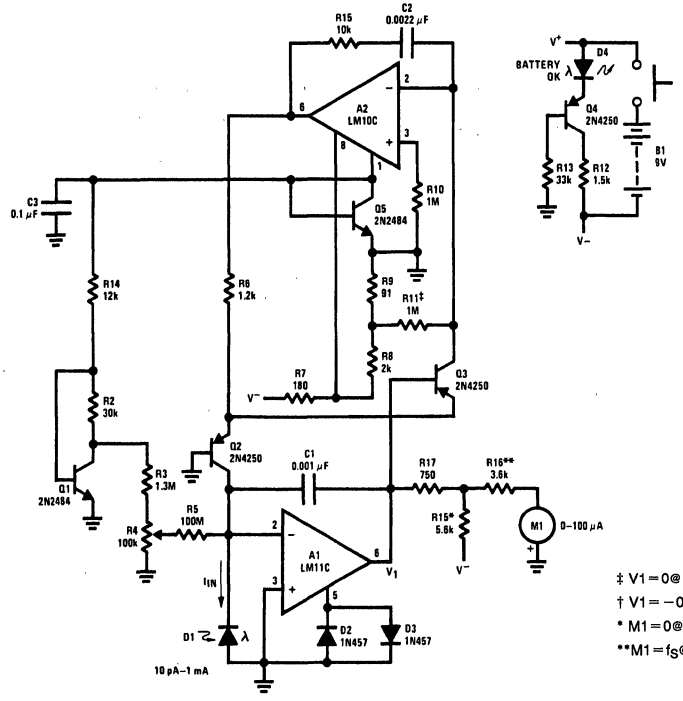
Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs, time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



a. Set R11 for $V_{OUT}=0$ at $I_{IN}=100$ nA
b. Set R8 for $V_{OUT}=3V$ at $I_{IN}=100$ μA
c. Set R3 for $V_{OUT}=-4V$ at $I_{IN}=10$ pA
† 3500 ppM/°C. Type Q81 available from Tel Labs Inc., Londonderry, N.H.

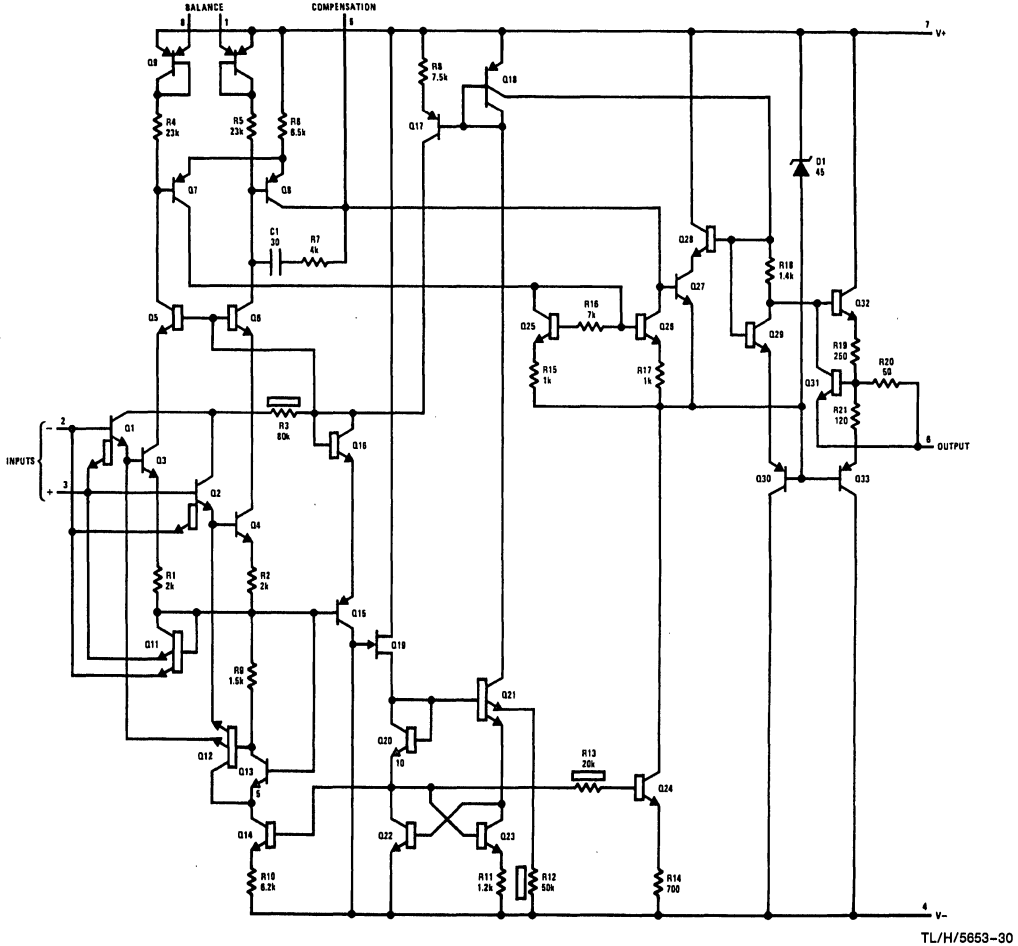
Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ V1 = 0@ $I_{IN}=100$ nA
† V1 = −0.24V@$I_{IN}=10$ pA
* M1 = 0@$I_{IN}=10$ pA
** M1 = f_S@$I_{IN}=1$ mA

TL/H/5653–29

Schematic Diagram



TL/H/5653–30

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Power Supply Rejection Ratio: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor

LM12 (L/C/CL) 150W Operational Amplifier

General Description

The LM12 is a power op amp capable of driving ±35V at ±10A while operating from ±40V supplies. The monolithic IC can deliver 150W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

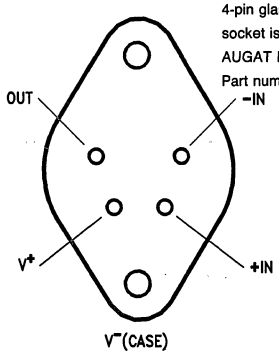
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150°C or as the supply voltage approaches the BV_{CEO} of the output transistors. The IC withstands overvoltages to 100V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/μs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with V^- on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. Two voltage grades are available; both are specified for either military or commercial temperature range.

Connection Diagram

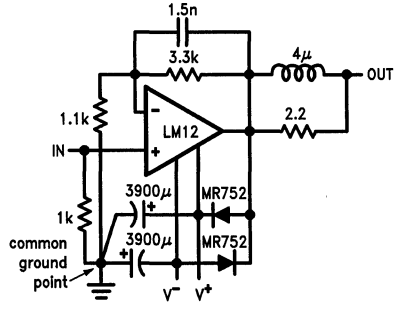


TL/H/8704-1

Bottom View

Order Number LM12K, LM12CK or LM12CLK
See NS Package Number K04A

Typical Application*



TL/H/8704-2

*Low distortion (0.01%) audio amplifier

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	LM12/LM12C	100V
	LM12L/LM12CL	80V
Input Voltage		Note 1
Output Current		Internally Limited
Junction Temperature		Note 2
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)		300°C

ESD Rating to be Determined.

Operating Ratings

Total Supply Voltage	LM12/LM12C	15V to 80V
	LM12L/LM12CL	15V to 60V

Electrical Characteristics (Note 3)

Parameter	Conditions	Typ 25°C	LM12 LM12L Limits	LM12C LM12CL Limits	Units
Input Offset Voltage	$\pm 10V \le V_S \le \pm 0.5\ V_{MAX}$, $V_{CM} = 0$	2	7/**15**	15/**20**	mV (max)
Input Bias Current	$V^- + 4V \le V_{CM} \le V^+ - 2V$	0.15	0.3/**1.0**	0.7/**1.0**	μA (max)
Input Offset Current	$V^- + 4V \le V_{CM} \le V^+ - 2V$	0.03	0.1/**0.3**	0.2/**0.3**	μA (max)
Common Mode Rejection	$V^- + 4V \le V_{CM} \le V^+ - 2V$	86	75/**70**	70/**65**	dB (min)
Power Supply Rejection	$V^+ = 0.5\ V_{MAX}$, $-6V \ge V^- \ge -0.5\ V_{MAX}$	90	75/**70**	70/**65**	dB (min)
	$V^- = -0.5\ V_{MAX}$, $6V \le V^+ \le 0.5\ V_{MAX}$	110	80/**75**	75/**70**	dB (min)
Output Saturation Threshold	t_{ON} = 1 ms, ΔV_{IN} = 5 (**10**) mV, I_{OUT} = 1A	1.8	2.2/**2.5**	2.2/**2.5**	V (max)
	8A	4	5/**7**	5/**7**	V (max)
	10A	5	8		V (max)
Large Signal Voltage Gain	t_{ON} = 2 ms, V_{SAT} = 2V, I_{OUT} = 0	100	50/**30**	30/**20**	V/mV (min)
	V_{SAT} = 8V, R_L = 4Ω	50	20/**15**	15/**10**	V/mV (min)
Thermal Gradient Feedback	P_{DISS} = 50W, t_{ON} = 65 ms	30	50	100	μV/W (max)
Output-Current Limit	t_{ON} = 10 ms, V_{DISS} = 10V	13	16	16	A (max)
	t_{ON} = 100 ms, V_{DISS} = 58V	1.5	1.0/**0.6**	0.9/**0.6**	A (min)
		1.5	1.7	1.7	A (max)
	LM12/LM12C t_{ON} = 100 ms, V_{DISS} = 78V	0.7	0.6/**0.4**	0.5/**0.35**	A (min)
Power Dissipation Rating	t_{ON} = 100 ms, V_{DISS} = 20V	100	90/**40**	80/**55**	W (min)
	V_{DISS} = 58V	80	58/**35**	52/**35**	W (min)
DC Thermal Resistance	(Note 4) V_{DISS} = 20V	2.3	2.6	2.9	°C/W (max)
	V_{DISS} = 58V	2.7	4.0	4.5	°C/W (max)
AC Thermal Resistance	(Note 4)	1.6	1.9	2.1	°C/W (max)
Supply Current	V_{OUT} = 0, I_{OUT} = 0	60	80/**90**	120/**140**	mA (max)

Note 1. Neither input should exceed the supply voltage by more than 50 volts nor should the voltage between one input and any other terminal exceed 80 volts for the LM12/LM12C or 60 volts for the LM12L/LM12CL.

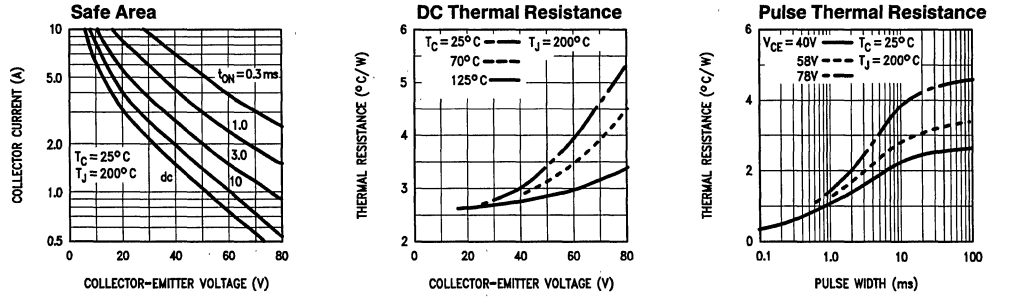
Note 2. Operating junction temperature is internally limited near 225°C within the power transistor and 160°C for the control circuitry.

Note 3. The supply voltage is ±40V (V_{MAX} = 80V) for the LM12/LM12C and ±30V (V_{MAX} = 60V) for the LM12L/LM12CL, unless otherwise specified. The voltage across the conducting output transistor (supply to output) is V_{DISS} and internal power dissipation is P_{DISS}. Temperature range is $-55°C \le T_C \le 125°C$ for the LM12/LM12L and $0°C \le T_C \le 70°C$ for LM12C/LM12CL, where T_C is the case temperature. Standard typeface indicates limits at 25°C **while boldface type refers to limits or special conditions over full temperature range.** With no heat sink, the package will heat at a rate of 35°C/sec per 100W of internal dissipation.

Note 4. This thermal resistance is based upon a peak temperature of 200°C in the center of the power transistor and a case temperature of 25°C measured at the center of the package bottom. The maximum junction temperature of the control circuitry can be estimated based upon a dc thermal resistance of 0.9°C/W or an ac thermal resistance of 0.6°C/W for any operating voltage.

Although the output and supply leads are resistant to electrostatic discharges from handling, the input leads are not. The part should be treated accordingly.

Output-Transistor Ratings (guaranteed)†



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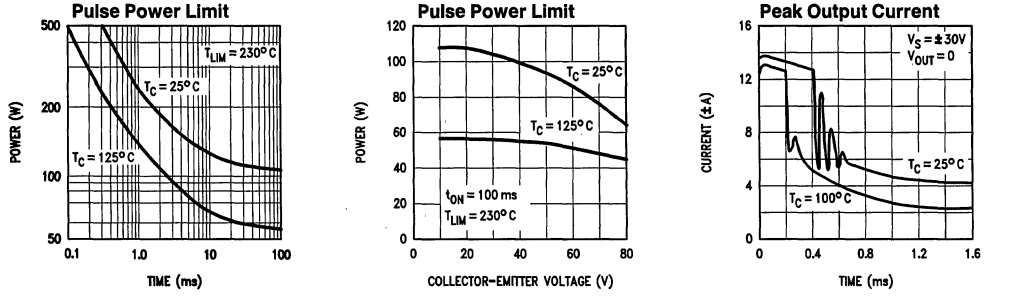
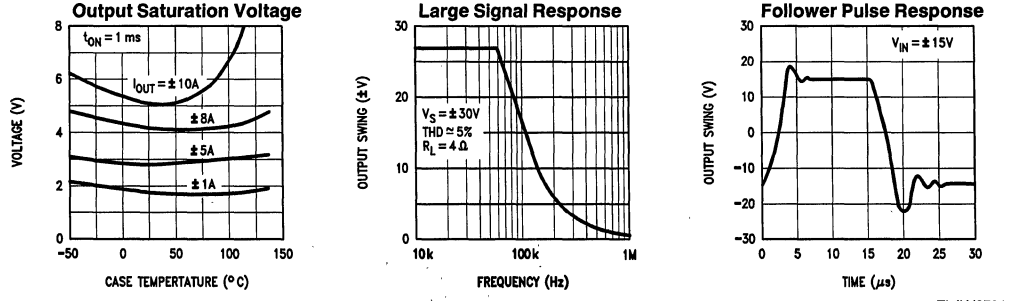
†LM12/LM12L. The power ratings of the LM12C/LM12CL are 10-percent less at 20V and 15-percent less at 60V, with a corresponding increase in thermal resistance and decrease in safe area current.

Typical Performance Characteristics





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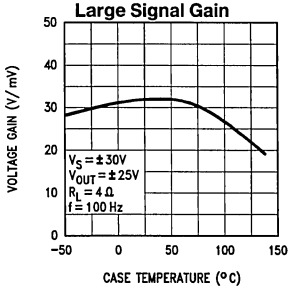
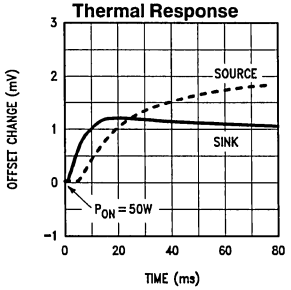
Typical Performance Characteristics (Continued)

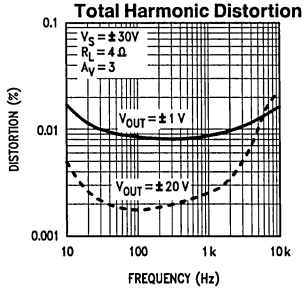
Large Signal Gain



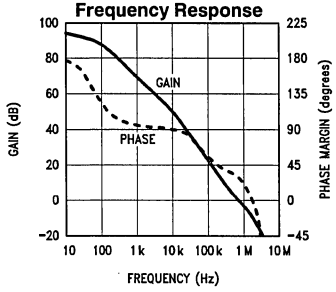
Thermal Response



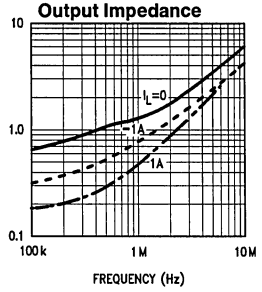
Total Harmonic Distortion



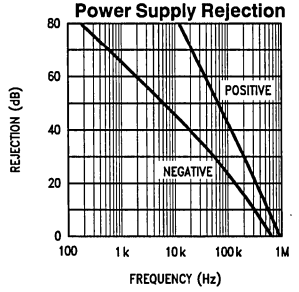
Frequency Response



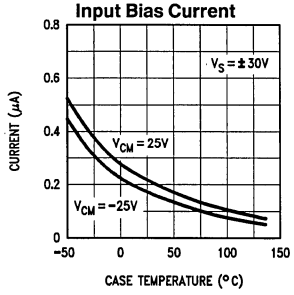
Output Impedance



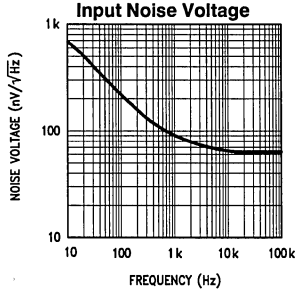
Power Supply Rejection



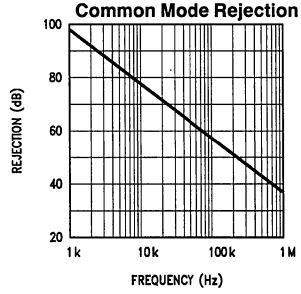
Input Bias Current



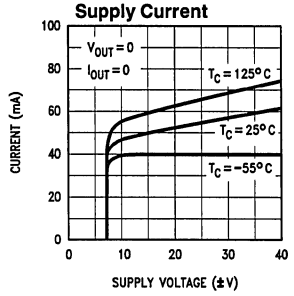
Input Noise Voltage



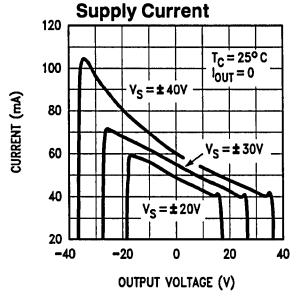
Common Mode Rejection



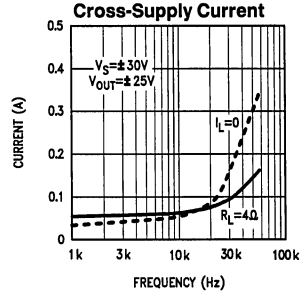
Supply Current



Supply Current



Cross-Supply Current



TL/H/8704–5

Application Information

GENERAL

Twenty five years ago the operational amplifier was a specialized design tool used primarily for analog computation. However, the availability of low cost IC op amps in the late 1960's prompted their use in rather mundane applications, replacing a few discrete components. Once a few basic principles are mastered, op amps can be used to give exceptionally good results in a wide range of applications while minimizing both cost and design effort.

The availability of a monolithic power op amp now promises to extend these advantages to high-power designs. Some conventional applications are given here to illustrate op amp design principles as they relate to power circuitry. The inevitable fall in prices, as the economies of volume production are realized, will prompt their use in applications that might now seem trivial. Replacing single power transistors with an op amp will become economical because of improved performance, simplification of attendant circuitry, vastly improved fault protection, greater reliability and the reduction of design time.

Power op amps introduce new factors into the design equation. With current transients above 10A, both the inductance and resistance of wire interconnects become important in a number of ways. Further, power ratings are a crucial factor in determining performance. But the power capability of the IC cannot be realized unless it is properly mounted to an adequate heat sink. Thus, thermal design is of major importance with power op amps.

This application summary starts off by identifying the origin of strange problems observed while using the LM12 in a wide variety of designs with all sorts of fault conditions. A few simple precautions will eliminate these problems. **One would do well to read the section on supply bypassing, lead inductance, output clamp diodes, ground loops and reactive loading before doing any experimentation. Should there be problems with erratic operation, blow-outs, excessive distortion or oscillation, another look at these sections is in order.**

The management and protection circuitry can also affect operation. Should the total supply voltage exceed ratings or drop below 15–20V, the op amp shuts off completely. Case temperatures above 150°C also cause shut down until the temperature drops to 145°C. This may take several seconds, depending on the thermal system. Activation of the dynamic safe-area protection causes both the main feedback loop to lose control and a reduction in output power, with possible oscillations. In ac applications, the dynamic protection will cause waveform distortion. Since the LM12 is well protected against thermal overloads, the suggestions for determining power dissipation and heat sink requirements are presented last.

SUPPLY BYPASSING

All op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals to avoid spurious oscillation problems. Power op amps require larger bypass capacitors. The LM12 is stable with good-quality electrolytic bypass capacitors greater than 20 μF. Other considerations may require larger capacitors.

The current in the supply leads is a rectified component of the load current. If adequate bypassing is not provided, this distorted signal can be fed back into internal circuitry. Low distortion at high frequencies requires that the supplies be bypassed with 470 μF or more, at the package terminals.

LEAD INDUCTANCE

With ordinary op amps, lead-inductance problems are usually restricted to supply bypassing. Power op amps are also sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load. Sensing to a remote load must be accompanied by a high-frequency feedback path directly from the output terminal. Lead inductance can also cause voltage surges on the supplies. With long leads to the power source, energy stored in the lead inductance when the output is shorted can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet ($>$ 1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

GROUND LOOPS

With fast, high-current circuitry, all sorts of problems can arise from improper grounding. In general, difficulties can be avoided by returning all grounds separately to a common point. Sometimes this is impractical. When compromising, special attention should be paid to the ground returns for the supply bypasses, load and input signal. Ground planes also help to provide proper grounding.

Many problems unrelated to system performance can be traced to the grounding of line-operated test equipment used for system checkout. Hidden paths are particularly difficult to sort out when several pieces of test equipment are used but can be minimized by using current probes or the new isolated oscilloscope pre-amplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope synchronization input solves one common problem.

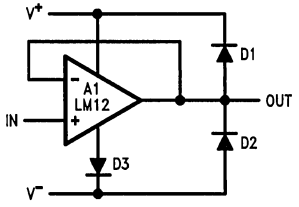
OUTPUT CLAMP DIODES

When a push-pull amplifier goes into power limit while driving an inductive load, the stored energy in the load inductance can drive the output outside the supplies. Although the LM12 has internal clamp diodes that can handle several amperes for a few milliseconds, extreme conditions can cause destruction of the IC. The internal clamp diodes are imperfect in that about half the clamp current flows into the supply to which the output is clamped while the other half flows across the supplies. Therefore, the use of external diodes to clamp the output to the power supplies is strongly recommended. This is particularly important with higher supply voltages.

Experience has demonstrated that hard-wire shorting the output to the supplies can induce random failures if these external clamp diodes are not used and the supply voltages are above $\pm$20V. Therefore it is prudent to use output-

Application Information (Continued)

clamp diodes even when the load is not particularly inductive. This also applies to experimental setups in that blowouts have been observed when diodes were not used. In packaged equipment, it may be possible to eliminate these diodes, providing that fault conditions can be controlled.



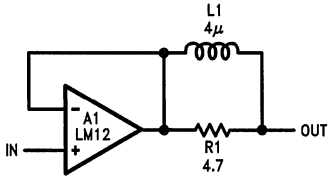
TL/H/8704–6

Heat sinking of the clamp diodes is usually unimportant in that they only clamp current transients. Forward drop with 15A fault transients is of greater concern. Usually, these transients die out rapidly. The clamp to the negative supply can have somewhat reduced effectiveness under worst case conditions should the forward drop exceed 1.0V. Mounting this diode to the power op amp heat sink improves the situation. Although the need has only been demonstrated with some motor loads, including a third diode (D3 above) will eliminate any concern about the clamp diodes. This diode, however, must be capable of dissipating continuous power as determined by the negative supply current of the op amp.

REACTIVE LOADING

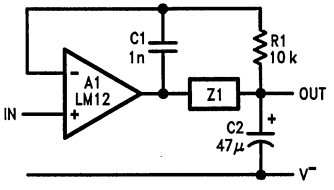
The LM12 is normally stable with resistive, inductive or smaller capacitive loads. Larger capacitive loads interact with the open-loop output resistance (about 1Ω) to reduce the phase margin of the feedback loop, ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier; a unity-gain follower can handle about 0.01 μF, while more than 1 μF does not cause problems if the loop gain is ten. With loop gains greater than unity, a speedup capacitor across the feedback resistor will aid stability. In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled and high-frequency feedback is derived directly from the output terminal, as recommended earlier.

So-called capacitive loads are not always capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this is not usually a problem; but the situation should be kept in mind.



TL/H/8704–7

Large capacitive loads (including series-resonant) can be accommodated by isolating the feedback amplifier from the load as shown above. The inductor gives low output impedance at lower frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series resonant circuits formed by capacitive loads. A low inductance, carbon-composition resistor is recommended. Optimum values of L and R depend upon the feedback gain and expected nature of the load, but are not critical. A 4 μH inductor is obtained with 14 turns of number 18 wire, close spaced, around a one-inch-diameter form.



TL/H/8704–8

The LM12 can be made stable for all loads with a large capacitor on the output, as shown above. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. It is appropriate for such applications as voltage regulators.

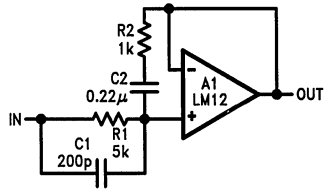
A feedback capacitor, C_1, is connected directly to the output pin of the IC. The output capacitor, C_2, is connected at the output terminal with short leads. Single-point grounding to avoid dc and ac ground loops is advised.

The impedance, Z_1, is the wire connecting the op amp output to the load capacitor. About 3-inches of number-18 wire (70 nH) gives good stability and 18-inches (400 nH) begins to degrade load-transient response. The minimum load capacitance is 47 μF, if a solid-tantalum capacitor with an equivalent series resistance (ESR) of 0.1Ω is used. Electrolytic capacitors work as well, although capacitance may have to be increased to 200 μF to bring ESR below 0.1Ω.

Loop stability is not the only concern when op amps are operated with reactive loads. With time-varying signals, power dissipation can also increase markedly. This is particularly true with the combination of capacitive loads and high-frequency excitation.

INPUT COMPENSATION

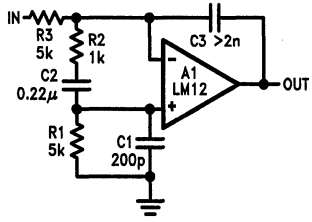
The LM12 is prone to low-amplitude oscillation bursts coming out of saturation if the high-frequency loop gain is near unity. The voltage follower connection is most susceptible. This glitching can be eliminated at the expense of small-signal bandwidth using input compensation. Input compensation can also be used in combination with LR load isolation to improve capacitive load stability.



TL/H/8704–9

An example of a voltage follower with input compensation is shown here. The R_2C_2 combination across the input works with R_1 to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, C_1, improves phase margin at the unity-gain crossover frequency. Proper operation requires that the output impedance of the circuitry driving the follower be well under 1 kΩ at frequencies up to a few hundred kilohertz.

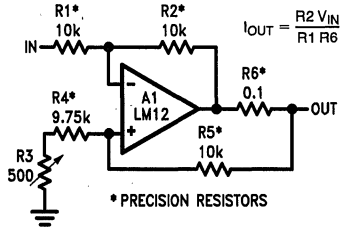
Application Information (Continued)



TL/H/8704–10

Extending input compensation to the integrator connection is shown here. Both the follower and this integrator will handle 1 μF capacitive loading without LR output isolation.

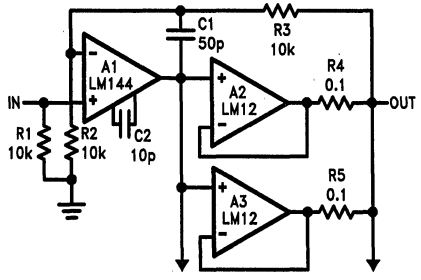
CURRENT DRIVE



TL/H/8704–11

This circuit provides an output current proportional to the input voltage. Current drive is sometimes preferred for servo motors because it aids in stabilizing the servo loop by reducing phase lag caused by motor inductance. In applications requiring high output resistance, such as operational power supplies running in the current mode, matching of the feedback resistors to 0.01% is required. Alternately, an adjustable resistor can be used for trimming.

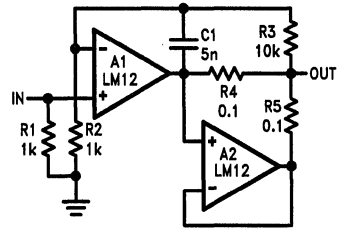
PARALLEL OPERATION



TL/H/8704–12

Output drive beyond the capability of one power amplifier can be provided as shown here. The power op amps are wired as followers and connected in parallel with the outputs coupled through equalization resistors. A standard, high-voltage op amp is used to provide voltage gain. Overall feedback compensates for the voltage dropped across the equalization resistors.

With parallel operation, there may be an increase in unloaded supply current related to the offset voltage across the equalization resistors. More output buffers, with individual equalization resistors, may be added to meet even higher drive requirements.

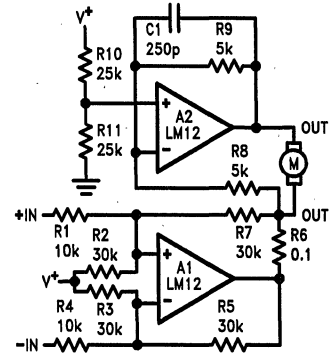


TL/H/8704–13

This connection allows increased output capability without requiring a separate control amplifier. The output buffer, A_2, provides load current through R_5 equal to that supplied by the main amplifier, A_1, through R_4. Again, more output buffers can be added.

Current sharing among paralleled amplifiers can be affected by gain error as the power-bandwidth limit is approached. In the first circuit, the operating current increase will depend upon the matching of high-frequency characteristics. In the second circuit, however, the entire input error of A_2 appears across R_4 and R_5. The supply current increase can cause power limiting to be activated as the slew limit is approached. This will not damage the LM12. It can be avoided in both cases by connecting A_1 as an inverting amplifier and restricting bandwidth with C_1.

SINGLE-SUPPLY OPERATION



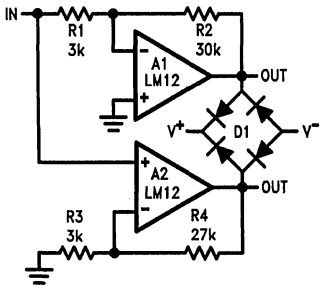
TL/H/8704–14

Although op amps are usually operated from dual supplies, single-supply operation is practical. This bridge amplifier supplies bi-directional current drive to a servo motor while operating from a single positive supply. The output is easily converted to voltage drive by shorting R_6 and connecting R_7 to the output of A_2, rather than A_1.

Either input may be grounded, with bi-directional drive provided to the other. It is also possible to connect one input to a positive reference, with the input signal varying about this voltage. If the reference voltage is above 5V, R_2 and R_3 are not required.

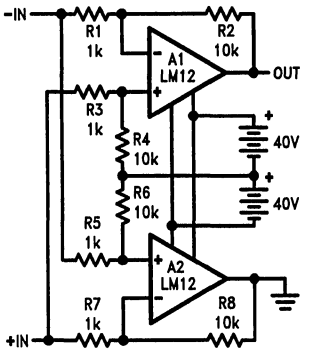
Application Information (Continued)

HIGH VOLTAGE AMPLIFIERS



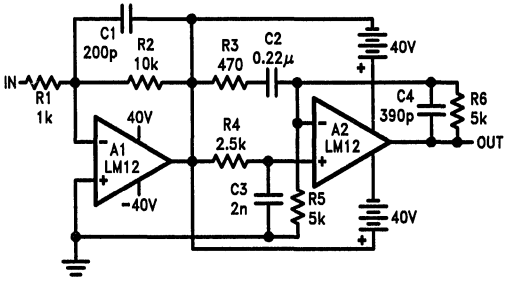
TL/H/8704–15

The voltage swing delivered to the load can be doubled by using the bridge connection shown here. Output clamping to the supplies can be provided by using a bridge-rectifier assembly.



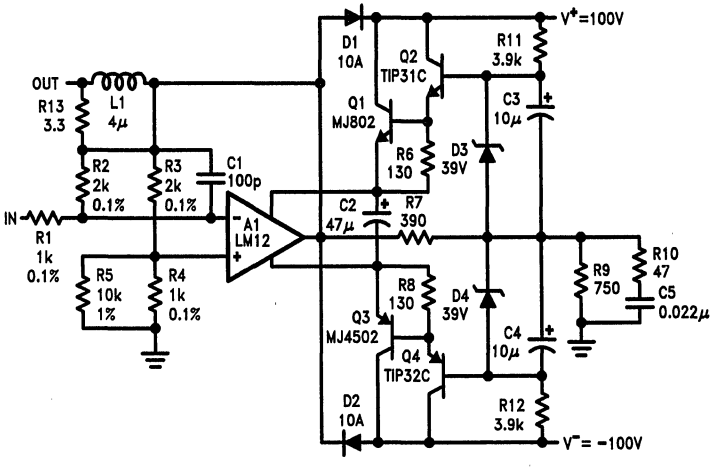
TL/H/8704–16

One limitation of the standard bridge connection is that the load cannot be returned to ground. This can be circumvented by operating the bridge with floating supplies, as shown above. For single-ended drive, either input can be grounded.



TL/H/8704–17

This circuit shows how two amplifiers can be cascaded to double output swing. The advantage over the bridge is that the output can be increased with any number of stages, although separate supplies are required for each.

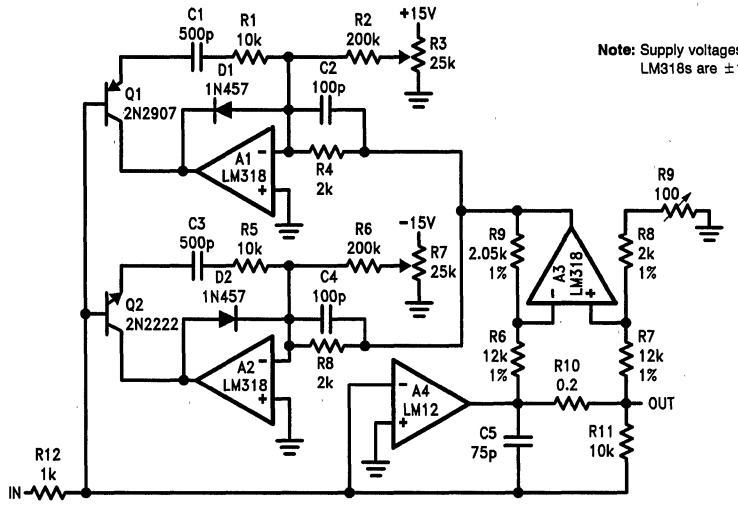


TL/H/8704–18

Discrete transistors can be used to increase output drive to ±90V at ±10A as shown above. With proper thermal design, the IC will provide safe-area protection for the external transistors. Voltage gain is about thirty.

Application Information (Continued)

OPERATIONAL POWER SUPPLY



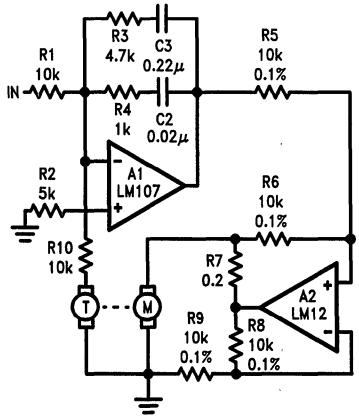
Note: Supply voltages for the LM318s are ±15V

TL/H/8704–19

External current limit can be provided for a power op amp as shown above. The positive and negative current limits can be set precisely and independently. Fast response is assured by D_1 and D_2. Adjustment range can be set down to zero with potentiometers R_3 and R_7. Alternately, the limit can be programmed from a voltage supplied to R_2 and R_6. This is the set up required for an operational power supply or voltage-programmable power source.

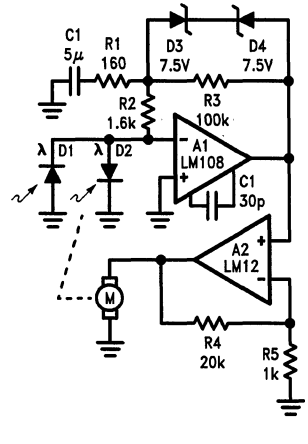
SERVO AMPLIFIERS

When making servo systems with a power op amp, there is a temptation to use it for frequency shaping to stabilize the servo loop. Sometimes this works; other times there are better ways; and occasionally it just doesn't fly. Usually it's a matter of how quickly and to what accuracy the servo must stabilize.



TL/H/8704–20

This motor/tachometer servo gives an output speed proportional to input voltage. A low-level op amp is used for frequency shaping while the power op amp provides current drive to the motor. Current drive eliminates loop phase shift due to motor inductance and makes high-performance servos easier to stabilize.

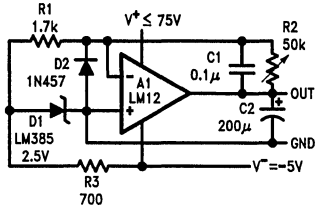


TL/H/8704–21

This position servo uses an op amp to develop the rate signal electrically instead of using a tachometer. In high-performance servos, rate signals must be developed with large error signals well beyond saturation of the motor drive. Using a separate op amp with a feedback clamp allows the rate signal to be developed properly with position errors more than an order of magnitude beyond the loop-saturation level as long as the photodiode sensors are positioned with this in mind.

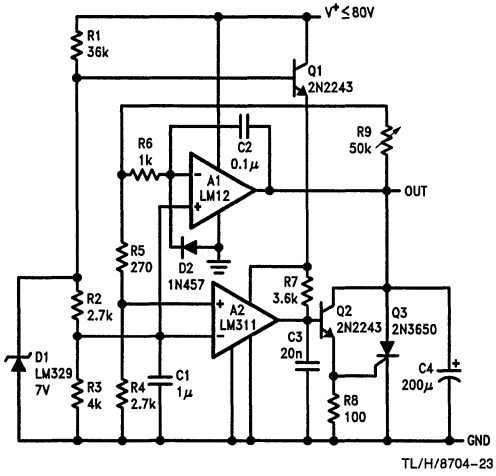
Application Information (Continued)

VOLTAGE REGULATORS



TL/H/8704–22

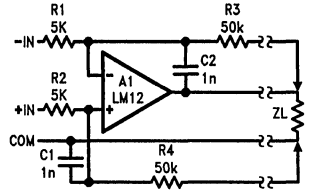
An op amp can be used as a positive or negative regulator. Unlike most regulators, it can sink current to absorb energy dumped back into the output. This positive regulator has a 0–70V output range.



TL/H/8704–23

Dual supplies are not required to use an op amp as a voltage regulator if zero output is not required. This 4V to 70V regulator operates from a single supply. Should the op amp not be able to absorb enough energy to control an overvoltage condition, a SCR will crowbar the output.

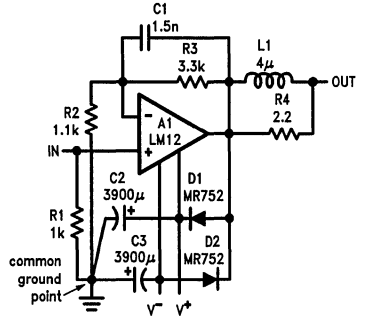
REMOTE SENSING



TL/H/8704–24

Remote sensing as shown above allows the op amp to correct for dc drops in cables connecting the load. Even so, cable drop will affect transient response. Degradation can be minimized by using twisted, heavy-gauge wires on the output line. Normally, common and one input are connected together at the sending end.

AUDIO AMPLIFIERS



TL/H/8704–25

A power amplifier suitable for use in high-quality audio equipment is shown above. Harmonic distortion is about 0.01-percent. Intermodulation distortion (60 Hz/7 kHz, 4:1) measured 0.015-percent. Transient response and saturation recovery are clean, and the 9 V/μs slew rate of the LM12 virtually eliminates transient intermodulation distortion. Using separate amplifiers to drive low- and high-frequency speakers gets rid of high-level crossover networks and attenuators. Further, it prevents clipping on the low-frequency channel from distorting the high frequencies.

Application Information (Continued)

DETERMINING MAXIMUM DISSIPATION

It is a simple matter to establish power requirements for an op amp driving a resistive load at frequencies well below 10 Hz. Maximum dissipation occurs when the output is at one-half the supply voltage with high-line conditions. The individual output transistors must be rated to handle this power continuously at the maximum expected case temperature. The power rating is limited by the maximum junction temperature as determined by

$$T_J = T_C + P_{DISS}\,\theta_{JC},$$

where T_C is the case temperature as measured at the center of the package bottom, P_{DISS} is the maximum power dissipation and θ_{JC} is the thermal resistance at the operating voltage of the output transistor. Recommended maximum junction temperatures are 200°C within the power transistor and 150°C for the control circuitry.

If there is ripple on the supply bus, it is valid to use the average value in worst-case calculations as long as the peak rating of the power transistor is not exceeded at the ripple peak. With 120 Hz ripple, this is 1.5 times the continuous power rating.

Dissipation requirements are not so easily established with time varying output signals, especially with reactive loads. Both peak and continuous dissipation ratings must be taken into account, and these depend on the signal waveform as well as load characteristics.

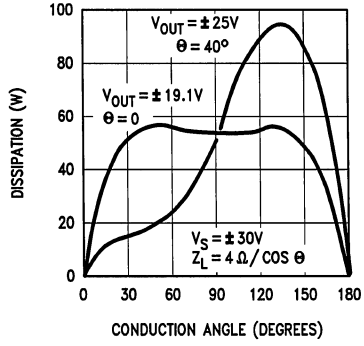
With a sine wave output, analysis is fairly straightforward. With supply voltages of $\pm V_S$, the maximum average power dissipation of both output transistors is

$$P_{MAX} = \frac{2V_S^2}{\pi^2 Z_L \cos\theta}, \quad \theta < 40°;$$

and

$$P_{MAX} = \frac{V_S^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right], \quad \theta \geq 40°,$$

where Z_L is the magnitude of the load impedance and θ its phase angle. Maximum average dissipation occurs below maximum output swing for $\theta < 40°$.



TL/H/8704–26

The instantaneous power dissipation over the conducting half cycle of one output transistor is shown here. Power dissipation is near zero on the other half cycle. The output level is that resulting in maximum peak and average dissipation. Plots are given for a resistive and a series RL load. The latter is representative of a 4Ω loudspeaker operating below resonance and would be the worst case condition in most audio applications. The peak dissipation of each transistor is about four times average. In ac applications, power capability is often limited by the peak ratings of the power transistor.

The pulse thermal resistance of the LM12 is specified for constant power pulse duration. Establishing an exact equivalency between constant-power pulses and those encountered in practice is not easy. However, for sine waves, reasonable estimates can be made at any frequency by assuming a constant power pulse amplitude given by:

$$P_{PK} \cong \frac{V_S^2}{2Z_L}\left[1\text{-}\cos(\phi - \theta)\right],$$

where $\phi = 60°$ and θ is the absolute value of the phase angle of Z_L. Equivalent pulse width is $t_{ON} \cong 0.4\tau$ for $\theta = 0$ and $t_{ON} \cong 0.2\tau$ for $\theta \geq 20°$, where τ is the period of the output waveform.

DISSIPATION DRIVING MOTORS

A motor with a locked rotor looks like an inductance in series with a resistance, for purposes of determining driver dissipation. With slow-response servos, the maximum signal amplitude at frequencies where motor inductance is significant can be so small that motor inductance does not have to be taken into account. If this is the case, the motor can be treated as a simple, resistive load as long as the rotor speed is low enough that the back emf is small by comparison to the supply voltage of the driver transistor.

A permanent-magnet motor can build up a back emf that is equal to the output swing of the op amp driving it. Reversing this motor from full speed requires the output drive transistor to operate, initially, along a loadline based upon the motor resistance and total supply voltage. Worst case, this loadline will have to be within the continuous dissipation rating of the drive transistor; but system dynamics may permit taking advantage of the higher pulse ratings. Motor inductance can cause added stress if system response is fast.

Shunt- and series-wound motors can generate back emf's that are considerably more than the total supply voltage, resulting in even higher peak dissipation than a permanent-magnet motor having the same locked-rotor resistance.

VOLTAGE REGULATOR DISSIPATION

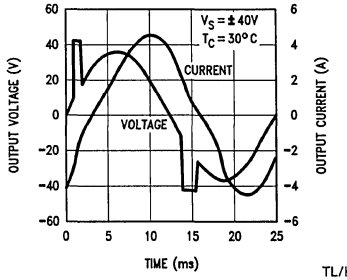
The pass transistor dissipation of a voltage regulator is easily determined in the operating mode. Maximum continuous dissipation occurs with high line voltage and maximum load current. As discussed earlier, ripple voltage can be averaged if peak ratings are not exceeded; however, a higher average voltage will be required to insure that the pass transistor does not saturate at the ripple minimum.

Conditions during start-up can be more complex. If the input voltage increases slowly such that the regulator does not go into current limit charging output capacitance, there are no problems. If not, load capacitance and load characteristics must be taken into account. This is also the case if automatic restart is required in recovering from overloads.

Automatic restart or start-up with fast-rising input voltages cannot be guaranteed unless the continuous dissipation rating of the pass transistor is adequate to supply the load current continuously at all voltages below the regulated output voltage. In this regard, the LM12 performs much better than IC regulators using foldback current limit, especially with high-line input voltage above 20V.

Application Information (Continued)

POWER LIMITING



TL/H/8704–27

Should the power ratings of the LM12 be exceeded, dynamic safe-area protection is activated. Waveforms with this power limiting are shown for the LM12 driving ±36V at 40 Hz into 4Ω in series with 24 mH (θ = 45°). With an inductive load, the output clamps to the supplies in power limit, as above. With resistive loads, the output voltage drops in limit. Behavior with more complex RCL loads is between these extremes.

Secondary thermal limit is activated should the case temperature exceed 150°C. This thermal limit shuts down the IC completely (open output) until the case temperature drops to about 145°C. Recovery may take several seconds.

POWER SUPPLIES

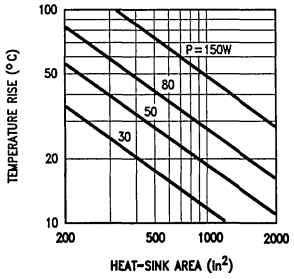
Power op amps do not require regulated supplies. However, the worst-case output power is determined by the low-line supply voltage in the ripple trough. The worst-case power dissipation is established by the average supply voltage with high-line conditions. The loss in power output that can be guaranteed is the square of the ratio of these two voltages.

Relatively simple off-line switching power supplies can provide voltage conversion, line isolation and 5-percent regulation while reducing size and weight.

The regulation against ripple and line variations can provide a substantial increase in the power output that can be guaranteed under worst-case conditions. In addition, switching power supplies can convert low-voltage power sources such as automotive batteries up to regulated, dual, high-voltage supplies optimized for powering power op amps.

HEAT SINKING

A semiconductor manufacturer has no control over heat sink design. Temperature rating can only be based upon case temperature as measured at the center of the package bottom. With power pulses of longer duration than 100 ms, case temperature is almost entirely dependent on heat sink design and the mounting of the IC to the heat sink.



TL/H/8704–28

The design of heat sink is beyond the scope of this work. Convection-cooled heat sinks are available commercially, and their manufacturers should be consulted for ratings. The preceding figure is a rough guide for temperature rise as a function of fin area (both sides) available for convection cooling.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important. Four to six inch-pounds is recommended.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like berylium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound. Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Definition of Terms

Input offset voltage: The absolute value of the voltage between the input terminals with the output voltage and current at zero.

Input bias current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input offset current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Output saturation threshold: The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Large signal voltage gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Thermal gradient feedback: The input offset voltage change caused by thermal gradients generated by heating of the output transistors, but not the package. This effect is delayed by several milliseconds and results in increased gain error below 100 Hz.

Output-current limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once the protection circuitry is activated.

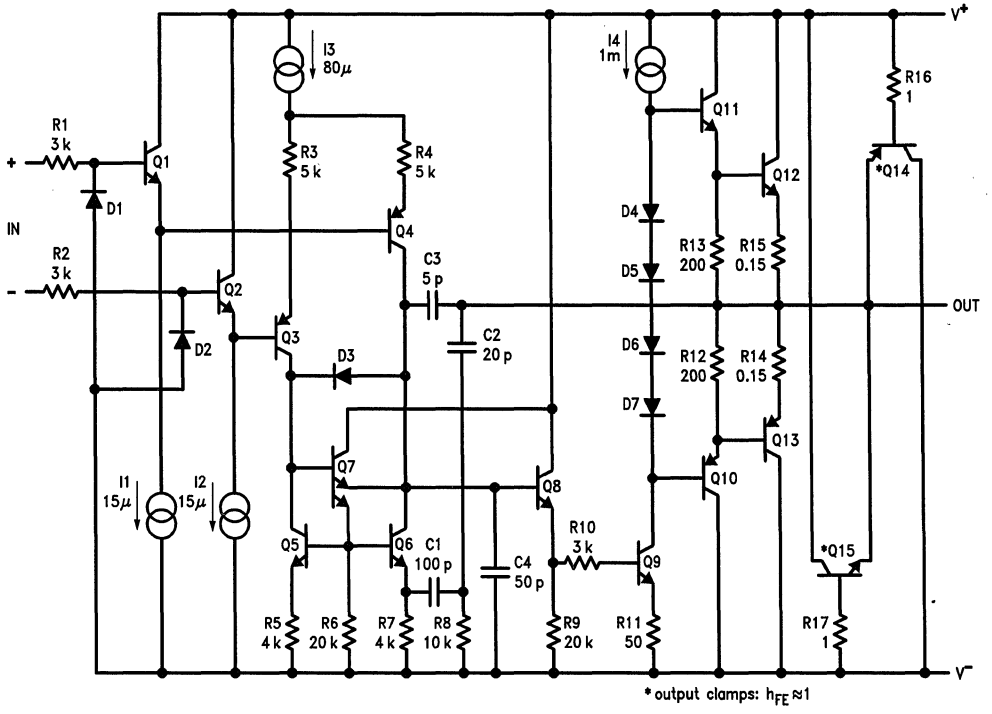
Power dissipation rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal resistance: The peak, junction-temperature rise, per unit of internal power dissipation, above the case temperature as measured at the center of the package bottom.

The dc thermal resistance applies when one output transistor is operating continuously. The ac thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Supply current: The current required from the power source to operate the amplifier with the output voltage and current at zero.

Equivalent Schematic (excluding active protection circuitry)



TL/H/8704–29

National Semiconductor

LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

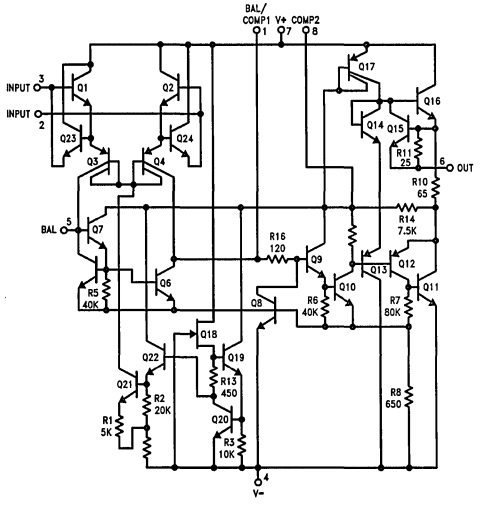
- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

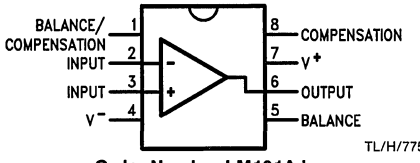
The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.

Schematic** and Connection Diagrams (Top View)



TL/H/7752-1

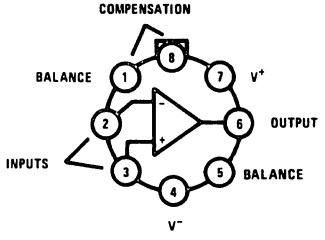
Dual-In-Line Package



TL/H/7752-4

Order Number LM101AJ, LM301AJ, LM201AN or LM301AN
See NS Package Number J08A or N08A

Metal Can Package

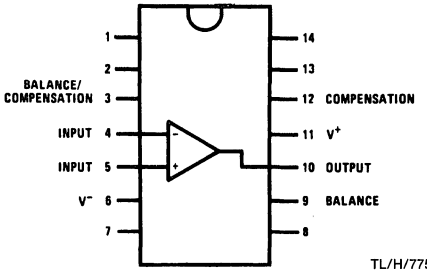


TL/H/7752-2

Note: Pin 4 connected to case.

Order Number LM101AH, LM201AH or LM301AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/7752-3

Order Number LM101AJ-14
See NS Package Number J14A

**Pin connections shown are for 8-pin packages.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM101A/LM201A	LM301A
Supply Voltage	±22V	±18V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Operating Ambient Temp. Range	−55°C to +125°C (LM101A) −25°C to +85°C (LM201A)	0°C to +70°C
T_J Max		
H-Package	150°C	100°C
N-Package	150°C	100°C
J-Package	150°C	100°C
M-Package		
Power Dissipation at T_A = 25°C		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	700 mW
N-Package	900 mW	500 mW
J-Package	1000 mW	650 mW
M-Package		
Thermal Resistance (Typical) θ_{jA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	67°C/W	67°C/W
N Package	135°C/W	135°C/W
J-Package	110°C/W	110°CmW
M-Package		
(Typical) θ_{jC}		
H-Package	25°C/W	25°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		
Metal Can or Ceramic	300°C	300°C
Plastic	260°C	260°C
ESD Tolerance (Note 5)	2000V	2000V

Electrical Characteristics (Note 3) $T_A = T_J$

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \leq 50\ k\Omega$			0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A = 25°C			1.5	10		3.0	50	nA
Input Bias Current	T_A = 25°C			30	75		70	250	nA
Input Resistance	T_A = 25°C		1.5	4.0		0.5	2.0		MΩ
Supply Current	T_A = 25°C	V_S = ±20V		1.8	3.0				mA
		V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \geq 2\ k\Omega$		50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0	15		6.0	30	µV/°C
Input Offset Current					20			70	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{MAX}$			0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \leq T_A \leq$ 25°C			0.02	0.2		0.02	0.6	nA/°C

Electrical Characteristics (Note 3) $T_A = T_J$ (Continued)

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Bias Current					0.1			0.3	μA
Supply Current	$T_A = T_{MAX}$, $V_S = \pm 20V$			1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k$		25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$		±15						V
	$V_S = \pm 15V$			±15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	96		dB

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

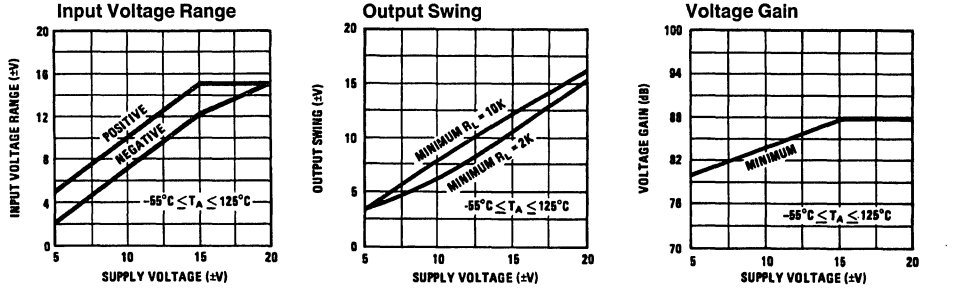
Note 2: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

Note 3: Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

Note 4: Refer to RETS101AX for LM101A military specifications.

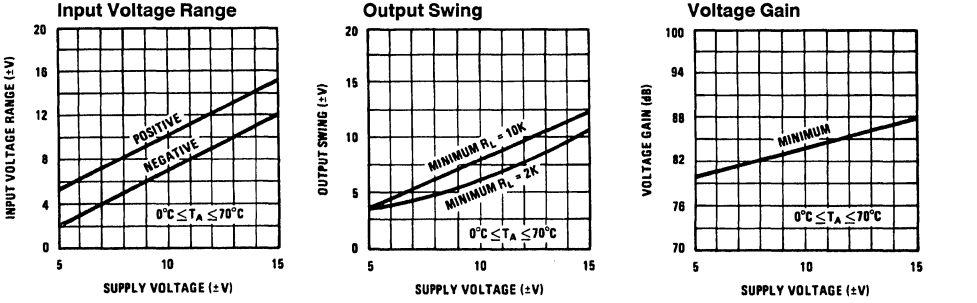
Note 5: Human body model, 100 pF discharged through 1.5 kΩ.

Guaranteed Performance Characteristics LM101A/LM201A



TL/H/7752–5

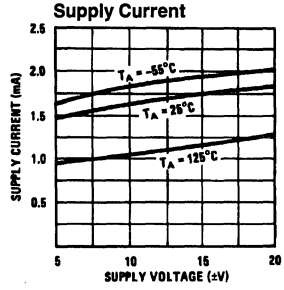
Guaranteed Performance Characteristics LM301A



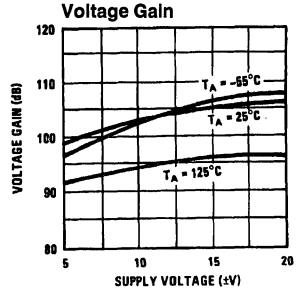
TL/H/7752–6

Typical Performance Characteristics

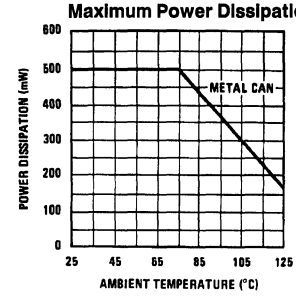
Supply Current



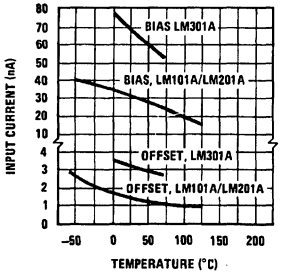
Voltage Gain



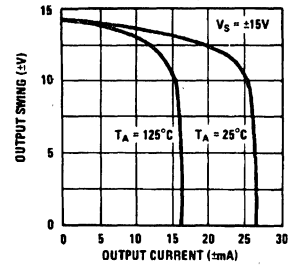
Maximum Power Dissipation



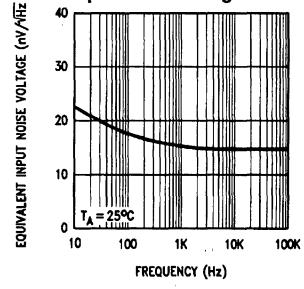
Input Current, LM101A/LM201A/LM301A



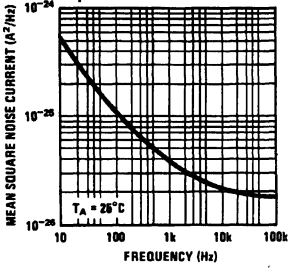
Current Limiting



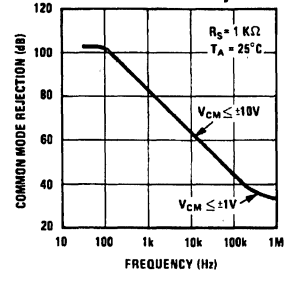
Input Noise Voltage



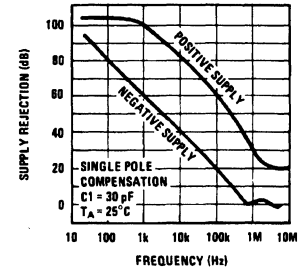
Input Noise Current



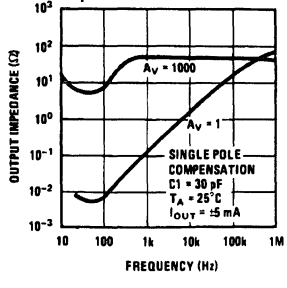
Common Mode Rejection



Power Supply Rejection



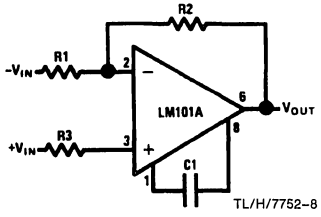
Closed Loop Output Impedance



TL/H/7752–7

Typical Performance Characteristics for Various Compensation Circuits**

Single Pole Compensation

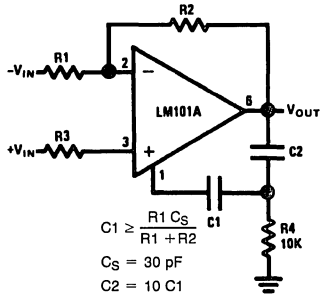


TL/H/7752-8

$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S = 30 pF

Two Pole Compensation



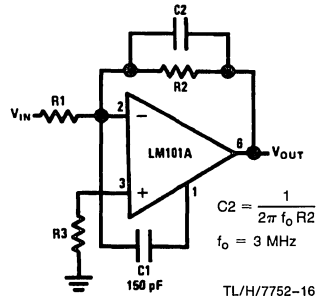
$$C1 \geq \frac{R1\,C_S}{R1 + R2}\ C1$$

C_S = 30 pF

C2 = 10 C1

TL/H/7752-12

Feedforward Compensation

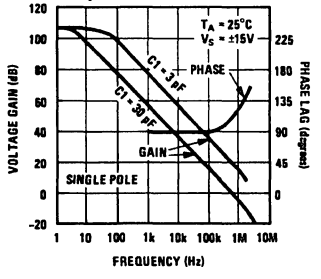


$$C2 = \frac{1}{2\pi\, f_o\, R2}$$

f_o = 3 MHz

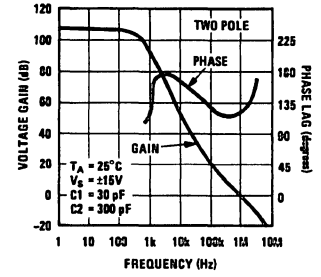
TL/H/7752-16

Open Loop Frequency Response



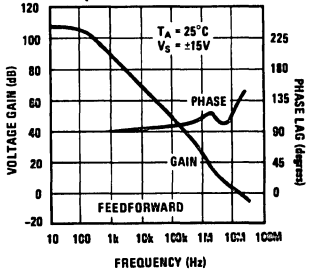
TL/H/7752-9

Open Loop Frequency Response



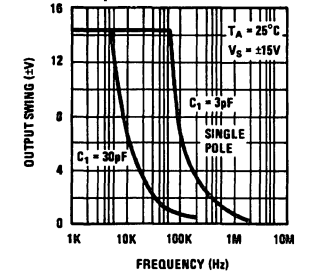
TL/H/7752-13

Open Loop Frequency Response



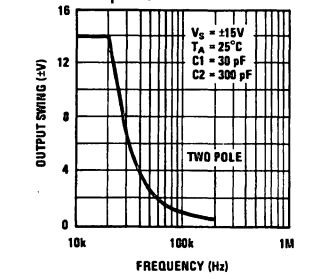
TL/H/7752-17

Large Signal Frequency Response



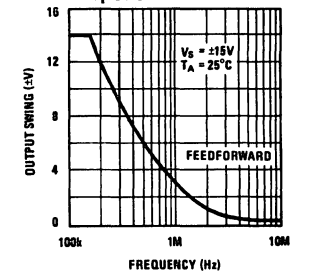
TL/H/7752-10

Large Signal Frequency Response



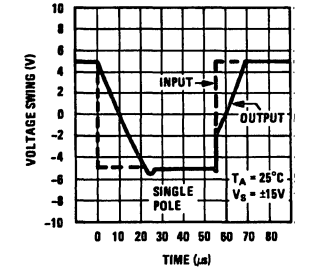
TL/H/7752-14

Large Signal Frequency Response



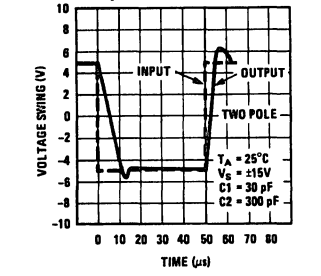
TL/H/7752-18

Voltage Follower Pulse Response



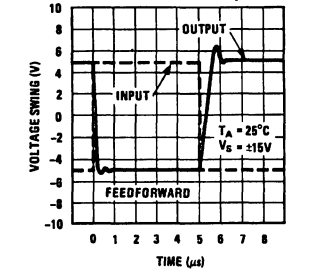
TL/H/7752-11

Voltage Follower Pulse Response



TL/H/7752-15

Inverter Pulse Response



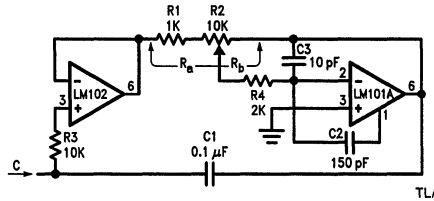
TL/H/7752-19

**Pin connections shown are for 8-pin packages.

Typical Applications**

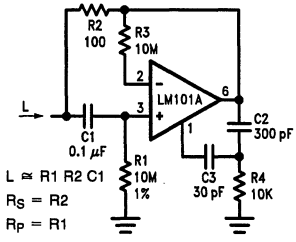
Variable Capacitance Multiplier

$$C = 1 + \frac{R_b}{R_a} C1$$



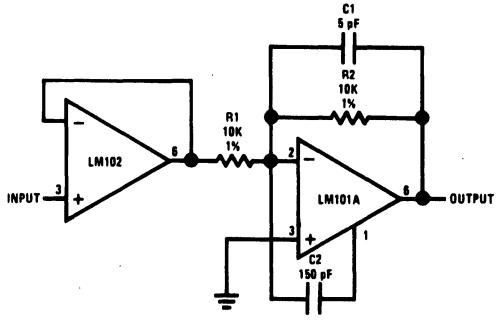
TL/H/7752-20

Simulated Inductor



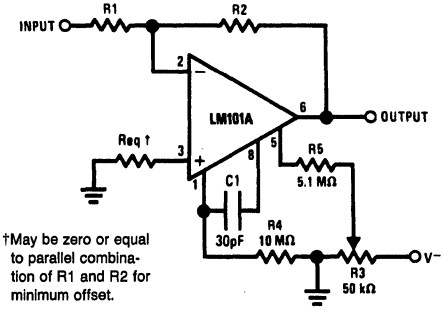
TL/H/7752-21

Fast Inverting Amplifier with High Input Impedance



TL/H/7752-22

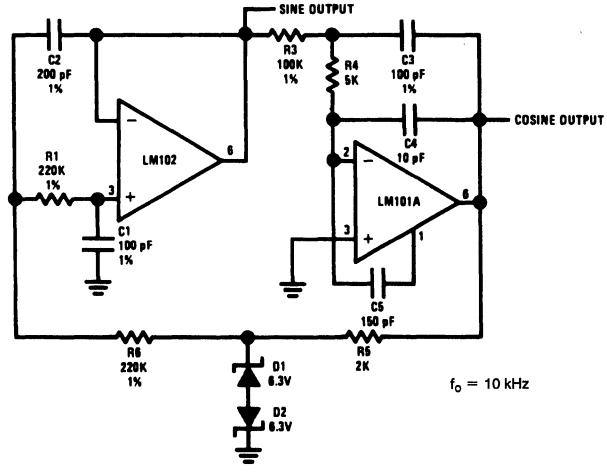
Inverting Amplifier with Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

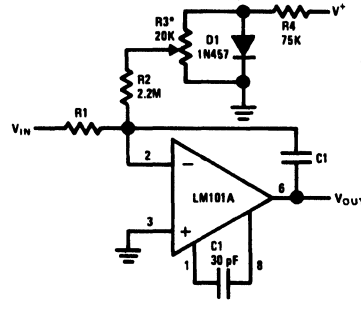
TL/H/7752-23

Sine Wave Oscillator



f_o = 10 kHz

Integrator with Bias Current Compensation



TL/H/7752-25

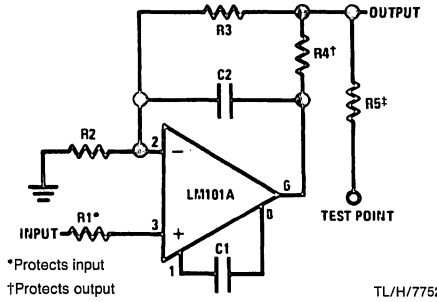
*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

TL/H/7752-24

**Pin connections shown are for 8-pin packages.

Application Hints**

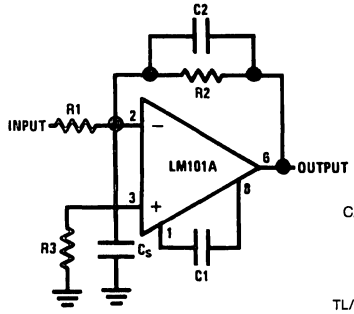
Protecting Against Gross Fault Conditions



*Protects input
†Protects output
‡Protects output—not needed when R4 is used.

TL/H/7752-26

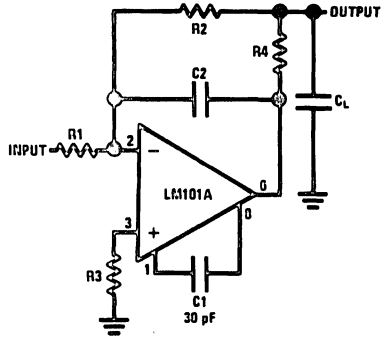
Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\ C_S}{R2}$$

TL/H/7752-27

Isolating Large Capacitive Loads



TL/H/7752-28

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

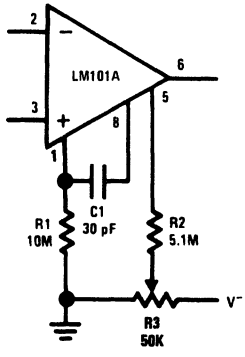
The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

**Pin connections shown are for 8-pin packages.

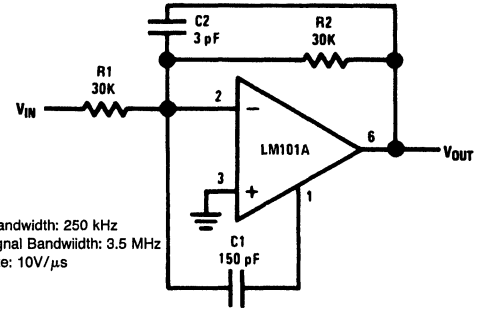
Typical Applications** (Continued)

Standard Compensation and Offset Balancing Circuit



TL/H/7752-29

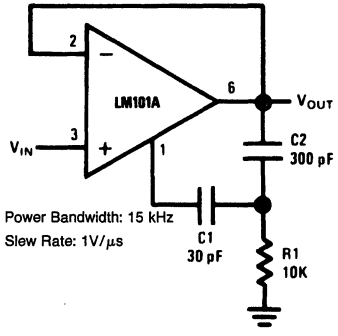
Fast Summing Amplifier



Power Bandwidth: 250 kHz
Small Signal Bandwiidth: 3.5 MHz
Slew Rate: 10V/μs

TL/H/7752-30

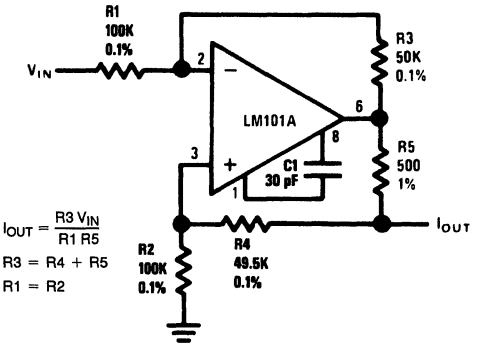
Fast Voltage Follower



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

TL/H/7752-31

Bilateral Current Source

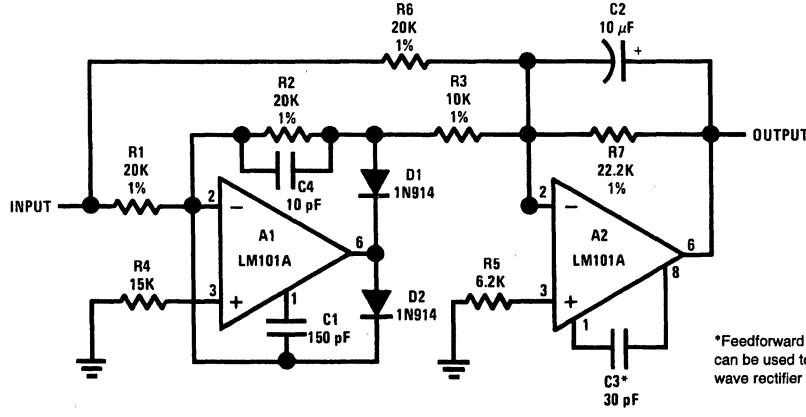


$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$

R3 = R4 + R5
R1 = R2

TL/H/7752-32

Fast AC/DC Converter*



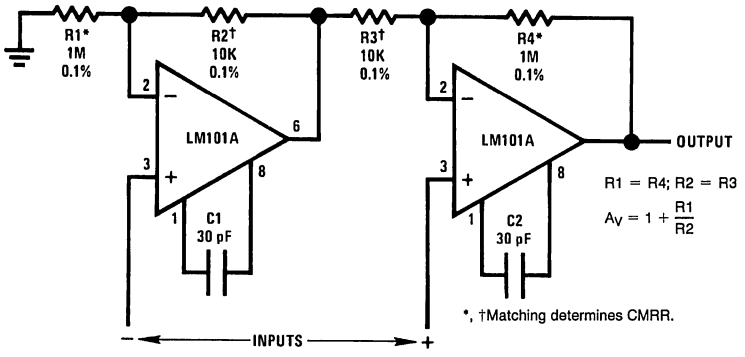
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

TL/H/7752-33

**Pin connections shown are for 8-pin packages.

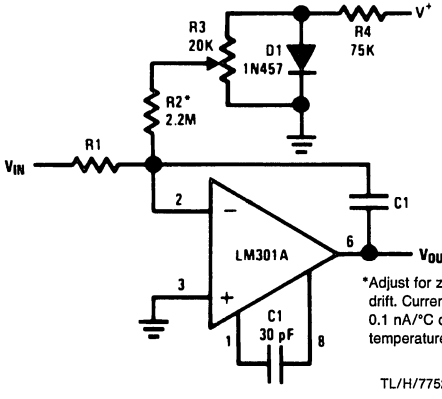
Typical Applications** (Continued)

Instrumentation Amplifier



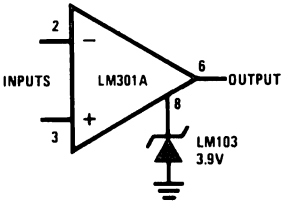
TL/H/7752–34

Integrator with Bias Current Compensation



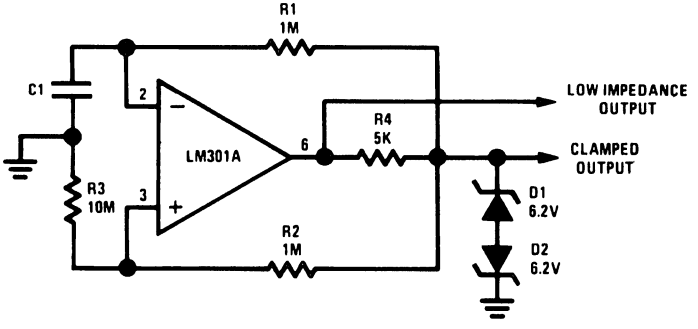
TL/H/7752–35

Voltage Comparator for Driving RTL Logic or High Current Driver



TL/H/7752–37

Low Frequency Square Wave Generator

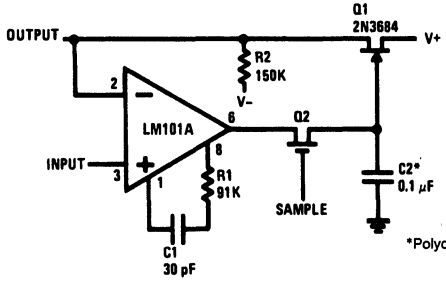


TL/H/7752–36

**Pin connections shown are for 8-pin packages.

Typical Applications** (Continued)

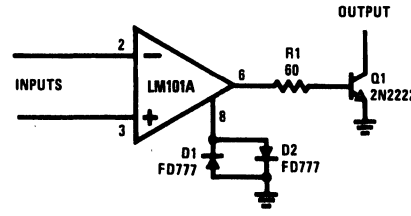
Low Drift Sample and Hold



*Polycarbonate-dielectric capacitor

TL/H/7752-38

Voltage Comparator for Driving DTL or TTL Integrated Circuits



TL/H/7752-39

**Pin connections shown are for 8-pin packages.

National Semiconductor

LM107/LM207/LM307 Operational Amplifiers

General Description

The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741.

The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

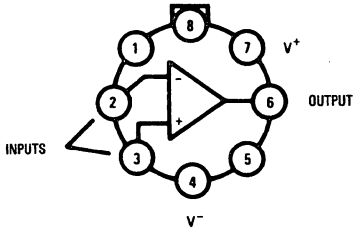
The LM107 is guaranteed over a −55°C to +125°C temperature range, the LM207 from −25°C to +85°C and the LM307 from 0°C to +70°C.

Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

Connection Diagrams

Metal Can Package



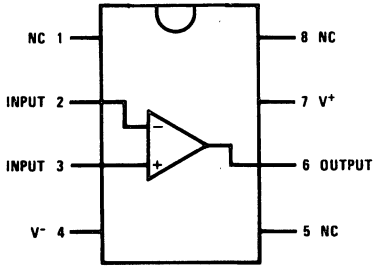
TL/H/7757–2

Note: Pin 4 connected to case.

Top View

Order Number LM107H, LM207H or LM307H
See NS Package Number H08C

Dual-in-Line Package



TL/H/7757–3

Top View

Order Number LM107J, LM207J or LM307J
See NS Package Number J08A
Order Number LM307M
See NS Package Number M08A
Order Number LM307N
See NS Package Number N08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM107/LM207	LM307
Supply Voltage	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous
Operating Temperature Range (T_A)		
(LM107)	−55°C to +125°C	0°C to +70°C
(LM207)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C	260°C

	T_{MIN}	T_{MAX}
LM107	−55°C	+125°C
LM207	−25°C	+85°C
LM307	0°C	+70°C

ESD rating to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$ $V_S = \pm 20V$ $V_S = \pm 15V$		1.8	3.0		 1.8	 3.0	 mA mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$ $V_S = \pm 15V$	±15	 +15 −13		 ±12	 +15 −13		V V
Common Mode Rejection Ratio	$R_S \leq 50\,k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\,k\Omega$	80	96		70	96		dB

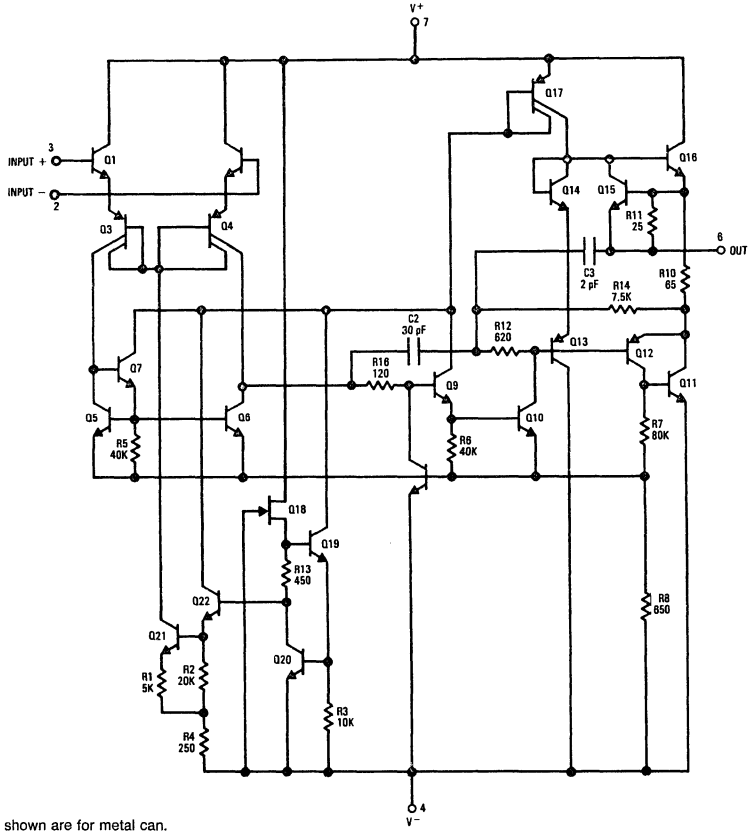
Note 1: The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 30°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq +125°C$ for the LM107 or $-25°C \leq T_A +85°C$ for the LM207, and $0°C \leq T_A \leq +70°C$ and $\pm 5V \leq V_S \leq \pm 15V$ for the LM307 unless otherwise specified.

Note 4: Refer to RETS107X for LM107H and LM107J military specifications.

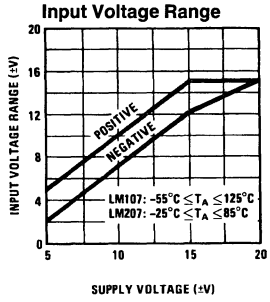
Schematic Diagram*

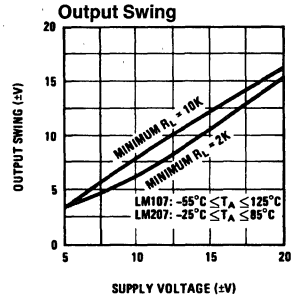


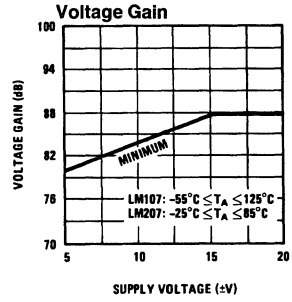
*Pin connections shown are for metal can.

TL/H/7757–1

Guaranteed Performance Characteristics LM107/LM207

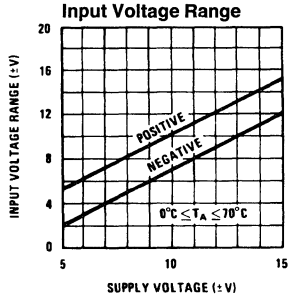


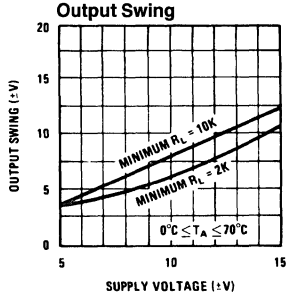


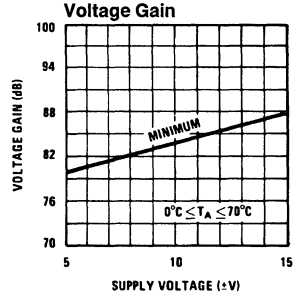


TL/H/7757–4

Guaranteed Performance Characteristics LM307

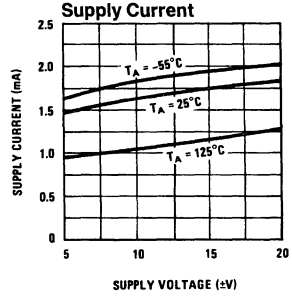


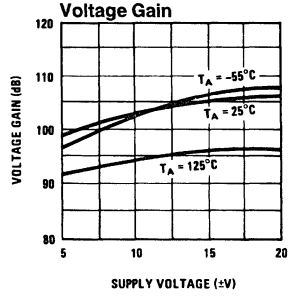


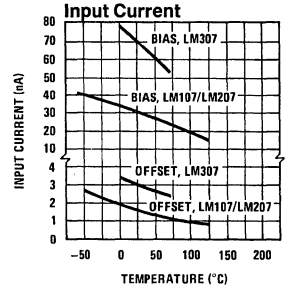


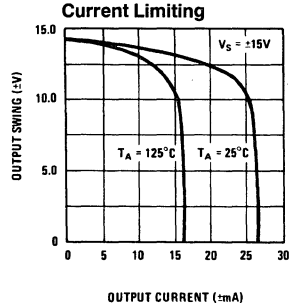
TL/H/7757–5

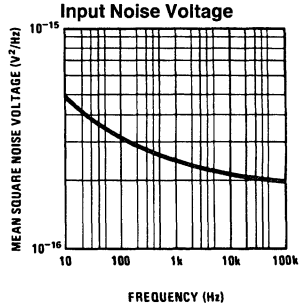
Typical Performance Characteristics

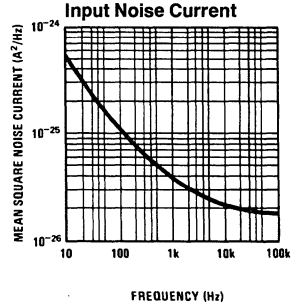








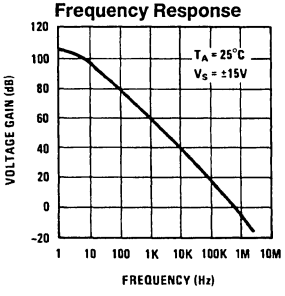




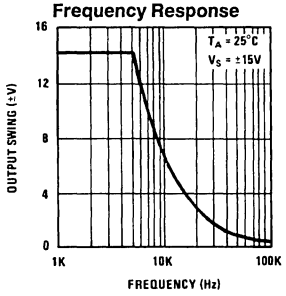
TL/H/7757–6

Typical Performance Characteristics (Continued)

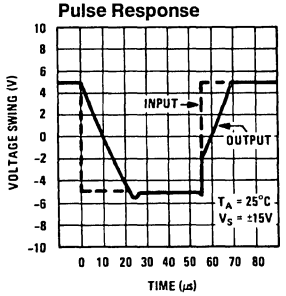
Open Loop Frequency Response



Large Signal Frequency Response



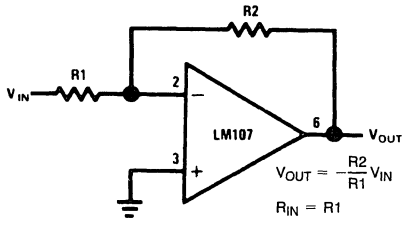
Voltage Follower Pulse Response



TL/H/7757-7

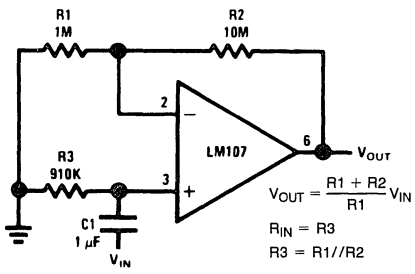
Typical Applications**

Inverting Amplifier



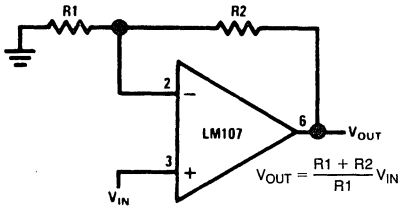
TL/H/7757-8

Non-Inverting AC Amplifier



TL/H/7757-9

Non-Inverting Amplifier

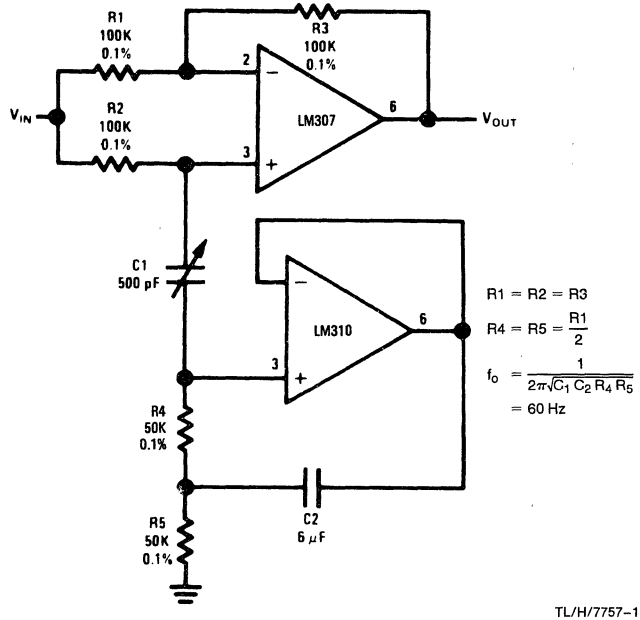


TL/H/7757-10

**Pin connections shown are for metal can.

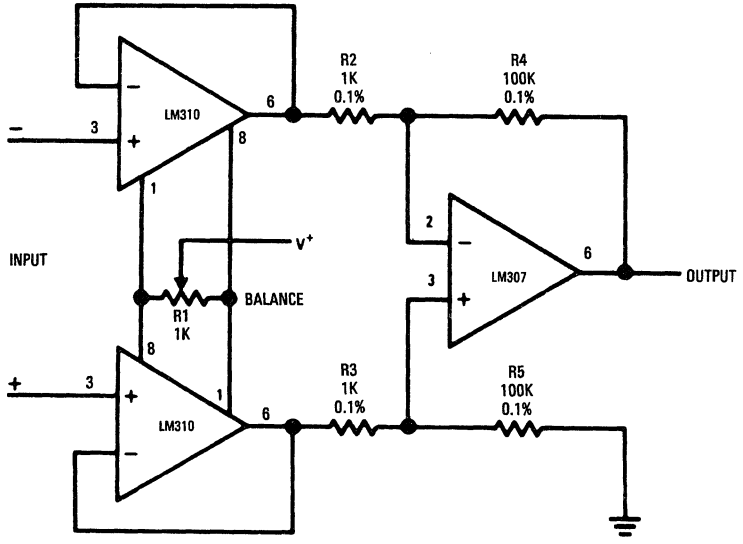
Typical Applications** (Continued)

Turntable Notch Filter



TL/H/7757–11

Differential Input Instrumentation Amplifier



TL/H/7757–12

**Pin connections shown are for metal can.

National Semiconductor

LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

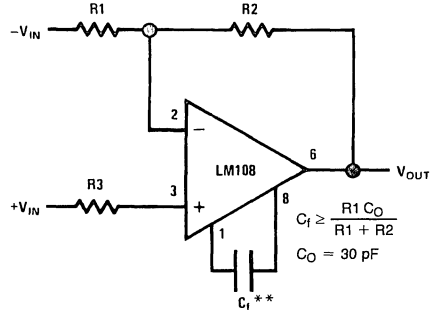
The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

Compensation Circuits

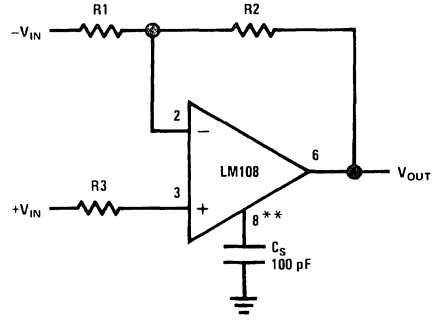
Standard Compensation Circuit



TL/H/7758–1

**Bandwidth and slew rate are proportional to $1/C_f$

Alternate* Frequency Compensation

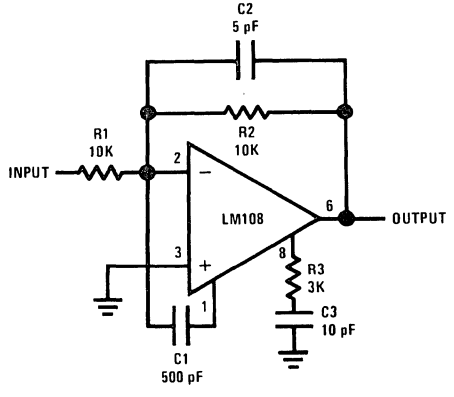


TL/H/7758–2

*Improves rejection of power supply noise by a factor of ten.

**Bandwidth and slew rate are proportional to $1/C_S$

Feedforward Compensation



TL/H/7758–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM108/LM208	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
(LM208)	−25°C to + 85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		
DIP	260°C	260°C
H Package Lead Temp		
(Soldering 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	
Small Outline Package		
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 6)	2000V	

Electrical Characteristics (Note 4)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = +125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Electrical Characteristics (Note 4) (Continued)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

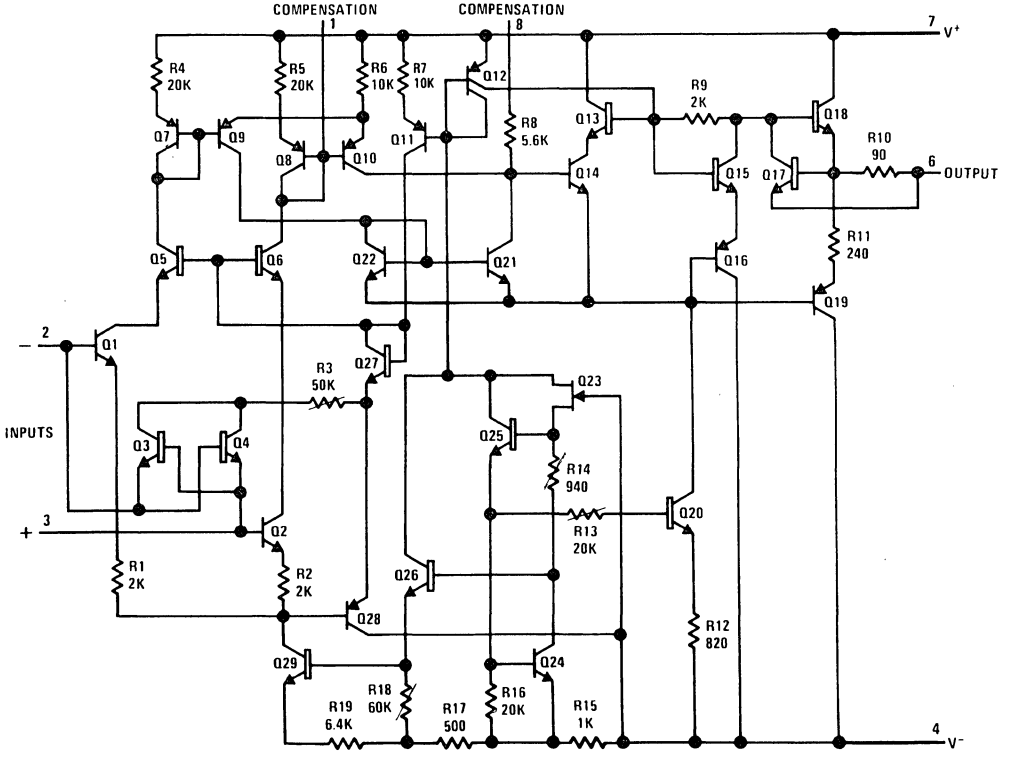
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LM308 they are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Refer to RETS108X for LM108 military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

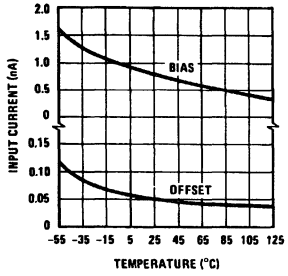
Schematic Diagram



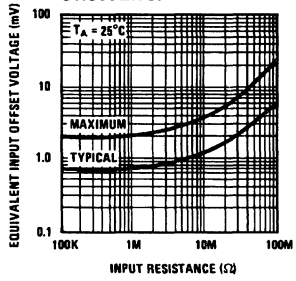
TL/H/7758–8

Typical Performance Characteristics LM108/LM208

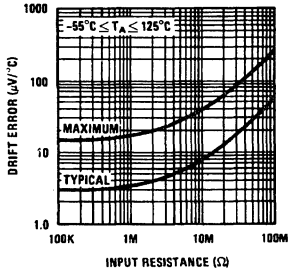
Input Currents



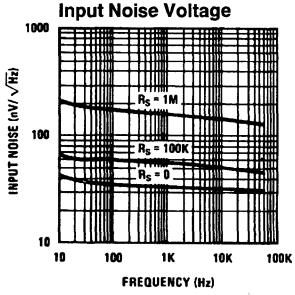
Offset Error



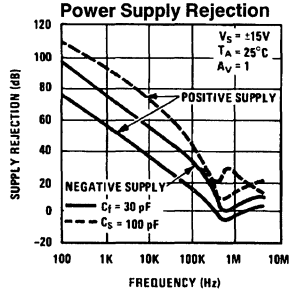
Drift Error



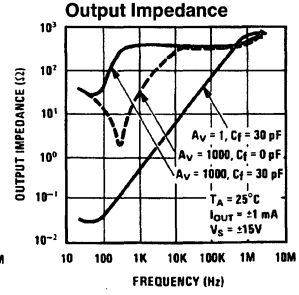
Input Noise Voltage



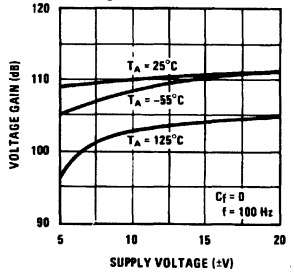
Power Supply Rejection



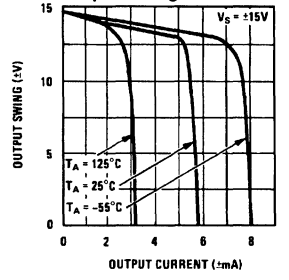
Closed Loop Output Impedance



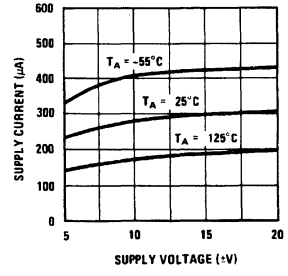
Voltage Gain



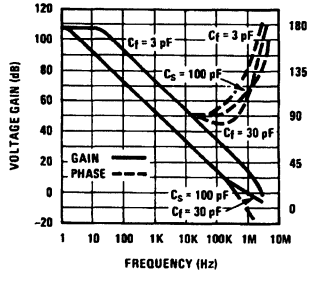
Output Swing



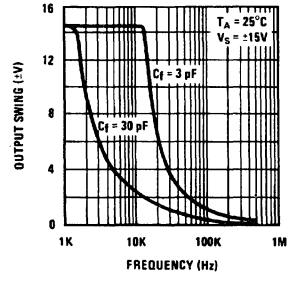
Supply Current



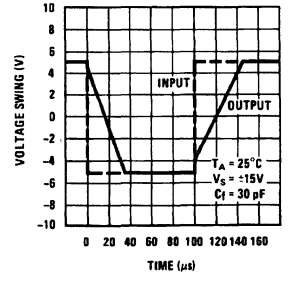
Open Loop Frequency Response



Large Signal Frequency Response



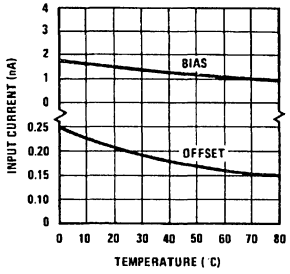
Voltage Follower Pulse Response



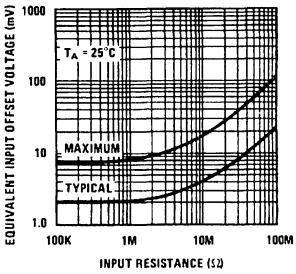
TL/H/7758–6

Typical Performance Characteristics LM308

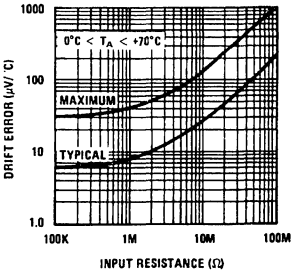
Input Currents



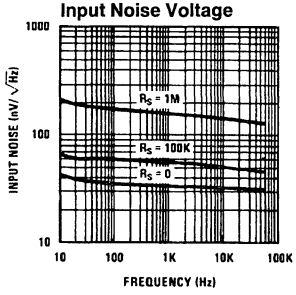
Offset Error



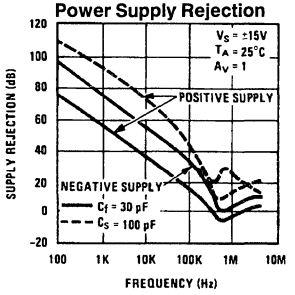
Drift Error



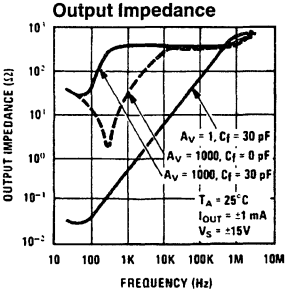
Input Noise Voltage



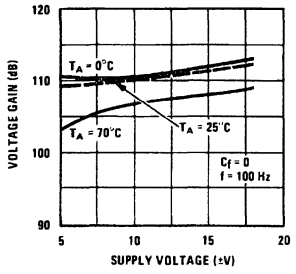
Power Supply Rejection



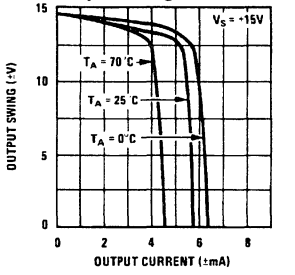
Closed Loop Output Impedance



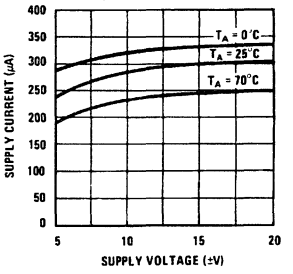
Voltage Gain



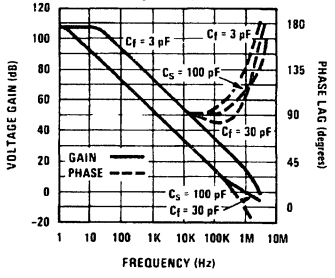
Output Swing



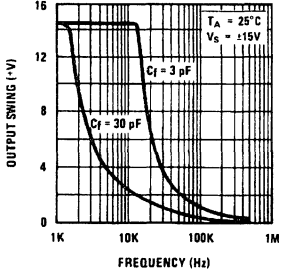
Supply Current



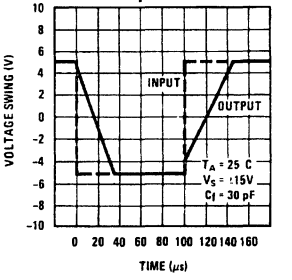
Open Loop Frequency Response



Large Signal Frequency Response



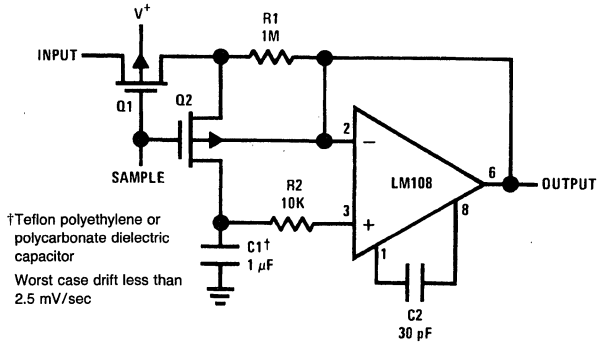
Voltage Follower Pulse Response



TL/H/7758–7

Typical Applications

Sample and Hold

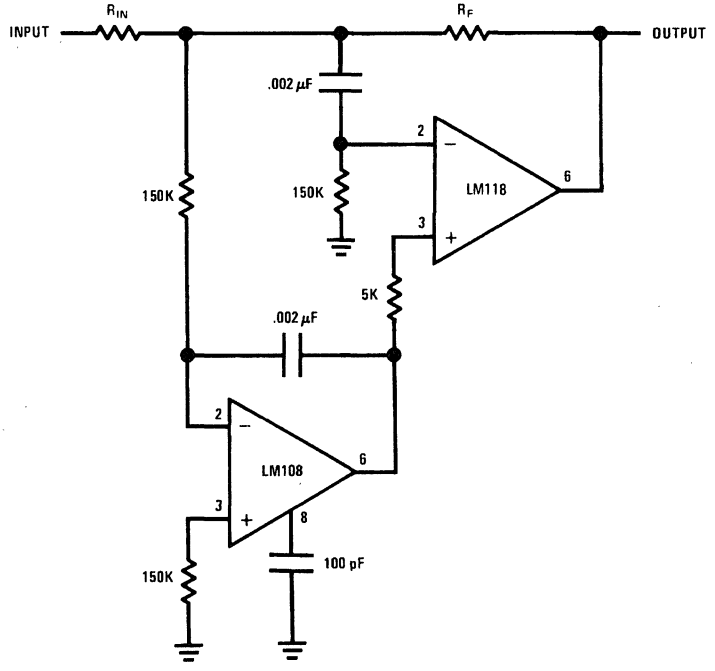


†Teflon polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

TL/H/7758–4

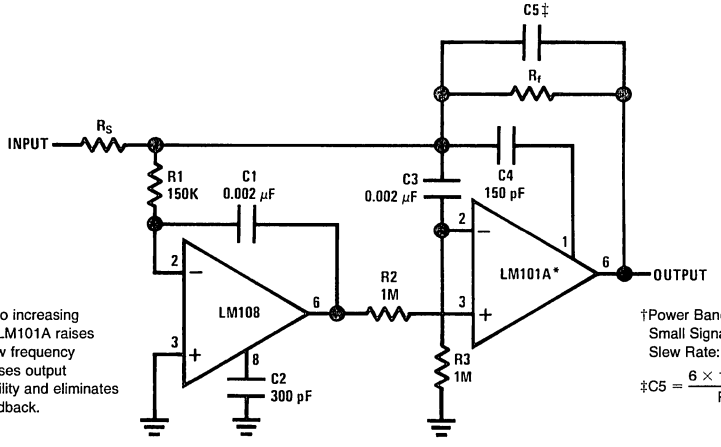
High Speed Amplifier with Low Drift and Low Input Current



TL/H/7758–5

Typical Applications (Continued)

Fast† Summing Amplifier



*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

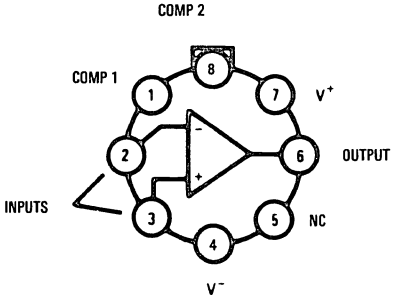
†Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

$$\ddagger C5 = \frac{6 \times 10^{-8}}{R_f}$$

TL/H/7758–12

Connection Diagrams

Metal Can Package



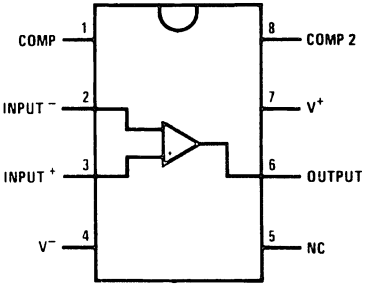
TL/H/7758–13

Order Number LM108H, LM208H or LM308H
See NS Package Number H08C

*Package is connected to Pin 4 (V^-)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Dual-In-Line Package



TL/H/7758–15

Top View

Order Number LM108J-8, LM208J-8, LM308J-8, LM308M or LM308N
See NS Package Number J08A, MO8A or NO8E

National Semiconductor

LM108A/LM208A/LM308A Operational Amplifiers

General Description

The LM108/LM108A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±18V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

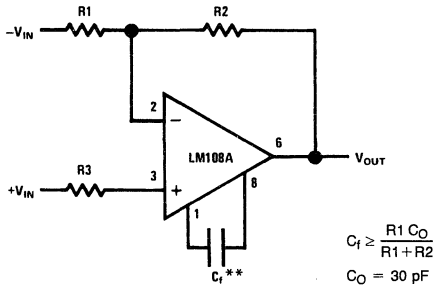
The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a −25°C to +85°C temperature range, instead of −55°C to +125°C. The LM308A devices have slightly-relaxed specifications and performances over a 0°C to +70°C temperature range.

Features

- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 μV/°C drift

Compensation Circuits

Standard Compensation Circuit



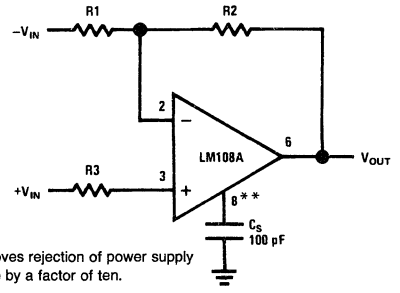
$C_f \geq \frac{R1\,C_O}{R1+R2}$

C_O = 30 pF

TL/H/7759–1

**Bandwidth and slew rate are proportional to $1/C_f$.

Alternate* Frequency Compensation

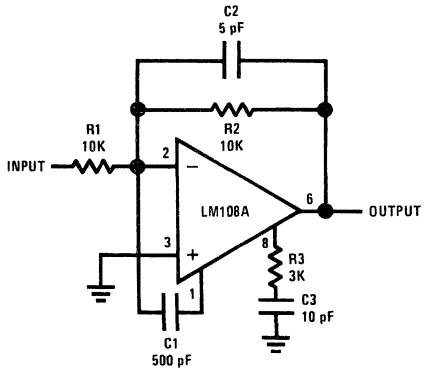


*Improves rejection of power supply noise by a factor of ten.

TL/H/7759–2

**Bandwidth and slew rate are proportional to $1/C_S$.

Feedforward Compensation



TL/H/7759–3

LM108A/LM208A Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous
Operating Free Air Temperature Range	
LM108A	−55°C to +125°C
LM208A	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) (DIP)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 6)	2000V

Electrical Characteristics (Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0	nA
Input Resistance	$T_A = 25°C$	30	70		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	80	300		V/mV
Input Offset Voltage				1.0	mV
Average Temperature Coefficient of Input Offset Voltage			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	$T_A = 125°C$		0.15	0.4	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	40			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

Note 5: Refer to RETS108AX for LM108AH and LM108AJ-8 military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

LM308A Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
H-Package Lead Temperature (Soldering, 10 sec.)	300°C
Lead Temperature (Soldering, 10 sec.) (DIP)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$		0.3	0.5	mV
Input Offset Current	$T_A = 25°C$		0.2	1	nA
Input Bias Current	$T_A = 25°C$		1.5	7	nA
Input Resistance	$T_A = 25°C$	10	40		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	80	300		V/mV
Input Offset Voltage	$V_S = \pm 15V$, $R_S = 100\Omega$			0.73	mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm 15V$, $R_S = 100\Omega$		2.0	5.0	μV/°C
Input Offset Current				1.5	nA
Average Temperature Coefficient of Input Offset Current			2.0	10	pA/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	60			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±14			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB

Note 1: The maximum junction temperature of the LM308A is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

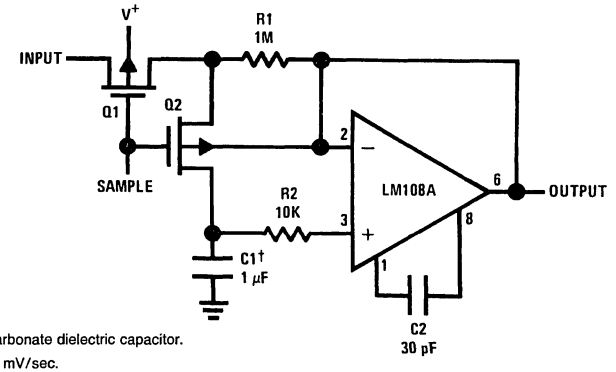
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$, unless otherwise specified.

Typical Applications

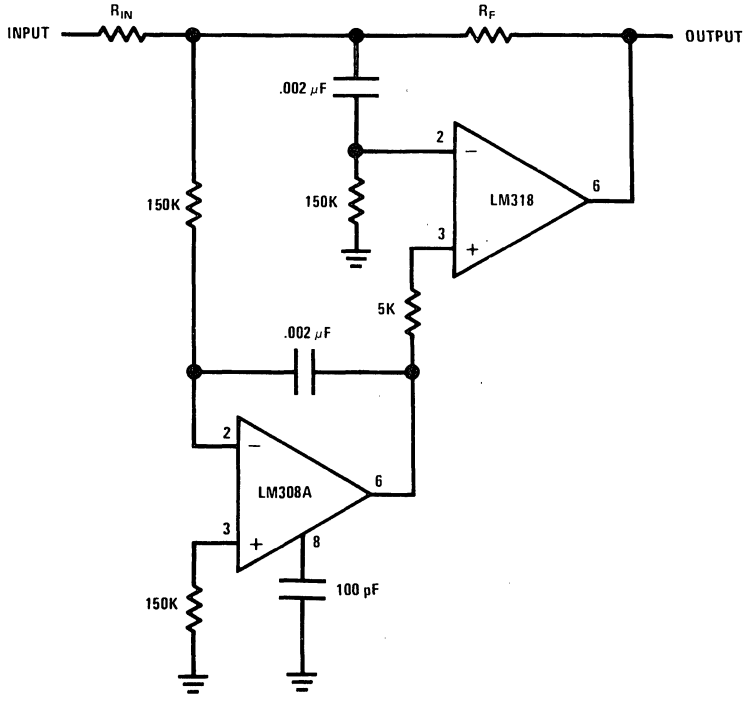
Sample and Hold



†Teflon, polyethylene or polycarbonate dielectric capacitor.
Worst case drift less than 2.5 mV/sec.

TL/H/7759–4

High Speed Amplifier with Low Drift and Low Input Current



TL/H/7759–5

Application Hints

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted.

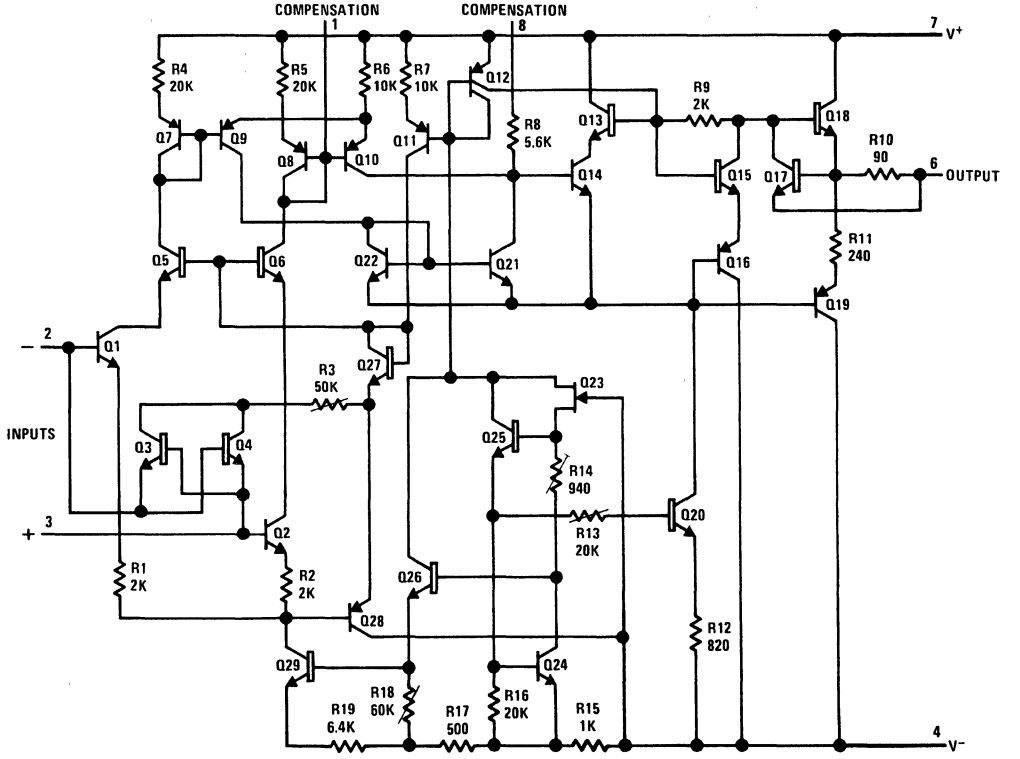
Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally, are the package-to-printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together helps greatly.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evanohm or manganin are best since they only generate about 2 μV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example, a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 μV error. All of the gain fixing resistor should be the same material.

Testing low drift amplifiers is also difficult. Standard drift testing technique such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method—do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal.

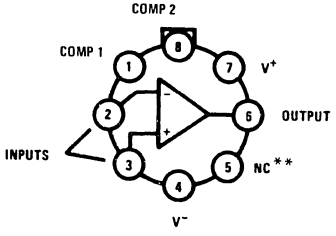
Schematic Diagram



TL/H/7759–6

Connection Diagrams

Metal Can Package



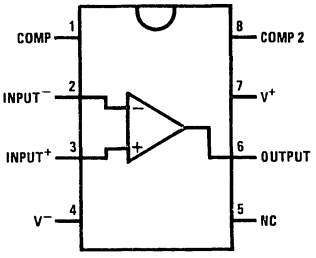
TL/H/7759–7

Pin 4 is connected to the case.

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Order Number LM108AH, LM208AH or LM208AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/7759–8

Top View

Order Number LM108AJ-8, LM208AJ-8, LM308AJ-8, LM308AM or LM308AN
See NS Package Number J08A, M08A or N08E

National Semiconductor

LM112/LM212/LM312 Operational Amplifiers

General Description

The LM112 series are micropower operational amplifiers with very low offset-voltage and input-current errors—at least a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range. Similar to the LM108 series, that also use supergain transistors, they differ in that they include internal frequency compensation and have provisions for offset adjustment with a single potentiometer.

These amplifiers will operate on supply voltages of ±2V to ±20V, drawing a quiescent current of only 300 μA. Performance is not appreciably affected over this range of voltages, so operation from unregulated power sources is easily accomplished. They can also be run from a single supply like the 5V used for digital circuits.

The LM112 series are the first IC amplifiers to improve reliability by including overvoltage protection for the MOS compensation capacitor. Without this feature, IC's have been known to suffer catastrophic failure caused by short-duration overvoltage spikes on the supplies. Unlike other internally-compensated IC amplifiers, it is possible to overcompensate with an external capacitor to increase stability margin.

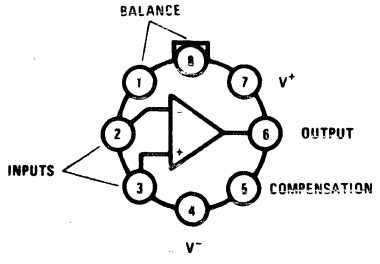
The LM212 is identical to the LM112, except that the LM212 has its performance guaranteed over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM312 is guaranteed over a 0°C to +70°C temperature range.

Features

- Maximum input bias current of 3 nA over temperature
- Offset current less than 400 pA over temperature
- Low noise
- Guaranteed drift specifications

Connection Diagram

Metal Can Package



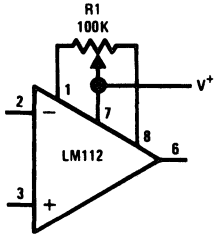
TL/H/7751–4

Top View

Order Number LM112H, LM212H, or LM312H
See NS Package Number H08C

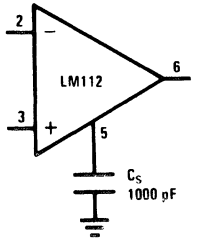
Auxiliary Circuits

Offset Balancing



TL/H/7751–2

Overcompensation for Greater Stability Margin



TL/H/7751–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 5)

	LM112/LM212	LM312
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range		
LM112	−55°C to +125°C	0°C to +70°C
LM212	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM112/LM212			LM312			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = 125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$	±13	±14		±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common-Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM112 is 150°C, LM212 is 100°C and LM312 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

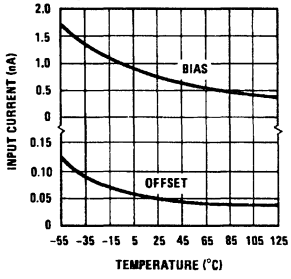
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM112), $-25°C \leq T_A \leq +85°C$ (LM212), $\pm 5V \leq V_S \leq \pm 15V$ and $0° C \leq T_A \leq +70°C$ (LM312) unless otherwise noted.

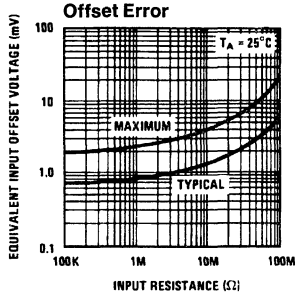
Note 5: Refer to RETS112X for LM112H military specifications.

Typical Performance Characteristics LM112/LM212

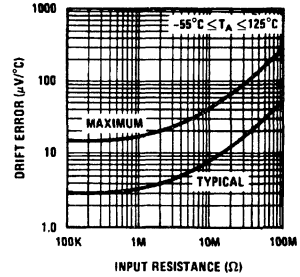
Input Currents



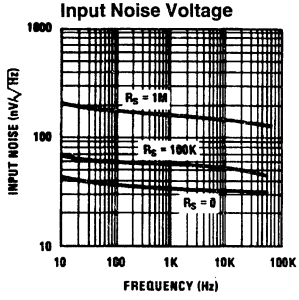
Offset Error



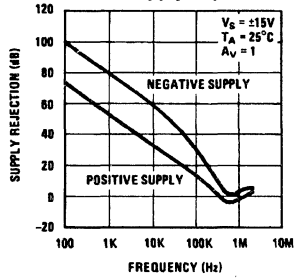
Drift Error



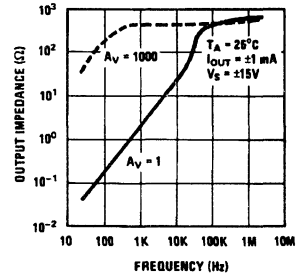
Input Noise Voltage



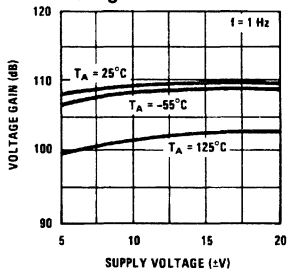
Power Supply Rejection



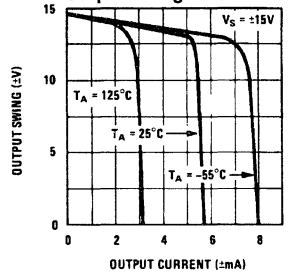
Closed Loop Output Impedance



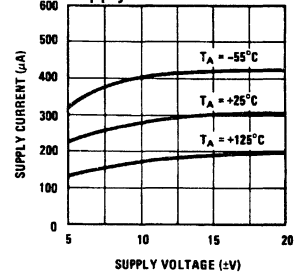
Voltage Gain



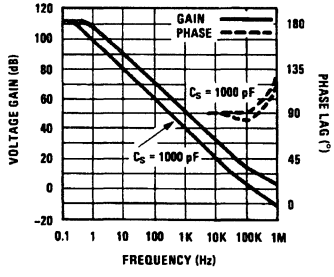
Output Swing



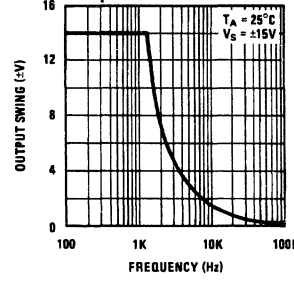
Supply Current



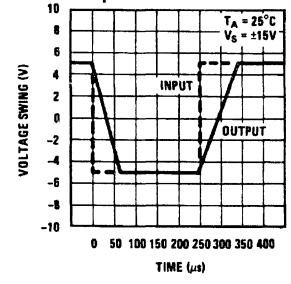
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



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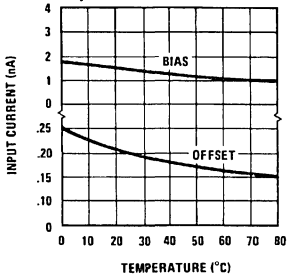
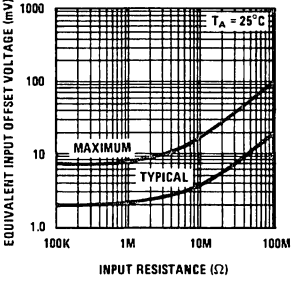
Typical Performance Characteristics LM312

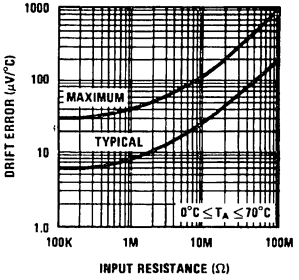
Input Currents



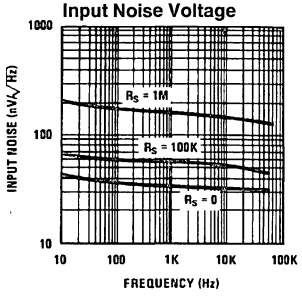
Offset Error



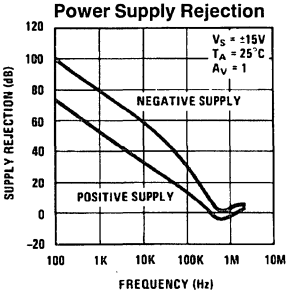
Drift Error



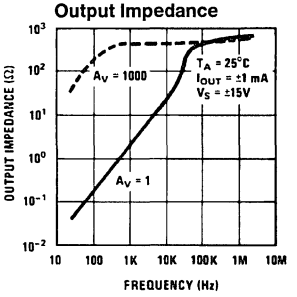
Input Noise Voltage



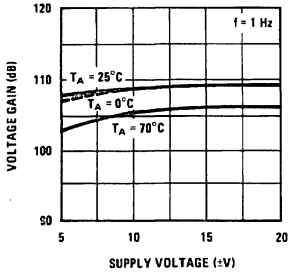
Power Supply Rejection



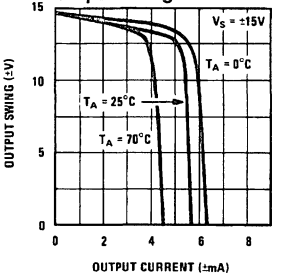
Closed Loop Output Impedance



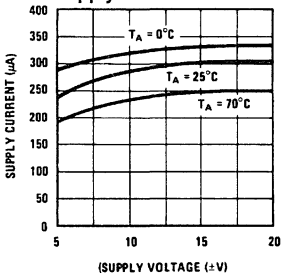
Voltage Gain



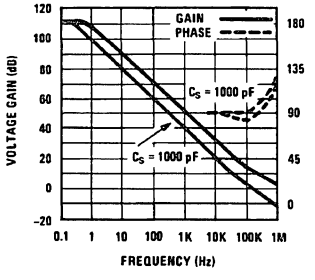
Output Swing



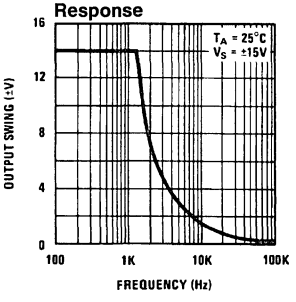
Supply Current



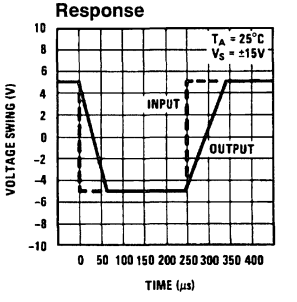
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



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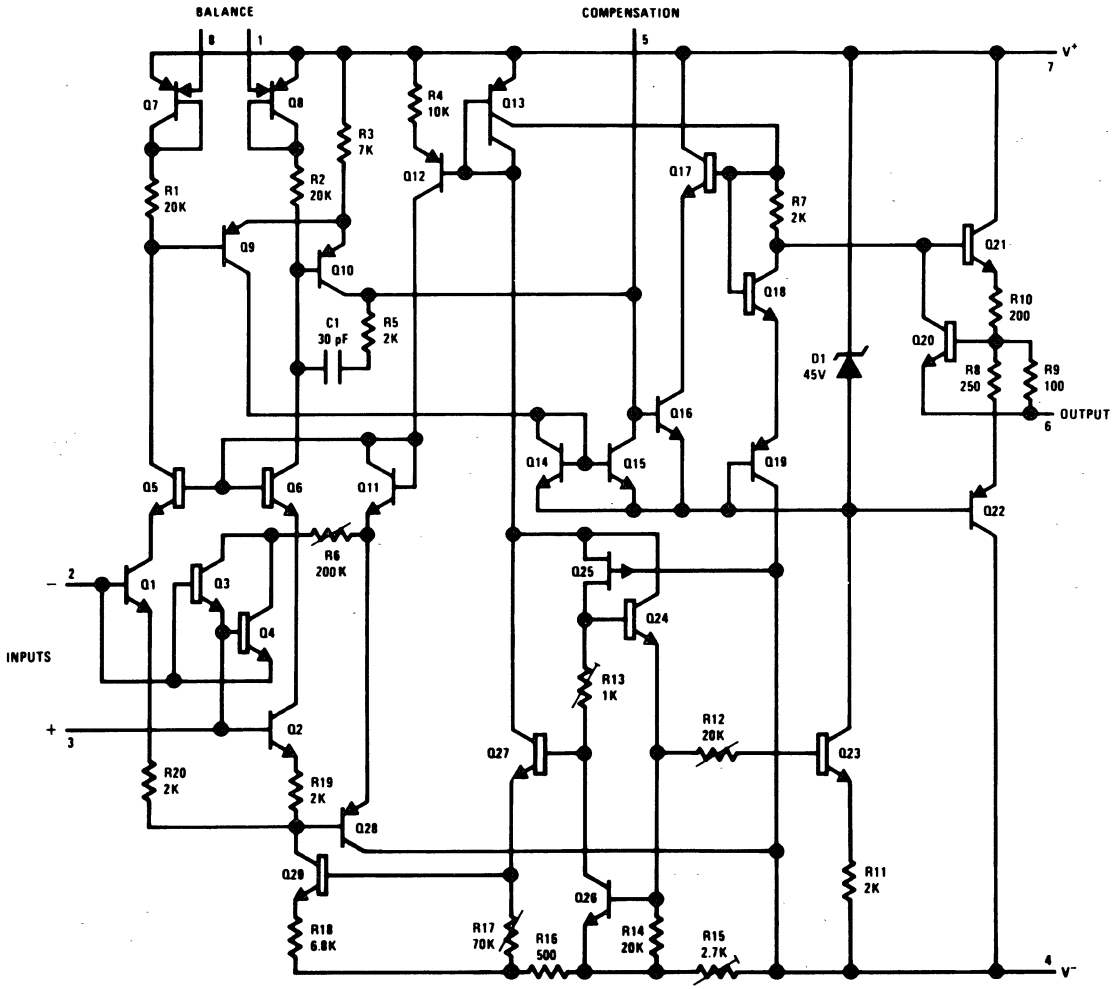
Schematic Diagram



TL/H/7751–1

National Semiconductor

LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

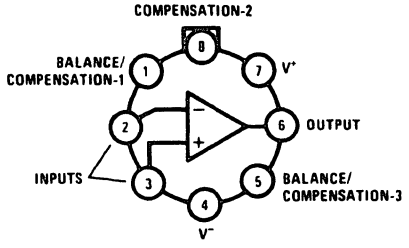
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Connection Diagrams

Metal Can Package*



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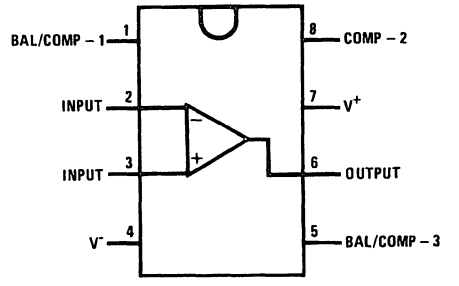
Top View

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H, LM218H or LM318H
See NS Package Number H08C

Dual-In-Line Package



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Top View

Order Number LM118J-8, LM318J-8, LM318M or LM318N
See NS Package Number J08A, M08A or N08B

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous

Operating Temperature Range	
LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Hermetic Package	300°C
Plastic Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7) 2000V

Electrical Characteristics (Note 4)

Parameter	Conditions	LM118/LM218			LM318			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2	4		4	10	mV
Input Offset Current	$T_A = 25°C$		6	50		30	200	nA
Input Bias Current	$T_A = 25°C$		120	250		150	500	nA
Input Resistance	$T_A = 25°C$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25°C$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25°C$, $V_S = \pm 15V$, $A_V = 1$ (Note 5)	50	70		50	70		V/μs
Small Signal Bandwidth	$T_A = 25°C$, $V_S = \pm 15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125°C$		4.5	7				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±12	±13		±12	±13		V
Input Voltage Range	$V_S = \pm 15V$	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM118), $-25°C \leq T_A \leq +85°C$ (LM218), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

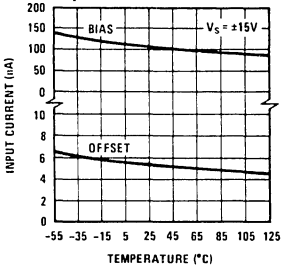
Note 5: Slew rate is tested with $V_S = \pm 15V$. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

Note 6: Refer to RETS118X for LM118H and LM118J-8 military specifications.

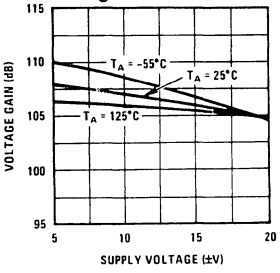
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics LM118, LM218

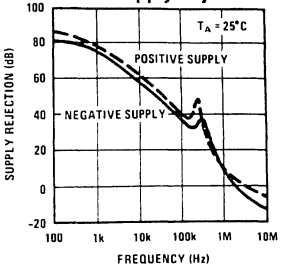
Input Current



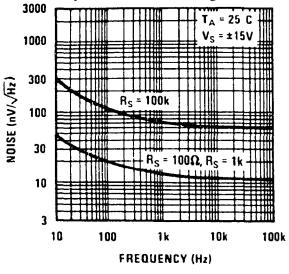
Voltage Gain



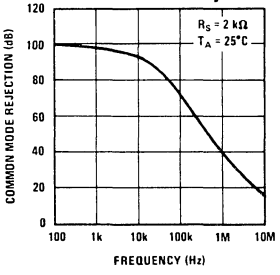
Power Supply Rejection



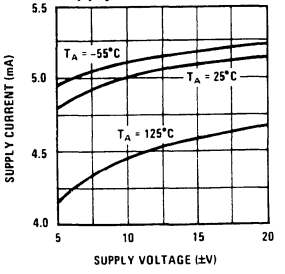
Input Noise Voltage



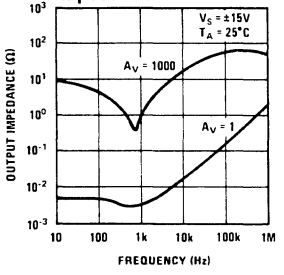
Common Mode Rejection



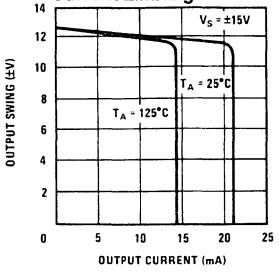
Supply Current



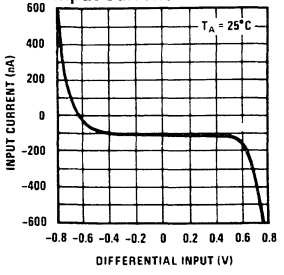
Closed Loop Output Impedance



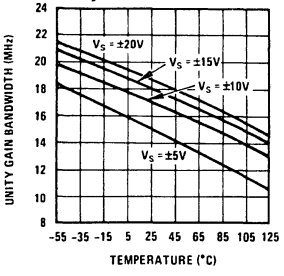
Current Limiting



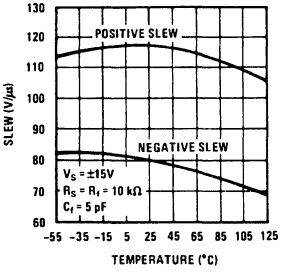
Input Current



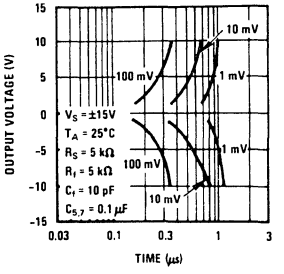
Unity Gain Bandwidth



Voltage Follower Slew Rate



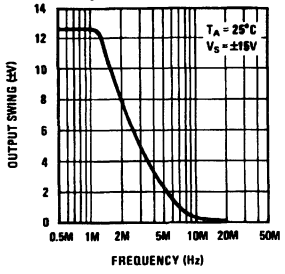
Inverter Settling Time



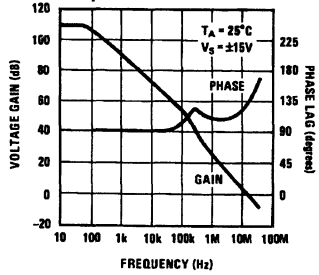
TL/H/7766–4

Typical Performance Characteristics LM118, LM218 (Continued)

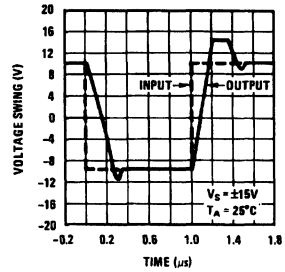
Large Signal Frequency Response



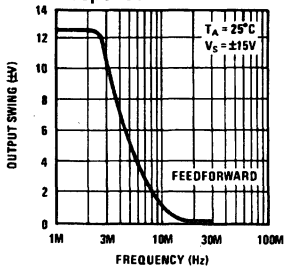
Open Loop Frequency Response



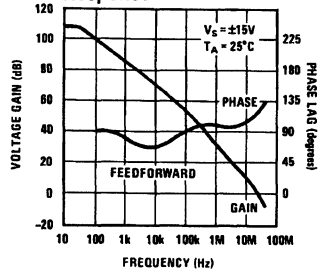
Voltage Follower Pulse Response



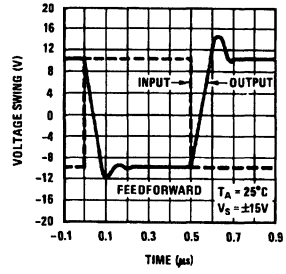
Large Signal Frequency Response



Open Loop Frequency Response



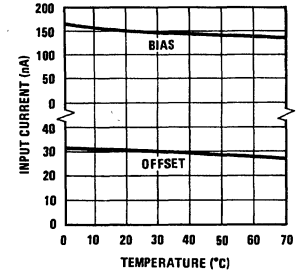
Inverter Pulse Response



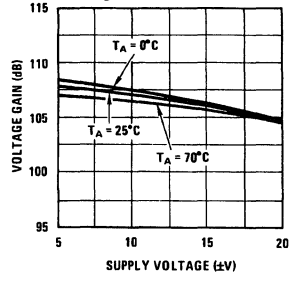
TL/H/7766–5

Typical Performance Characteristics LM318

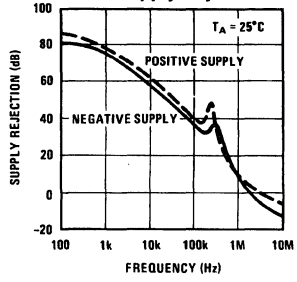
Input Current



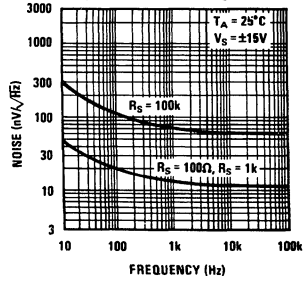
Voltage Gain



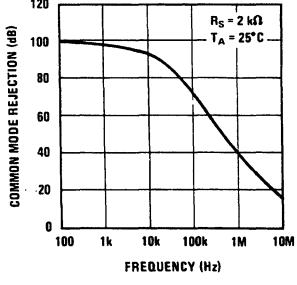
Power Supply Rejection



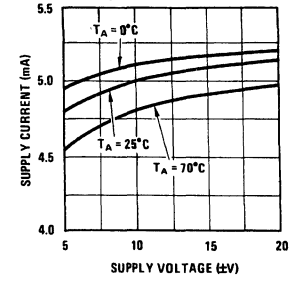
Input Noise Voltage



Common Mode Rejection



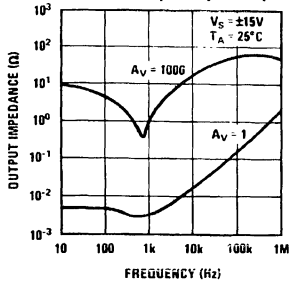
Supply Current



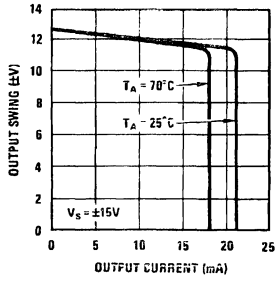
TL/H/7766–6

Typical Performance Characteristics LM318 (Continued)

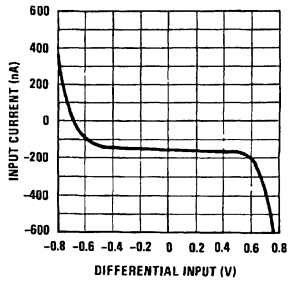
Closed Loop Output Impedance



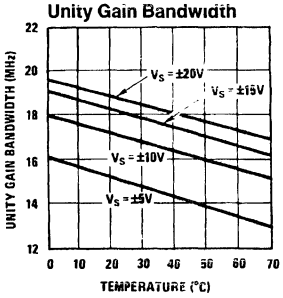
Current Limiting



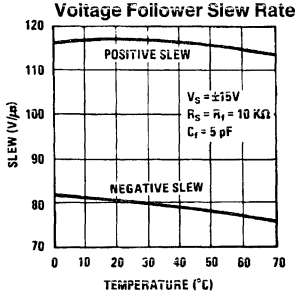
Input Current



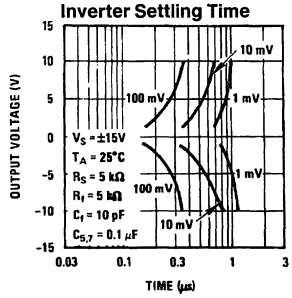
Unity Gain Bandwidth



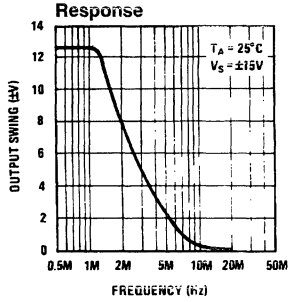
Voltage Follower Slew Rate



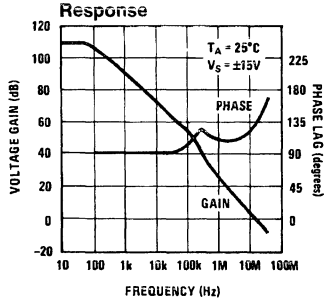
Inverter Settling Time



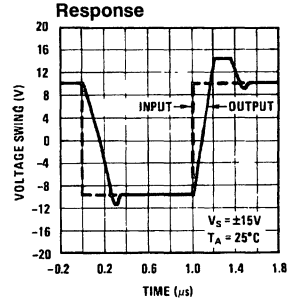
Large Signal Frequency Response



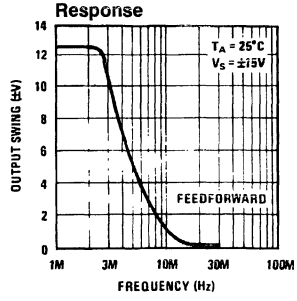
Open Loop Frequency Response



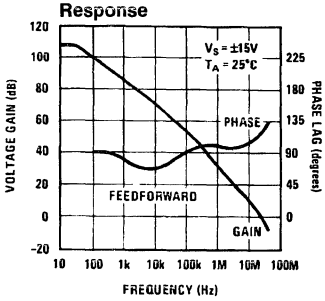
Voltage Follower Pulse Response



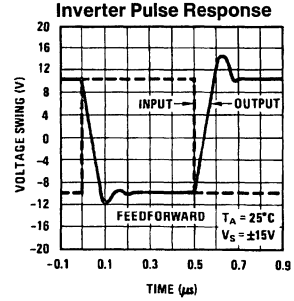
Large Signal Frequency Response



Open Loop Frequency Response



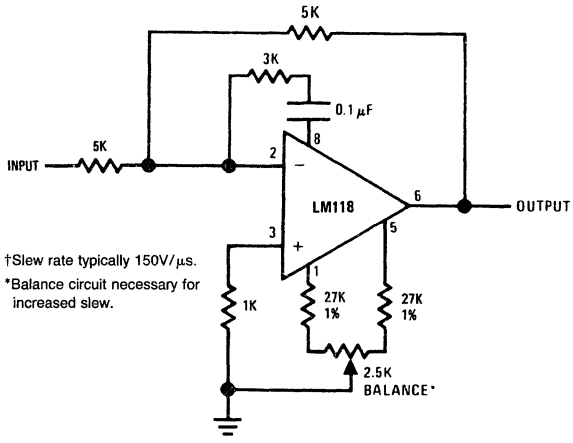
Inverter Pulse Response



TL/H/7766–7

Auxiliary Circuits

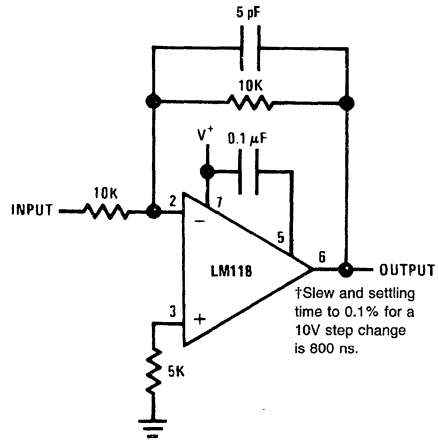
Feedforward Compensation for Greater Inverting Slew Rate†



†Slew rate typically 150V/μs.
*Balance circuit necessary for increased slew.

TL/H/7766–8

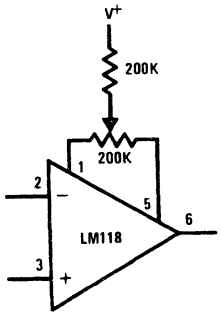
Compensation for Minimum Settling† Time



†Slew and settling time to 0.1% for a 10V step change is 800 ns.

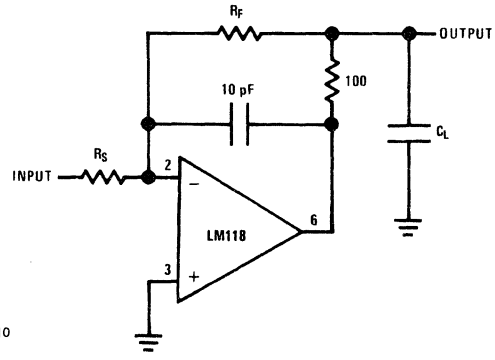
TL/H/7766–9

Offset Balancing



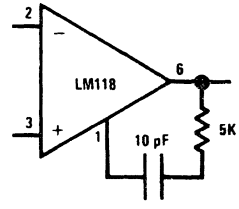
TL/H/7766–10

Isolating Large Capacitive Loads



TL/H/7766–11

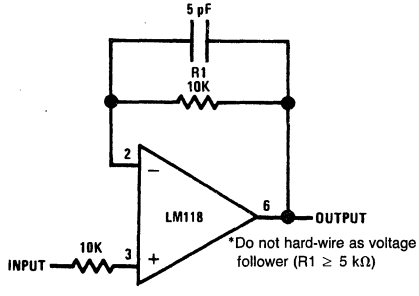
Overcompensation



TL/H/7766–12

Typical Applications

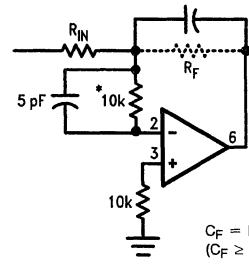
Fast Voltage Follower*



*Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

TL/H/7766–13

Integrator or Slow Inverter



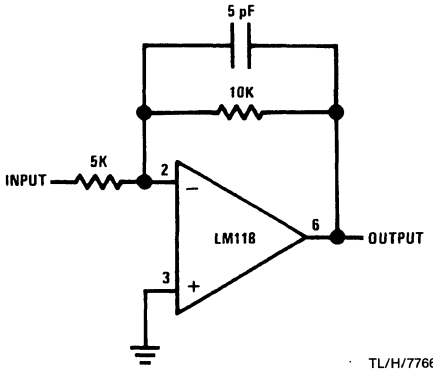
C_F = Large ($C_F \geq 50$ pF)

TL/H/7766–14

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

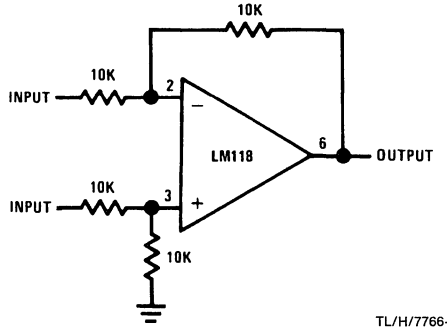
Typical Applications (Continued)

Fast Summing Amplifier



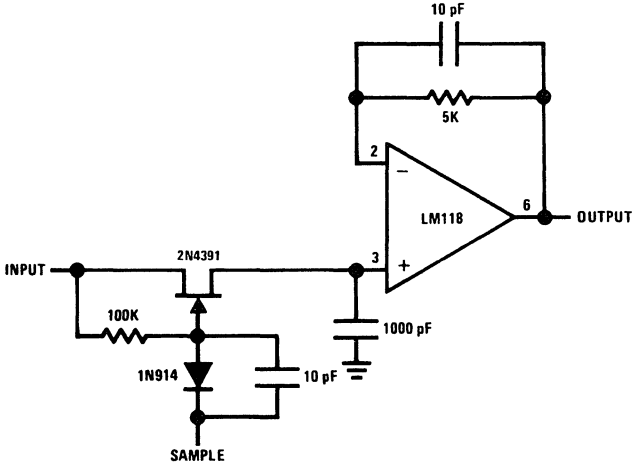
TL/H/7766-15

Differential Amplifier



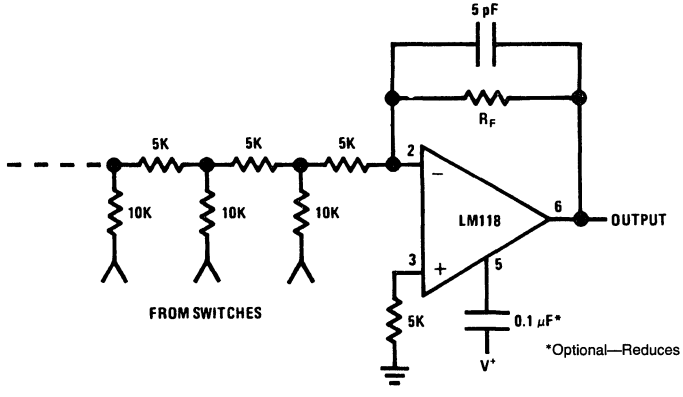
TL/H/7766-16

Fast Sample and Hold



TL/H/7766-18

D/A Converter Using Ladder Network

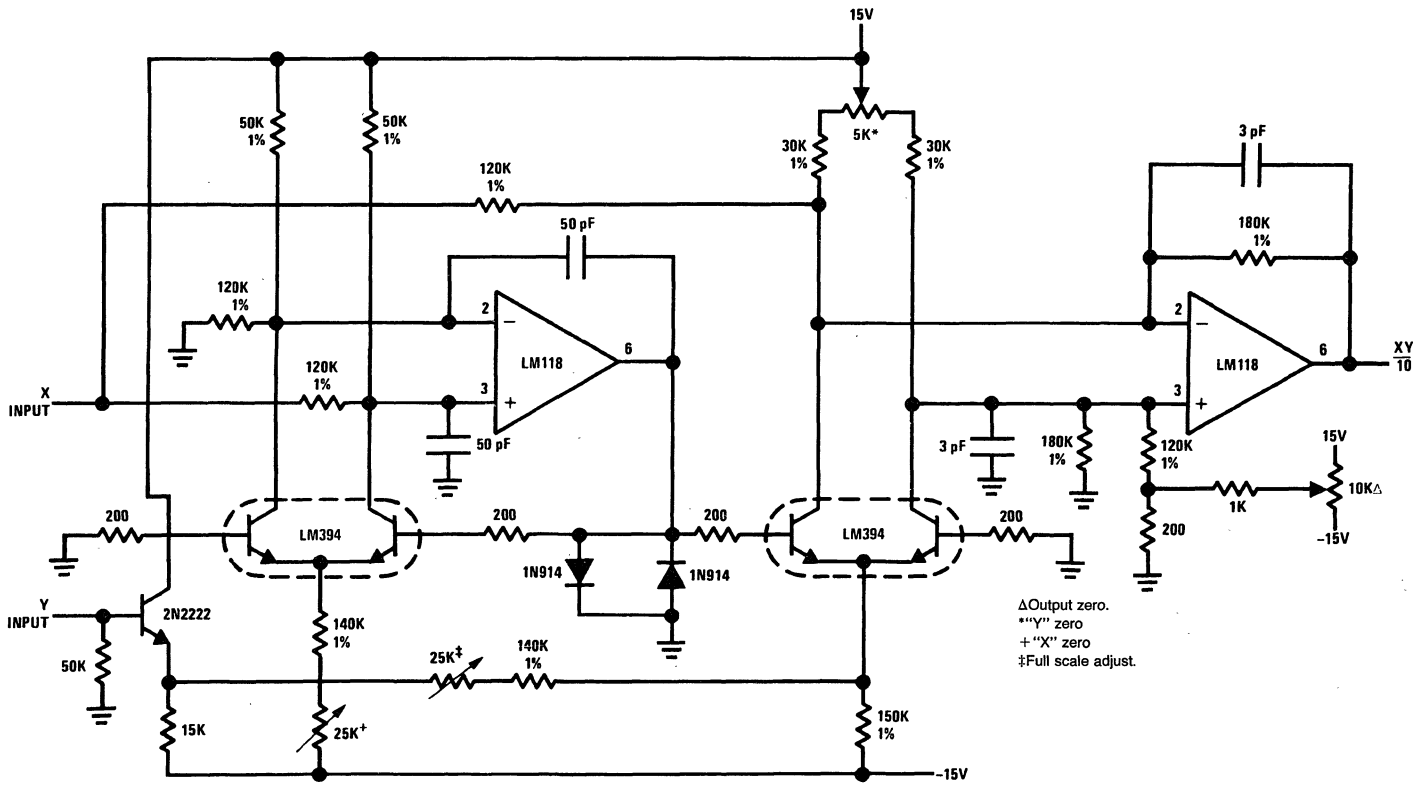


*Optional—Reduces settling time.

TL/H/7766-19

Typical Applications (Continued)

Four Quadrant Multiplier

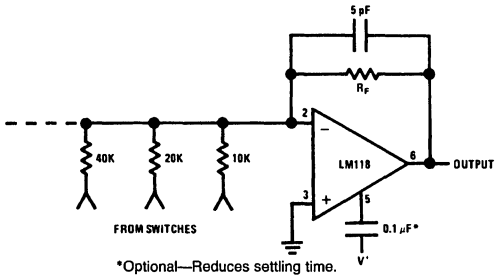


ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

TL/H/7766–17

Typical Applications (Continued)

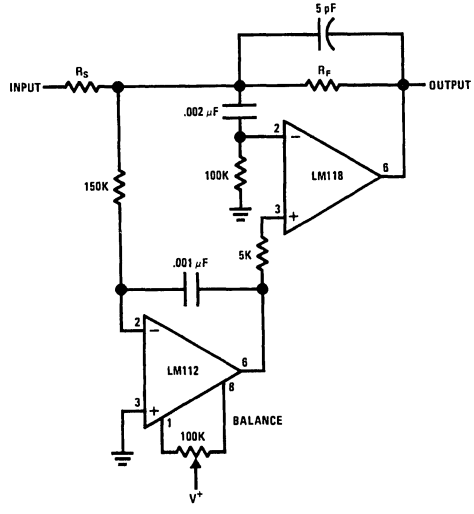
D/A Converter Using Binary Weighted Network



*Optional—Reduces settling time.

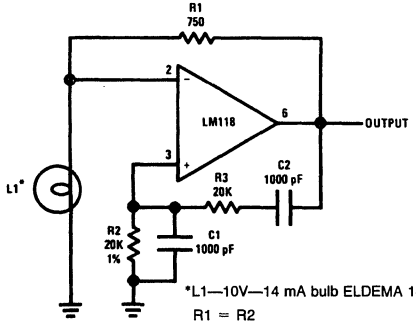
TL/H/7766–20

Fast Summing Amplifier with Low Input Current



TL/H/7766–21

Wein Bridge Sine Wave Oscillator



*L1—10V—14 mA bulb ELDEMA 1869

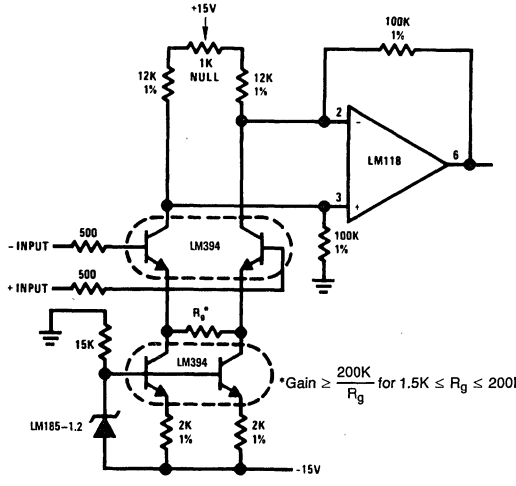
R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\,C1}$$

TL/H/7766–22

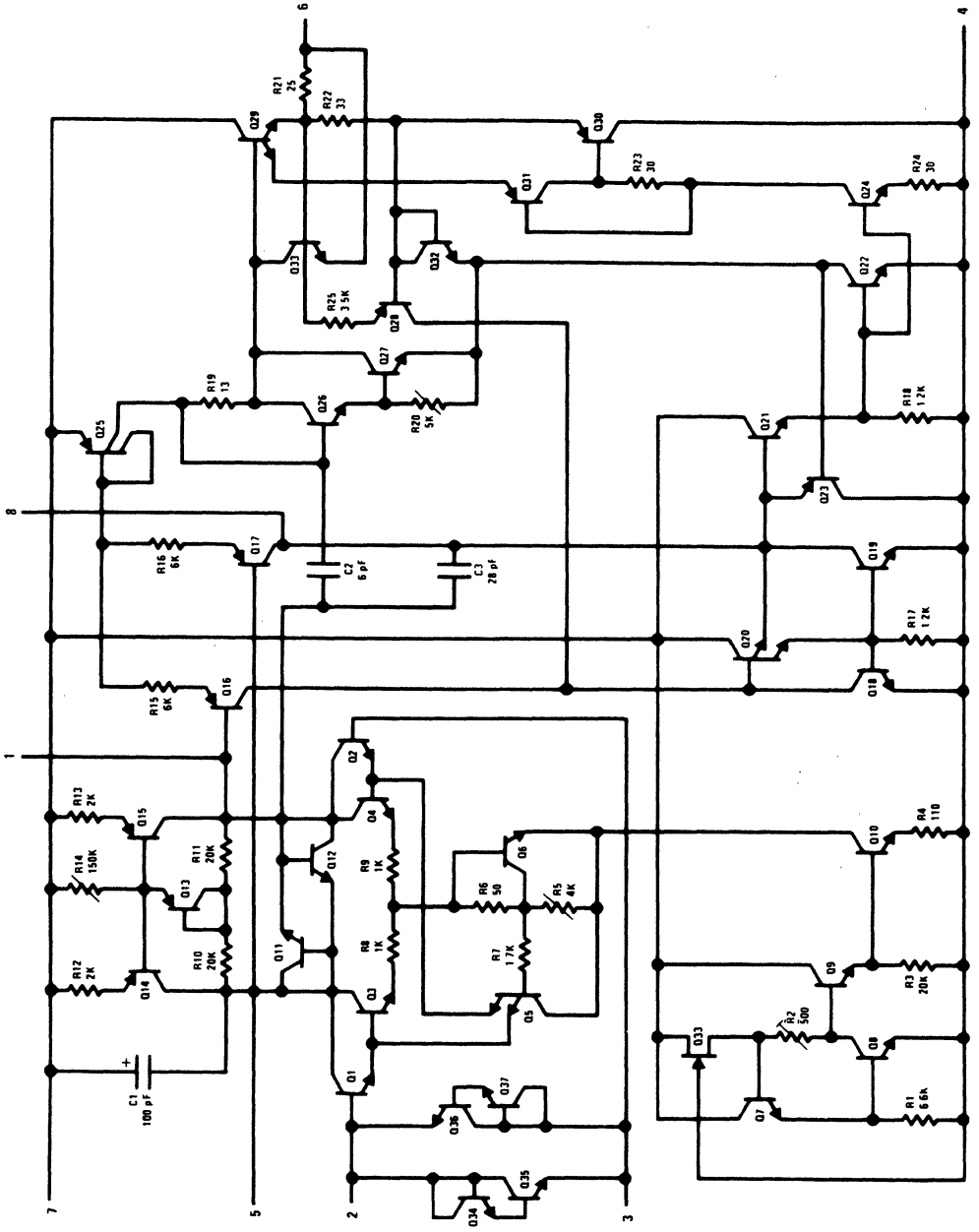
Instrumentation Amplifier



TL/H/7766–23

3

Schematic Diagram



National Semiconductor

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

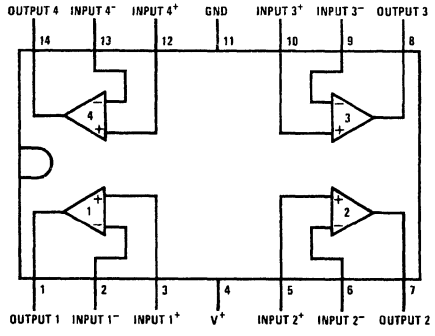
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 32 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package

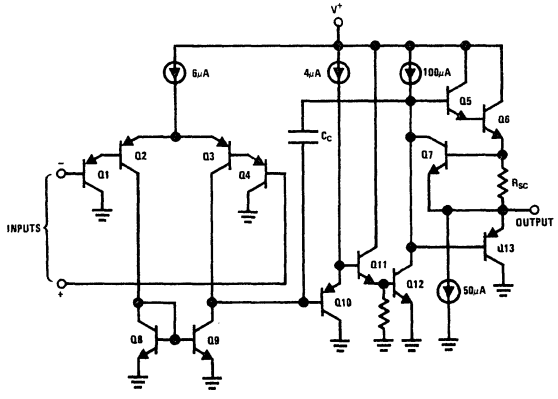


TL/H/9299–1

Top View

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N
See NS Package Number J14A, M14A or N14A

Schematic Diagram (Each Amplifier)



TL/H/9299–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A		LM224A		LM324A		LM124/LM224		LM324		LM2902		Units
		Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$	±1	±2	±1	±3	±2	±3	±2	±5	±2	±7	±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	20	50	40	80	45	100	45	150	45	250	45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	±2	±10	±2	±15	±5	±30	±3	±30	±5	±50	±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, (LM2902, $V^+ = 26\ V_{DC}$), $T_A = 25°C$	0 $V^+-1.5$		0 $V^+-1.5$		0 $V^+-1.5$		0 $V^+-1.5$		0 $V^+-1.5$		0 $V^+-1.5$		V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps													
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)	1.5	3	1.5	3	1.5	3	1.5	3	1.5	3	1.5	3	mA_{DC}
	$V^+ = 5V$	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $R_L \geq 2\ k\Omega$, ($V_O = 1\ V_{DC}$ to 11 V_{DC}), $T_A = 25°C$	50 100		50 100		25 100		50 100		25 100		25 100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$, $T_A = 25°C$	70 85		70 85		65 85		70 85		65 85		50 70		dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to 30 V_{DC} (LM2902, $V^+ = 5\ V_{DC}$ to 26 V_{DC}), $T_A = 25°C$	65 100		65 100		65 100		65 100		65 100		50 100		dB

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
	Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
		$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 200\ mV_{DC}$, $T_A = 25°C$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground		(Note 2) $V^+ = 15\ V_{DC}$, $T_A = 25°C$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage		(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift		$R_S = 0\Omega$		±7	±20		±7	±20		±7	±30		±7			±7			±7		$\mu V/°C$
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±30			±30			±75			±100			±150		±45	±200	nA$_{DC}$
Input Offset Current Drift		$R_S = 0\Omega$		±10	±200		±10	±200		±10	±200		±10			±10			±10		$pA_{DC}/°C$
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA$_{DC}$
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30\ V_{DC}$ (LM2902, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain		$V^+ = +15\ V_{DC}$ (V_O Swing = 1 V_{DC} to 11 V_{DC}) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
		$R_L \geq 10\ k\Omega$ (LM2902, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
	V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2\ V_{DC}$	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	Sink		$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications are limited to $-55°C \le T_A \le +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \le T_A \le +70°C$, and the LM2902 specifications are limited to $-40°C \le T_A \le +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$) at 25°C; for LM2902, V^+ from 5 V_{DC} to 26 V_{DC}.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902), independent of the magnitude of V^+.

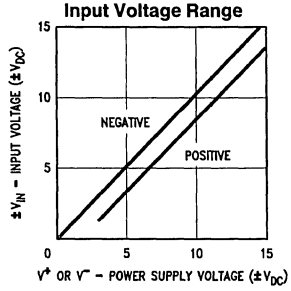
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

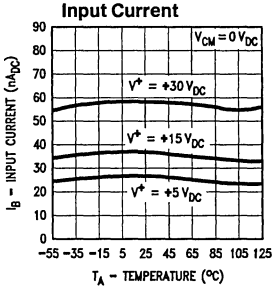
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

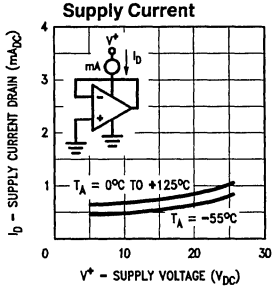
Input Voltage Range



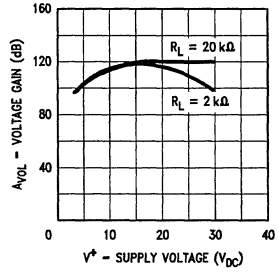
Input Current



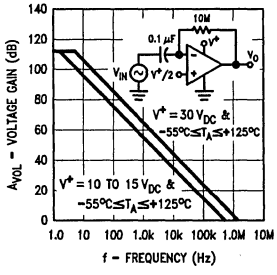
Supply Current



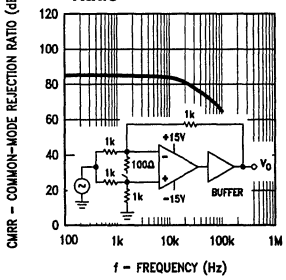
Voltage Gain



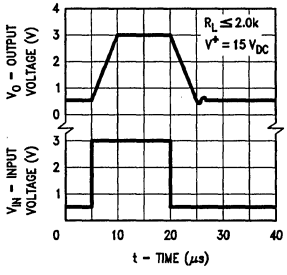
Open Loop Frequency Response



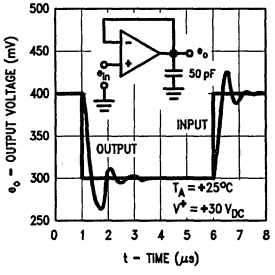
Common Mode Rejection Ratio



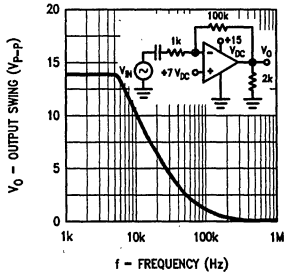
Voltage Follower Pulse Response



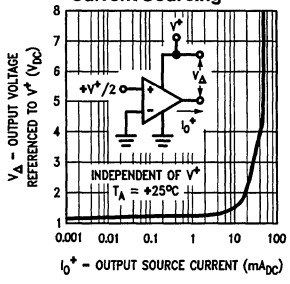
Voltage Follower Pulse Response (Small Signal)



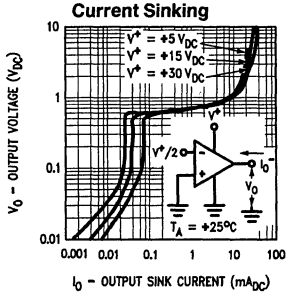
Large Signal Frequency Response



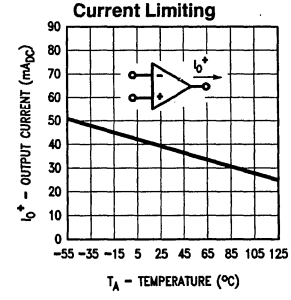
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



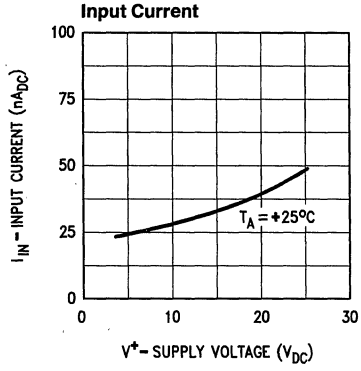
Current Limiting

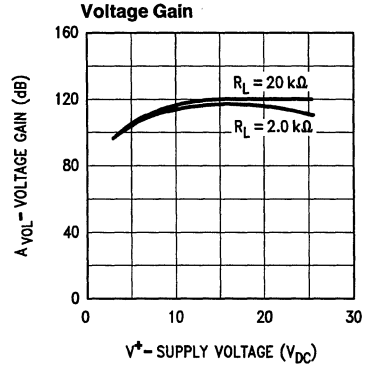


TL/H/9299–3

3

Typical Performance Characteristics (LM2902 only)





TL/H/9299–4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

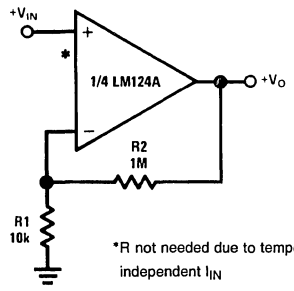
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

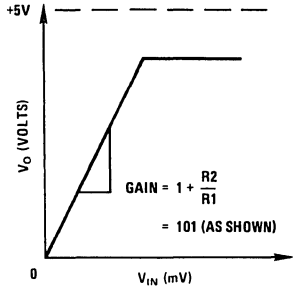
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

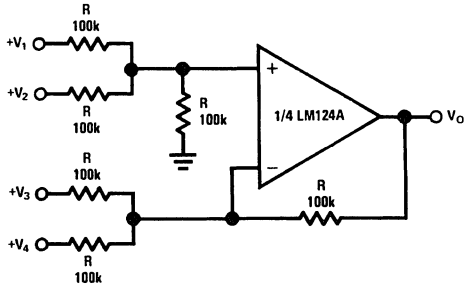
Non-Inverting DC Gain (0V Input = 0V Output)





TL/H/9299–5

DC Summing Amplifier
($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



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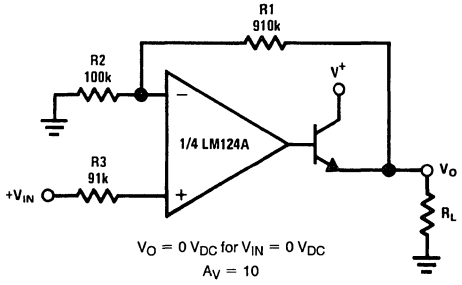
Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

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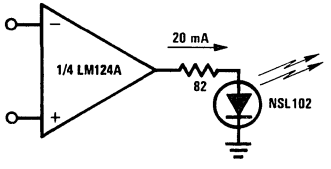
LED Driver



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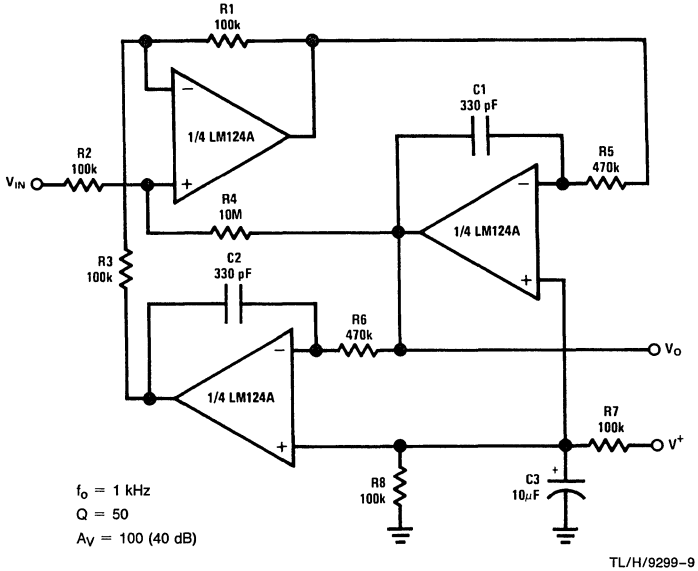
"BI-QUAD" RC Active Bandpass Filter



$f_o = 1$ kHz
$Q = 50$
$A_V = 100$ (40 dB)

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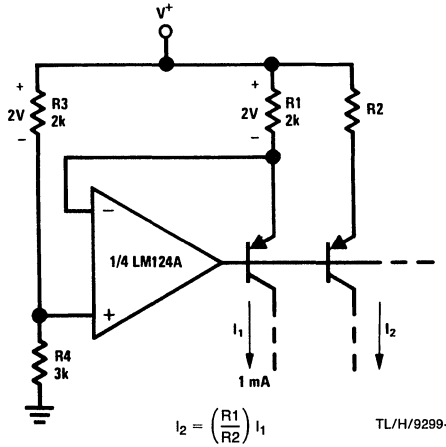
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

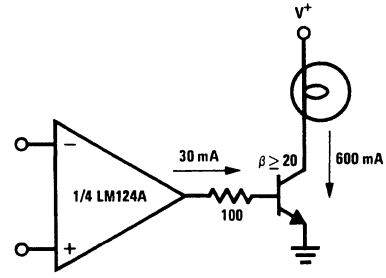
Fixed Current Sources



$I_2 = \left(\frac{R1}{R2}\right) I_1$

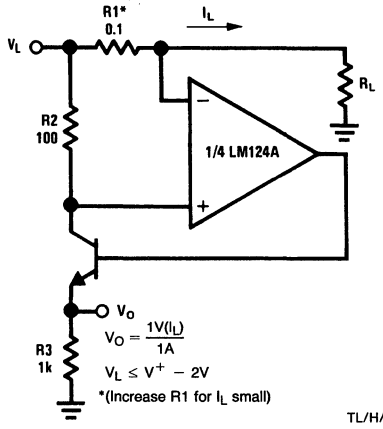
TL/H/9299–10

Lamp Driver



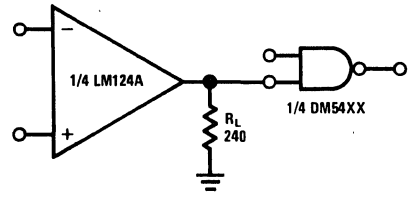
TL/H/9299–11

Current Monitor



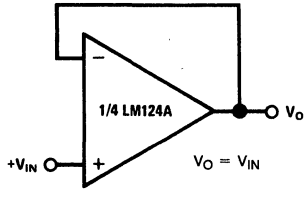
TL/H/9299–12

Driving TTL



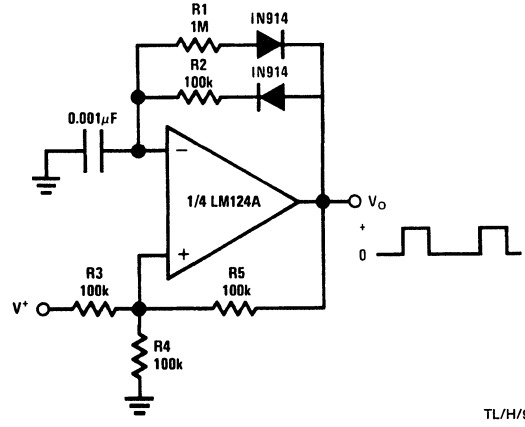
TL/H/9299–13

Voltage Follower



TL/H/9299–14

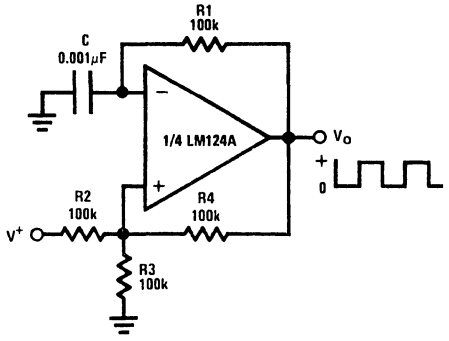
Pulse Generator



TL/H/9299–15

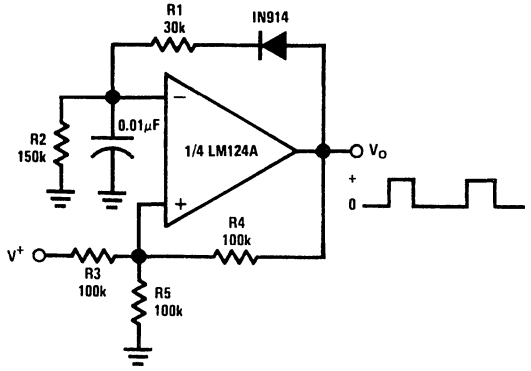
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



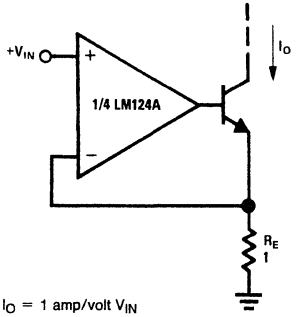
TL/H/9299–16

Pulse Generator



TL/H/9299–17

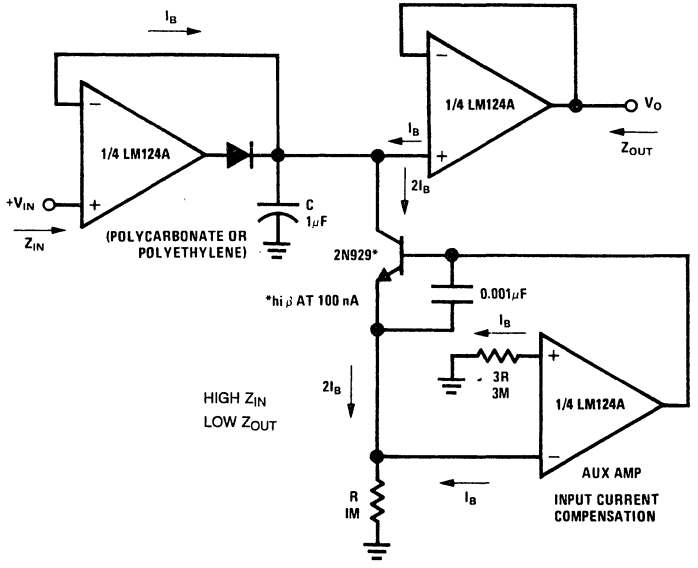
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

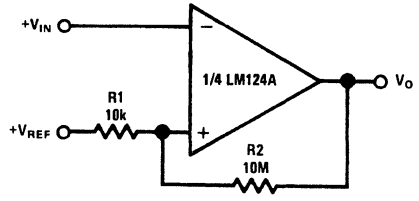
TL/H/9299–18

Low Drift Peak Detector



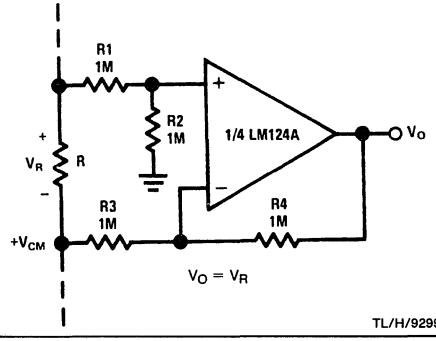
TL/H/9299–19

Comparator with Hysteresis



TL/H/9299–20

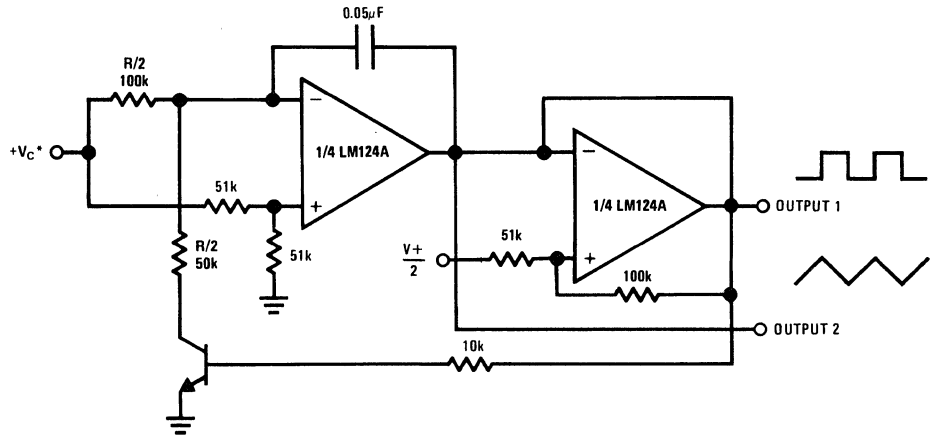
Ground Referencing a Differential Input Signal



TL/H/9299–21

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

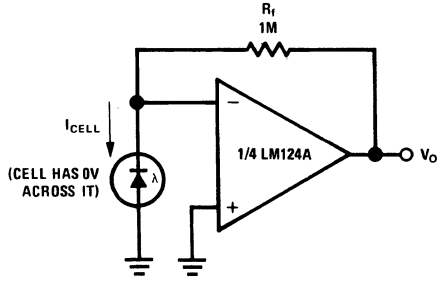
Voltage Controlled Oscillator Circuit



TL/H/9299–22

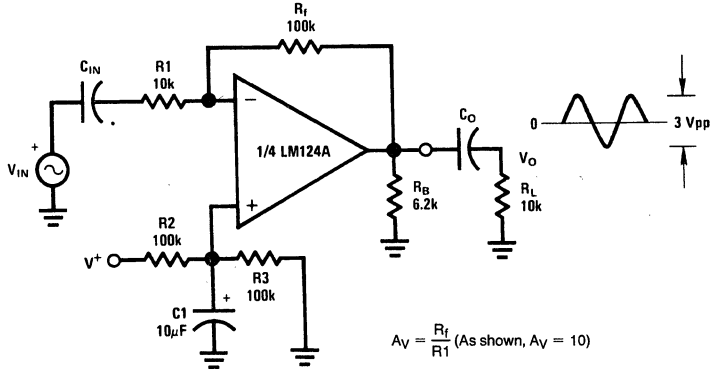
*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2\,(V^+ - 1.5\,V_{DC})$

Photo Voltaic-Cell Amplifier



TL/H/9299–23

AC Coupled Inverting Amplifier

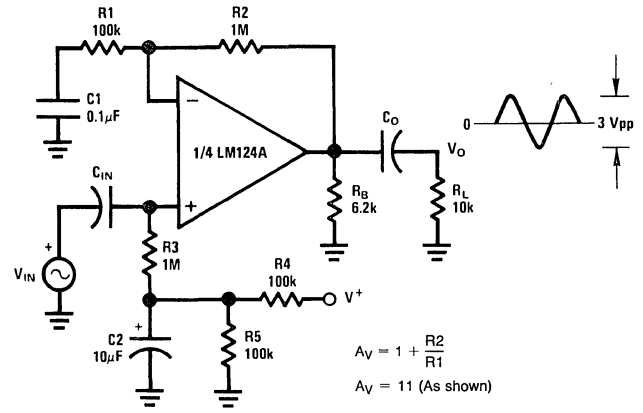


$A_V = \frac{R_f}{R1}$ (As shown, A_V = 10)

TL/H/9299–24

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

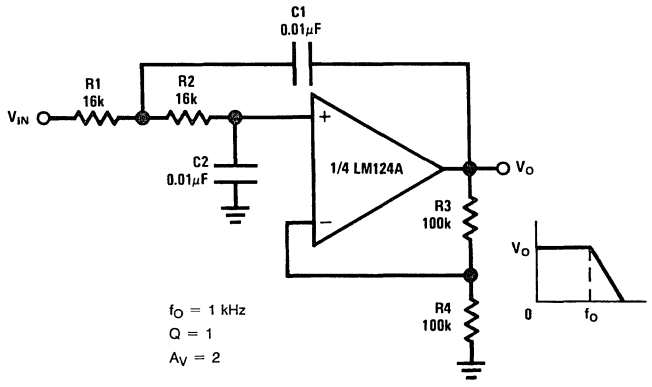


$A_V = 1 + \frac{R2}{R1}$

A_V = 11 (As shown)

TL/H/9299–25

DC Coupled Low-Pass RC Active Filter



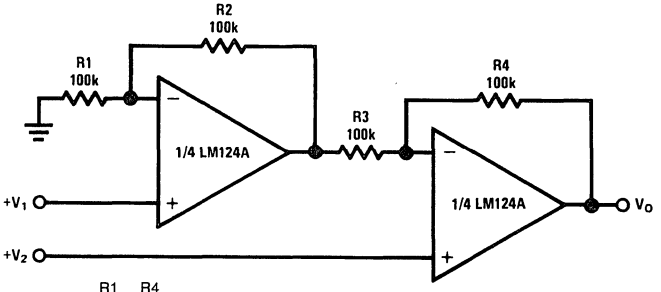
f_O = 1 kHz

Q = 1

A_V = 2

TL/H/9299–26

High Input Z, DC Differential Amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

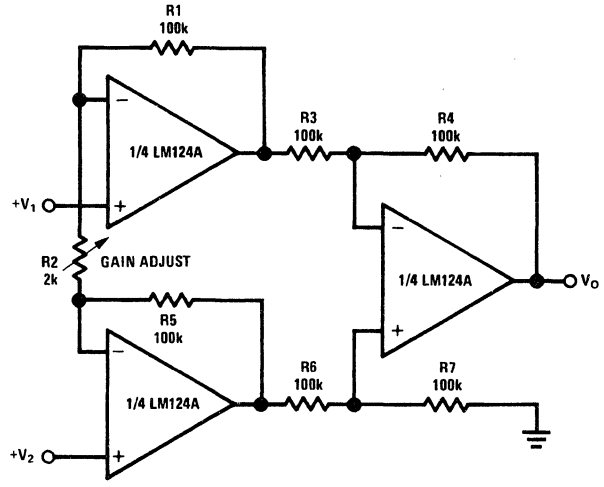
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

TL/H/9299–27

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier



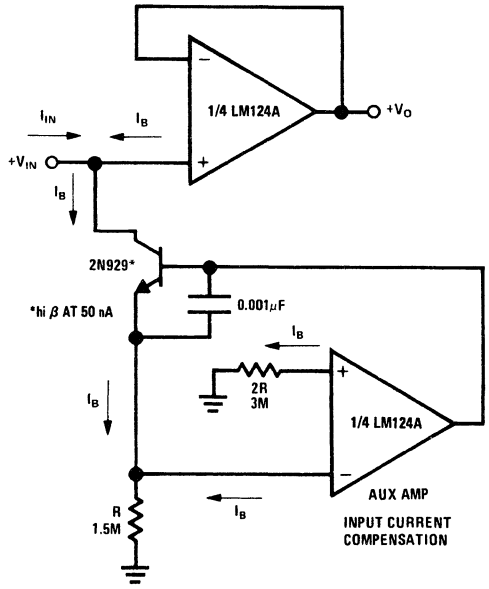
TL/H/9299–28

If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

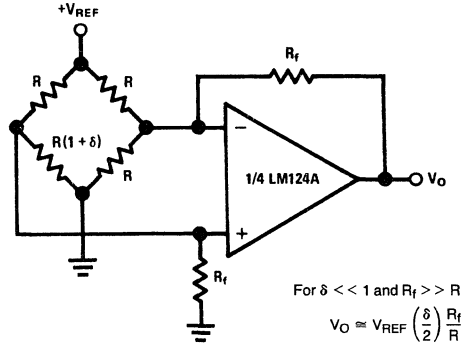
As shown $V_O = 101\,(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/9299–29

Bridge Current Amplifier



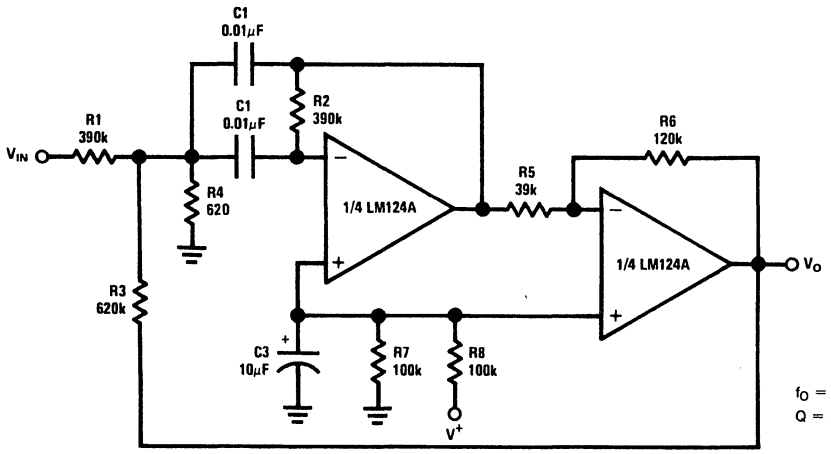
For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299–30

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Bandpass Active Filter



TL/H/9299–31

National Semiconductor

LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

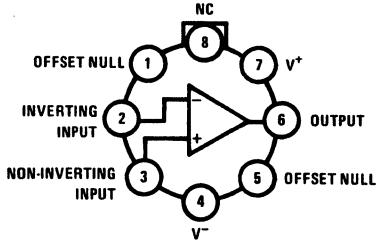
- Wide supply voltage range ±4.0V to ±40V
- Large output voltage swing ±37V
- Wide input common-mode range ±38V
- Input overvoltage protection Full ±40V
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 8.0 nA
- Low input offset current 1.0 nA
- High slew rate—essentially independent of temperature and supply voltage 2.5V/μs
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagram

Metal Can Package
Top View



TL/H/7783–1

Order Number LM143H or LM343H
See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 sec.)	300°C	300°C
ESD rating to be determined.		

Electrical Characteristics (Note 3)

Parameter	Conditions	LM143			LM343			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	±24	±26		±22	±26		V
Supply Current (Note 5)	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$		2.5			2.5		V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\ V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤ 1%		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max T_A = Min			6.0 6.0			10 10	mV
Input Offset Current	T_A = Max T_A = Min		0.8 1.8	4.5 7.0		0.8 1.8	14 14	nA
Input Bias Current	T_A = Max T_A = Min		5.0 16	35 35		5.0 16	55 55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max $R_L \geq 100\ k\Omega$, T_A = Min	50k 50k	150k 220k		50k 50k	150k 220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max $R_L \geq 5.0\ k\Omega$, T_A = Min	22 22	26 25		20 20	26 25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 155°C/W, junction to ambient, or 20°C/W, junction to case.

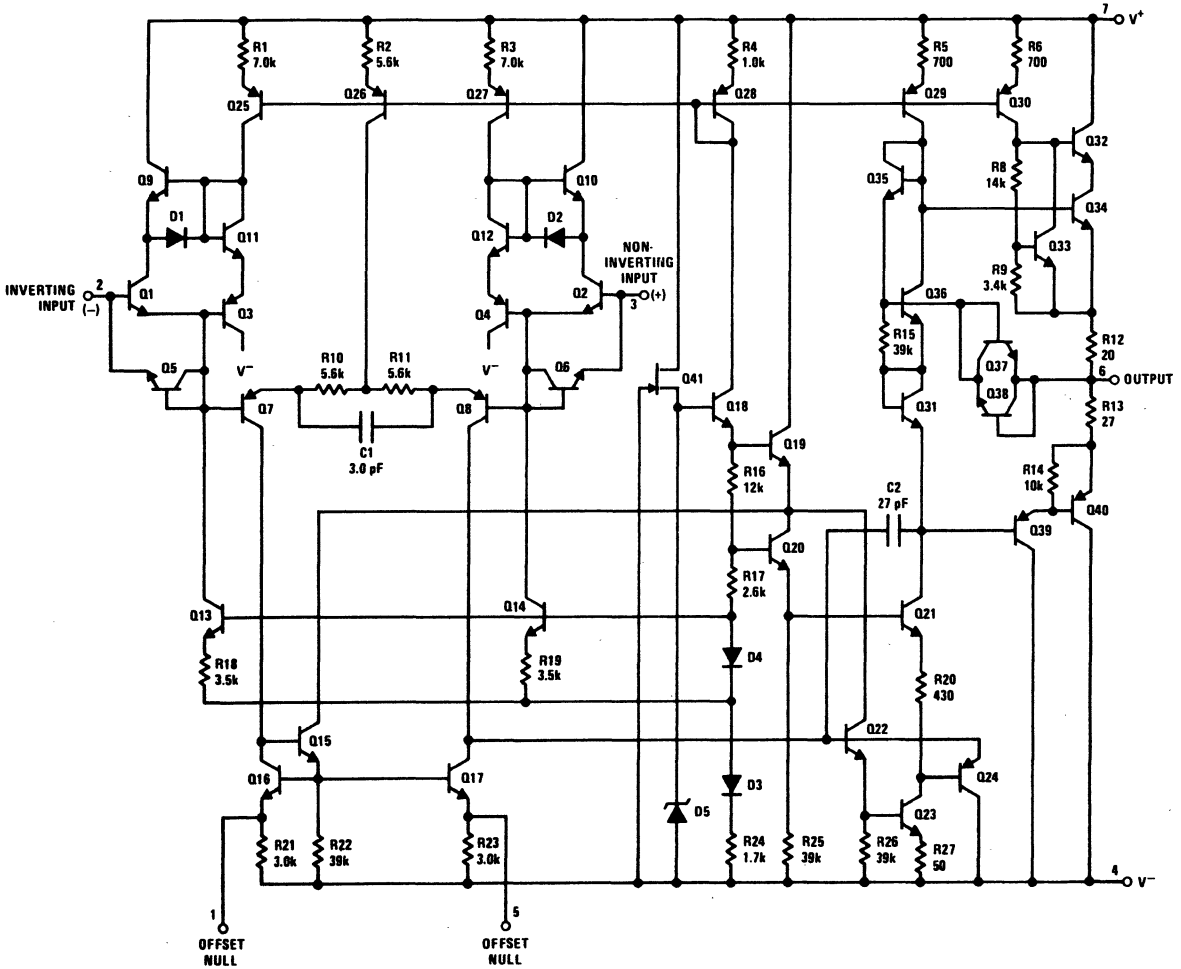
Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 28V$. For LM143, T_A = max = 125°C and T_A = min = −55°C. For LM343, T_A = max = 70°C and T_A = min = 0°C.

Note 4: Refer to RETS143X for LM143H and LM1536H military specifications.

Note 5: The maximum supply currents are guaranteed at $V_S = \pm 40V$ for the LM143 and $V_S = \pm 34V$ for the LM343.

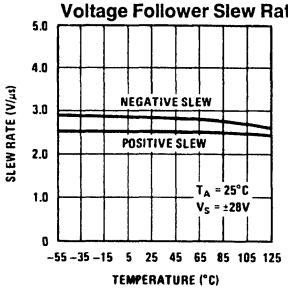
Schematic Diagram



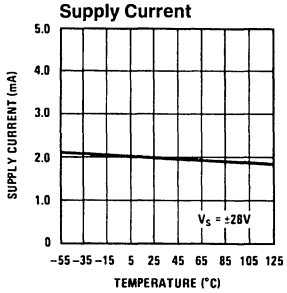
TL/H/7783–2

Typical Performance Characteristics

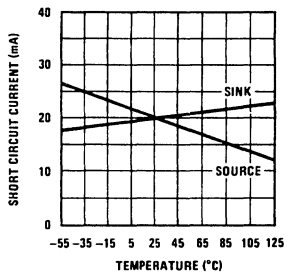
Voltage Follower Slew Rate



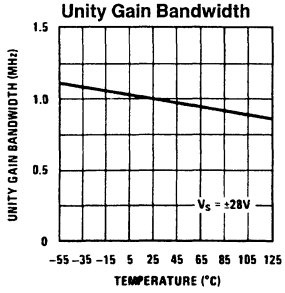
Supply Current



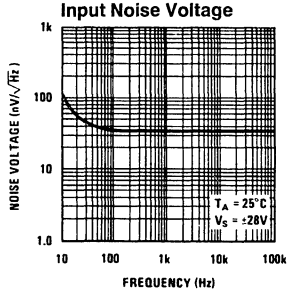
Short Circuit Current



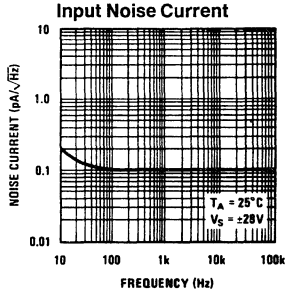
Unity Gain Bandwidth



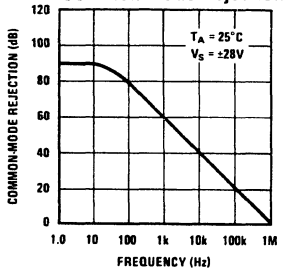
Input Noise Voltage



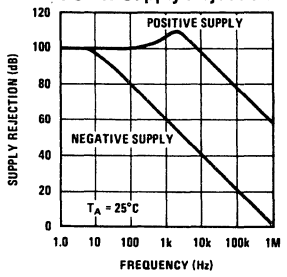
Input Noise Current



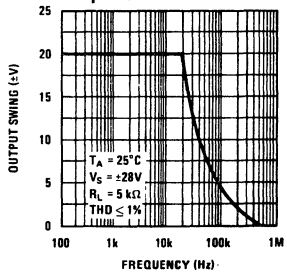
Common-Mode Rejection



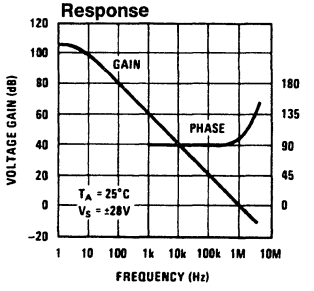
Power Supply Rejection



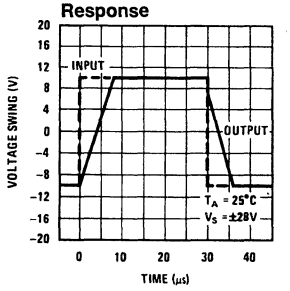
Large Signal Frequency Response



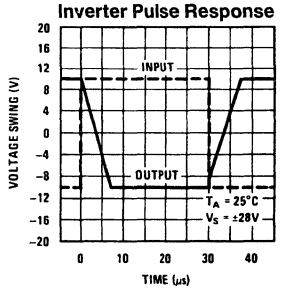
Open Loop Frequency Response



Voltage Follower Pulse Response

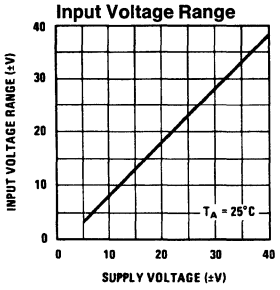


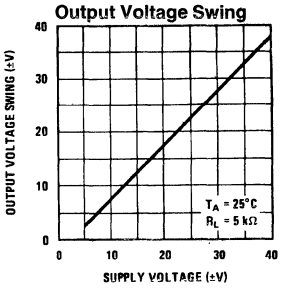
Inverter Pulse Response

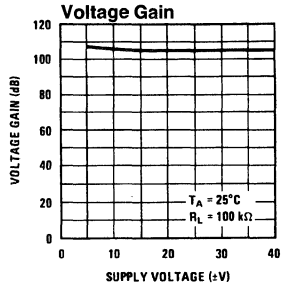


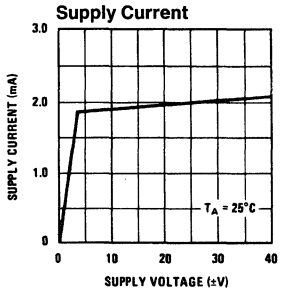
TL/H/7783–4

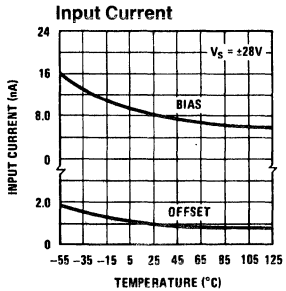
Typical Performance Characteristics (Continued)

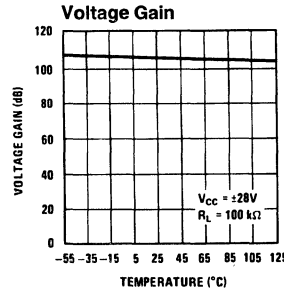












TL/H/7783–3

Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

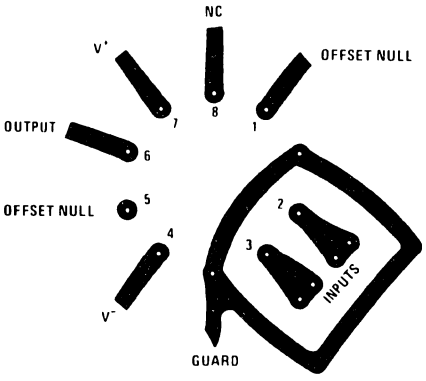
Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3* and *4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage abilities of the LM143.

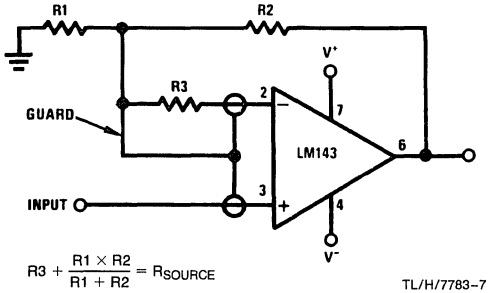
Application Hints (See AN-127) (Continued)



TL/H/7783–5

Bottom View

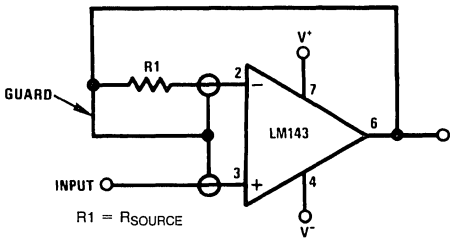
FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package



$$R3 + \frac{R1 \times R2}{R1 + R2} = R_{SOURCE}$$

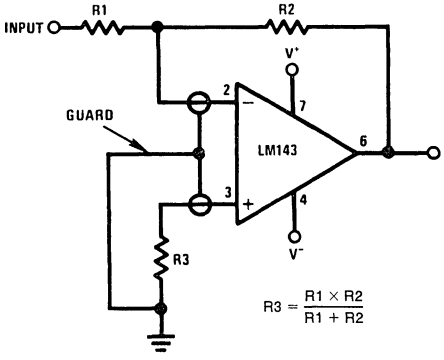
TL/H/7783–7

FIGURE 3. Guarded Non-Inverting Amplifier



TL/H/7783–6

FIGURE 2. Guarded Voltage Follower

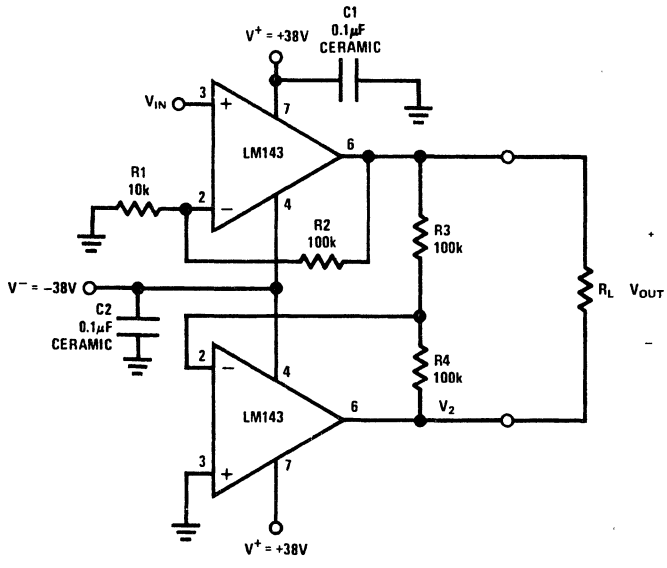


TL/H/7783–8

FIGURE 4. Guarded Inverting Amplifier

Typical Applications ‡ (For more detail see AN-127)

130 V_{p-p} Drive Across a Floating Load



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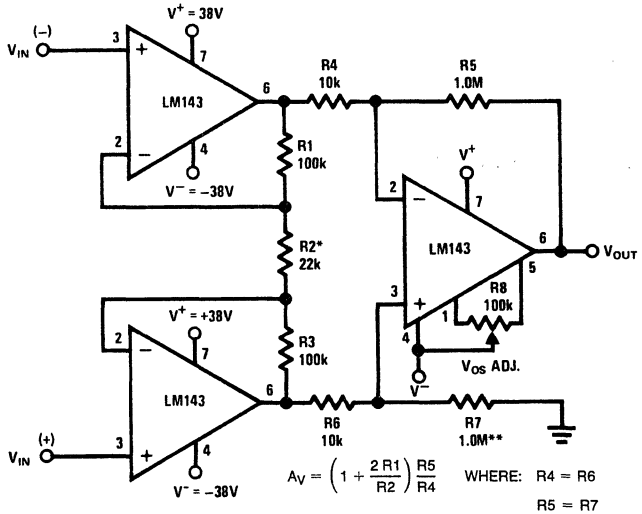
±34V Common-Mode Instrumentation Amplifier



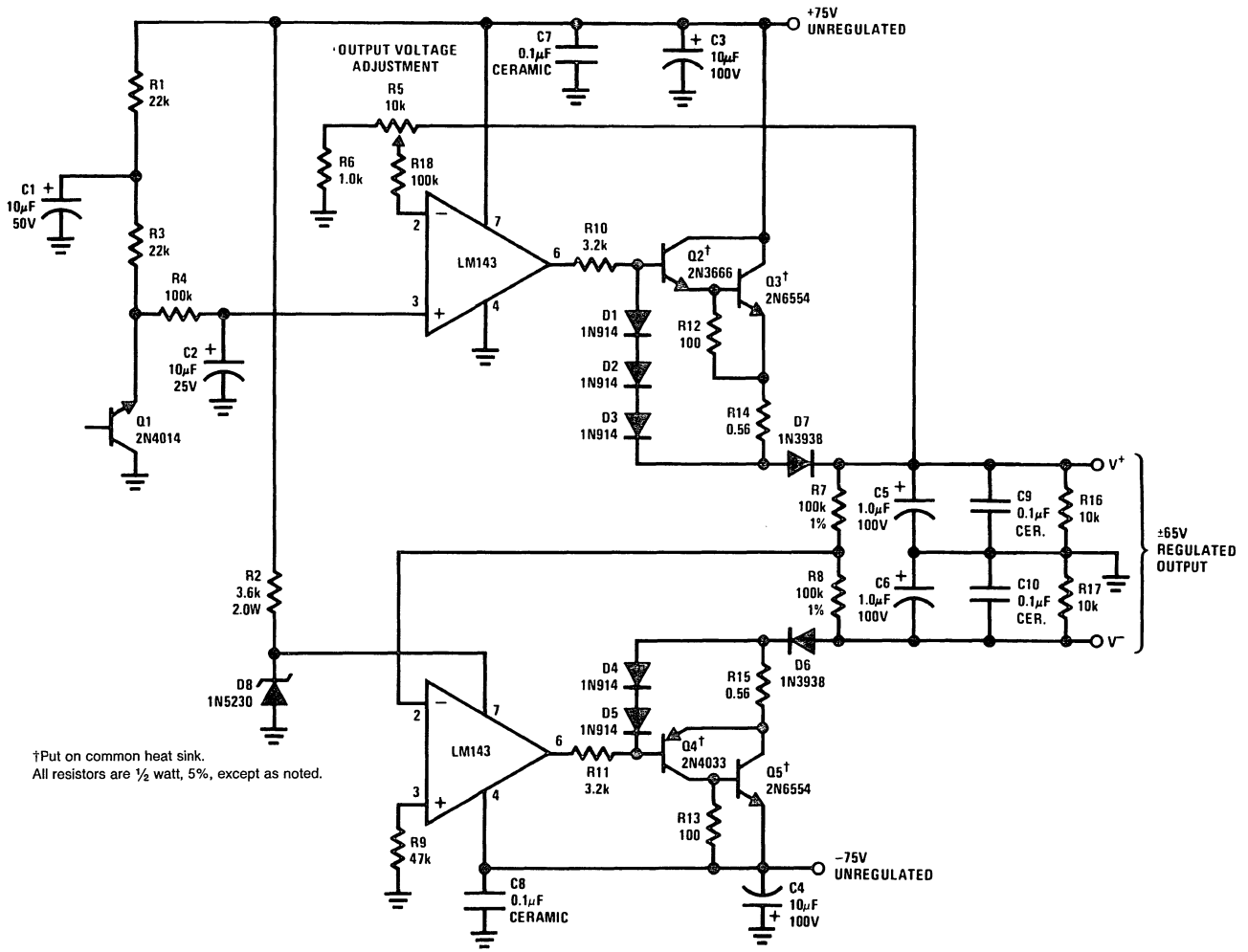
TL/H/7783–10

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection



†Put on common heat sink.
All resistors are ½ watt, 5%, except as noted.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

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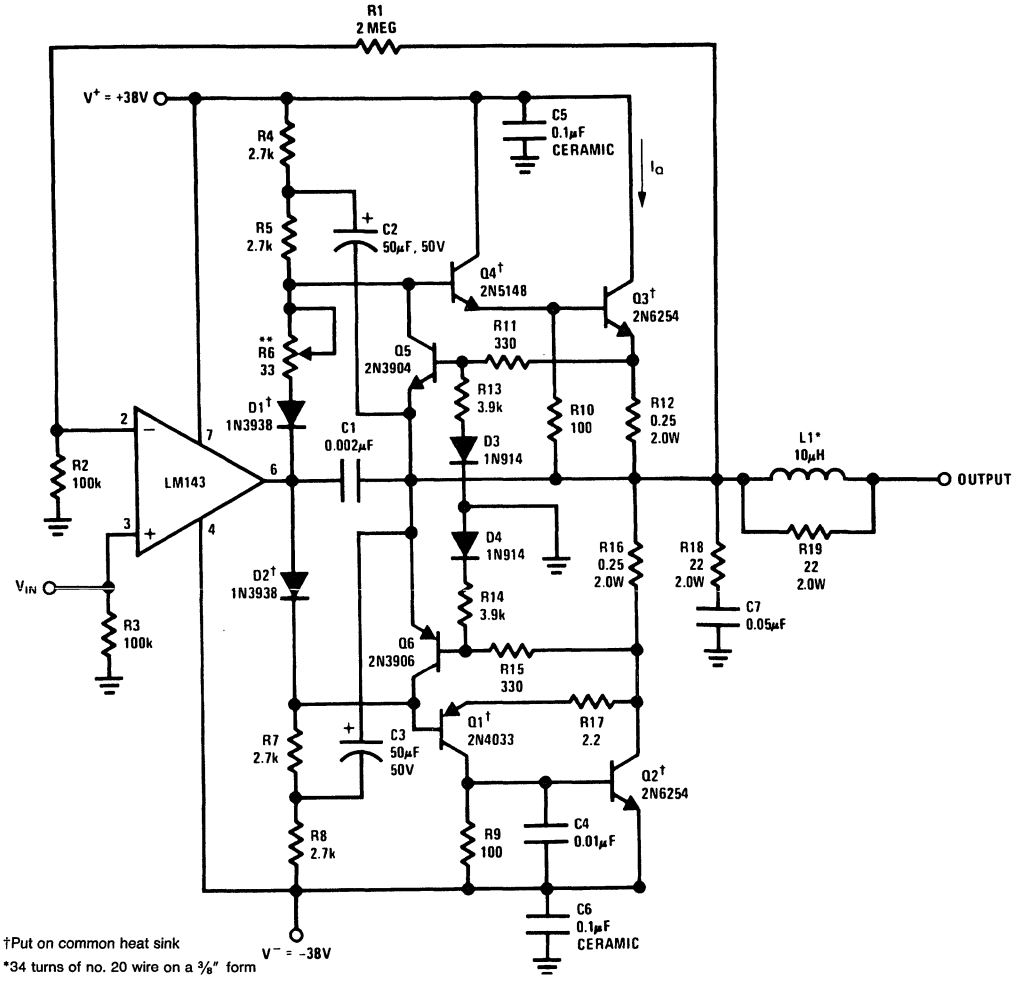
Typical Applications ‡ (Continued) (For more detail see AN-127)

90W Audio Power Amplifier with Safe Area Protection



†Put on common heat sink

*34 turns of no. 20 wire on a ⅜" form

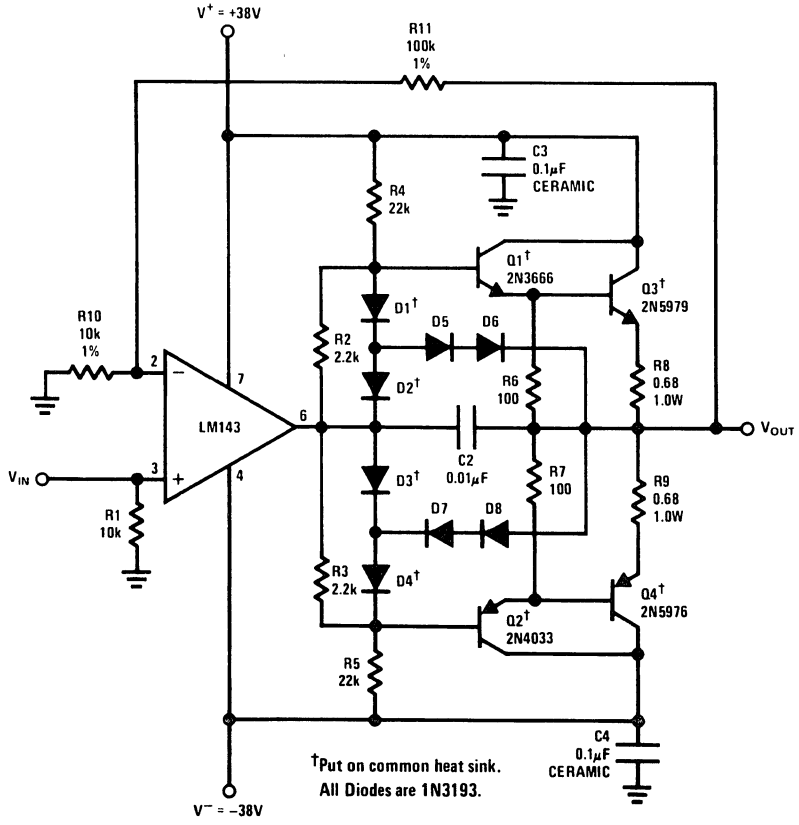
**Adjust R6 to set I_Q = 100 mA

TL/H/7783–12

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Typical Applications ‡ (Continued) (For more detail see AN-127)

1 Amp Power Amplifier with Short Circuit Protection



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‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

National Semiconductor

LM144/LM344 High Voltage, High Slew Rate Operational Amplifier

General Description

The LM144 is a general purpose high voltage, uncompensated operational amplifier featuring operation to ±36V, complete input overvoltage protection up to the supply voltages and input currents comparable to those of other super-β op amps. Increased slew rate, together with high common-mode and supply rejection, insure excellent performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, due to thermal symmetry on the die, gain is unaffected by output loading at high supply voltages.

With the unique advantages of low input current, high gain, and high slew rate, the LM144 can increase accuracy and useful frequency range in many existing applications. For example, the LM144 is a plug-in replacement for the LM101A, as well as other general purpose op amps.

The LM144 can be compensated with a single capacitor, thus giving the user the ability to optimize ac parameters to suit the application. For example, in applications such as audio power amplifiers, the LM144 with a gain of 10 can provide a ±30V output swing, a slew rate of approximately 30V/μs, and a 120 kHz full power bandwidth. In applications where capacitive loads or cables must be driven, the LM144 can be overcompensated for increased stability.

The LM344 is similar to the LM144 for applications in less severe supply voltage and temperature environments.

Features

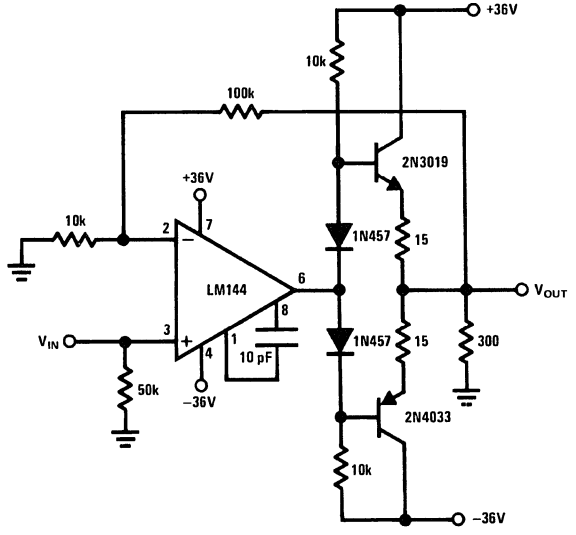
- External compensation provides large power bandwidth ($A_V \geq 10$) — 120 kHz
- Wide operating voltage range — ±4.0V to ±36V
- Large output voltage swing — ±30V
- Wide input common-mode range
- Input overvoltage protection
- Electrical characteristics independent of supply voltage and temperature

Unique Characteristics

- Low input bias current — 8.0 nA
- Low input offset current — 1.0 nA
- High slew rate ($A_V \geq 10$) — 30V/μs
- High voltage gain — 100k min
- Offset voltage null capability

Typical Application

Large Power Bandwidth, Current Boosted Audio Line Driver



TL/H/7784–1

Absolute Maximum Ratings (These ratings are not concurrent)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM144	LM344
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 sec)	300°C	300°C

ESD rating to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM144			LM344			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	24	26		22	26		V
Supply Current	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$ $T_A = 25°C$, $A_V = 10$, C1 = 3 pF		2.5 30			2.5 30		V/μs V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\ V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤ 1%, $A_V = 1$		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max T_A = Min			6.0 6.0			10 10	mV mV
Input Offset Current	T_A = Max T_A = Min		0.8 1.8	4.5 7.0		0.8 1.8	14 14	nA nA
Input Bias Current	T_A = Max T_A = Min		5.0 16	35 35		5.0 16	55 55	nA nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max $R_L \geq 100\ k\Omega$, T_A = Min	50k 50k	150k 220k		50k 50k	150k 220k		V/V V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max $R_L \geq 5.0\ k\Omega$, T_A = Min	22 22	26 25		20 20	26 25		V V

Note 1: The maximum junction temperature of the LM144 is 150°C, while that of the LM344 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 20°C/W, junction to case.

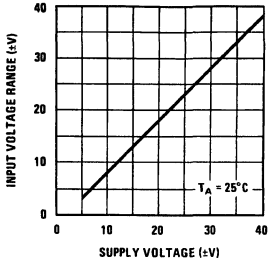
Note 2: For supply voltage less than ±40V for the LM144 and less than ±34V for the LM344, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 28V$. For the LM144, T_A = max = 125°C and T_A = min = −55°C. For the LM344, T_A = max = 70°C and T_A = min = 0°C.

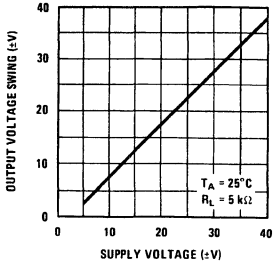
Note 4: Refer to RETS144X for LM144H specifications.

Typical Performance Characteristics

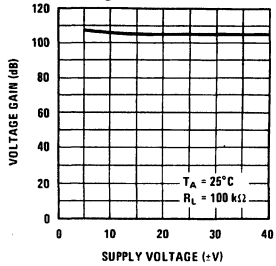
Input Voltage Range



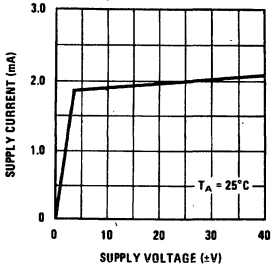
Output Voltage Swing



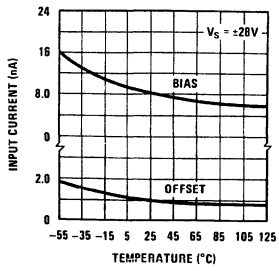
Voltage Gain



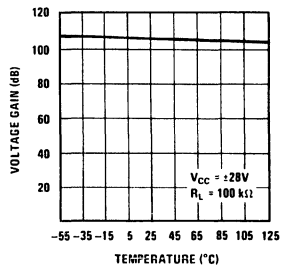
Supply Current



Input Current



Voltage Gain



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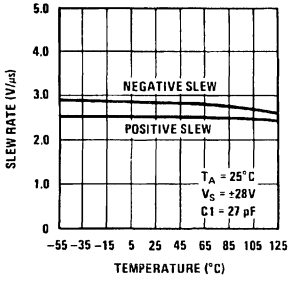
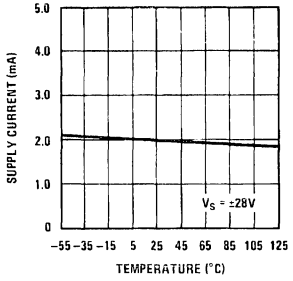
Typical Performance Characteristics (Continued)

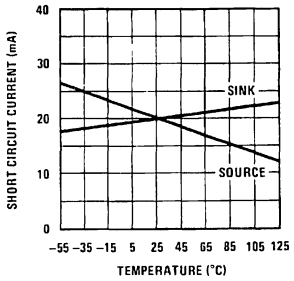
Voltage Follower Slew Rate



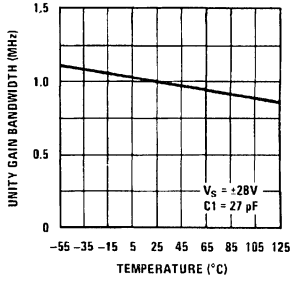
Supply Current



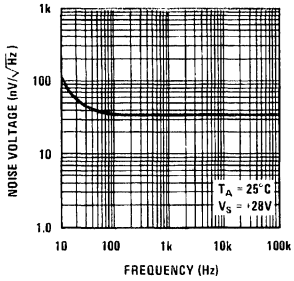
Short Circuit Current



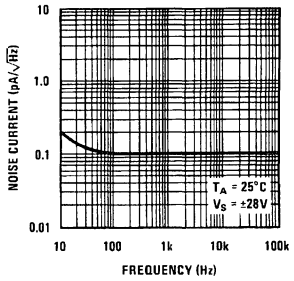
Unity Gain Bandwidth



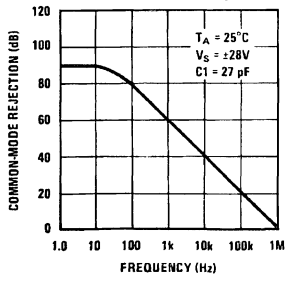
Input Noise Voltage



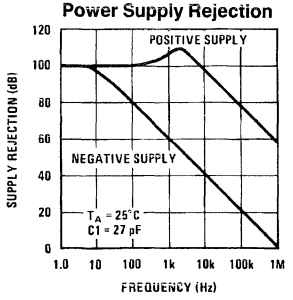
Input Noise Current



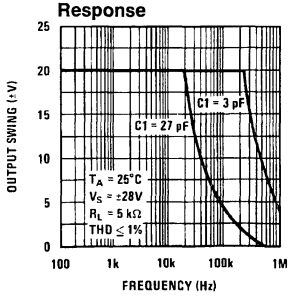
Common-Mode Rejection



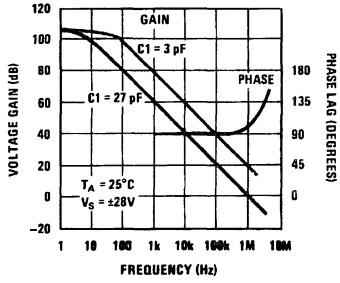
Power Supply Rejection



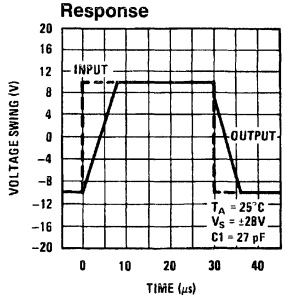
Large Signal Frequency Response



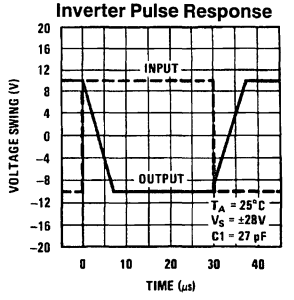
Open Loop Frequency Response



Voltage Follower Pulse Response



Inverter Pulse Response



TL/H/7784–4

Application Hints (See Also AN-127)

The LM144 is designed for trouble-free operation at any supply voltage up to a maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM144 remains virtually blow-out proof.

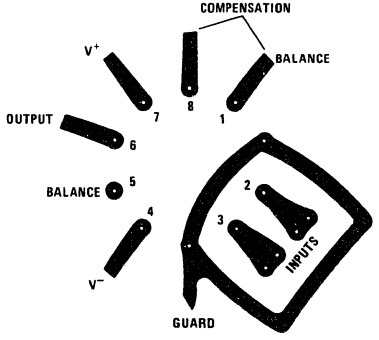
Although output short circuits to ground or either supply can be sustained indefinitely for supply voltages, below ±18V, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM144 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltge pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads. See *Figures 5, 6 and 7.*

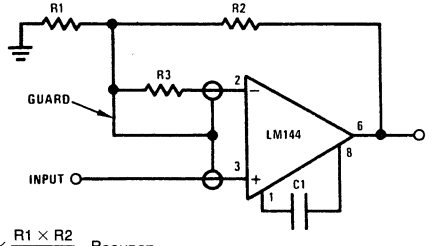
Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.



TL/H/7784–5

Bottom View

FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package



$R3 \times \frac{R1 \times R2}{R1 + R2}$ R_{SOURCE}

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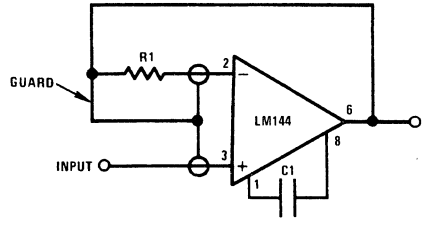
FIGURE 3. Guarded Non-Inverting Amplifier



$R1 = R_{SOURCE}$

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FIGURE 2. Guarded Voltage Follower

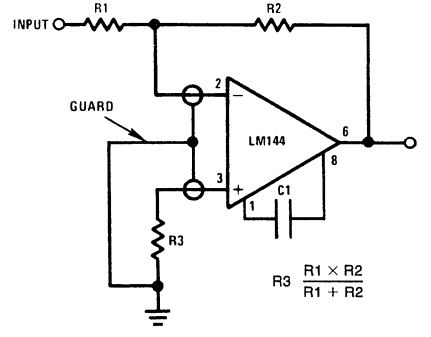

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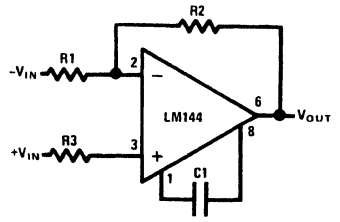
FIGURE 4. Guarded Inverting Amplifier

Application Hints (Continued)



$$C1 = \frac{R1\,C_C}{R1 + R2} \quad \text{NON-INVERTING}$$

$$C1 = \frac{R1\,C_C}{R2} \quad \text{INVERTING}$$

$C_C = 27\ PF$

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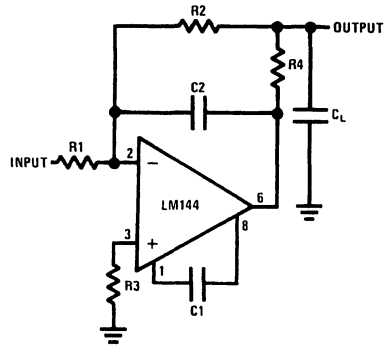
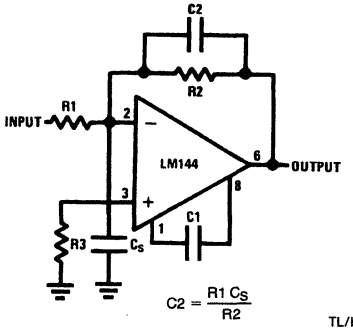
FIGURE 5. Single Pole Compensation



TL/H/7784–10

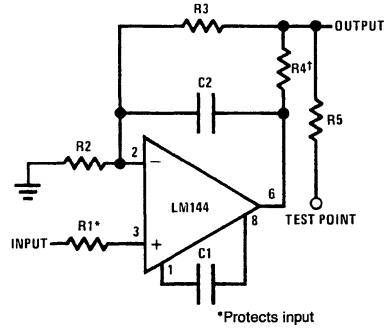
FIGURE 6. Isolating Large Capacitive Loads



$$C2 = \frac{R1\,C_S}{R2}$$

TL/H/7784–11

FIGURE 7. Compensating For Stray Input Capacitances or Large Feedback Resistor



*Protects input
†Protects output
∴Protects output—not needed when R4 is used

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FIGURE 8. Protecting Against Gross Fault Conditions

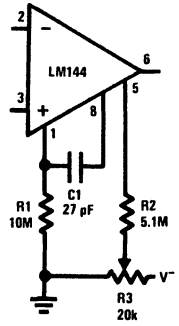

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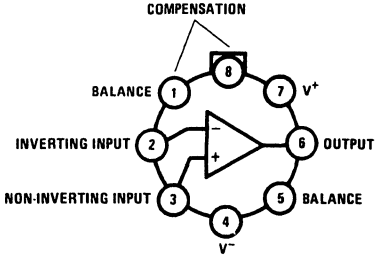
FIGURE 9. Balancing Circuit

Connection Diagram

Metal Can Package



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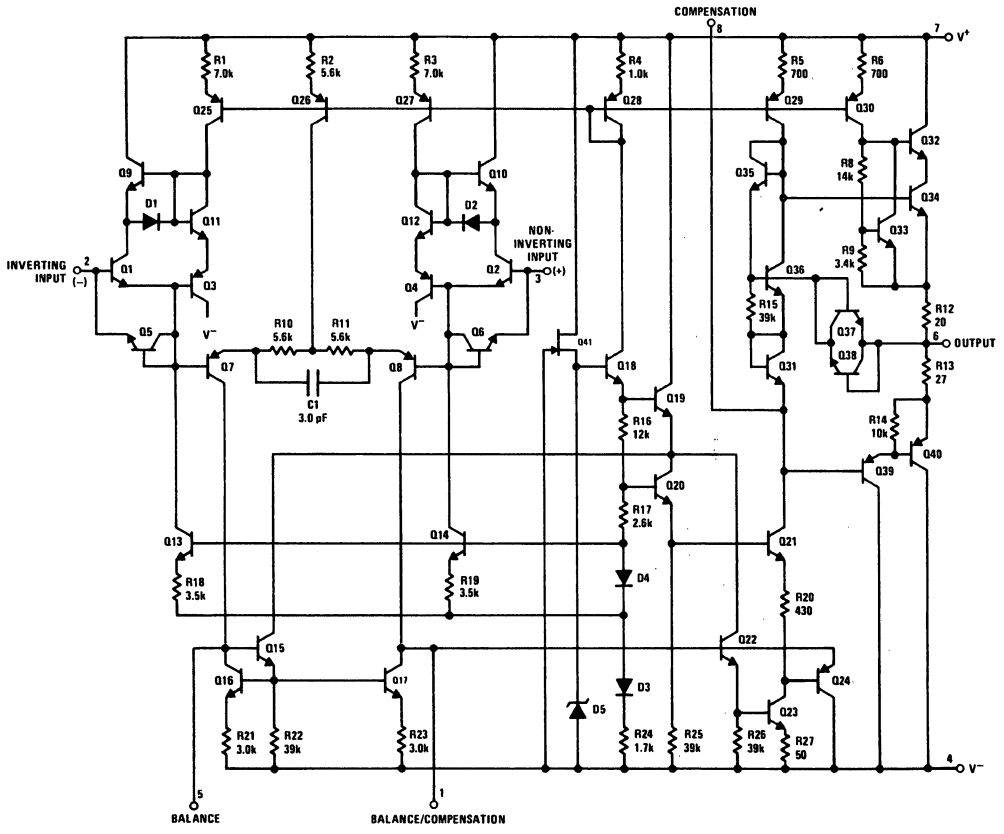
Top View

Pin 4 is connected to case

Order Number LM144H or LM344H
See NS Package Number H08C

Schematic Diagram



TL/H/7784–2

National Semiconductor

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

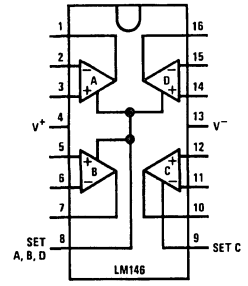
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA/amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagram (Dual-In-Line Package, Top View)



TL/H/5654–1

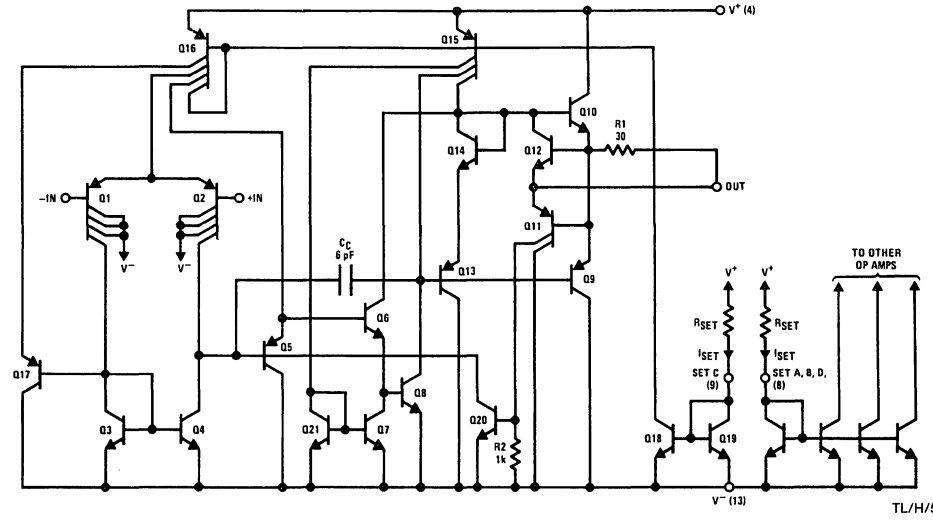
Order Number LM146J, LM246J, LM346J, LM346M or LM346N
See NS Package Number J16A, M16A or N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4/μs (I_{SET}/10 μA)
Input Bias Current ≈ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 5)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C	260°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (J) Pd	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Small Outline (M) θ_{jA}			115°C/W
Molded DIP (N) Pd			500 mW
θ_{jA}			90°C/W
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	+260°C	+260°C	+260°C
Small Outline Package			
Vapor Phase (60 seconds)	+215°C	+215°C	+215°C
Infrared (15 seconds)	+220°C	+220°C	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	6	mV
Input Offset Current	$V_{CM} = 0V$, $T_A = 25°C$		2	20		2	100	nA
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		50	100		50	250	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$, $T_A = 25°C$	100	1000		50	1000		V/mV
Input CM Range	$T_A = 25°C$	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10\ k\Omega$, $T_A = 25°C$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$, $T_A = 25°C$	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±12	±14		±12	±14		V
Short-Circuit	$T_A = 25°C$	5	20	35	5	20	35	mA
Gain Bandwidth Product	$T_A = 25°C$	0.8	1.2		0.5	1.2		MHz
Phase Margin	$T_A = 25°C$		60			60		Deg
Slew Rate	$T_A = 25°C$		0.4			0.4		V/μs
Input Noise Voltage	$f = 1$ kHz, $T_A = 25°C$		28			28		$nV/\sqrt{Hz}$
Channel Separation	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = 0V$ to $\pm 12V$, $T_A = 25°C$		120			120		dB
Input Resistance	$T_A = 25°C$		1.0			1.0		MΩ
Input Capacitance	$T_A = 25°C$		2.0			2.0		pF
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	$V_{CM} = 0V$		2	25		2	100	nA
Input Bias Current	$V_{CM} = 0V$		50	100		50	250	nA
Supply Current (4 Op Amps)			1.7	2.2		1.7	2.5	mA
Large Signal Voltage Gain	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$	50	1000		25	1000		V/mV

DC Electrical Characteristics (Continued) ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V

DC Electrical Characteristic ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

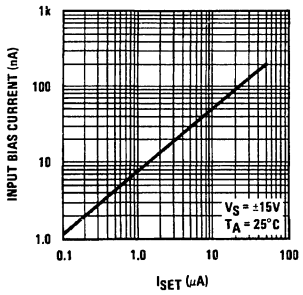
Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

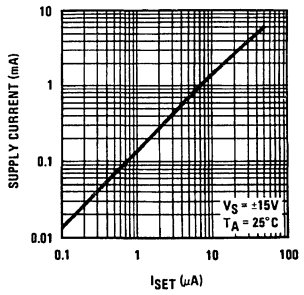
Note 5: Refer to RETS146X for LM146J military specifications.

Typical Performance Characteristics

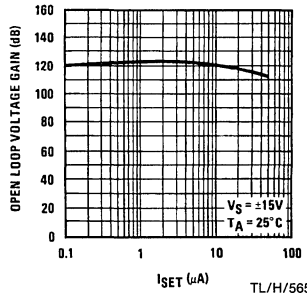
Input Bias Current vs I_{SET}



Supply Current vs I_{SET}



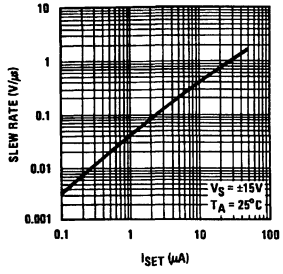
Open Loop Voltage Gain vs I_{SET}



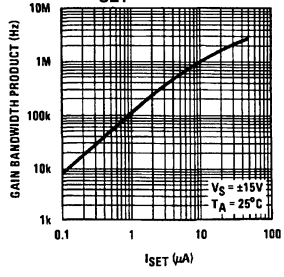
TL/H/5654–3

Typical Performance Characteristics

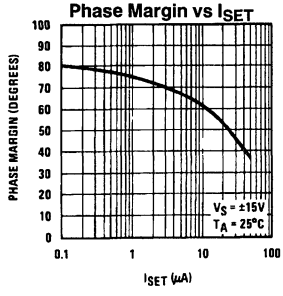
Slew Rate vs I_{SET}



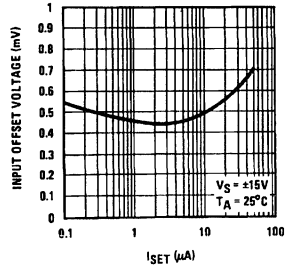
Gain Bandwidth Product vs I_{SET}



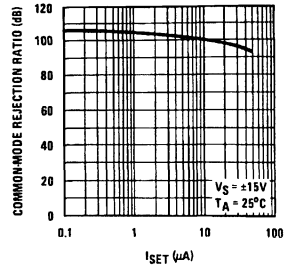
Phase Margin vs I_{SET}



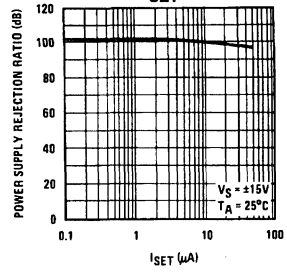
Input Offset Voltage vs I_{SET}



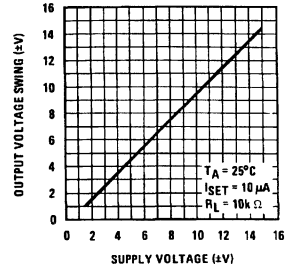
Common-Mode Rejection Ratio vs I_{SET}



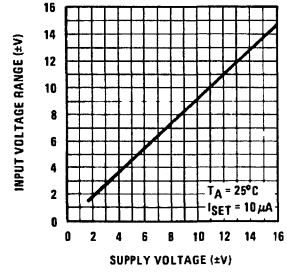
Power Supply Rejection Ratio vs I_{SET}



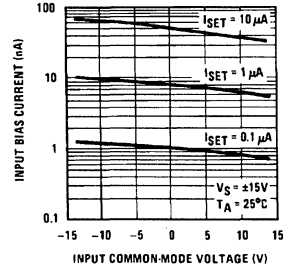
Output Voltage Swing vs Supply Voltage



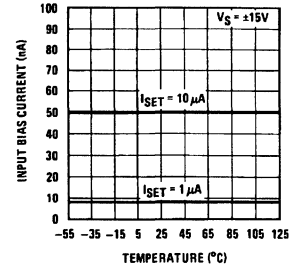
Input Voltage Range vs Supply Voltage



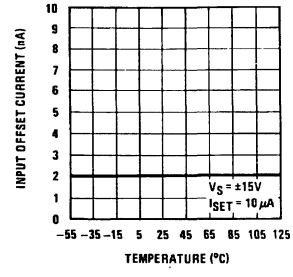
Input Bias Current vs Input Common-Mode Voltage



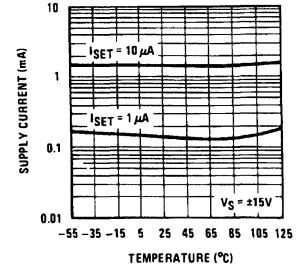
Input Bias Current vs Temperature



Input Offset Current vs Temperature



Supply Current vs Temperature



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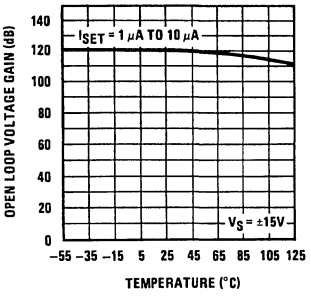
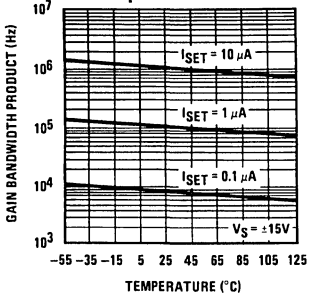
Typical Performance Characteristics (Continued)

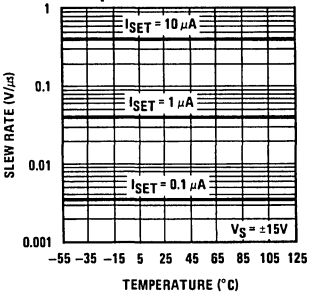
Open Loop Voltage Gain vs Temperature



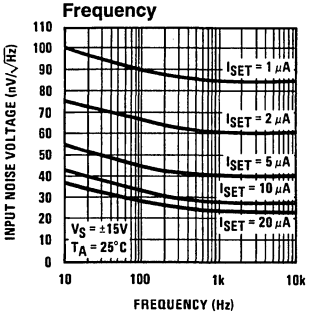
Gain Bandwidth Product vs Temperature



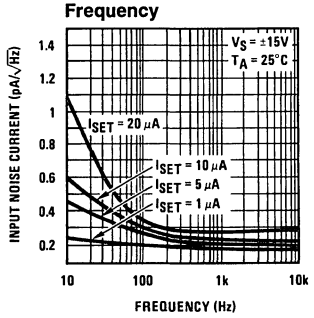
Slew Rate vs Temperature



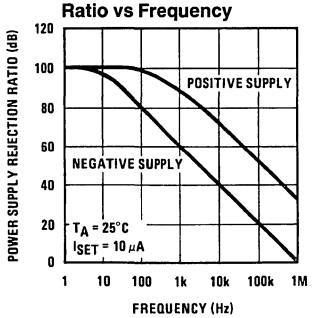
Input Noise Voltage vs Frequency



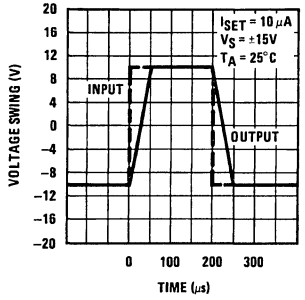
Input Noise Current vs Frequency



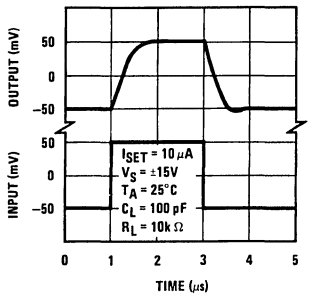
Power Supply Rejection Ratio vs Frequency



Voltage Follower Pulse Response



Voltage Follower Transient Response



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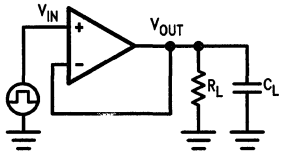
Transient Response Test Circuit



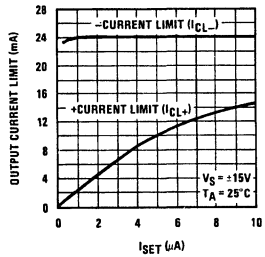
TL/H/5654–6

Application Hints

Avoid reversing the power supply polarity; the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

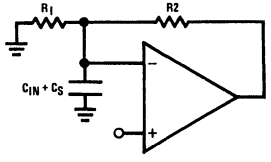
Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output current capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.



TL/H/5654–7

FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback (*Figure 2*), this pole occurs at $\frac{1}{2\pi}$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.



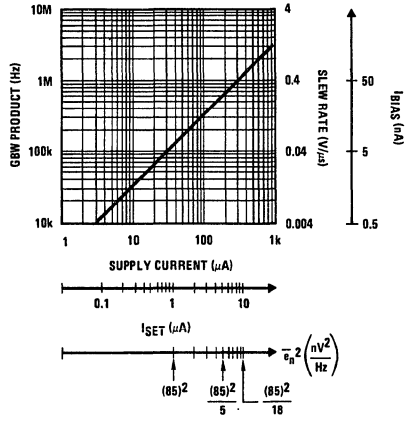
TL/H/5654–9

FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behaviour is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5−4 MHz.

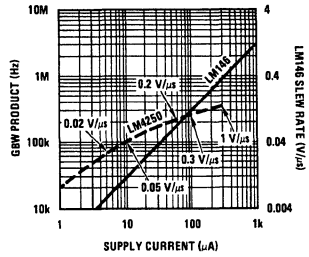


TL/H/5654–8

FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz. For GBW products below 200 kHz, the LM4250 will consume less power.

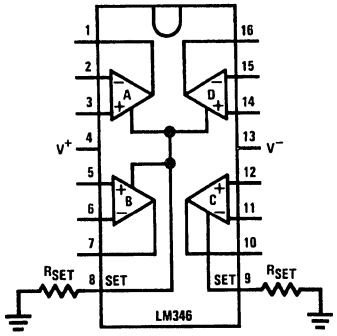


TL/H/5654–10

FIGURE 4. LM146 vs LM4250

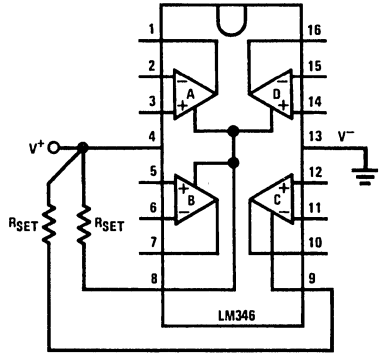
Typical Applications

Dual Supply or Negative Supply Biasing



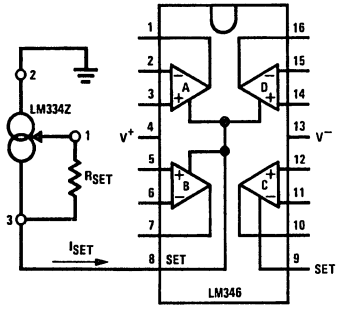
$$I_{SET} \cong \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



$$I_{SET} \cong \frac{V^+ - 0.6V}{R_{SET}}$$

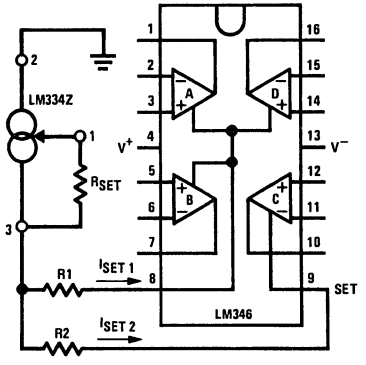
Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product Temperature coefficient of the LM346.

Biasing all 4 Amplifiers with Single Current Source



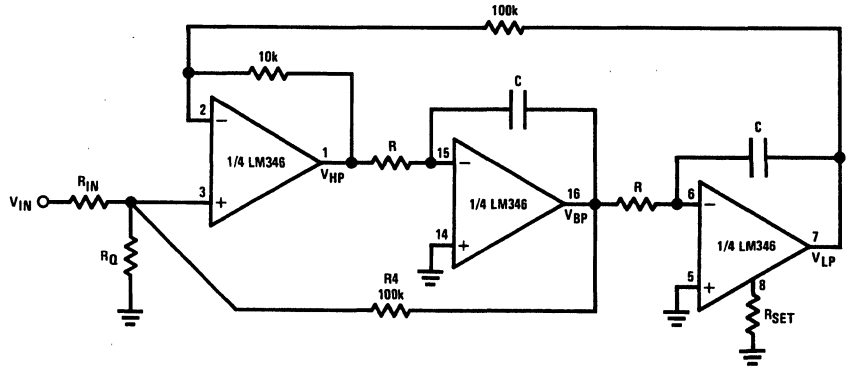
TL/H/5654–11

$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- For $I_{SET1} \cong I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



TL/H/5654–12

- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

Circuit synthesis equations (for circuit analysis equations, consult with the LM148 data sheet).

Need to know desired: f_o = center frequency measured at the BP output

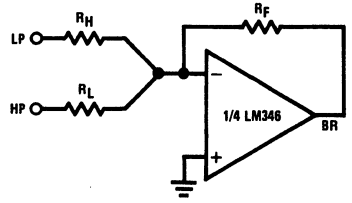
Q_o = quality factor measured at the BP output

H_o = gain at the output of interest (BP or HP or LP or all of them)

- Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$
- $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)
- For BP output: $R_Q = \left(\dfrac{3.478\,Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.748 \times Q_o}\right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\,Q_o}{H_{o(BP)}} - 1\right)}{\dfrac{1}{RQ} + 10^{-5}}$
- For HP ouput: $R_Q = \dfrac{1.1 \times 10^5}{3.478\,Q_o\,(1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$

Note. All resistor values are given in ohms.

- For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\,Q_o\,(11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$
- For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\,\frac{f_{notch}}{f_o}$$

TL/H/5654–13

Determine R_F according to the desired gains: $H_{o(BR)}\Big|_{f<<f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\Big|_{f>>f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\ \mu A} \times \frac{1}{f_o \times H_o}\ (\text{Volts})$$

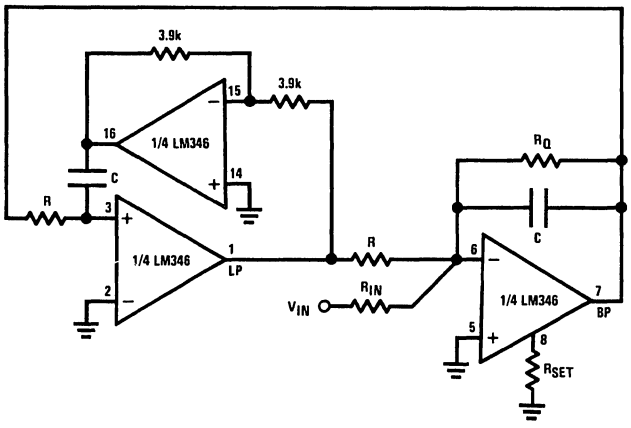
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \cong \frac{f_o}{1 + \dfrac{2\,f_o}{GBW}},\ Q_{real} \cong \frac{Q_o}{1 - \dfrac{3.2\,f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



TL/H/5654–14

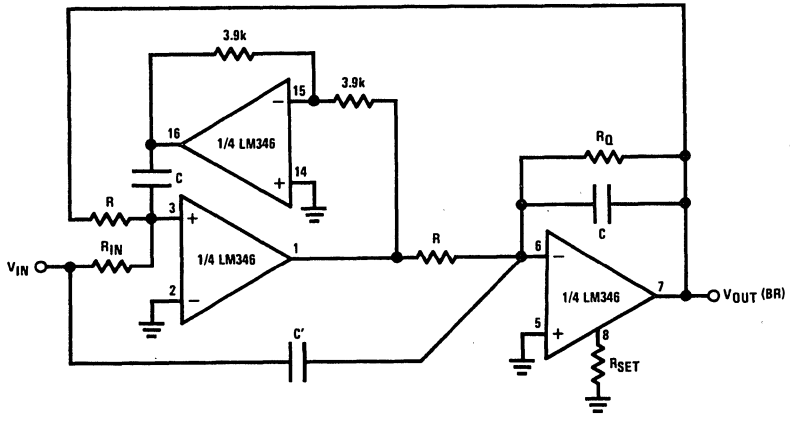
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



TL/H/5654–15

Circuit Synthesis Equations

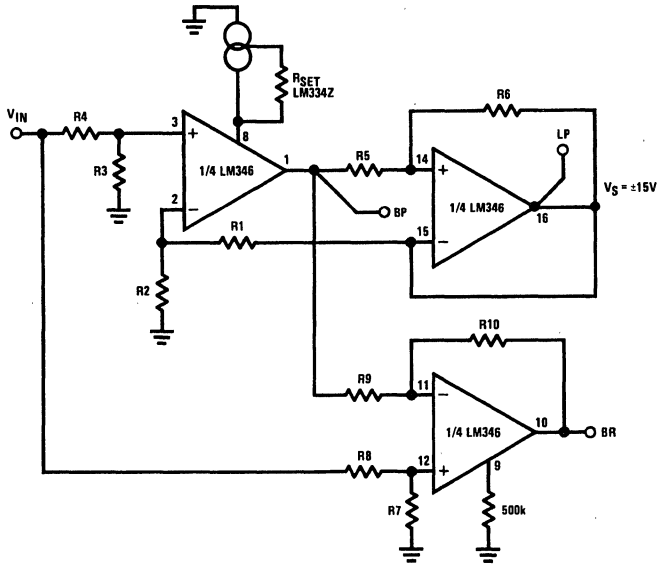
$$R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}} \quad H_{o(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)



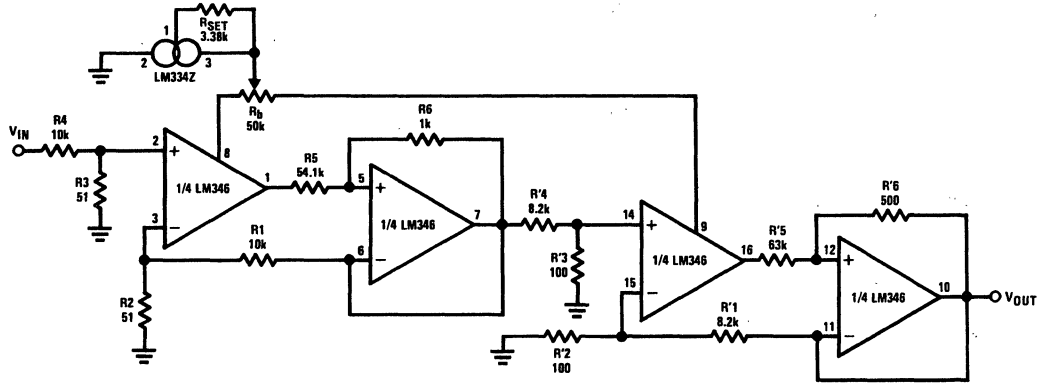
TL/H/5654–16

- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed Vpeak(out) $\leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}(\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R(+ R10}$, $f_{o(BP)} = f_u\sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$, $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

$f_{o(BR)} = f_{o(BP)}$, $\left(1 - \frac{c}{b}\right) \cong f_{o(BP)}$ $(C < < 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.

- Advantage: f_oQ_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; (b < 1)
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}. This adjusts the unity gain frequency (f_u) of the op amp.

A 4th Order Butterworth Low Pass Capacitorless Filter



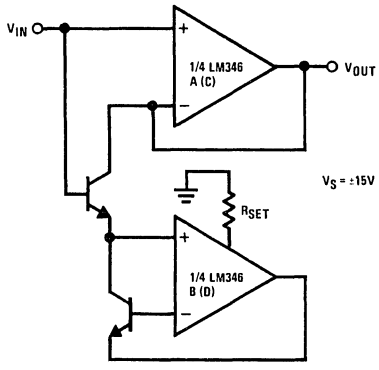
TL/H/5654–17

Ex: f_c = 20 kHz, H_o (gain of the filter) = 1, Q_{01} = 0.541, Q_{o2} = 1.306.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

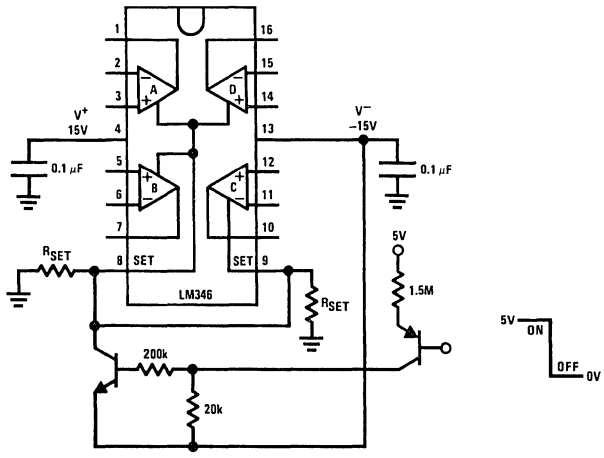
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



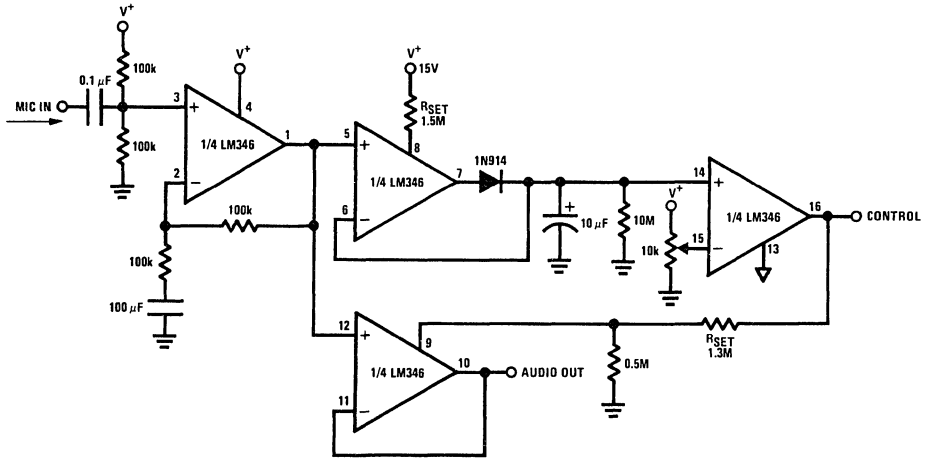
- For better performance, use a matched NPN pair.

Circuit Shutdown



- By pulling the SET pin(s) to V− the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

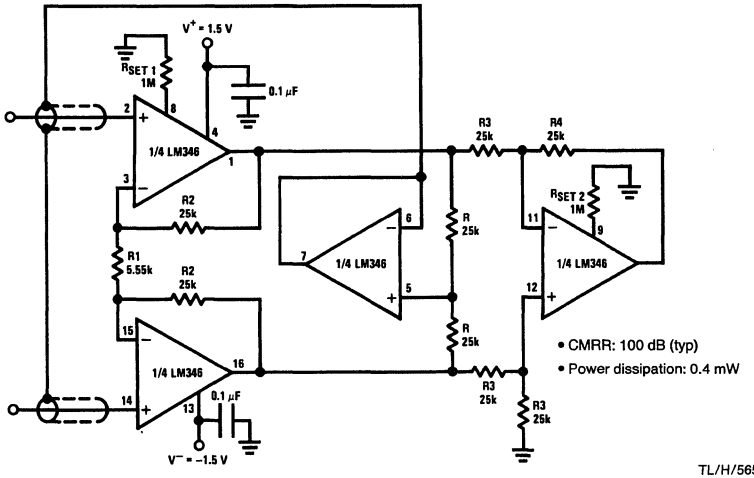
Voice Activated Switch and Amplifier



TL/H/5654–18

Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



TL/H/5654–19

National Semiconductor

LM148/LM149 Series Quad 741 Op Amp

LM148/LM248/LM348 Quad 741 Op Amps
LM149/LM249/LM349 Wide Band Decompensated ($A_{V\,(MIN)} = 5$)

General Description

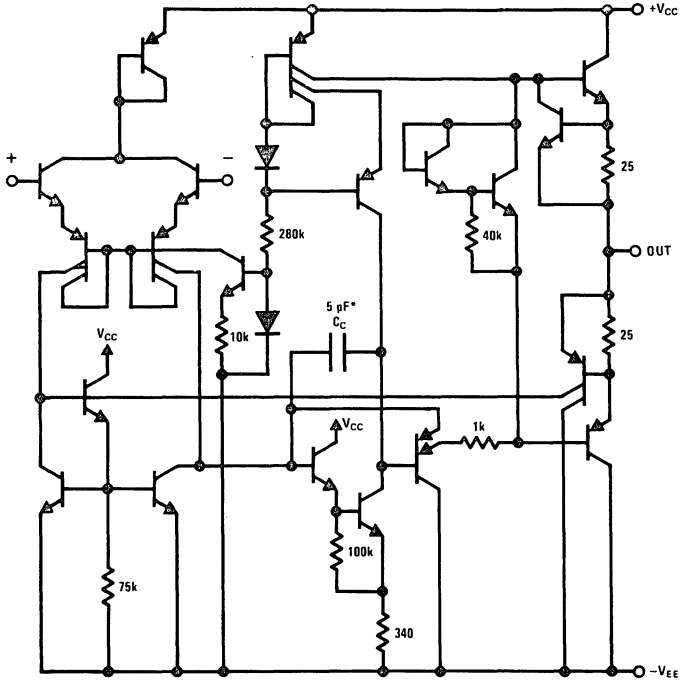
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

- 741 op amp operating characteristics
- Low supply current drain — 0.6 mA/Amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1 mV
- Low input offset current — 4 nA
- Low input bias current — 30 nA
- Gain bandwidth product
  - LM148 (unity gain) — 1.0 MHz
  - LM149 ($A_V \geq 5$) — 4 MHz
- High degree of isolation between amplifiers — 120 dB
- Overload protection for inputs and outputs

Schematic Diagram



TL/H/7786–1

*1 pF in the LM149

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM148/LM149	LM248/LM249	LM348/LM349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and			
Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	—	—	750 mW
θ_{jA}	—	—	100°C/W
Cavity DIP (J) P_d	1100 mW	800 mW	700 mW
θ_{JA}	110°C/W	110°C/W	110°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C	300°C	300°C
Lead Temperature (Soldering, 10 sec.) Plastic			260°C
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	220°C	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5)	500V	500V	500V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM148/LM149			LM248/LM249			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \le 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	LM148 Series $T_A = 25°C$ LM149 Series		1.0 4.0			1.0 4.0			1.0 4.0		MHz MHz
Phase Margin	LM148 Series ($A_V = 1$) $T_A = 25°C$ LM149 Series ($A_V = 5$)		60 60			60 60			60 60		degrees degrees
Slew Rate	LM148 Series ($A_V = 1$) $T_A = 25°C$ LM149 Series ($A_V = 5$)		0.5 2.0			0.5 2.0			0.5 2.0		V/μs V/μs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM148/LM149			LM248/LM249			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$	25			15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
Input Voltage Range	$V_S = \pm 15V$	± 12			± 12			± 12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

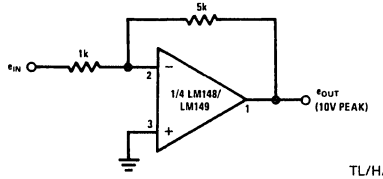
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

Note 4: Refer to RETS 148X for LM148 military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Cross Talk Test Circuit



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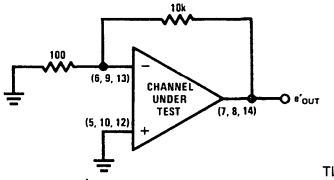


TL/H/7786–7

$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$V_S = \pm 15V$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

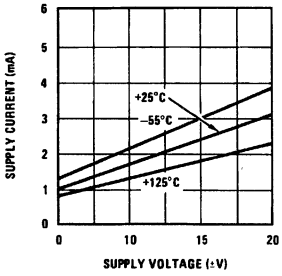
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

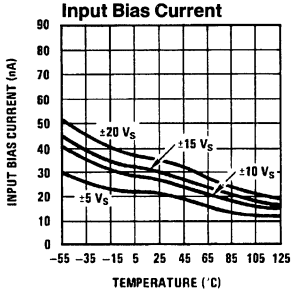
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Performance Characteristics

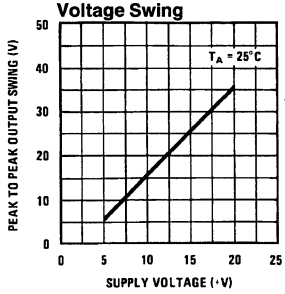
Supply Current



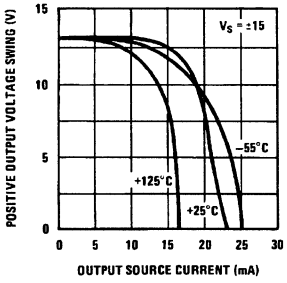
Input Bias Current



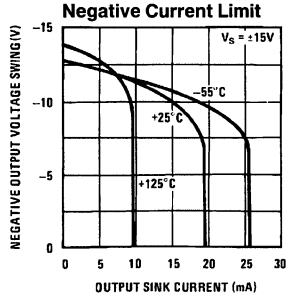
Voltage Swing



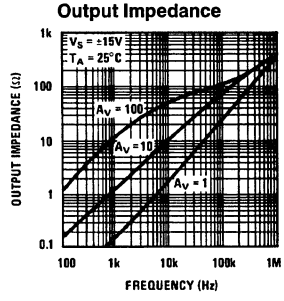
Positive Current Limit



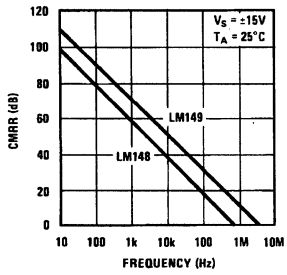
Negative Current Limit



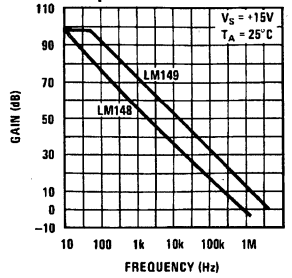
Output Impedance



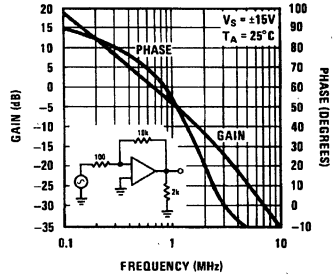
Common-Mode Rejection Ratio



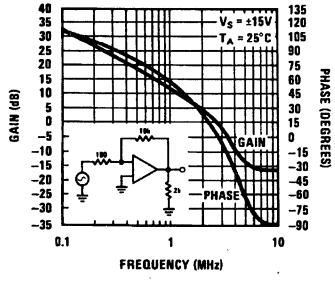
Open Loop Frequency Response



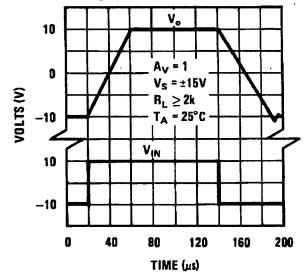
Bode Plot LM148



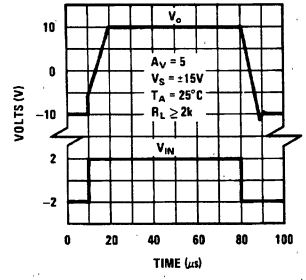
Bode Plot LM149



Large Signal Pulse Response (LM148)



Large Signal Pulse Response (LM149)



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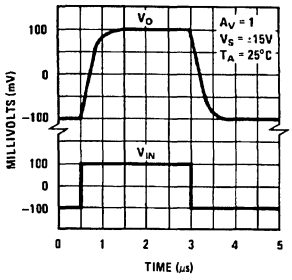
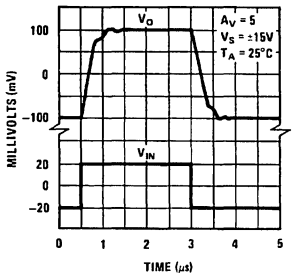
Typical Performance Characteristics (Continued)

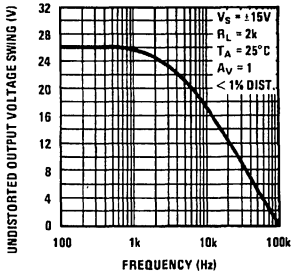
Small Signal Pulse Response (LM148)



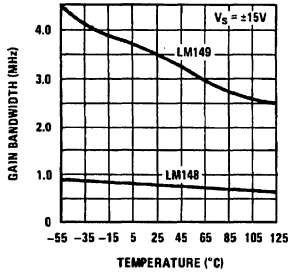
Small Signal Pulse Response (LM149)



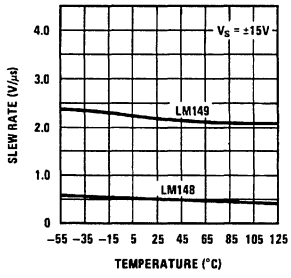
Undistorted Output Voltage Swing



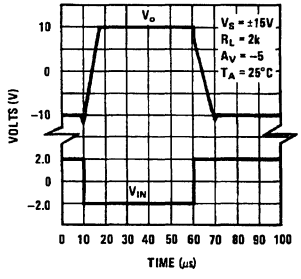
Gain Bandwidth



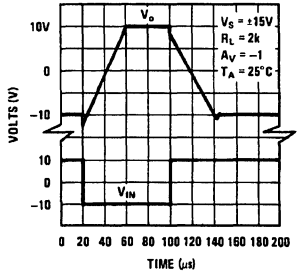
Slew Rate



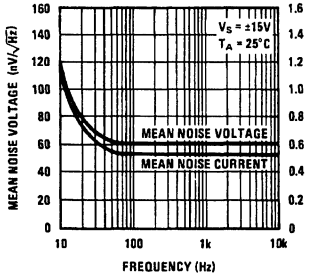
Inverting Large Signal Pulse Response (LM149)



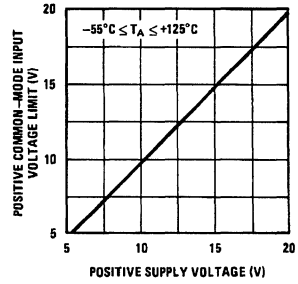
Inverting Large Signal Pulse Response (LM148)



Input Noise Voltage and Noise Current



Positive Common-Mode Input Voltage Limit



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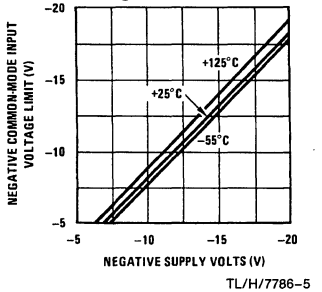
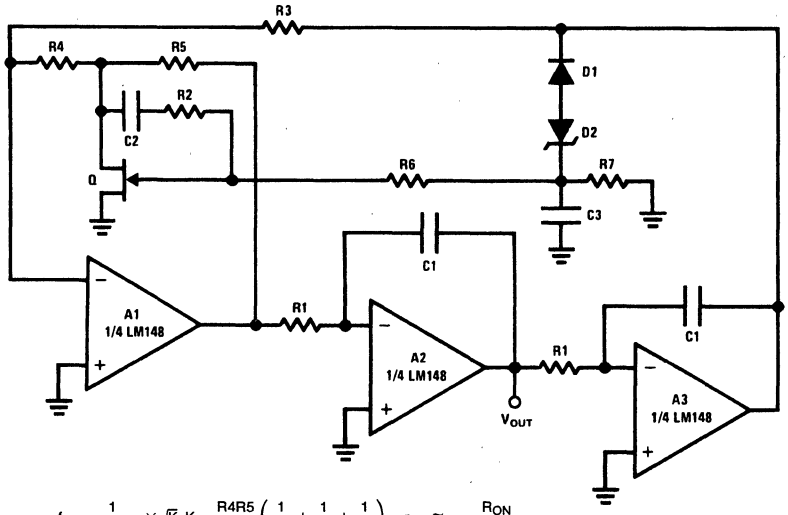
Negative Common-Mode Input Voltage Limit



TL/H/7786–5

Typical Applications—LM148

One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

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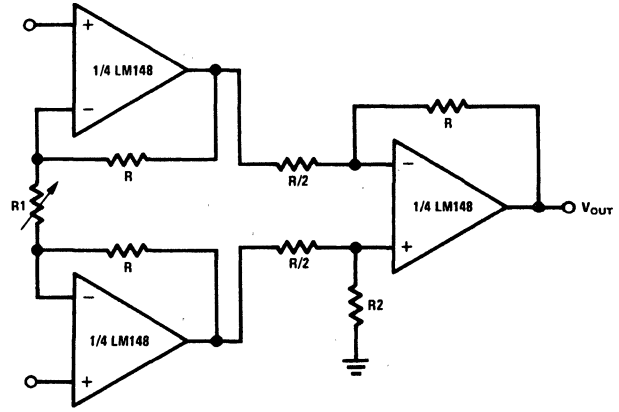
f_{MAX} = 5 kHz, THD ≤ 0.03%

R1 = 100k pot. C1 = 0.0047 μF, C2 = 0.01 μF, C3 = 0.1 μF, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier



TL/H/7786–9

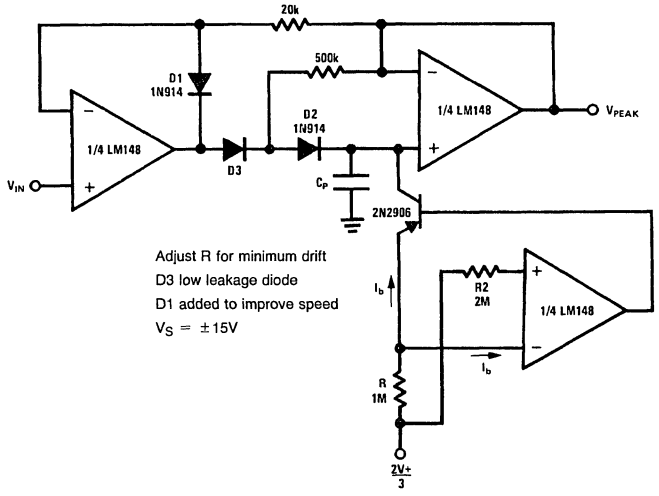
$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right)$, $V_S^- - 3V \le V_{IN\,CM} \le V_S^+ - 3V$,

V_S = ±15V

R = R2, trim R2 to boost CMRR

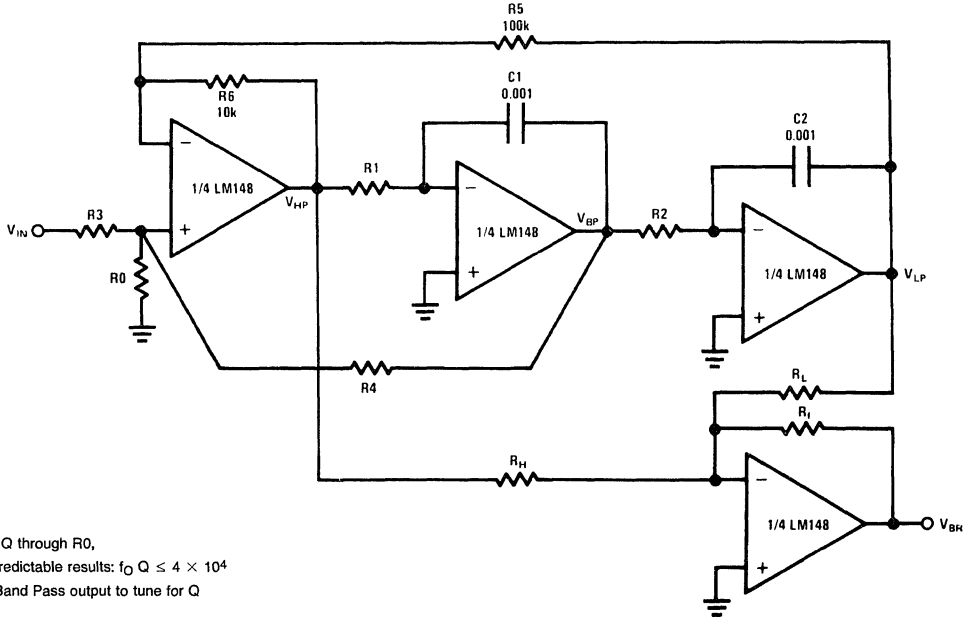
Typical Applications—LM148 (Continued)

Low Drift Peak Detector with Bias Current Compensation



TL/H/7786–10

Universal State-Variable Filter



Tune Q through R0,
For predictable results: $f_O\ Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

TL/H/7786–11

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o{}^2$$

$$N_{HP(s)} = S^2\,H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O\,H_{OBP}}{Q}\quad N_{LP} = \omega_o{}^2\,H_{OLP}.$$

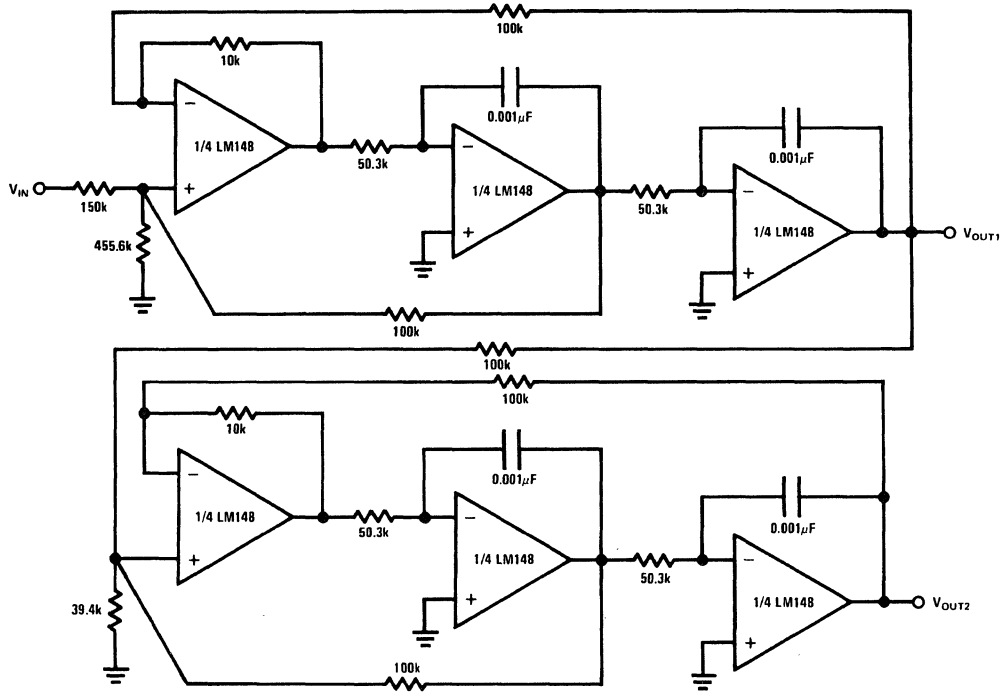
$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6\,t_1}{R5\,t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\,t_1\,t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Typical Applications—LM148 (Continued)

A 1 kHz 4 Pole Butterworth



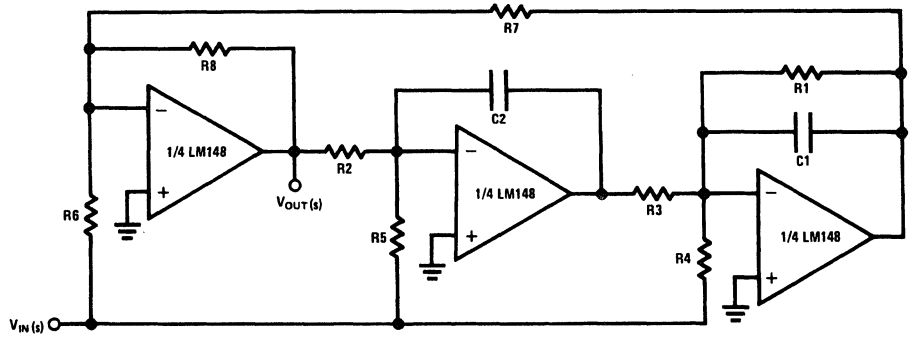
TL/H/7786–12

Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



TL/H/7786–13

$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

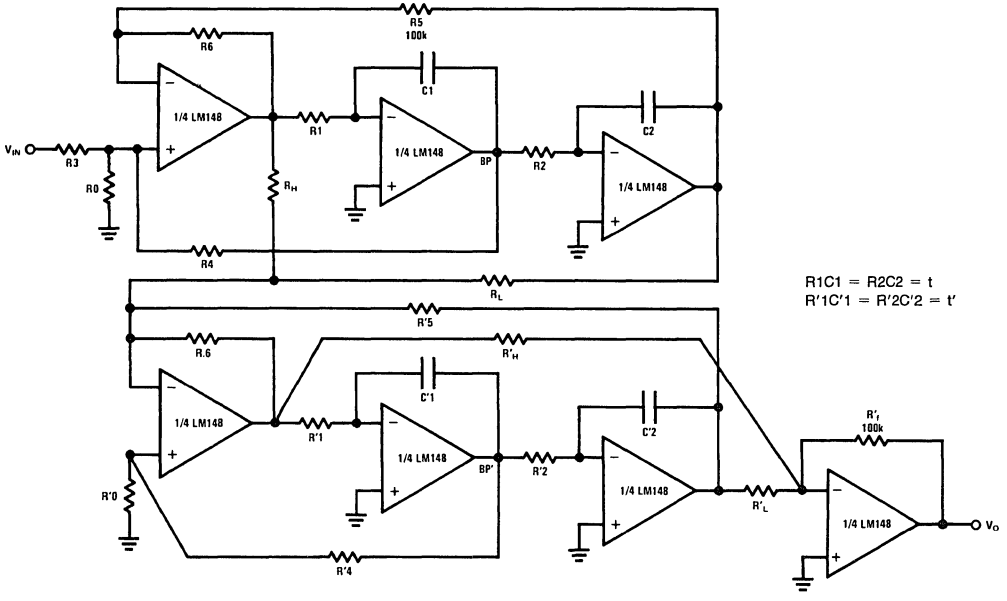
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001 μF

Better noise performance than the state-space approach.

Typical Applications—LM148 (Continued)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



TL/H/7786–14

f_C = 1 kHz, f_S = 2 kHz, f_p = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

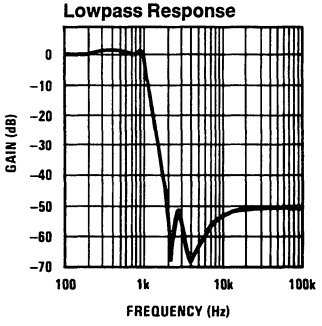
$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001 μF.

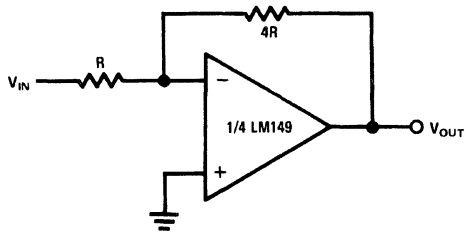
Lowpass Response



TL/H/7786–15

Typical Applications—LM149

Minimum Gain to Insure LM149 Stability



TL/H/7786–16

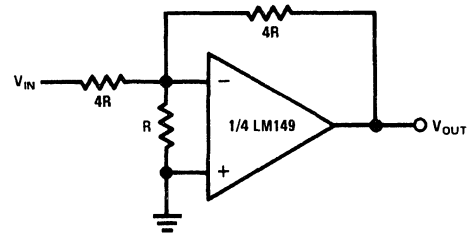
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL(s)}}\right)} \cong -4$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\, V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

The LM149 as a Unity Gain Inverter



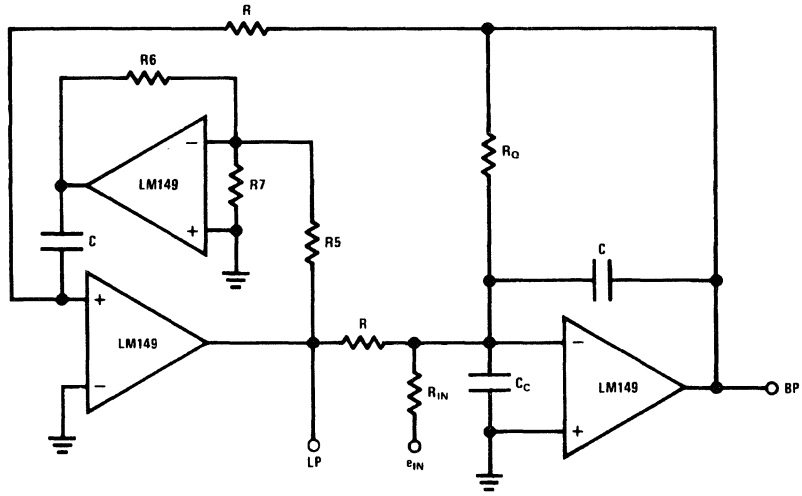
TL/H/7786–17

$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1 + \frac{6}{A_{OL(s)}}}\right) \cong -1$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\, V_{OS}$$

Small Signal BW = G BW/5

Non-inverting-Integrator Bandpass Filter



TL/H/7786–18

For stability purposes: R7 = R6/4, 10R6 = R5, C_C = 10C

$$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6}} \times \frac{1}{RC},\ Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}},\ Ho_{BP} = \frac{R_Q}{R_{IN}}$$

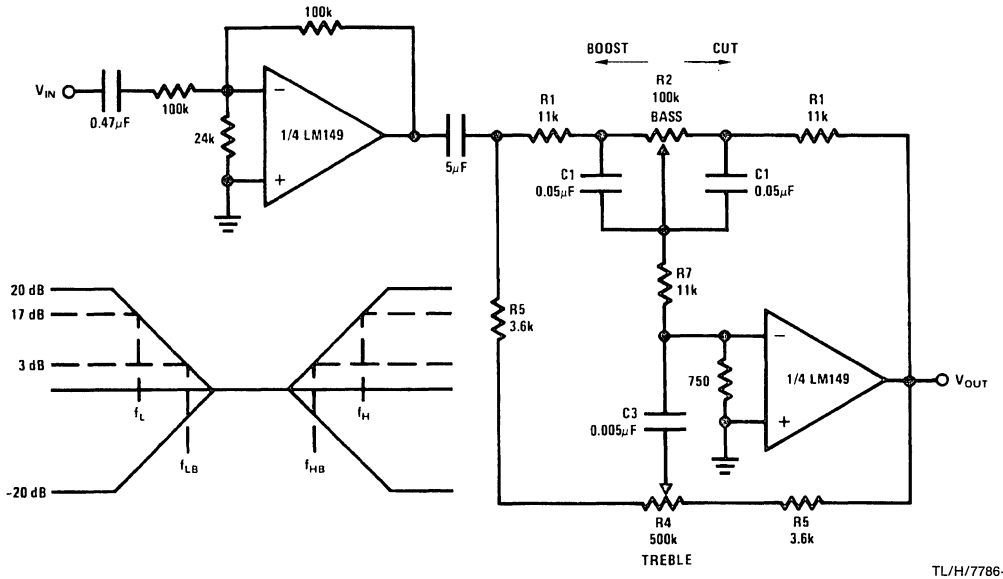
$f_{O(MAX)}$, Q_{MAX} = 20 kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, C_C added for compensation

Typical Applications—LM149 (Continued)

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)



TL/H/7786–19

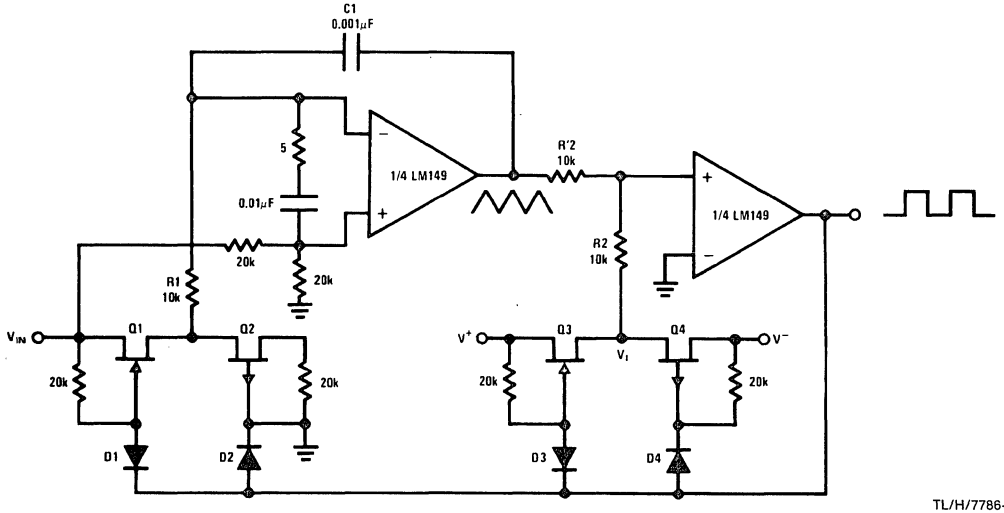
$V_S = \pm 15V$, $V_{OUT(MAX)} = 9.1\ V_{RMS}$,
$f_{MAX} = 20$ kHz, THD ≤ 1%
Duplicate the above circuit for stereo

$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C3},\ f_{HB} = \frac{1}{2\pi(R1 + 2R7)\,C3}$$

Max Bass Gain ≅ (R1 + R2)/R1
Max Treble Gain ≅ (R1 + 2R7)/R5
as shown: $f_L \cong 32$ Hz, $f_{LB} \cong 320$ Hz
$f_H \cong 11$ kHz, $f_{HB} \cong 1.1$ Hz

Triangular Squarewave Generator



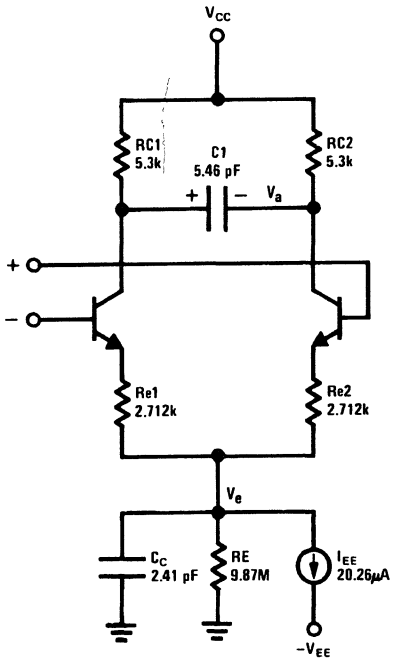
TL/H/7786–20

$$f = \frac{K \times V_{IN}}{8V^+C1R1},\ K = R2/R'2,\ \frac{2V_I}{K} \le 25V,\ V^+ = V^-,\ V_S = \pm 15V$$

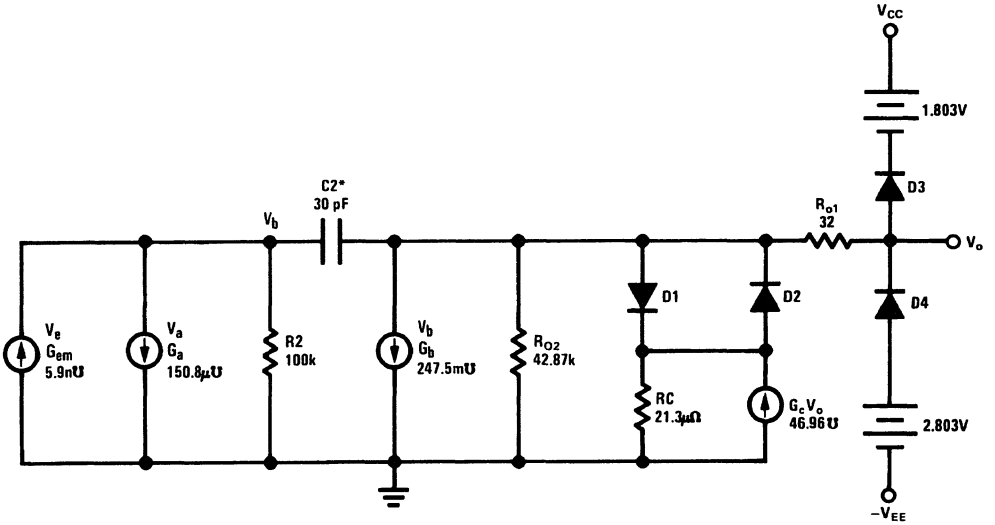
Use LM125 for ±15V supply
The circuit can be used as a low frequency V/F for process control.
Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

Typical Simulation

LM148, LM149, LM741 Macromodel for Computer Simulation



TL/H/7786–21



TL/H/7786–22

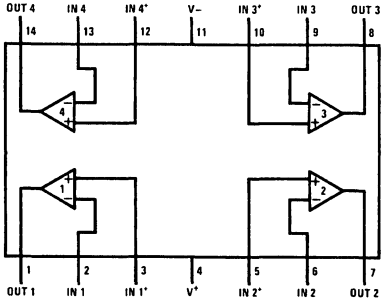
$\beta_{o1} = 112$ $I_S = 8 \times 10^{-16}$

$\beta_{o2} = 144$ *C2 = 6 pF for LM149

For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

Connection Diagram

Dual-In-Line Package



TL/H/7786–2

Top View

Order Number LM148J, LM248J, LM348J, LM149J, LM249J, LM349J, LM348M, LM348N or LM349N
See NS Package Number J14A, M14A or N14A

National Semiconductor

LM158/LM258/LM358, LM158A/LM258A/LM358A, LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

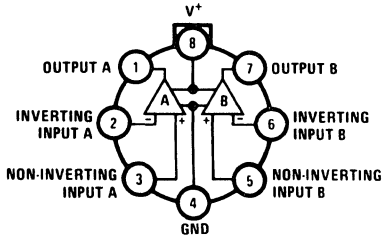
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 32 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC}
  and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

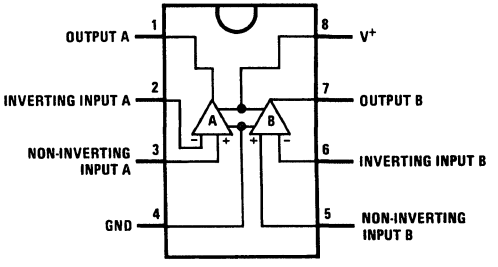
Connection Diagrams (Top Views)

Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H
See NS Package Number H08C



TL/H/7787–2

Order Number LM158J, LM158AJ or LM358J
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP (LM358N)	830 mW	830 mW
Metal Can (LM158H/ LM258H/LM358H)	550 mW	
Small Outline Package	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, unless otherwise stated

Parameter	Conditions	LM158A		LM258A		LM358A		LM158/LM258		LM358		LM2904		Units
		Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$	±1	±2	±1	±3	±2	±3	±2	±5	±2	±7	±2	±7	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)	20	50	40	80	45	100	45	150	45	250	45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	±2	±10	±2	±15	±5	±30	±3	±30	±5	±50	±5	±50	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps													
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)	1	2	1	2	1	2	1	2	1	2	1	2	mA_{DC}
	$V^+ = 5V$	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	mA_{DC}

Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

Parameter	Conditions	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1\ V_{DC}$ to $11\ V_{DC}$)	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$	70	85		70	85		65	85		85	85		65	85		50	70		dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2904, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$), $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $V^+ = 15\ V_{DC}$, $T_A = 25°C$, $V_O = 2\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $T_A = 25°C$, $V_O = 200\ mV_{DC}$, $V^+ = 15\ V_{DC}$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2), $V^+ = 15\ V_{DC}$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage	(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	15		7	15		7	20		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±30			±30			±75			±100			±150		±45	±200	nA_{DC}
Input Offset Current Drift	$R_S = 0\Omega$		10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}

Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

Parameter	Conditions	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2904, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ ($V_O = 1\ V_{DC}$ to $11\ V_{DC}$) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$ (LM2904, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current	$V_O = 2\ V_{DC}$																			
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a $+125°C$ maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a $+150°C$ maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$) at 25°C. For LM2904, V^+ from $5\ V_{DC}$ to $26\ V_{DC}$.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2904), independent of the magnitude of V^+.

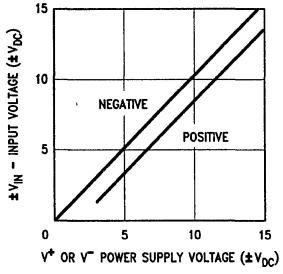
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

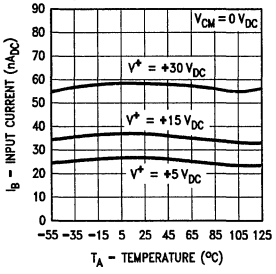
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

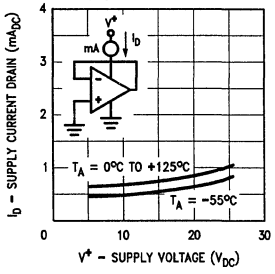
Input Voltage Range



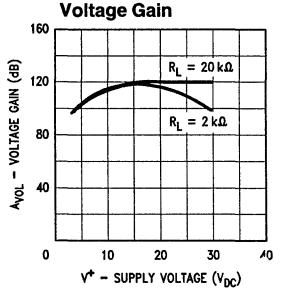
Input Current



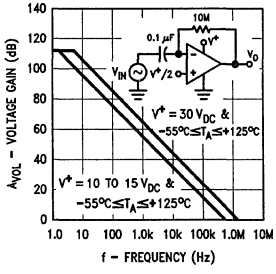
Supply Current



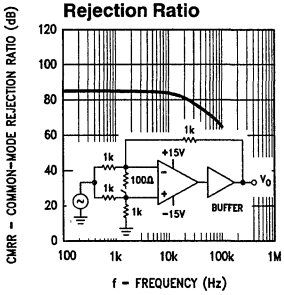
Voltage Gain



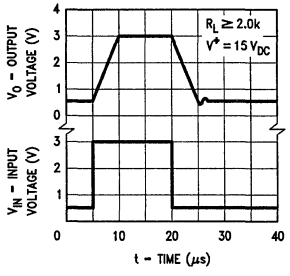
Open Loop Frequency Response



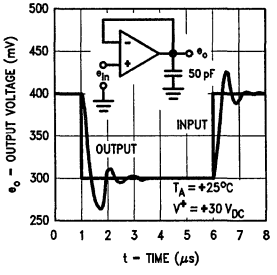
Common-Mode Rejection Ratio



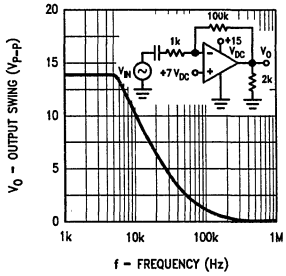
Voltage Follower Pulse Response



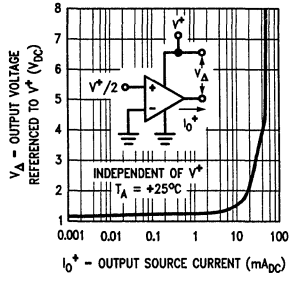
Voltage Follower Pulse Response (Small Signal)



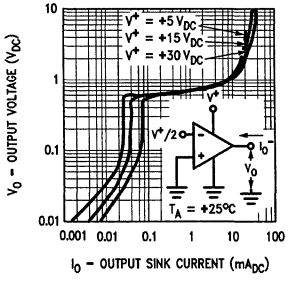
Large Signal Frequency Response



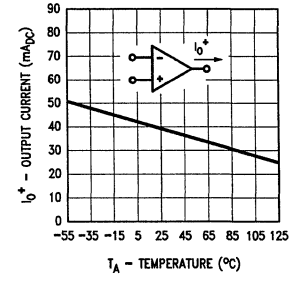
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

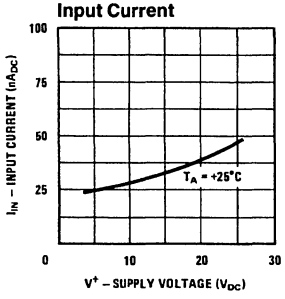


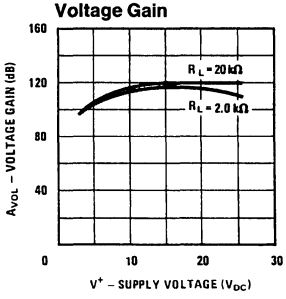
Current Limiting



TL/H/7787–4

Typical Performance Characteristics (Continued) (LM2902 only)





TL/H/7787–5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

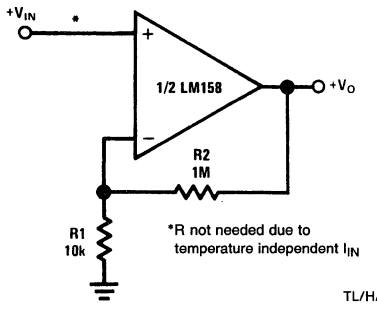
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

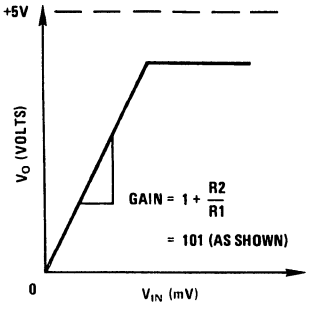
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

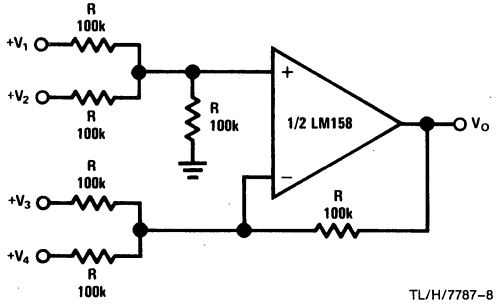


TL/H/7787–6



TL/H/7787–7

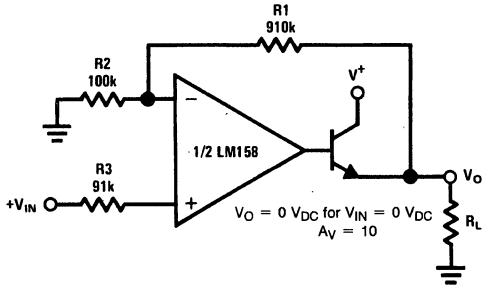
DC Summing Amplifier
($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq 0\ V_{DC}$)



TL/H/7787–8

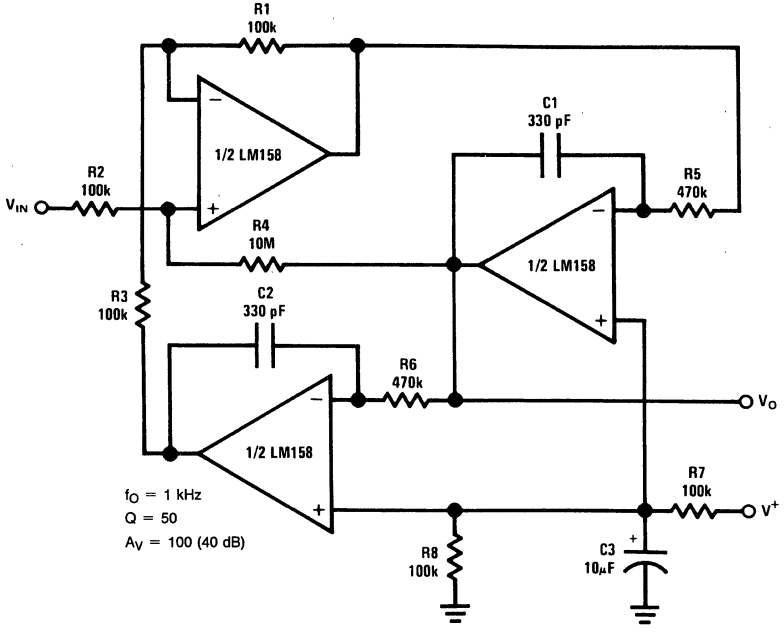
Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



TL/H/7787–9

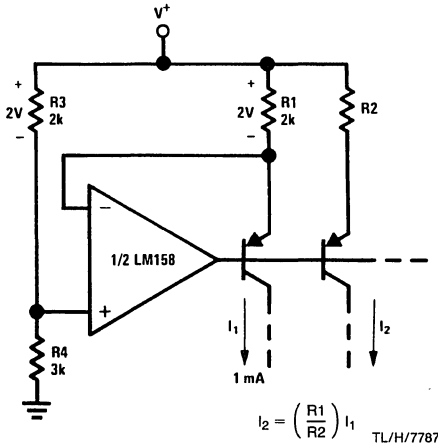
"BI-QUAD" RC Active Bandpass Filter



TL/H/7787–10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

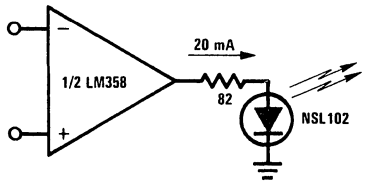
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

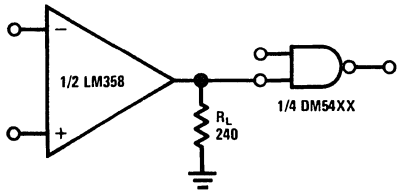
TL/H/7787–11

LED Driver



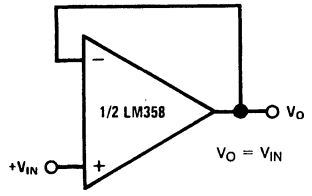
TL/H/7787–13

Driving TTL



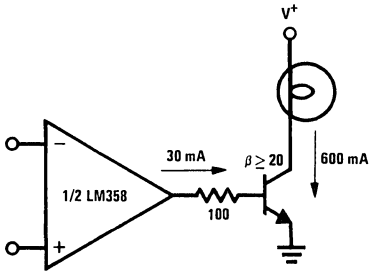
TL/H/7787–15

Voltage Follower



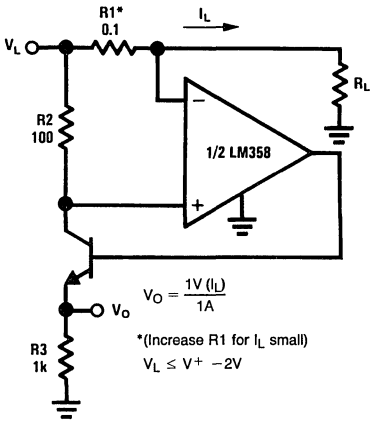
TL/H/7787–17

Lamp Driver



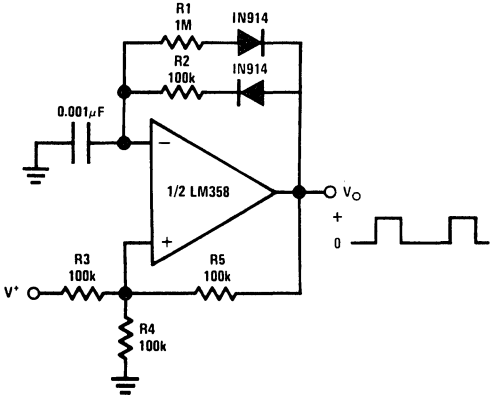
TL/H/7787–12

Current Monitor



TL/H/7787–14

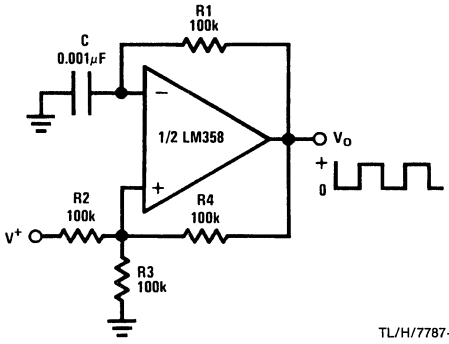
Pulse Generator



TL/H/7787–16

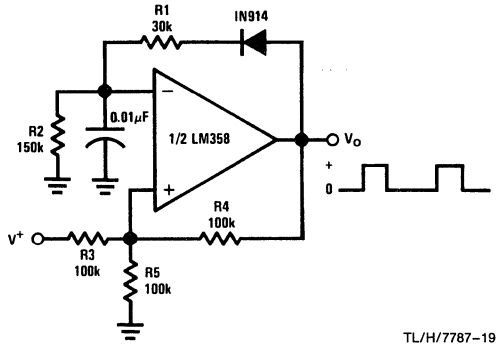
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



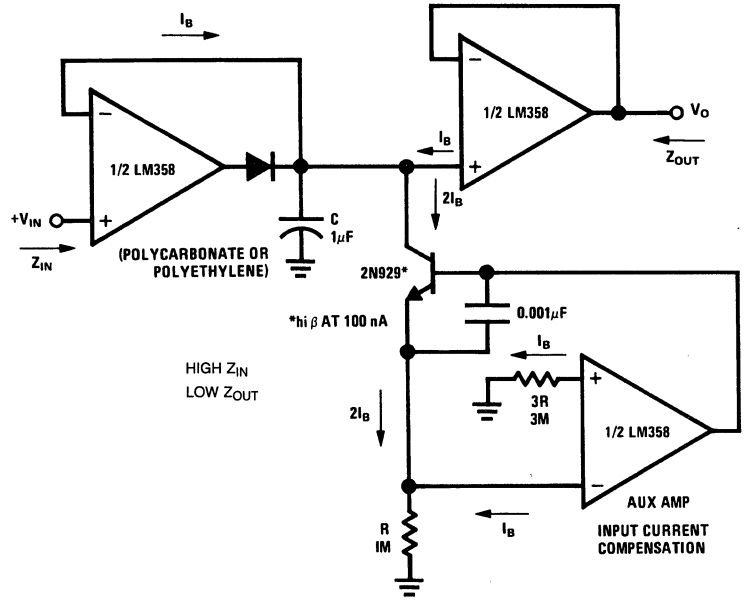
TL/H/7787–18

Pulse Generator



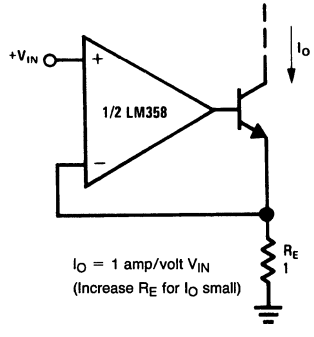
TL/H/7787–19

Low Drift Peak Detector



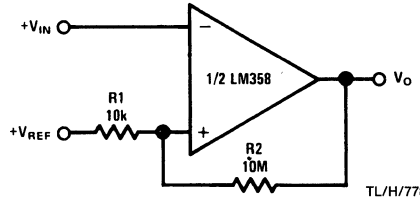
TL/H/7787–20

High Compliance Current Sink



TL/H/7787–21

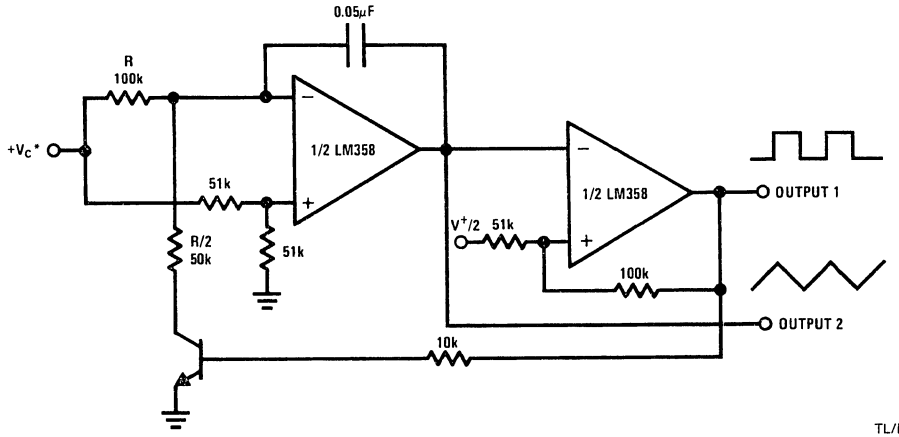
Comparator with Hysteresis



TL/H/7787–22

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

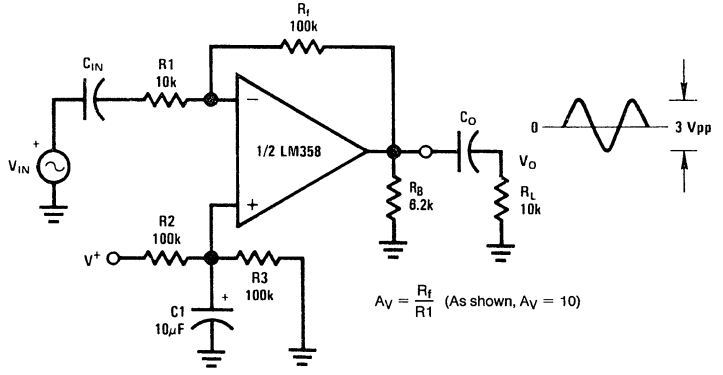
Voltage Controlled Oscillator (VCO)



TL/H/7787–23

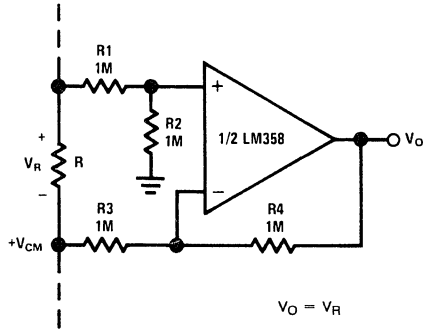
*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

AC Coupled Inverting Amplifier



TL/H/7787–24

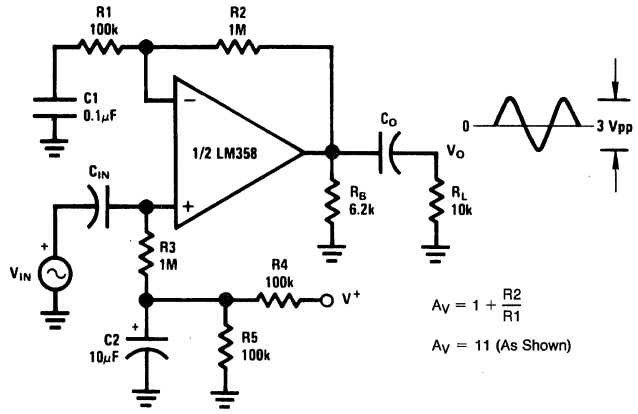
Ground Referencing a Differential Input Signal



TL/H/7787–25

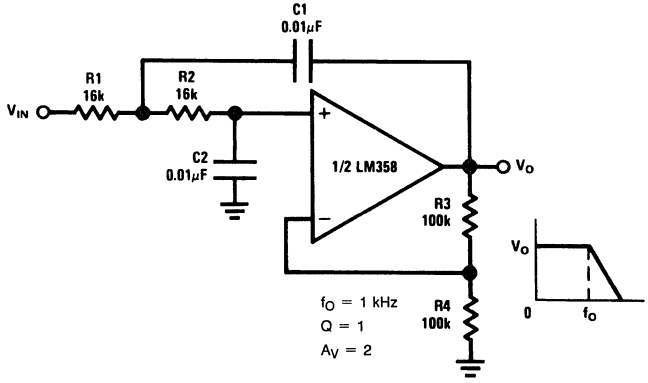
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier



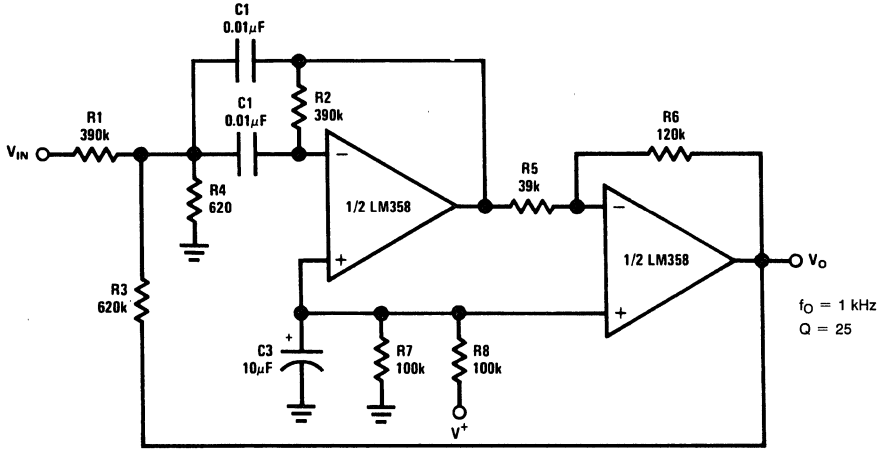
TL/H/7787–26

DC Coupled Low-Pass RC Active Filter



TL/H/7787–27

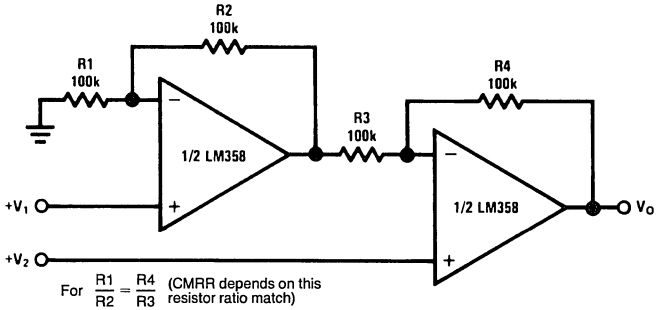
Bandpass Active Filter



TL/H/7787–28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier



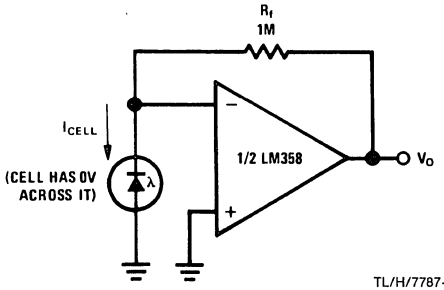
TL/H/7787–29

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

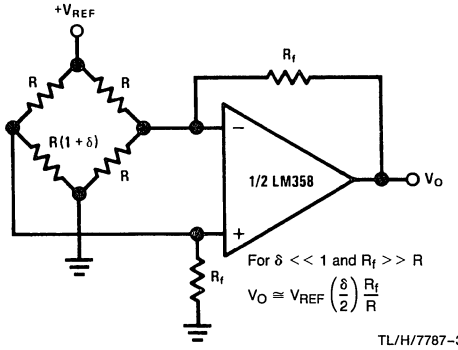
As Shown: $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787–30

Bridge Current Amplifier

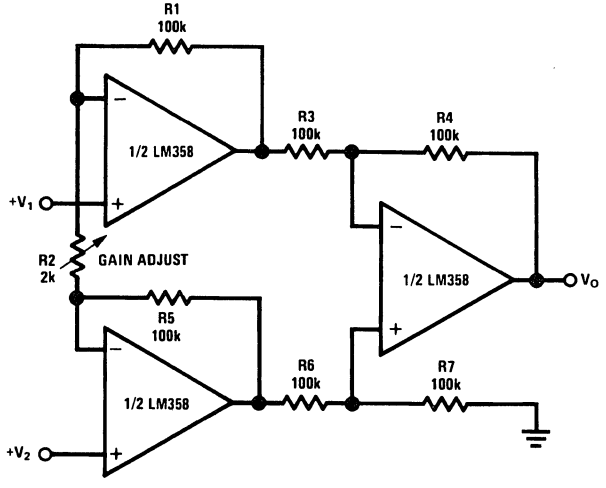


For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/7787–33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787–31

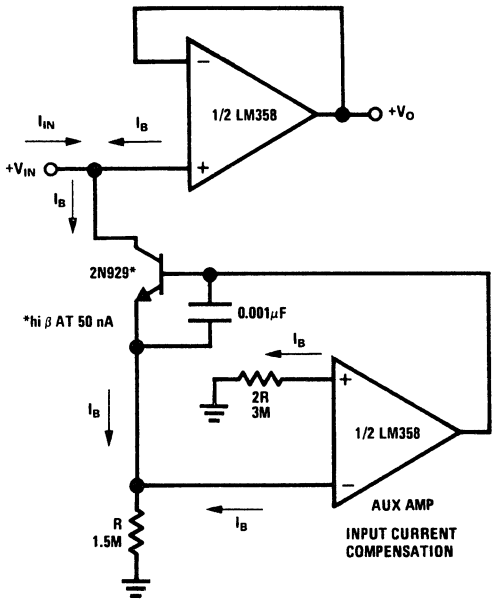
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

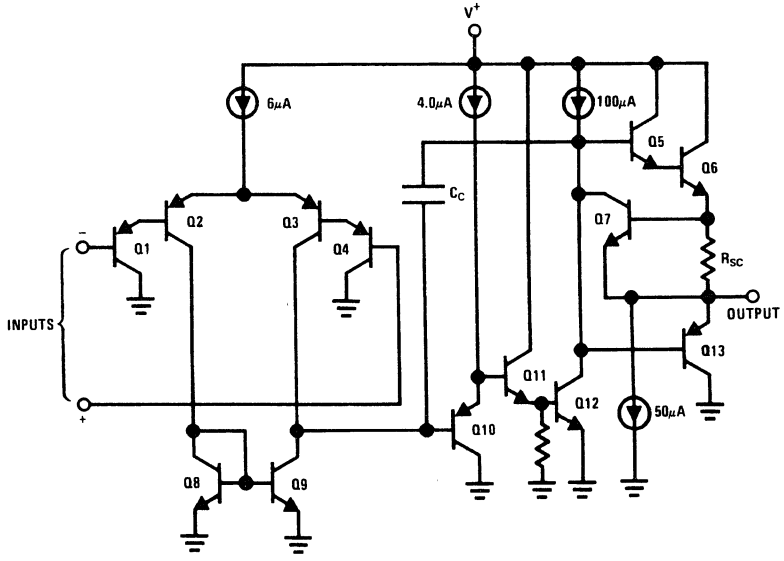
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/7787–32

Schematic Diagram (Each Amplifier)



TL/H/7787–3

National Semiconductor

LM392/LM2924
Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Features

- Wide power supply voltage range
  Single supply 3V to 32V
  Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to V^+ − 1.5V

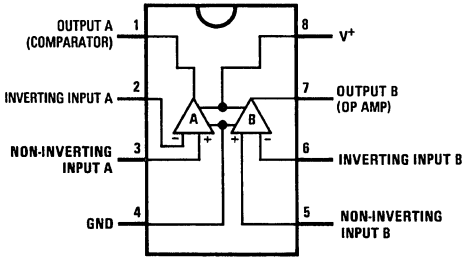
ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagram (Top View)

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Dual-In-Line Package



TL/H/7793–1

Order Number LM2924J
See NS Package Number J08A
Order Number LM392M
See NS Package Number M08A
Order Number LM392N or LM2924N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM392	LM2924
Supply Voltage, V^+	32V or ±16V	26V or ±13V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP (LM392N, LM2924N)	820 mW	820 mW
Small Outline Package	530 mW	530 mW
Output Short-Circuit to Ground (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM392	0°C to +70°C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
ESD rating to be determined.		
Soldering Information		
Dual-in-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±7	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 6), $V_{CM} = 0V$		50	250		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±5	±50		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$, $V^+ = 30V$, (LM2924, $V^+ = 26V$)		1	2		1	2	mA
Supply Current	$R_L = \infty$, $V^+ = 5V$		0.5	1		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8)		−100			−100		dB
Input Offset Voltage	(Note 5)			±7			±7	mV
Input Bias Current	IN(+) or IN(−)			400			500	nA
Input Offset Current	IN(+) − IN(−)			150			200	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if Used), (Note 9)			32			26	V
OP AMP ONLY								
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, V_o swing = 1 V_{DC} to 11 V_{DC}, $R_L = 2\ k\Omega$, $T_A = 25°C$	25	100		25	100		V/mV

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated)

(Note 4) (Continued)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
OP AMP ONLY								
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$, $V_{CM} = 0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$	65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		50	100		dB
Output Current Source	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		mA
Output Current Sink	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		mA
	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 200\ mV$, $T_A = 25°C$	12	50		12	50		μA
Input Offset Voltage Drift	$R_S = 0\Omega$		7			7		μV/°C
Input Offset Current Drift	$R_S = 0\Omega$		10			10		pA_{DC}/°C
COMPARATOR ONLY								
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 10)		1.3			1.5		μs
Output Sink Current	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V_o \geq 1.5\ V_{DC}$, $T_A = 25°C$	6	16		6	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400			400	mV
	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700	mV
Output Leakage Current	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1		nA
	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 30\ V_{DC}$			1.0			1.0	μA

Note 1: For operating at temperatures above 25°C, the LM392 and the LM2924 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications apply for $V^+ = 5V$, unless otherwise stated. For the LM392, temperature specifications are limited to $0°C \leq T_A \leq +70°C$ and the LM2924 temperature specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

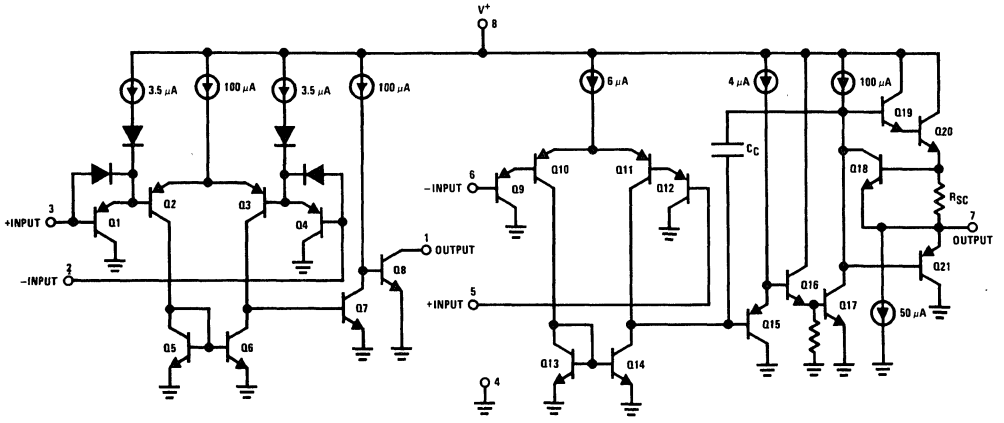
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

Note 8: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 10: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



Comparator A **Amplifier B**

TL/H/7793–2

Application Hints

Please refer to the application hints section of the LM193 and the LM158 datasheets.

National Semiconductor

LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

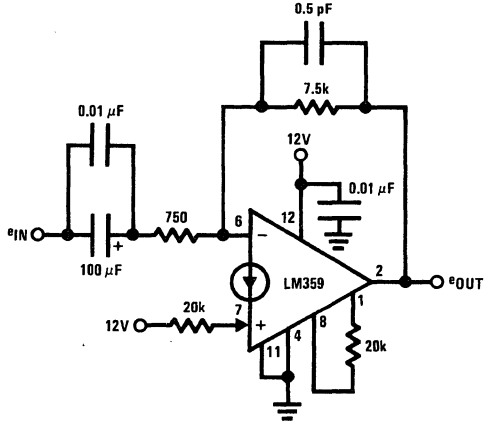
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product (I_{SET} = 0.5 mA)
  400 MHz for A_V = 10 to 100
  30 MHz for A_V = 1
- High slew rate (I_{SET} = 0.5 mA)
  60 V/μs for A_V = 10 to 100
  30 V/μs for A_V = 1
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to V_{CC} − 2V
- Low spot noise, 6 nV/$\sqrt{Hz}$, for f > 1 kHz

Typical Application

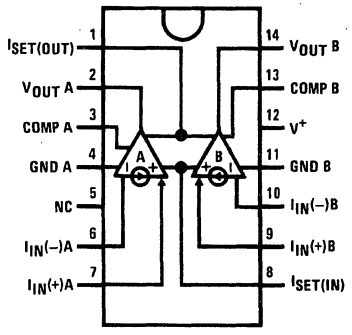


TL/H/7788–1

- A_V = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

Connection Diagram

Dual-In-Line Package



TL/H/7788–2

Top View

Order Number LM359J, LM359M or LM359N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 22 V_{DC} or ±11 V_{DC}

Power Dissipation (Note 1)
- J Package 1W
- N Package 750 mW

Maximum T_J
- J Package +150°C
- N Package +125°C

Thermal Resistance

J Package

θ_{jA} 147°C/W still air
110°C/W with 400 linear feet/min air flow

N Package

θ_{jA} 100°C/W still air
75°C/W with 400 linear feet/min air flow

Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$ 10 mA_{DC}

Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$ 2 mA_{DC}

Operating Temperature Range
- LM359 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 260°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 sec.) 260°C
- Small Outline Package
  - Vapor Phase (60 sec.) 215°C
  - Infrared (15 sec.) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics $I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12$V, $T_A = 25$°C unless otherwise noted

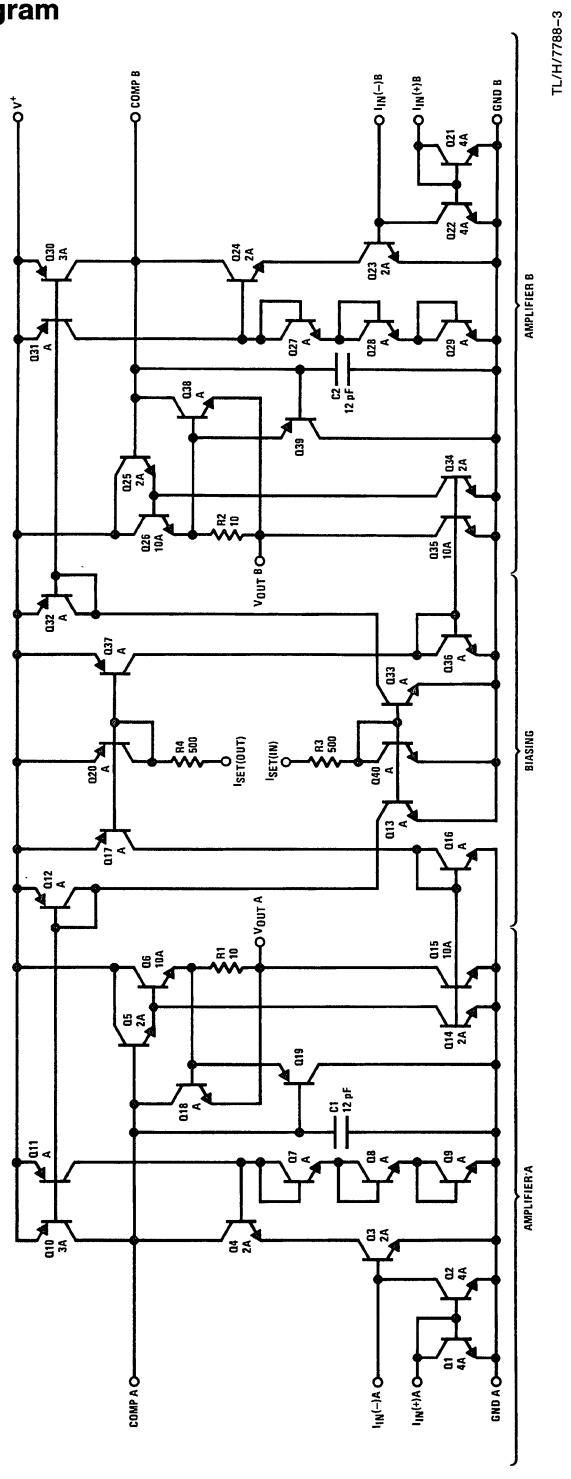
Parameter	Conditions	LM359			Units
		Min	Typ	Max	
Open Loop Voltage Gain	$V_{supply} = 12V$, $R_L = 1k$, f = 100 Hz $T_A = 125°C$	62	72 68		dB dB
Bandwidth Unity Gain	$R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF	15	30		MHz
Gain Bandwidth Product Gain of 10 to 100	$R_{IN} = 50\Omega$ to 200Ω	200	400		MHz
Slew Rate Unity Gain Gain of 10 to 100	 $R_{IN} = 1\ k\Omega$, $C_{comp} = 10$ pF $R_{IN} < 200\Omega$		 30 60		 V/μs V/μs
Amplifier to Amplifier Coupling	f = 100 Hz to 100 kHz, $R_L = 1k$		−80		dB
Mirror Gain (Note 2)	at 2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$, $T_A = 25°C$ at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp. at 20 μA $I_{IN}(+)$, $I_{SET} = 5\ \mu A$ Over Temp.	0.9 0.9 0.9	1.0 1.0 1.0	1.1 1.1 1.1	μA/μA μA/μA μA/μA
ΔMirror Gain (Note 2)	at 20 μA to 0.2 mA $I_{IN}(+)$ Over Temp, $I_{SET} = 5\ \mu A$		3	5	%
Input Bias Current	Inverting Input, $T_A = 25°C$ Over Temp.		8	15 30	μA μA
Input Resistance (βre)	Inverting Input		2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, f = 1 MHz		3.5		Ω
Output Voltage Swing V_{OUT} High V_{OUT} Low	$R_L = 600\Omega$ $I_{IN}(-)$ and $I_{IN}(+)$ Grounded $I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$	9.5	10.3 2	 50	V mV
Output Currents Source Sink (Linear Region) Sink (Overdriven)	 $I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100\Omega$ $V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$ $I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	 16 1.5	 40 4.7 3	 	 mA mA mA
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$		18.5	22	mA
Power Supply Rejection (Note 3)	f = 120 Hz, $I_{IN}(+)$ Grounded	40	50		dB

Note 1: See Maximum Power Dissipation graph.

Note 2: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

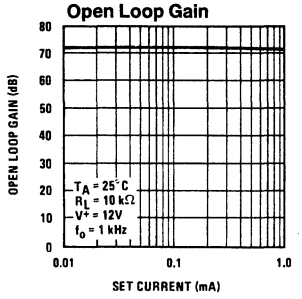
Note 3: See Supply Rejection graphs.

Schematic Diagram

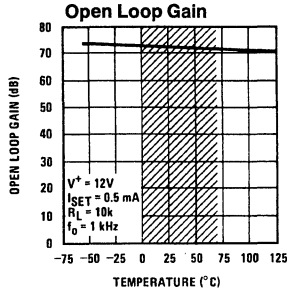


Typical Performance Characteristics

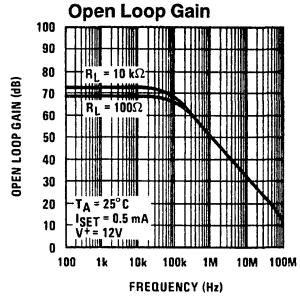
Open Loop Gain



Open Loop Gain

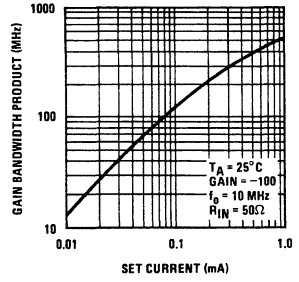


Open Loop Gain

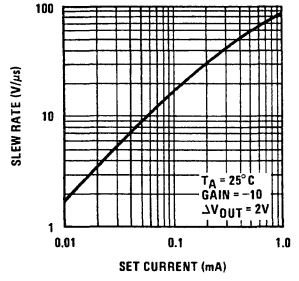


Note: Shaded area refers to LM359

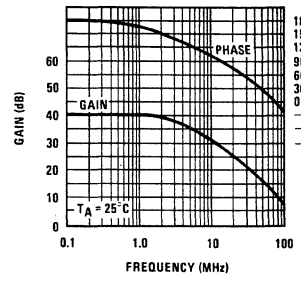
Gain Bandwidth Product



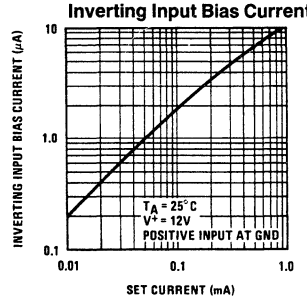
Slew Rate



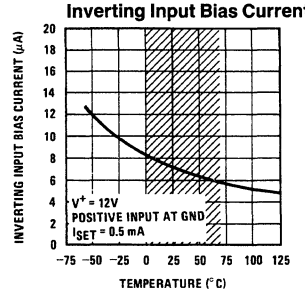
Gain and Phase
Feedback Gain = −100



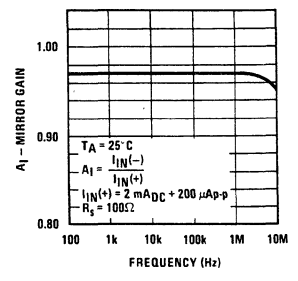
Inverting Input Bias Current



Inverting Input Bias Current

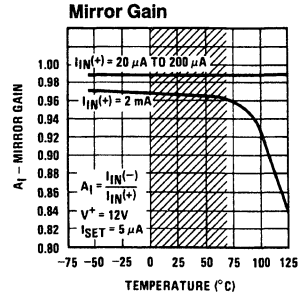


Mirror Gain

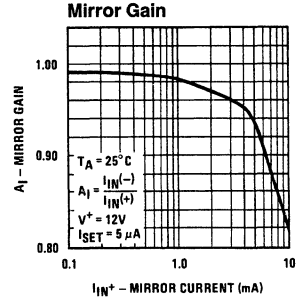


Note: Shaded area refers to LM359

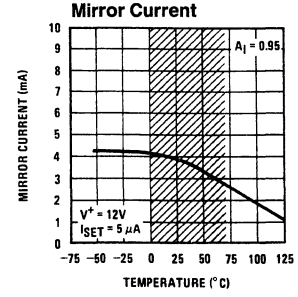
Mirror Gain



Mirror Gain



Mirror Current

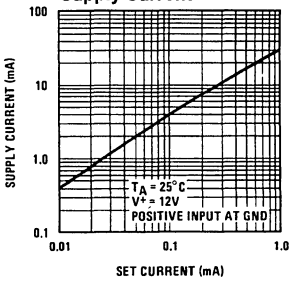


TL/H/7788–4

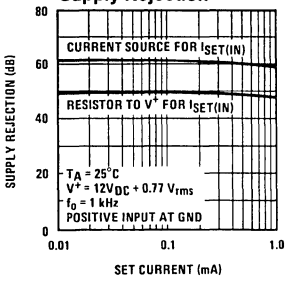
Note: Shaded area refers to LM359

Typical Performance Characteristics (Continued)

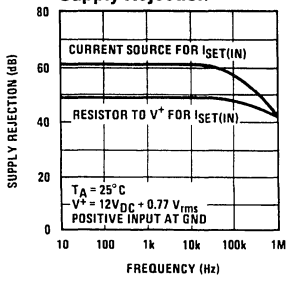
Supply Current



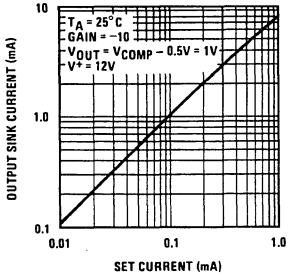
Supply Rejection



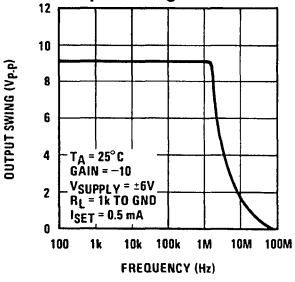
Supply Rejection



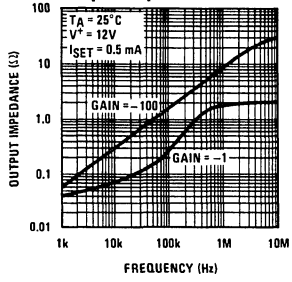
Output Sink Current



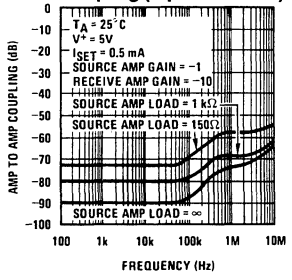
Output Swing



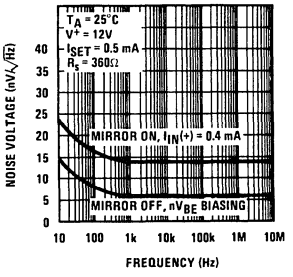
Output Impedance



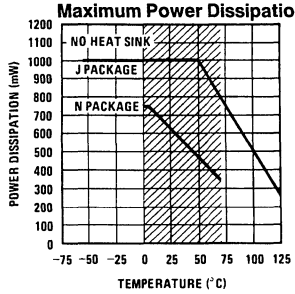
Amplifier to Amplifier Coupling (Input Referred)



Noise Voltage



Maximum Power Dissipation



Note: Shaded area refers to LM359J/LM359N

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Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

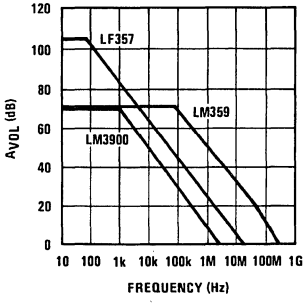

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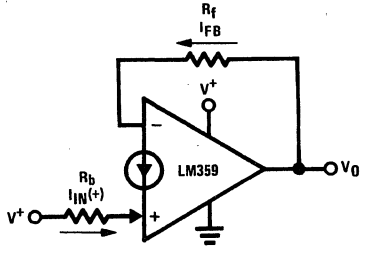
FIGURE 1

Application Hints (Continued)

DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input.* The mirror gain (A_I) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2.*



$$V_{o(DC)} = V_{BE}(-) + I_{FB}\,R_f$$

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$$I_{FB} = I_{IN}(+)\,A_I + I_b(-)$$

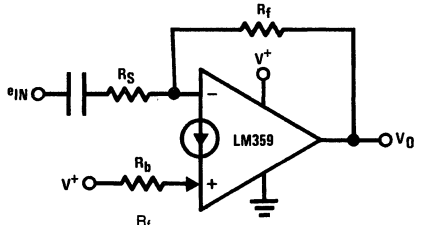
$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

$I_b(-)$ is the inverting input bias current

FIGURE 2

The DC input voltage at each input is a transistor V_{BE} ($\cong$ 0.6 V_{DC}) and must be considered for DC biasing. For most applications, the supply voltage, V^+, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10I_b(-)$.

The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

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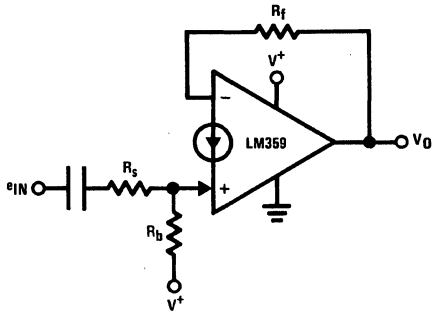
$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

FIGURE 3. Biasing an Inverting AC Amplifier



$$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$$

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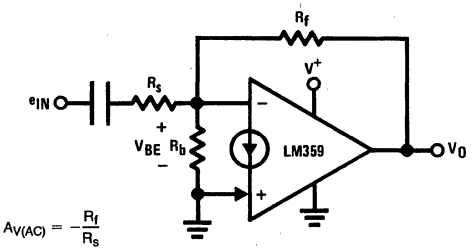
$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

FIGURE 4. Biasing a Non-Inverting AC Amplifier



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$$

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FIGURE 5. nV_{BE} Biasing

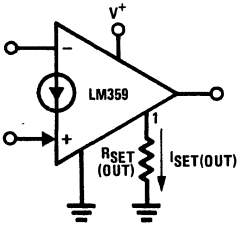
The nV_{BE} biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6*, this current is equal to:



$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

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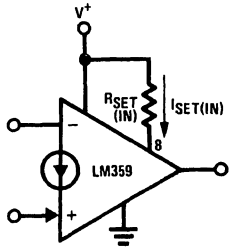
FIGURE 6. Establishing the Output Set Current

Application Hints (Continued)

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$.* This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:



$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

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FIGURE 7. Establishing the Input Set Current

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\, (10^{-6})}{C_{comp}}\ (V/\mu s)$$

$$\text{frequency of dominant pole} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\, (0.026V)}\ (Hz)$$

$$\text{input resistance} = \beta re \cong \frac{150\ (0.026V)}{3 I_{SET(IN)}}\ (\Omega)$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed (KT/q = 26 mV and β_{typ} = 150). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

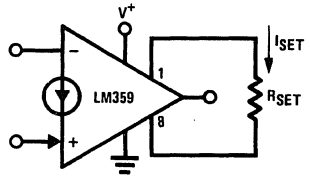
$$I_{supply} \cong 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 *(Figure 8)*.

$$I_{SET} = \frac{V^+ - 2\, V_{BE}}{R_{SET} + 1\ k\Omega} \text{ where } V_{BE} \cong 0.6V$$



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$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

FIGURE 8. Single Resistor Programming of I_{SET}

This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \cong 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

Application Hints (Continued)

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9*.

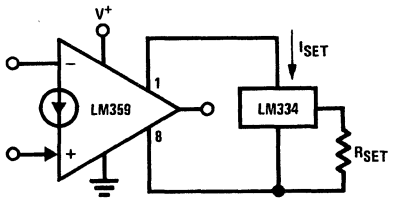


FIGURE 9. Current Source Programming of I_{SET}

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2 ") but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10*.

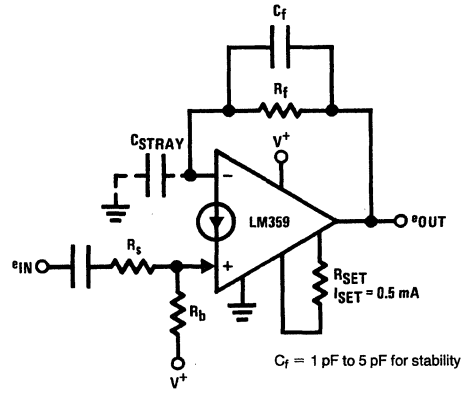


FIGURE 10. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11*. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

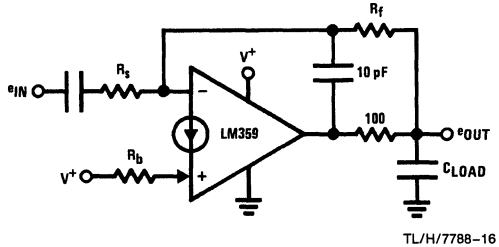


FIGURE 11. Isolating Large Capacitive Loads

Application Hints (Continued)

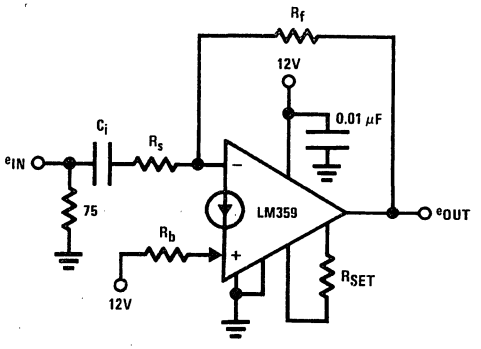
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



TL/H/7788–17

2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\ MHz = 100\ MHz$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

Actual GBW = 10 × 40 MHz = 400 MHz

I_{SET} required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = \frac{10.8V}{0.5\,mA} - 1\,k\Omega = 20.6\,k\Omega$$

3. Determine maximum value for R_f to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3\,I_{SET}}{\beta} = 100\,\mu A \text{ minimum DC feedback current}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$\approx \frac{(V^+ - 3\,V_{BE}) - 2\,mV}{2}$$

$$V_{oDC(opt)} \cong \frac{12 - 1.8V}{2} = \frac{10.2V}{2} = 5.1\,V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE(-)}}{I_{f(MIN)}} = \frac{5.1V - 0.6V}{100\,\mu A} = 45\,k\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select R_s to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega \text{ Let } R_s = 750\Omega$$

5. Select R_f for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10\,R_s = 7.5\,k\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since R_f = 7.5k, for the output to be biased to 5.1 V_{DC}, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1V - V_{BE(-)}}{R_f} = \frac{5.1V - 0.6V}{7.5\,k\Omega} = 600\,\mu A$$

Now R_b can be found by:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{IN}(+)} = \frac{12 - 0.6}{600\,\mu A} = 19\,k\Omega$$

7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

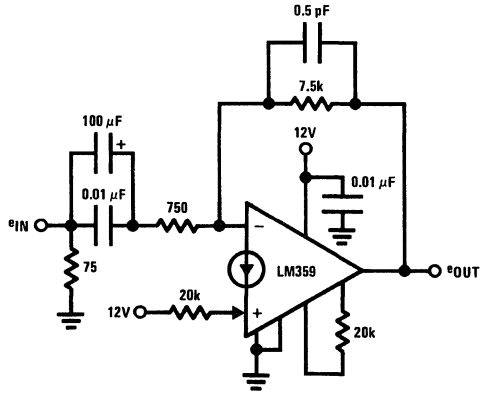
$$C_i \geq \frac{1}{2\pi\,R_s\,(f_{low})} = \frac{1}{2\pi\,(750\Omega)\,(8\,Hz)} = 26\,\mu F$$

A larger value of C_i will allow a flat frequency response down to 8 Hz and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

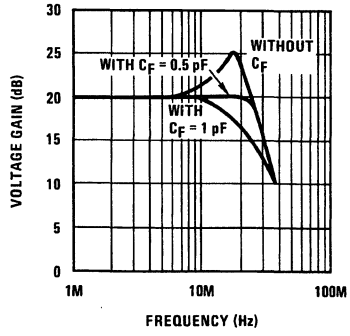
Application Hints (Continued)

Final Circuit Using Standard 5% Tolerance Resistor Values:



TL/H/7788–18

Circuit Performance:



TL/H/7788–19

$V_{O(DC)}$ = 5.1V

Differential phase error < 1° for 3.58 MHz f_{IN}

Differential gain error < 0.5% for 3.58 MHz f_{IN}

$f_{-3\ dB}$ low = 2.5 Hz

A NON-INVERTING VIDEO AMPLIFIER

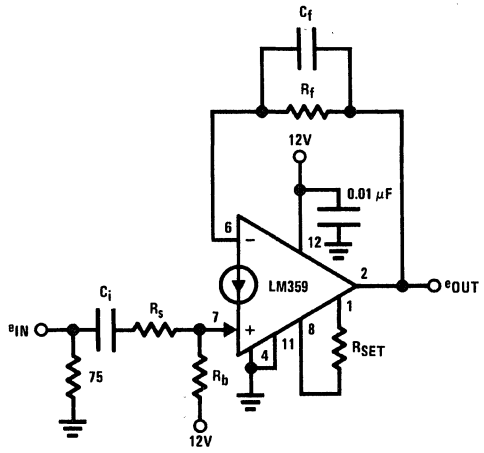
For this case several design considerations must be dealt with.

- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (−) input.

DESIGN EXAMPLE:

e_{IN} = 50 mV (MAX), f_{IN} = 10 MHz (MAX), desired circuit BW = 20 MHz, A_V = 20 dB, driving source impedance = 75Ω, V^+ = 12V.

1. Basic circuit configuration:



TL/H/7788–20

2. Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_f and C_f. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET}:

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = 20.6\,k\Omega$$

3. Since the closed loop bandwidth will be determined by

$$R_f \text{ and } C_f \left(f_{-3\,dB} = \frac{1}{2\pi\, R_f\, C_f} \right)$$

Application Hints (Continued)

to obtain a 20 MHz bandwidth, both R_f and C_f should be kept small. It can be assumed that C_f can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of:

$$\frac{1}{2\pi\ 5\ \text{pF}\ 20\ \text{MHz}} \leq R_f \leq \frac{1}{2\pi\ 1\ \text{pF}\ 20\ \text{MHz}}$$

or $1.6\ \text{k}\Omega \leq R_f \leq 7.96\ \text{k}\Omega$

Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω.
5. For $A_v = 10$; R_f is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4\ V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE(-)}}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640\ \mu A = I_{IN(+)}$$

DC biasing predictability will be insured because 640 μA is greater than the minimum of $I_{SET}/5$ or 100 μA.

For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be;

$$\frac{\pm e_{in\ peak}}{R_s + r_e} = \frac{\pm 50\ \text{mV}}{750\Omega} = \pm 66\ \mu A$$

therefore the total mirror current range will be 574 μA to 706 μA which will insure gain accuracy.

8. R_b can now be found:

$$R_b = \frac{V^+ - V_{BE}(+)}{I_{IN}(+)} = \frac{12 - 0.6}{640\ \mu A} = 17.8\ \text{k}\Omega$$

9. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\ I_{IN(+)}} = \frac{26\ \text{mV}}{640\ \mu A} \cong 40\Omega\ \text{at}\ 25°C$$

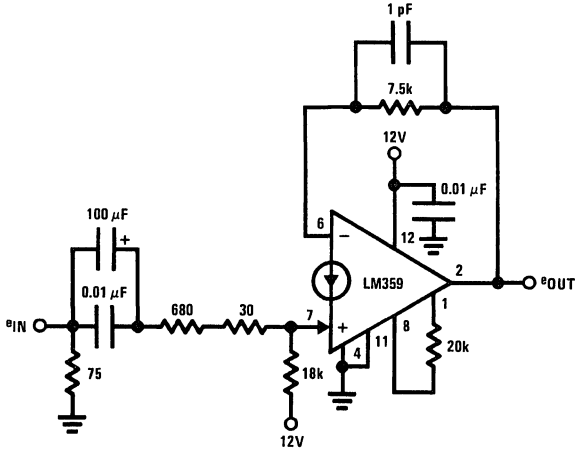
R_s must be 750Ω−40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

10. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\ (R_s + r_e)\ f_{low}} = \frac{1}{2\pi\ (750\Omega)\ (8\ \text{Hz})} = 26.5\ \mu F$$

A larger value may be used and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

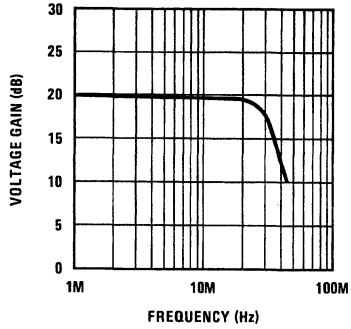
Final Circuit Using Standard 5% Tolerance Resistor Values



TL/H/7788–21

Application Hints (Continued)

Circuit Performance



TL/H/7788–22

$V_{o(DC)}$ = 5.4V
Differential phase error < 0.5°
Differential gain error < 2%
$f_{-3\ dB}$ low = 2.5 Hz

GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

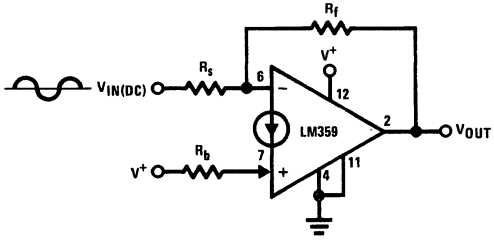
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET}, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure

Typical Applications

DC Coupled Inputs

Inverting

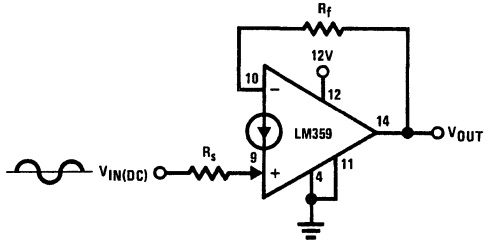


TL/H/7788–23

$$V_{o(DC)} = \left[\frac{V^+ - V_{BE(+)}}{R_b} - \frac{V_{IN(DC)} - V_{BE(-)}}{R_s}\right] R_f + V_{BE(-)}$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

Non-Inverting



TL/H/7788–24

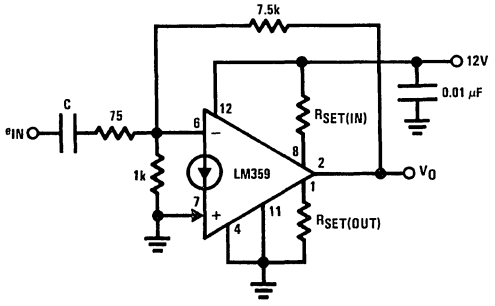
$$V_{o(DC)} = V_{BE(-)} + \frac{(V_{IN(DC)} - V_{BE(+)}) R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_{e(+)}}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

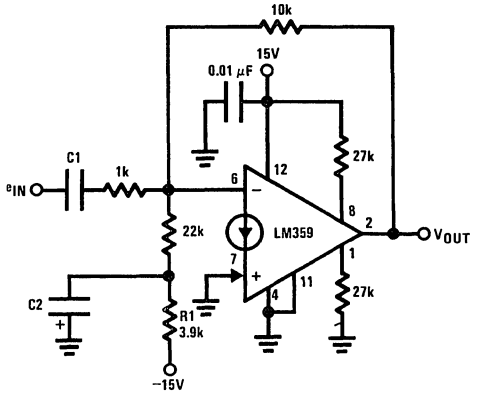
Application Hints (Continued)

Noise Reduction using nV_{BE} Biasing



TL/H/7788–25

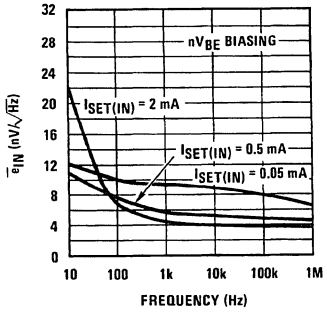
nV_{BE} Biasing with a Negative Supply



TL/H/7788–26

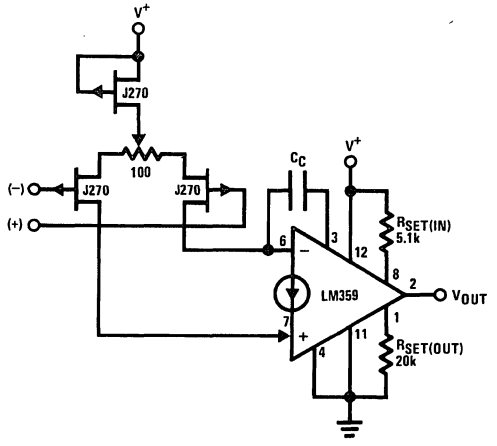
- R1 and C2 provide additional filtering of the negative biasing supply

Typical Input Referred Noise Performance



TL/H/7788–27

Adding a JFET Input Stage

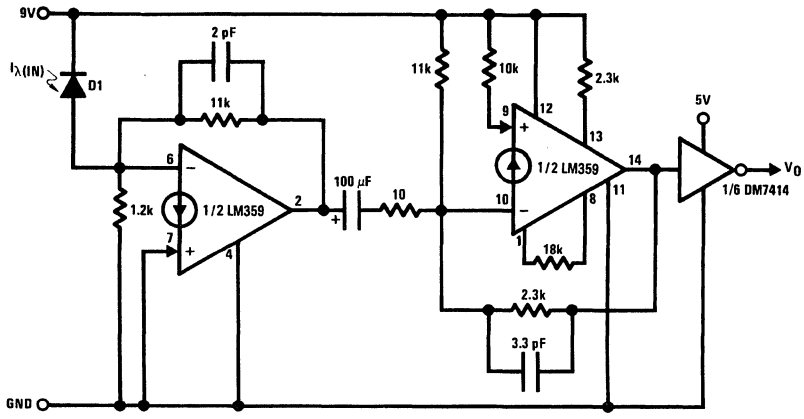


TL/H/7788–28

- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, $S_r = 60\ V/\mu s$; $C_C = 51$ pF
- For $A_V = +11$; BW = 24 MHz, $S_r = 130\ V/\mu s$; $C_C = 5$ pF
- For $A_V = +100$; BW = 4.5 MHz, $S_r = 150\ V/\mu s$; $C_C = 2$ pF
- V_{OS} is typically <25 mV; 100Ω potentiometer allows a V_{OS} adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

Typical Applications (Continued)

Photo Diode Amplifier

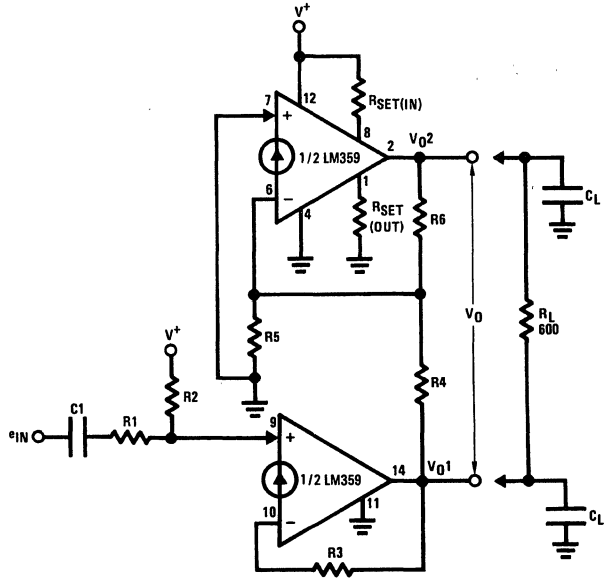


TL/H/7788–29

D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- T_{PDL} = 45 ns, T_{PDH} = 50 ns − T^2L output

Balanced Line Driver



TL/H/7788–30

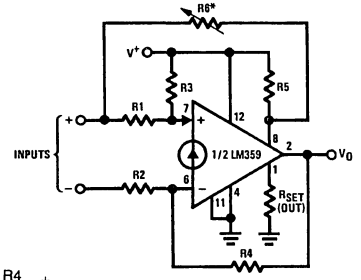
For $V_o1 = V_o2 = \frac{V^+}{2}$, $\frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive C_L = 1500 pF with no additional compensation, ±0.01 μF with C_{comp} = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Typical Applications (Continued)

Difference Amplifier



TL/H/7788-31

$$V_{O(DC)} = \frac{R4}{R3}(V^+ - \phi) \text{ where } \phi = 0.6V$$

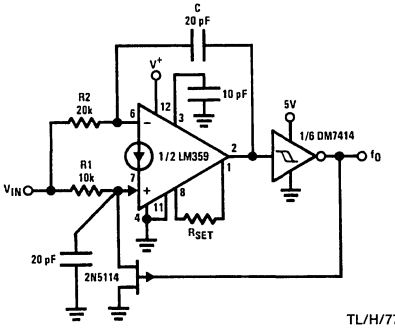
$$A_V = \frac{R4}{R1} \text{ for } R1 = R2$$

*CMRR is adjusted for max at expected CM input signal

$$R6 \approx \frac{R5}{5}, \text{ for } R5 = 100\ k\Omega$$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Voltage Controlled Oscillator



TL/H/7788-32

$$f_O = \frac{V_{IN} - \phi}{4\,C\Delta V\,R1}$$

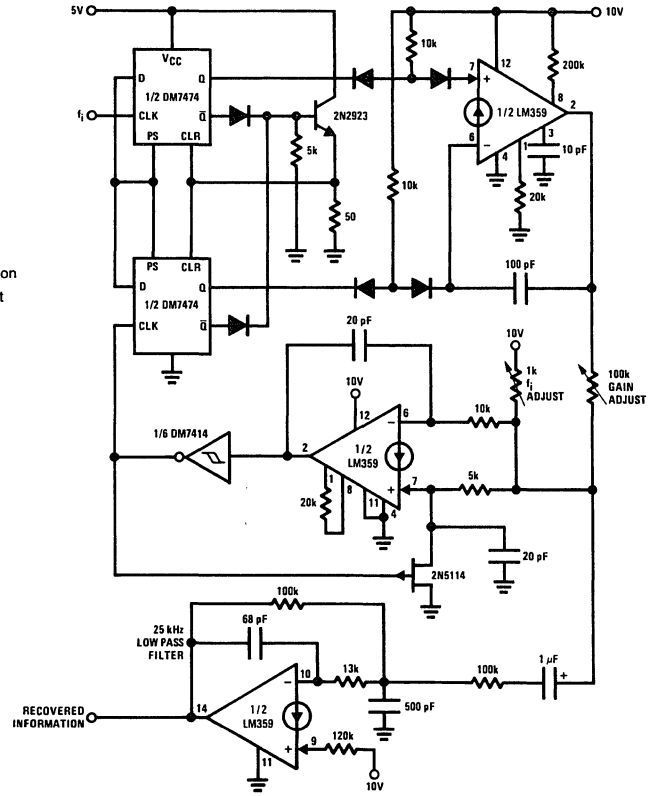
where: R2 = 2R1

ϕ = amplifier input voltage = 0.6V

ΔV = DM7414 hysteresis, typ 1V

- 5 MHz operation
- T^2L output

Phase Locked Loop



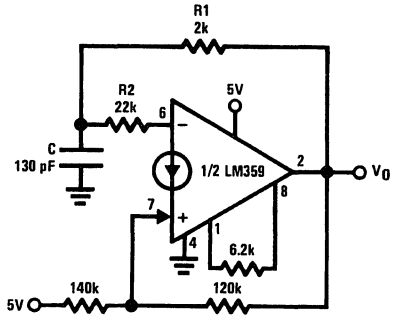
- Up to 5 MHz operation
- T^2L compatible input

All diodes = 1N914

TL/H/7788-33

Typical Applications (Continued)

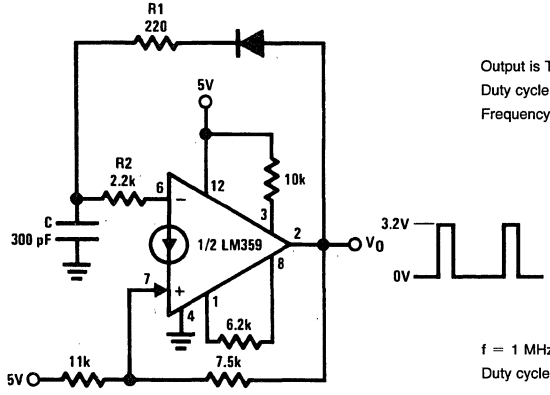
Squarewave Generator



TL/H/7788–34

f = 1 MHz
Output is TTL compatible
Frequency is adjusted by R1 & C (R1 ≪ R2)

Pulse Generator

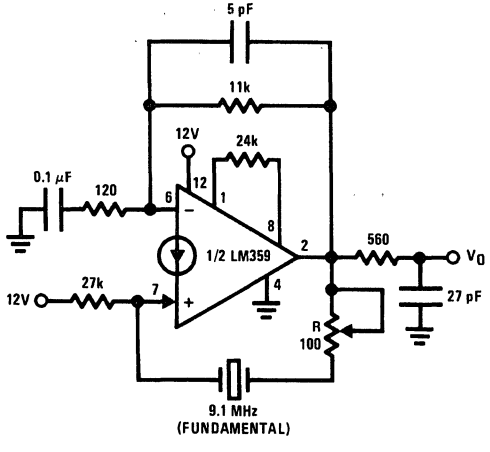


Output is TTL compatible
Duty cycle is adjusted by R1
Frequency is adjusted by C

f = 1 MHz
Duty cycle = 20%

TL/H/7788–36

Crystal Controlled Sinewave Oscillator

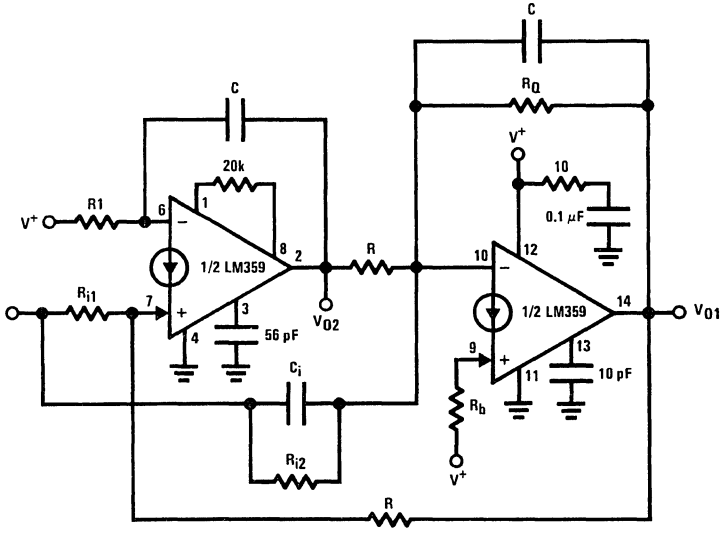


V_o = 500 mVp-p
f = 9.1 MHz
THD < 2.5%

TL/H/7788–37

Typical Applications (Continued)

High Performance 2 Amplifier Biquad Filter(s)



TL/H/7788–35

- The high speed of the LM359 allows the center frequency Q_o product of the filter to be: $f_o \times Q_o \leq 5$ MHz
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

DC Biasing Equations for $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+/2$

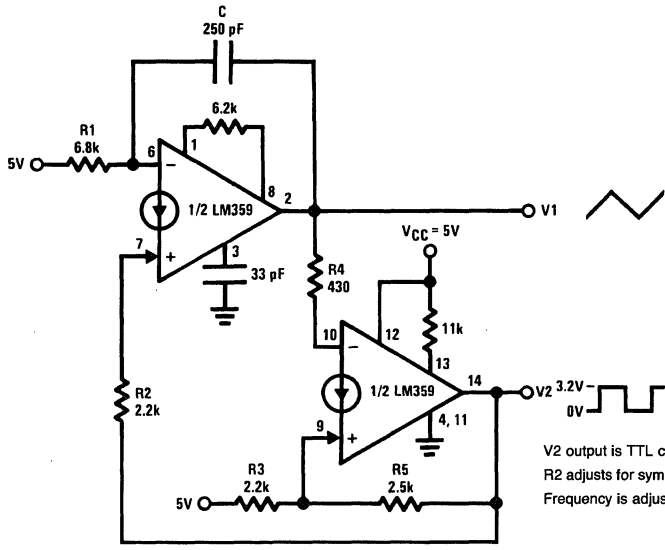
Type I	$\frac{2\,V_{IN(DC)}}{V^+\,(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; $\frac{1}{R1} = \frac{V_{IN(DC)}}{V^+\,(R_{i1})} + \frac{1}{2R}$

Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	$f_{Z(notch)}$	$H_{o(LP)}$	$H_{o(BP)}$	$H_{o(HP)}$	$H_{o(BR)}$
I	BP	LP	O	R_{i2}	∞	$\frac{1}{2}\pi RC$	R_Q/R	—	R/R_{i2}	R_Q/R_{i2}	—	—
II	HP	BP	C_i	∞	∞	$\frac{1}{2}\pi RC$	R_Q/R	—	—	R_QC_i/RC	C_i/C	—
III	Notch/ BR	—	C_i	∞	R_{i1}	$\frac{1}{2}\pi RC$	R_Q/R	$\frac{1}{2}\pi\sqrt{RR_iCC_i}$	—	—	—	$H_o\Big\vert_{f \to \infty} = C_i/C$ $H_o\Big\vert_{f \to O} = C/R_i$

Typical Applications (Continued)

Triangle Waveform Generator



V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

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National Semiconductor

LM604A/LM604 4 Channel Mux-Amp

General Description

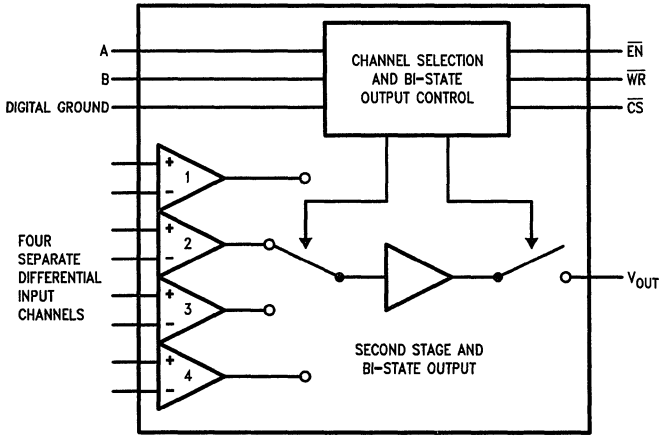
The LM604 Mux-Amp is an op-amp with four selectable differential inputs, combining the functions of a multiplexer with an op-amp. The LM604 can select, buffer, and amplify one of four different input signals, providing a complete system for multiplexing analog signals. It also has the unique Bi-State output which allows two or more Mux-Amps to be connected together at their outputs to increase the number of multiplexed channels. Channel selection and the Bi-State output are controlled by internal logic that interfaces directly to a microprocessor. Besides these unique features, the LM604 has excellent AC and DC op-amp specifications and is internally compensated.

Applications include signal multiplexing and linear circuits that are controlled by digital signals (i.e., programmable gain blocks, filters, and other op-amp circuits).

Features

- Multiplexes four differential input channels to a single op-amp
- Easy to interface to microprocessor, or operates "stand alone"
- Bi-State output: Operates in two states, Active and Disabled. When disabled, it becomes a high impedance.
- Wide operating voltage range
  - single supply: 4V to 32V
  - split supply: ±2V to ±16V
- Wide input common mode range: V^- to $V^+ - 1V$
- Fast channel to channel switching time: 5 μs
- Output will drive a 600Ω load

Block Diagram



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Channel Selection

A	B	$\overline{WR}$	$\overline{CS}$	Channel
0	0	0	0	1
0	1	0	0	2
1	0	0	0	3
1	1	0	0	4
X	X	X	1	Unchanged
X	X	1	X	Unchanged

Bi-State Output Control

$\overline{EN}$	$\overline{WR}$	$\overline{CS}$	Output State
0	0	0	Enabled
1	0	0	Disabled, High Z
X	X	1	Unchanged
X	1	X	Unchanged

Order Number LM604AMJ, LM604IJ, LM604IN, LM604ACN, LM604CN, LM604ACM, or LM604CM
See NS Package Number J18A, N18A or M20B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V or ±18V
Differential Input Voltage	±Supply Voltage
Input Voltage Range	±Supply Voltage
Output Short Circuit to Gnd	Continuous (Note 1)
ESD Tolerance (C_{ZAP} = 120 pF, R_{ZAP} = 1500Ω)	2,000V
Lead Temperature (Soldering, 5 sec.)	300°C
Storage Temperature Range	−65°C to 150°C

Operating Ambient Temperature Range	
LM604AM	$-55°C \le T_A \le 125°C$
LM604I	$-40°C \le T_A \le 85°C$
LM604AC, LM604C	$0°C \le T_A \le 70°C$

	J Pkg.	M Pkg.	N Pkg.
Power Dissipation (Note 2)	1,600 mW	1,500 mW	1,900 mW
T_{JMAX}	150°C	150°C	150°C
θ_{JA} (Typical, Board Mounted)	75°C/W	83°C/W	65°C/W

DC Electrical Characteristics V_{SUPPLY} = ±15V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage (V_{OS})	R_S = 10 kΩ	LM604	1.0			3.0	**5.0**	3.0	**5.0**	mV
		LM604A	0.5	1.0				1.0	**3.0**	(Max)
				3.0						
V_{OS} Temperature Drift			5.5							µV/°C
Input Offset Current (I_{OS})			2	10		10	**12**	10	**12**	nA
				12						(Max)
I_{OS} Temperature Drift			10							pA/°C
Input Bias Current (I_B)		LM604	50			80	**100**	80	**100**	nA
		LM604A	30	50				50	**60**	(Max)
				60						
I_B Temperature Drift			55							pA/°C
Input Common Mode Voltage Range		Upper Limit	14.0	13.5		13.5	**13.0**	13.5	**13.0**	V
				13.0						(Min)
		Lower Limit	−15.0	−15.0		−15.0	**−15.0**	−15.0	**−15.0**	V
				−15.0						(Max)
Input Resistance			1.0							Meg Ω
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	13.4	13.0		13.0	**12.5**	13.0	**12.5**	V
				12.5						(Min)
		Lower Limit	−14.2	−13.8		−13.8	**−13.3**	−13.8	**−13.3**	V
				−13.3						(Max)
	R_L = 600Ω	Upper Limit	12.7	12.3		12.3	**10.0**	12.3	**10.0**	V
				10.0						(Min)
		Lower Limit	−12.6	−12.2		−12.2	**−11.7**	−12.2	**−11.7**	V
				−11.7						(Max)
Large Signal Voltage Gain	V_{OUT} = ±10V	R_L = 2 kΩ	200	50		50	**25**	50	**25**	V/mV
				25						(Min)
		R_L = 600Ω	200	50		50	**25**	50	**25**	
				25						
Common Mode Rejection Ratio	V_{CM} = −15.0V to 13.5V		100	80		80	**70**	80	**70**	dB
				70						(Min)

DC Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 3)

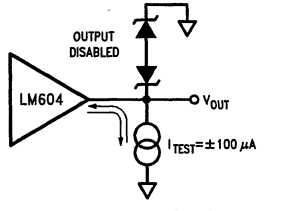
Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 5.0V$ to $\pm 16.0V$	100	80 **70**		80	**70**	80	**70**	dB (Min)
Output Short Circuit Current		±35	±50 **±60**		±50	**±60**	±50	**±60**	mA (Max)
Output Leakage Current	$V_{OUT} = -13.5V$ to 13.0V Bi-State Output Disabled	4.0	10.0 **20.0**		10.0	**20.0**	10.0	**20.0**	µA (Max)
Output Capacitance	Bi-State Output Disabled See *Figure 1*	10							pF
Supply Current		7.0	9.0 **10.0**		9.0	**10.0**	9.0	**10.0**	mA (Max)

AC Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 3)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	$A_V = 1$, $R_L = 2 k\Omega$	3.0	2.0 **1.5**		2.0	**1.5**	2.0	**1.5**	V/µs (Min)
Gain Bandwidth Product	f = 100 kHz	7.0	6.0 **3.0**		6.0	**3.0**	6.0	**3.0**	MHz (Min)
Unity Gain Frequency		3.0		2.5		2.5		2.5	MHz (Min)
Phase Margin	$R_L = 2 k\Omega$, $C_L = 200$ pF	50							Degrees
Settling Time to 0.1% of Final Value	$A_V = -1$, $V_{OUT} = -5.0V$ to 5.0V $R_L = 2 k\Omega$	4.0							µs
Channel Switching Time	See *Figure 2* t_{SW1}	4.0	5.5 **6.5**		5.5	**6.5**	5.5	**6.5**	µs (Max)
	t_{SW2}	5.0		6.5		6.5		6.5	
Channel to Channel Isolation	$R_S = 10 k\Omega$, f = 10 kHz $V_{IN} = 10.0V_{p-p}$	100							dB
Input Noise Voltage	$R_S = 100\ \Omega$, f = 1 kHz	20							$nV/\sqrt{Hz}$
Input Noise Current	f = 1 kHz	0.3							$pA/\sqrt{Hz}$
Mux-Amp Enable Time	See *Figure 3* t_{EN1}	3.0	4.0 **5.0**		4.0	**5.0**	4.0	**5.0**	µs (Max)
	t_{EN2}	4.0		5.5		5.5		5.5	
Mux-Amp Disable Time (t_{DIS})	See *Figure 3*	1.0	2.0 **3.0**		2.0	**3.0**	2.0	**3.0**	µs (Max)

DC Electrical Characteristics V_{SUPPLY} = 5V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage	R_S = 10 kΩ V_{OUT} = 2.0V	LM604 LM604A	1.0 0.5	 1.0 **3.0**		3.0	**5.0**	3.0 1.0	**5.0** **3.0**	mV (Max)
Input Offset Current	V_{OUT} = 2.0V		3.0	10 **18**		10	**18**	10	**18**	nA (Max)
Input Bias Current	V_{OUT} = 2.0V	LM604 LM604A	70 50	 80 **110**		130	**150**	130 80	**150** **110**	nA (Max)
Input Common Mode Voltage Range	V_{OUT} = 2.0V	Upper Limit	4.0	3.5 **3.0**		3.5	**3.0**	3.5	**3.0**	V (Min)
		Lower Limit	0	0 **0**		0	**0**	0	**0**	
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	3.5	3.2 **3.0**		3.2	**3.0**	3.2	**3.0**	V (Min)
		Lower Limit	0.5	0.7 **0.8**		0.7	**0.8**	0.7	**0.8**	V (Max)
	R_L = 600Ω	Upper Limit	3.3	3.0 **2.8**		3.0	**2.8**	3.0	**2.8**	V (Min)
		Lower Limit	0.4	0.6 **0.7**		0.6	**0.7**	0.6	**0.7**	V (Max)
Large Signal Voltage Gain	V_{OUT} = 0.8V to 2.8V	R_L = 2 kΩ	200		50 **25**		50 **25**		50 **25**	V/mV (Min)
		R_L 600Ω	200		50 **25**		50 **25**		50 **25**	
Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)
Power Supply Rejection Ratio	V^+ = 4.0V to 5.0V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)



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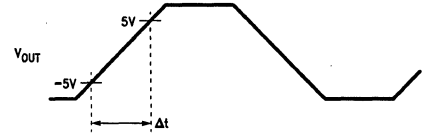

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$$C_{OUT} = \frac{\Delta t}{10V} \times 100\ \mu A$$

FIGURE 1. Output Capacitance Test

Digital Input Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 6)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
V_{INHI}			1.8 **2.0**		1.8	**2.0**	1.8	**2.0**	V (Min)
V_{INLO}			1.0 **0.8**		1.0	**0.8**	1.0	**0.8**	V (Max)
I_{INHI}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
I_{INLO}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
Minimum Pulse Width for WR & CS				**100**		**100**		**100**	ns (Min)
Minimum Set-Up Time (t_S)	See *Figures 3* and *5*			**100**		**100**		**100**	ns (Min)
Minimum Hold Time (t_H)	See *Figures 3* and *5*			**50**		**50**		**50**	ns (Min)
Input Capacitance		5							pF

Note 1: Applies to both single and split supply operation. Continuous short circuit operation can result in exceeding the maximum allowed junction temperature.

Note 2: When operating at $T_A > 25°C$, the maximum power dissipation must be derated based on θ_{JA}.

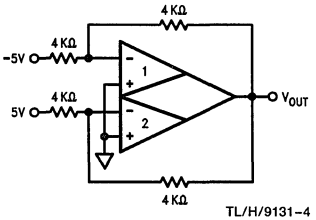
Note 3: Unless specified otherwise, all limits are guaranteed for $T_A = T_J = 25°C$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1Meg\Omega$. **Boldface** limits apply at $0°C \leq T_J \leq 70°C$ for LM604AC and LM604C, $-40°C \leq T_J \leq 85°C$ for LM604I, and $-55°C \leq T_J$ 125°C for LM604AM.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed but not 100% production tested. These numbers are not used to calculate outgoing quality levels.

Note 6: Unless specified otherwise, all units are guaranteed at $T_A = T_J = 25°C$. **Boldface** limits apply at the junction temperature extremes specified in note 3. Input voltage levels are with respect to digital ground (pin 4) which must be at least 4.0V below V^+.

Switching from Channel 1 to 2 with Channel Select preset to $\overline{AB}$ before $\overline{WR}$ = 0. This test applies to all channels.



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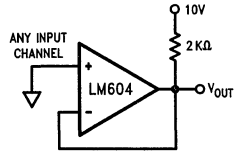

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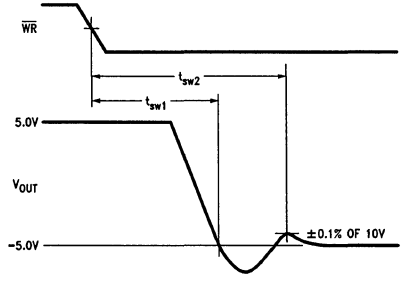

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FIGURE 2. Channel Switching Time Test

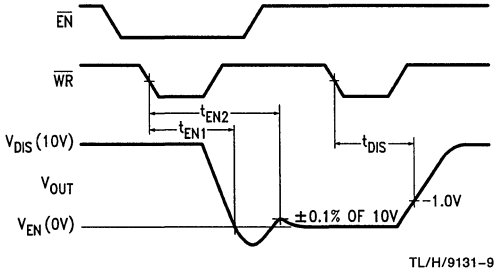

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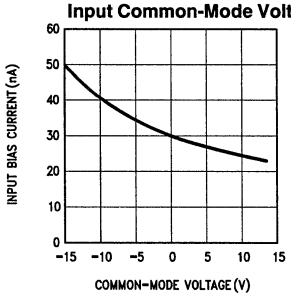
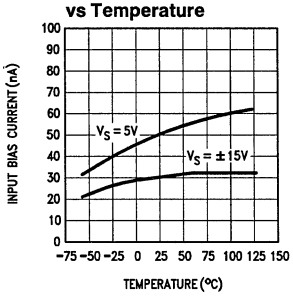
FIGURE 3. Bi-State Output Enable and Disable Time Test

Typical Performance Characteristics (Note 7)

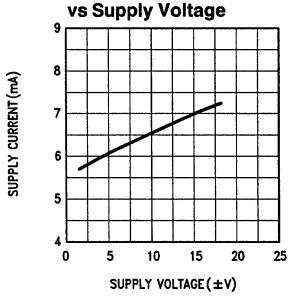
Input Bias Current vs Input Common-Mode Voltage



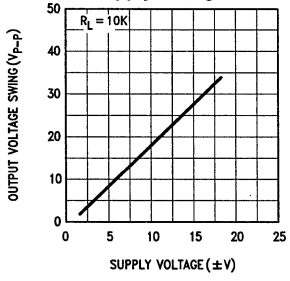
Input Bias Current vs Temperature



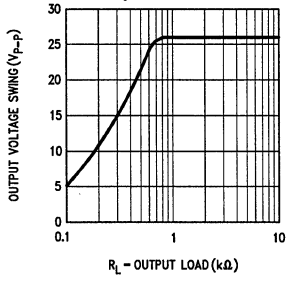
Supply Current vs Supply Voltage



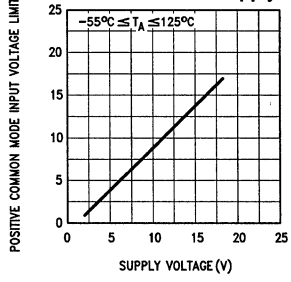
Output Voltage Swing vs Supply Voltage



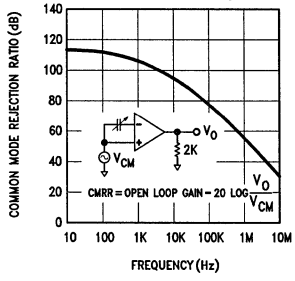
Output Voltage Swing vs Output Load Resistance



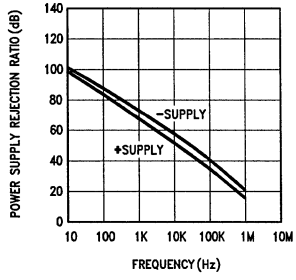
Upper Common-Mode Voltage Limit vs Positive Supply Voltage



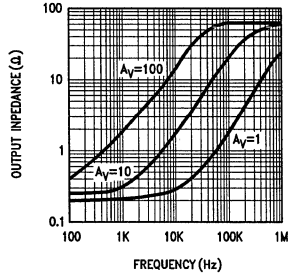
Common-Mode Rejection Ratio vs Frequency



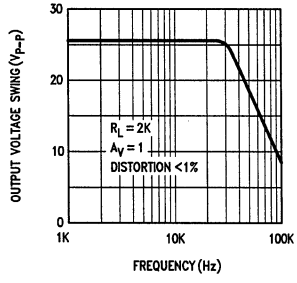
Power Supply Rejection Ratio vs Frequency



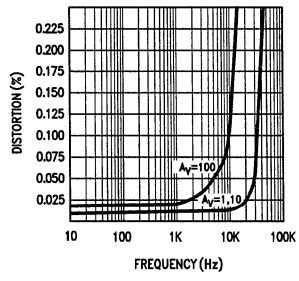
Output Impedance vs Frequency



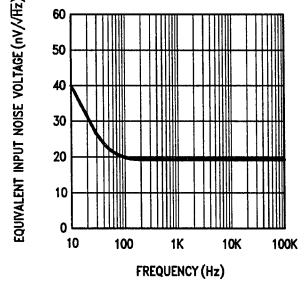
Undistorted Output Voltage Swing vs Frequency



Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



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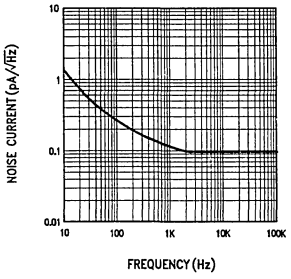
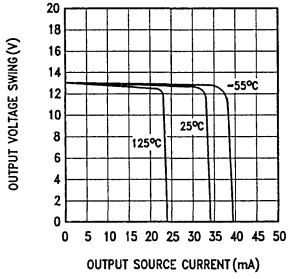
Typical Performance Characteristics (Note 7)

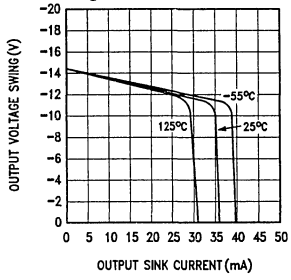
Equivalent Input Noise Current vs Frequency



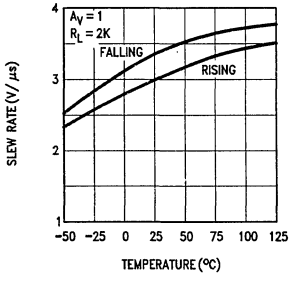
Positive Current Limit



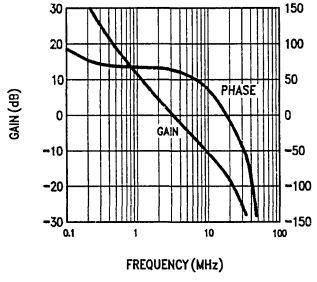
Negative Current Limit



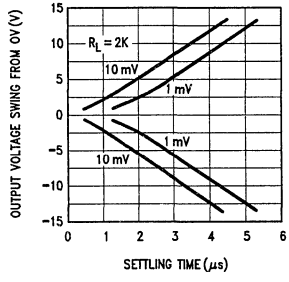
Slew Rate vs Temperature



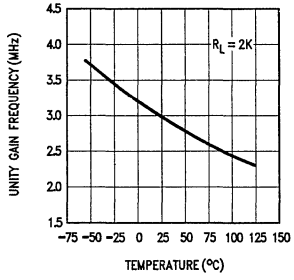
Bode Plot



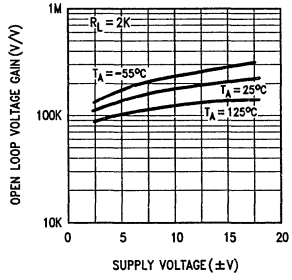
Inverter Settling Time vs Output Voltage Swing



Unity Gain Frequency vs Temperature



Open Loop Voltage Gain

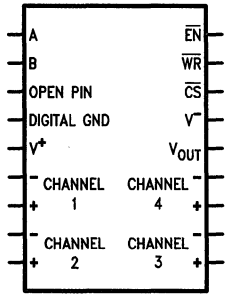


TL/H/9131–7

Note 7: Unless specified otherwise, $T_A = T_J = 25°C$, $V_S = \pm 15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1$ Meg.

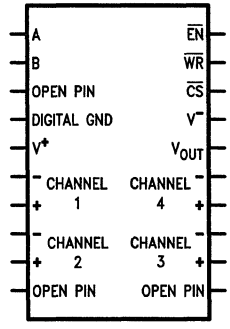
Connection Diagrams

18 Pin Dual-In-Line Package



TL/H/9131–25

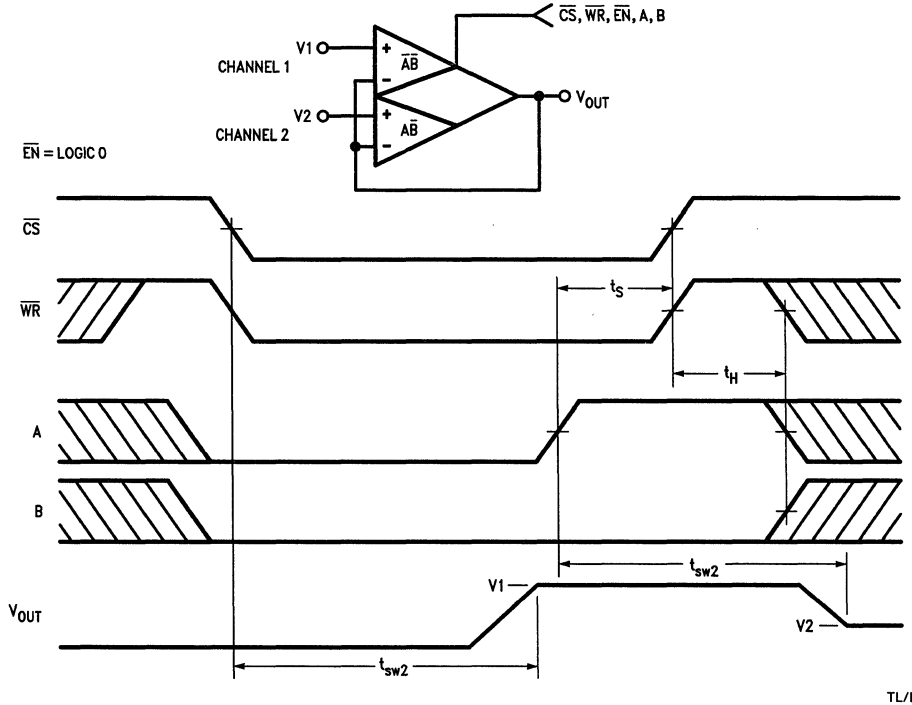
20 Pin Small Outline Package



TL/H/9131–26

FIGURE 4

Timing Diagrams



TL/H/9131–11

FIGURE 5. Channel Switching Timing Diagram

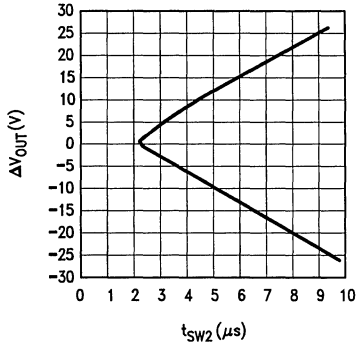
Functional Description

INPUT CHANNEL SELECTION

The LM604 contains four differential input channels that are selected one at a time. An input is selected by writing its binary code to pins A and B when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram. The LM604 always has one of its inputs selected. In order to isolate all four channels from the output, the Bi-State output can be disabled.

Figure 5 illustrates how the LM604 switches from one channel to another. The switching begins on the falling edge of $\overline{WR}$ if A and B are valid before $\overline{WR}$ is a logic 0, or when A and B become valid while $\overline{WR}$ is a logic 0. In either case, the channel switching time (t_{SW2}) remains the same. If a channel is to remain selected, its binary code must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H.

Channel switching time is specified by t_{SW1} and t_{SW2} as shown in *Figure 2*. t_{SW1} is the time it takes the output to first reach its new value, and t_{SW2} is the time it takes the output to settle to within 0.1% of its new value. Clearly, t_{SW2} is a more useful parameter for specifying switching time, but it is difficult to test on a production basis. Therefore, t_{SW1} is tested and this allows t_{SW2} to be guaranteed. Channel switching time will vary as a function of how far the output swings to reach its new value. This is shown in *Figure 6* where t_{SW2} is plotted as a function of output voltage swing (ΔV_{OUT}).



TL/H/9131–12

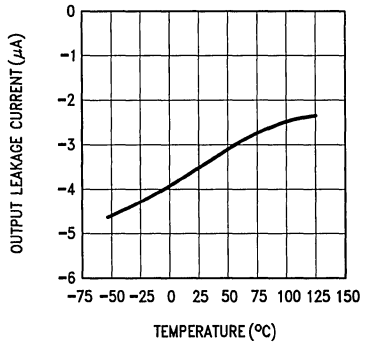
$\Delta V_{OUT} = V_{OUT}$ (Selected Channel) $- V_{OUT}$ (Previous Channel)

FIGURE 6. t_{SW2} vs ΔV_{OUT}

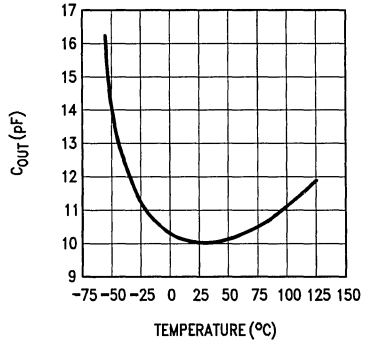
BI-STATE OUTPUT

The Bi-State output can be either enabled (on) or disabled (off). When disabled, the output becomes a high impedance load that can be driven by another output stage. This allows several Mux-Amps to be connected together at their outputs by having only one output enabled at one time. Thus, several Mux-Amps can be in parallel to the same output to increase the number of multiplexed channels. The Bi-State output is controlled by $\overline{EN}$ when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram.

When the output is disabled and driven by another output, it behaves like a small capacitive load with a few microamps of leakage current. The data sheet specifies this with the parameters "Output Capacitance" and "Output Leakage Current". Both parameters vary with temperature, as shown in *Figure 7*.



TL/H/9131–13



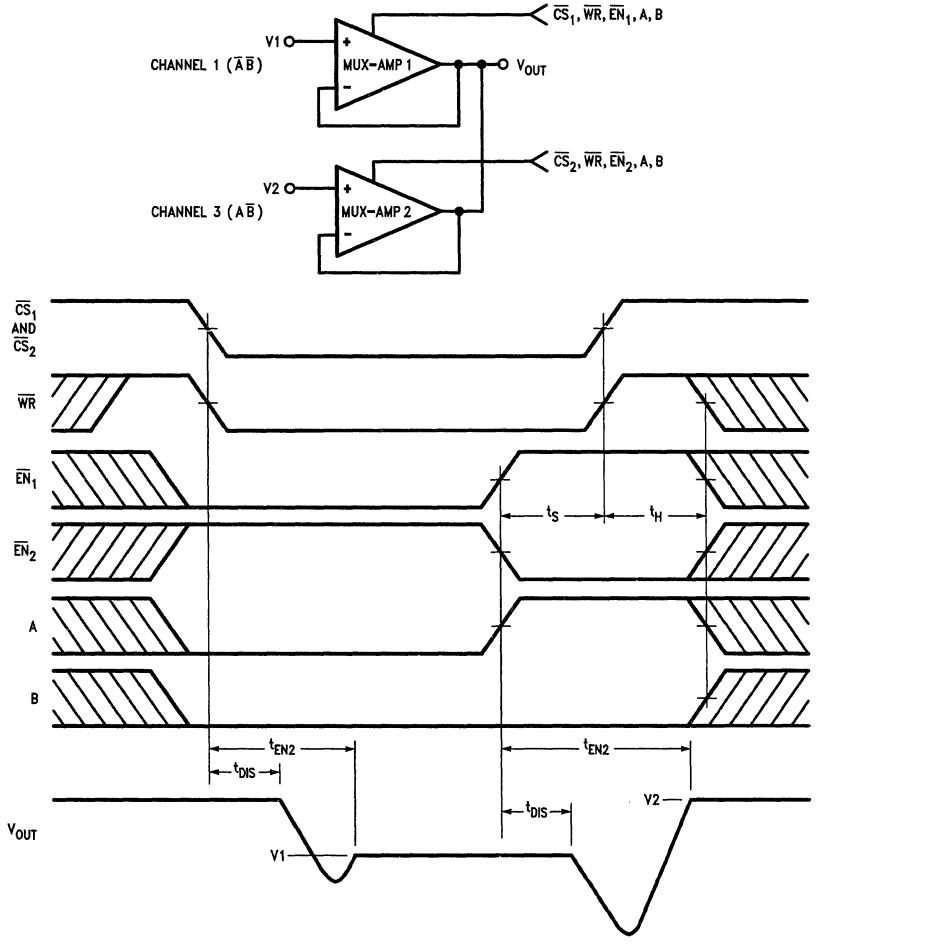
TL/H/9131–14

FIGURE 7. $I_{LEAKAGE}$ and C_{OUT} vs Temperature

Figure 8 illustrates switching between two Mux-Amps that are connected in parallel to the same output. Switching begins on the falling edge of $\overline{WR}$ if the $\overline{EN}$ signals are correctly set before $\overline{WR}$ is a logic 0, or when the $\overline{EN}$ signals become valid while $\overline{WR}$ is a logic 0. The Bi-State output takes less time to become disabled than it does to become enabled, and this insures the outputs are switched in a "break before make" method. If an in output is to remain enabled or disabled after $\overline{WR}$ becomes a logic 1, $\overline{EN}$ must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H. Note that when a Mux-Amp has its output enabled, the binary code for the selected input channel must also be written.

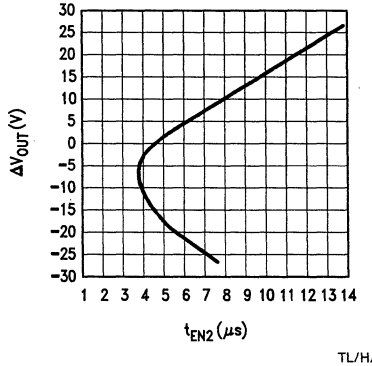
Bi-State output enable time (t_{EN1} and t_{EN2}) and disable time (t_{DIS}) are defined in *Figure 3*. t_{EN1} is the time it takes the output to first reach its enabled value (V_{EN}), and t_{EN2} is the time it takes the output to settle to within 0.1% of V_{EN}. As with channel switching time, t_{EN1} is a tested parameter that allows t_{EN2} to be guaranteed. t_{DIS} is the time it takes the output to become a high impedance. Output enable time will vary according to how far the output swings from V_{DIS} to V_{EN}, and this is plotted in *Figure 9*.

Functional Description (Continued)



TL/H/9131–15

FIGURE 8. Timing Diagram for Switching Bi-State Outputs



TL/H/9131–16

$\Delta V_{OUT} = V_{EN} - V_{DIS}$

FIGURE 9. t_{EN2} vs ΔV_{OUT}

DIGITAL CONTROL

As mentioned in the previous sections, the input channels and Bi-State output are controlled by logic levels on pins A, B, and $\overline{EN}$. There are two ways to apply logic levels to these pins. 1) Hardwire $\overline{WR}$ and $\overline{CS}$ directly to digital ground so that the LM604 operates in a "stand alone" mode. This allows input logic levels to directly control the LM604. 2) Write digital signals to A, B, and $\overline{EN}$ as shown in the timing diagrams of *Figures 5* and *8*. This method is used when the LM604 interfaces to a microprocessor. Note that $\overline{CS}$ and $\overline{WR}$ can occur simultaneously, so set-up and hold times are not required for $\overline{CS}$. Also, notice that $\overline{WR}$ must remain a logic 1 during the hold time period.

Input logic levels are referenced to a 1.4V threshold voltage, making the LM604 compatible with TTL and CMOS logic. This threshold voltage is referenced to digital ground. The voltage level of digital ground can be as low as V^- (pin 15) and as high as 4V below V^+ (pin 5).

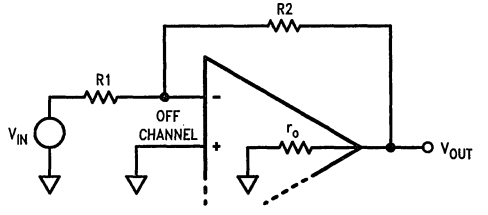
Application Hints

USING MULTIPLE FEEDBACK LOOPS

Each input channel of the LM604 is used as a single op-amp with its own feedback loop. Two examples of this are circuits with multiple inverting gain channels and non-inverting gain channels (*Figure 10*). These circuits have multiple feedback loops connected to the same output with one feedback loop connected to a selected channel and the others connected to "off" channels. The feedback loop of the selected channel determines the gain of these circuits. The off channel feedback loops affect these circuits in two ways. 1) They create an additional load at the output. 2) Feedback loops for inverting gain channels provide feedthrough paths from the inputs of the off channels to the output.

In *Figure 10*, the loading affect of multiple feedback loops is given in terms of current flowing through the feedback loops (I_F). In circuits with non-inverting gain channels, I_F is a function of V_{OUT} and the resistance of the feedback loops. In circuits with inverting gain channels, I_F is different for each channel selected because it is also a function of the off channel input voltages. This additional loading must be accounted for when designing Mux-Amp circuits. Otherwise, the output load resistance will be less than anticipated.

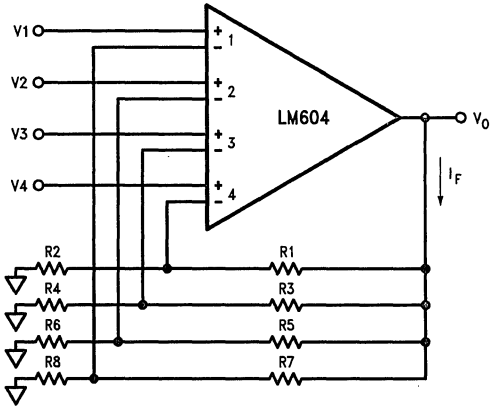
Figure 11 illustrates feedthrough in an off inverting gain channel. Feedthrough occurs because the feedback resistors and the Mux-Amp output impedance (r_o) form a voltage divider. This divider allows a portion of the off channel's input signal to appear at the output. The amount of signal that feeds through depends on the ratio of output impedance to feedback loop resistance. Output impedance varies according to Mux-Amp gain (gain of the selected channel) and the frequency of the feedthrough signal. This variation must be considered when calculating feedthrough, and it is plotted in the "Typical Device Characteristics" section.



TL/H/9131–17

$$V_{OUT} = V_{IN}\left(\frac{r_o}{R1 + R2 + r_o}\right)$$

FIGURE 11. Inverting Gain Channel Feedthrough

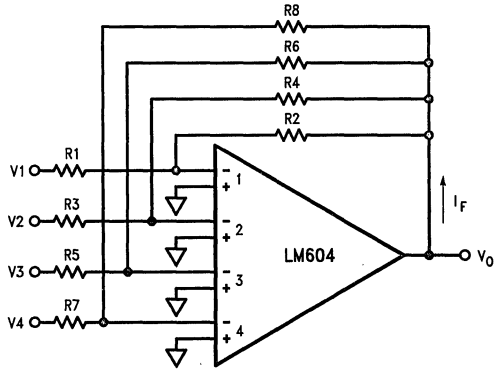


TL/H/9131–19

Channel	V_o
1	$V1\left(1 + \frac{R7}{R8}\right)$
2	$V2\left(1 + \frac{R5}{R6}\right)$
3	$V3\left(1 + \frac{R3}{R4}\right)$
4	$V4\left(1 + \frac{R1}{R2}\right)$

$$I_F = V_o\left(\frac{1}{R1 + R2} + \frac{1}{R3 + R4} + \frac{1}{R5 + R6} + \frac{1}{R7 + R8}\right)$$

Multiple Non-Inverting Gain Channels



TL/H/9131–18

Channel	V_o	I_F
1	$-V1\left(\frac{R2}{R1}\right)$	$\frac{V_o}{R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V3}{R5 + R6} + \frac{V_o - V4}{R7 + R8}$
2	$-V2\left(\frac{R4}{R3}\right)$	$\frac{V_o}{R4} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V3}{R5 + R6} + \frac{V_o - V4}{R7 + R8}$
3	$-V3\left(\frac{R6}{R5}\right)$	$\frac{V_o}{R6} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V4}{R7 + R8}$
4	$-V4\left(\frac{R8}{R7}\right)$	$\frac{V_o}{R8} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V3}{R5 + R6}$

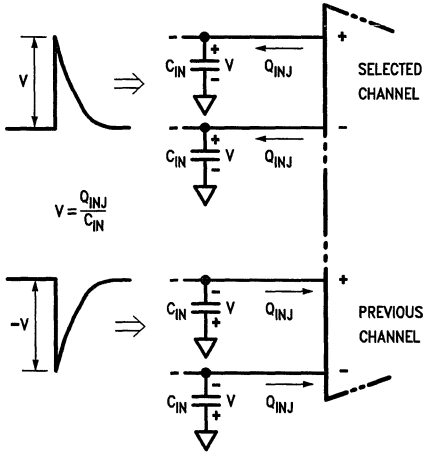
Multiple Inverting Gain Channels

FIGURE 10. Circuits Using Multiple Inverting and Non-Inverting Gain Channels

Application Hints (Continued)

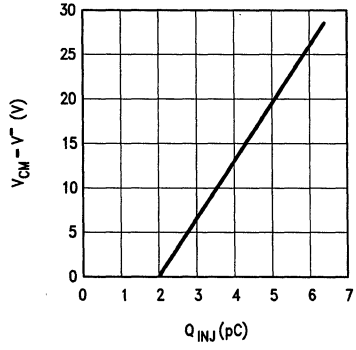
INPUT CHARGE INJECTION

When the Mux-Amp switches channels, charge is injected from the inputs of the selected and previous channels, see *Figure 12*. This causes a positive error voltage at the input of the selected channel and a negative voltage at the previous channel. The amplitude of this error voltage equals Q_{INJ}/C_{IN}, where C_{IN} is the total capacitance at the input and Q_{INJ} is the charge injected. As plotted in *Figure 13*, Q_{INJ} increases proportionally with the difference in voltage between a channel's input common mode voltage and the negative supply. The RC time constant of C_{IN} times resistance seen from the input will determine how long the error voltage remains at the input.



TL/H/9131–20

FIGURE 12. Error Voltage From Input Charge Injection



TL/H/9131–21

FIGURE 13. Q_{INJ} vs $V_{CM} - V^-$

MAXIMUM OUTPUT LOAD CONDITIONS

The Mux-Amp is guaranteed to drive a 600Ω load as specified over its entire operating range. Reducing the load resistance below this value may cause the output to current limit. It may also cause the junction temperature limit to be exceeded when operating the part near its maximum ambient temperature.

The Mux-Amp is unconditionally stable with as much as 500 pF connected from the output to ground. If the output is required to drive a larger capacitive load, the Mux-Amp may need to operate with at least a gain of 10. Otherwise, it may become unstable when sinking current.

DIGITAL FEEDTHROUGH

When interfacing the Mux-Amp to a microprocessor, pins A, B, $\overline{EN}$, and $\overline{WR}$ are connected to an address bus where high frequency digital signals are present. The fast edges of these signals can propagate into the Mux-Amp's analog signal path, causing fast transients to appear at the output. To avoid this problem, the following precautions should be taken.

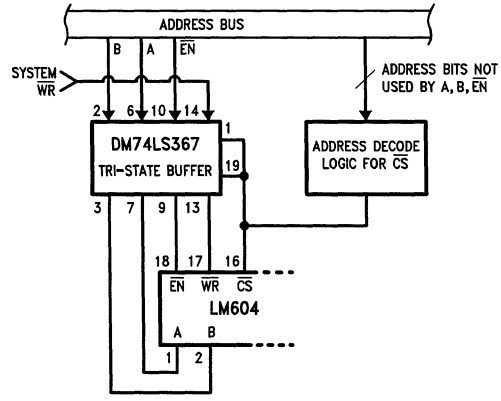
1) Analog and digital ground must be kept separate. They can only be connected together back at the power supply or supply bus.

2) Bypass capacitors should have low inductance to prevent noise spikes on the voltage supply pins. A ceramic disc capacitor of 0.1 μF is usually sufficient.

3) All lead lengths should be kept short to prevent them from picking up digital signals.

By using these rules, digital signals can be attenuated at the input channels by typically 100 dB.

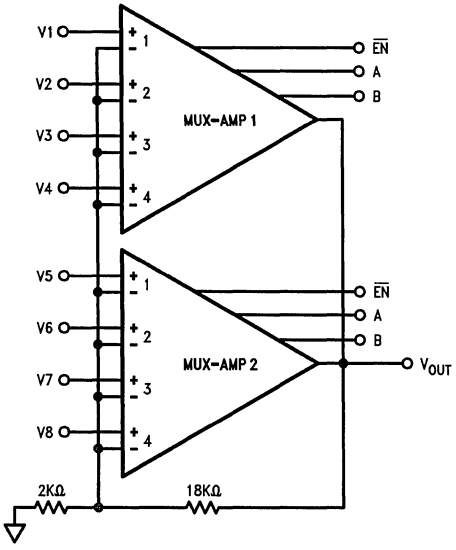
Lab measurements have shown a minimum digital feedthrough signal of 2 mV occurs at the output even when the best layout precautions are taken. This is fine for many applications, but to completely eliminate digital feedthrough, any signals coming directly from the bus must be sent to the Mux-Amp via a Tri-State buffer, see *Figure 14*. This isolates the Mux-Amp's digital pins from the address bus to prevent pin to pin feedthrough. CS can be used to enable the Tri-State buffers when signals are sent to the Mux-Amp from the address bus.



TL/H/9131–22

FIGURE 14. Isolating Mux-Amp from Address Bus by Using a Tri-State Buffer

Typical Applications



Mux-Amp 1			Mux-Amp 2			Input
A	B	$\overline{EN}$	A	B	$\overline{EN}$	
0	0	0	X	X	1	V1
0	1	0	X	X	1	V2
1	0	0	X	X	1	V3
1	1	0	X	X	1	V4
X	X	1	0	0	0	V5
X	X	1	0	1	0	V6
X	X	1	1	0	0	V7
X	X	1	1	1	0	V8

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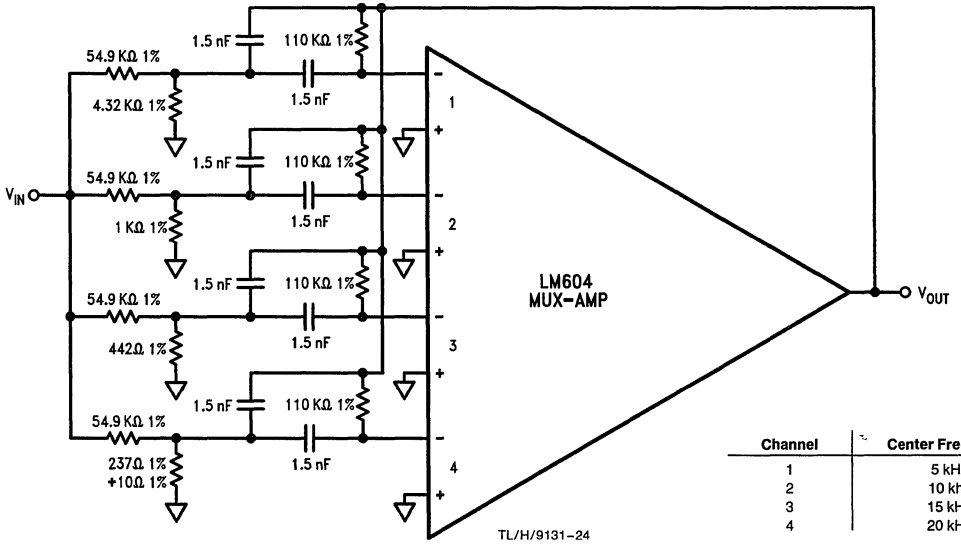
Eight Channel Multiplexer and Amplifier with a Gain of 10



Channel	Center Frequency
1	5 kHz
2	10 khz
3	15 kHz
4	20 kHz

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Programmable Bandpass Filter: Each channel has a 2 kHz bandwidth and a gain of 1 at the center frequency

National Semiconductor

LM607/LM607A/LM607B Precision Operational Amplifier

General Description

The LM607 series of precision operational amplifiers are trimmed at wafer sort to extremely low values of offset voltage. Advanced circuit design and testing techniques allow guaranteed drift specifications as low as 0.3 μV/°C with offsets as low as 25 μV.

Other input parameters are equally impressive. The typical open loop voltage gain of 5 Million yields extremely low error in high-gain applications. CMRR and PSRR are typically 140 dB.

Using Super-Beta transistors in the front end enables the LM607 to operate at high input stage current while maintaining low values of input bias current (1 nA typ.) This gives the part its low input voltage noise: 6.5 nV/√Hz.

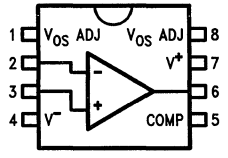
High operating currents also help give the LM607 its high gain-bandwidth product of 1.8 MHz and slew rate of 0.7V/μs. Despite its higher speed, the LM607 draws less supply current than OP-07 and OP-77 types: only 1 mA at ±15V supplies.

Features

■ Low V_{OS}	LM607A:	25 μV max
■ Low drift	LM607A:	0.3 μV/°C max
■ Drift *100% tested:*	A and B grades	
■ High gain	LM607A:	5 million min
■ High CMRR	LM607A:	124 dB min
■ High PSRR	LM607A:	120 dB min
■ Low noise		6.5 nV/√Hz @ 1 kHz 7.2 nV/√Hz @ 10 Hz
■ High speed		1.8 MHz gain-bandwidth 0.7V/μs slew rate
■ Low supply current		1 mA
■ Wide input common mode range		±13.5V
■ Wide supply range		±3V to ±18V
■ Overcompensation		Allows driving high C_L

Connection Diagrams

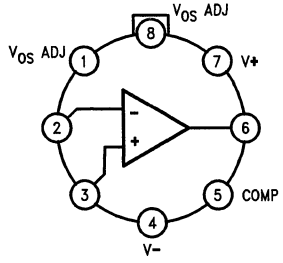
Cerdip and Molded DIP



TL/H/8787–10

Top View

TO-99 Metal Package



TL/H/8787–11

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM607AMH LM607BMH	LM607ACH LM607BCH LM607CH	H08C
8-Pin Cerdip	LM607AMJ LM607BMJ	LM607ACJ LM607BCJ LM607CJ	J08A
8-Pin Molded DIP		LM607ACN LM607BCN LM607CN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Overdrive Current (Note 7)	±25 mA
Supply Voltage	44V
Input Voltage	Supply Voltage
Output Short Circuit to Gnd	Continuous
Power Dissipation (Note 9)	500 mW
Maximum Junction Temperture	150°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance C_{ZAP} = 100 pF R_{ZAP} = 1.5 kΩ	2000V

Operating Rating

Temperature Range (Note 9)	
LM607AM/LM607BM	$-55°C \le T_J \le +125°C$
LM607C/LM607AC/LM607BC	$0°C \le T_J \le +70°C$

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AM		LM607BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **80**		60 **120**		μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**		μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2					μV/mo Max
Input Bias Current		1	2 **4**		3 **6**		nA Max
Input Offset Current		0.5	2 **4**		2.8 **5.6**		nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5	μV p-p Max
Input Noise Voltage Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	 10 	18 8	 10 	nV/√Hz Max
Input Noise Current	0.1 to 10 Hz	14					pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12					pA/√Hz Max
Input Resistance	Differential Mode Common Mode	2 100					MΩ GΩ
Input Voltage Range		±13.5	±13 **±12.5**		±13 **±12.5**		V Min
Common-Mode Rejection Ratio	V_{CM} = ±13V **V_{CM} = ±12.5V**	140	124 **120**		116 **112**		dB Min
Power Supply Rejection Ratio	V_S = ±3V to ±18V (Note 8)	140	120 **117**		114 **112**		dB Min
Large-Signal Voltage Gain	V_O = ±10V $R_L \ge 2$ kΩ $R_L \ge 1$ kΩ	10000 5000	5000 **2000** 1500		2000 **1500** 1000		V/mV Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AM		LM607BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Output Voltage Swing	$R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	±13.8	±13 **±12.5** ±12.5		±13 **±12.5** ±12.5		V Min
Slew Rate		0.7		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0	MHz Min
Open-Loop Output Resistance		50					Ω
Supply Current		1	1.5 **2.0**		1.5 **2.0**		mA Max
Offset Adjust Range		1.5					mV

Electrical Characteristics All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **40**		60 **90**		150	**250**	μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**			**2.5**	μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2							μV/mo Max
Input Bias Current		1	2	**4**	3	**6**	10	**14**	nA Max
Input Offset Current		0.5	2	**4**	2.8	**5.6**	6	**10**	nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5		0.5	μV p-p Max
Input Voltage Noise Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	 10 	18 8	 10 	20 11.5	 13.5 	$nV/\sqrt{Hz}$ Max
Input Noise Current	0.1 to 10 Hz	14							pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12							$pA/\sqrt{Hz}$ Max
Input Resistance	Differential Mode Common Mode	2 100							MΩ GΩ
Input Voltage Range		±13.5	±13	**±12.5**	±13	**±12.5**	±13	**±12.5**	V Min
Common-Mode Rejection Ratio	V_{CM} = ±13V **V_{CM} = ±12.5 V**	140	124	**120**	116	**112**	110	**108**	dB Min
Power Supply Rejection Ratio	V_S = ±3V to ±18V (Note 8)	140	120	**117**	114	**112**	110	**108**	dB Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Large-Signal Voltage Gain	$V_O = \pm 10V$ $R_L \geq 2\,k\Omega$ $R_L \geq 1\,k\Omega$	10000 5000	5000 1500	**2000**	2000 1000	**1500**	1500 1000	**1000**	V/mV Min
Output Voltage Swing	$R_L \geq 2\,k\Omega$ $R_L \geq 1\,k\Omega$	±13.8	±13 ±12.5	**±12.5**	±13 ±12.5	**±12.5**	±12.5 ±12	**±12**	V Min
Slew Rate		0.7		0.4		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0		1.0	MHz Min
Open-Loop Output Resistance		50							Ω
Supply Current		1	1.5	**2.0**	1.5	**2.0**	1.8	**2.2**	mA Max
Offset Adjust Range		1.5							mV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 3 μV settling out in 5 minutes. The LM607C offset voltage is measured by automated test equipment within 200 ms of applying power.

Note 3: Input offset voltage drift is defined as $[V_{OS}(70°C) - V_{OS}(-5°C)]/75°C$ for the commercial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $[V_{OS}(25°C) - V_{OS}(-55°C)]/80°C$ and $[V_{OS}(125°C) - V_{OS}(25°C)]/100°C$.

Note 4: Input offset voltage long term stability refers to the average trend line of V_{OS} vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2 μV.

Note 5: Guaranteed and 100% production tested.

Note 6: Limits at temperature extremes are guaranteed via correlation using Standard Statistical Quality Control (SQC) Methods. All limits are to be used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

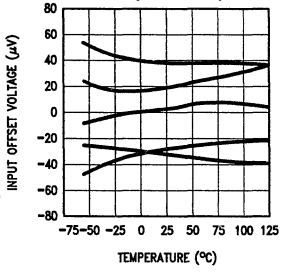
Note 8: Power Supply Rejection Ratio is tested by moving both power supplies together from their minimum to maximum values.

Note 9: Typical thermal resistance of the molded package is 95°C/W junction-to-ambient. Typical thermal resistance of the metal can package is 150°C/W junction-to-ambient and 17°C/W junction-to-case.

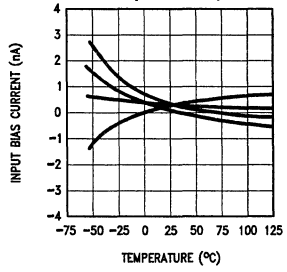
Note 10: These units selected to illustrate the type of variations that may be encountered. (This note refers to particular curves within the Typical Performance Characteristics.)

Typical Performance Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$ unless otherwise indicated

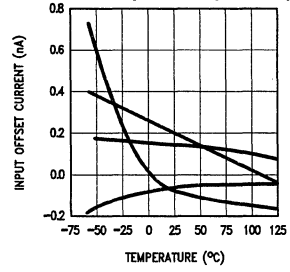
Input Offset Voltage of 5 Representative Units vs Temperature (Note 10)



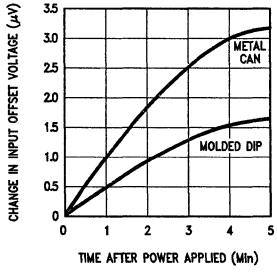
Input Bias Current of 4 Representative Units vs Temperature (Note 10)



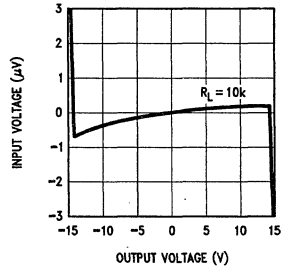
Input Offset Current of 4 Representative Units vs Temperature (Note 10)



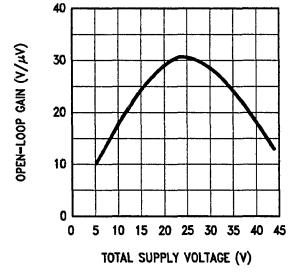
Warmup Drift



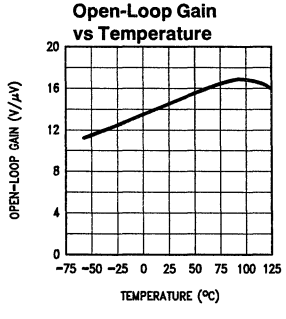
Input Voltage vs Output Voltage



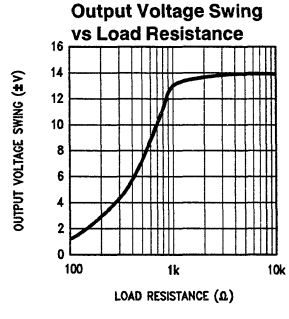
Open-Loop Gain vs Supply Voltage



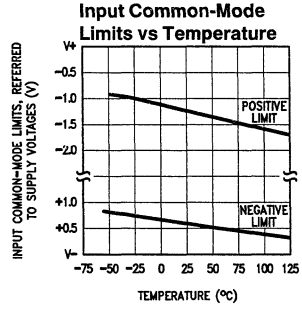
Open-Loop Gain vs Temperature



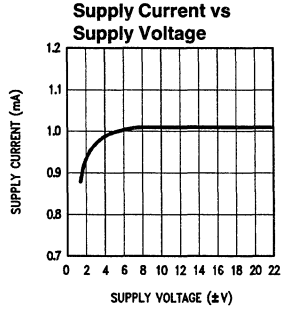
Output Voltage Swing vs Load Resistance



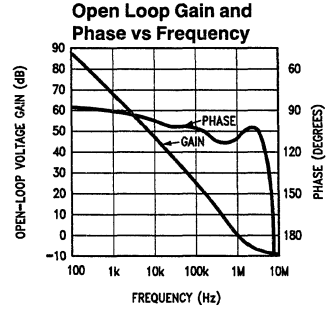
Input Common-Mode Limits vs Temperature



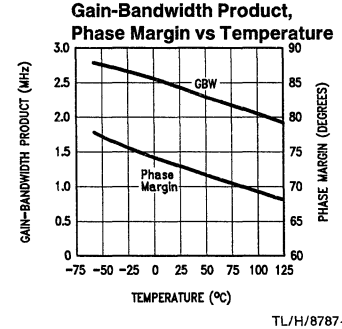
Supply Current vs Supply Voltage



Open Loop Gain and Phase vs Frequency



Gain-Bandwidth Product, Phase Margin vs Temperature



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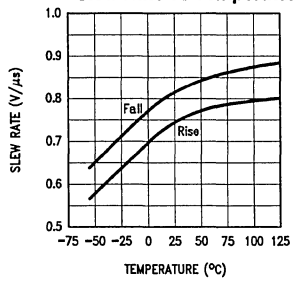
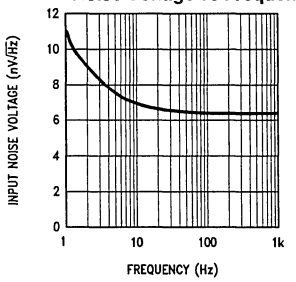
Typical Performance Characteristics (Continued)

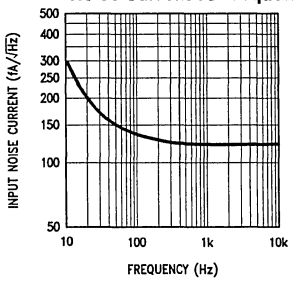
Slew Rate vs Temperature



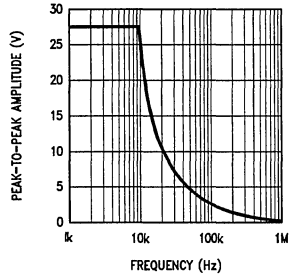
Noise Voltage vs Frequency



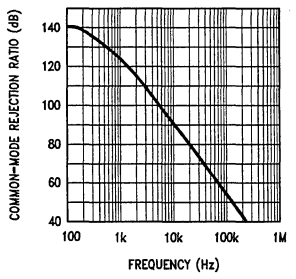
Noise Current vs Frequency



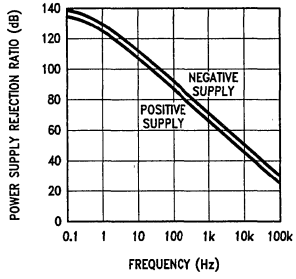
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



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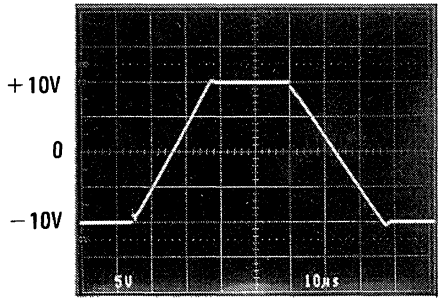
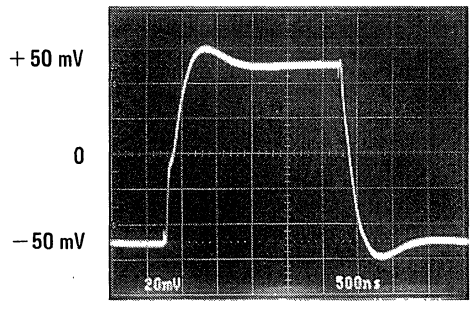
Large-Signal Pulse Response, $A_V = +1$



TIME (10 μs/DIV)

TL/H/8787–14

Small-Signal Pulse Response, $A_V = +1$



TIME (500 ns/DIV)

TL/H/8787–15

3

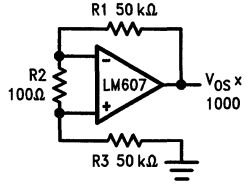
Application Hints

OFFSET VOLTAGE

Offset voltage of the LM607 is internally trimmed to a very low value. The data sheet V_{OS} specification applies at T_J = 25°C, V_{CM} = 0 and ±15V supplies. For other conditions, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Although the LM607C is specified as T_J = 25°C, the 3 μV typical warmup drift is a small fraction of its 100 μV max offset. For the 25 μV LM607A and 50 μV LM607B grades, the offset voltage is measured fully warmed up with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure V_{OS} with high accuracy, gain must be taken right at the device as shown, otherwise the offset voltage would get swamped out by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimized airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal EMF. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

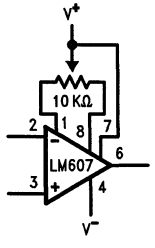


TL/H/8787–3

FIGURE 1. Offset Voltage Test Circuit

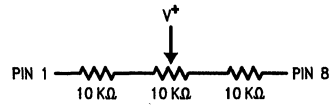
OFFSET NULLING

This is usually not required on the LM607 family since its offset voltage is internally trimmed. An offset adjust range of approximately ±1.5 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2*. With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiometer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. For example the circuit of *Figure 3* has an adjustment range of ±150 μV.



TL/H/8787–4

FIGURE 2. Offset Adjust Circuit



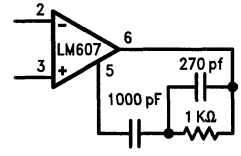
TL/H/8787–5

FIGURE 3. Improved Sensitivity Offset Adjust

Because adjusting the offset voltage of an LM607 will alter its offset voltage temperature drift, caution is advised. Every 100 μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM607C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

OVERCOMPENSATION

Without any external compensation, the LM607 is stable at unity gain and up to 750 pF load capacitance. It has a slew rate of 0.7V/μs and a gain-bandwidth product of 1.8 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4*. This increases maximum capacitive loading to 0.01 μF while decreasing slew rate to 0.13V/μs and bandwidth to 200 kHz. If overcompensation is not desired, pin 5 should be left open.

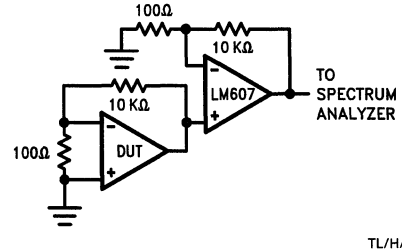


TL/H/8787–6

FIGURE 4. Overcompensation

NOISE

The LM607 achieves lower voltage noise than the OP-07 primarily by operating at higher input stage current. Its superbeta input transistors and trimmed bias-current compensation prevent the bias current from increasing. When measuring spot noise, a circuit as shown in *Figure 5* is recommended. The DUT runs at a gain of 100 will not roll off until approximately 15 kHz. Another gain of 100 amplifier following brings total DUT-input-referred gain up to 10,000 to minimize sensitivity to EMI in the environment. When measuring spot noise at 100 Hz, it is recommended that the bandwidth be 20 Hz or less to minimize pickup of 120 Hz, the second harmonic of line frequency.



TL/H/8787–7

FIGURE 5. Spot Noise Test Circuit

Application Hints (Continued)

The circuit used to measure peak-to-peak noise in the 0.1 to 10 Hz range is shown in *Figure 6*. The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, in addition to the single zero rolloff. The measuring equipment must be flat beyond this bandwidth. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.

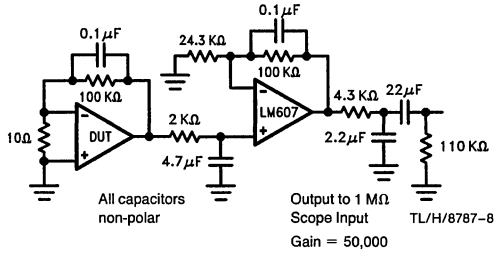


FIGURE 6. 0.1 to 10 Hz Noise Test Circuit

Input Overdrive

The LM607's input-protection diodes prevent zener breakdown of the input transistors and the ensuing degradation of input DC parameters. Current limiting resistors have not been included as they would degrade input noise voltage. Input current should be limited to ±25 mA to avoid potential damage to the IC metallization.

In voltage follower applications, large input voltage steps may be coupled directly to the op amp's output via the protection diodes. If the input and feedback resistances are low in value, the output stage may be driven temporarily into current limit. The resulting output waveform exhibits an initial fast step when the diodes are conducting followed by a slight glitch as the amplifier comes out of current limit before true slewing is observed. For best results, use input and feedback resistors of 2 kΩ each in parallel with 30 pF capacitors. The capacitors eliminate input and feedback poles which respectively cause signal rolloff and instabilities.

National Semiconductor

LM611A/LM611
Operational Amplifier and Adjustable Reference

General Description

The operational amplifier is a versatile common-mode-to-the-negative-supply ("single-supply") type similar to the LM124 series, but with improved slew rate, improved power bandwidth, reduced cross-over distortion, and low supply current even while driven beyond swing limits. Lateral PNP input transistors enable low input currents for large differential input voltages and swings above V^+.

The voltage reference is a three-terminal shunt-type bandgap similar to the adjustable LM185 series, but with improved voltage accuracy to ±0.4% accuracy by wafer trim. Two resistors program the reference from 1.24V to 6.3V. The reference features operation over a current range of 16 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+.

As a member of National's new Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features (Guaranteed over temperature and supply)

OP AMP

- Low operating current — 300 μA (op amp), 16 μA (ref)
- Large supply voltage range — 4V to 36V
- Large output swing (10k load) — $(V^- + 1V)$ to $(V^+ - 1.8V)$
- Input common-mode range includes — V^- to $(V^+ - 1.4V)$
- Wide input differential voltage — ±36V

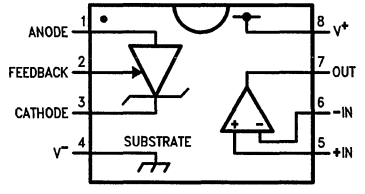
REFERENCE

- Adjustable output voltage — 1.2V to 6.3V
- Tight initial tolerance available — ±0.4%
- Tolerant of load capacitance — 0 to ∞

Applications

- Power supplies
- Signal conditioning

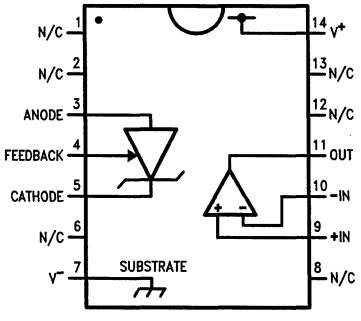
Connection Diagrams



TL/H/9221-1

Top View

See NS Package Number J08A or N08E



TL/H/9221-2

Top View

See NS Package Number M14A
M Narrow (0.15")

Order Number

Prime Military	LM611MJ
$(-55°C \le T_A \le +125°C)$	
tested at −55°C, +25°C, +125°C	
drift tested at −55°C, +25°C, +125°C	
Prime Industrial	LM611AIN
$(-40°C \le T_A \le +85°C)$	
tested at +25°C	
drift tested at −40°C, +25°C, +85°C	
Industrial	LM611IN
$(-40°C \le T_A \le +85°C)$	LM611IM
tested at +25°C	
Commercial	LM611CN
$(0 \le T_A \le +70°C)$	LM611CM
tested at +25°C	

Packages

J	Hermetic Dual-In-Line
N	Plastic Dual-In-Line
M	Plastic Surface Mount Narrow (0.15")

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on any Pin Except Cathode Pin (referred to V^- pin)
(Note 1) −0.3V (Min)
Military and Industrial 36V
Commercial 32V

Current through any Input Pin & Cathode Pin ±20 mA

Differential Input Voltage
Military and Industrial ±36V
Commercial ±32V

Short Circuit Duration, Op Amp (Note 2) Continuous

Storage Temperature Range −65°C to +150°C

Maximum Junction Temperature 150°C

Operating Junction Temperature Range T_{MIN} to T_{MAX}
LM611M −55°C to +125°C
LM611I −40°C to +85°C
LM611C 0°C to +70°C

Soldering Information
Dual-In-Line Package
Soldering (10 seconds) 260°C
Small Outline Package
Vapor Phase (60 seconds) 215°C
Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Package Thermal Resistance (Note 3)
Hermetic DIP J08 105°C/W
Molded DIP N08 100°C/W
Molded SO M14 Narrow 150°C/W

ESD Tolerance (Note 4)
120 pF, 1.5 kΩ ±1 kV
200 pF, < 1Ω ±250V

Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{MIN} to T_{MAX}.

Parameter	Conditions	Typical (Note 5)	LM611M		LM611AI, LM611I		LM611C		Units
			Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ Over T_J Range (Commercial 32V)	210 **221**	300 **320**		300	**320**	350	**370**	μA max μA max
Supply Voltage Range	Meets Total Supply Current, and See V_R Change with V^+ Change Test	2.2 **2.9**	2.8 **3**		2.8	**3**	2.8	**3**	V min V min
		46 **43**	37 **36**		36	**36**	32	**32**	V max V max
OPERATIONAL AMPLIFIERS									
V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ Commercial)	±1.5 **±2.0**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.4V$), V^+ = 30V	±1.0 **±1.5**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
Average V_{OS} Drift	(Note 8)	**±15**	**±25**		**±30**				max μV/°C
Input Bias Current	I_{B+IN} and I_{B-IN}	−10 **−11**	±20 **±25**		±25	**±30**	±35	**±40**	nA max nA max
Input Offset Current	$I_{OS} = I_{B+IN} - I_{B-IN}$	±0.2 **±0.3**	±4 **±4**		±4	**±5**	±4	**±5**	nA max nA max
Average I_{OS} Drift		**±4**							pA/°C
Input Resistance	Differential: Common-Mode:	1800 3800							MΩ MΩ

Electrical Characteristics

These specifications apply for T_J = 25°C, V^- = GND = 0V, V^+ = 5V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{MIN} to T_{MAX}. (Continued)

Parameter	Conditions	Typical (Note 5)	LM611M		LM611AI, LM611I		LM611C		Units
			Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
Input Cap.	C-to-GND, Non-Inverting Input of Follower	5.7							pF
Voltage Noise	100 Hz, Input Referred	74							nV/√Hz
Current Noise	100 Hz Bias Current Noise	58							fA/√Hz
Common-Mode Reject Ratio	V^+ = 30V, 0V ≤ V_{CM} ≤ (V^+ − 1.4V), CMRR = 20 log {$\Delta V_{CM}/\Delta V_{OS}$}	95 **90**	85 **80**		80	 **75**	75	 **70**	dB min dB min
Power Supply Reject Ratio	4V ≤ V^+ ≤ 30V, V_{CM} = $V^+/2$, PSRR = 20 log {$\Delta V^+/\Delta V_{OS}$}	110 **100**	85 **80**		80	 **75**	75	 **70**	dB min dB min
Voltage Gain, Open Loop	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V, Open-Loop A_V = $\lvert\Delta V_{OUT}/\Delta V_{INDIFF}\rvert$	500 **50**	100 **40**		100	 **40**	94	 **40**	V/mV min
Slew Rate	V^+ = 30V, (Note 9)	±0.70 **±0.65**	±0.55 **±0.45**		±0.55	 **±0.45**	±0.50	 **±0.45**	V/μs min
Gain-Bandwidth	Closed Loop Gain = −1000, −3 dB Frequency × Gain, C_L = 50 pF	0.79 **0.52**							MHz
Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V Commercial)	V^+ − 1.4 **V^+ − 1.6**	V^+ − 1.6 **V^- − 1.8**		V^+ − 1.7	 **V^+ − 1.9**	V^+ − 1.8	 **V^+ − 1.9**	V min V min
Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V Commercial)	V^- + 0.8 **V^- + 0.9**	V^- + 0.90 **V^- + 1.0**		V^- + 0.90	 **V^- + 1.0**	V^- + 0.95	 **V^- + 1.0**	V max V max
I_{OUT} Source	V_{OUT} = V^+ −2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	−25 **−15**	−20 **−13**		−20	 **−13**	−16	 **−13**	mA max mA max
I_{OUT} Sink	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	15 **8**		14	 **11**	13	 **11**	mA min mA min
Short-Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source:	−30 **−40**	−37 **−46**		−40	 **−48**	−43	 **−50**	mA min mA min
	V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink:	30 **32**	40 **60**		60	 **80**	70	 **90**	mA max mA max

Electrical Characteristics

These specifications apply for T_J = 25°C, V^- = GND = 0V, V^+ = 5V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{MIN} to T_{MAX}. (Continued)

Parameter	Conditions	Typical (Note 5)	LM611M		LM611AI, LM611I		LM611C		Units
			Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
VOLTAGE REFERENCE (Note 10)									
Reference Voltage		1.244	1.2390 1.2490 (±0.4%)		1.2365 1.2515 (±0.6%)		1.2191 1.2689 (±2%)		V min V max
Average Temp. Drift	(Note 11) LM611AI:	**10**	**20**		**20**	**80**		**150**	PPM/°C max
Average Time Drift	T_J = 40°C T_J = 150°C	400 1000							PPM/kHr PPM/kHr
Hysteresis	Hyst = (Vro′ − Vro)/ΔT_J (Note 12)	**±3.2**							μV/°C
V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[16\ \mu A]}$	0.05 **0.1**	±1 **±1**		±1	**±1.1**	±1	**±1.1**	mV max mV max
	$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 13)	1.5 **2.0**	5 **5**		5	**5.5**	5	**5.5**	mV max mV max
Resistance	$\Delta V_{R[10 \rightarrow 0.1\ mA]}$/9.9 mA: $\Delta V_{R[100 \rightarrow 16\ \mu A]}$/84 μA:	0.2 0.6		**0.51** **12**		**0.56** **13**		**0.56** **13**	Ω max Ω max
V_R Change with High V_{RO}	$V_{R[Vro = Vr]} - V_{R[Vro = 6.3V]}$ {5.06V between Anode and FEEDBACK}	2.5 **2.8**	5 **8**		7	**10**	7	**10**	mV max mV max
V_R Change with V^+ Change	$V_{R[V^+ = 5V]} - V_{R[V^+ = 36V]}$ (V^+ = 32V Commercial)	−0.1 **−0.1**	±1.2 **±1.2**		±1.2	**±1.3**	±1.2	**±1.3**	mV max mV max
	$V_{R[V^+ = 5V]} - V_{R[V^+ = 3V]}$	0.01 **0.01**	±1 **±1**		±1	**±1.5**	±1	**±1.5**	mV max mV max
V_R Change with V_{ANODE} Change	$V^+ = V^+_{MAX}$ $\Delta V_R = V_R$ (@ V_{ANODE} = V^- = GND) − V_R (@ $V_{ANODE} = V^+ - 1.0V$)	0.7 **3.3**	1.5 **5.0**		1.5	**4.0**	1.6	**3.0**	mV max mV max
FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \le V_{FB} \le 5.06V$	−22 **−29**	−35 **−40**		−35	**−40**	−50	**−55**	nA min nA min
V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30							μV_{RMS}

Electrical Characteristics Notes

Note 1: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltage on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 2: Simultaneous short-circuit of op amp and reference while using high voltage supplies may force junction temperature above maximum, and thus should not be continuous.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{jA}$. The given thermal resistances are worst-case for packages in sockets in still air. Nominal θ_{jA} are 95°C/W for LM611 in J package, 90°C/W for the N package, 135°C/W for the M package, for packages soldered to copper-clad board with dissipation from one op amp or reference power transistor.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typcial values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply to the military temperature range. These values represent the most likely parametric norm.

Note 6: Tested limits are guaranteed and 100% tested.

Note 7: Design limits are guaranteed via correlation, but are not 100% tested.

Note 8: Offset voltage drift is calculated from the measurement of the offset voltage at 25°C and at the temperature extremes. The drift is $\Delta V_{OS}/\Delta T$, where ΔV_{OS} is the lowest value subtracted from the highest, and ΔT is the temperature range.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_{ro} is the Cathode-to-Anode voltage (1.2V to 6.3V) and V_r is the Cathode-to-FEEDBACK voltage (1.2V).

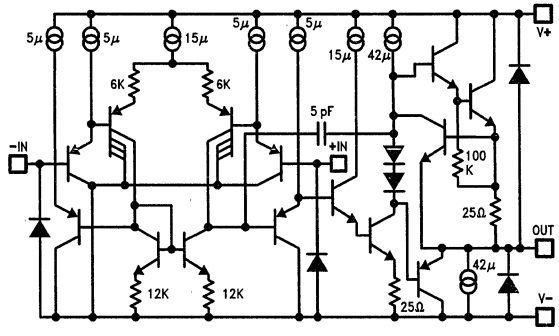
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range.

Note 12: Hysteresis is $\Delta V_{RO}/\Delta T_J$, where ΔV_{RO} is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 125°C, −55°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp



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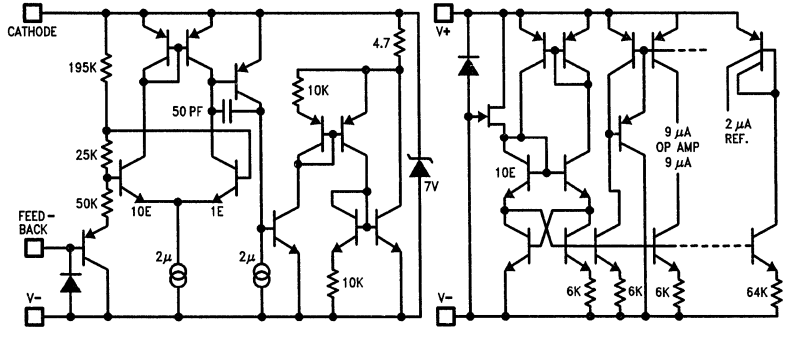
Reference

Bias

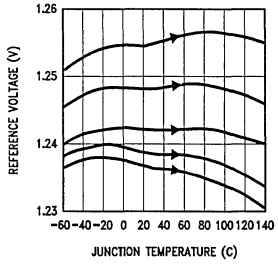


TL/H/9221–4

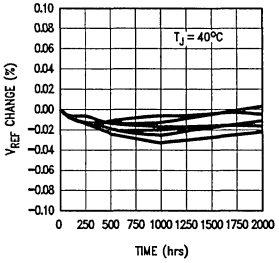
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

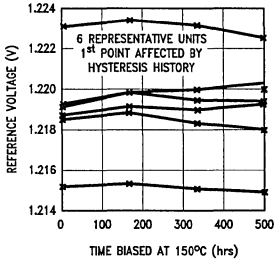
Reference Voltage vs Temp on 5 Representative Units



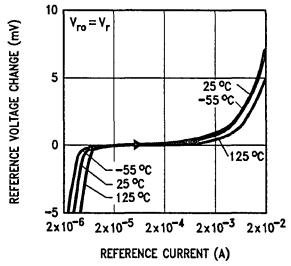
Reference Voltage Drift



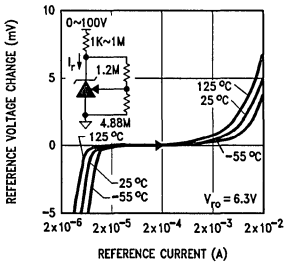
Accelerated Reference Voltage Drift vs Time



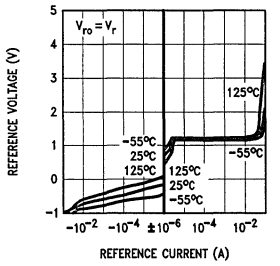
Reference Voltage vs Current and Temperature



Reference Voltage vs Current and Temperature



Reference Voltage vs Reference Current



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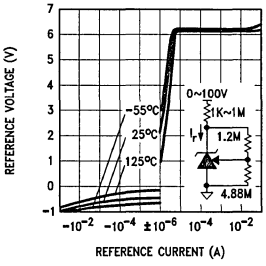
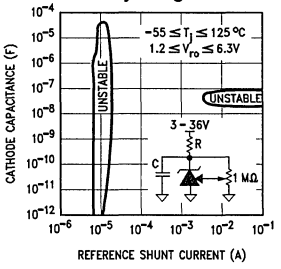
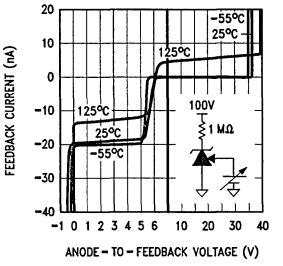
Reference Voltage vs Reference Current



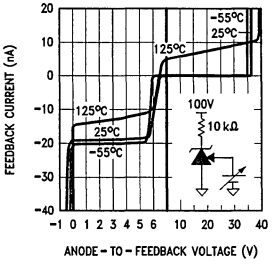
Reference AC Stability Range



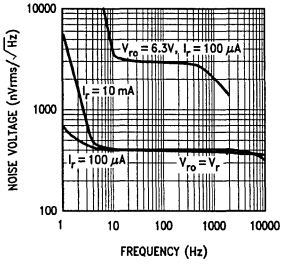
Feedback Current vs Feedback-to-Anode Voltage



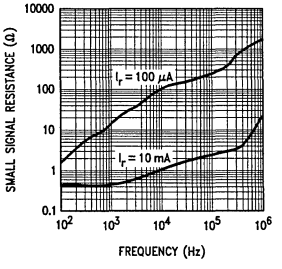
Feedback Current vs Feedback-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

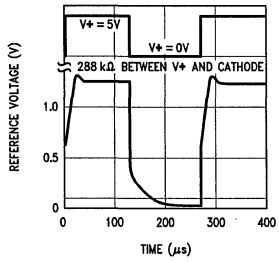


TL/H/9221–6

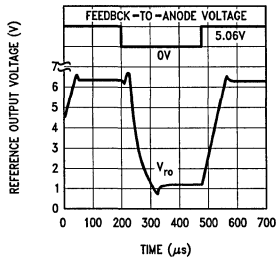
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

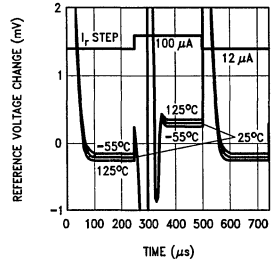
Reference Power-Up Time



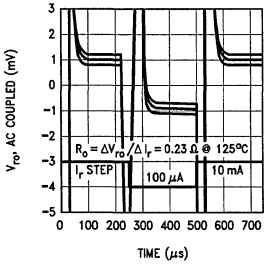
Reference Voltage with Feedback Voltage Step



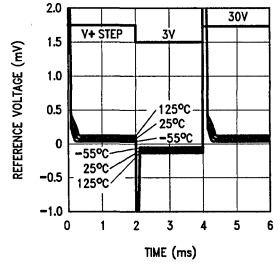
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

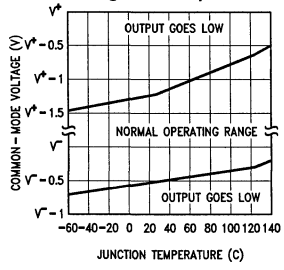


TL/H/9221-7

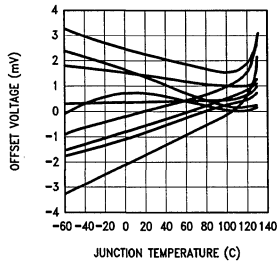
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

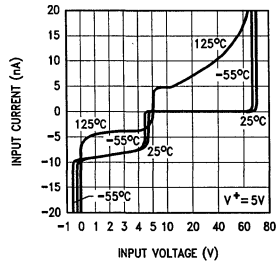
Input Common-Mode Voltage Range vs Temperature



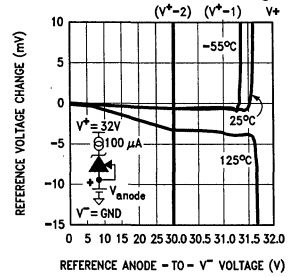
V_{OS} vs Junction Temperature



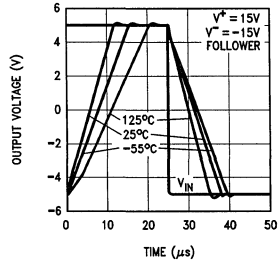
Input Bias Current vs Common-Mode Voltage



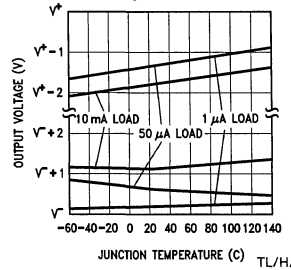
Reference Change vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

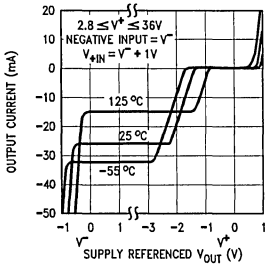


TL/H/9221-8

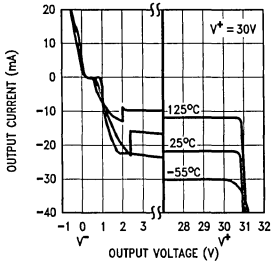
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

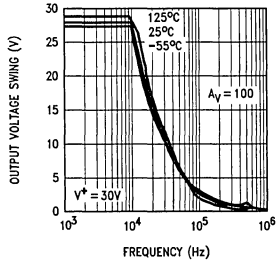
Output Source Current vs Output Voltage and Temp.



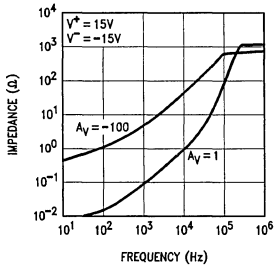
Output Sink Current vs Output Voltage



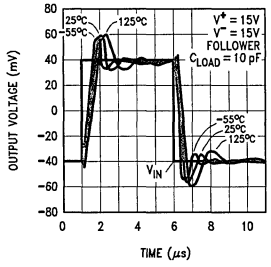
Output Swing, Large Signal



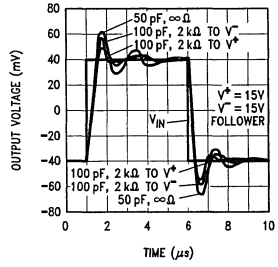
Output Impedance vs Frequency and Gain



Small Signal Pulse Response vs Temp.



Small-Signal Pulse Response vs Load



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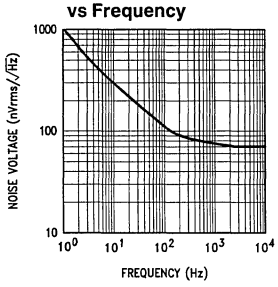
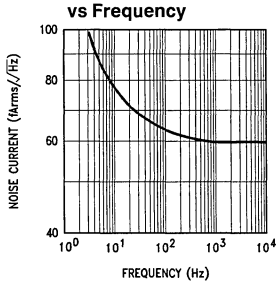
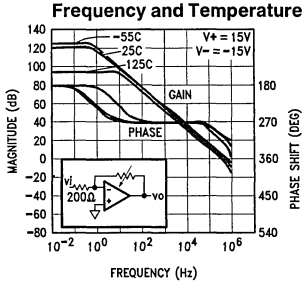
Op Amp Voltage Noise vs Frequency



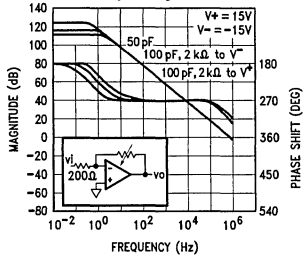
Op Amp Current Noise vs Frequency



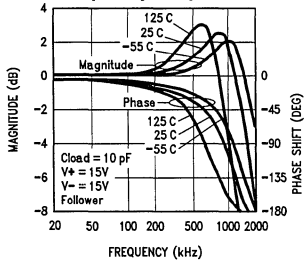
Small-Signal Voltage Gain vs Frequency and Temperature



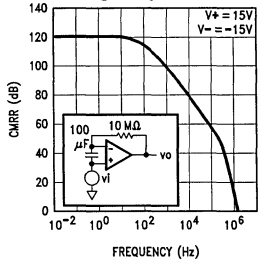
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

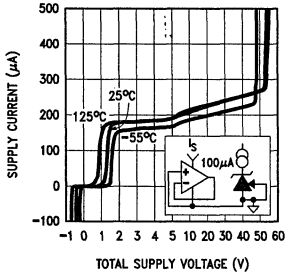


TL/H/9221–10

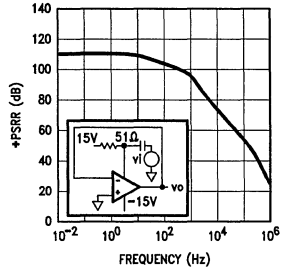
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, V^- Q GND $= 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

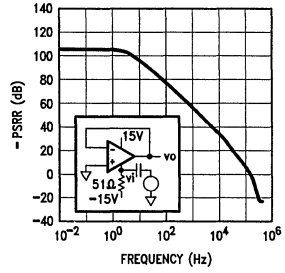
Power Supply Current vs Power Supply Voltage



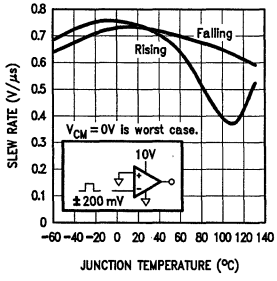
Positive Power Supply Voltage Rejection Ratio



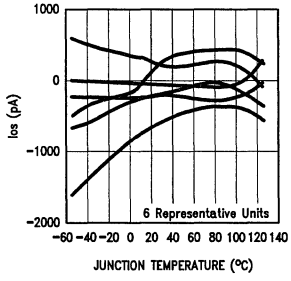
Negative Power Supply Voltage Rejection Ratio



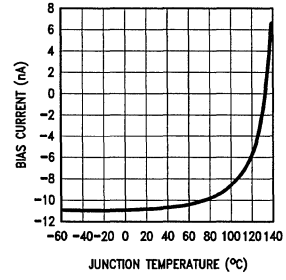
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



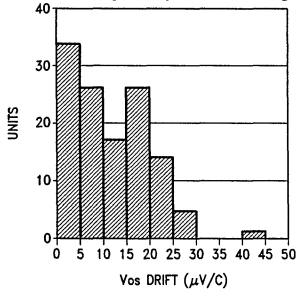
Input Bias Current vs Junction Temperature



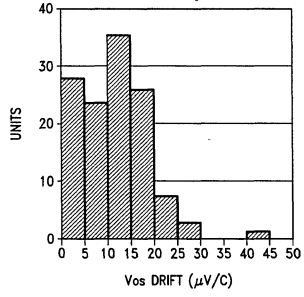
TL/H/9221–11

Typical Performance Distributions

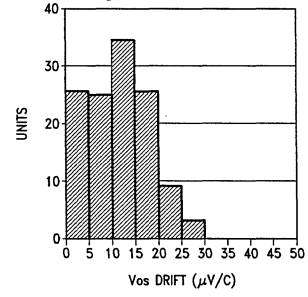
Average V_{OS} Drift Military Temperature Range



Average V_{OS} Drift Industrial Temperature Range

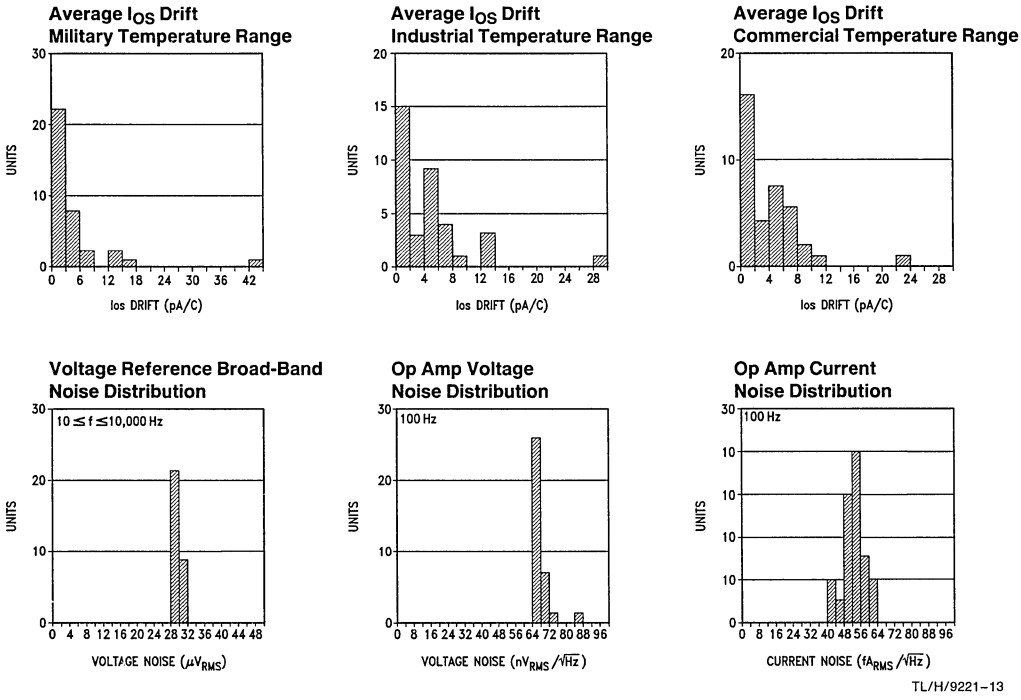


Average V_{OS} Drift Commercial Temperature Range



TL/H/9221–12

Typical Performance Distributions (Continued)



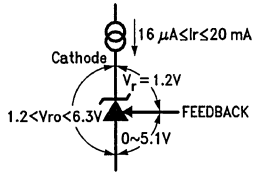
TL/H/9221–13

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

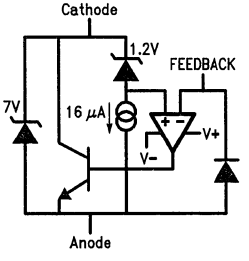


TL/H/9221–14

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

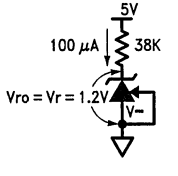
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9221–15

FIGURE 2. Reference Equivalent Circuit



TL/H/9221–16

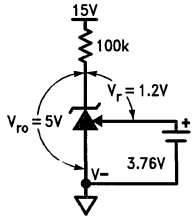
FIGURE 3. 1.2V Reference

Application Information (Continued)

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

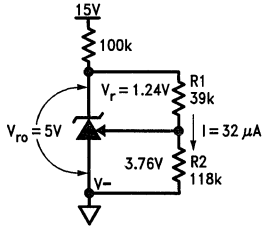
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part.)



TL/H/9221–17

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



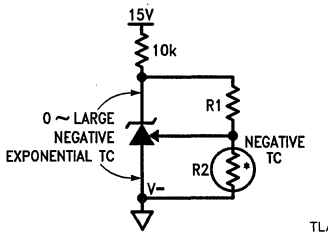
TL/H/9221–18

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\{(Vro/Vr) - 1\} = 39k\{(5/1.24) - 1)\} = 118k$$

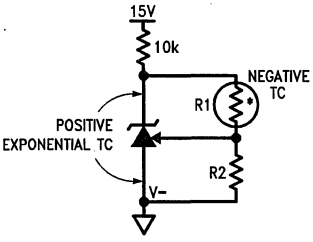
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



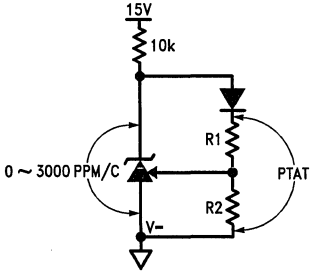
TL/H/9221–19

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9221–20

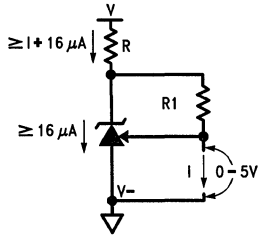
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9221–21

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

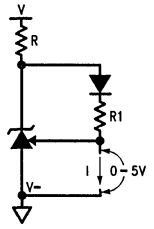


TL/H/9221–22

$$I = Vr/R1 = 1.24/R1$$

FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9221–23

FIGURE 10. Proportional-to-Absolute-Temperature Current Source

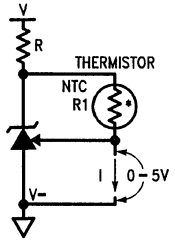


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FIGURE 11. Negative −TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2) Cross-over Distortion: The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

For typical applications, refer to the LM124 Op Amp and LM185 Adjustable Reference datasheets.

National Semiconductor

LM613A/LM613
Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The operational amplifiers are a versatile common-mode-to-the-negative-supply ("single supply") type similar to the LM124 series, but with improved slew rate, improved power bandwidth, reduced cross-over distortion, and low supply current even when driven beyond output swing limits. The comparators are also a common-mode-to-the-negative-supply type, similar to the LM139 series. The op amps and comparators have lateral PNP input transistors which enable low input currents for large differential input voltages and swings above V^+.

The voltage reference is a three-terminal shunt-type bandgap similar to the adjustable LM185 series, but with anode committed to the V^- terminal and improved voltage accuracy to ±0.4%. Two resistors program the reference from 1.24V to 6.3V. The reference features operation over a shunt current range of 16 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+.

As a member of National's new Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features (Guaranteed over temperature & supply)

OP AMPS AND COMPARATORS

- Low operating current — 1000 μA (op amps & comparators), 16 μA (reference)
- Large supply voltage range — 4V to 36V
- Large output swing (10 kΩ load) — $(V^- + 1V)$ to $(V^+ - 1.8V)$
- Input common-mode range — V^- to $(V^+ - 1.4V)$
- Wide differential input voltage — ±36V

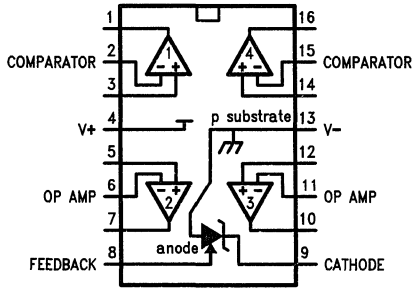
REFERENCE

- Adjustable output voltage — 1.2V to 6.3V
- Tight initial tolerance available — ±0.4%
- Tolerant of load capacitance

Applications

- Power supplies
- Signal conditioning

Connection Diagram



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Top View

Order Number LM613IJ, LM613MJ, LM613CWM, LM613IWM, LM613AIN, LM613CN or LM613IN
See NS Package Number J16A, M16B or N16A

Order Number

Prime Military — LM613MJ
Tested at −55°C, +25°C, +125°C
Drift tested at −55°C, +25°C, +125°C

Prime Industrial — LM613AIN
Tested at 25°C
Drift tested at −40°C, +25°C, +85°C

Industrial — LM613IN
Tested at +25°C — LM613IJ, LM613IWM

Commercial — LM613CN
Tested at +25°C — LM613CWM

Packages

J	Hermetic Dual-In-Line
N	Plastic Dual-In-Line
WM	Plastic Surface Mount Wide (0.3")

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except Cathode Pin (referred to V− pin) (Note 2)
(Note 3) −0.3V (Min)
LM613M, LM613AI, LM613I 36V
LM613C 32V

Current through Any Input Pin & Cathode Pin ±20 mA

Differential Input Voltage
LM613M, LM613AI, LM613I ±36V
LM613C ±32V

Short Circuit Duration, Op Amp (Note 4) Continuous

Storage Temperature Range −65°C to +150°C

Maximum Junction Temperature 150°C

Soldering Information
J, N Packages
Soldering (10 seconds) 260°C
WM Package
Vapor Phase (60 seconds) 215°C
Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance, Junction-to-Ambient (Note 5)
LM613MJ, LM613IJ 100 °C/W
LM613AIN, LM613IN, LM613CN 95 °C/W
LM613IWM, LM613CWM 144 °C/W

ESD Tolerance (Note 6) ±1 kV

Operating Junction Temperature Range T_{MIN} to T_{MAX}
LM613M −55°C to +125°C
LM613I −40°C to +85°C
LM613C 0°C to +70°C

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = V^+ /2, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for **T_{MIN} to T_{MAX}**.

Parameter	Conditions	Typ (Note 7)	LM613M		LM613AI, LM613I		LM613C		Units
			Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	
Total Supply Current	V^+ Current, R_{LOAD} = ∞, 4V ≤ V^+ ≤ 36V (32V for LM613C)	450 **550**	900 **1000**		940	 **1000**	1000	 **1070**	μA (Max) μA (Max)
Supply Voltage Range	Total Supply Current Specification is Met	2.2 **2.9**	2.8 **3**		2.8	 **3**	2.8	 **3**	V (Min) V (Min)
		46 **43**	36 **36**		36	 **36**	32	 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS									
Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C)	±1.5 ±**2.0**	±3.5 ±**5.0**		±3.5	 ±**6.0**	±5.0	 ±**7.0**	mV (Max) mV (Max)
Offset Voltage over V_{CM}	0V ≤ V_{CM} ≤ (V^+ − 1.4V), V^+ = 30V	±1.0 ±**1.5**	±3.5 ±**5.0**		±3.5	 ±**6.0**	±5.0	 ±**7.0**	mV (Max) mV (Max)
Average Offset Voltage Drift	LM613M and LM613AI Op Amp 3 Only, (Note 10)	**15**	**25**		**30**				μV/°C (Max)
Input Bias Current		−10 −**11**	±20 ±**25**		±25	 ±**30**	±35	 ±**40**	nA (Max) nA (Max)
Input Offset Current		±0.2 ±**0.3**	±4 ±**4**		±4	 ±**5**	±4	 ±**5**	nA (Max) nA (Max)
Average Offset Current Drift		±**4**							pA/°C
Input Resistance		>1000							MΩ
Input Capacitance	Differential Non-Inv. Input to GND	0.6 6							pF pF

Electrical Characteristics These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{MIN} to T_{MAX}. (Continued)

Parameter	Conditions	Typ (Note 7)	LM613M		LM613AI, LM613I		LM613C		Units
			Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	
OPERATIONAL AMPLIFIERS (Continued)									
Voltage Noise	f = 100 Hz	74							nV/√Hz
Current Noise	f = 100 Hz	58							fA/√Hz
Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ (V^+ − 1.4V), V^+ = 30V	95 **90**	85 **80**		80	 **75**	75	 **70**	dB (Min) dB (Min)
Power Supply Rejection Ratio	4V ≤ V^+ ≤ 30V, $V_{CM} = V^+/2$	100 **90**	85 **80**		80	 **75**	75	 **70**	dB (Min) dB (Min)
Voltage Gain, Open Loop	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	100 **40**		100	 **40**	94	 **40**	V/mV (Min)
Slew Rate	V^+ = 30V (Note 11)	±0.70 **±0.65**	±0.55 **±0.45**		±0.55	 **±0.45**	±0.50	 **±0.45**	V/μs (Min)
Gain-Bandwidth Product	C_L = 50 pF	0.8 **0.5**							MHz MHz
Output Voltage Swing	R_L = 10 kΩ to GND, V^+ = 36V (32V for LM613C)	$V^+ - 1.4$ $\mathbf{V^+ - 1.6}$	$V^+ - 1.6$ $\mathbf{V^+ - 1.8}$		$V^+ - 1.7$	 $\mathbf{V^+ - 1.9}$	$V^+ - 1.8$	 $\mathbf{V^+ - 1.9}$	V (Min) V (Min)
	R_L = 10 kΩ to V^+, V^+ = 36V (32V for LM613C)	$V^- + 0.8$ $\mathbf{V^- + 0.9}$	$V^- + 0.90$ $\mathbf{V^- + 1.0}$		$V^- + 0.90$	 $\mathbf{V^- + 1.0}$	$V^- + 0.95$	 $\mathbf{V^- + 1.0}$	V (Max) V (Max)
Output Current (Sourcing)	$V_{OUT} = V^+ - 2.5V$, V_{+IN} = 0V, V_{-IN} = −0.3V	−25 **−15**	−20 **−13**		−20	 **−13**	−16	 **−13**	mA (Max) mA (Max)
(Sinking)	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = −0.3V	17 **9**	15 **8**		14	 **11**	13	 **11**	mA (Min) mA (Min)
Output Short-Circuit Current (Sourcing)	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V	−30 **−40**	−37 **−46**		−40	 **−48**	−43	 **−50**	mA (Min) mA (Min)
(Sinking)	V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V	30 **32**	40 **60**		60	 **80**	70	 **90**	mA (Max) mA (Max)
COMPARATORS									
Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C), R_L = 15 kΩ	±1.0 **±2.0**	±2.5 **±4.0**		±3.0	 **±6.0**	±5.0	 **±7.0**	mV (Max) mV (Max)
Offset Voltage over V_{CM}	0V ≤ V_{CM} (V^+ − 1.4V), V^+ = 30V, R_L = 15 kΩ	±1.0 **±1.5**	±2.5 **±4.0**		±3.0	 **±6.0**	±5.0	 **±7.0**	mV (Max) mV (Max)
Average Offset Voltage Drift		**15**							μV/°C (Max)
Input Bias Current		−5 **−8**	±20 **±25**		±25	 **±30**	±35	 **±40**	nA (Max) nA (Max)

Electrical Characteristics These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for **T_{MIN} to T_{MAX}**. (Continued)

Parameter	Conditions	Typ (Note 7)	LM613M		LM613AI, LM613I		LM613C		Units
			Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	Tested Limit (Note 8)	Design Limit (Note 9)	
COMPARATORS (Continued)									
Input Offset Current		±0.2 **±0.3**	±4 **±4**		±4	**±5**	±4	**±5**	nA (Max) nA (Max)
Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C), 2V ≤ V_{OUT} ≤ 27V	500 **100**							V/mV V/mV
Large Signal Response Time	V_{+IN} = 1.4V, V_{-IN} = TTL Swing, R_L = 5.1 kΩ	1.5 **2.0**							μs μs
Output Sink Current	V_{+IN} = 0V, V_{-IN} = 1V, V_{OUT} = 1.5V	20 **13**	12 **8**		10	**8**	10	**8**	mA (Min) mA (Min)
	V_{OUT} = 0.4V	2.8 **2.4**	1.0 **0.8**		1.0	**0.5**	0.8	**0.5**	mA (Min) mA (Min)
Output Leakage Current	V_{+IN} = 1V, V_{-IN} = 0V, V_{OUT} = 36V (32V for LM613C)	0.1 **0.2**	10 **10**		10		10		μA (Max) μA (Max)
VOLTAGE REFERENCE (Note 12)									
Reference Voltage		1.244	1.2390 1.2490 (±0.4%)		1.2365 1.2515 (±0.6%)		1.2191 1.2689 (±2%)		V (Min) V (Max)
Average Temp. Drift	(Note 13) LM613AI	**10**	**20**		**20**	**80**		**150**	ppm/°C (Max)
Average Time Drift	T_J = 40°C T_J = 150°C	400 1000							ppm/kH ppm/kH
Hysteresis	(Note 14)	**±3.2**							μV/°C
V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[16\ \mu A]}$	0.05 **0.1**	±1 **±1**		±1	**±1.1**	±1	**±1.1**	mV (Max) mV (Max)
	$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 15)	1.5 **2.0**	5 **5**		5	**5.5**	5	**5.5**	mV (Max) mV (Max)
Resistance	$\Delta V_{R[10 \rightarrow 0.1\ mA]}/9.9$ mA $\Delta V_{R[100 \rightarrow 16\ \mu A]}/84$ μA	0.2 0.6		**0.51** **12**		**0.56** **13**		**0.56** **13**	Ω (Max) Ω (Max)
V_R Change with High V_{RO}	$V_{R[Vro=Vr]} - V_{R[Vro=6.3V]}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	5 **8**		7	**10**	7	**10**	mV (Max) mV (Max)
V_R Change with V^+ Change	$V_{R[V+=5V]} - V_{R[V+=36V]}$ (V^+ = 32V for LM613C)	0.1 **0.1**	±1.2 **±1.2**		±1.2	**±1.3**	±1.2	**±1.3**	mV (Max) mV (Max)
	$V_{R[V+=5V]} - V_{R[V+=3V]}$	0.01 **0.01**	±1 **±1**		±1	**±1.5**	±1	**±1.5**	mV (Max) mV (Max)
FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	−22 **−29**	−35 **−40**		−35	**−40**	−50	**−55**	nA (Min) nA (Min)
Voltage Noise	BW = 10 Hz to 10 kHz, $V_{RO} = V_R$	30							μV_{RMS}

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple op amps or comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistances are worst-case for packages in sockets in still air. Nominal θ_{JA} are 85°C/W for LM613 in J package, 80°C/W for the N package, and 135°C/W for the WM package, for packages soldered to copper-clad board with dissipation from one op amp, comparator, or reference output transistor.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply to the military temperature range. These values represent the most likely parametric norm.

Note 8: Tested limits are guaranteed and 100% tested.

Note 9: Design limits are guaranteed via correllation, but are not 100% tested.

Note 10: Offset voltage drift is calculated from the measurement of the offset voltage at 25°C and at the temperature extremes. The drift is $\Delta V_{OS}/\Delta T$, where ΔV_{OS} is the lowest value subtracted from the highest, and ΔT is the temperature range.

Note 11: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transistion is sampled at 20V and 10V.

Note 12: V_{RO} is the Cathode-to-Anode voltage (i.e. the reference output voltage, 1.2V to 6.3V). V_R is the Cathode-to-FEEDBACK voltage (nominally 1.2V).

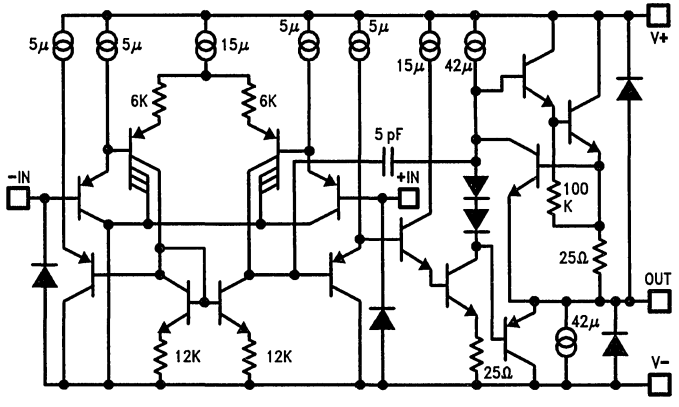
Note 13: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / V_{R[25°C]} \bullet \Delta T_J$, where ΔVR is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range.

Note 14: Hysteresis is $\Delta V_{RO}/\Delta T_J$, where ΔV_{RO} is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 125°C, −55°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 15: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp



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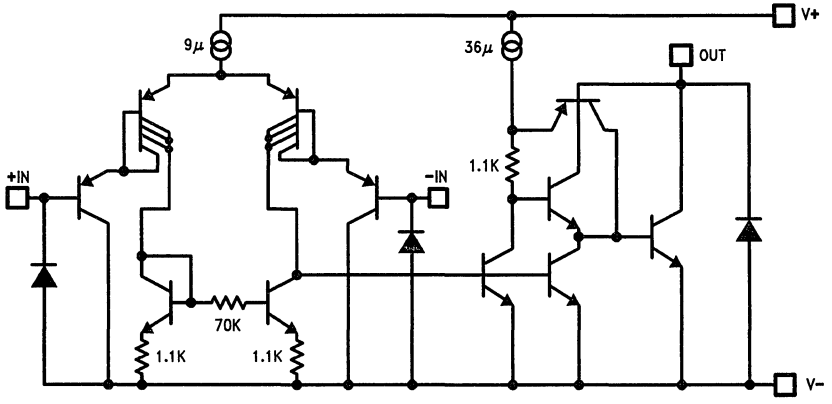
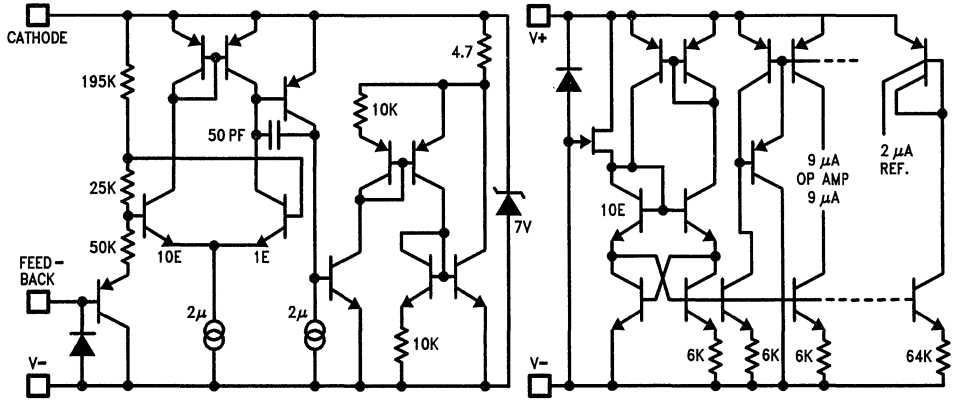
Comparator



TL/H/9226-3

Reference

Bias

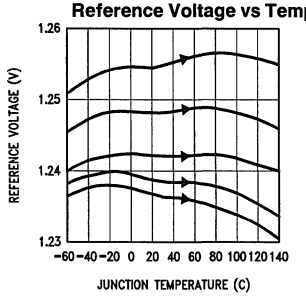


TL/H/9226-4

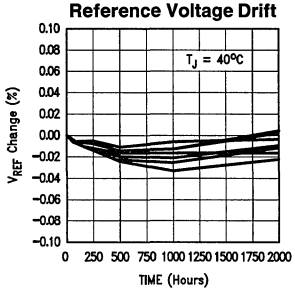
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

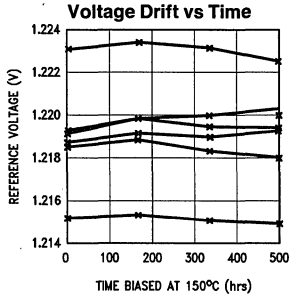
Reference Voltage vs Temp.



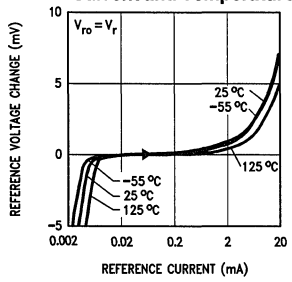
Reference Voltage Drift



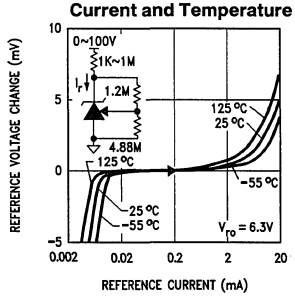
Accelerated Reference Voltage Drift vs Time



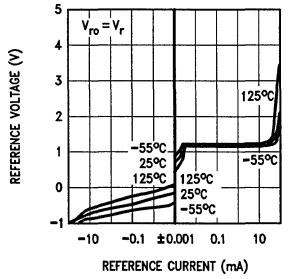
Reference Voltage vs Current and Temperature



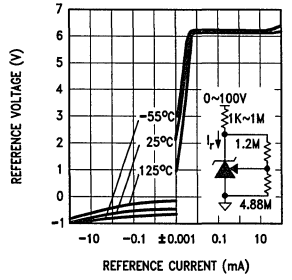
Reference Voltage vs Current and Temperature



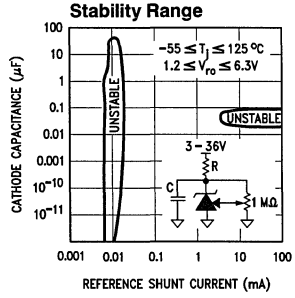
Reference Voltage vs Reference Current



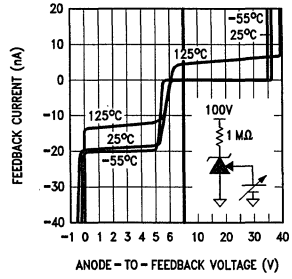
Reference Voltage vs Reference Current



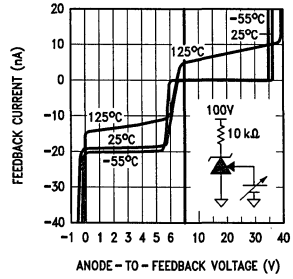
Reference AC Stability Range



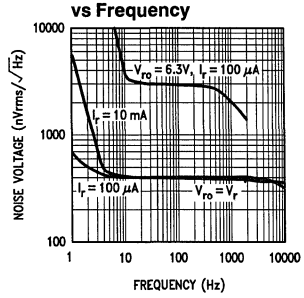
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



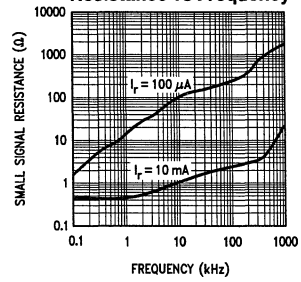
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

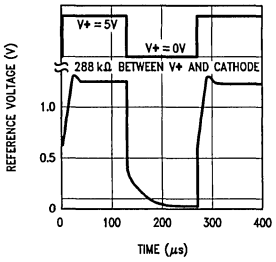


TL/H/9226-5

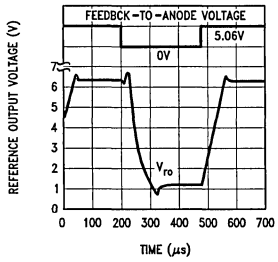
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

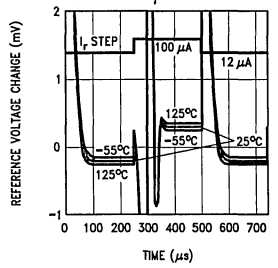
Reference Power-Up Time



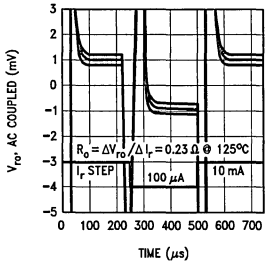
Reference Voltage with FEEDBACK Voltage Step



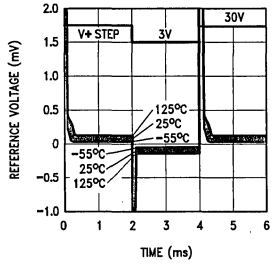
Reference Voltage with 100 ~ 12 μA Current Step



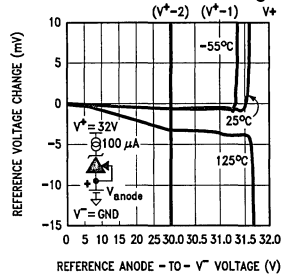
Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage

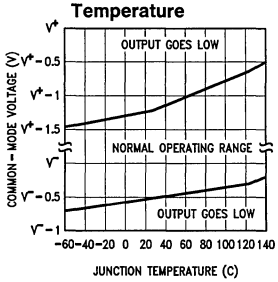


TL/H/9226-6

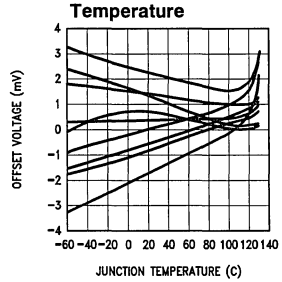
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

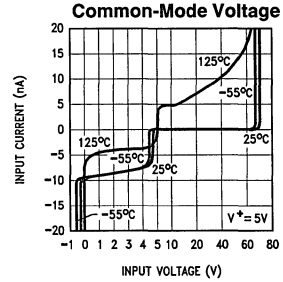
Input Common-Mode Voltage Range vs Temperature



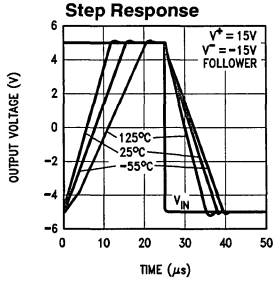
V_{OS} vs Junction Temperature



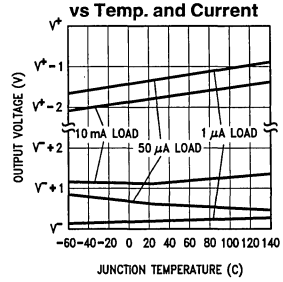
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

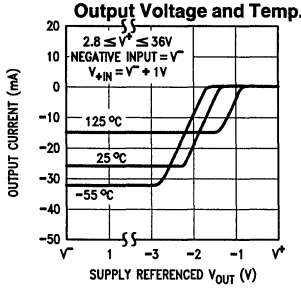


TL/H/9226-7

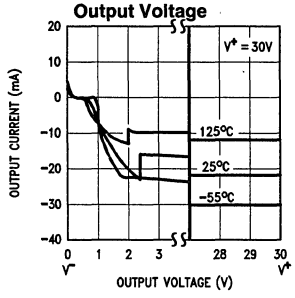
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

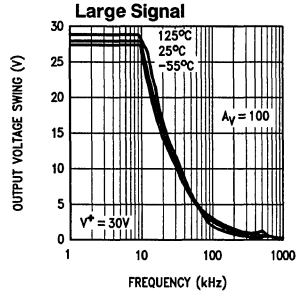
Output Source Current vs Output Voltage and Temp.



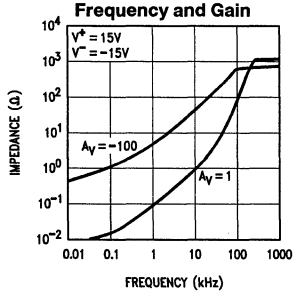
Output Sink Current vs Output Voltage



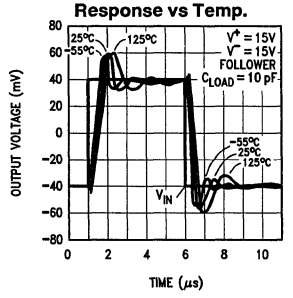
Output Swing, Large Signal



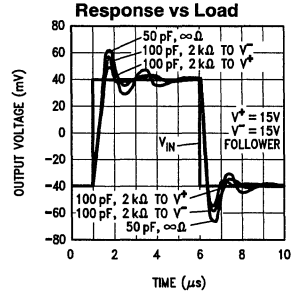
Output Impedance vs Frequency and Gain



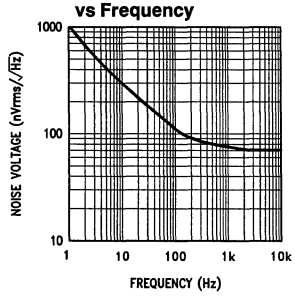
Small Signal Pulse Response vs Temp.



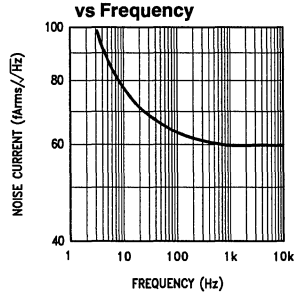
Small-Signal Pulse Response vs Load



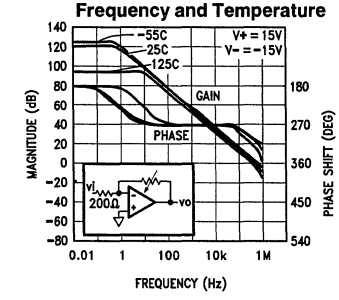
Op Amp Voltage Noise vs Frequency



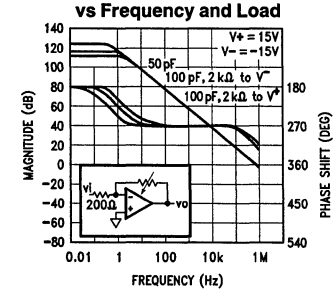
Op Amp Current Noise vs Frequency



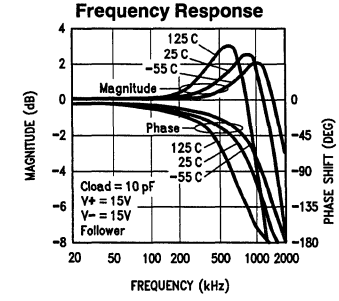
Small-Signal Voltage Gain vs Frequency and Temperature



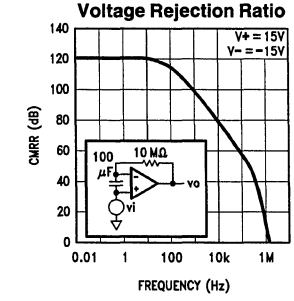
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

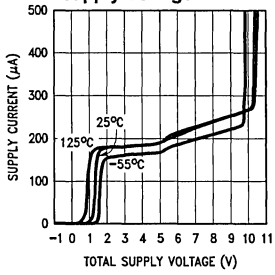


TL/H/9226–8

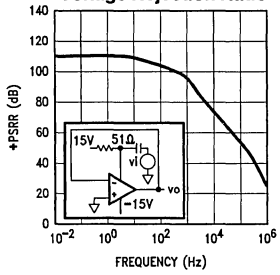
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

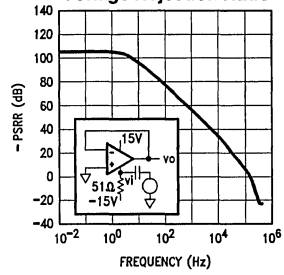
Supply Current vs Supply Voltage



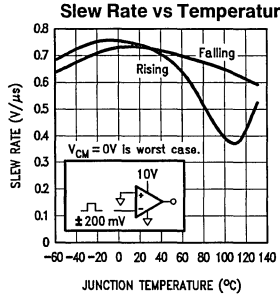
Positive Power Supply Voltage Rejection Ratio



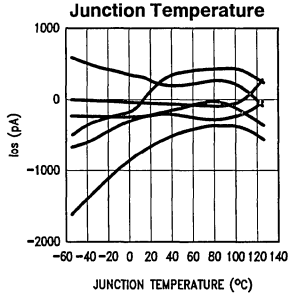
Negative Power Supply Voltage Rejection Ratio



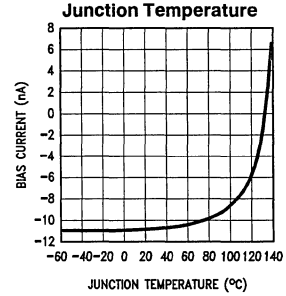
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



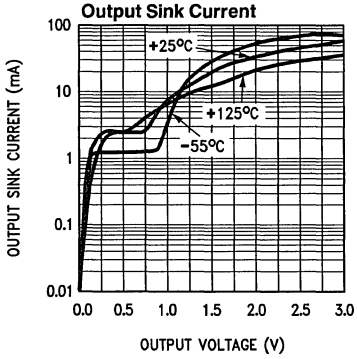
Input Bias Current vs Junction Temperature



TL/H/9226-9

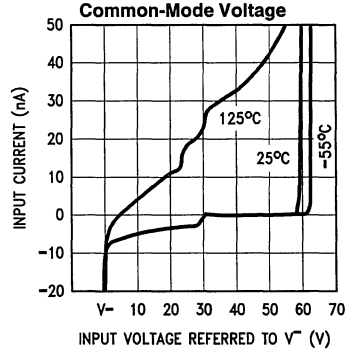
Typical Performance Characteristics (Comparators)

Output Sink Current



TL/H/9226-10

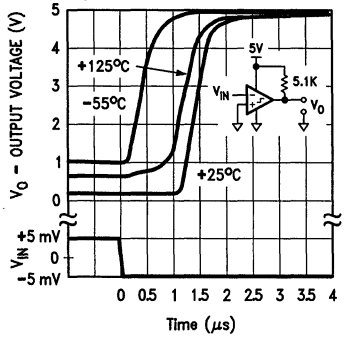
Input Bias Current vs Common-Mode Voltage



TL/H/9226-11

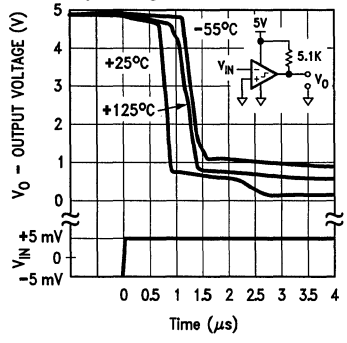
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Inverting Input, Positive Transition



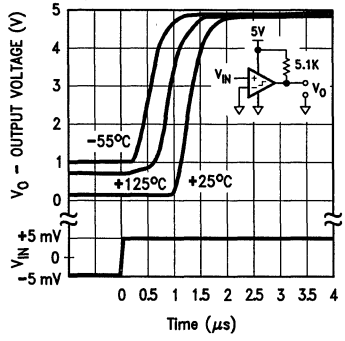
TL/H/9226–12

Comparator Response Times—Inverting Input, Negative Transition



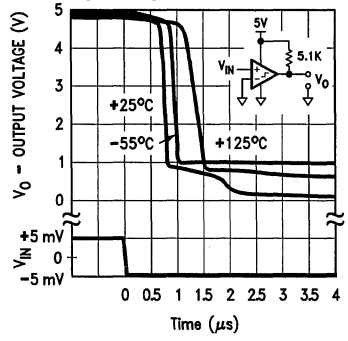
TL/H/9226–13

Comparator Response Times—Non-Inverting Input, Positive Transition



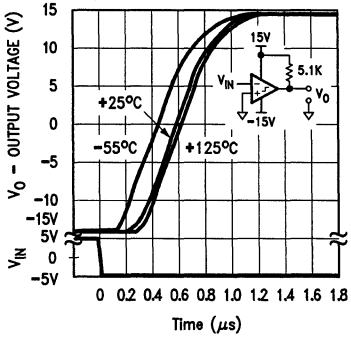
TL/H/9226–14

Comparator Response Times—Non-Inverting Input, Negative Transition



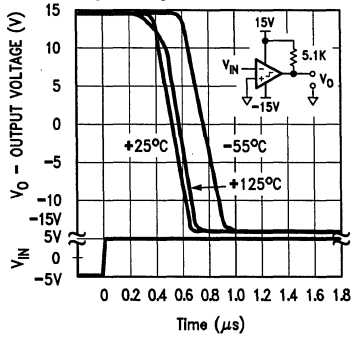
TL/H/9226–15

Comparator Response Times—Inverting Input, Positive Transition



TL/H/9226–16

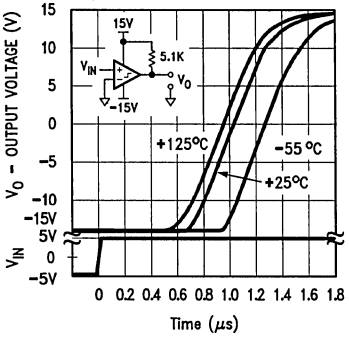
Comparator Response Times—Inverting Input, Negative Transition



TL/H/9226–17

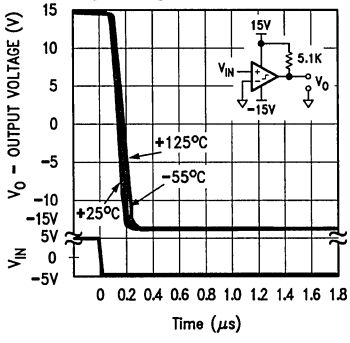
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Non-Inverting Input, Positive Transition



TL/H/9226–18

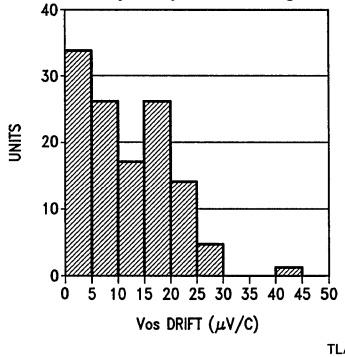
Comparator Response Times—Non-Inverting Input, Negative Transition



TL/H/9226–19

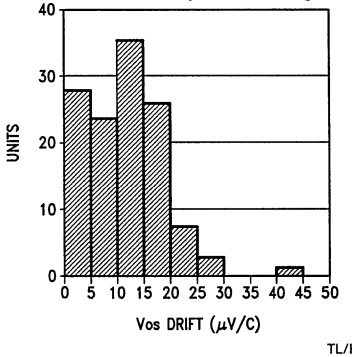
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



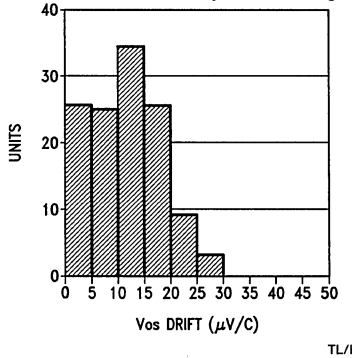
TL/H/9226–20

Average V_{OS} Drift Industrial Temperature Range



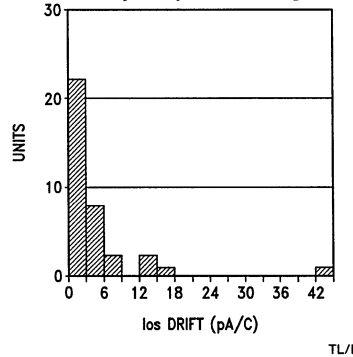
TL/H/9226–21

Average V_{OS} Drift Commercial Temperature Range



TL/H/9226–22

Average I_{OS} Drift Military Temperature Range

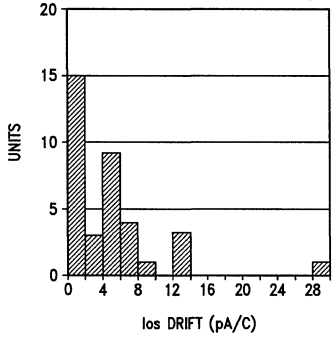


TL/H/9226–23

3

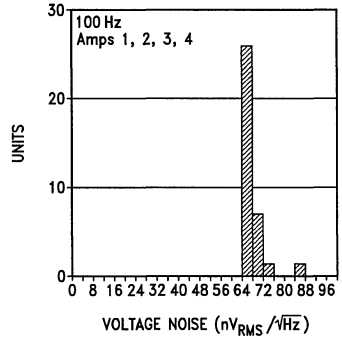
Typical Performance Distributions (Continued)

Average I_{OS} Drift Industrial Temperature Range



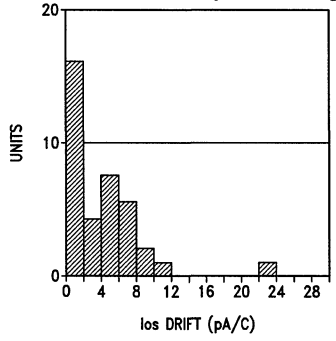
TL/H/9226-24

Op Amp Voltage Noise Distribution



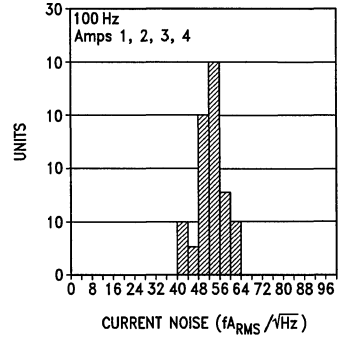
TL/H/9226-27

Average I_{OS} Drift Commercial Temperature Range



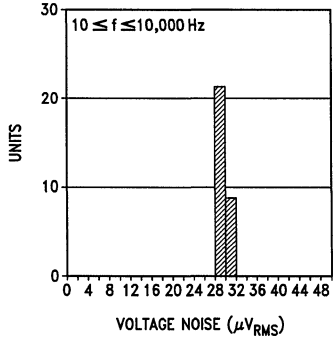
TL/H/9226-25

Op Amp Current Noise Distribution



TL/H/9226-28

Voltage Reference Broad-Band Noise Distribution



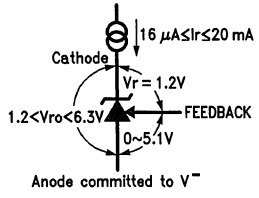
TL/H/9226-26

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.



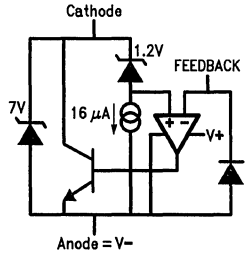
TL/H/9226-29

FIGURE 1. Voltage Associated with Reference (current source I_r is external)

Application Information (Continued)

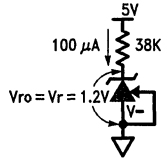
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9226–30

FIGURE 2. Reference Equivalent Circuit



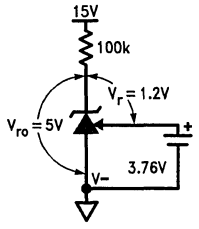
TL/H/9226–31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

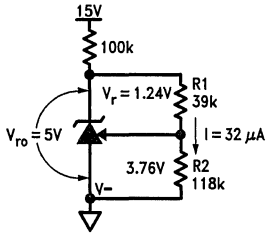
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Ancde with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part).



TL/H/9226–32

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



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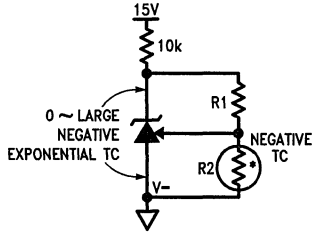
R1 = Vr/I = 1.24/32μ = 39k

R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9226–34

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

3

Application Information (Continued)

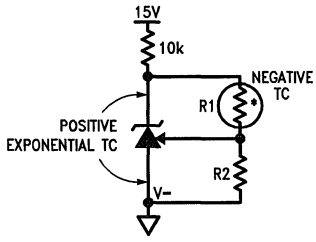


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FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

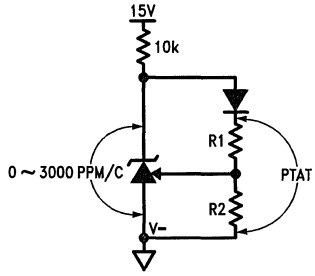

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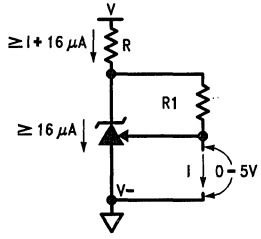
FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



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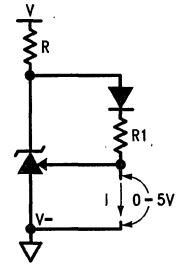
$I = Vr/R1 = 1.24/R1$

FIGURE 9. Current Source is Programmed by R1



TL/H/9226–38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source

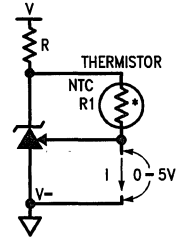


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FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating point that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.

Application Information (Continued)

2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA.

Op Amp and Comparator Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

For typical applications, refer to the LM124 Op Amp, LM139 Comparator, and LM185 Adjustable Reference datasheets.

National Semiconductor

LM614A/LM614 Quad Operational Amplifiers and Adjustable Reference

General Description

The quad operational amplifiers are a versatile common-mode-to-the-negative-supply ("single supply") type similar to the LM124 series, but with improved slew rate, improved power bandwidth, reduced cross-over distortion, and low supply current even while driven beyond swing limits. Lateral PNP input transistors enable low input currents for large differential input voltages and swings above V^+.

The voltage reference is a three-terminal shunt-type bandgap similar to the adjustable LM185 series, but with anode committed to the V^- terminal and improved voltage accuracy to ±0.4%. Two resistors program the reference from 1.24V to 6.3V. The reference features operation over a shunt current range of 16 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features (Guaranteed over temperature & supply)

Op Amps

■ Low operating current	250 μA (per op amp) 16 μA (reference)
■ Large supply voltage range	4V to 36V
■ Large output swing (10k load)	(V^- + 1V) to (V^+ − 1.8V)
■ Input common-mode includes	V^- to (V^+ − 1.4V)
■ Wide input differential voltage	±36V
■ Standard quad op amp pin-out	

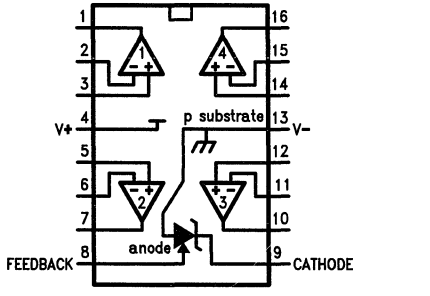
Reference

■ Adjustable output voltage	1.2V to 6.3V
■ Tight initial tolerance available	±0.4%
■ Tolerant of load capacitance	0 to ∞

Applications

- Power supplies
- Signal conditioning

Connection Diagram



TL/H/9326–1

Top View

Order Number LM614IJ, LM614MJ, LM614CWM, LM614IWM, LM614AIN, LM614CN or LM614IN
See NS Package Number J16A, M16B or N16A

Order Number

Prime Military — LM614MJ
Tested at −55°C, +25°C, +125°C
Drift tested at −55°C, +25°C, +125°C

Prime Industrial — LM614AIN
Tested at +25°C
Drift tested at −40°C, +25°C, +85°C

Industrial — LM614IN, LM614IJ, LM614IWM
Tested at +25°C

Commerical — LM614CN, LM614CWM
Tested at +25°C

Packages

J	Hermetic Dual-In-Line
N	Plastic Dual-In-Line
WM	Plastic Surface Mount Wide (0.3")

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin except Cathode Pin (referred to V^- pin)
(Note 1) −0.3V (Min)
Military and Industrial 36V
Commercial 32V

Current through Any Input Pin and Cathode Pin ±20 mA

Differential Input Voltage
Military and Industrial ±36V
Commercial ±32V

Short Circuit Duration, Op Amp (Note 2) Continuous

Storage Temperature Range −65°C to +150°C

Maximum Junction Temperature 150°C

Operating Junction Temperature Range T_{Min} to T_{Max}
LM614M −55°C to +125°C
LM614I −40°C to +85°C
LM614C 0°C to +70°C

Soldering Information
Dual-In-Line Package
(Soldering, 10 seconds) 260°C
Small Outline Package
Vapor Phase (60 seconds) 215°C
Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Package Thermal Resistance (Note 3)
Hermetic DIP J16 100°C/W
Molded DIP N16 95°C/W
Molded SO M16 Wide 140°C/W

ESD Tolerance (Note 4)
120 pF, 1.5 kΩ ±1 kV
200 pF, < 1Ω ±250V

Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for **T_{Min} to T_{Max}**.

Parameter	Conditions	Typical (Note 5)	LM614M Tested Limit (Note 6)	LM614M Design Limit (Note 7)	LM614AI, LM614I Tested Limit (Note 6)	LM614AI, LM614I Design Limit (Note 7)	LM614C Tested Limit (Note 6)	LM614C Design Limit (Note 7)	Units
Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ Over T_J Range (Commercial 32V)	450 **550**	900 **1000**		940	**1000**	1000	**1070**	μA max μA max
Supply Voltage Range	Meets Total Supply Current, and See V_R Change with V^+ Change Test	2.2 **2.9**	2.8 **3**		2.8	**3**	2.8	**3**	V min V min
		46 **43**	36 **36**		36	**36**	32	**32**	V max V max
OPERATIONAL AMPLIFIERS									
V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ Commercial)	±1.5 **±2.0**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.4V$), V^+ = 30V	±1.0 **±1.5**	±3.5 **±5.0**		±3.5	**±6.0**	±5.0	**±7.0**	mV max mV max
Average V_{OS} Drift	LM614M & AI, Op Amp 3 Only (Note 8)	**15**	**25**		**30**				μV/°C max
Input Bias Current	I_{B+IN} and I_{B-IN}	−10 **−11**	±20 **±25**		±25	**±30**	±35	**±40**	nA max nA max
Input Offset Current	$I_{OS} = I_{B+IN} - I_{B-IN}$	±0.2 **±0.3**	±4 **±4**		±4	**±5**	±4	**±5**	nA max nA max
Average I_{OS} Drift		**±4**							pA/°C

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{Min} to T_{Max}.

Parameter	Conditions	Typical (Note 5)	LM614M		LM614AI, LM614I		LM614C		Units
			Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
Input Resistance	Differential: Common-Mode:	1800 3800							MΩ MΩ
Input Cap.	C-to-GND, Non-Inverting Input of Follower	5.7							pF
Voltage Noise	100 Hz, Input Referred	74							nV/√Hz
Current Noise	100 Hz Bias Current Noise	58							fA/√Hz
Common-Mode Reject Ratio	V^+ = 30V, 0V ≤ V_{CM} ≤ (V^+ − 1.4V), CMRR = 20 log {$\Delta V_{CM}/\Delta V_{OS}$}	95 **90**	85 **80**		80	**75**	75	**70**	dB min dB min
Power Supply Reject Ratio	4V ≤ V^+ ≤ 30V, $V_{CM} = V^+/2$, PSRR = 20 log {$\Delta V^+/\Delta V_{OS}$}	110 **100**	85 **80**		80	**75**	75	**70**	dB min dB min
Voltage Gain, Open Loop	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V, Open-Loop $A_V = \lvert\Delta V_{OUT}/\Delta V_{INDIFF}\rvert$	500 **50**	100 **40**		100	**40**	94	**40**	V/mV min
Slew Rate	V^+ = 30V (Note 9)	±0.70 **±0.65**	±0.55 **±0.45**		±0.55	**±0.45**	±0.50	**±0.45**	V/μs min
Gain-Bandwidth	Closed Loop Gain = −1000, −3 dB Frequency × Gain, C_L = 50 pF	0.79 **0.52**							MHz
Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V Commercial)	$V^+ - 1.4$ $\mathbf{V^+ - 1.6}$	$V^+ - 1.6$ $\mathbf{V^- - 1.8}$		$V^+ - 1.7$	$\mathbf{V^+ - 1.9}$	$V^+ - 1.8$	$\mathbf{V^+ - 1.9}$	V min V min
Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V Commercial)	$V^- + 0.8$ $\mathbf{V^- + 0.9}$	$V^- + 0.90$ $\mathbf{V^- + 1.0}$		$V^- + 0.90$	$\mathbf{V^- + 1.0}$	$V^- + 0.95$	$\mathbf{V^- + 1.0}$	V max V max
I_{OUT} Source	$V_{OUT} = V^+ - 2.5V$, V_{+IN} = 0V, V_{-IN} = −0.3V	−25 **−15**	−20 **−13**		−20	**−13**	−16	**−13**	mA max mA max

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, any package, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply for T_{Min} to T_{Max}.

Parameter	Conditions	Typical (Note 6)	LM614M		LM614AI, LM614I		LM614C		Units
			Tested Limit (Note 7)	Design Limit (Note 8)	Tested Limit (Note 7)	Design Limit (Note 8)	Tested Limit (Note 7)	Design Limit (Note 8)	
I_{OUT} Sink	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	15 **8**		14	 **11**	13	 **11**	mA min mA min
Short-Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source:	−30 **−40**	−37 **−46**		−40	 **−48**	−43	 **−50**	mA min mA min
	V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink:	30 **32**	40 **60**		60	 **80**	70	 **90**	mA max mA max
VOLTAGE REFERENCE (Note 10)									
Reference Voltage		1.244	1.2390 1.2490 (±0.4%)		1.2365 1.2515 (±0.6%)		1.2191 1.2689 (±2%)		V min V max
Average Temp. Drift	(Note 11) LM614AI	**10**	**20**		 **20**	**80**		**150**	PPM/C max
Average Time Drift	T_J = 40°C T_J = 150°C	400 1000							PPM/kHr PPM/kHr
Hysteresis	Hyst = (Vro′ − Vro)/ΔT_J (Note 12)	**±3.2**							μV/C
V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[16\ \mu A]}$	0.05 **0.1**	±1 **±1**		±1	 **±1.1**	±1	 **±1.1**	mV max mV max
	$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 13)	1.5 **3.0**	5 **5**		5	 **5.5**	5	 **5.5**	mV max mV max
Resistance	$\Delta V_{R[10 \rightarrow 0.1\ mA]}$/9.9 mA: $\Delta V_{R[100 \rightarrow 16\ \mu A]}$/84 μA:	0.2 0.6		**0.51** **12**		**0.56** **13**		**0.56** **13**	Ω max Ω max
V_R Change with High V_{RO}	$V_{R[Vro\ =\ Vr]} - V_{R[Vro\ =\ 6.3V]}$ {5.06V between Anode and FEEDBACK}	2.5 **2.8**	5 **8**		7	 **10**	7	 **10**	mV max mV max
V_R Change with V^+ Change	$V_{R[V^+\ =\ 5V]} - V_{R[V^+\ =\ 36V]}$ (V^+ = 32V Commercial)	0.1 **0.1**	±1.2 **±1.2**		±1.2	 **±1.3**	±1.2	 **±1.3**	mV max mV max
	$V_{R[V^+\ =\ 5V]} - V_{R[V^+\ =\ 3V]}$	0.01 **0.01**	±1 **±1**		±1	 **±1.5**	±1	 **±1.5**	mV max mV max
FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \leq V_{FB} \leq$ 5.06V	−22 **−29**	−35 **−40**		−35	 **−40**	−50	 **−55**	nA min nA min
V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30							μV_{RMS}

Electrical Characteristics Notes

Note 1: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltage on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 2: Simultaneous short-circuit of multiple op amps and reference while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{jA}$. The given thermal resistances are worst-case for packages in sockets in still air. Nominal θ_{jA} are 85°C/W for LM614 in J package, 80°C/W for the N package, and 110°C/W for the WM package, for packages soldered to copper-clad board with dissipation from one op amp or reference output transistor.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply to the military temperature range. These values represent the most likely parametric norm.

Note 6: Tested limits are guaranteed and 100% tested.

Note 7: Design limits are guaranteed via correlation, but are not 100% tested.

Note 8: Offset voltage drift is calculated from the measurement of the offset voltage at 25°C and at the temperature extremes. The drift is $\Delta V_{OS}/\Delta T$, where ΔV_{OS} is the lowest value subtracted from the highest, and ΔT is the temperature range.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_{ro} is the Cathode-to-Anode voltage (i.e. the reference output voltage, 1.2V to 6.3V). V_r is the Cathode-to-FEEDBACK voltage (nominally 1.2V).

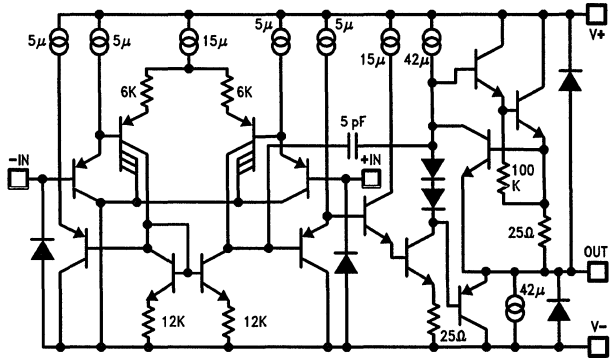
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range.

Note 12: Hysteresis is $\Delta V_{RO}/\Delta T_J$, where ΔV_{RO} is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 125°C, −55°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp



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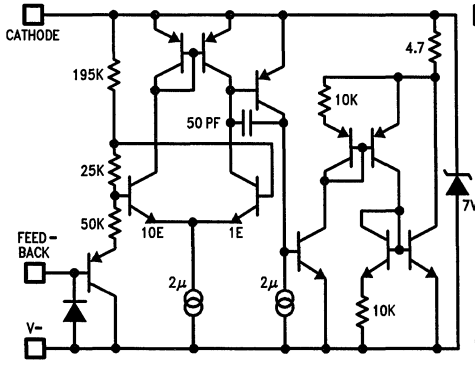
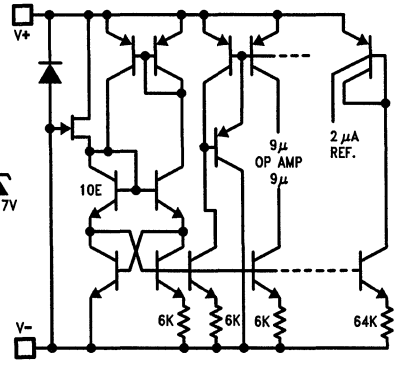
Reference



Bias

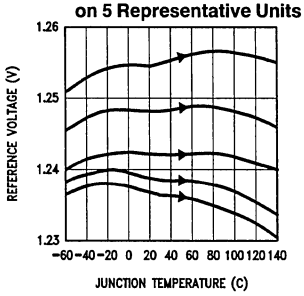


TL/H/9326–3

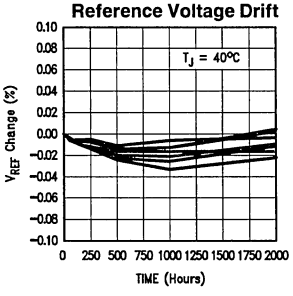
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

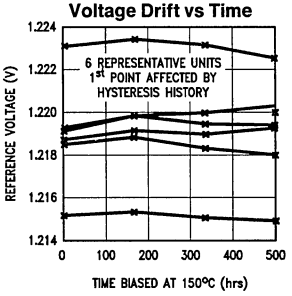
Reference Voltage vs Temperature on 5 Representative Units



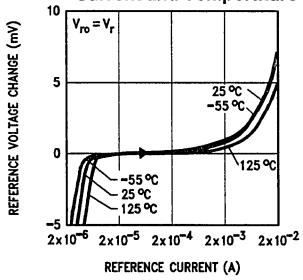
Reference Voltage Drift



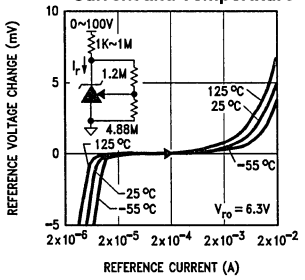
Accelerated Reference Voltage Drift vs Time



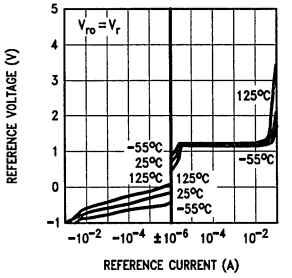
Reference Voltage vs Current and Temperature



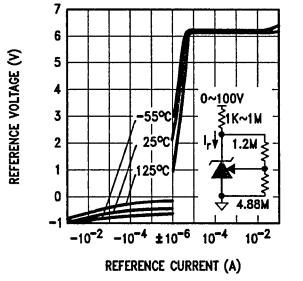
Reference Voltage vs Current and Temperature



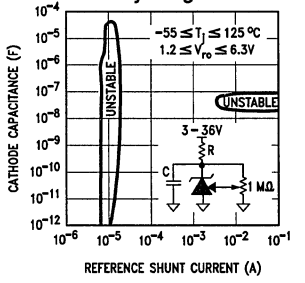
Reference Voltage vs Reference Current



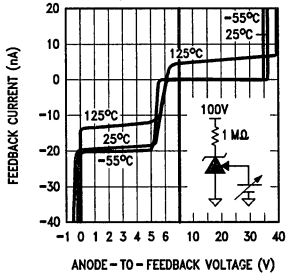
Reference Voltage vs Reference Current



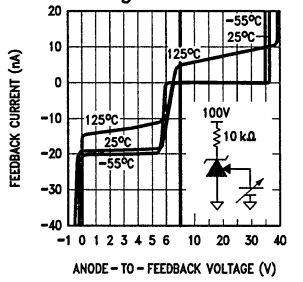
Reference AC Stability Range



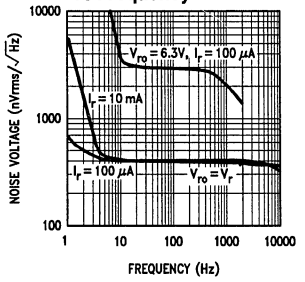
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



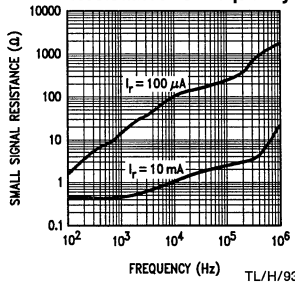
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency



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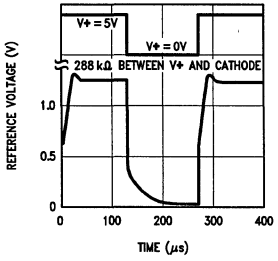
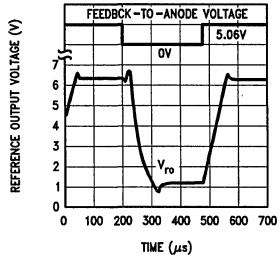
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

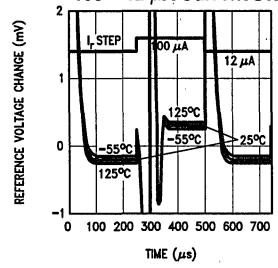
Reference Power-Up Time



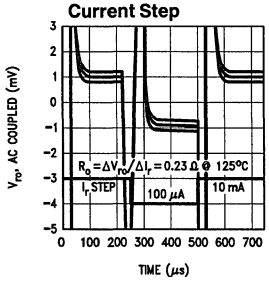
Reference Voltage with FEEDBACK Voltage Step



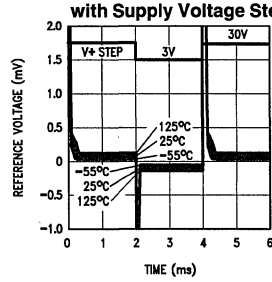
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



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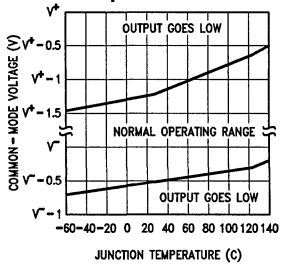
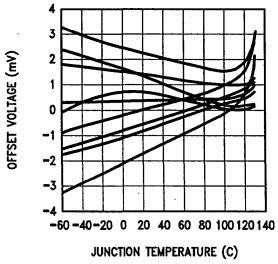
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = OV, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

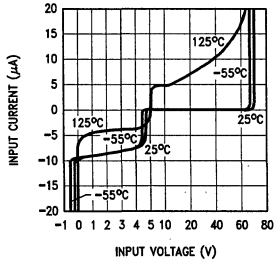
Input Common-Mode Voltage Range vs Temperature



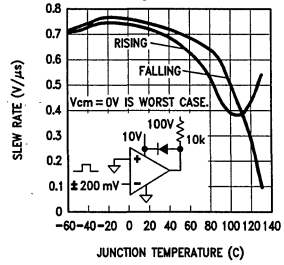
V_{OS} vs Junction Temperature on 9 Representative Units



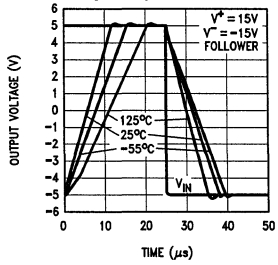
Input Bias Current vs Common-Mode Voltage



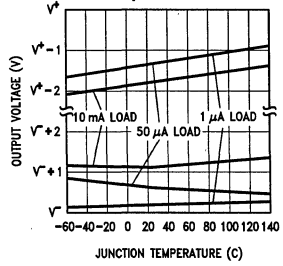
Slew Rate vs Temperature and Output Sink Current



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current



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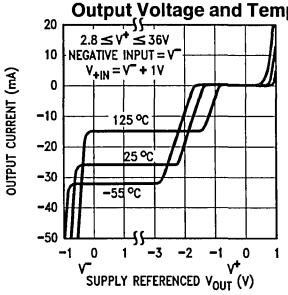
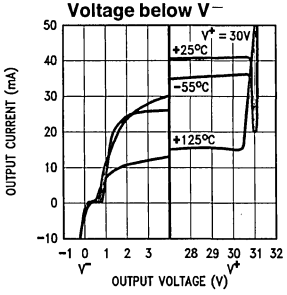
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

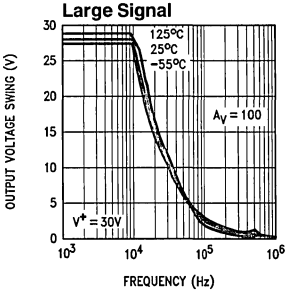
Output Sink Current vs Output Voltage and Temp.



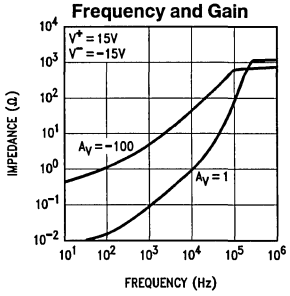
Slew Rate vs. Temp with Common-Mode Voltage below V−



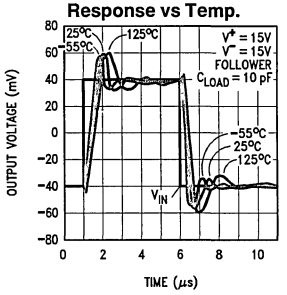
Output Swing, Large Signal



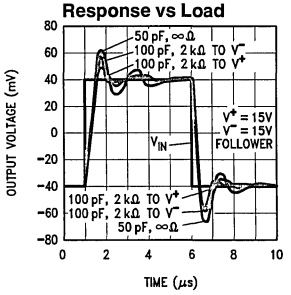
Output Impedance vs Frequency and Gain



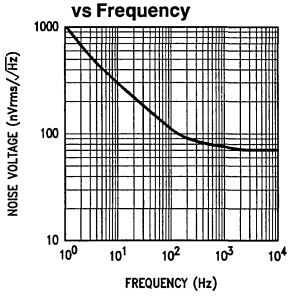
Small-Signal Pulse Response vs Temp.



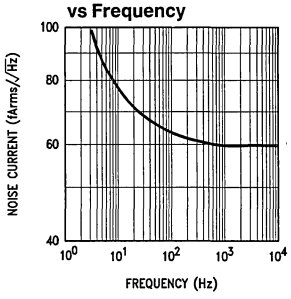
Small-Signal Pulse Response vs Load



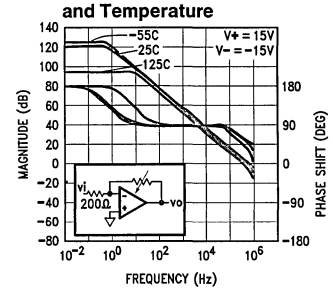
Op Amp Voltage Noise vs Frequency



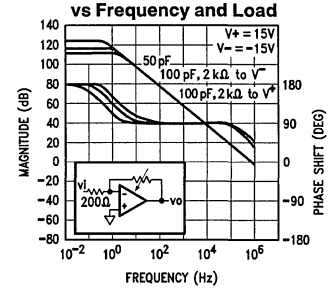
Op Amp Current Noise vs Frequency



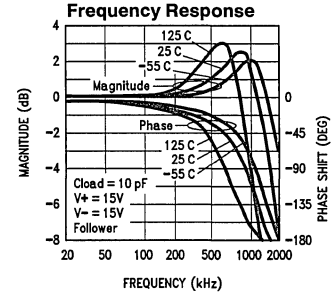
Small-Signal Voltage Gain vs Frequency and Temperature



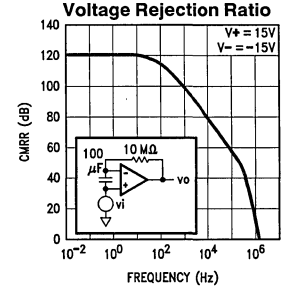
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

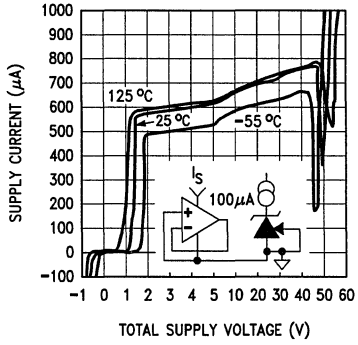


TL/H/9326–6

Typical Performance Characteristics (Op Amps) (Continued)

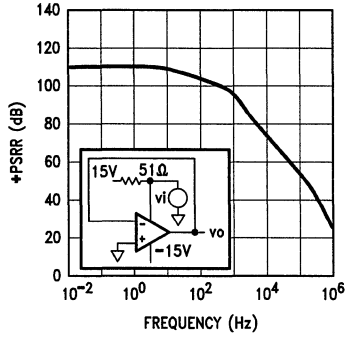
$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Power Supply Current vs Power Supply Voltage



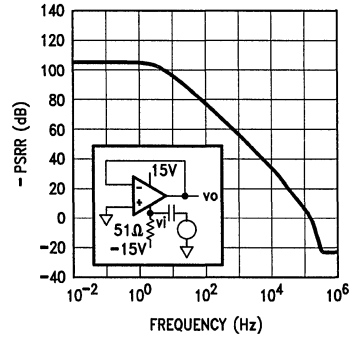
TL/H/9326-7

Positive Power Supply Voltage Rejection Ratio



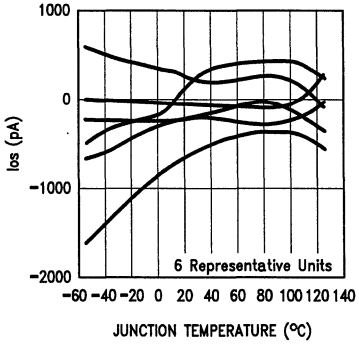
TL/H/9326-21

Negative Power Supply Voltage Rejection Ratio



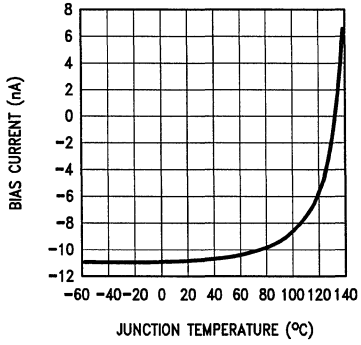
TL/H/9326-22

Input Offset Current vs Junction Temperature



TL/H/9326-24

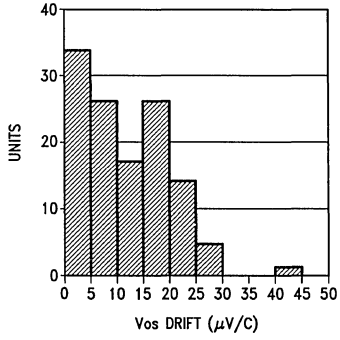
Input Bias Current vs Junction Temperature



TL/H/9326-38

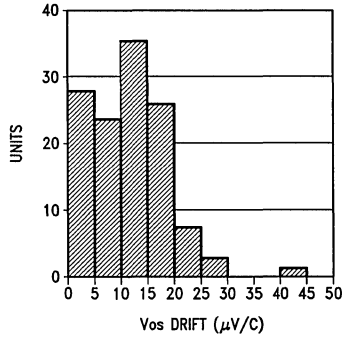
Typical Performance Distributions

Average V_{OS} Drift
Military Temperature Range



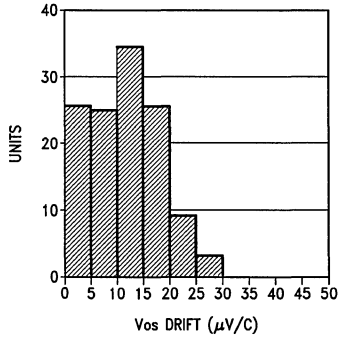
TL/H/9326–29

Average V_{OS} Drift
Industrial Temperature Range



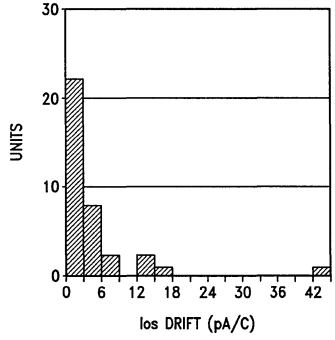
TL/H/9326–30

Average V_{OS} Drift
Commercial Temperature Range



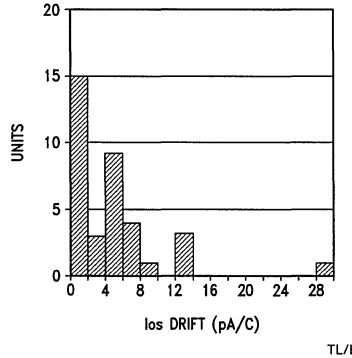
TL/H/9326–31

Average I_{OS} Drift
Military Temperature Range



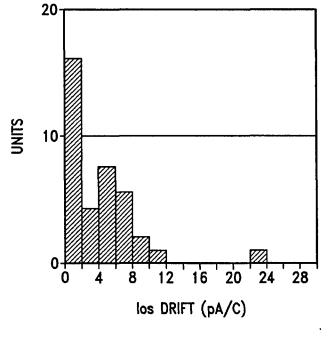
TL/H/9326–32

Average I_{OS} Drift
Industrial Temperature Range



TL/H/9326–33

Average I_{OS} Drift
Commercial Temperature Range

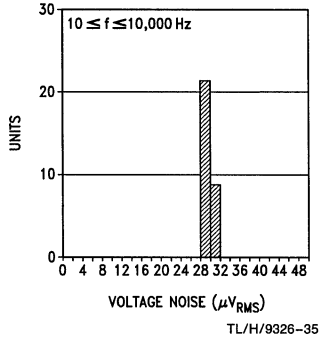


TL/H/9326–34

3

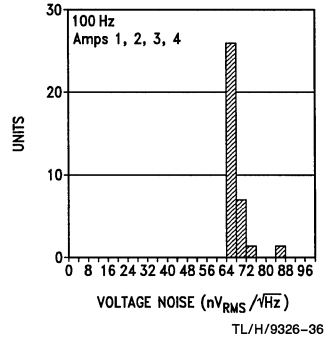
Typical Performance Distributions (Continued)

Voltage Reference Broad-Band Noise Distribution



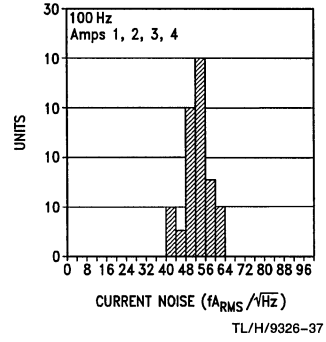
TL/H/9326-35

Op Amp Voltage Noise Distribution



TL/H/9326-36

Op Amp Current Noise Distribution



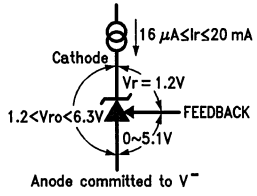
TL/H/9326-37

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.



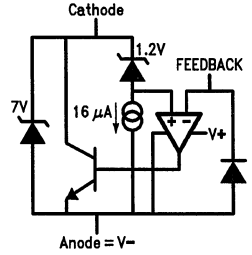
TL/H/9326-9

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

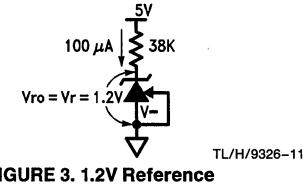
To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.



TL/H/9326-10

FIGURE 2. Reference Equivalent Circuit



TL/H/9326-11

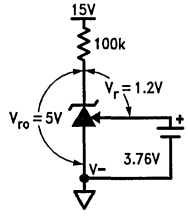
FIGURE 3. 1.2V Reference

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then V_{ro} = V_r = 1.24V. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constaint V_r generates a current I = R1/V_r flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2 = 3.76/I. Keep I

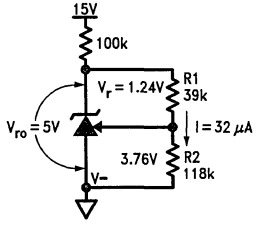
Application Information (Continued)

greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part.)



TL/H/9326–12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



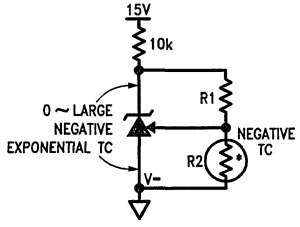
TL/H/9326–13

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\{(Vro/Vr) - 1\} = 39k\{(5/1.24) - 1)\} = 118k$$

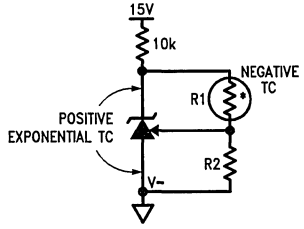
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



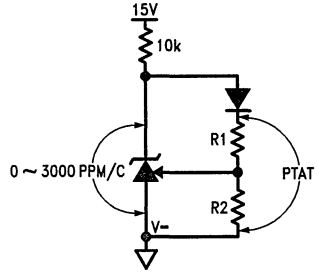
TL/H/9326–14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9326–15

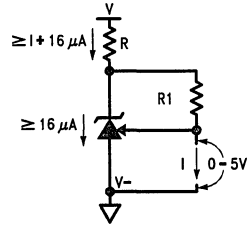
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9326–16

FIGURE 8. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

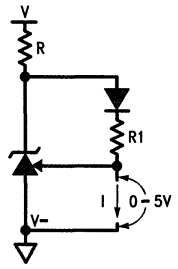


TL/H/9326–17

$$I = Vr/R1 = 1.24/R1$$

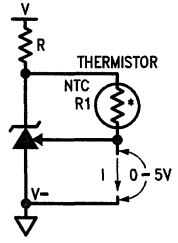
FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9326–18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9326–19

FIGURE 11. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). One amp input may be outside the common-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

OP Amp Output Stage

These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain
2) Cross-over Distortion: The LM614 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

OP Amp Input Stage

The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

For typical applications, refer to the LM124 Op Amp and LM185 Adjustable Reference datasheets.

National Semiconductor

LM627/LM637
Precision Operational Amplifiers

General Description

The LM627/LM637 series feature extremely low noise and excellent precision along with high speed. Voltage noise is a low 3 nV/$\sqrt{Hz}$ in the flat band and rises to only 3.5 nV/$\sqrt{Hz}$ at 10 Hz. The A grades offer guaranteed specifications of 25 μV offset voltage and 0.3 μV/°C drift, and their *guaranteed* 126 dB CMRR, 120 dB PSRR and voltage gain of 5 Million ensure an ultra-low V_{OS} under all conditions.

The unity-gain stable LM627 is nearly twice as fast as the OP-27 with a slew rate of 4.5 V/μs and a 14 MHz gain-bandwidth product. Stable at gains of 5 or more, the decompensated LM637 is considerably faster.

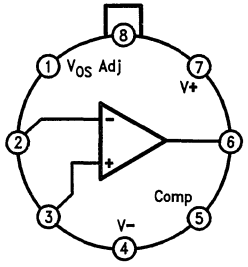
Other enhancements of the LM627/LM637 include a guaranteed 600Ω load drive capability over temperature: ±10V output swing at voltage gains over one million. Bias current has been reduced to 10 nA for the A and B grades and 25 nA for the C grade. Furthermore the LM627 may be overcompensated to allow it to drive capacitive loads up to 2000 pF while maintaining its superb dc specs.

Features

- Low Noise — 3 nV/$\sqrt{Hz}$@1 kHz; 3.5 nV/$\sqrt{Hz}$@ 10 Hz
- Low V_{OS} — 25 μV Max
- Low Drift — 0.3 μV/°C Max
- Offset Drift 100% Tested (A and B grades)
- Noise Voltage 100% Tested (A and B grades)
- High Gain — 5 Million Min
- High CMRR — 126 dB Min
- High PSRR — 120 dB Min
- High Speed
  - LM627: 14 MHz Gain-Bandwidth; 4.5 V/μs Slew Rate
  - LM637: 65 MHz Gain-Bandwidth; 14 V/μs Slew Rate
- *Guaranteed* 600Ω drive over temperature
- Wide Power Supply Range — ±3.5V to ±18V
- Overcompensation Pin — Allows driving high C_L

Connection Diagrams

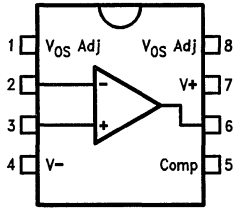
Metal Can Package



TL/H/9212–1

Top View

DIP Packages



TL/H/9212–2

Ordering Information

LM627

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM627AMH LM627BMH	LM627ACH LM627BCH LM627CH	H08C
8-Pin Cerdip	LM627AMJ LM627BMJ	LM627ACJ LM627BCJ LM627CJ	J08A
8-Pin Molded DIP		LM627ACN LM627BCN LM627CN	N08E

LM637

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM637AMH LM637BMH	LM637ACH LM637BCH LM637CH	H08C
8-Pin Cerdip	LM637AMJ LM637BMJ	LM637ACJ LM637BCJ LM637CJ	J08A
8-Pin Molded DIP		LM637ACN LM637BCN LM637CN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Overdrive Current (Note 7)	±25 mA
Supply Voltage	44V
Input Voltage	Supply Voltage
Output Short Circuit to Gnd	Continuous
Power Dissipation (Note 8)	
Molded DIP	1300 mW
Ceramic DIP	1190 mW
Metal Can	830 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 sec.)	260°C
Maximum Junction Temperature	150°C
ESD Rating	3 kV
C_{ZAP} = 100 pF, R_{ZAP} = 1.5 kΩ	

Operating Ratings

Temperature Range (Note 8)	
AM and BM grades	$-55°C \le T_J \le +125°C$
AC, BC, and C grades	$-25°C \le T_J \le +85°C$

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0 and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM627AM LM637AM		LM627BM LM637BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **55**		50 **110**		μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**		μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2					μV/mo Max
Input Bias Current		3	10 **20**		10 **20**		nA Max
Input Offset Current		2	10 **20**		10 **20**		nA Max
Input Noise Voltage	0.1 to 10Hz	0.08		0.18		0.18	μV p-p Max
Input Noise Voltage Density	f = 10Hz f = 30Hz f = 1kHz	3.5 3.1 3.0	5.5 4.5 3.8		5.5 4.5 3.8		$nV/\sqrt{Hz}$ Max
Input Noise Current Density	f = 10Hz f = 30Hz f = 1kHz	1.7 1.0 0.4					$pA/\sqrt{Hz}$ Max
Input Resistance	Common-Mode	20					GΩ
Input Voltage Range		±12	±11.5 **±10.5**		±11.5 **10.5**		V Min
Common-Mode Rejection Ratio	V_{CM} = ±11.5V **V_{CM} = ±10.5V**	140	126 **120**		126 **120**		dB Min
Power Supply Rejection Ratio	V_S = ±3.5V to ±18V	140	120 **117**		120 **117**		dB Min
Large-Signal Voltage Gain	V_O = ±12V $R_L \ge 2$ kΩ V_O = ±10V $R_L \ge 1$ kΩ $R_L \ge 600$Ω	10000 7000 6000	5000 **3000** 4000 **2000** 3000 **1500**		5000 **2000** 3500 **1500** 2000 **1000**		V/mV Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM627AM LM637AM		LM627BM LM637BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±13.8	±13 **±12.5**		±13 **±12.5**		V Min
	$R_L \geq 600\Omega$	±12.5	±11 **±10.5**		±11 **±10.5**		
Slew Rate	LM627 R_L = 2k	4.5		3		3	V/μs
	LM637	14		10		10	Min
Gain-Bandwidth Product	LM627 f = 10 kHz	14		10		10	MHz
	LM637	65		45		45	Min
Output Resistance	Open Loop	50					Ω
Supply Current		3	4.5 **5.5**		4.5 **5.5**		mA Max
Offset Adjust Range	$R_P \geq 10\,k\Omega$	±2					mV

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0 and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM627AC LM637AC		LM627BC LM637BC		LM627C LM637C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **50**		50 **110**		100	**210**	μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.6**		**1.0**			**1.8**	μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2							μV/mo Max
Input Bias Current		3	10	**20**	10	**20**	25	**50**	nA Max
Input Offset Current		2	10	**20**	10	**20**	25	**50**	nA Max
Input Noise Voltage	0.1 to 10 Hz	0.08		0.18		0.18		0.25	μV p-p Max
Input Voltage Noise Density	f = 10 Hz	3.5	5.5		5.5			8.0	$nV/\sqrt{Hz}$
	f = 30 Hz	3.1	4.5		4.5			5.6	
	f = 1 kHz	3.0	3.8		3.8			4.5	Max
Input Noise Current Density	f = 10 Hz	1.7							$pA/\sqrt{Hz}$
	f = 30 Hz	1.0							
	f = 1 kHz	0.4							Max
Input Resistance	Common Mode	20							GΩ
Input Voltage Range		±12	±11.5	**±11**	±11.5	**±11**	±11.5	**±11**	V Min
Common-Mode Rejection Ratio	V_{CM} = ±11.5V	140	126	**120**	126	**120**	120	**116**	dB Min
	V_{CM} = ±11V								
Power Supply Rejection Ratio	V_S = ±3.5V to ±18V	140	120	**117**	120	**117**	110	**108**	dB Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM627AC LM637AC		LM627BC LM637BC		LM627C LM637C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Large-Signal Voltage Gain	$V_O = \pm 12V$ $R_L \geq 2k\Omega$	10000	5000	**3000**	5000	**3000**	4000	**2500**	V/mV Min
	$V_O = \pm 10V$ $R_L \geq 1k\Omega$	7000	4000	**2500**	3500	**2000**	2500	**1500**	
	$R_L \geq 600\Omega$	6000	3000	**2000**	2000	**1500**	1500	**1000**	
Output Voltage Swing	$R_L \geq 2k\Omega$	±13.8	±13	**±12.5**	±13	**±12.5**	±13	**±12.5**	V Min
	$R_L \geq 600\Omega$	±12.5	±11	**±10.5**	±11	**±10.5**	±10.5	**±10**	
Slew Rate	LM627 $R_L = 2k$	4.5		3		3		3	V/μs Min
	LM637	14		10		10		10	
Gain-Bandwidth Product	LM627 $f = 10$ kHz	14		10		10		10	MHz Min
	LM637	65		45		45		45	
Output Resistance	Open Loop	50							Ω
Supply Current		3	4.5	**5**	4.5	**5**	4.8	**5.2**	mA Max
Offset Adjust Range	$R_P \geq 10\ k\Omega$	±2							mV

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 5 μV settling out in 5 minutes. The LM627C/LM637C offset voltage is measured by automated test equipment within 200 ms of applying power.

Note 3: Input offset voltage drift is defined as $(V_{OS}(85°C) - V_{OS}(-25°C))/110°C$ for the industrial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $(V_{OS}(25°C) - V_{OS}(-55°C))/80°C$ and $(V_{OS}(125°C) - V_{OS}(25°C))/100°C$.

Note 4: Input offset voltage long term stability refers to the average trend line of V_{OS} vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2 μV.

Note 5: Guaranteed and 100% production tested. These limits are used to calculate outgoing quality levels.

Note 6: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

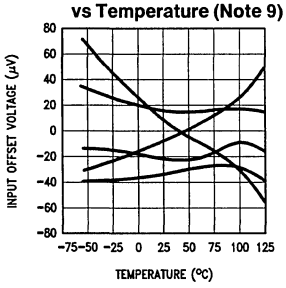
Note 8: For operation above 25°C, the maximum power dissipation specification must be derated. Typical junction-to-ambient thermal resistance of the molded DIP and the ceramic DIP are 95°C/W and 105°C/W respectively. The metal can package has a typical junction-to-ambient thermal resistance of 150°C/W and a typical junction-to-case thermal resistance of 17°C/W.

Note 9: These units selected to illustrate the types of variations that may be encountered. (This note refers to particular curves within the Typical Performance Characteristics.)

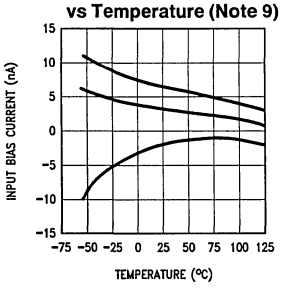
Typical DC Performance Characteristics (LM627, LM637)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$ unless othewise indicated.

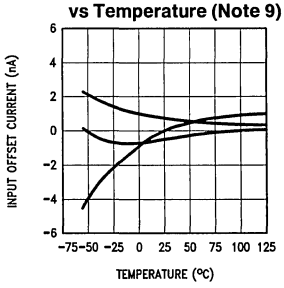
Input Offset Voltage of 5 Representative Units vs Temperature (Note 9)



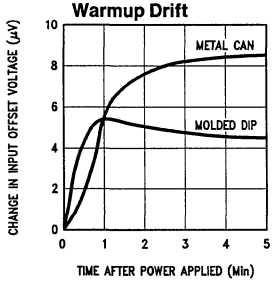
Input Bias Current of 3 Representative Units vs Temperature (Note 9)



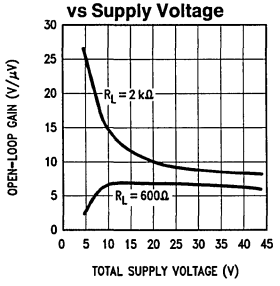
Input Offset Current of 3 Representative Units vs Temperature (Note 9)



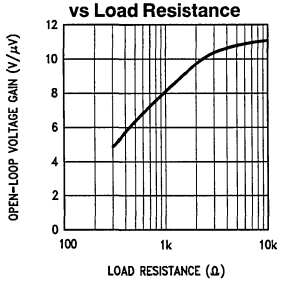
Warmup Drift



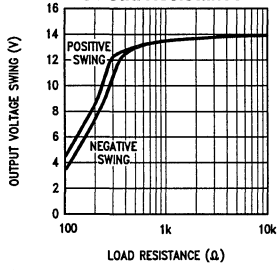
Open Loop Gain vs Supply Voltage



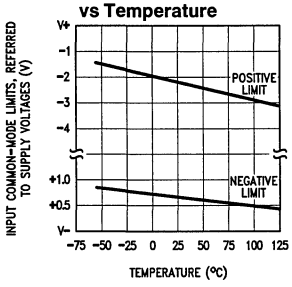
Open Loop Gain vs Load Resistance



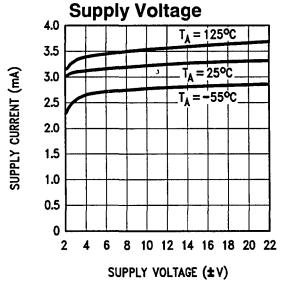
Output Voltage Swing vs Load Resistance



Input Common-Mode Limits vs Temperature



Supply Current vs Supply Voltage

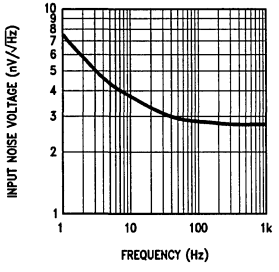


TL/H/9212-9

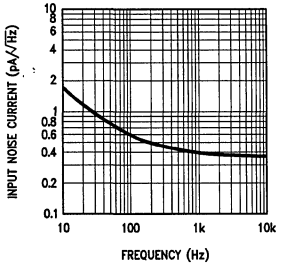
Typical Noise Characteristics (LM627, LM637)

$V_S = \pm 15V$, $T_A = 25°C$

Noise Voltage vs Frequency



Noise Current vs Frequency

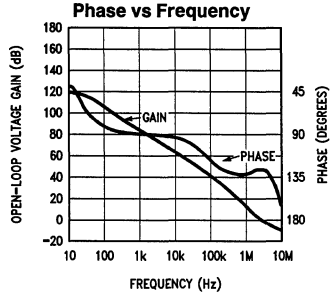


TL/H/9212-10

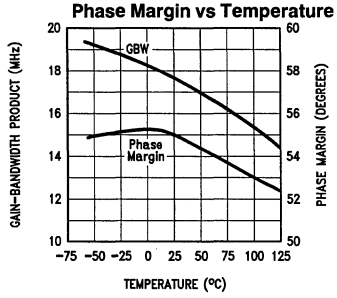
Typical AC Performance Characteristics (LM627)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$

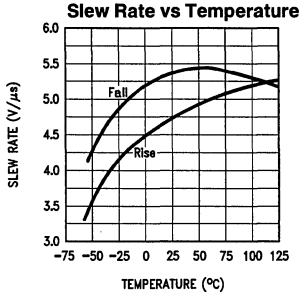
Open-Loop Gain and Phase vs Frequency



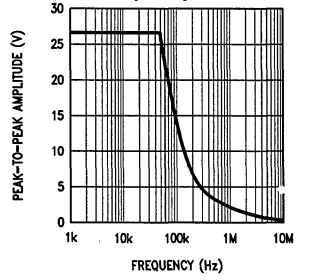
Gain-Bandwidth Product, Phase Margin vs Temperature



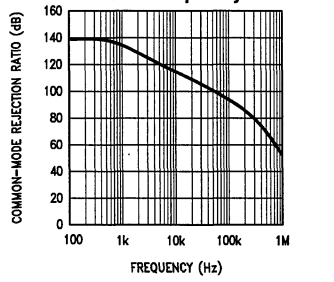
Slew Rate vs Temperature



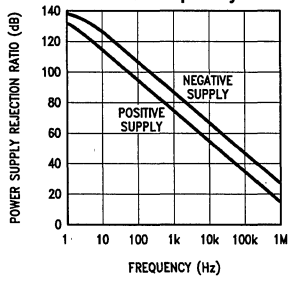
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

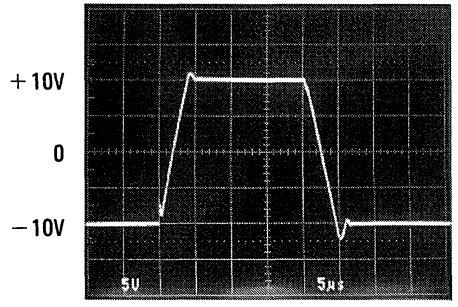


Power Supply Rejection Ratio vs Frequency



TL/H/9212–11

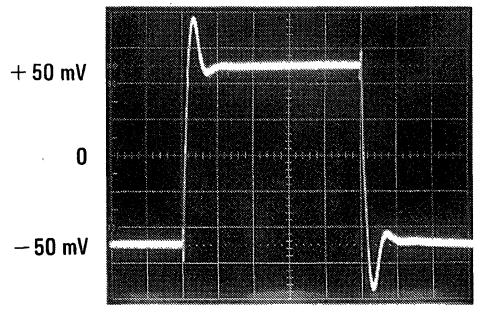
Large-Signal Pulse Response, $A_V = +1$



TIME (5 μs/DIV)

TL/H/9212–12

Small-Signal Pulse Response, $A_V = +1$



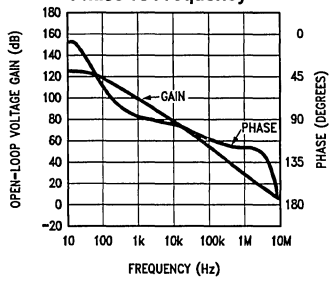
TIME (500 ns/DIV)

TL/H/9212–13

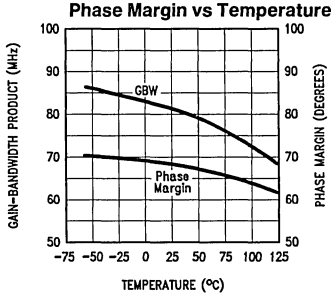
Typical AC Performance Characteristics (LM637)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$

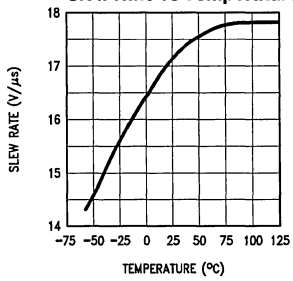
Open-Loop Gain and Phase vs Frequency



Gain-Bandwidth Product, Phase Margin vs Temperature

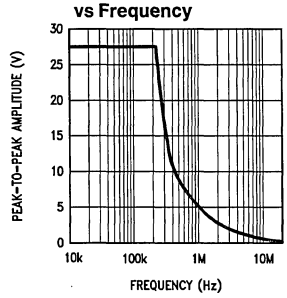


Slew Rate vs Temperature

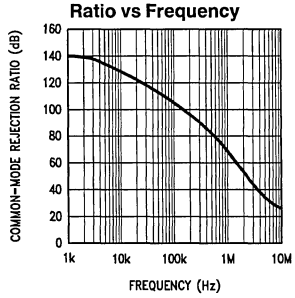


TL/H/9212–14

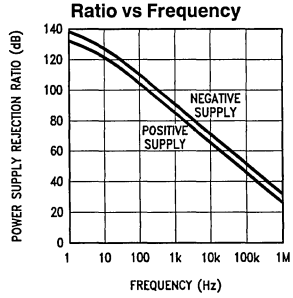
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

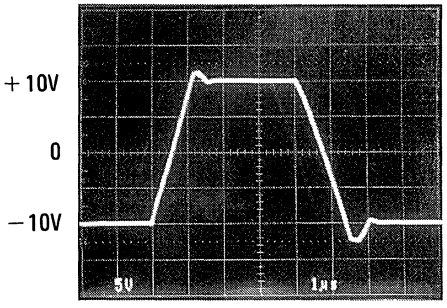


Power Supply Rejection Ratio vs Frequency



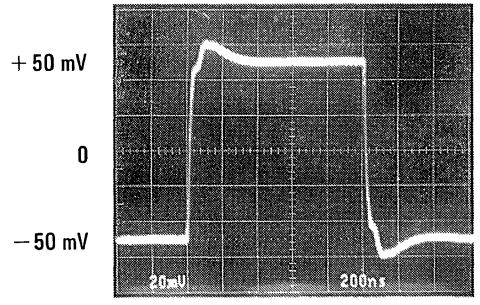
TL/H/9212–15

Large-Signal Pulse Response, $A_V = +5$



TIME (1 μs/DIV)

Small-Signal Pulse Response, $A_V = +5$



TIME (200 ns/DIV)

TL/H/9212–16

TL/H/9212–17

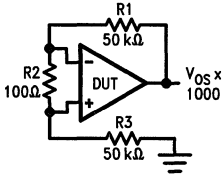
Application Hints

OFFSET VOLTAGE

Offset voltage of the LM627/637 is internally trimmed to a very low value. The data sheet V_{OS} specification applies at $T_J = 25°C$, $V_{CM} = 0$ and $\pm 15V$ supplies. For other temperatures, common-mode voltages, and supply voltages, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Since the LM627/LM637C offset voltage is measured within 200 ms of applying power, the 5 μV typical warmup drift is not accounted for in the measurement. Fortunately, the warmup drift is a small fraction of its 100 μV max offset. For the 25 μV A and 50μV B grades, the offset voltage is measured with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure V_{OS} with high accuracy, V_{OS} must be amplified right at the device as shown; otherwise the offset voltage can be obscured by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimize airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal EMF. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

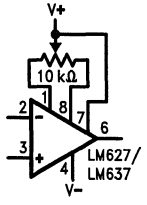


TL/H/9212–3

FIGURE 1. Offset Voltage Test Circuit

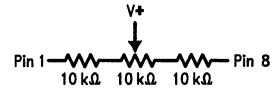
OFFSET NULLING

This is usually not required on the LM627/637 family since its offset voltage is internally trimmed. An offset adjust range of approximately ± 2 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2.* With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiomer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. The circuit of *Figure 3,* which uses this technique, has an adjustment range of ± 200 μV. Because adjusting the offset voltage of an LM627/637 will alter its offset voltage temperature drift, caution is advised.



TL/H/9212–4

FIGURE 2. Offset Adjust Circuit



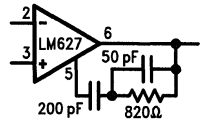
TL/H/9212–5

FIGURE 3. Improved Sensitivity Offset Adjust

Every 100μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM627C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

OVERCOMPENSATION

Without any external compensation, the LM627 is stable at unity gain and up to 500 pF load capacitance. It has a slew rate of 4.5 V/μs and a gain-bandwidth product of 14 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4.* This increases maximum capacitive loading to 2000 pF while decreasing slew rate to 1.5 V/μs and bandwidth to 1.5 MHz. If overcompensation of the LM627 (or the LM637) is not desired, pin 5 should be left open.

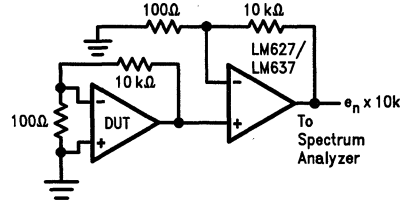


TL/H/9212–6

FIGURE 4. Overcompensation

NOISE

When measuring spot noise voltage, a circuit as shown in *Figure 5* is recommended. The DUT running at a gain of 100 will not roll off until approximately 140 kHz. Adding the second gain of 100 amplifier brings total DUT-input-referred gain up to 10,000, which minimizes to minimize sensitivity to EMI in the environment. When measuring spot noise at 30 Hz, it is recommended that the spectrum analyzer bandwidth be 20 Hz or less to minimize pickup at line frequency.

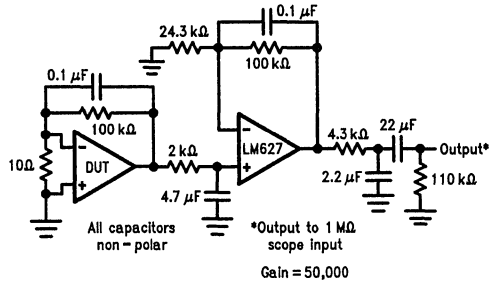


TL/H/9212–7

FIGURE 5. Spot Noise Test Circuit

Application Hints (Continued)

The circuit used to measure peak-to-peak noise voltage in the 0.1 to 10 Hz range is shown in *Figure 6.* The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, as does the single zero rolloff. The measuring equipment must be flat down to 0.1 Hz. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.



TL/H/9212–8

FIGURE 6. 0.1 Hz to 10 Hz Noise Test Circuit

National Semiconductor

LM675 Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

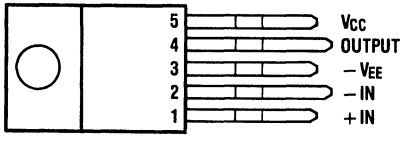
- 3A current capability
- A_{VO} typicaly 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/μs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)



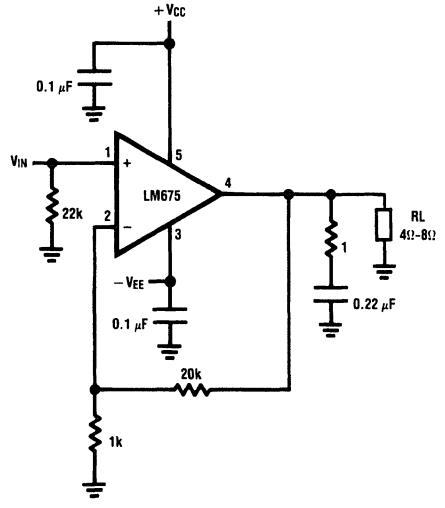
TL/H/6739–1

Front View

Order Number LM675T
See NS Package T05B

Typical Applications

Non-Inverting Amplifier



TL/H/6739–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±30V
Input Voltage	$-V_{EE}$ to V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Note 1)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating to be determined.

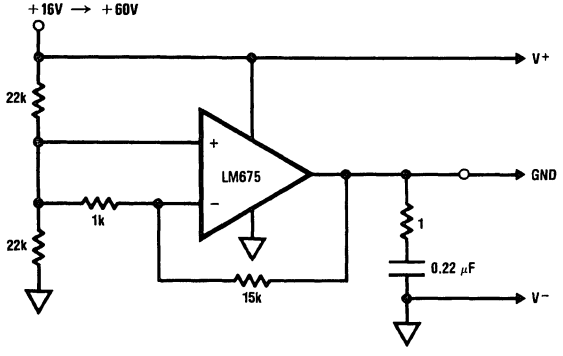
Electrical Characteristics $V_S = \pm 25V$, $T_A = 25°C$ unless otherwise specified.

Parameter	Conditions	Typical	Tested Limit	Units
Supply Current	$P_{OUT} = 0W$	18	50 (max)	mA
Input Offset Voltage	$V_{CM} = 0V$	1	10 (max)	mV
Input Bias Current	$V_{CM} = 0V$	0.2	2 (max)	μA
Input Offset Current	$V_{CM} = 0V$	50	500 (max)	nA
Open Loop Gain	$R_L = \infty\Omega$	90	70 (min)	dB
PSRR	$\Delta V_S = \pm 5V$	90	70 (min)	dB
CMRR	$V_{IN} = \pm 20V$	90	70 (min)	dB
Output Voltage Swing	$R_L = 8\Omega$	±21	±18 (min)	V
Offset Voltage Drift Versus Temperature	$R_S < 100\ k\Omega$	25		μV/°C
Offset Voltage Drift Versus Output Power		25		μV/W
Output Power	THD = 1%, $f_O = 1$ kHz, $R_L = 8\Omega$	25	20	W
Gain Bandwidth Product	$f_O = 20$ kHz, $A_{VCL} = 1000$	5.5		MHz
Max Slew Rate		8		V/μs
Input Common Mode Range		±22	±20 (min)	V

Note 1: Assumes T_A equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

Typical Applications (Continued)

Generating a Split Supply From a Single Supply

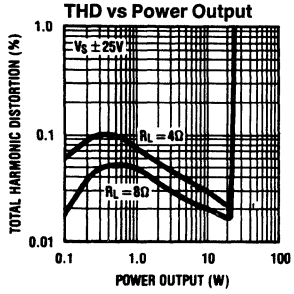


$V_S = \pm 8V \rightarrow \pm 30V$

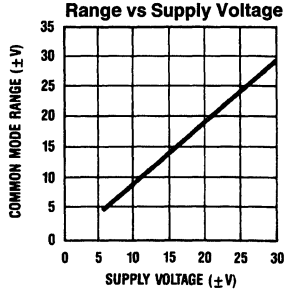
TL/H/6739–3

Typical Performance Characteristics

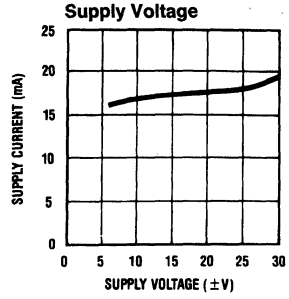
THD vs Power Output



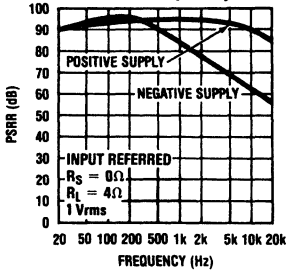
Input Common Mode Range vs Supply Voltage



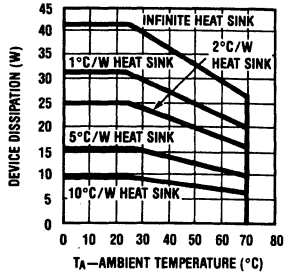
Supply Current vs Supply Voltage



PSRR vs Frequency

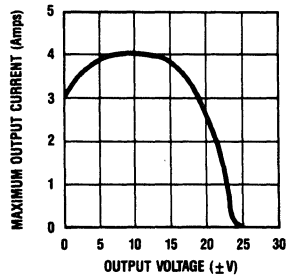


Device Dissipation vs Ambient Temperature†



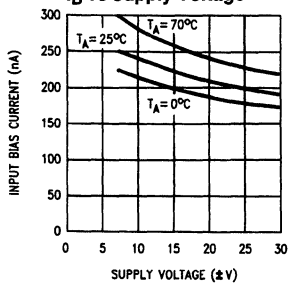
†θ INTERFACE = 1° C/W.
See Application Hints.

Current Limit vs Output Voltage*

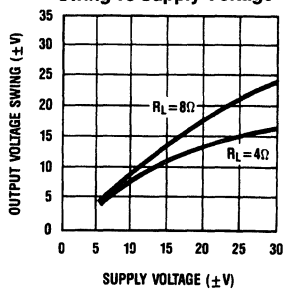


*V_S = ±25V

I_B vs Supply Voltage

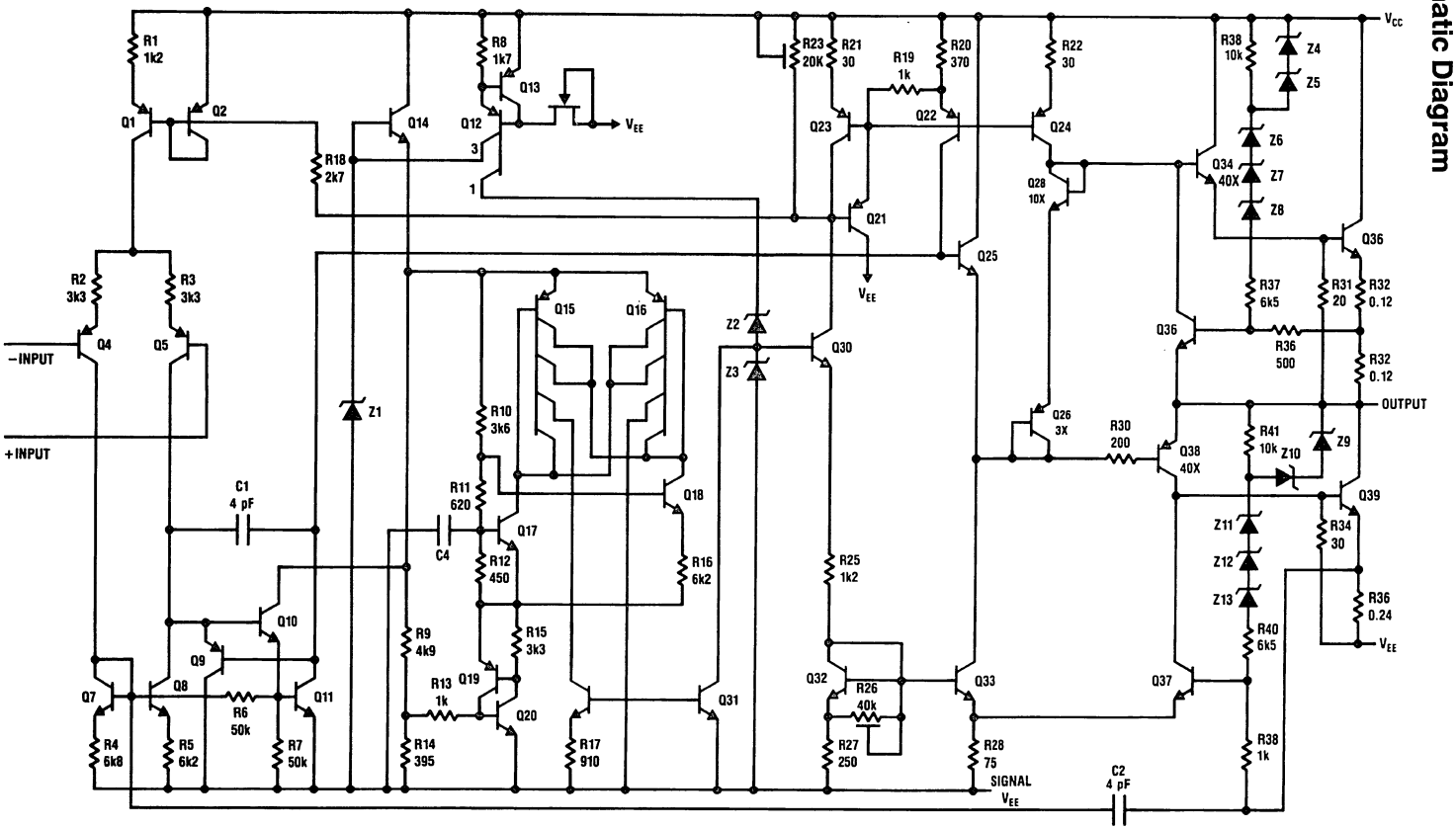


Output Voltage Swing vs Supply Voltage



TL/H/6739–4

Schematic Diagram



TL/H/6739–5

Application Hints

STABILITY

The LM675 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM675 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a printed circuit board layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM675 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM675 is no exception. If the output of the LM675 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM675. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic operational power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM675 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM675, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM675 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM675 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. This circuitry is 100% tested without a heat sink.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operaton. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor.

POWER DISSIPATION AND HEAT SINKING

The LM675 should always be operated with a heat sink, even though at idle worst case power dissipation will be only 1.8W (30 mA $\times$ 60V) which corresponds to a rise in die temperature of 97°C above ambient assuming θ_{jA} = 54°C/W for a TO-220 package. This in itself will not cause the thermal protection circuitry to shut down the amplifier when operating at room temperature, but a mere 0.9W of additional power dissipation will shut the amplifier down since T_J will then increase from 122°C (97°C + 25°C) to 170°C.

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM675 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D\,(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM675, R_L is the load resistance and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. As an example, if the LM675 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using θ_{JC} = 2°C/W, the sum of the case-to-heat sink interface thermal resistance and the heat-sink-to-ambient

Application Hints (Continued)

thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

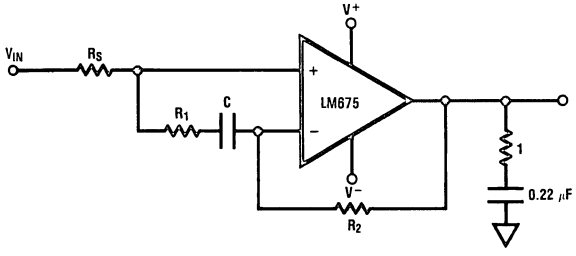
$$4.2°C/W - 2°C/W - 1.6°C/W = 0.6°C/W.$$

This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be restricted to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load will be roughly that of the same amplifier driving the resistive part of that load. For example, some reactive loads may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 8Ω × cos 60° or 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Typical Applications (Continued)

Non-Inverting Unity Gain Operation



TL/H/6739–6

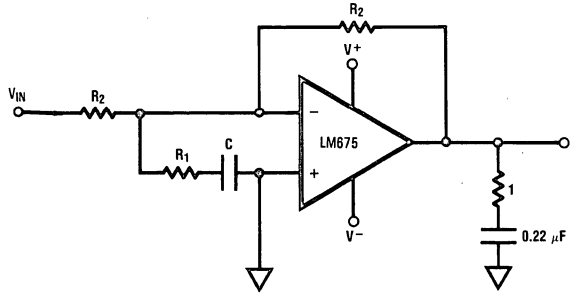
$$R_1C \geq \frac{1}{2\pi 500\ kHz}$$

$$R_1 \leq \frac{R_S + R_2}{10}$$

$A_{V(DC)} = 1$

UNITY GAIN BANDWIDTH ≅ 50 kHz

Inverting Unity Gain Operation



TL/H/6739–7

$$R_1C \geq \frac{1}{2\pi 500\ kHz}$$

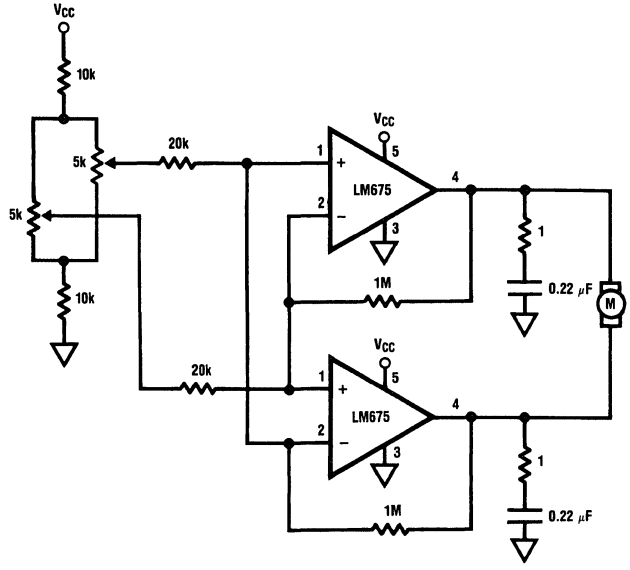
$$R_1 \leq \frac{R_2}{10}$$

$A_{V(DC)} = -1$

UNITY GAIN BANDWIDTH ≅ 50 kHz

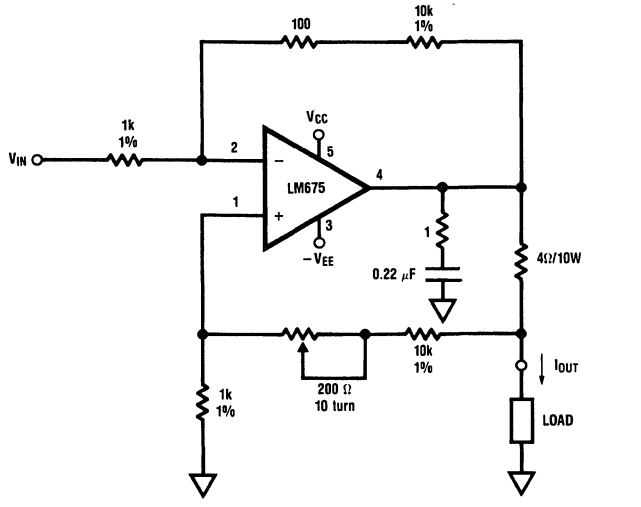
Typical Applications (Continued)

Servo Motor Control



TL/H/6739–8

High Current Source/Sink



TL/H/6739–9

$I_{OUT} = V_{IN} \times 2.5$ amps/volt
i.e. $I_{OUT} = 1A$ when $V_{IN} = 400$ mV
Trim pot for max R_{OUT}

National Semiconductor

LM725/LM725A/LM725C Operational Amplifier

General Description

The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

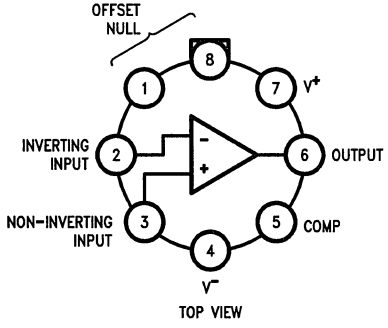
The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a −55°C to +125°C temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

Features

■ High open loop gain	3,000,000
■ Low input voltage drift	0.6 μV/°C
■ High common mode rejection	120 dB
■ Low input noise current	0.15 pA/√Hz
■ Low input offset current	2 nA
■ High input voltage range	±14V
■ Wide power supply range	±3V to ±22V
■ Offset null capability	
■ Output short circuit protection	

Connection Diagrams and Ordering Information

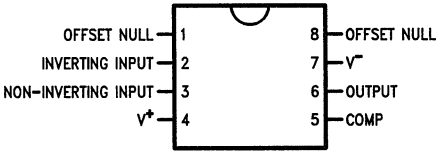
Metal Can Package



TL/H/10474–1

Order Number LM725H, LM725AH or LM725CH
See NS Package Number H08C

Dual-In-Line Package



TL/H/10474–2

Order Number LM725CN
See NS Package Number N08E

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	260°C
Maximum Junction Temperature	150°C

Operating Temperature Range	$T_{A(MIN)}$		$T_{A(MAX)}$
LM725	−55°C	to	+125°C
LM725A	−55°C	to	+125°C
LM725C	0°C	to	+70°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Without External Trim)	T_A = 25°C, $R_S \leq 10\ k\Omega$			0.5		0.5	1.0		0.5	2.5	mV
Input Offset Current	T_A = 25°C		2.0	5.0		2.0	20		2.0	35	nA
Input Bias Current	T_A = 25°C		42	80		42	100		42	125	nA
Input Noise Voltage	T_A = 25°C f_o = 10 Hz f_o = 100 Hz f_o = 1 kHz		 15 9.0 8.0			 15 9.0 8.0			 15 9.0 8.0		 nV/√Hz nV/√Hz nV/√Hz
Input Noise Current	T_A = 25°C f_o = 10 Hz f_o = 100 Hz f_o = 1 kHz		 1.0 0.3 0.15			 1.0 0.3 0.15			 1.0 0.3 0.15		 pA/√Hz pA/√Hz pA/√Hz
Input Resistance	T_A = 25°C		1.5			1.5			1.5		MΩ
Input Voltage Range	T_A = 25°C	±13.5	±14		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	T_A = 25°C, $R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	1000	3000		1000	3000		250	3000		V/mV
Common-Mode Rejection Ratio	T_A = 25°C, $R_S \leq 10\ k\Omega$	120			110	120		94	120		dB
Power Supply Rejection Ratio	T_A = 25°C, $R_S \leq 10\ k\Omega$		2.0	5.0		2.0	10		2.0	35	μV/V
Output Voltage Swing	T_A = 25°C, $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	 ±12.5 ±12.0	 ±13.5 ±13.5		 ±12 ±10	 ±13.5 ±13.5		 ±12 ±10	 ±13.5 ±13.5		 V V
Power Consumption	T_A = 25°C		80	105		80	105		80	150	mW
Input Offset Voltage (Without External Trim)	$R_S \leq 10\ k\Omega$			0.7			1.5			3.5	mV
Average Input Offset Voltage Drift (Without External Trim)	R_S = 50Ω			2.0		2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (With External Trim)	R_S = 50Ω		0.6	1.0		0.6			0.6		μV/°C
Input Offset Current	$T_A = T_{MAX}$ $T_A = T_{MIN}$		1.2 7.5	4.0 18.0		1.2 7.5	20 40		1.2 4.0	35 50	nA nA
Average Input Offset Current Drift			35	90		35	150		10		pA/°C
Input Bias Current	$T_A = T_{MAX}$ $T_A = T_{MIN}$		20 80	70 180		20 80	100 200			125 250	nA nA

Electrical Characteristics (Note 3) (Continued)

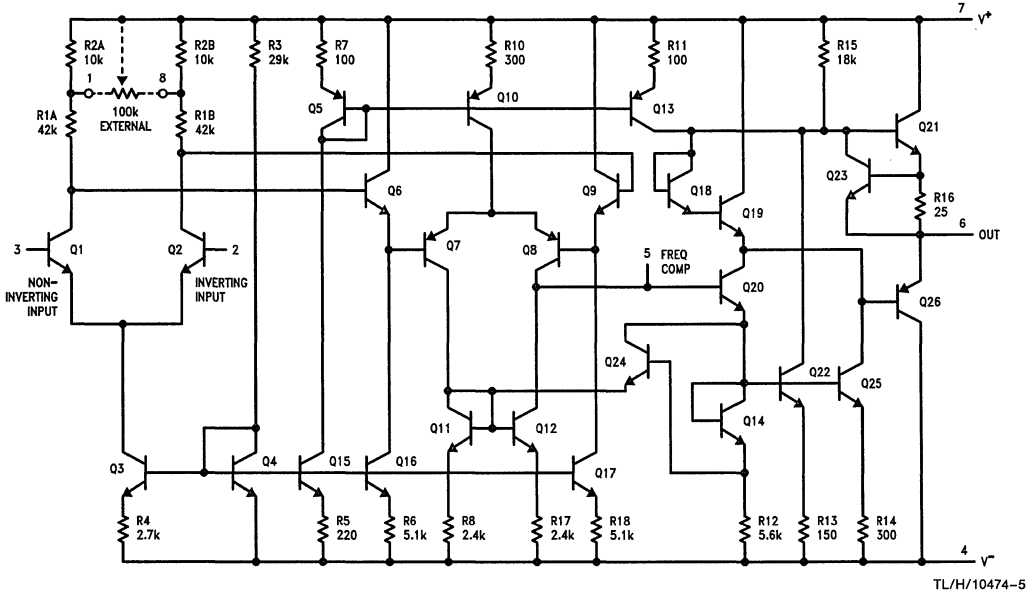
Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $T_A = T_{MAX}$ $R_L \geq 2\ k\Omega$ $T_A = T_{MIN}$	1,000,000 500,000			1,000,000 250,000			125,000 125,000			V/V V/V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110			100				115		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			8.0			20		20		μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12			±10			±10			V

Note 1: Derate at 150°C/W for operation at ambient temperatures above 75°C.

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for V_S = ±15V unless otherwise specified.

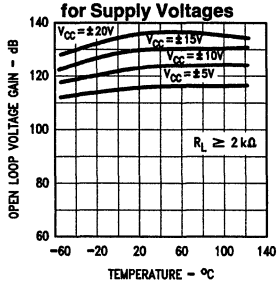
Schematic Diagram



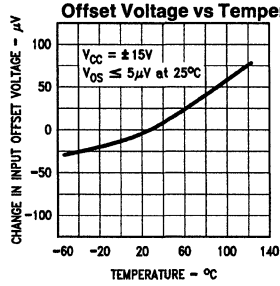
TL/H/10474–5

Typical Performance Characteristics

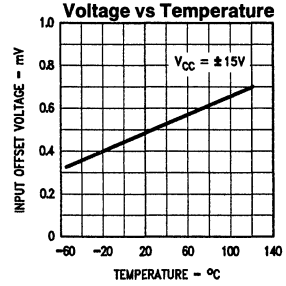
Voltage Gain vs Temperature for Supply Voltages



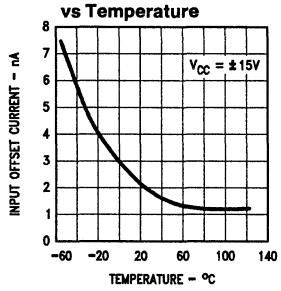
Change in Trimmed Input Offset Voltage vs Temperature



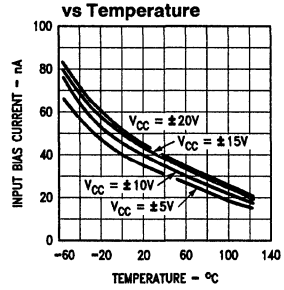
Untrimmed Input Offset Voltage vs Temperature



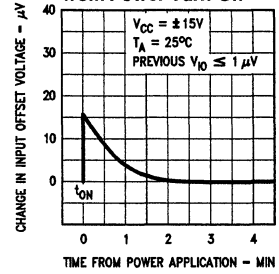
Input Offset Current vs Temperature



Input Bias Current vs Temperature



Stabilization Time of Input Offset Voltage from Power Turn-On



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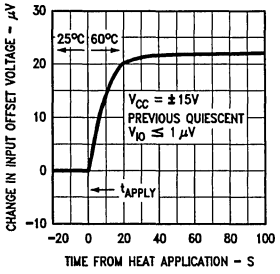
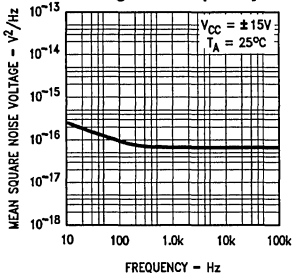
Typical Performance Characteristics (Continued)

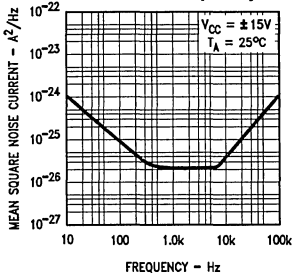
Change in Input Offset Voltage Due to Thermal Shock vs Time



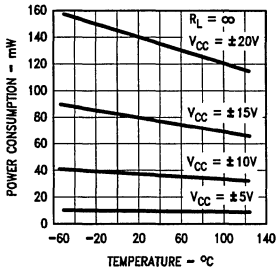
Input Noise Voltage vs Frequency



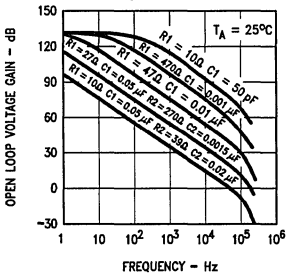
Input Noise Current vs Frequency



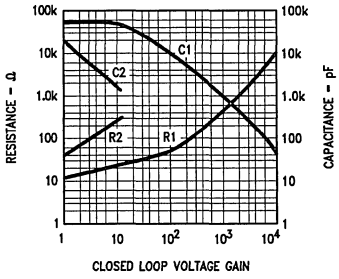
Power Consumption vs Temperature



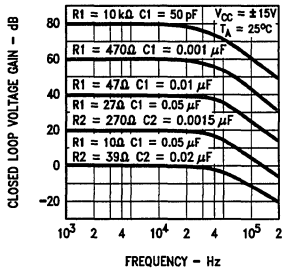
Open Loop Frequency Response for Values of Compensation (Note 1)



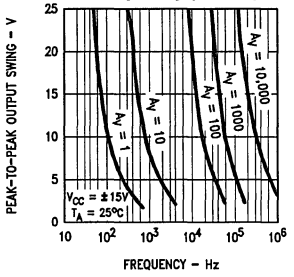
Values for Suggested Compensation Networks vs Various Close Loop Voltage Gains



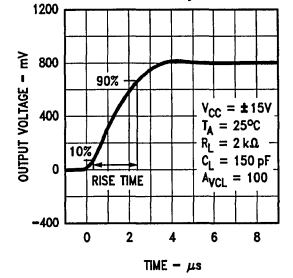
Frequency Response for Various Close Loop Gain (Note 1)



Output Voltage Swing vs Frequency (Note 1)



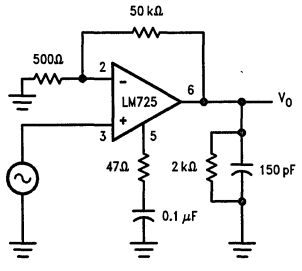
Transient Response



TL/H/10474–7

Note 1: Performance is shown using recommended compensation networks.

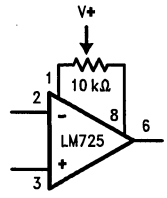
Transient Response Test Circuit



TL/H/10474–8

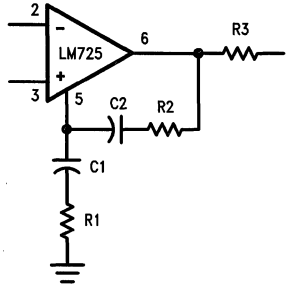
Auxiliary Circuits

Voltage Offset Null Circuit



TL/H/10474–3

Frequency Compensation Circuit



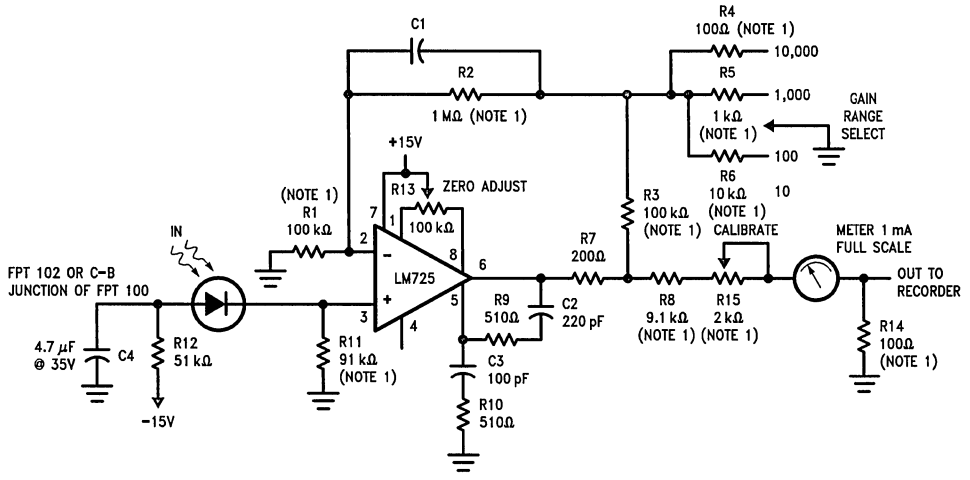
TL/H/10474–4

Compensation Component Values

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10k	50 pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

Typical Applications

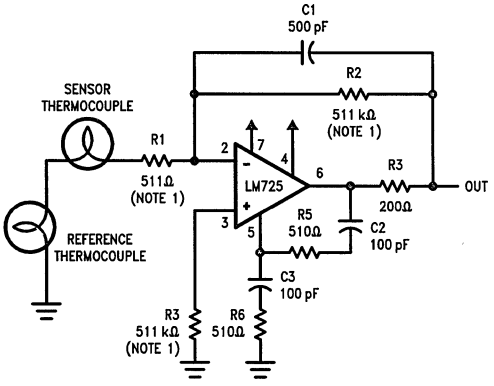
Photodiode Amplifier



TL/H/10474–9

DC Gains = 10,000; 1,000; 100; and 10
Bandwidth = Determined by value of C1

Thermocouple Amplifier



TL/H/10474–10

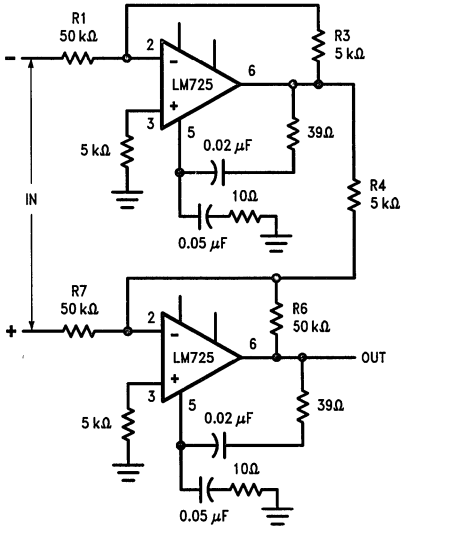
$\frac{R2}{R5} = \frac{R6}{R7}$ for best CMR

R1 = R4
R2 = R5

$\text{Gain} = \frac{R6}{R2} + \left(\frac{2R1}{R3}\right)$

DC Gain = 1000
Bandwidth = DC to 540 Hz
Equivalent Input Noise = 0.24 μV_{rms}

±100V Common Mode Range Differential Amplifier

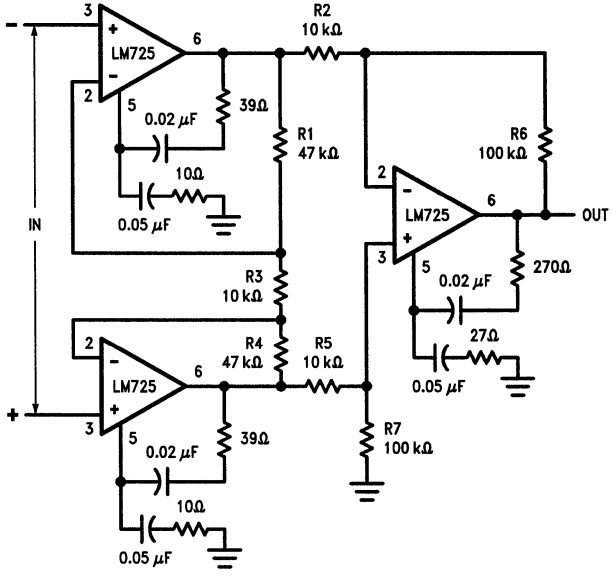


TL/H/10474–11

Note 1: Indicates ±1% metal film resistors recommended for temperature stability.

Typical Applications (Continued)

Instrumentation Amplifier with High Common Mode Rejection



TL/H/10474–12

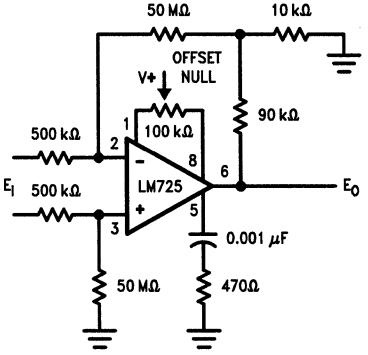
$\frac{R1}{R6} = \frac{R3}{R4}$ for best CMRR

R3 = R4

R1 = R6 = 10 R3

Gain = $\frac{R6}{R7}$

Precision Amplifier A_{VCL} = 1000



TL/H/10474–13

National Semiconductor

LM741/LM741A/LM741C/LM741E Operational Amplifier

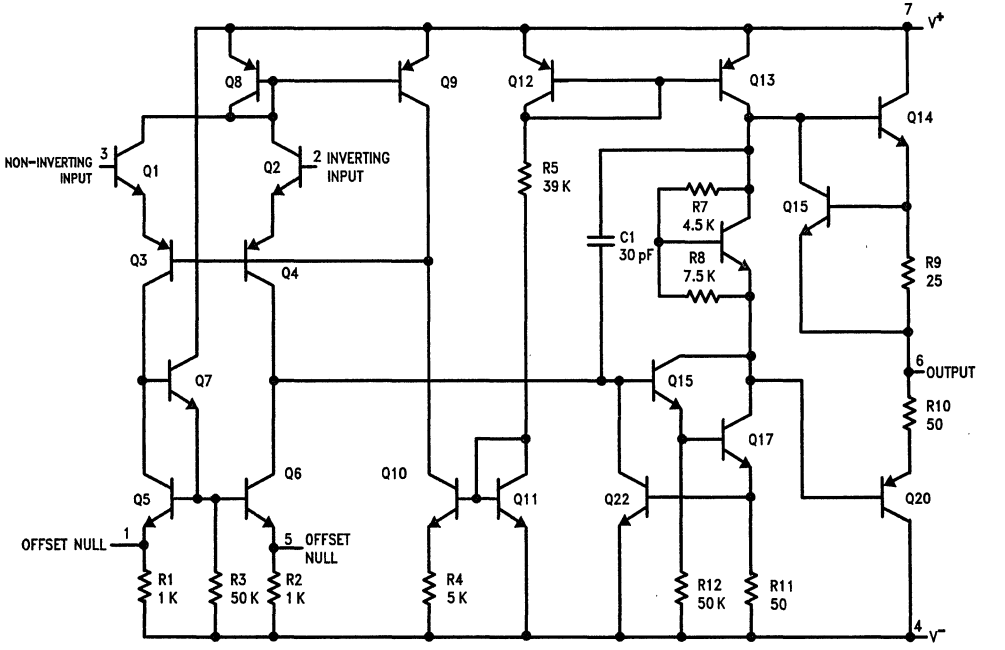
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

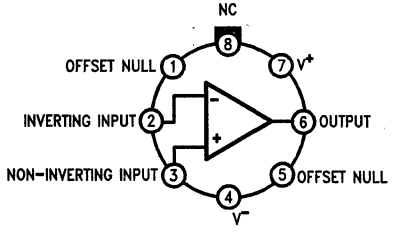
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)



TL/H/9341–1

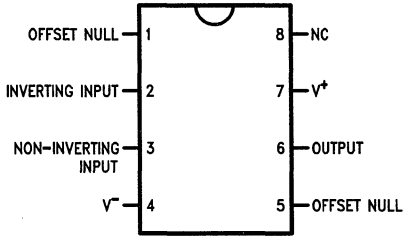
Metal Can Package



TL/H/9341–2

Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package Number H08C

Dual-In-Line or S.O. Package



TL/H/9341–3

Order Number LM741J, LM741AJ, LM741CJ, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		 0.8	 3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			 6.0			 7.5	mV mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$	50			 50	 200		 20	 200		 V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$ $V_S = \pm 5V, V_O = \pm 2V$	 32 10			 25			 15			 V/mV V/mV V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	± 16									V
	$R_L \geq 2\ k\Omega$	± 15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				± 12	± 14		± 12	± 14		V
	$R_L \geq 2\ k\Omega$				± 10	± 13		± 10	± 13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		$V/\mu s$
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM759/LM77000
Power Operational Amplifiers

General Description

The LM759 and LM77000 are high performance operational amplifiers that feature high output current capability. The LM759 is capable of providing 325 mA and the LM77000 providing 250 mA. Both amplifiers feature small signal characteristics that are better than the LM741. The amplifiers are designed to operate from a single or dual power supply with an input common mode range that includes the negative supply. The high gain and high output power provide superior performance. Internal current limiting, thermal shutdown, and safe area compensation are employed making the LM759 and LM77000 essentially indestructible.

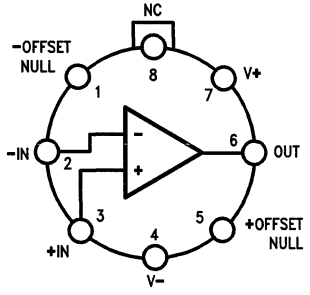
Features

- Output current
  - LM759—325 mA minimum
  - LM77000—250 mA minimum
- Internal short circuit current limiting
- Internal thermal overload protection
- Internal output transistors safe-area protection
- Input common mode voltage range includes ground or negative supply

Applications

- Voltage regulators
- Audio amplifiers
- Servo amplifiers
- Power drivers

Connection Diagrams and Ordering Information

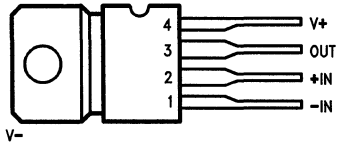


TL/H/10075–1

Lead 4 connected to case.

Top View

Order Number LM759MH or LM759CH
See NS Package Number H08C



TL/H/10075–2

Top View

Order Number LM759CP or LM77000CP
See NS Package Number P04A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Metal Can: −65°C to +175°C
- Plastic Package: −65°C to +150°C

Operating Junction Temperature Range
- Military (LM759M): −55°C to +150°C
- Commercial (LM759C, LM77000C): 0°C to +125°C

Lead Temperature
- Metal Can (soldering, 60 sec): 300°C
- Plastic Package (soldering, 10 sec): 265°C

Internal Power Dissipation (Note 1): Internally Limited
Supply Voltage: ±18V
Differential Input Voltage: 30V
Input Voltage (note 2): ±15V

LM759
Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	3.0	mV
I_{IO}	Input Offset Current				5.0	30	nA
I_{IB}	Input Bias Current				50	150	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC}-V_O \rvert \leq 10V$	±325	±500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	50	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			5.0		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.6		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq +150°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			4.5	mV
I_{IO}	Input Offset Current					60	nA
I_{IB}	Input Bias Current					300	nA
CMRR	Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

LM759C

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC} - V_O \rvert = 30V$		± 200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC} - V_O \rvert \leq 10V$	± 325	± 500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMRR	Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	± 10	± 12.5		V

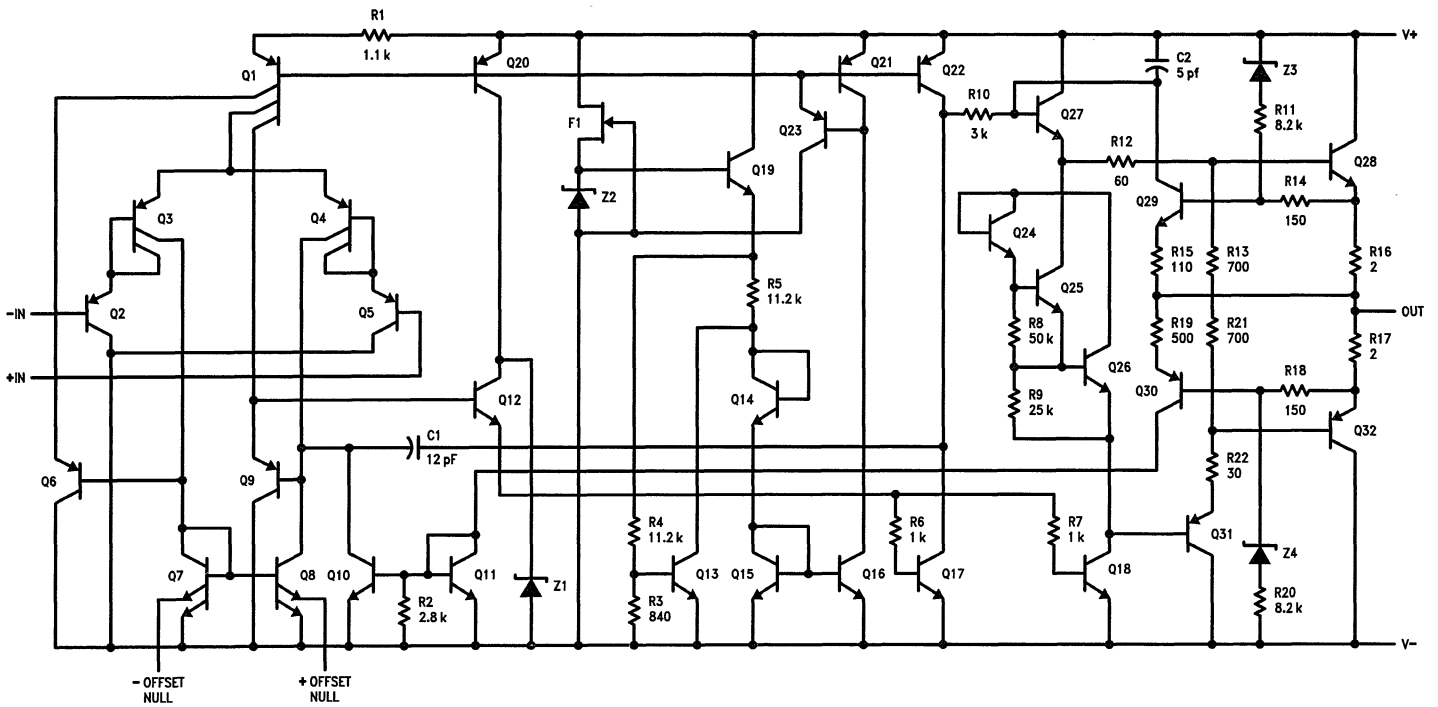
LM77000
Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	8.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			+13 to V^-	+13 to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC}-V_O \rvert \leq 10V$	±250	±400		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			10	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

Note 1: Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the Equivalent Circuit Schematic.

Note 2: For a supply voltage less than 30V between V^+ and V^-, the absolute maximum input voltage is equal to the supply voltage.

Equivalent Circuit



TL/H/10075–3

Note: All resistor values in ohms.

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
Plastic Package (P)	8.0	12	75	80
Metal Can (H)	30	40	120	150

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D\theta_{JA} \text{ (without a heat sink)}$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance

Mounting Hints

Metal Can Package (LM759CH/LM759MH)

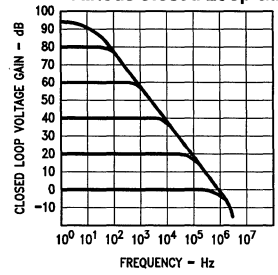
The LM759 in the 8-Lead TO-99 metal can package must be used with a heat sink. With ±15V power supplies, the LM759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the LM759 is internally connected to the negative power supply terminal.

Plastic Package (LM759CP/LM77000CP)

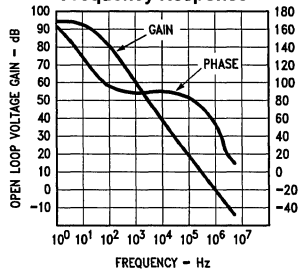
The LM759CP and LM77000CP are designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

Typical Performance Characteristics

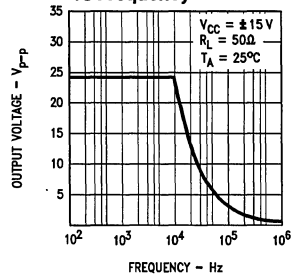
Frequency Response for Various Closed Loop Gains



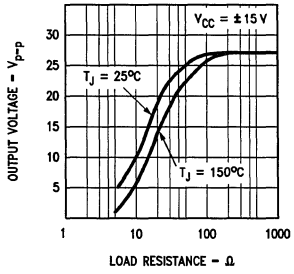
Open Loop vs Frequency Response



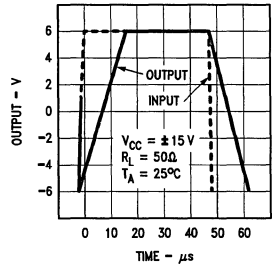
Output Voltage vs Frequency



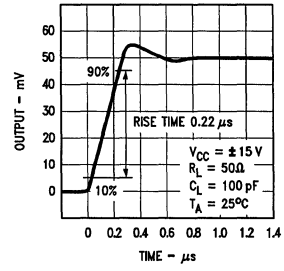
Output Voltage vs Load Resistance



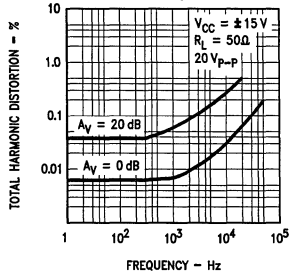
Voltage Follower Large Signal Pulse Response



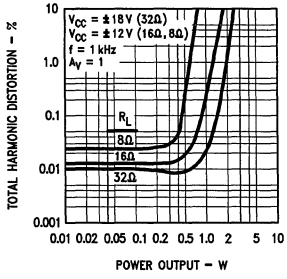
Voltage Follower Transient Response



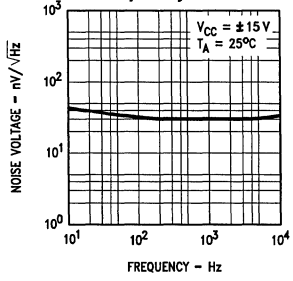
Total Harmonic Distortion vs Frequency



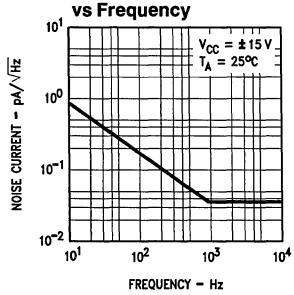
Total Harmonic Distortion vs Power Output



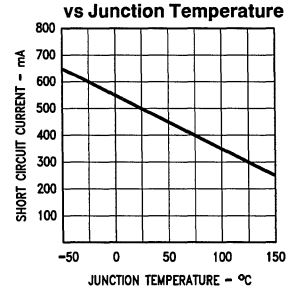
Input Noise Voltage vs Frequency



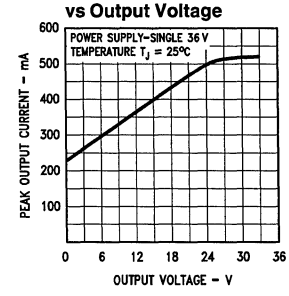
Noise Current vs Frequency



Short Circuit Current vs Junction Temperature



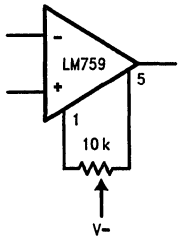
Peak Output Current vs Output Voltage



TL/H/10075–4

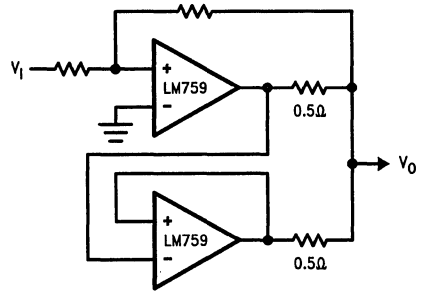
Applications

Offset Null Circuit



TL/H/10075–5

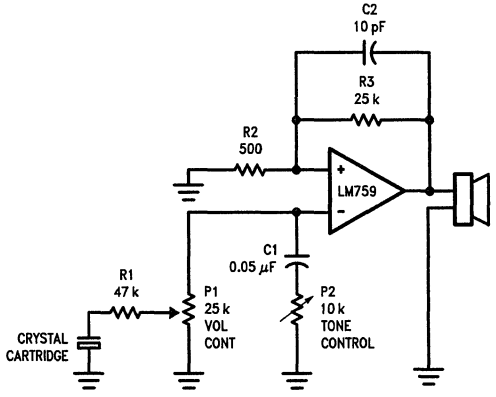
Paralleling LM759 Power Op Amps



TL/H/10075–6

Audio Applications

Low Cost Phono Amplifier

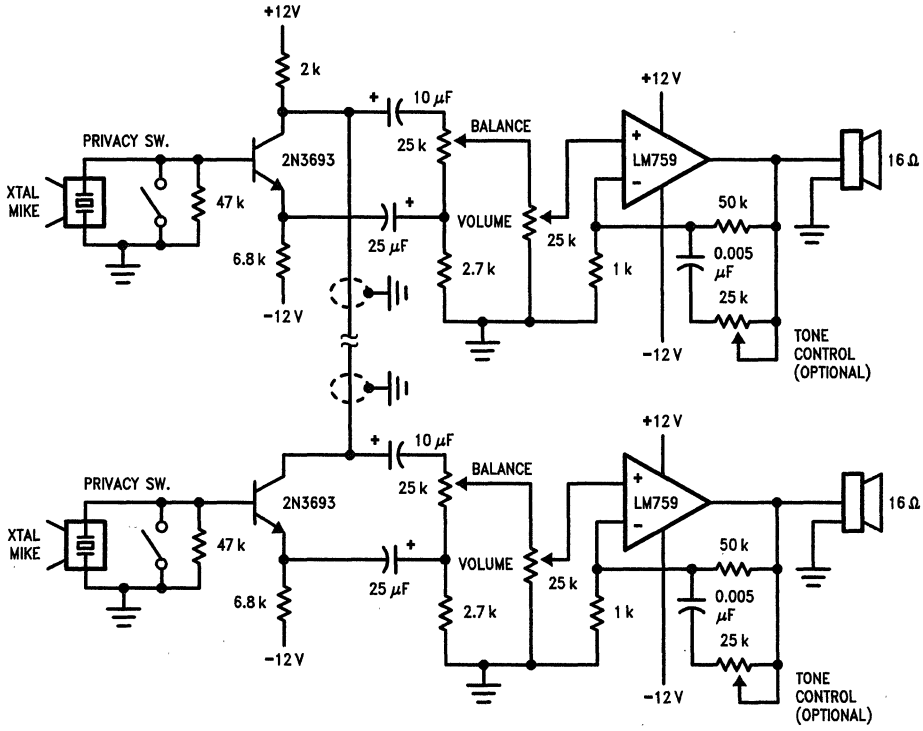


TL/H/10075–7

Speaker Impedance (Ohms)	Output Power (Watts)	Min Supply (Volts)	V_{OP-P} (Volts)
4	0.18	9	2.4
8	0.36	12	4.8
16	0.72	15	9.6
32	1.44	25	19.2

Applications (Continued)

Bi-Directional Intercom System Using the LM759 Power Op Amp



TL/H/10075–9

Features:

Circuit Simplicity

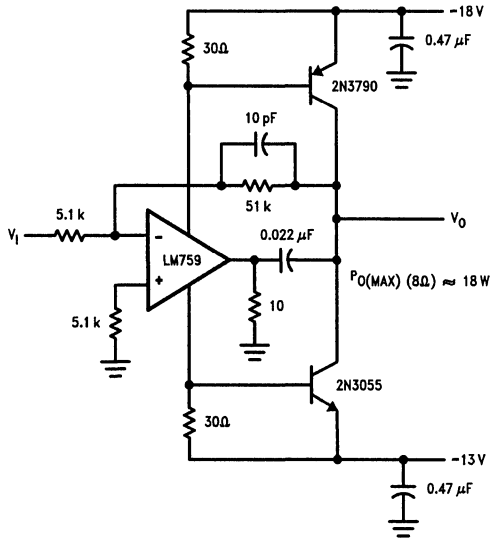
1 Watt of Audio Output

Duplex operation with only one two-wire cable as interconnect.

Note 1: All resistor values in ohms.

Applications (Continued)

High Slew Rate Power Op Amp/Audio Amp



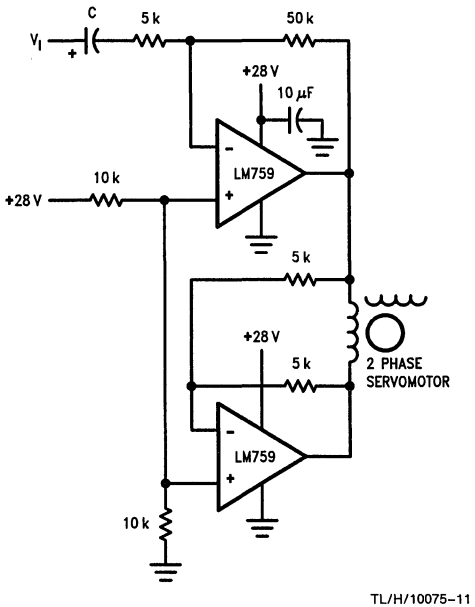
TL/H/10075–10

Features:

High Slew Rate 9 V/μs
High 3 dB Power Bandwidth 85 kHz
18 Watts Output Power into an 8Ω load.
Low Distortion—0.2%, 10 Vrms, 1 kHz into 8Ω
Design Consideration
$A_V \geq 10$

Servo Applications

AG Servo Amplifier—Bridge Type



TL/H/10075–11

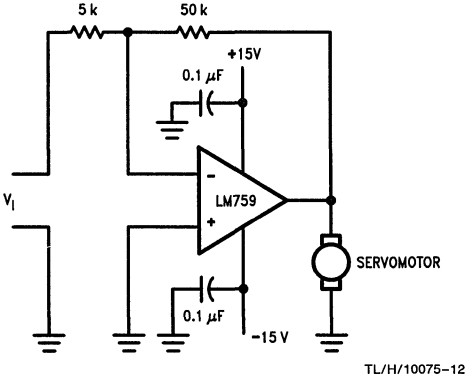
Features:

Gain of 10
Use of LM759 Means Simple Inexpensive Circuit

Design Considerations:

325 mA Max Output Current

DC Servo Amplifier



TL/H/10075–12

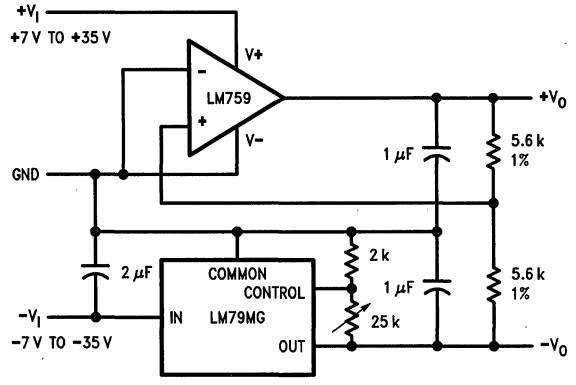
Features:

Circuit Simplicity
One Chip Means Excellent Reliability
Design Considerations
$I_O \leq 325$ mA

Note 1: All resistor values in ohms.

Regulator Applications

Adjustable Dual Tracking Regulator



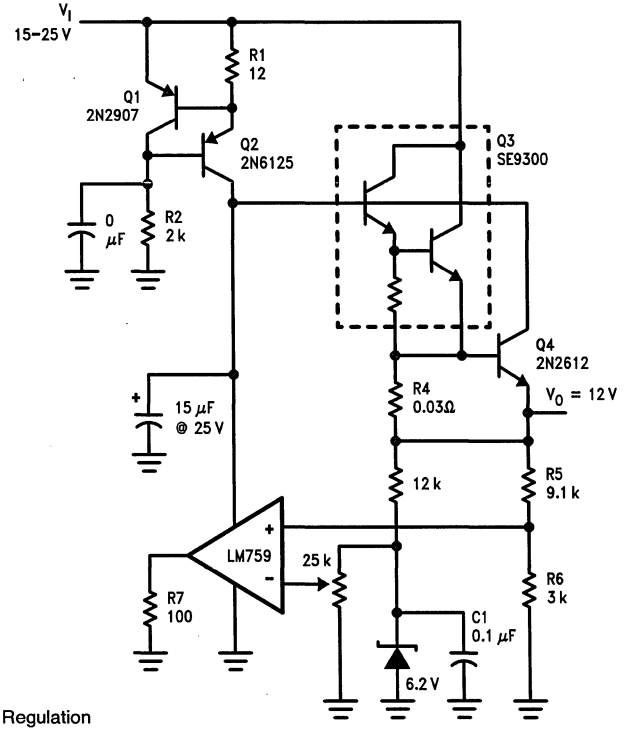
TL/H/10075–13

Features:

Wide Output Voltage Range (±2.2V to ±30V)
Excellent Load Regulation ΔV_O < ±5 mV for ΔI_O = ±0.2 A
Excellent Line Regulation ΔV_O < ±2 mV for ΔV_I = 10V

Note 1: All resistor values in ohms.

10 Amp — 12 Volt Regulator



TL/H/10075–14

Features:

Excellent Load and Line Regulation
Excellent Temperature Coefficient-Depends
Largely on Tempco of the Reference Zener

Note 1: All resistor values in ohms.

National Semiconductor

LM776
Multi-Purpose Programmable Operational Amplifier

General Description

The LM776 Programmable Operational Amplifier is constructed using the Planar Epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano watt power consumption or for characteristics similar to the LM741. Internal frequency compensation, absence of latch up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

Features

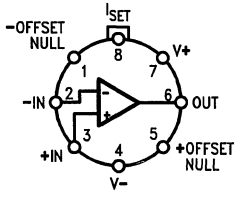
- Micropower consumption
- ±1.2V to ±18V operation
- No frequency compensation required
- Low input bias currents
- Wide programming range
- High slew rate
- Low noise
- Short circuit protection
- Offset null capability
- No latch up

Applications

- Battery-powered instrumentation
- High-gain amp
- Filters
- Sample-and-Hold

Connection Diagrams

8-Lead Metal Package



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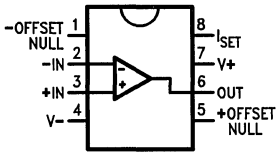
Top View

Lead 4 connected to case.

8-Lead DIP



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Top View

Ordering Information

Device Code	Package Code	Package Description
LM776H	H08A	Metal
LM776CH	H08A	Metal
LM776CN	N08E	Molded DIP

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Metal Can	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (LM776M)	−55°C to +125°C
Commercial (LM776C)	0°C to +70°C
Lead Temperature	
Metal Can (Soldering, 60 sec.)	300°C
Molded DIP (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1, 2)	
8L-Metal Can	1.00W
8L-Molded DIP	0.93W
Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Voltage Between Offset Null and V^-	±0.5V
Output Short Circuit Duration (Note 4)	Indefinite
I_{SET} (Maximum Current at I_{SET})	500 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V^+ - 2.0V) \leq V_{SET} \leq V^+$
ESD Tolerance	(to be determined)

LM776
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	5.0		2.0	5.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	3.0		2.0	15	nA
I_{IB}	Input Bias Current				2.0	7.5		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				20	25		160	180	μA
P_C	Power Consumption					0.75			5.4	mW
I_{OS}	Output Short Circuit Current				3.0			12		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10V$, $R_L \geq 75\ k\Omega$	200	400					V/mV
			$V_O = \pm 10V$, $R_L \geq 5.0\ k\Omega$				100	400		
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±12	±14					V
			$R_L = 5.0\ k\Omega$				±10	±13		
TR	Transient Response	Rise Time	$V_I = 20\ mV$, $R_L = 5.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		1.6			0.35		μs
		Overshoot			0			10		%
SR	Slew Rate		$R_L = 5.0\ k\Omega$, $A_V = 1.0$		0.1			0.8		V/μs
The following specifications apply $-55°C \leq T_A \leq +125°C$										
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			6.0			6.0	mV
I_{IO}	Input Offset Current		$T_A = +125°C$			5.0			15	nA
			$T_A = -55°C$			10			40	
I_{IB}	Input Bias Current		$T_A = +125°C$			7.5			50	nA
			$T_A = -55°C$			20			120	
I_{CC}	Supply Current					30			200	μA
P_C	Power Consumption					0.9			6.0	mW
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	90		70	90		dB
V_{IR}	Input Voltage Range			±10			±10			V
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$		25	150		25	150	μV/V
A_{VS}	Large Signal Voltage Gain		$V_O = +10V$, $R_L \geq 75\ k\Omega$	100			75			V/mV
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±10			±10			V

LM776
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 3.0V$, unless otherwise specified

Symbol	Parameter		Conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	5.0		2.0	5.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	3.0		2.0	15	nA
I_{IB}	Input Bias Current				2.0	7.5		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				13	20		130	160	μA
P_C	Power Consumption				78	120		780	960	μW
I_{OS}	Output Short Circuit Current				3.0			5.0		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 1.0V$, $R_L \geq 75\ k\Omega$	50	200					V/mV
			$V_O = \pm 1.0V$, $R_L \geq 5.0\ k\Omega$				50	200		
TR	Transient Response	Rise Time	$V_I = 20\ mV$, $R_L = 5.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		3.0			0.6		μs
		Overshoot			0			5		%
SR	Slew Rate		$R_L = 5.0\ k\Omega$, $A_V = 1.0$		0.03			0.35		V/μs
The following specifications apply $-55°C \leq T_A \leq +125°C$										
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			6.0			6.0	mV
I_{IO}	Input Offset Current		$T_A = +125°C$			5.0			15	nA
			$T_A = -55°C$			10			40	
I_{IB}	Input Bias Current		$T_A = +125°C$			7.5			50	nA
			$T_A = -55°C$			20			120	
I_{CC}	Supply Current					25			180	μA
P_C	Power Consumption					150			1080	μW
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	86		70	86		dB
V_{IR}	Input Voltage Range			±1.0			±1.0			V
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$		25	150		25	150	μV/V
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 1.0V$, $R_L \geq 75\ k\Omega$	25						V/mV
			$V_O = \pm 1.0V$, $R_L \geq 5.0\ k\Omega$				25			
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±2.0	±2.4					V
			$R_L = 5.0\ k\Omega$				±1.9	±2.1		

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP, and 175°C for the Metal Can.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Short Circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature for $I_{SET} \leq 30\ \mu A$.

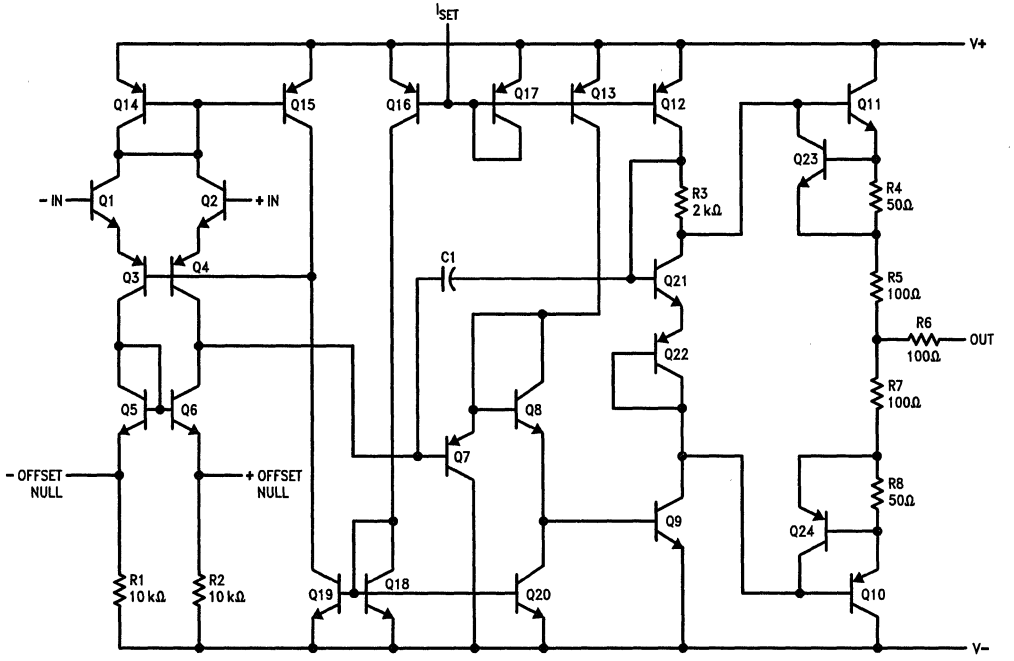
LM776C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	6.0		2.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	6.0		2.0	25	nA
I_{IB}	Input Bias Current				2.0	10		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				20	30		160	190	μA
P_c	Power Consumption					0.9			5.7	mW
I_{OS}	Output Short Circuit Current				3.0			12		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10V$, $R_L \geq 75\ k\Omega$	50	400					V/mV
			$V_O = \pm 10V$, $R_L \geq 5.0\ k\Omega$				50	400		
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±12	±14					V
			$R_L = 5.0\ k\Omega$				±10	±13		
TR	Transient Response	Rise Time	$V_I = 20\ mV$, $R_L \geq 5.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		1.6			0.35		μs
		Overshoot			0			10		%
SR	Slew Rate		$R_L = 5.0\ k\Omega$, $A_V = 1.0$		0.1			0.8		V/μs
The following specifications apply $0°C \leq T_A \leq +70°C$										
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5			7.5	mV
I_{IO}	Input Offset Current		$T_A = 70°C$			6.0			25	nA
			$T_A = 0°C$			10			40	
I_{IB}	Input Bias Current		$T_A = 70°C$			10			50	nA
			$T_A = 0°C$			20			100	
I_{CC}	Supply Current					35			200	μA
P_c	Power Consumption					1.05			6.0	mW
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	90		70	90		dB
V_{IR}	Input Voltage Range			±10			±10			V
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$		25	200		25	200	μV/V
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10V$, $R_L \geq 75\ k\Omega$	50			50			V/mV
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±10			±10			V

LM776C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 3.0V$, unless otherwise specified

Symbol	Parameter		Conditions	$I_{SET} = 1.5\ \mu A$			$I_{SET} = 15\ \mu A$			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	6.0		2.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	6.0		2.0	25	nA
I_{IB}	Input Bias Current				2.0	10		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				13	20		130	170	μA
P_C	Power Consumption				78	120		780	1020	μW
I_{OS}	Output Short Circuit Current				3.0			5.0		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 1.0V$, $R_L \geq 75\ k\Omega$	25	200					V/mV
			$V_O = \pm 1.0V$, $R_L \geq 5.0\ k\Omega$				25	200		
TR	Transient Response	Rise Time	$V_I = 20\ mV$, $R_L \geq 5.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		3.0			0.6		μs
		Overshoot			0			5		%
SR	Slew Rate		$R_L = 5.0\ k\Omega$, $A_V = 1.0$		0.03			0.35		V/μs
The following specifications apply $0°C \leq T_A \leq +70°C$										
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5			7.5	mV
I_{IO}	Input Offset Current		$T_A = 70°C$			6.0			25	nA
			$T_A = 0°C$			10			40	
I_{IB}	Input Bias Current		$T_A = 70°C$			10			50	nA
			$T_A = 0°C$			20			100	
I_{CC}	Supply Current					25			180	μA
P_C	Power Consumption					150			1080	μW
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	86		70	86		dB
V_{IR}	Input Voltage Range			±1.0			±1.0			V
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$		25	200		25	200	μV/V
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 1.0V$, $R_L \geq 75\ k\Omega$	25						V/mV
			$V_O = \pm 1.0V$, $R_L \geq 5.0\ k\Omega$				25			
V_{OP}	Output Voltage Swing		$R_L = 75\ k\Omega$	±2.0	±2.4					V
			$R_L = 5.0\ k\Omega$				±2.0	±2.1		

Equivalent Circuit



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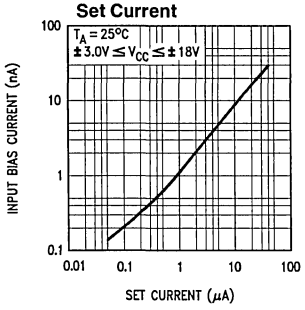
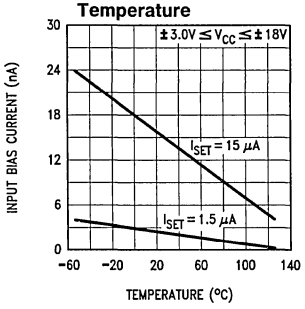
Typical Performance Characteristics for LM776 and LM776C

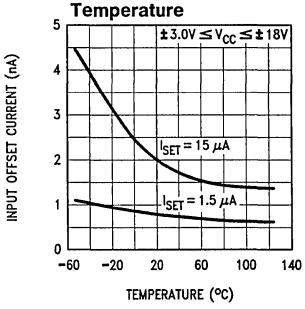
Input Bias Current vs Set Current



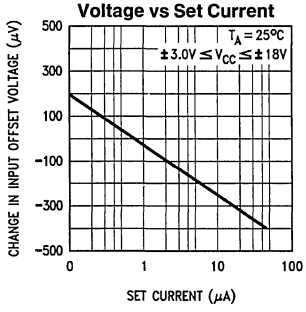
Input Bias Current vs Temperature



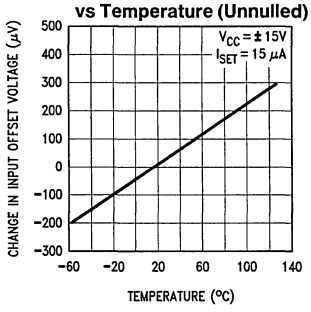
Input Offset Current vs Temperature



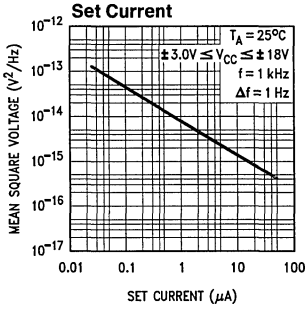
Change in Input Offset Voltage vs Set Current



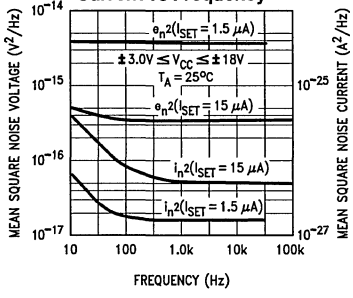
Change in Input Offset Voltage vs Temperature (Unnulled)



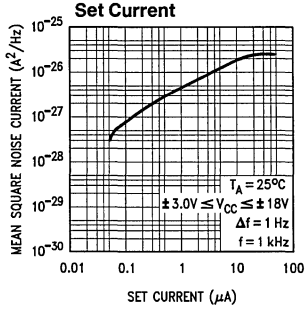
Input Noise Voltage vs Set Current



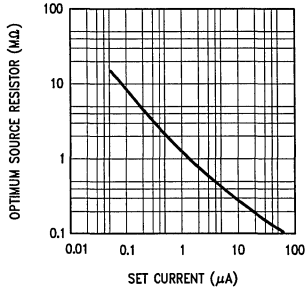
Input Noise Voltage and Current vs Frequency



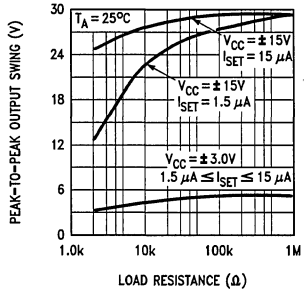
Input Noise Current vs Set Current



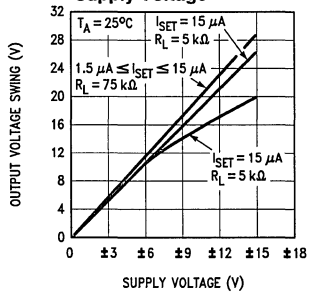
Optimum Source Resistor for Minimum Noise vs Set Current



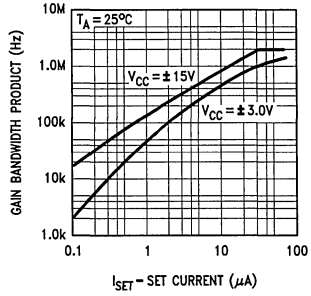
Output Voltage Swing vs Load Resistance



Output Voltage Swing vs Supply Voltage



Gain Bandwidth Product vs Set Current



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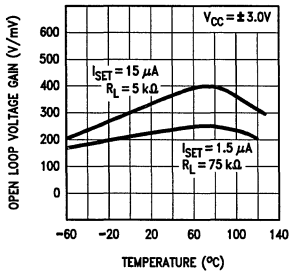
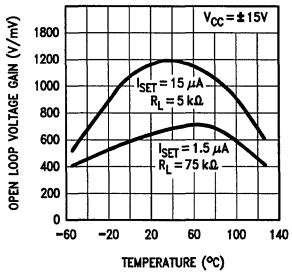
Typical Performance Characteristics for LM776 and LM776C (Continued)

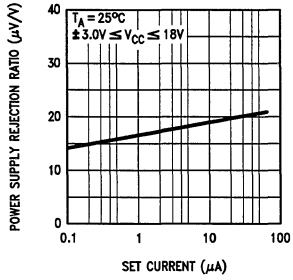
Voltage Gain vs Temperature



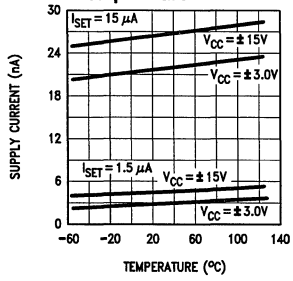
Voltage Gain vs Temperature



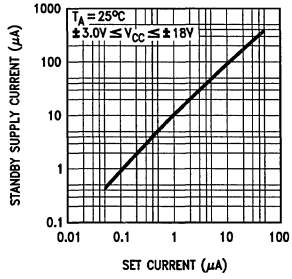
Power Supply Rejection Ratio vs Set Current



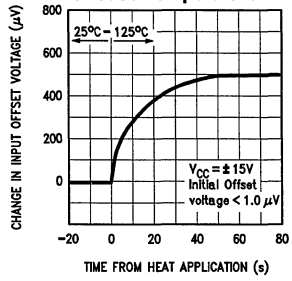
Supply Current vs Temperature



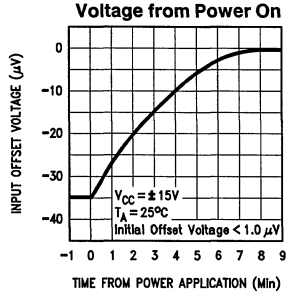
Standby Supply Current vs Set Current



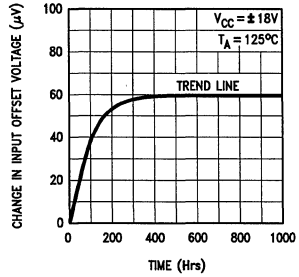
Thermal Response of Input Offset Voltage to Step Change of Case Temperature



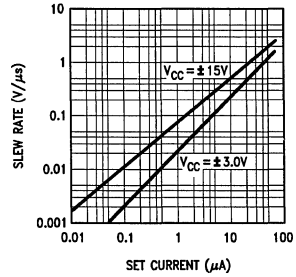
Stabilization Time of Input Offset Voltage from Power On



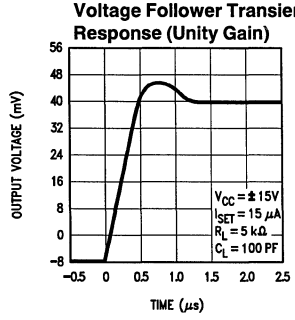
Input Offset Voltage Drift vs Time



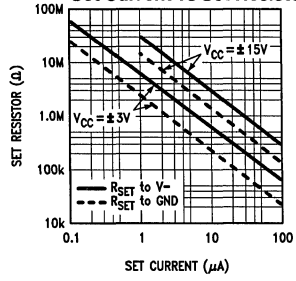
Slew Rate vs Set Current



Voltage Follower Transient Response (Unity Gain)



Set Current vs Set Resistor



TL/H/10073–5

Applications Information

Quiescent Current Setting Resistor (I_{SET} to V^-)

V_S	I_{SET}	
	1.5 μA	15 μA
±1.5V	1.7 MΩ	170 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15V	20 MΩ	2.0 MΩ

Note: The LM776 may be operated with R_{SET} connected to ground or V.

I_{SET} Equations

$$I_{SET} = \frac{(V^+) - 0.7 - (V^-)}{R_{SET}}$$

where:

R_{SET} is connected to V^-

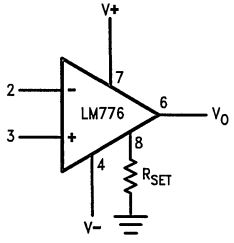
$$I_{SET} = \frac{(V^+) - 0.7}{R_{SET}}$$

where:

R_{SET} is connected to ground.

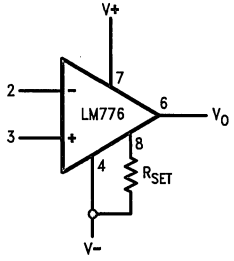
Biasing Circuits

Resistor Biasing



TL/H/10073–6

R_{SET} Connected to Ground

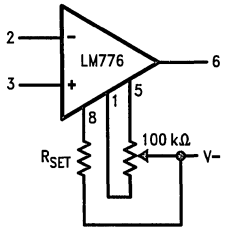


TL/H/10073–7

R_{SET} Connected to V^-

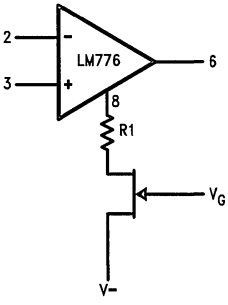
*Recommended for supply voltages less than ±6V.

Voltage Offset Null Circuit



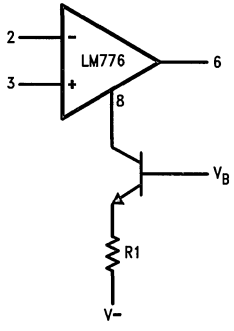
TL/H/10073–9

FET Current Source Biasing



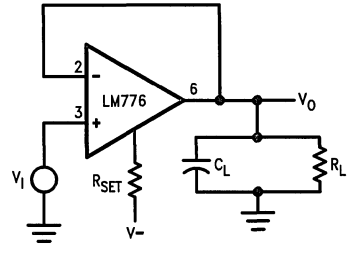
TL/H/10073–10

Transistor Current Biasing



TL/H/10073–8

Transient Response Test Circuit



TL/H/10073–11

National Semiconductor

LM833 Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

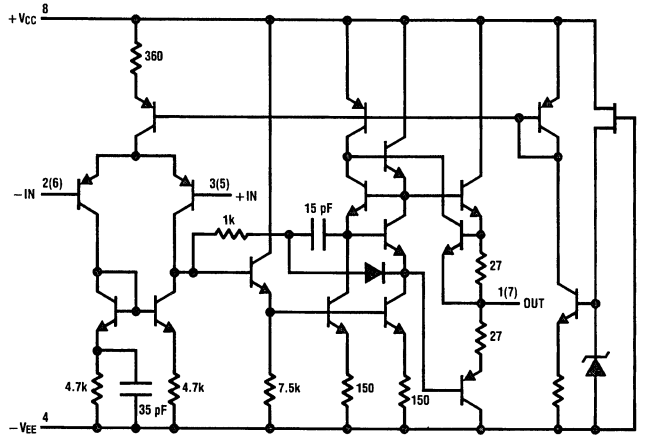
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

Features

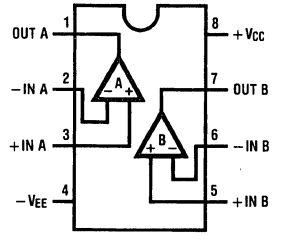
■ Wide dynamic range	>140 dB
■ Low input noise voltage	4.5 nV/√Hz
■ High slew rate	7 V/μs (typ) 5 V/μs (min)
■ High gain bandwidth product	15 MHz (typ) 10 MHz (min)
■ Wide power bandwidth	120 kHz
■ Low distortion	0.002%
■ Low offset voltage	0.3 mV
■ Large phase margin	60°

Schematic Diagram (1/2 LM833)



TL/H/5218–1

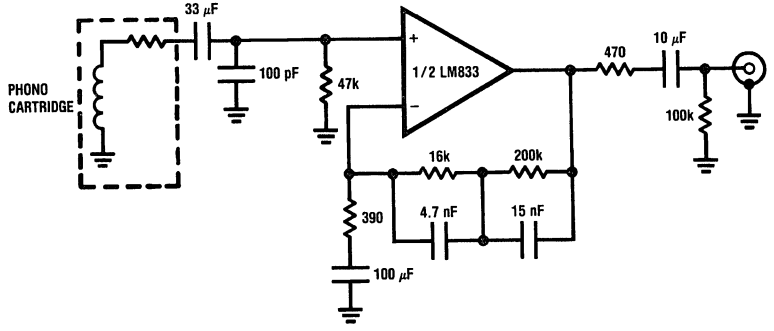
Connection Diagram



TL/H/5218–2

Order Number LM833M or LM833N
See NS Package Number
M08A or N08E

Typical Application RIAA Preamp



TL/H/5218–3

A_V = 35 dB f = 1 kHz
E_n = 0.33 μV A Weighted
S/N = 90 dB A Weighted, V_{IN} = 10 mV @ f = 1 kHz

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	$V_{CC}-V_{EE}$	36V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Input Voltage Range (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	500 mW
Operating Temperature Range	T_{OPR}	−40 ~ 85°C
Storage Temperature Range	T_{STG}	−60 ~ 150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 1600V

DC Electrical Characteristics (T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ R_L = 2 kΩ	±12 ±10	±13.5 ±13.4		V V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics (T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics (T_A = 25°C, V_S = ±15V)

The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	nV/√Hz
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA/√Hz
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

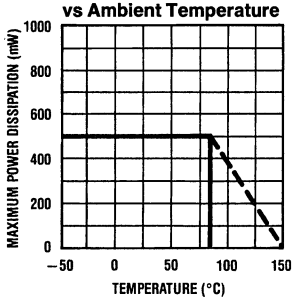
Note 1: If supply voltage is less than ±15V, it is equal to supply voltage.

Note 2: This is the permissible value at $T_A \leq 85°C$.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

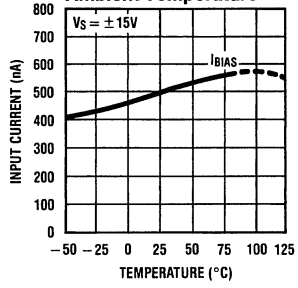
Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



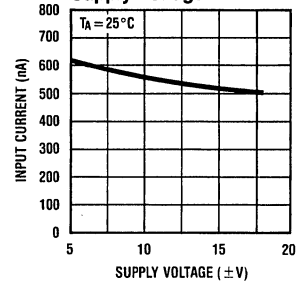
TL/H/5218–4

Input Bias Current vs Ambient Temperature



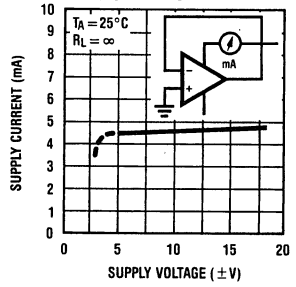
TL/H/5218–5

Input Bias Current vs Supply Voltage



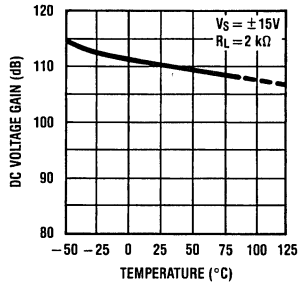
TL/H/5218–6

Supply Current vs Supply Voltage



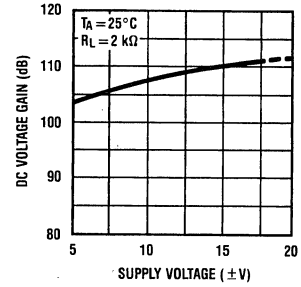
TL/H/5218–7

DC Voltage Gain vs Ambient Temperature



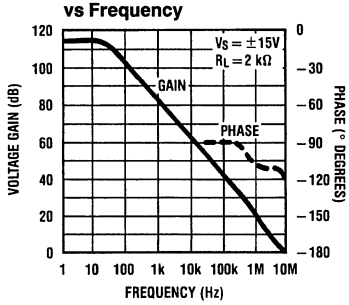
TL/H/5218–8

DC Voltage Gain vs Supply Voltage



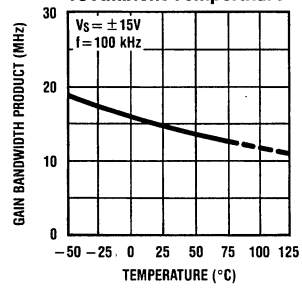
TL/H/5218–9

Voltage Gain & Phase vs Frequency



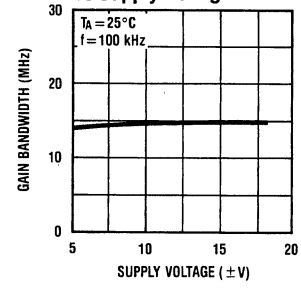
TL/H/5218–10

Gain Bandwidth Product vs Ambient Temperature



TL/H/5218–11

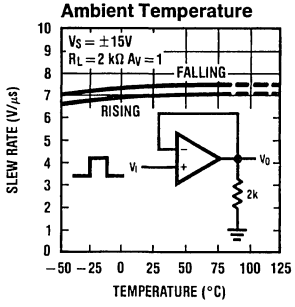
Gain Bandwidth vs Supply Voltage



TL/H/5218–12

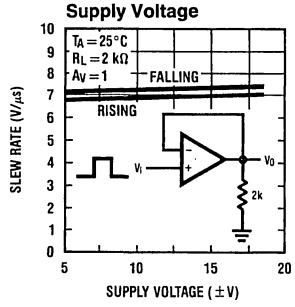
Typical Performance Characteristics (Continued)

Slew Rate vs Ambient Temperature



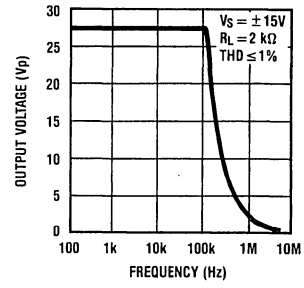
TL/H/5218–13

Slew Rate vs Supply Voltage



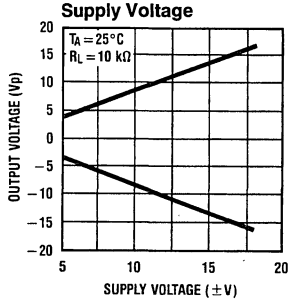
TL/H/5218–14

Power Bandwidth



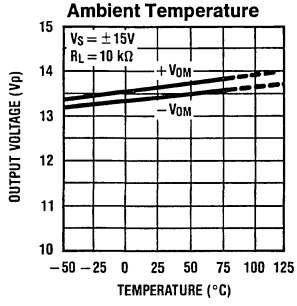
TL/H/5218–15

Maximum Output Voltage vs Supply Voltage



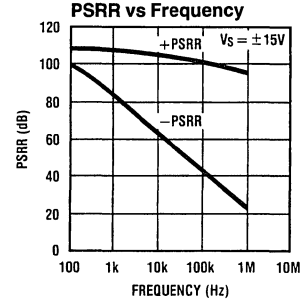
TL/H/5218–16

Maximum Output Voltage vs Ambient Temperature



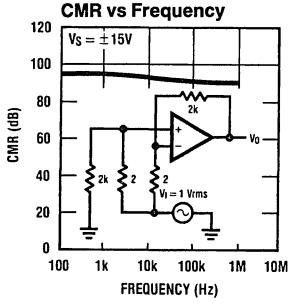
TL/H/5218–17

PSRR vs Frequency



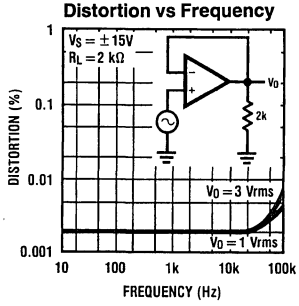
TL/H/5218–18

CMR vs Frequency



TL/H/5218–19

Distortion vs Frequency

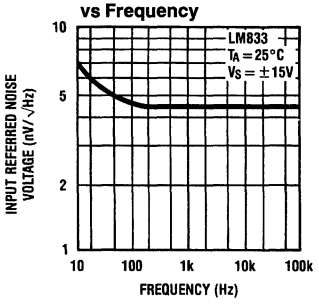


TL/H/5218–20

3

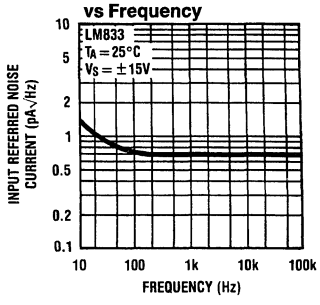
Typical Performance Characteristics (Continued)

Spot Noise Voltage vs Frequency



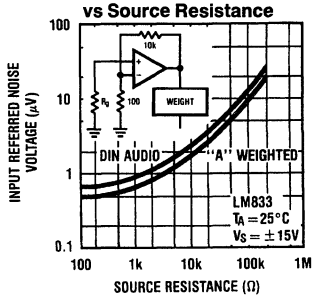
TL/H/5218–21

Spot Noise Current vs Frequency



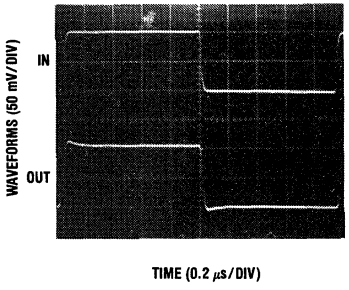
TL/H/5218–22

Input Referred Noise Voltage vs Source Resistance



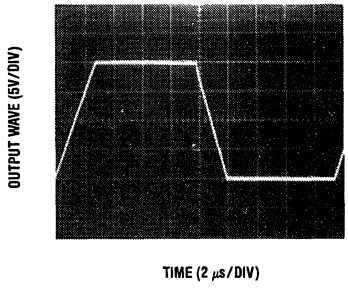
TL/H/5218–23

Noninverting Amp



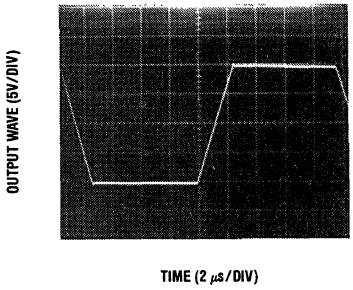
TL/H/5218–24

Noninverting Amp



TL/H/5218–25

Inverting Amp



TL/H/5218–26

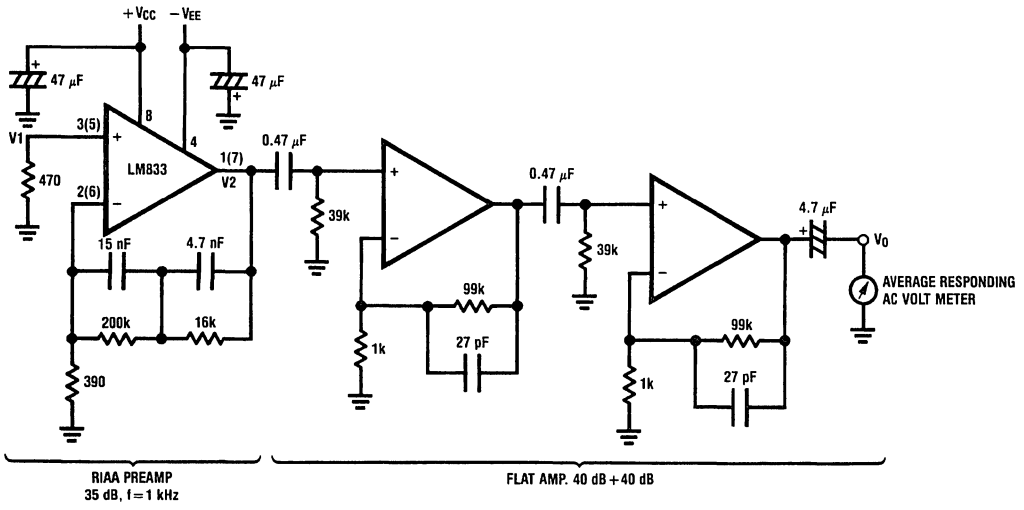
Application Hints

The LM833 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit

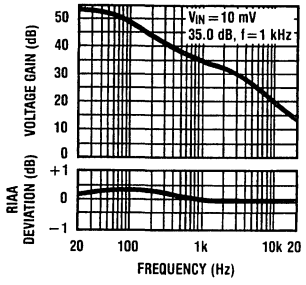
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.



TL/H/5218–27

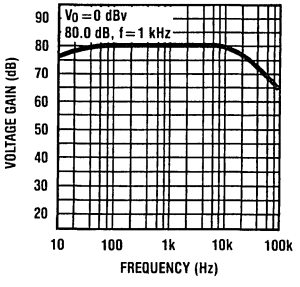
Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: e_n = V0/560,000 (V)

RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency



TL/H/5218–28

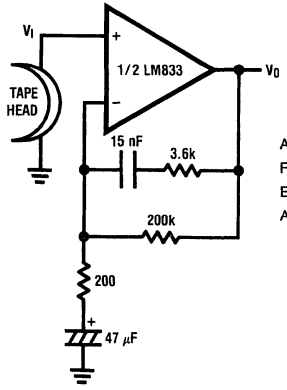
Flat Amp Voltage Gain vs Frequency



TL/H/5218–29

Typical Applications

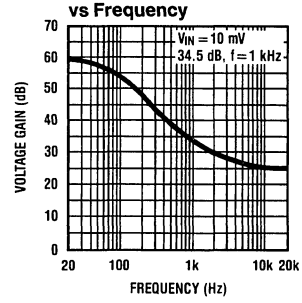
NAB Preamp



A_V = 34.5
F = 1 kHz
E_n = 0.38 µV
A Weighted

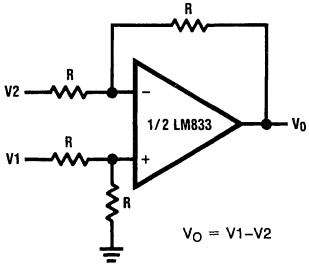
TL/H/5218–30

NAB Preamp Voltage Gain vs Frequency



TL/H/5218–31

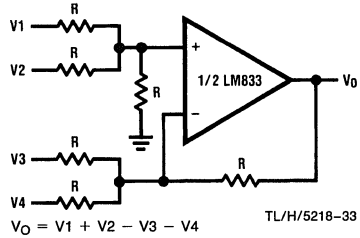
Balanced to Single Ended Converter



$V_O = V1 - V2$

TL/H/5218–32

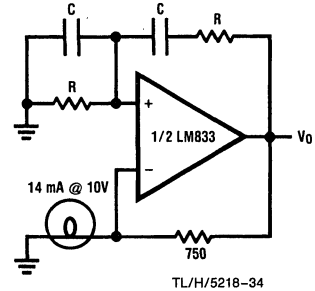
Adder/Subtracter



$V_O = V1 + V2 - V3 - V4$

TL/H/5218–33

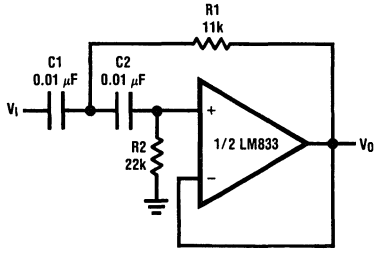
Sine Wave Oscillator



TL/H/5218–34

$$f_o = \frac{1}{2\pi RC}$$

Second Order High Pass Filter (Butterworth)



TL/H/5218–35

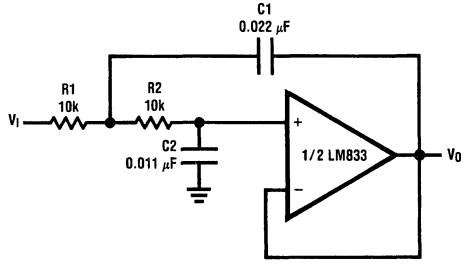
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Second Order Low Pass Filter (Butterworth)



TL/H/5218–36

if R1 = R2 = R

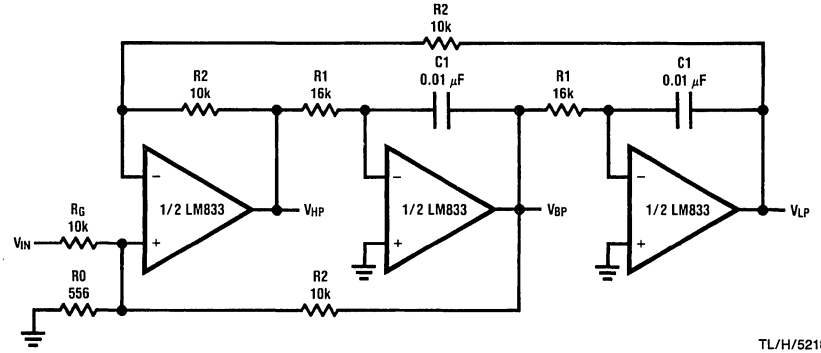
$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Typical Applications (Continued)

State Variable Filter

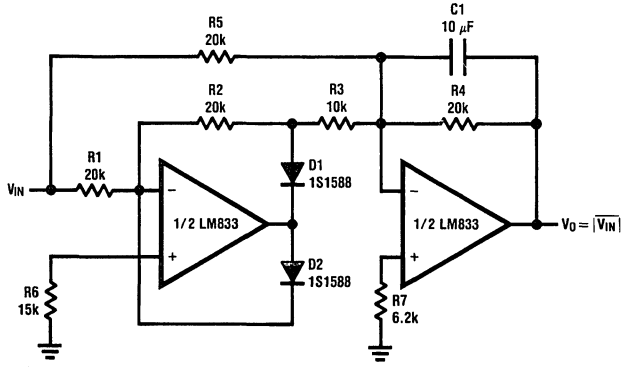


TL/H/5218-37

$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

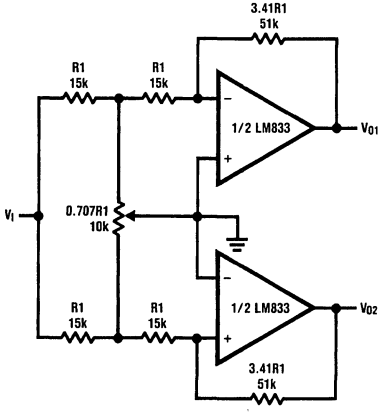
Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

AC/DC Converter



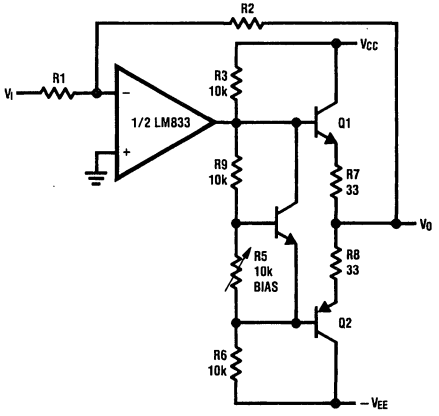
TL/H/5218-38

2 Channel Panning Circuit (Pan Pot)



TL/H/5218-39

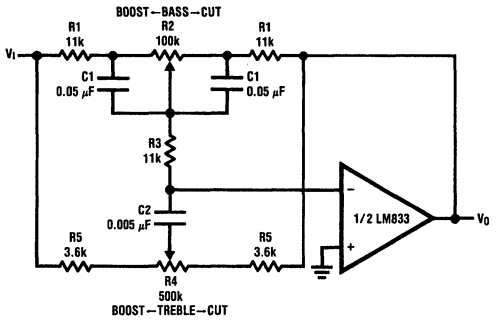
Line Driver



TL/H/5218-40

Typical Application (Continued)

Tone Control



TL/H/5218–41

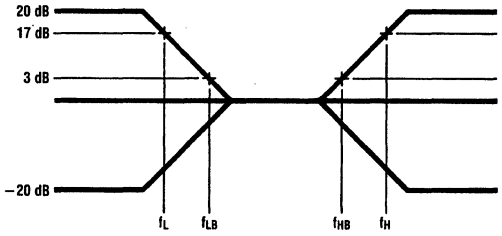
$$f_L = \frac{1}{2\pi R2C1}, f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2}, f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H = 11 kHz, f_{HB} = 1.1 kHz



TL/H/5218–42

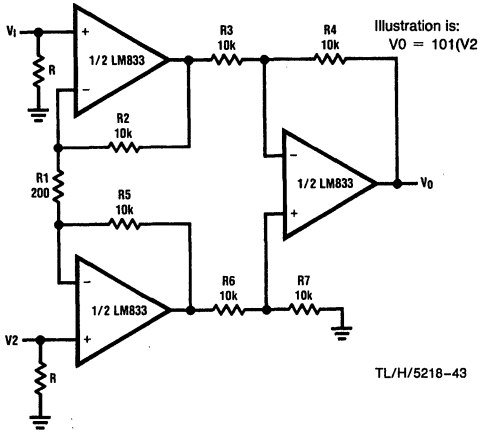
Balanced Input Mic Amp

If R2 = R5, R3 = R6, R4 = R7

$$VO = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

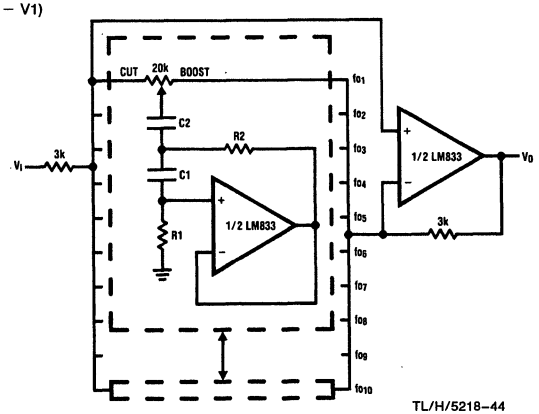
Illustration is:

VO = 101(V2 − V1)



TL/H/5218–43

10 Band Graphic Equalizer



TL/H/5218–44

fo(Hz)	C_1	C_2	R_1	R_2
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

At volume of change = ±12 dB

Q = 1.7

Reference: "AUDIO/RADIO HANDBOOK", National Semiconductor, 1980, Page 2–61

National Semiconductor

LM837 Low Noise Quad Operational Amplifier

General Description

The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

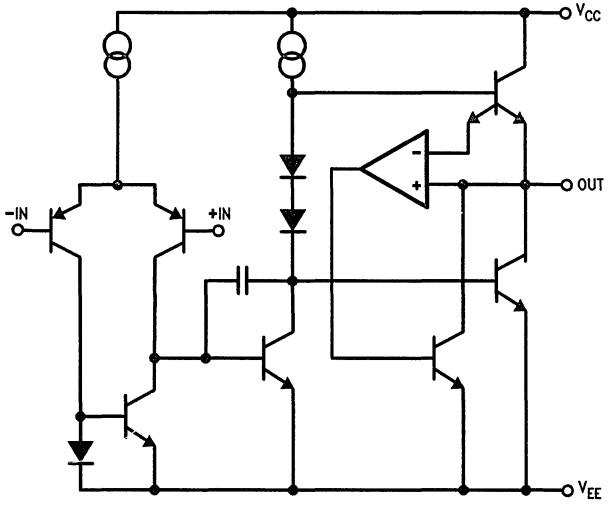
The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Features

■ High slew rate	10 V/μs (typ) 8 V/μs (min)
■ Wide gain bandwidth product	25 MHz (typ) 15 MHz (min)
■ Power bandwidth	200 kHz (typ)
■ High output current	±40 mA
■ Excellent output drive performance	>600Ω
■ Low input noise voltage	4.5 nV/√Hz
■ Low total harmonic distortion	0.0015%
■ Low offset voltage	0.3 mV

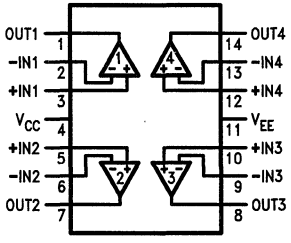
Schematic and Connection Diagrams

1/4 Quad



TL/H/9047–1

Dual-In-Line Package



TL/H/9047–2

Top View

Order Number LM837M or LM837N
See NS Package Number M14A or N14A

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	V_{CC}/V_{EE}	±18V
Differential Input Voltage (Note 1)	V_{ID}	±30V
Common Mode Input Voltage (Note 1)	V_{IC}	±15V
Power Dissipation (Note 2)	P_D	1.2W (N) 830 mW (M)
Operating Temperature Range	T_{OPR}	−40°C to +85°C
Storage Temperature Range	T_{STG}	−60°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

ESD rating is to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Large Signal Voltage Gain	$R_L = 2\,k\Omega$, $V_{OUT} = \pm 10V$	90	110		dB
V_{OM}	Output Voltage Swing	$R_L = 2\,k\Omega$	±12	±13.5		V
		$R_L = 600\Omega$	±10	±12.5		V
V_{CM}	Common Mode Input Voltage		±12	±14.0		V
CMRR	Common Mode Rejection Ratio	$V_{IN} = \pm 12V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 15 \sim 5, -15 \sim -5$	80	100		dB
I_S	Power Supply Current	$R_L = \infty$, Four Amps		10	15	mA

AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	$R_L = 600\Omega$	8	10		V/μs
GBW	Gain Bandwidth Product	$f = 100\,kHz, R_L = 600\Omega$	15	25		MHz

Design Electrical Characteristics $T_A = 25°C, V_S = \pm 15V$ (Note 3)

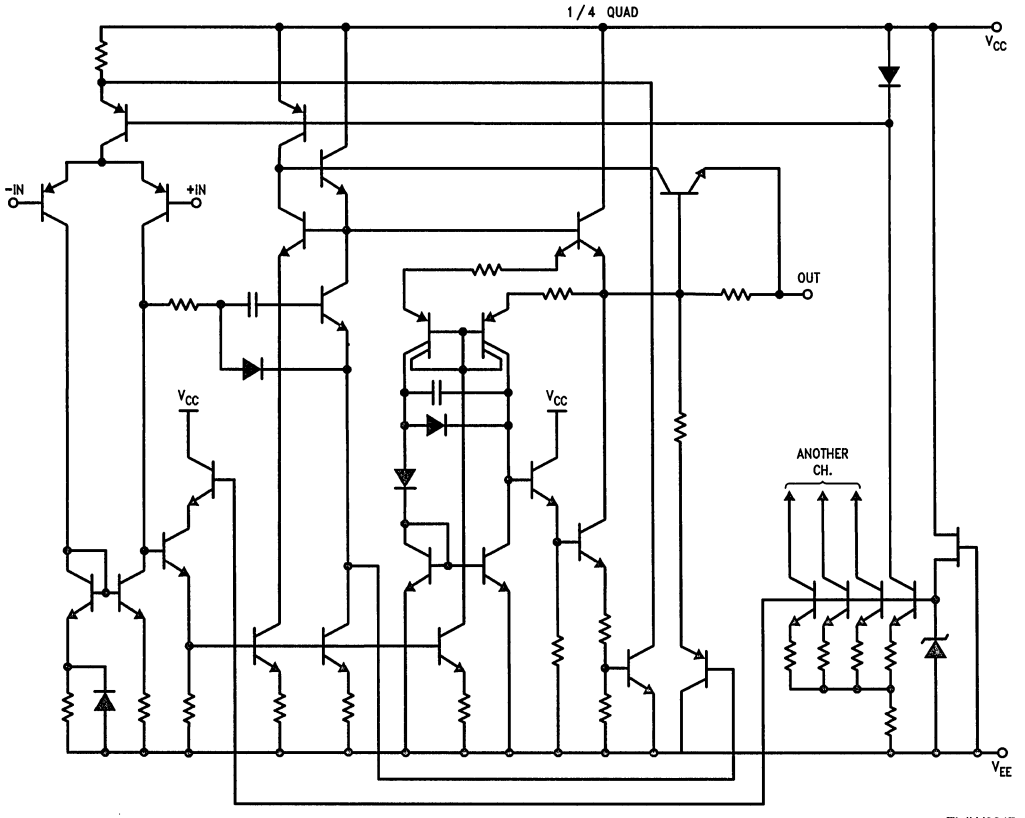
Symbol	Parameter	Condition	Min	Typ	Max	Units
PBW	Power Bandwidth	$V_O = 25\,V_{P-P}, R_L = 600\Omega$, THD < 1%		200		kHz
e_{n1}	Equivalent Input Noise Voltage	JIS A, $R_S = 100\Omega$		0.5		μV
e_{n2}	Equivalent Input Noise Voltage	f = 1 kHz		4.5		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1 kHz		0.7		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	$A_V = 1, V_{OUT} = 3\,Vrms$, $f = 20 \sim 20\,kHz, R_L = 600\Omega$		0.0015		%
f_U	Zero Cross Frequency	Open Loop		12		MHz
ϕ_m	Phase Margin	Open Loop		45		deg
	Input-Referred Crosstalk	$f = 20 \sim 20\,kHz$		−120		dB
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			2		μV/°C

Note 1: Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.

Note 2: For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90°C/W; LM837M, 150°C/W.

Note 3: The following parameters are not tested or guaranteed.

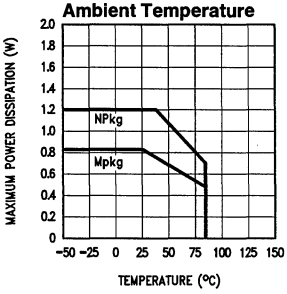
Detailed Schematic



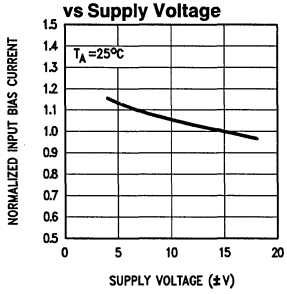
TL/H/9047–3

Typical Performance Characteristics

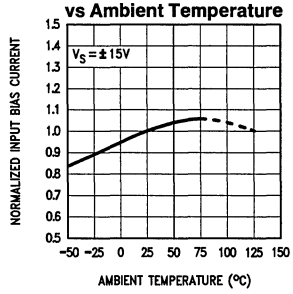
Maximum Power Dissipation vs Ambient Temperature



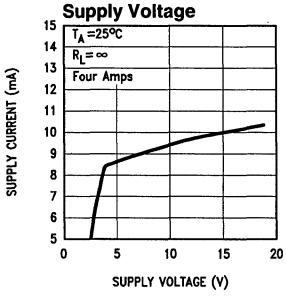
Normalized Input Bias Current vs Supply Voltage



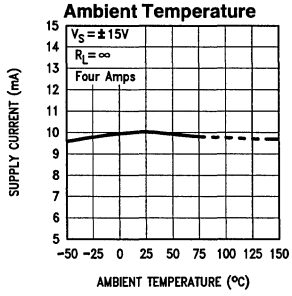
Normalized Input Bias Current vs Ambient Temperature



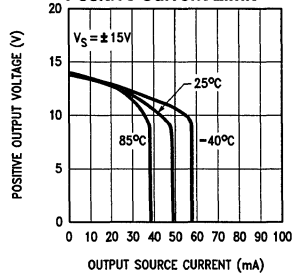
Supply Current vs Supply Voltage



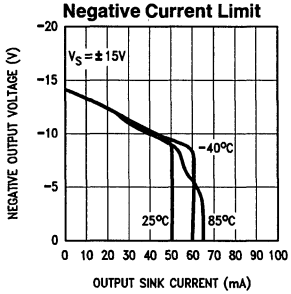
Supply Current vs Ambient Temperature



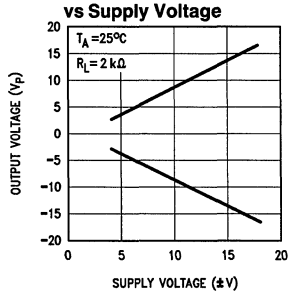
Positive Current Limit



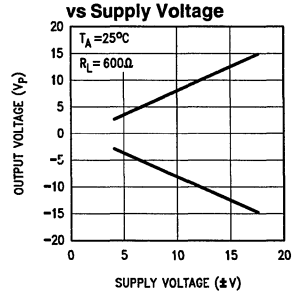
Negative Current Limit



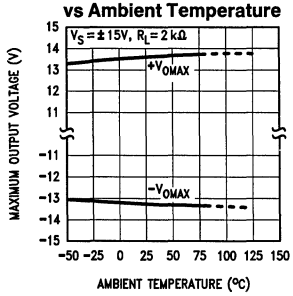
Maximum Output Voltage vs Supply Voltage



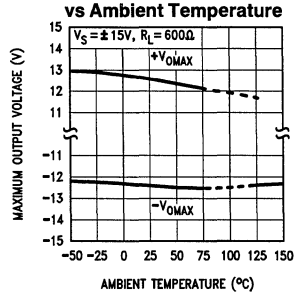
Maximum Output Voltage vs Supply Voltage



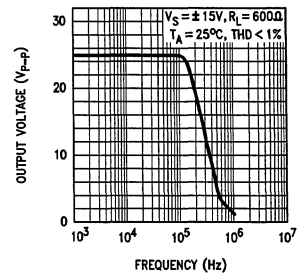
Maximum Output Voltage vs Ambient Temperature



Maximum Output Voltage vs Ambient Temperature



Power Bandwidth



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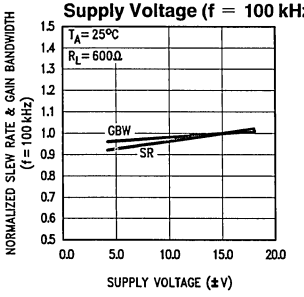
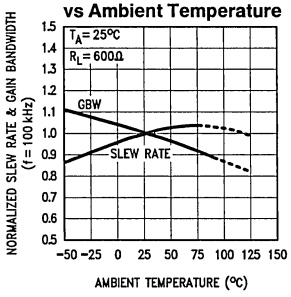
Typical Performance Characteristics (Continued)

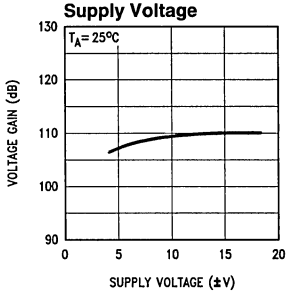
Normalized Slew Rate & Gain Bandwidth vs Supply Voltage (f = 100 kHz)



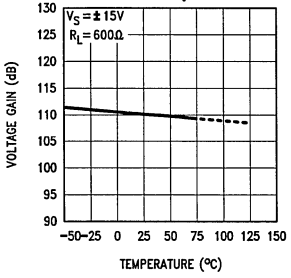
Normalized Slew Rate & Gain Bandwidth (f = 100 kHz) vs Ambient Temperature



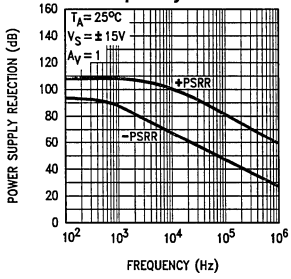
Voltage Gain vs Supply Voltage



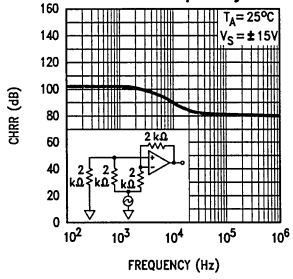
Voltage Gain vs Ambient Temperature



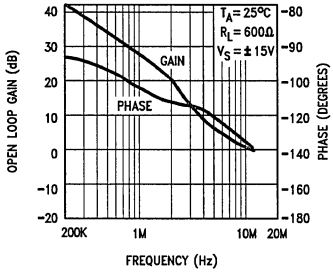
Power Supply Rejection vs Frequency



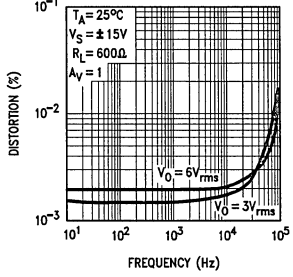
CMRR vs Frequency



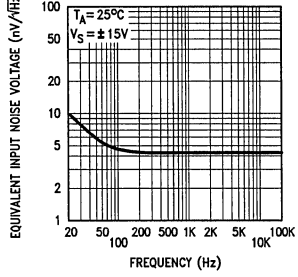
Open Loop Gain & Phase vs Frequency



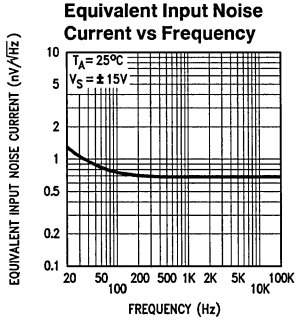
Total Harmonic Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



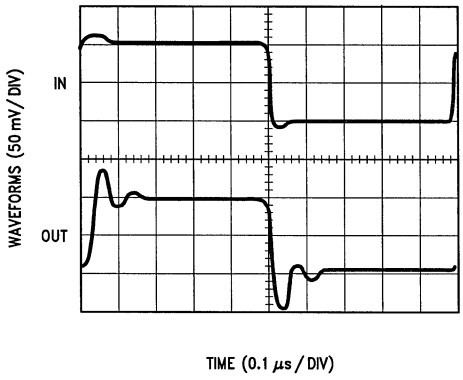
Equivalent Input Noise Current vs Frequency



TL/H/9047–5

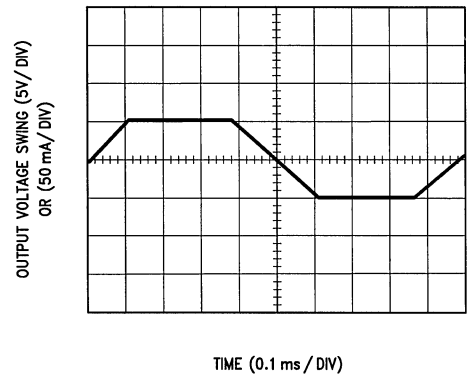
Typical Performance Characteristics (Continued)

Small Signal, Non-Inverting
$T_A = 25°C, A_V = 1, R_L = 600\Omega, V_S = \pm 15V$



TL/H/9047–6

Current Limit
$T_A = 25°C, V_S = \pm 15V, R_L = 100\Omega, A_V = 1$



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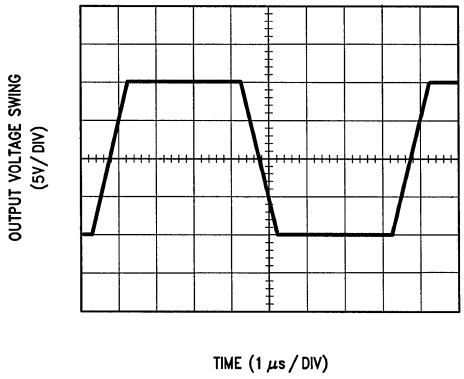
Large Signal Non-Inverting
$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$



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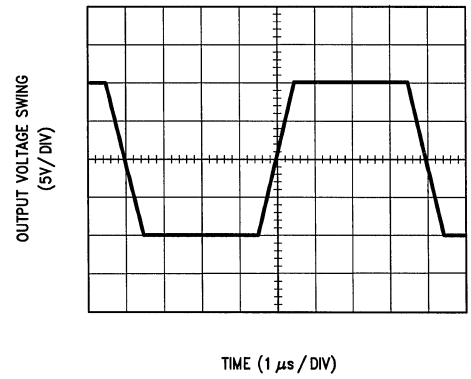
Large Signal Inverting
$T_A = 25°C, R_L = 600\Omega, V_S = \pm 15V$



TL/H/9047–9

National Semiconductor

LM1558/LM1458 Dual Operational Amplifier

General Description

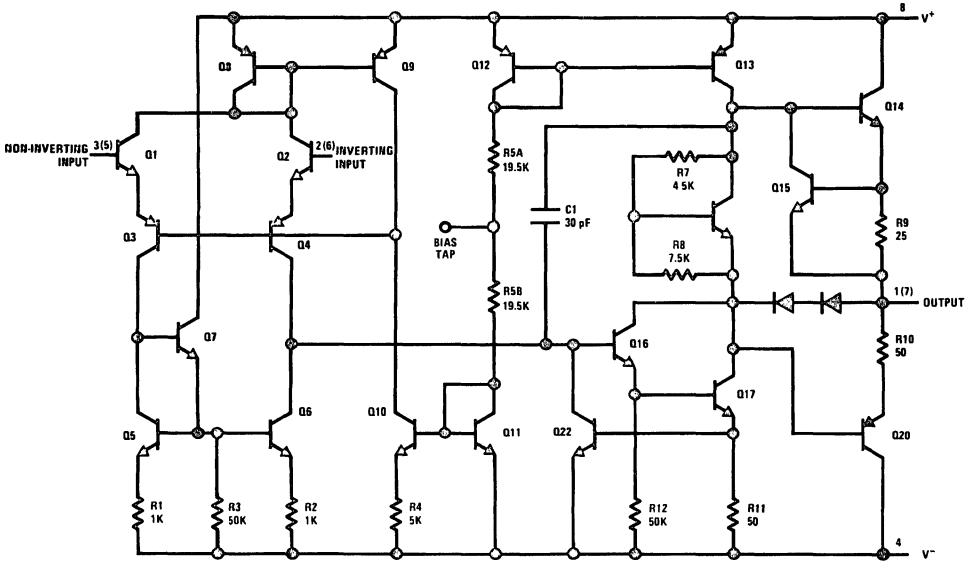
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

Schematic and Connection Diagrams



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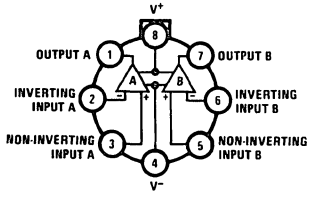
Note: Numbers in parentheses are pin numbers for amplifier B.

Metal Can Package



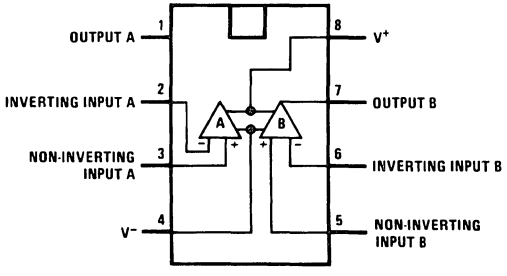
TL/H/7886–2

Top View

Order Number LM1558H or LM1458H

See NS Package Number H08C

Dual-In-Line Package



TL/H/7886–3

Top View

Order Number LM1558J, LM1458J, LM1458M or LM1458N

See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage	
LM1558	±22V
LM1458	±18V
Power Dissipation (Note 1)	
LM1558H/LM1458H	500 mW
LM1458N	400 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LM1558	−55°C to +125°C
LM1458	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5) 300V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM1558			LM1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		80	200		80	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		20	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 20°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = \pm 15V$.

Note 4: Refer to RETS 1558V for LM1558J and LM1558H military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM2900/LM3900/LM3301/LM3401 Quad Amplifiers

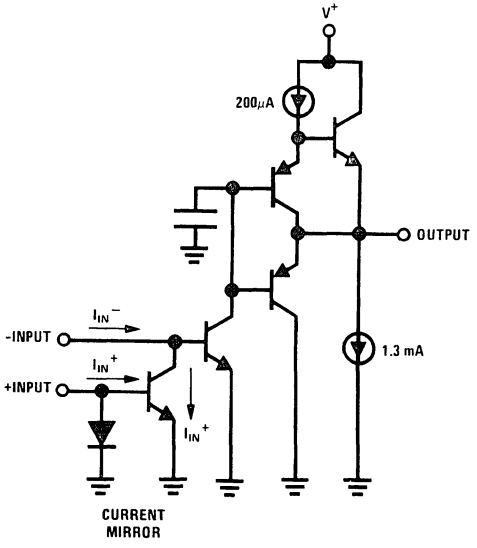
General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Features

- Wide single supply voltage — 4 V_{DC} to 32 V_{DC}
  Range or dual supplies — ±2 V_{DC} to ±16 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (unity gain)
- Large output voltage swing — (V^+ − 1) Vp-p
- Internally frequency compensated for unity gain
- Output short-circuit protection

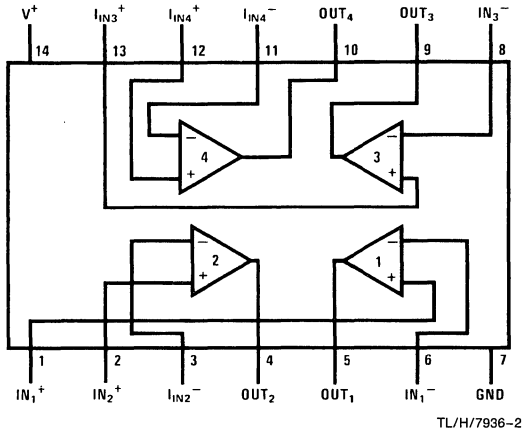
Schematic and Connection Diagrams



TL/H/7936–1

Order Number LM3900M
See NS Package Number M14A

Dual-In-Line and Flat Package



TL/H/7936–2

Top View

Order Number LM2900N, LM3900N, LM3301N or LM3401N
See NS Package Number N14A

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM2900/LM3900	LM3301	LM3401
Supply Voltage	32 V_{DC} ±16 V_{DC}	28 V_{DC} ±14 V_{DC}	18 V_{DC} ±9 V_{DC}
Power Dissipation (T_A = 25°C) (Note 1)			
Molded DIP	1080 mW	1080 mW	1080 mW
S.O. Package	765 mW		
Input Currents, I_{IN}^+ or I_{IN}^-	20 mA_{DC}	20 mA_{DC}	20 mA_{DC}
Output Short-Circuit Duration—One Amplifier T_A = 25°C (See Application Hints)	Continuous	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C	0°C to +75°C
LM2900	−40°C to +85°C		
LM3900	0°C to +70°C		
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C	260°C	260°C
Soldering Information			
Dual-In-Line Package			
Soldering (10 sec.)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 sec.)	215°C	215°C	215°C
Infrared (15 sec.)	220°C	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 7)	2000V	2000V	2000V

Electrical Characteristics T_A = 25°C, V^+ = 15 V_{DC}, unless otherwise stated

Parameter		Conditions		LM2900			LM3900			LM3301			LM3401			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open Loop	Voltage Gain	Over Temp.											0.8			V/mV
	Voltage Gain	ΔV_O = 10 V_{DC} Inverting Input		1.2	2.8		1.2	2.8		1.2	2.8		1.2	2.8		
	Input Resistance				1			1			1		0.1	1		MΩ
	Output Resistance				8			8			9			8		kΩ
Unity Gain Bandwidth		Inverting Input			2.5			2.5			2.5			2.5		MHz
Input Bias Current		Inverting Input, V^+ = 5 V_{DC} Inverting Input			30	200		30	200		30	300		30	300 500	nA
Slew Rate		Positive Output Swing Negative Output Swing			0.5 20			0.5 20			0.5 20			0.5 20		V/μs
Supply Current		R_L = ∞ On All Amplifiers			6.2	10		6.2	10		6.2	10		6.2	10	mA_{DC}
Output Voltage Swing	V_{OUT} High	R_L = 2k, V^+ = 15.0 V_{DC}	I_{IN}^- = 0, I_{IN}^+ = 0	13.5			13.5			13.5			13.5			V_{DC}
	V_{OUT} Low		I_{IN}^- = 10 μA, I_{IN}^+ = 0		0.09	0.2		0.09	0.2		0.09	0.2		0.09	0.2	
	V_{OUT} High	V^+ = Absolute Maximum Ratings	I_{IN}^- = 0, I_{IN}^+ = 0 R_L = ∞,	29.5			29.5			26.0			16.0			
Output Current Capability	Source			6	18		6	10		5	18		5	10		mA_{DC}
	Sink	(Note 2)		0.5	1.3		0.5	1.3		0.5	1.3		0.5	1.3		
	I_{SINK}	V_{OL} = 1V, I_{IN}^- = 5 μA			5			5			5			5		

Electrical Characteristics (Note 6), $V^+ = 15\ V_{DC}$, unless otherwise stated (Continued)

Parameter	Conditions	LM2900			LM3900			LM3301			LM3401			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection	$T_A = 25°C$, f = 100 Hz		70			70			70			70		dB
Mirror Gain	@ 20 μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	0.90	1	1.10	μA/μA
	@ 200 μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	0.90	1	1.10	
ΔMirror Gain	@ 20 μA to 200 μA (Note 3)		2	5		2	5		2	5		2	5	%
Mirror Current	(Note 4)		10	500		10	500		10	500		10	500	μA_{DC}
Negative Input Current	$T_A = 25°C$ (Note 5)		1.0			1.0			1.0			1.0		mA_{DC}
Input Bias Current	Inverting Input		300			300								nA

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 92°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. Thermal resistance for the S.O. package is 131°C/W.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10 μA. This is therefore a typical design center for many of the application circuits.

Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately $-0.3\ V_{DC}$. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

Note 6: These specs apply for $-40°C \leq T_A \leq +85°C$, unless otherwise stated.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Application Hints

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated $+5\ V_{DC}$ power supply at $T_A = 25°C$ with a 100 kΩ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above T_J max. Larger feedback resistors will reduce the current, 11 MΩ provides approximately 30 mA, an open circuit provides 1.3 mA, and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to V^+ as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at $T_A = 25°C$.

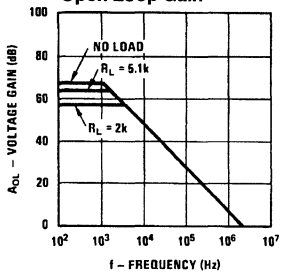
Unintentional signal coupling from the output to the non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional AC signal pickup.

Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{BE}$. Internal clamp transistors (see note 5) catch-negative input voltages at approximately $-0.3\ V_{DC}$ but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately 100 μA.

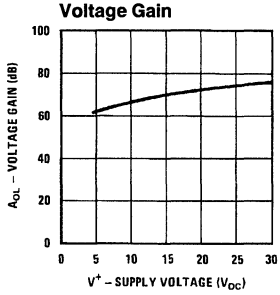
This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a DC amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the AC gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output DC voltage.

Typical Performance Characteristics

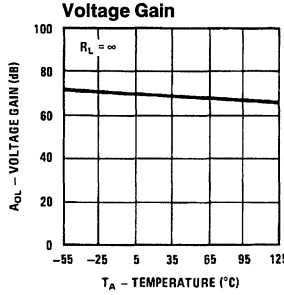
Open Loop Gain



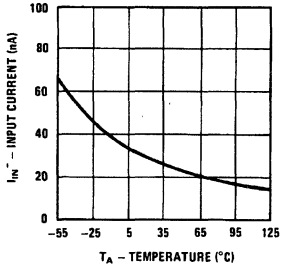
Voltage Gain



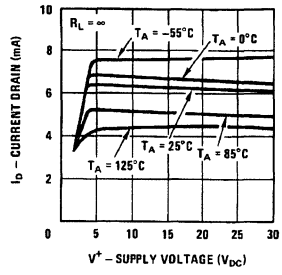
Voltage Gain



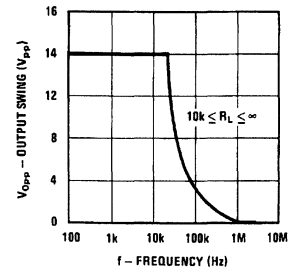
Input Current



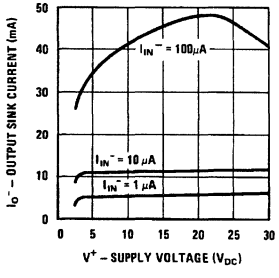
Supply Current



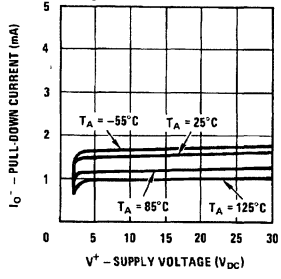
Large Signal Frequency Response



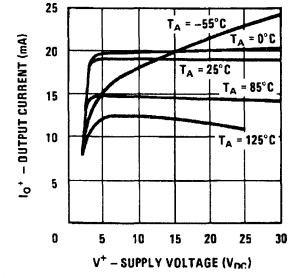
Output Sink Current



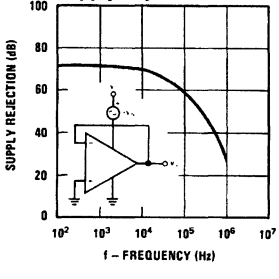
Output Class-A Bias Current



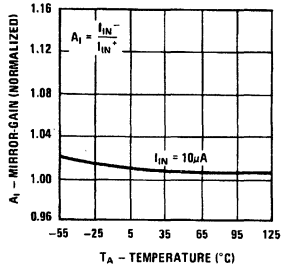
Output Source Current



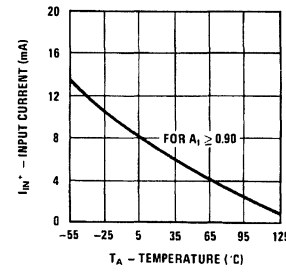
Supply Rejection



Mirror Gain



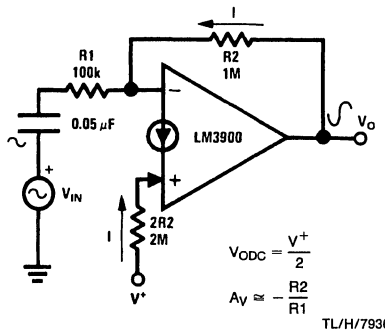
Maximum Mirror Current



TL/H/7936–9

Typical Applications ($V^+ = 15\ V_{DC}$)

Inverting Amplifier

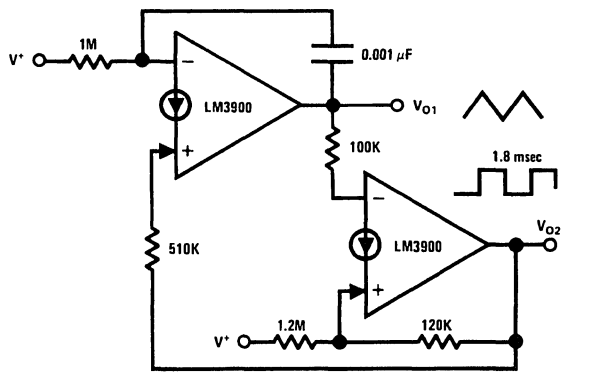


$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong -\frac{R2}{R1}$$

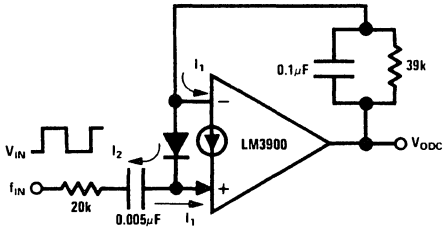
TL/H/7936-3

Triangle/Square Generator



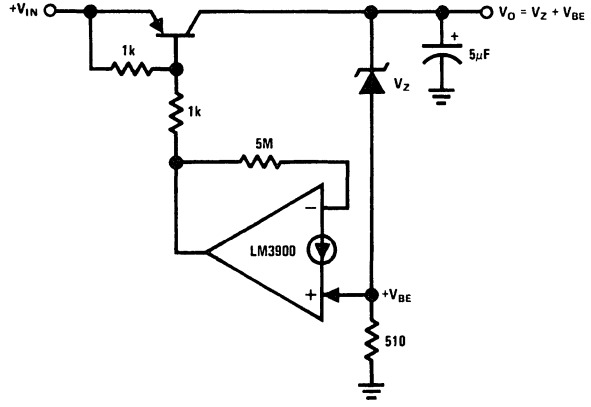
TL/H/7936-4

Frequency-Doubling Tachometer



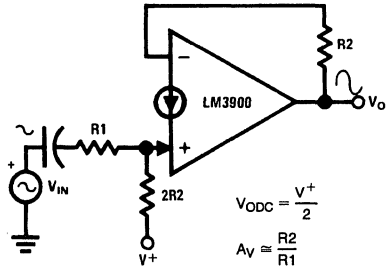
TL/H/7936-5

Low $V_{IN} - V_{OUT}$ Voltage Regulator



TL/H/7936-6

Non-Inverting Amplifier

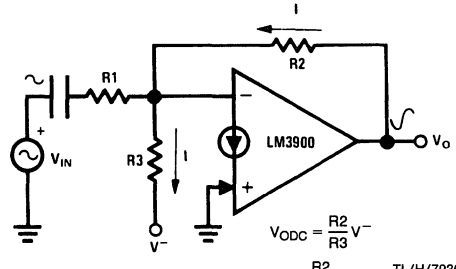


$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-7

Negative Supply Biasing



$$V_{ODC} = \frac{R2}{R3}V^-$$

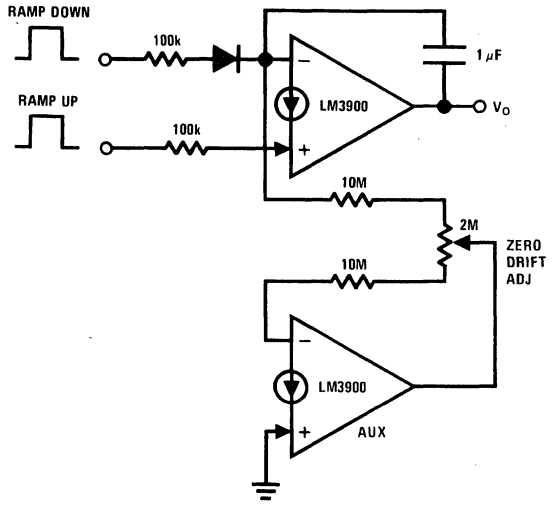
$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-8

3

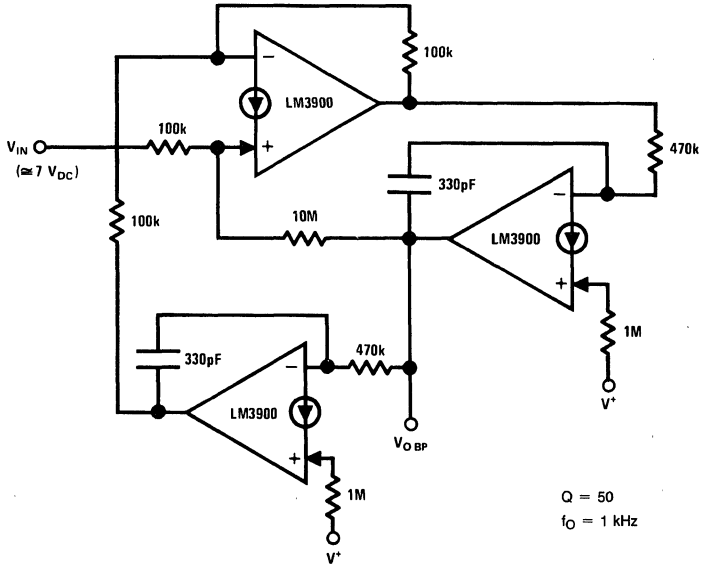
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Drift Ramp and Hold Circuit



TL/H/7936–10

Bi-Quad Active Filter
(2nd Degree State-Variable Network)

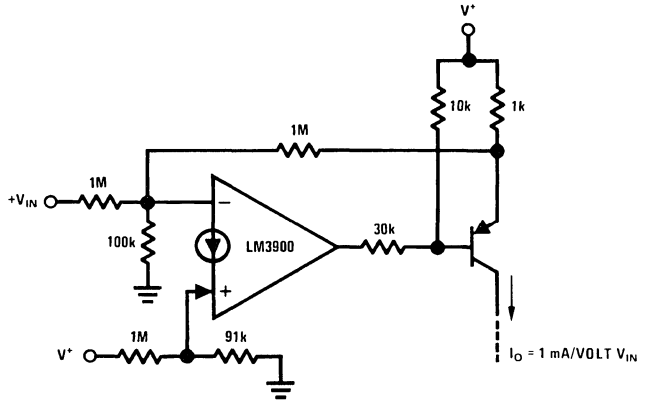


Q = 50
f_O = 1 kHz

TL/H/7936–11

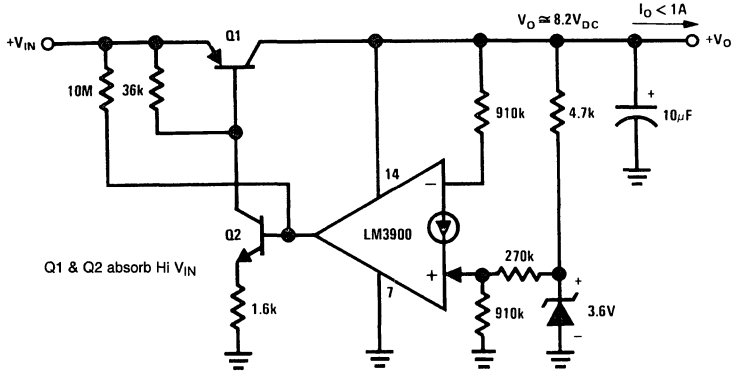
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Voltage-Controlled Current Source (Transconductance Amplifier)



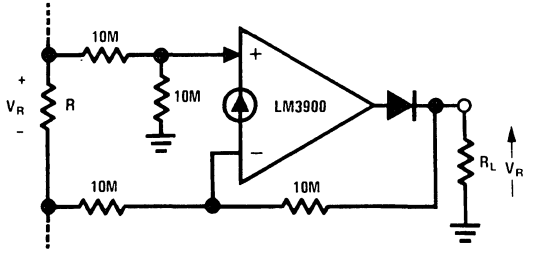
TL/H/7936–12

Hi V_{IN}, Lo (V_{IN} − V_O) Self-Regulator



TL/H/7936–13

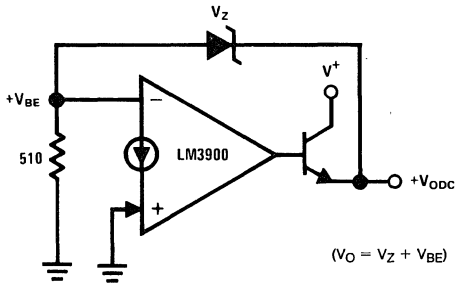
Ground-Referencing a Differential Input Signal



TL/H/7936–14

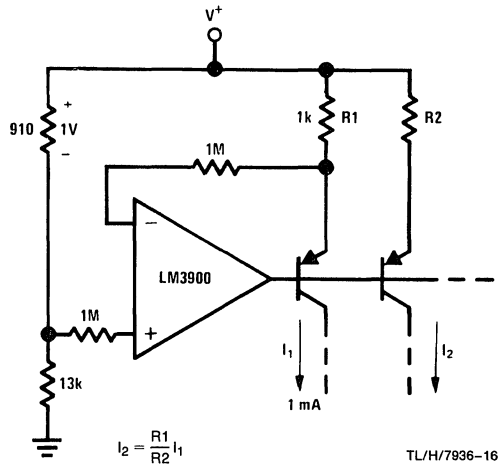
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Voltage Regulator



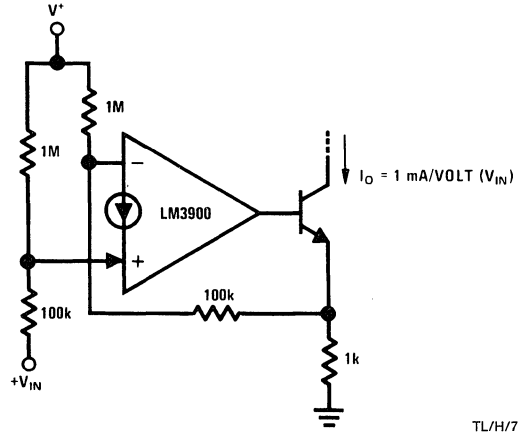
TL/H/7936–15

Fixed Current Sources



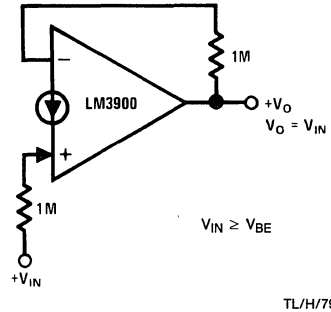
TL/H/7936–16

Voltage-Controlled Current Sink (Transconductance Amplifier)



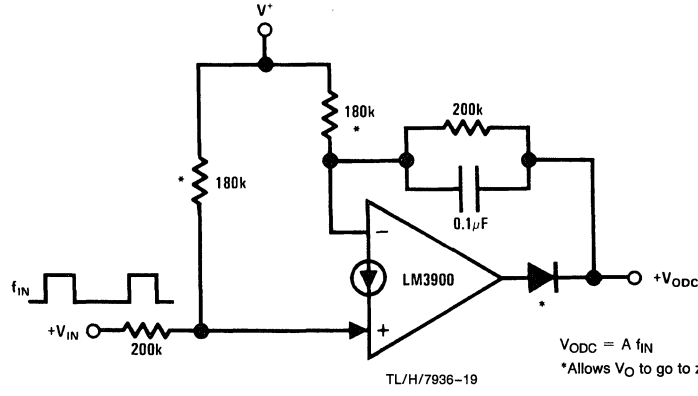
TL/H/7936–17

Buffer Amplifier



TL/H/7936–18

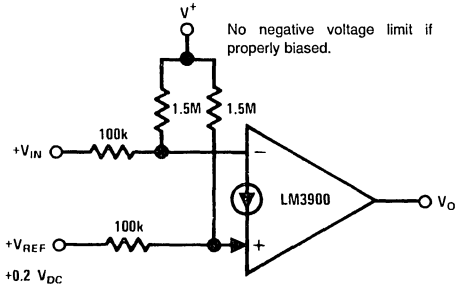
Tachometer



TL/H/7936–19

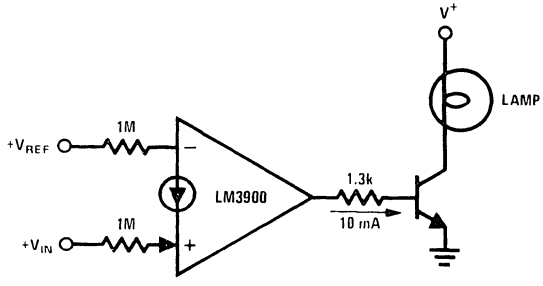
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Voltage Comparator



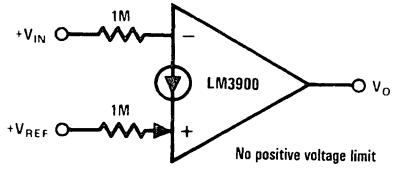
TL/H/7936–20

Power Comparator



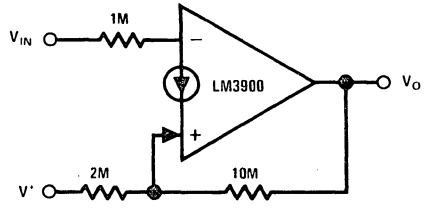
TL/H/7936–21

Comparator



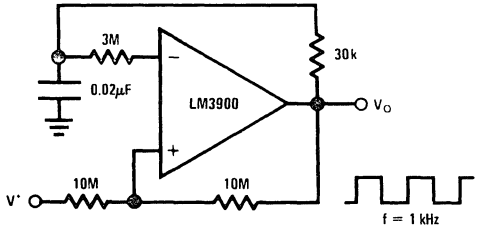
TL/H/7936–22

Schmitt-Trigger



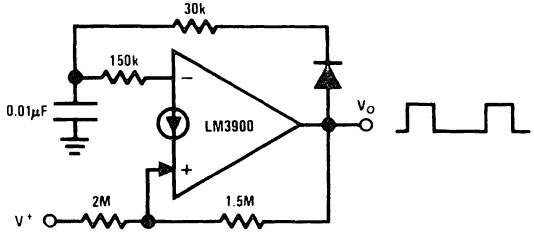
TL/H/7936–23

Square-Wave Oscillator



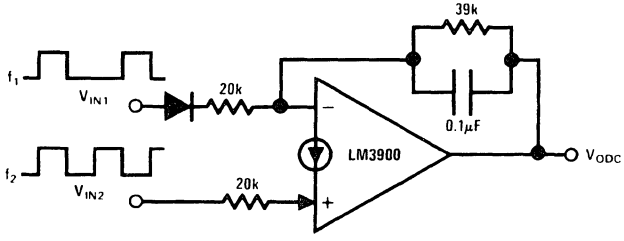
TL/H/7936–24

Pulse Generator



TL/H/7936–25

Frequency Differencing Tachometer

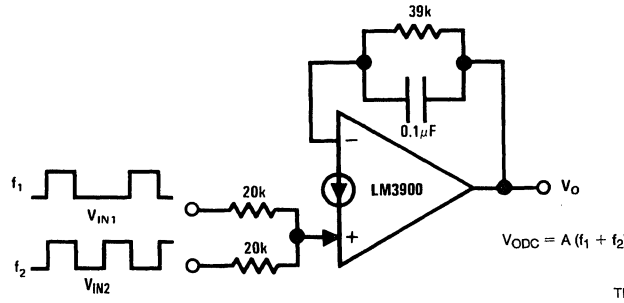


$V_{ODC} = A\ (f_1 - f_2)$

TL/H/7936–26

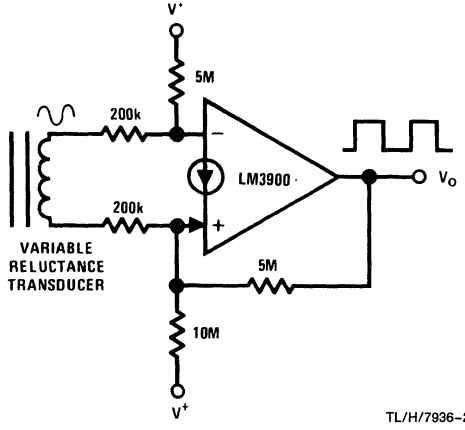
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Frequency Averaging Tachometer



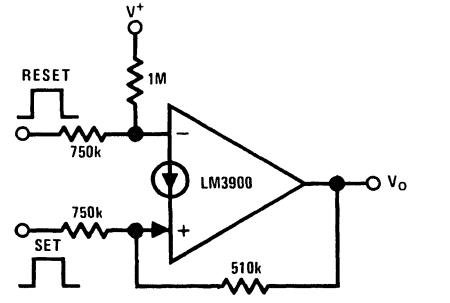
TL/H/7936-27

Squaring Amplifier (W/Hysteresis)



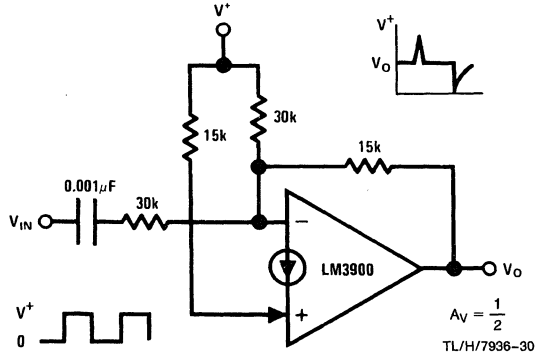
TL/H/7936-28

Bi-Stable Multivibrator



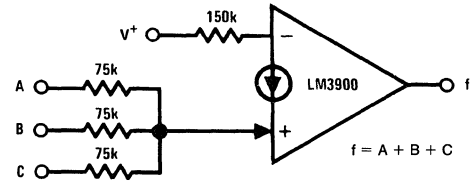
TL/H/7936-29

Differentiator (Common-Mode Biasing Keeps Input at $+V_{BE}$)



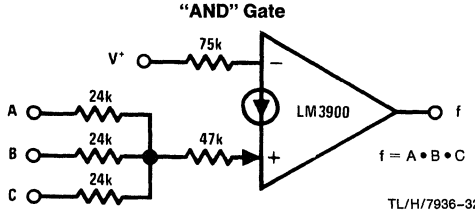
TL/H/7936-30

"OR" Gate



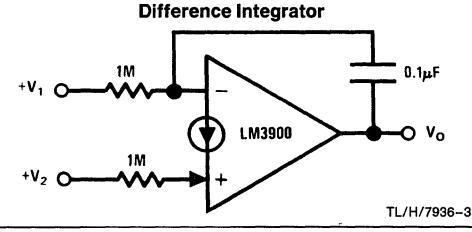
TL/H/7936-31

"AND" Gate



TL/H/7936-32

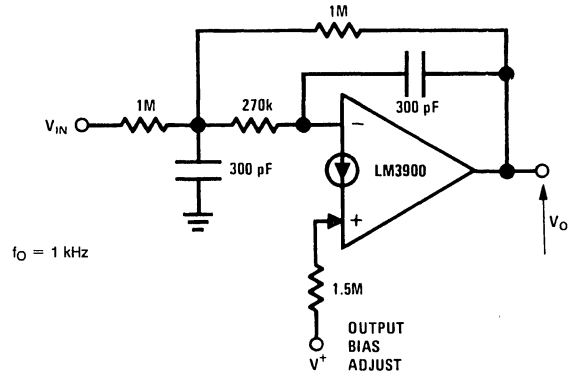
Difference Integrator



TL/H/7936-33

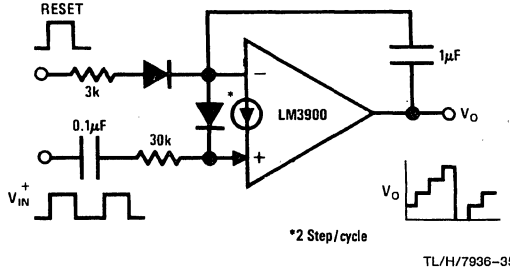
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Low Pass Active Filter



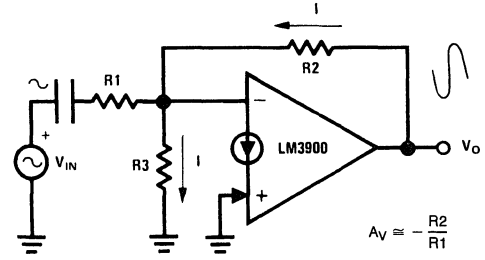
TL/H/7936–34

Staircase Generator



TL/H/7936–35

V_{BE} Biasing

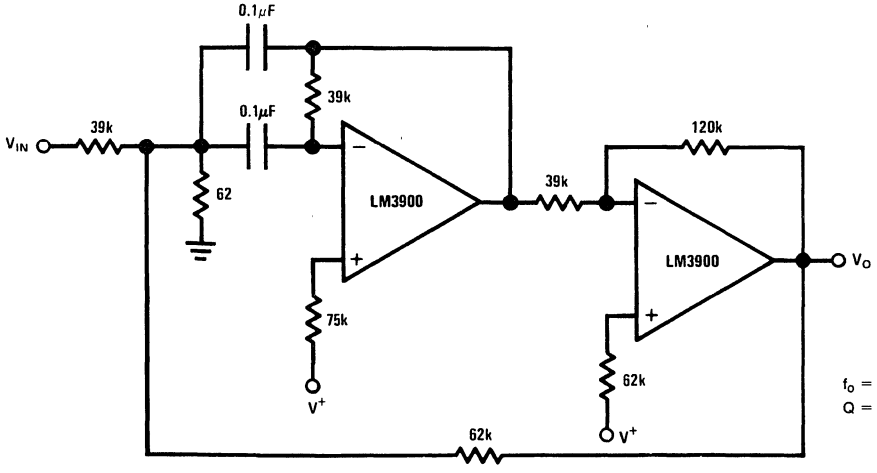


$V_{BE} = 0.5\ V_{DC}$

$V_{ODC} = V_{BE}\left(1 + \frac{R2}{R3}\right)$

TL/H/7936–36

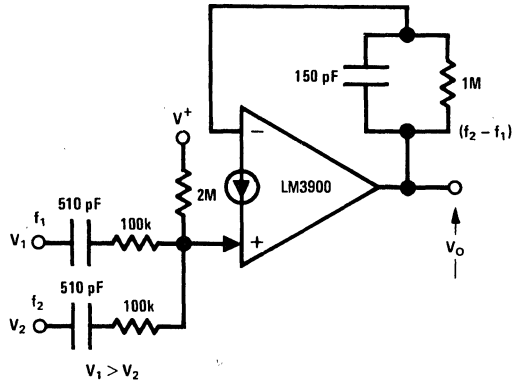
Bandpass Active Filter



TL/H/7936–37

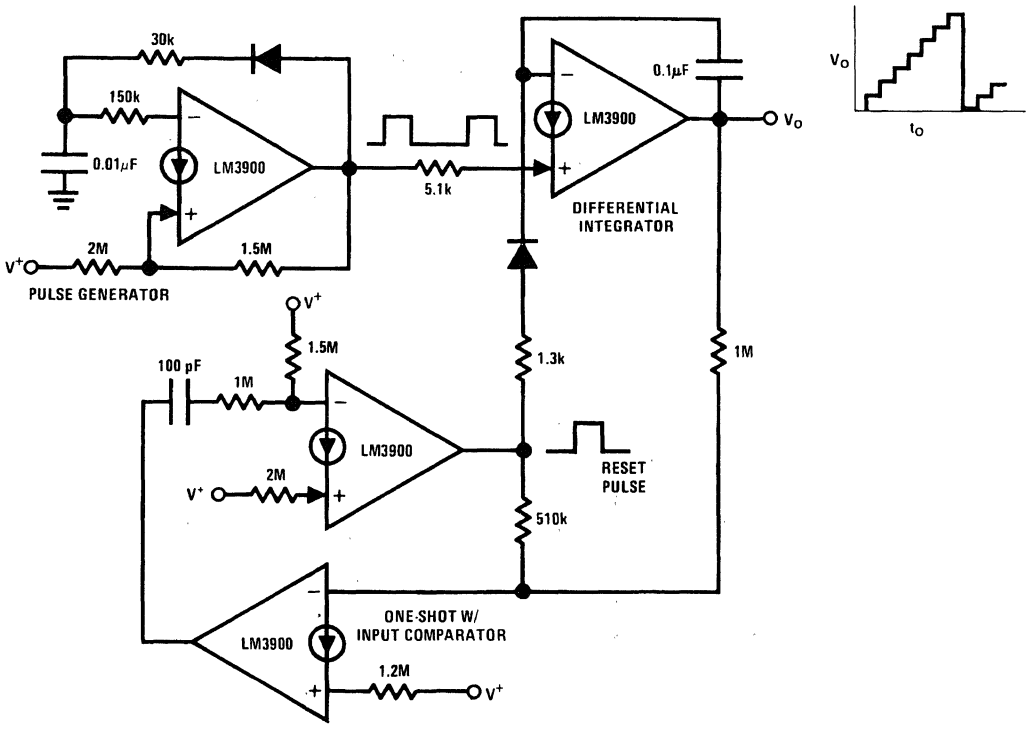
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Frequency Mixer



TL/H/7936–38

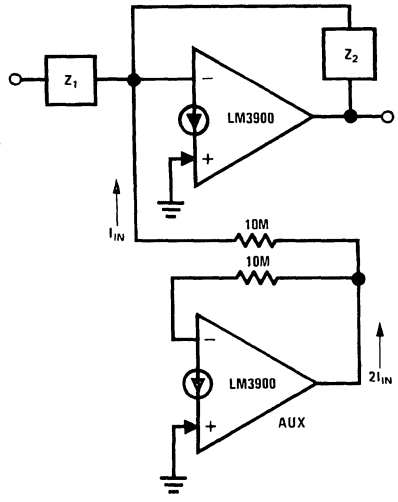
Free-Running Staircase Generator/Pulse Counter



TL/H/7936–39

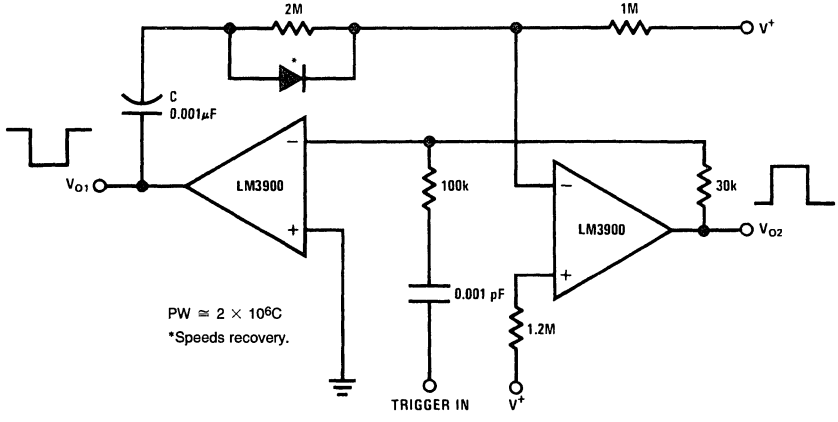
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Supplying I_{IN} with Aux. Amp (to Allow Hi-Z Feedback Networks)



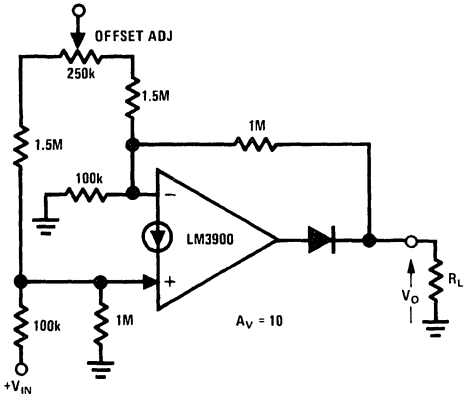
TL/H/7936–40

One-Shot Multivibrator



TL/H/7936–41

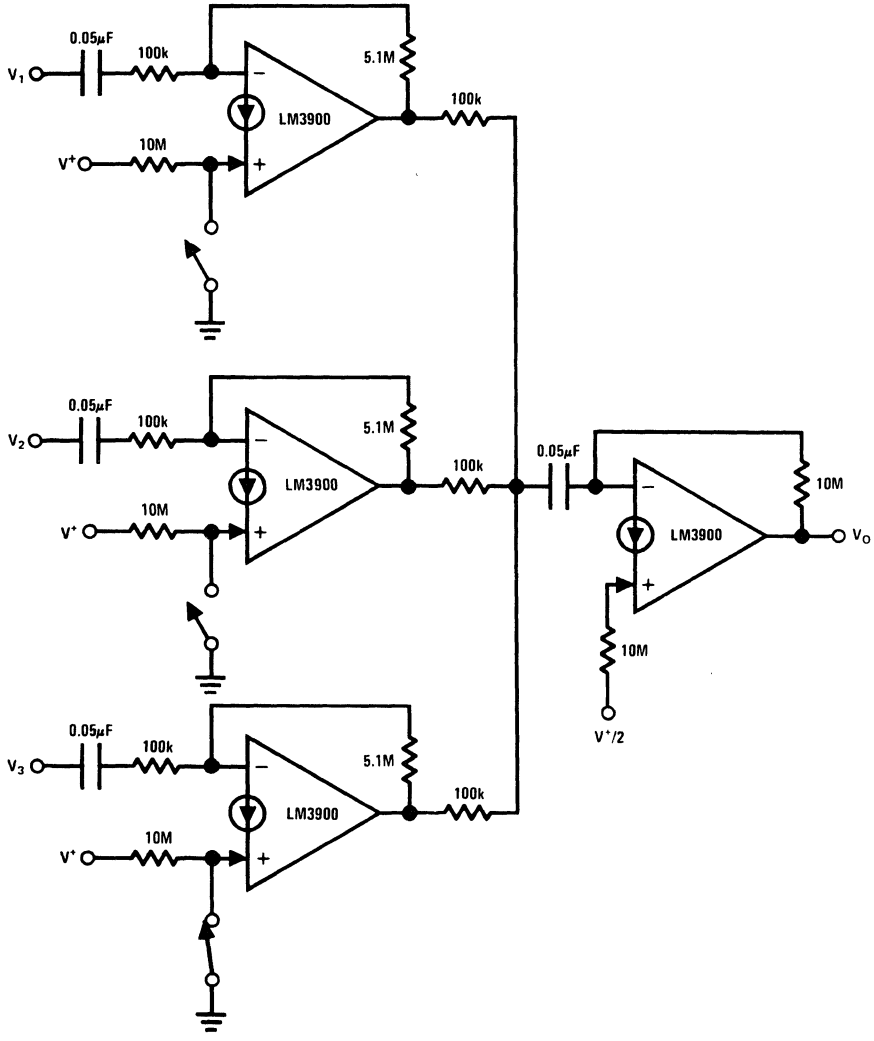
Non-Inverting DC Gain to (0,0)



TL/H/7936–42

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

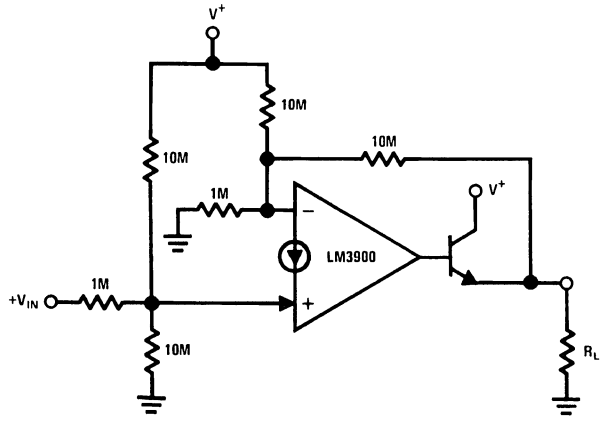
Channel Selection by DC Control (or Audio Mixer)



TL/H/7936–43

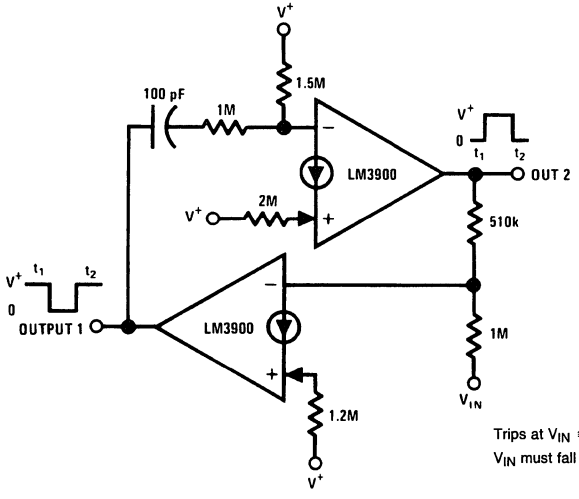
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Power Amplifier



TL/H/7936–44

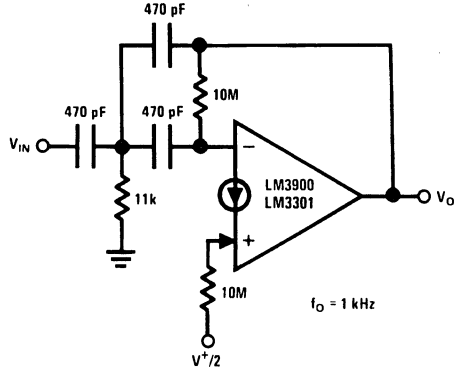
One-Shot with DC Input Comparator



Trips at $V_{IN} \cong 0.8\ V^+$
V_{IN} must fall 0.8 V^+ prior to t_2

TL/H/7936–45

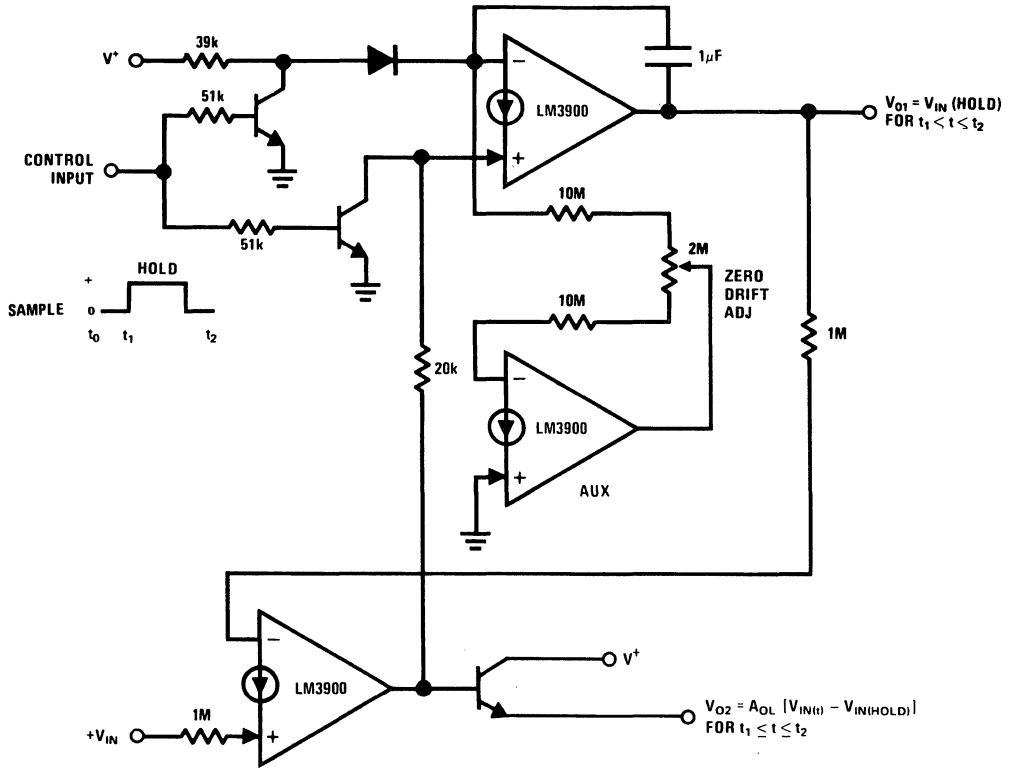
High Pass Active Filter



TL/H/7936–46

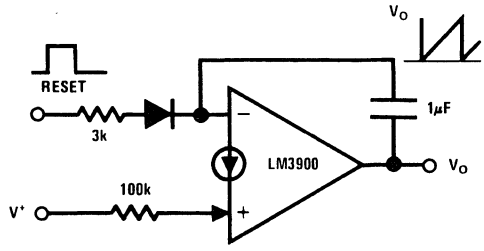
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Sample-Hold and Compare with New $+V_{IN}$



TL/H/7936–47

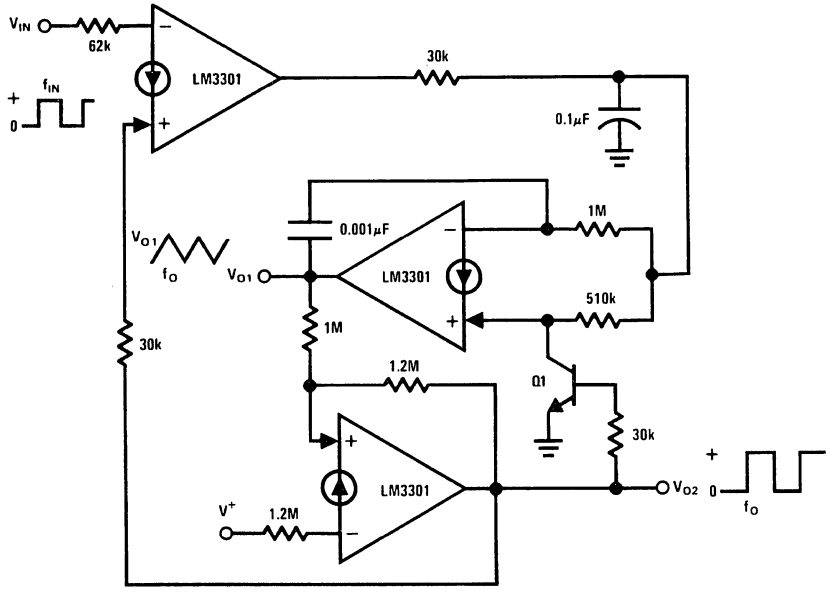
Sawtooth Generator



TL/H/7936–48

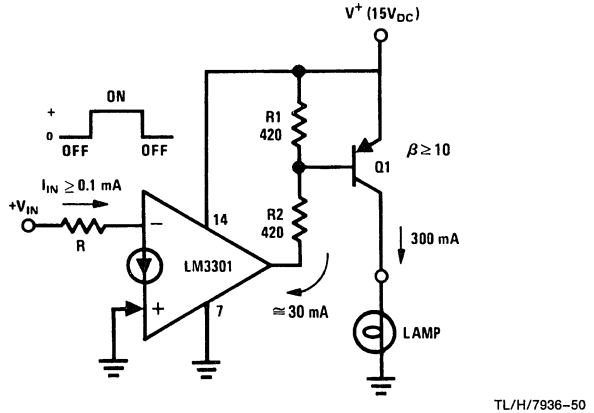
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Phase-Locked Loop



TL/H/7936–49

Boosting to 300 mA Loads

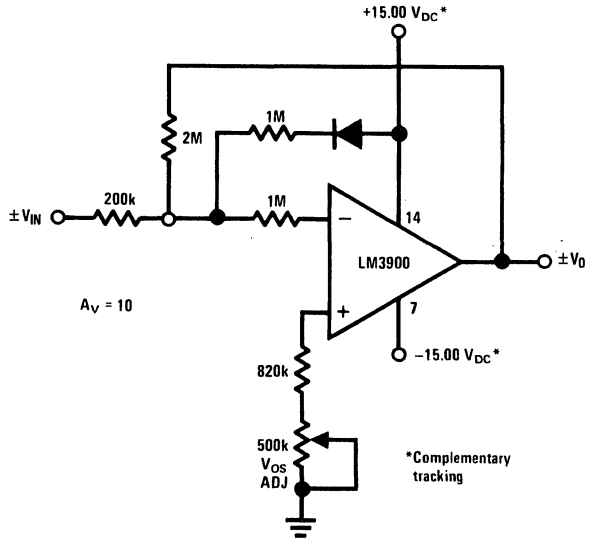


TL/H/7936–50

3

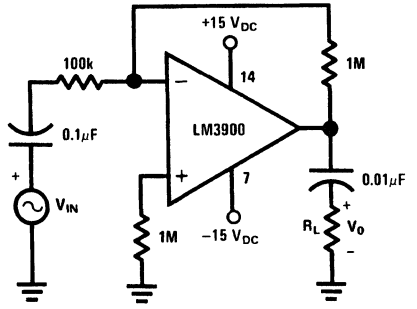
Split-Supply Applications ($V^+ = +15\ V_{DC}$ & $V^- = -15\ V_{DC}$)

Non-Inverting DC Gain



TL/H/7936–51

AC Amplifier



TL/H/7936–52

National Semiconductor

LM3080/LM3080A
Operational Transconductance Amplifier

General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

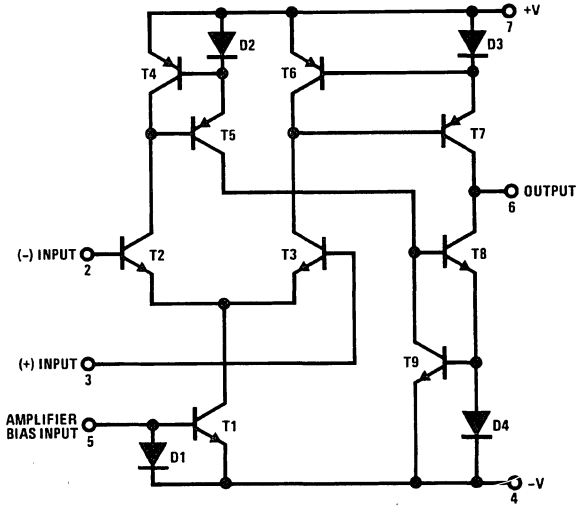
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080N and LM3080AN are guaranteed from 0°C to +70°C.

Features

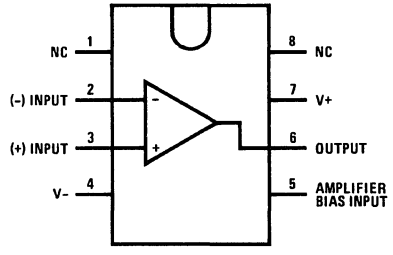
- Slew rate (unity gain compensated): 50 V/μs
- Fully adjustable gain: 0 to $g_m \bullet R_L$ limit
- Extended g_m linearity: 3 decades
- Flexible supply voltage range: ±2V to ±18V
- Adjustable power consumption

Schematic and Connection Diagrams



TL/H/7148–1

Dual-In-Line Package



TL/H/7148–2

Top View

Order Number LM3080AN or LM3080N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)	
LM3080	±18V
LM3080A	±22V
Power Dissipation	250 mW
Differential Input Voltage	±5V
Amplifier Bias Current (I_{ABC})	2 mA
DC Input Voltage	$+V_S$ to $-V_S$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM3080N or LM3080AN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 1)

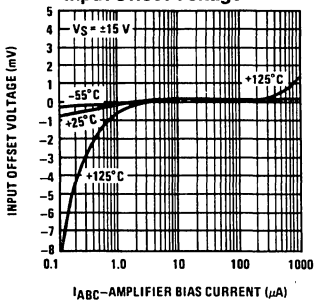
Parameter	Conditions	LM3080			LM3080A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.4	5		0.4	2	mV
	Over Specified Temperature Range			6			5	mV
	I_{ABC} = 5 μA		0.3			0.3	2	mV
Input Offset Voltage Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	7		1	8	μA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			μmho
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0	350	500	650	350	500	650	μA
	R_L = 0							
	Over Specified Temperature Range	300			300			μA
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Amplifier Supply Current			1.1			1.1		mA
Input Offset Voltage Sensitivity								
Positive	$\Delta V_{OFFSET}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OFFSET}/\Delta V-$		20	150		20	150	μV/V
Common Mode Rejection Ratio		80	110		80	110		dB
Common Mode Range		±12	±14		±12	±14		V
Input Resistance		10	26		10	26		kΩ
Magnitude of Leakage Current	I_{ABC} = 0		0.2	100		0.2	5	nA
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	5	nA
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs

Note 1: These specifications apply for V_S = ±15V and T_A = 25°C, amplifier bias current (I_{ABC}) = 500 μA, unless otherwise specified.

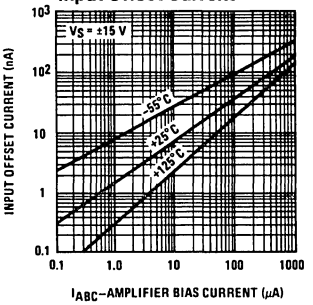
Note 2: Selection to supply voltage above ±22V, contact the factory.

Typical Performance Characteristics

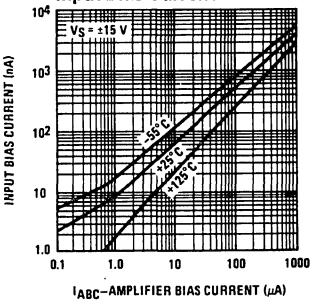
Input Offset Voltage



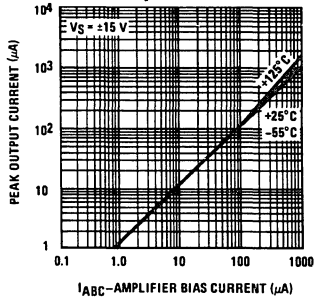
Input Offset Current



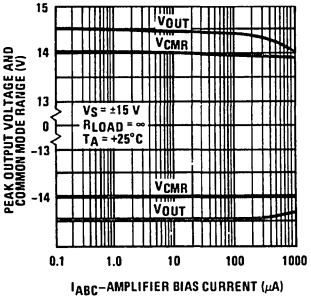
Input Bias Current



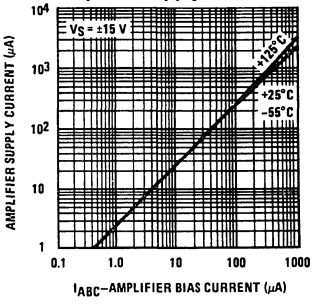
Peak Output Current



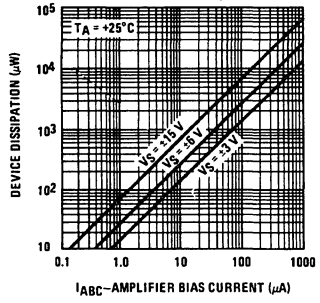
Peak Output Voltage and Common Mode Range



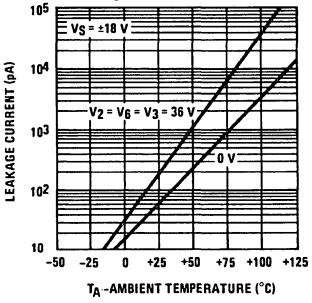
Amplifier Supply Current



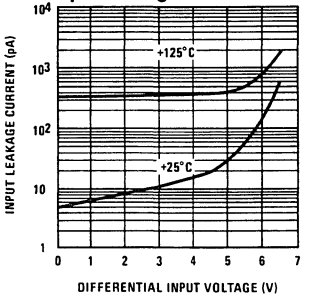
Total Power Dissipation



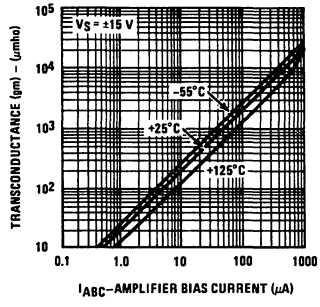
Leakage Current



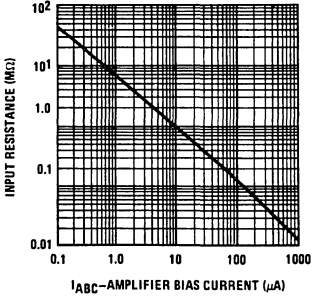
Input Leakage



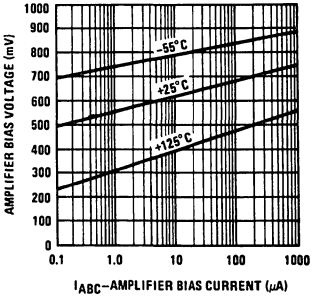
Transconductance



Input Resistance



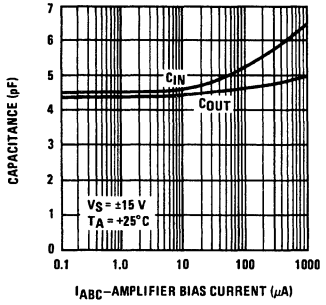
Amplifier Bias Voltage vs Amplifier Bias Current



TL/H/7148–3

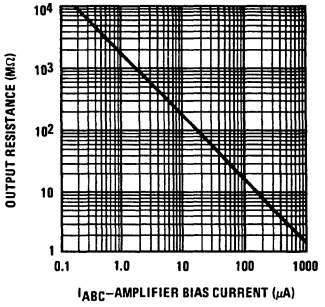
Typical Performance Characteristics (Continued)

Input and Output Capacitance



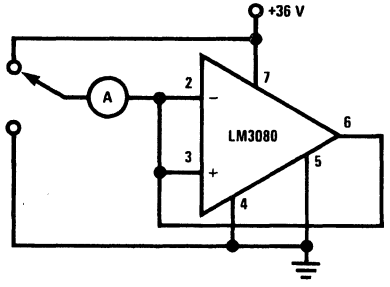
TL/H/7148–4

Output Resistance



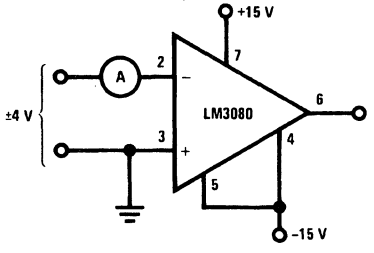
TL/H/7148–5

Leakage Current Test Circuit



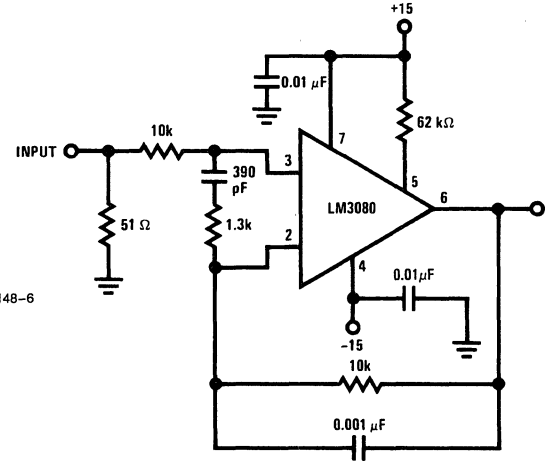
TL/H/7148–6

Differential Input Current Test Circuit



TL/H/7148–7

Unity Gain Follower



TL/H/7148–8

National Semiconductor

LM3303/LM3403/LM3503 Quad Operational Amplifiers

General Description

The LM3303, LM3403, and LM3503 are monolithic quad operational amplifiers consisting of four independent high gain, internally frequency compensated, operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

Features

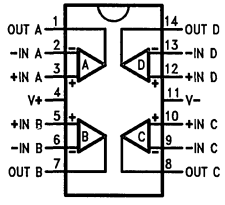
- Input common mode voltage range includes ground or negative supply
- Output voltage can swing to ground or negative supply
- Four internally compensated operational amplifiers in a single package
- Wide power supply range single supply of 3.0V to 36V dual supply of ±1.5V to ±18V
- Class AB output stage for minimal crossover distortion
- Short circuit protected outputs
- High open loop gain 200k
- LM741 operational amplifier type performance

Applications

- Filters
- Voltage controlled oscillators

Connection Diagram

14-Lead DIP and SO-14 Package



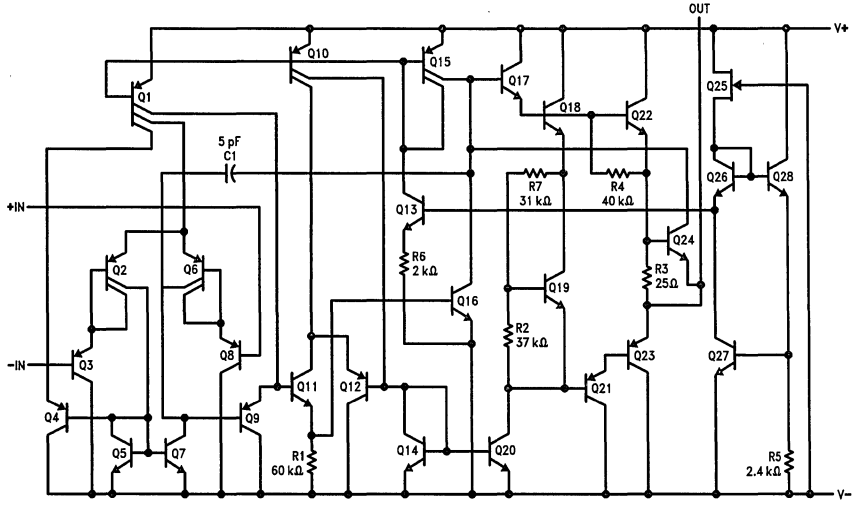
TL/H/10064-1

Top View

Order Information

Device Code	Package Code	Package Description
LM3303J	J14A	Ceramic DIP
LM3303N	N14A	Molded DIP
LM3403J	J14A	Ceramic DIP
LM3403N	N14A	Molded DIP
LM3403M	M14A	Molded Surface Mount
LM3503J	J14A	Ceramic DIP

Equivalent Circuit (¼ of Circuit)



TL/H/10064-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-14: −65°C to +150°C

Operating Temperature Range
- Military (LM3503): −55°C to +125°C
- Industrial (LM3303): −40°C to +85°C
- Commercial (LM3403): 0°C to +70°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-14 (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 14L-Ceramic DIP: 1.36W
- 14L-Molded DIP: 1.04W
- SO-14: 0.93W

Supply Voltage between V+ and V−: 36V

Differential Input Voltage (Note 3): ±30V

Input Voltage: (V−) − 0.3V to V+

ESD Tolerance: (To Be Determined)

LM3303 and LM3403 Electrical Characteristics

T_A = 25°C, V_{CC} = ±15V, unless otherwise specified

Symbol	Parameter		Conditions	LM3303			LM3403			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				2.0	8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				30	75		30	50	nA
I_{IB}	Input Bias Current				200	500		200	500	nA
Z_I	Input Impedance			0.3	1.0		0.3	1.0		MΩ
I_{CC}	Supply Current		V_O = 0V, R_L = ∞		2.8	7.0		2.8	7.0	mA
CMR	Common Mode Rejection		R_S ≤ 10 kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range			+12V to V−	+12.5V to V−		+13V to V−	+13.5V to V−		V
PSRR	Power Supply Rejection Ratio				30	150		30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier) (Note 4)			±10	±30	±45	±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain		V_O = ±10V, R_L ≥ 2.0 kΩ	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing		R_L = 10 kΩ	±12	12.5		±12	+13.5		V
			R_L = 2.0 kΩ	±10	12		±10	±13		
TR	Transient Response	Rise Time/ Fall Time	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		0.3			0.3		μs
		Overshoot	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		5.0			5.0		%
BW	Bandwidth		V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		1.0			1.0		MHz
SR	Slew Rate		V_I = −10V to +10V, A_V = 1.0		0.6			0.6		V/μs

LM3303 and LM3403 (Continued)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

The following specifications apply for $-40°C \leq T_A \leq +85°C$ for the LM3303, and $0°C \leq T_A \leq +70°C$ for the LM3403

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				10			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10			10		μV/°C
I_{IO}	Input Offset Current				250			200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50			50		pA/°C
I_{IB}	Input Bias Current				1000			800	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2.0\ k\Omega$	15			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$	±10			±10			V

LM3303 and LM3403 Electrical Characteristics $T_A = 25°C$, V+ = 5.0V, V− = GND, unless otherwise specified

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				75		30	50	nA
I_{IB}	Input Bias Current				500		200	500	nA
I_{CC}	Supply Current			2.5	7.0		2.5	7.0	mA
PSRR	Power Supply Rejection Ratio				150			150	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0\ k\Omega$	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing (Note 5)	$R_L = 10\ k\Omega$	3.3			3.3			V
		5.0V ≤ V+ ≤ 30V, $R_L = 10\ k\Omega$	(V+) −2.0			(V+) −2.0			
CS	Channel Separation	1.0 Hz ≤ f ≤ 20 kHz (Input Referenced)		−120			−120		dB

LM3503 Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter	Conditions	LM3503			Units
			Min	Typ	Max	
V_{IO}	Input Offset Voltage			2.0	5.0	mV
I_{IO}	Input Offset Current			30	50	nA
I_{IB}	Input Bias Current			200	500	nA
Z_I	Input Impedance		0.3	1.0		MΩ
I_{CC}	Supply Current	$V_O = 0V$, $R_L = \infty$		2.8	4.0	mA
CMR	Common Mode Rejection	$R_S \leq 10\ k\Omega$	70	90		dB

LM3503
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified (Continued)

Symbol	Parameter		Conditions	LM3503			Units
				Min	Typ	Max	
V_{IR}	Input Voltage Range			+13V to V−	+13.5V to V−		V
PSRR	Power Supply Rejection Ratio				30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier) (Note 4)			±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10V$, $R_L \geq 2.0\ k\Omega$	50	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10\ k\Omega$	±12	±13.5		V
			$R_L = 2.0\ k\Omega$	±10	±13		
TR	Transient Response	Rise Time	$V_O = 50\ mV$, $A_V = 1.0$, $R_L = 10\ k\Omega$		0.3		μs
		Overshoot	$V_O = 50\ mV$, $A_V = 1.0$, $R_L = 10\ k\Omega$		5.0		%
BW	Bandwidth		$V_O = 50\ mV$, $A_V = 1.0$, $R_L = 10\ k\Omega$		1.0		MHz
SR	Slew Rate		$V_I = -10V$ to $+10V$, $A_V = 1.0$		0.6		V/μs

LM3503
Electrical Characteristics $-55°C \leq T_A \leq +125°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter	Conditions	LM3503			Units
			Min	Typ	Max	
V_{IO}	Input Offset Voltage				6.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10		μV/°C
I_{IO}	Input Offset Current				200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50		pA/°C
I_{IB}	Input Bias Current				1200	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2.0\ k\Omega$	25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$	±10			V
The following specifications apply for $T_A = 25°C$, $V+ = +5.0V$, $V- = GND$						
V_{IO}	Input Offset Voltage			2.0	5.0	mV
I_{IO}	Input Offset Current			30	50	nA
I_{IB}	Input Bias Current			200	500	nA
I_{CC}	Supply Current			2.5	4.0	mA
PSRR	Power Supply Rejection Ratio				150	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0\ k\Omega$	20	200		V/mV
V_{OP}	Output Voltage Swing (Note 5)	$R_L = 10\ k\Omega$	3.3			V
		$5.0V \leq V+ \leq 30V$, $R_L = 10\ k\Omega$	(V+) −2.0			
CS	Channel Separation	1.0 Hz ≤ f ≤ 20 kHz (Input Referenced)		−120		dB

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

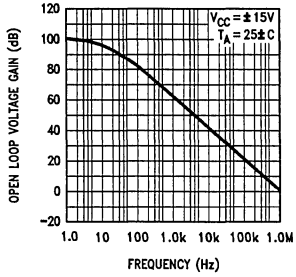
Note 3: For supply voltage less than 30V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Not to exceed maximum package power dissipation.

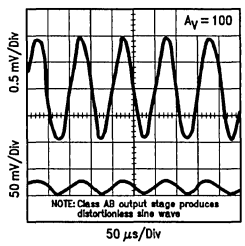
Note 5: Output will swing to ground.

Typical Performance Characteristics

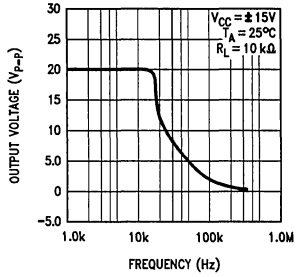
Open Loop Frequency Response



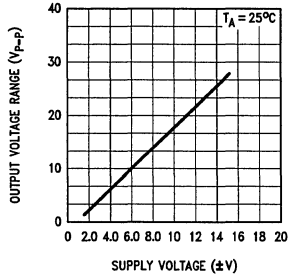
Sine Wave Response



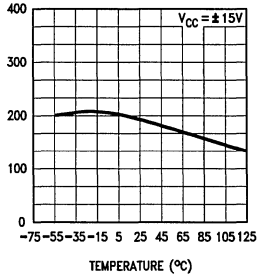
Output Voltage vs Frequency



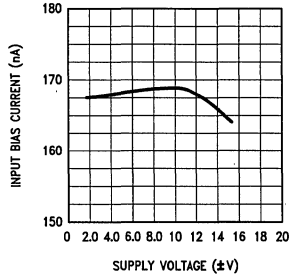
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage

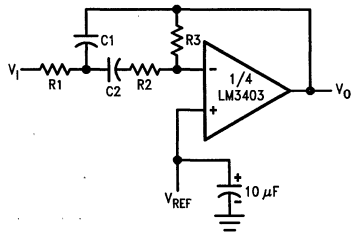


TL/H/10064–3

3

Typical Applications

Multiple Feedback Bandpass Filter



TL/H/10064–4

f_o = center frequency
BW = Bandwidth
R in kΩ
C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

$$R1 = R2 = 1\ R3 = 9Q^2 - 1$$ } Using scaling factors in these expressions.

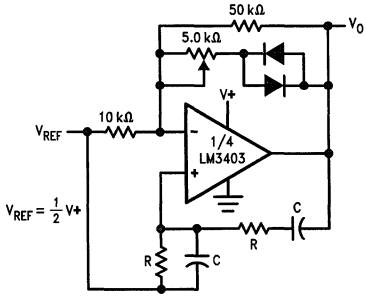
If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: Q = 5, f_o = 1 kHz
Let R1 = R2 = 10 kΩ
then R3 = $9(5)^2 - 10$
R3 = 215 kΩ

$$C = \frac{5}{3} = 1.6\ nF$$

Wein Bridge Oscillator

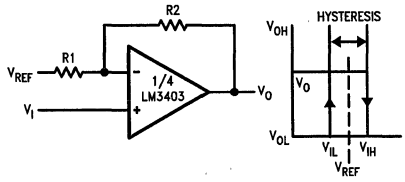


TL/H/10064–5

$$f_o = \frac{1}{2\pi RC} \text{ for } f_o = 1\ kHz$$

R = 16 kΩ
C = 0.01 μF

Comparator with Hysteresis



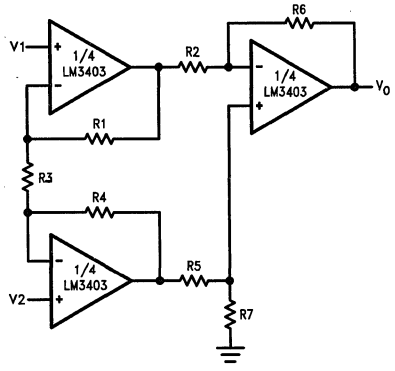
TL/H/10064–6

$$V_{IL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

High Impedance Differential Amplifier



TL/H/10064–7

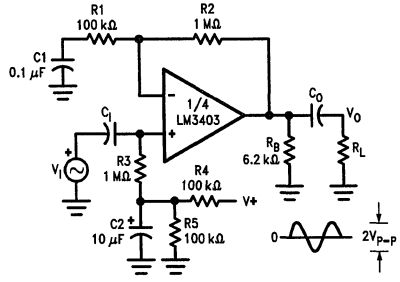
$$V_{OUT} = C(1 + a + b)(V2 - V1)$$

$$\frac{R2}{R5} \equiv \frac{R6}{R7} \text{ for best CMRR}$$

R1 = R4
R2 = R5

$$\text{Gain} = \frac{R6}{R5}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$$

AC Coupled Non-Inverting Amplifier



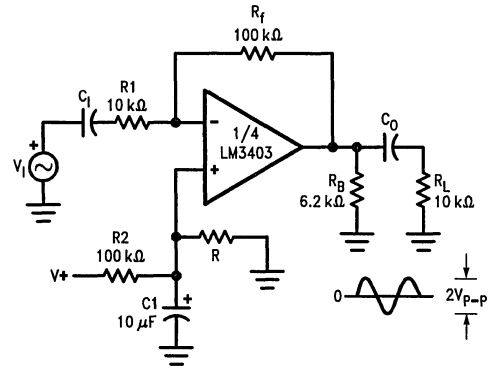
TL/H/10064–9

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (as shown)

Typical Applications (Continued)

AC Coupled Inverting Amplifier

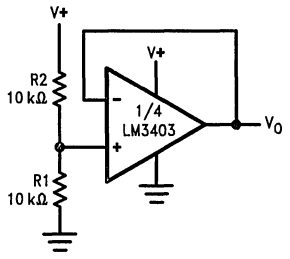


TL/H/10064–8

$A_V = \frac{Rf}{R1}$

A_V = 10 (as shown)

Voltage Reference

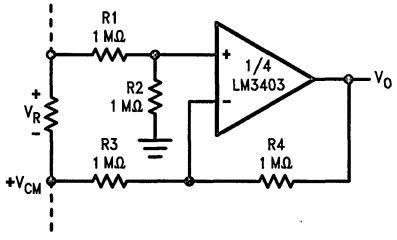


TL/H/10064–10

$V_O = \frac{R1}{R1 + R2}\left(= \frac{V+}{2} \text{ as shown}\right)$

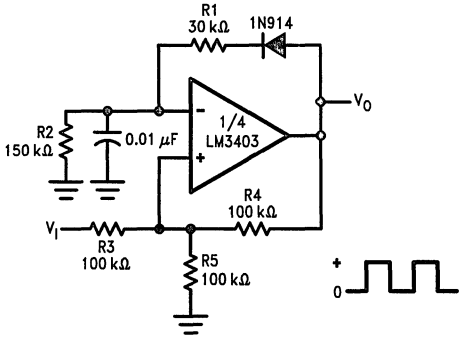
$V_O = \frac{1}{2}V+$

Ground Referencing a Differential Input Signal



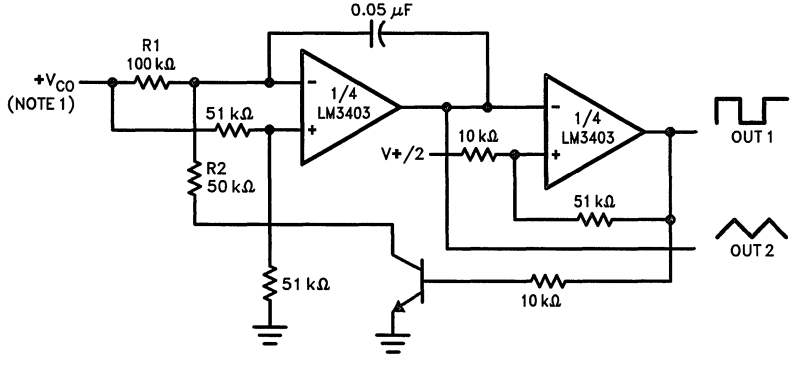
TL/H/10064–11

Pulse Generator



TL/H/10064–14

Voltage Controlled Oscillator

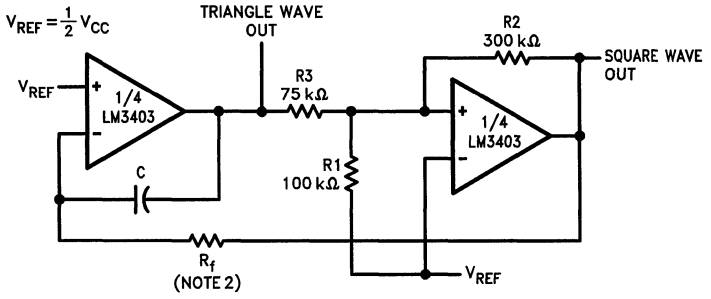


TL/H/10064–12

Note 1: Wide Control Voltage Range:
0V ≤ V_{CO} ≤ 2 (V ±1.5V)

Typical Applications (Continued)

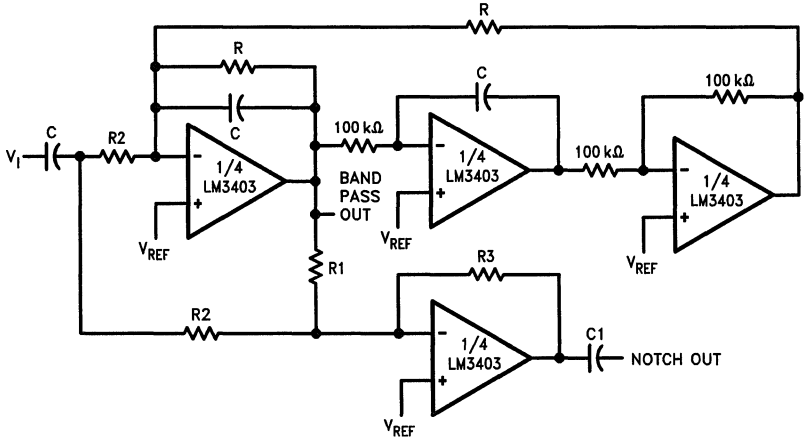
Function Generator



TL/H/10064–13

Note 2: $f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

Bi-Quad Filter



TL/H/10064–15

$Q = \frac{BW}{f_o}$

where:

T_{BP} = Center Frequency Gain
T_N = Bandpass Notch Gain

$f_o = \frac{1}{2\pi RC}$, $V_{REF} = \frac{1}{2} V_{CC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$
$C1 = 10\ C$

Example:

f_o = 1000 Hz
BW = 100 Hz
T_{BP} = 1
T_N = 1
R = 160 kΩ
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
C = 0.001 μF

National Semiconductor

LM4136
Quad Operational Amplifier

General Description

The LM4136 monolithic quad operational amplifier consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the LM4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

Features

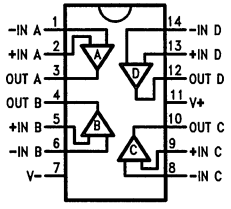
- Unity gain bandwidth—3.0 MHz
- Continuous short circuit protection
- No frequency compensation required
- No latch up
- Large common mode and differential voltage range
- LM741 operational amplifier type performance
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Applications

- Audio preamplifiers
- Signal conditioning

Connection Diagram

14-Lead DIP and SO-14 Package



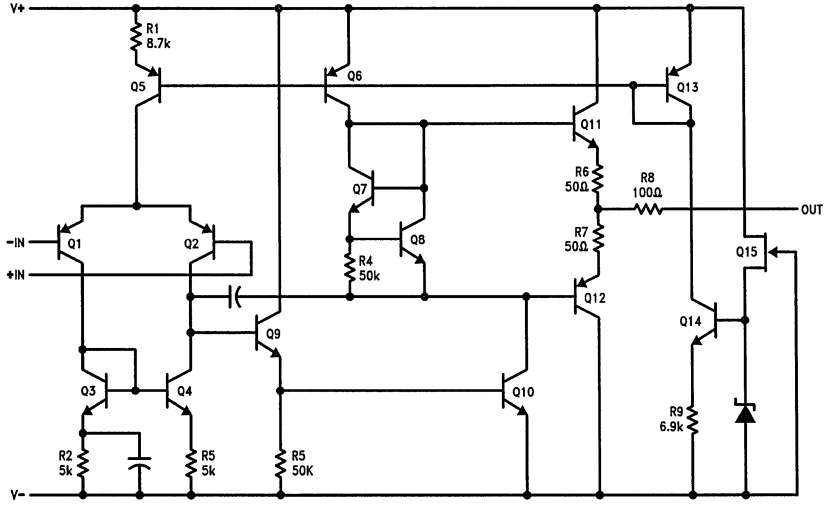
TL/H/10065–1

Top View

Ordering Information

Device Code	NS Package Number	Package Description
LM4136CJ	J14A	Ceramic DIP
LM4136CN	N14A	Molded DIP
LM4136CM	M14A	Molded Surface Mount

Equivalent Circuit (1/4 of Circuit)



TL/H/10065–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Molded DIP and SO-14 (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Notes 1, 2)	
14L-Ceramic DIP	1.36W
14L-Molded DIP	1.04W
SO-14	0.93W
Supply Voltage	±18V
Differential Input Voltage (Note 3)	±30V
Input Voltage (Note 1)	±15V
Output Short Circuit Duration (Note 4)	Indefinite
ESD Tolerance	1000V

LM4136
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \le 10\ k\Omega$		0.5	6.0	mV
I_{IO}	Input Offset Current				5.0	200	nA
I_{IB}	Input Bias Current				40	500	nA
Z_I	Input Impedance			0.3	5.0		MΩ
P_C	Power Consumption				210	340	mW
CMR	Common Mode Rejection		$R_S \le 10\ k\Omega$	70	90		dB
V_{IR}	Input Voltage Range			±12	±14		V
PSRR	Power Supply Rejection Ratio		$R_S \le 10\ k\Omega$		30	150	μV/V
A_{VS}	Large Signal Voltage Gain		$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	20	300		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10\ k\Omega$	±12	±14		V
			$R_L = 2.0\ k\Omega$	±10	±13		
TR	Transient Response	Rise Time	$V_I = 20$ mV, $R_L = 2.0\ k\Omega$, $C_L = 100$ pF, $A_V = 1.0$		0.13		μs
		Overshoot			5.0		%
BW	Bandwidth		$A_V = 1.0$		3.0		MHz
SR	Slew Rate		$R_L = 2.0\ k\Omega$, $A_V = 1.0$		1.0		V/μs
CS	Channel Separation		f = 10 kHz, $R_S = 1.0\ k\Omega$ Open Loop		105		dB
			f = 10 kHz, $R_S = 1.0\ k\Omega$ $A_V = 100$		105		

The following specifications apply over the range of $0°C \le T_A \le +70°C$

V_{IO}	Input Offset Voltage	$R_S \le 10\ k\Omega$			7.5	mV
I_{IO}	Input Offset Current				300	nA
I_{IB}	Input Bias Current				800	nA
P_C	Power Consumption	$T_A = T_{A\ Max}$		180	300	mW
		$T_A = T_{A\ Min}$		240	400	
A_{VS}	Large Signal Voltage Gain	$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$, $V_{CC} = \pm 15V$	±10			V

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.

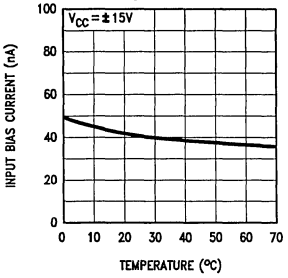
Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Note 3: For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

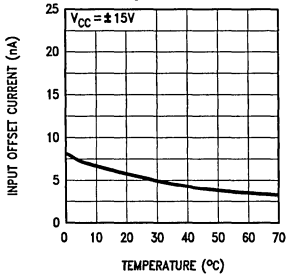
Note 4: Short circuit may be to ground, one amplifier only.

Typical Performance Characteristics

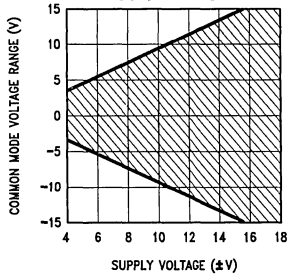
Input Bias Current vs Temperature



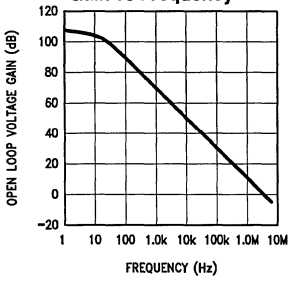
Input Offset Current vs Temperature



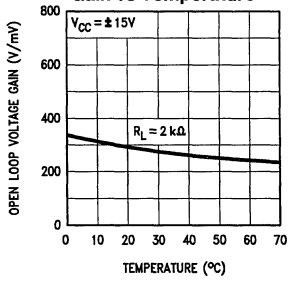
Common Mode Range vs Supply Voltage



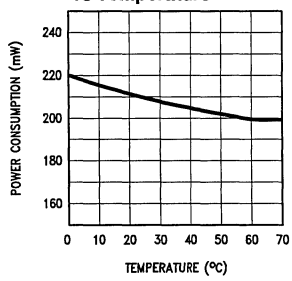
Open Loop Voltage Gain vs Frequency



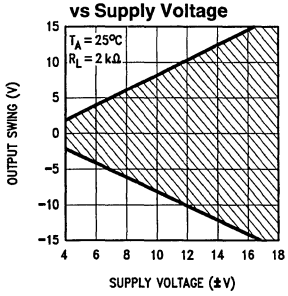
Open Loop Voltage Gain vs Temperature



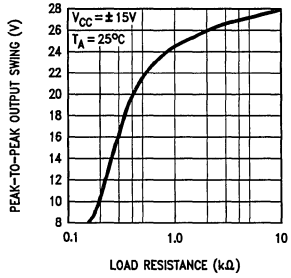
Power Consumption vs Temperature



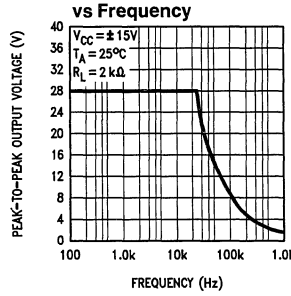
Typical Output Voltage vs Supply Voltage



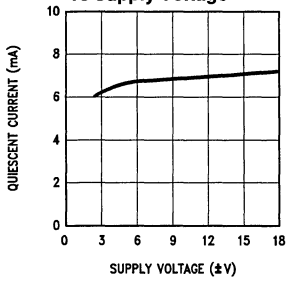
Output Voltage Swing vs Load Resistance



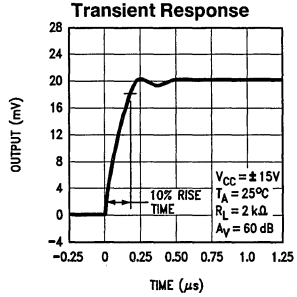
Output Voltage Swing vs Frequency



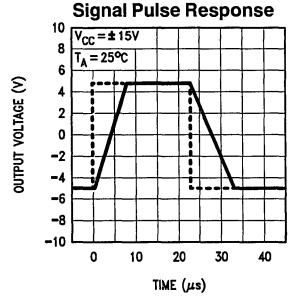
Quiescent Current vs Supply Voltage



Transient Response



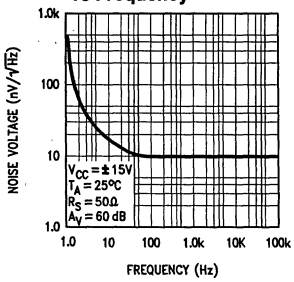
Voltage Follower Large Signal Pulse Response



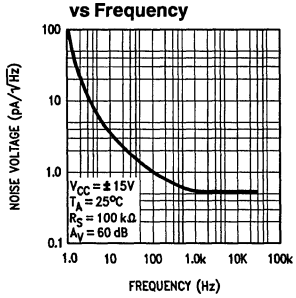
TL/H/10065–3

Typical Performance Characteristics (Continued)

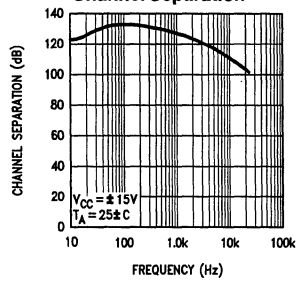
Input Noise Voltage vs Frequency



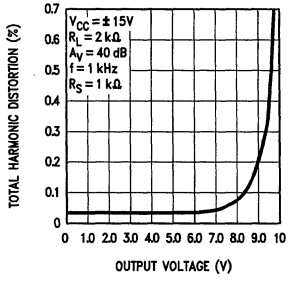
Input Noise Current vs Frequency



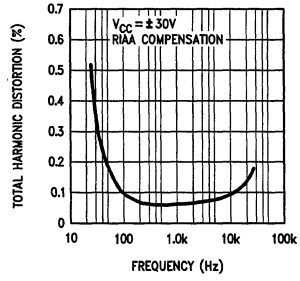
Channel Separation



Distortion vs Output Voltage (f = 1 kHz)



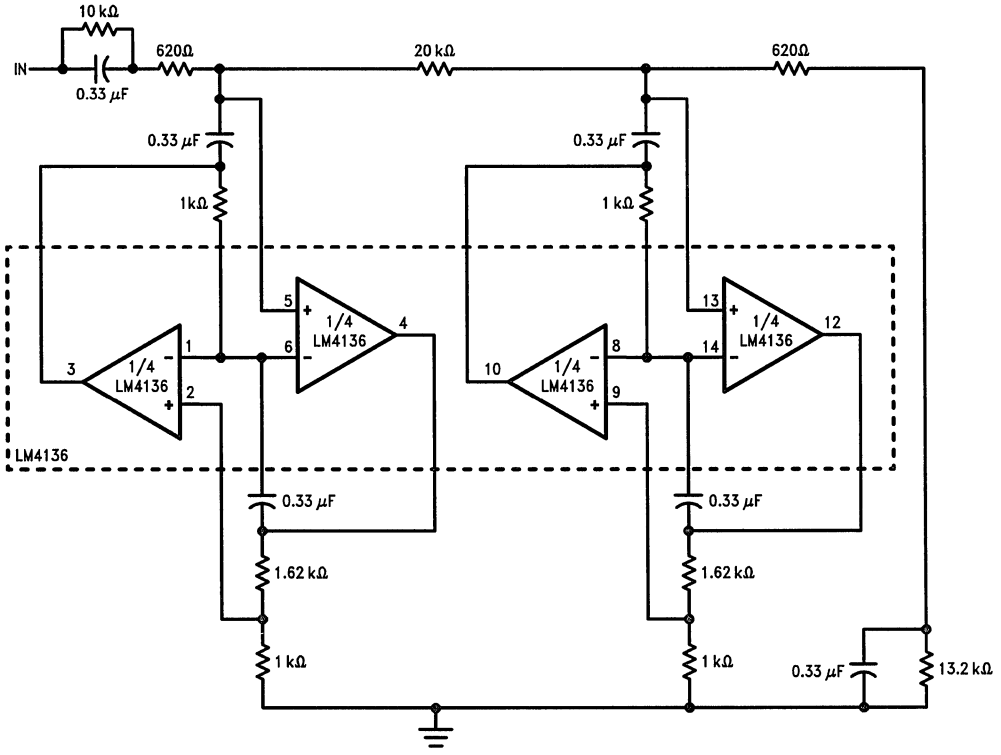
Distortion vs Frequency (V_O = 1 V_{rms})



TL/H/10065–4

Typical Applications

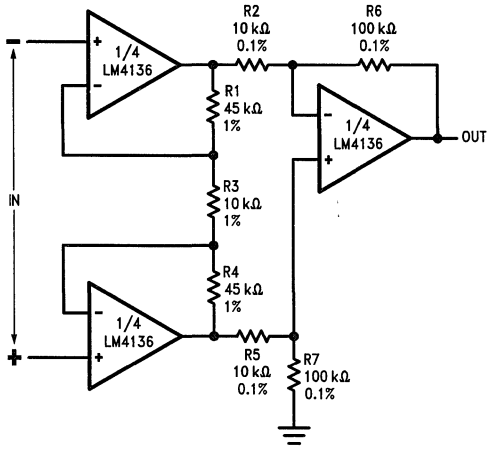
400 Hz Lowpass Butterworth Active Filter



TL/H/10065–5

Typical Applications (Continued)

Differential Input Instrumentation Amplifier with High Common Mode Rejection

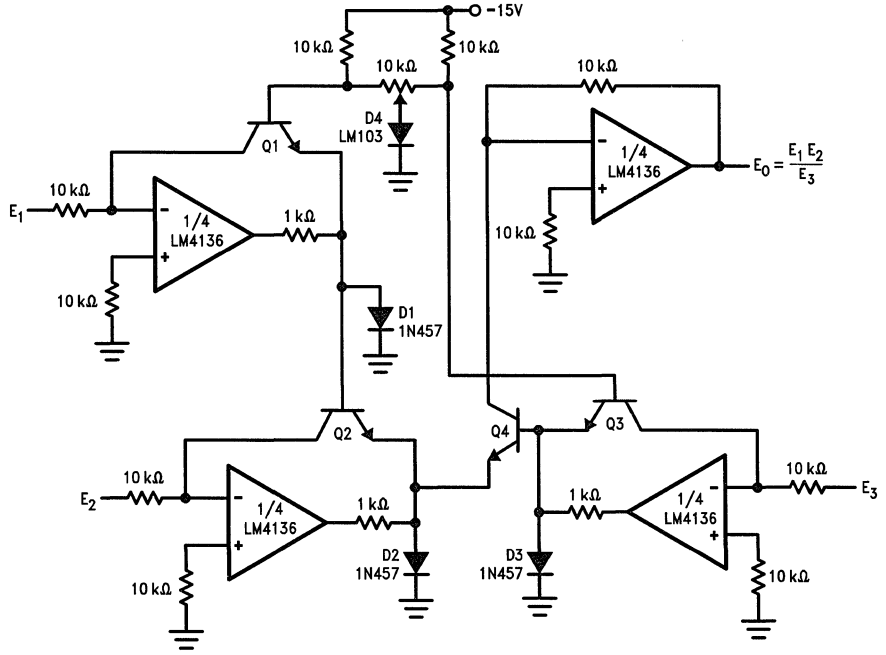


$$A_V = \frac{R6}{R2}\left(1 + \frac{2\,R1}{R3}\right)$$

Matching determines CMRR:
R1 = R4
R2 = R5
R6 = R7

TL/H/10065–6

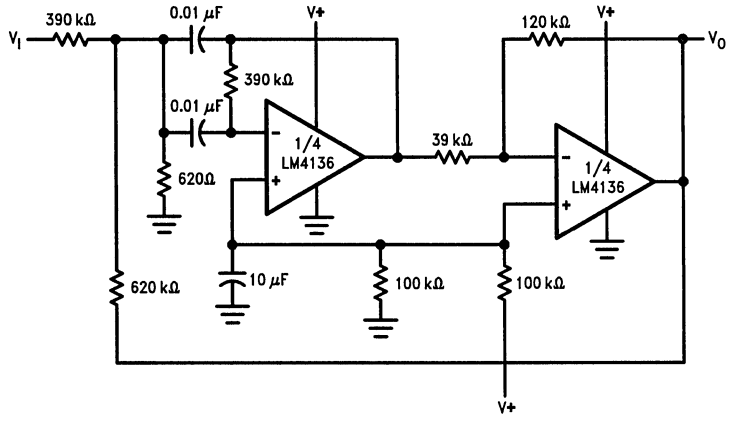
Analog Multiplier/Divider



TL/H/10065–7

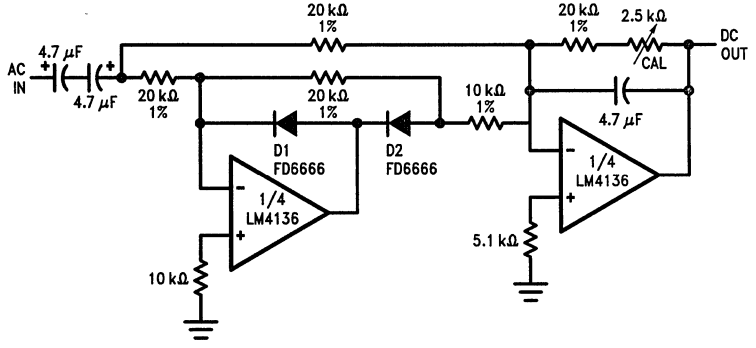
Typical Applications (Continued)

1 kHz Bandpass Active Filter



TL/H/10065–8

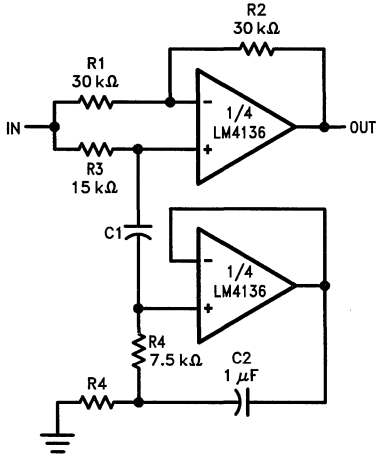
Full-Wave Rectifier and Averaging Filter



TL/H/10065–9

Typical Applications (Continued)

Notch Filter Using the LM4136 as a Gyrator

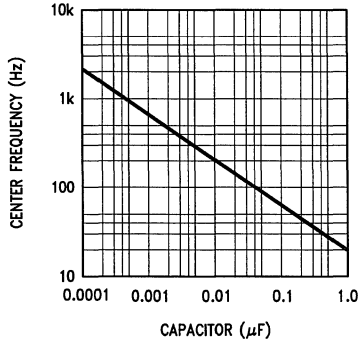


TL/H/10065–10

Trim R, Such That

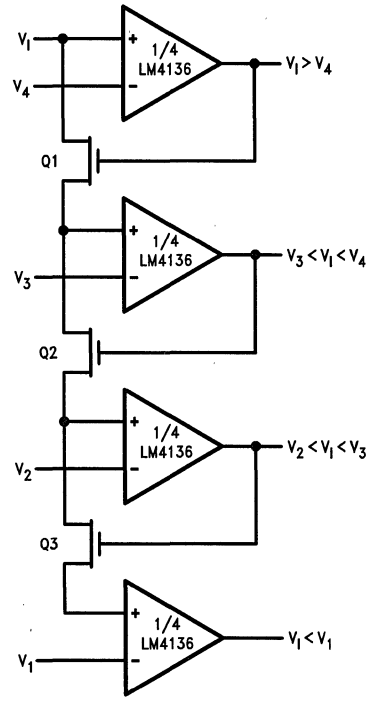
$$\frac{R1}{R2} = \frac{R3}{2\,R4}$$

Notch Frequency vs Capacitor



TL/H/10065–12

Multiple Aperture Window Discriminator



TL/H/10065–11

National Semiconductor

LM4250/LM4250C Programmable Operational Amplifier

General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

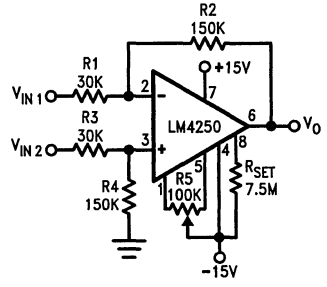
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Typical Applications

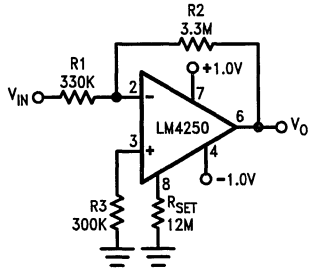
X5 Difference Amplifier



Quiescent P_D = 0.6 mW

TL/H/9300-3

500 Nano-Watt X10 Amplifier

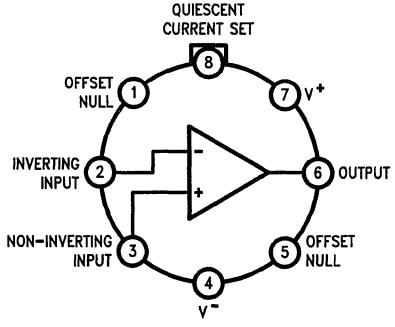


TL/H/9300-4

Quiescent P_D = 500 nW

Connection Diagrams

Metal Can Package

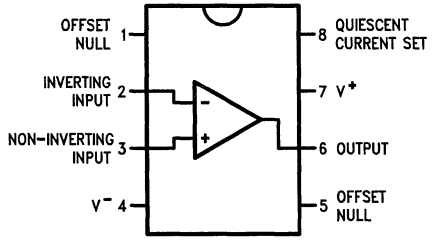


TL/H/9300-2

Top View

Order Number LM4250H or LM4250CH
See NS Package Number H08C

Dual-In-Line Package



TL/H/9300-5

Top View

Order Number LM4250J, LM4250CJ, LM4250CN or LM4250M
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 2)

	LM4250	LM4250C
Supply Voltage	±18V	±18V
Operating Temp. Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
I_{SET} Current	150 nA	150 nA
Output Short Circuit Duration	Continuous	Continuous
T_{JMAX}		
H-Package	150°C	100°C
N-Package		100°C
J-Package	150°C	100°C
M-Package		100°C
Power Dissipation at $T_A = 25°C$		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	1200 mW
N-Package		500 mW
J-Package	1000 mW	600 mW
M-Package		350 mW
Thermal Resistance (Typical) θ_{JA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	65°C/W	65°C/W
N-Package		130°C/W
J-Package	108°C/W	108°C/W
M-Package		190°C/W
(Typical) θ_{JC}		
H-Package	21°C/W	21°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 800V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Refer to RETS4250X for military specifications.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V^-

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Electrical Characteristics LM4250 ($0°C \le T_A \le +70°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	40k		50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		5 nA 3 nA		10 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	30k		30k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	100k		100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		25 nA 3 nA		25 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

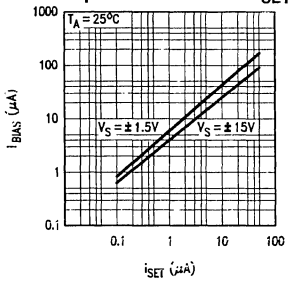
Electrical Characteristics LM4250C ($-55°C \le T_A \le +125°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	25k		25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S \le 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	25k		25k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

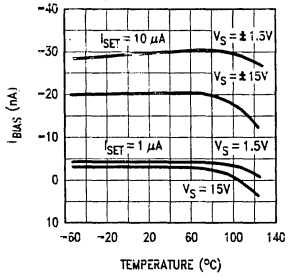
Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	60k		60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \le 100\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Typical Performance Characteristics

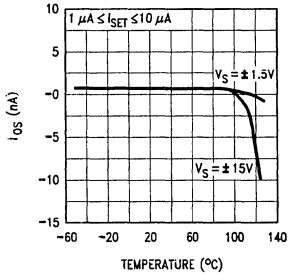
Input Bias Current vs i_{SET}



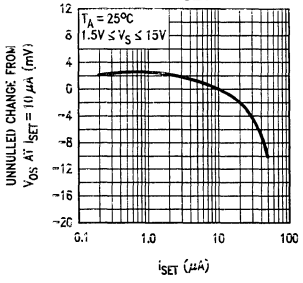
Input Bias Current vs Temperature



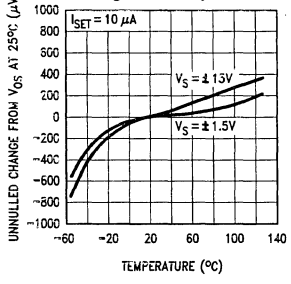
Input Offset Current vs Temperature



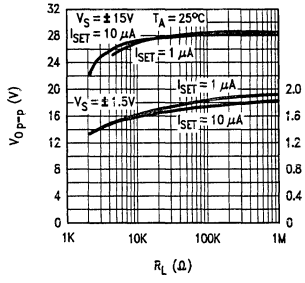
Unnulled Input Offset Voltage Change vs i_{SET}



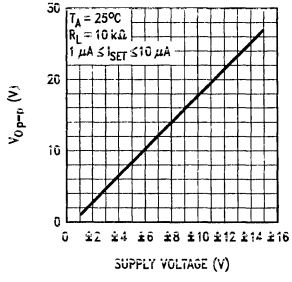
Unnulled Input Offset Voltage Change vs Temperature



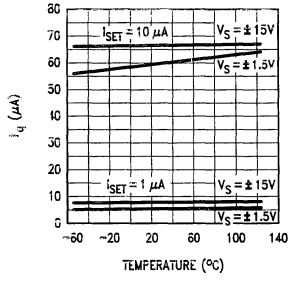
Peak to Peak Output Voltage Swing vs Load Resistance



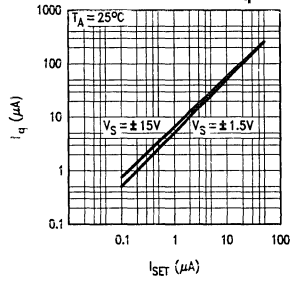
Peak to Peak Output Voltage Swing vs Supply Voltage



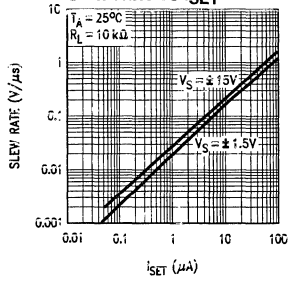
Quiescent Current (I_Q) vs Temperature



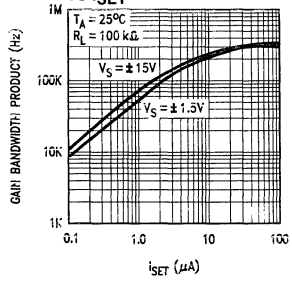
Quiescent Current (I_Q) vs i_{SET}



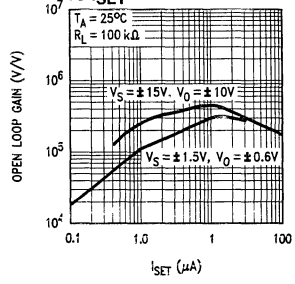
Slew Rate vs i_{SET}



Gain Bandwidth Product vs i_{SET}



Open Loop Voltage Gain vs i_{SET}



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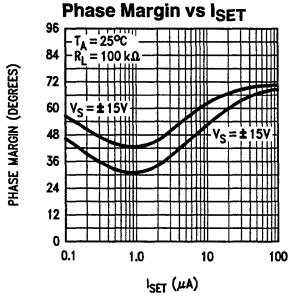
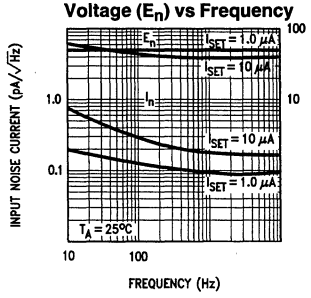
3

Typical Performance Characteristics (Continued)

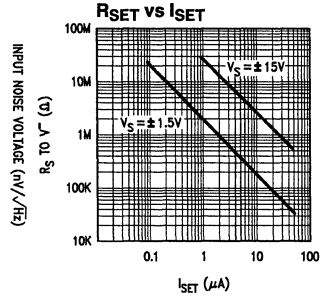
Phase Margin vs I_{SET}



Input Noise Current (I_n) and Voltage (E_n) vs Frequency



R_{SET} vs I_{SET}



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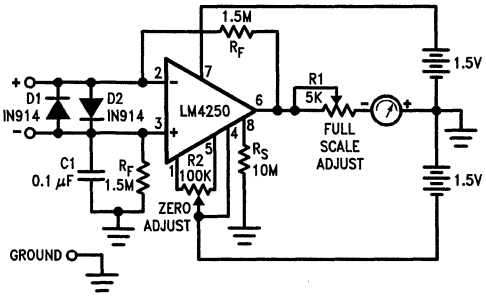
Typical Applications (Continued)

Floating Input Meter Amplifier
100 nA Full Scale



Quiescent P_D = 1.8 μW

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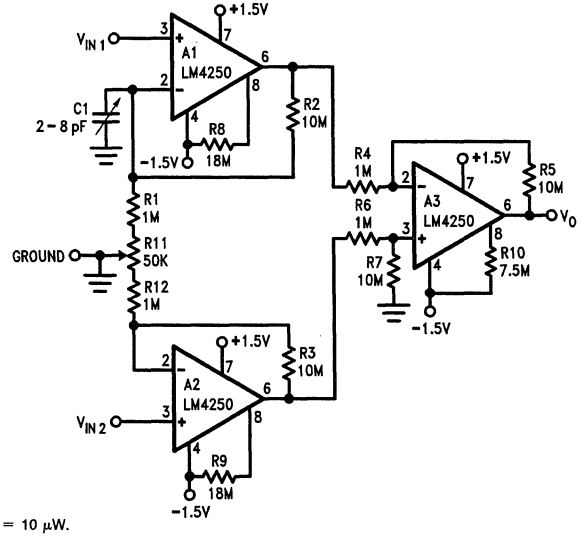
*Meter movement (0–100 μA, 2 kΩ) marked for 0–100 nA full scale.

X100 Instrumentation Amplifier 10 μW



Note 1: Quiescent P_D = 10 μW.

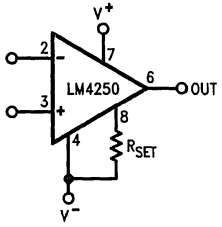
TL/H/9300–9

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors.

Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

Typical Applications (Continued)

R_{SET} Connected to V^-



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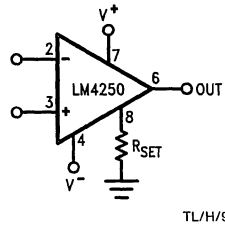
R_{SET} Connected to Ground



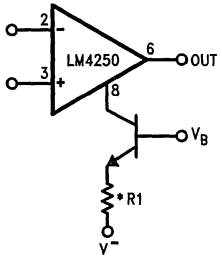
TL/H/9300–11

I_{SET} Equations:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$ where R_{SET} is connected to V^-

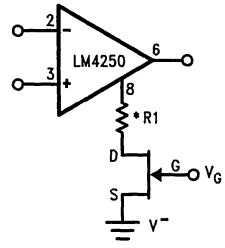
$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$ where R_{SET} is connected to ground.

Transistor Current Sourcing Biasing



*R1 limits I_{SET} maximum TL/H/9300–12

FET Current Sourcing Biasing



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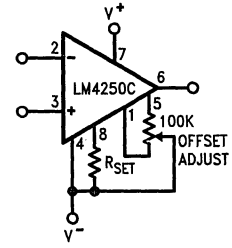
Offset Null Circuit



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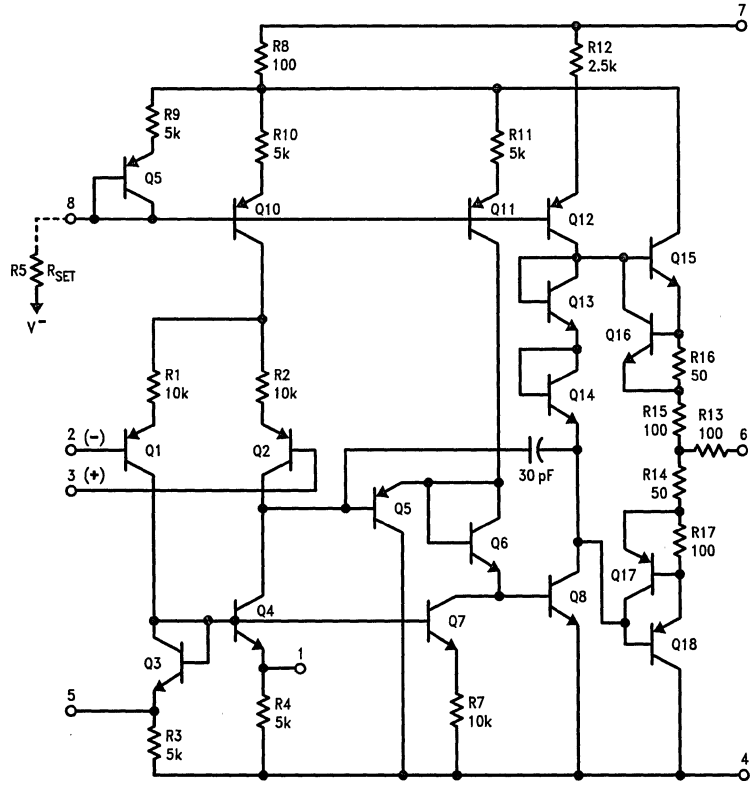
Schematic Diagram



TL/H/9300–1

National Semiconductor

LM6118/LM6218A/LM6218
Fast Settling Dual Operational Amplifier

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

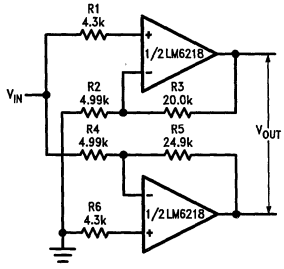
Features

	Typical
■ Low offset voltage	0.2 mV
■ 0.01% settling time	400 ns
■ Slew rate $A_V = -1$	140 V/μs
■ Slew rate $A_V = +1$	75 V/μs
■ Gain bandwidth	17 MHz
■ Total supply current	5.5 mA
■ Output drives 50Ω load (±1V)	
■ Well-behaved, easy to use	

Applications

- D/A converters
- Fast integrators
- Active filters

Typical Applications

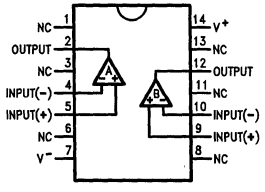


TL/H/10254–1

Single ended input to differential output
A_V = 10, BW = 3.2 MHz
40 V_{p-p} Response = 1.4 MHz
V_S = ±15V

Wide-Band, Fast-Settling 40 V_{p-p} Amplifier

Small Outline Package (WM)



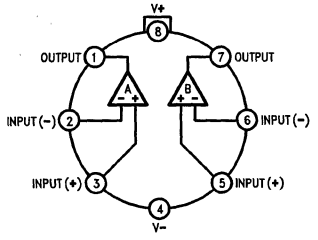
TL/H/10254–3

Top View

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

Connection Diagrams and Order Information

Metal Can Package (H)



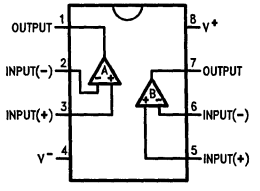
TL/H/10254–2

Top View

Note: Pin 4 connected to case

Order Number LM6118H or LM6218AH
See NS Package Number H08A

Dual-In-Line Package (J or N)



TL/H/10254–4

Top View

Order Number LM6118J, LM6218AJ, LM6218AN or LM6218N
See NS Package Number J08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	±2 kV
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	−55°C to +125°C
LM6218A	−40°C to +85°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25°C$, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Note 6)	LM6218A Limits (Note 7)	LM6218 Limits (Note 7)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	0.3	1.5 **2.5**	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	20	50 **100**	50 **100**	100 **200**	nA (max)
Input Bias Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	200	350 **950**	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \le V^+ \le 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \le V^- \le -5V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 17V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 **100**	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ (±20 mA)	200	50 **30**	50 **30**	40 **25**	V/mV (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	80	80	80	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 **50**	100 **50**	100 **50**	V/μs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 **30**	50 **30**	50 **30**	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_V = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is ($V^+ - 1V$) to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

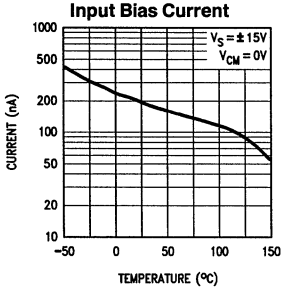
Note 5: Devices must be derated using a thermal resistance of 150°C/W junction to ambient for the H package, 90°C/W for the N, J and WM packages. If a heat sink is used on the H package, use a thermal resistance of 45°C/W junction to case.

Note 6: All limits are 100% production tested at 25°C and at temperature extremes. All limits are used to calculate AOQL, (Average Outgoing Quality Level).

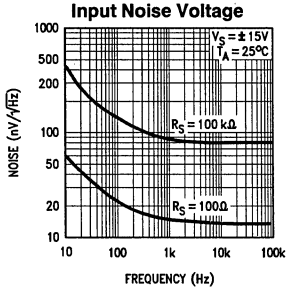
Note 7: 25°C limits are 100% production tested. Temperature extreme limits are guaranteed via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL.

Typical Performance Characteristics

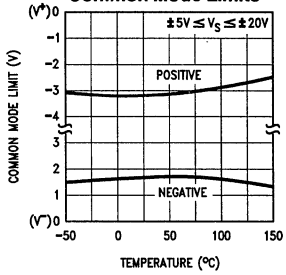
Input Bias Current



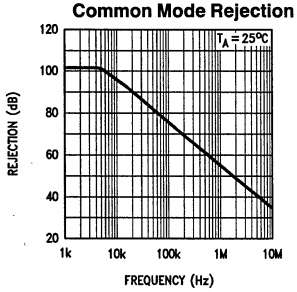
Input Noise Voltage



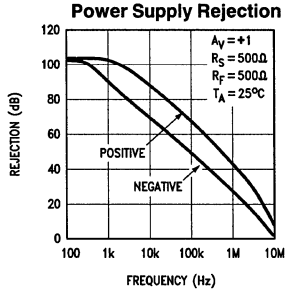
Common Mode Limits



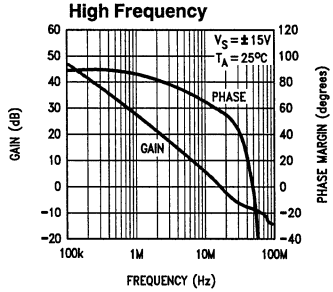
Common Mode Rejection



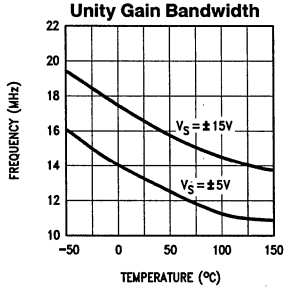
Power Supply Rejection



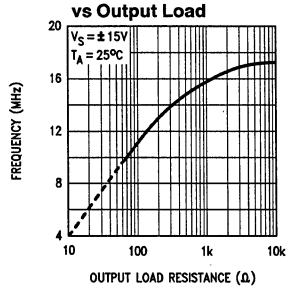
Frequency Response High Frequency



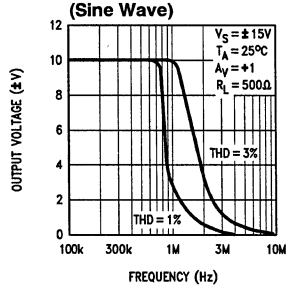
Unity Gain Bandwidth



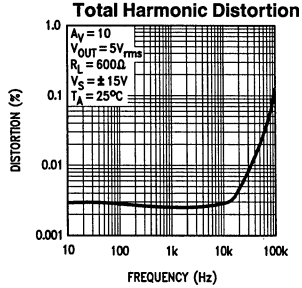
Unity Gain Bandwidth vs Output Load



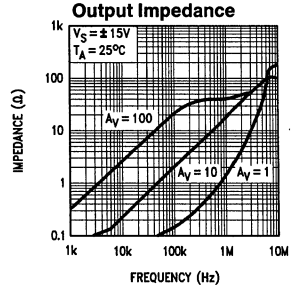
Large Signal Response (Sine Wave)



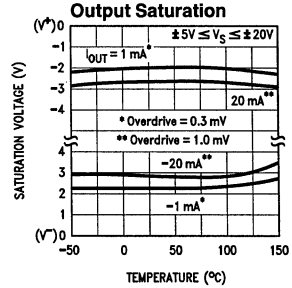
Total Harmonic Distortion



Output Impedance



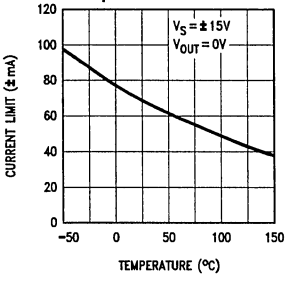
Output Saturation



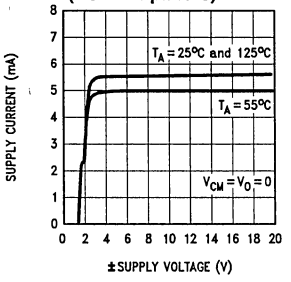
TL/H/10254–5

Typical Performance Characteristics (Continued)

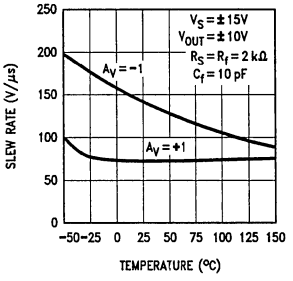
Output Current Limit



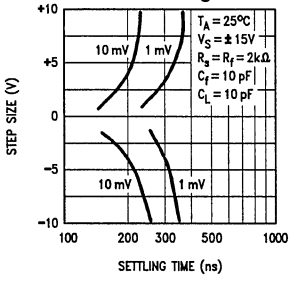
Supply Current (Both Amplifiers)



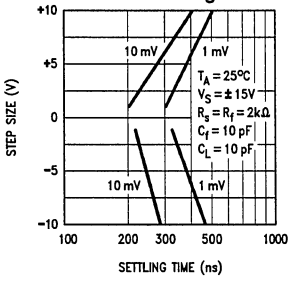
Slew Rate



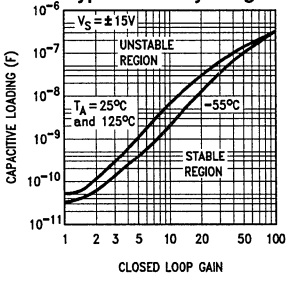
Inverter Settling Time



Follower Settling Time

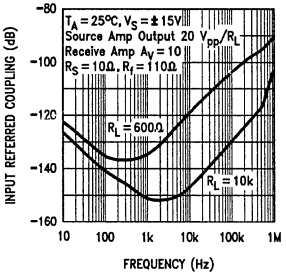


Typical Stability Range



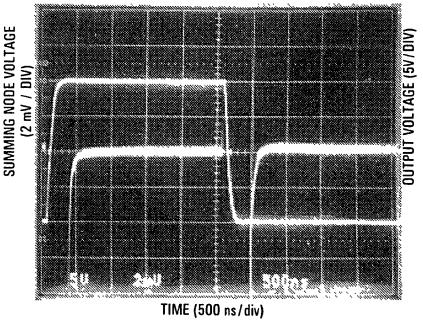
TL/H/10254–6

Amplifier to Amplifier Coupling



TL/H/10254–23

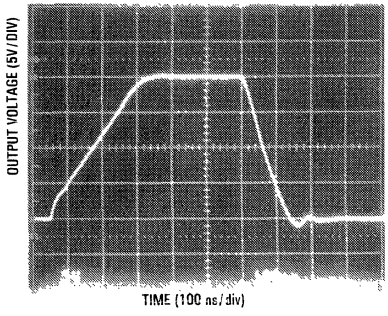
Settling Time, Vs = ±15V



TL/H/10254–7

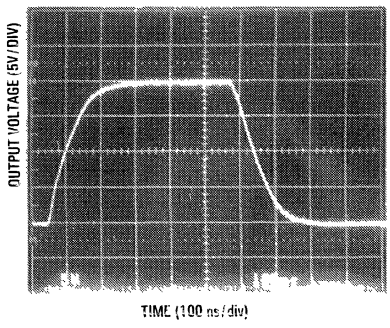
Typical Performance Characteristics (Continued)

Step Response, Av = +1, Vs = ±15V



TL/H/10254–8

Step Response, Av = −1, Vs = ±15V



TL/H/10254–9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 μF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an H package with a heat sink or a N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

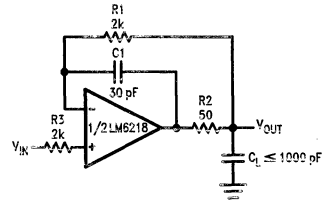
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

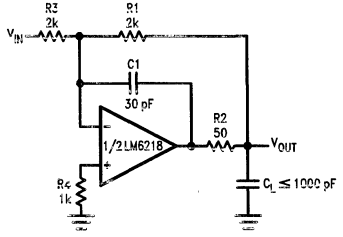
Voltage Follower



TL/H/10254–10

For C_L = 1000 pF, Small signal BW = 5 MHz
20 V_{p-p} BW = 500 kHz

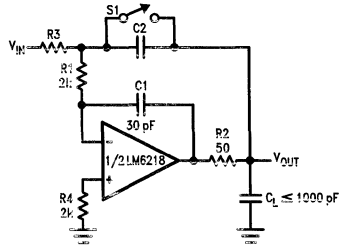
Inverter



TL/H/10254–11

Settling time to 0.01%, 10V Step
For C_L = 1000 pF, settling time ≈ 1500 ns
For C_L = 300 pF, settling time ≈ 500 ns

Integrator



TL/H/10254–12

Application Information (Continued)

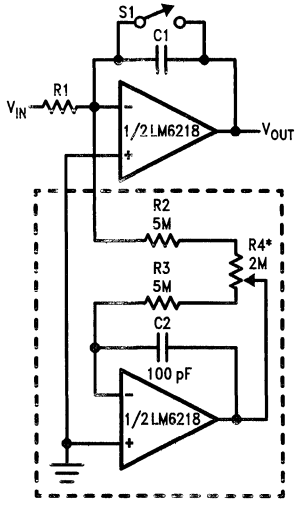
Examples of unity gain connections for a voltage follower, inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

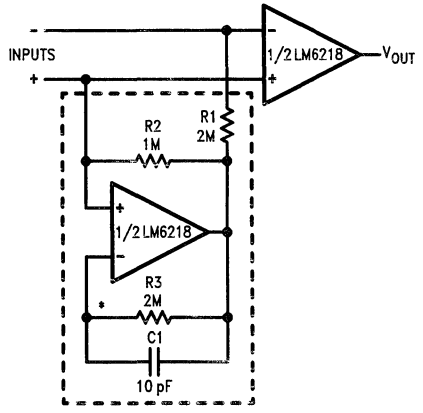
Bias Current Compensation



*adjust for zero integrator drift

TL/H/10254–13

(a) Inverting Input Bias Compensation for Integrator Application

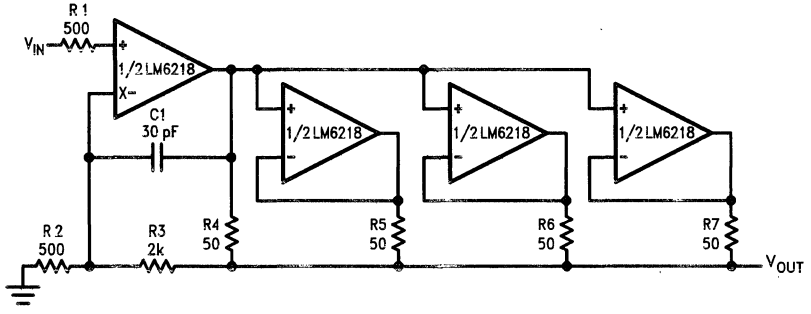


TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer

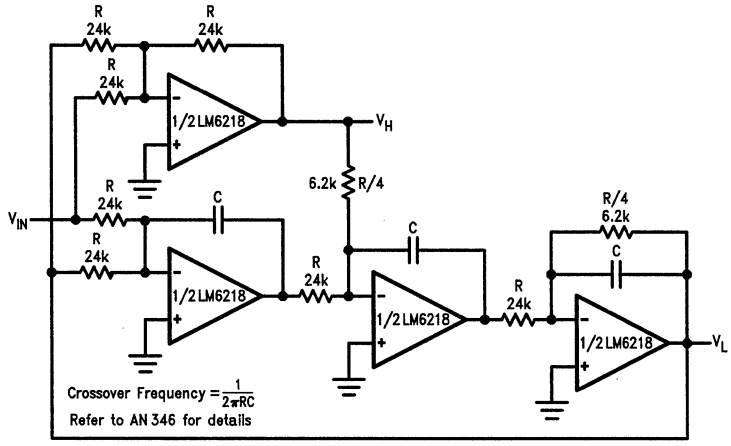


TL/H/10254–15

A_V = +5, $I_{OUT} \leq$ 80 mA
V_S = ±15V, $C_L \leq$ 0.01 μF
Large and small signal B.W. = 1.3 MHz (THD = 3%)

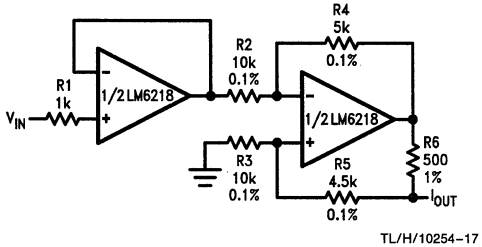
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope



TL/H/10254–16

Bilateral Current Source



TL/H/10254–17

$V_S = \pm 15V$, $-10 \leq V_{IN} \leq 10V$

$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\,R6} = \frac{1\,mA}{1V}$

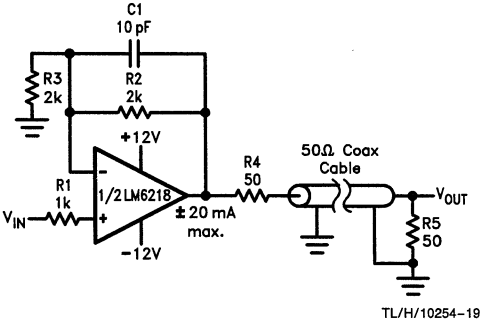
Output dynamic range = 10V − R6 $|I_{OUT}|$

R_L = 500Ω, small signal BW = 6 MHz

Large signal response = 800 kHz

C_{out} equiv. = $\frac{R2 + R4}{2\pi\, f_O\, R2\, R6}$ = 32 pF (f_O = 15 MHz)

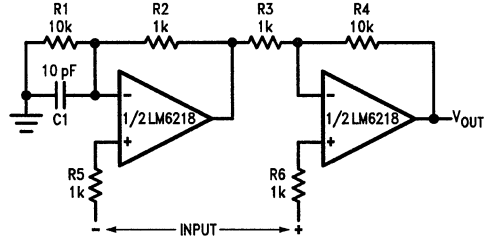
Coaxial Cable Driver



TL/H/10254–19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

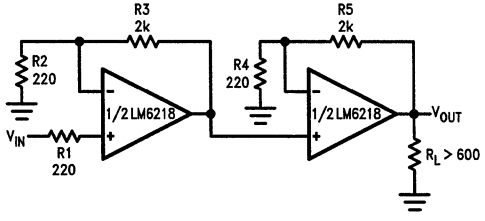


TL/H/10254–18

A_V = 10, $V_S = \pm 15V$, All resistors 0.01%

Small signal and large signal (20 V_{P-P}) B.W. ≈ 800 kHz

150 MHz Gain-Bandwidth Amplifier



TL/H/10254–20

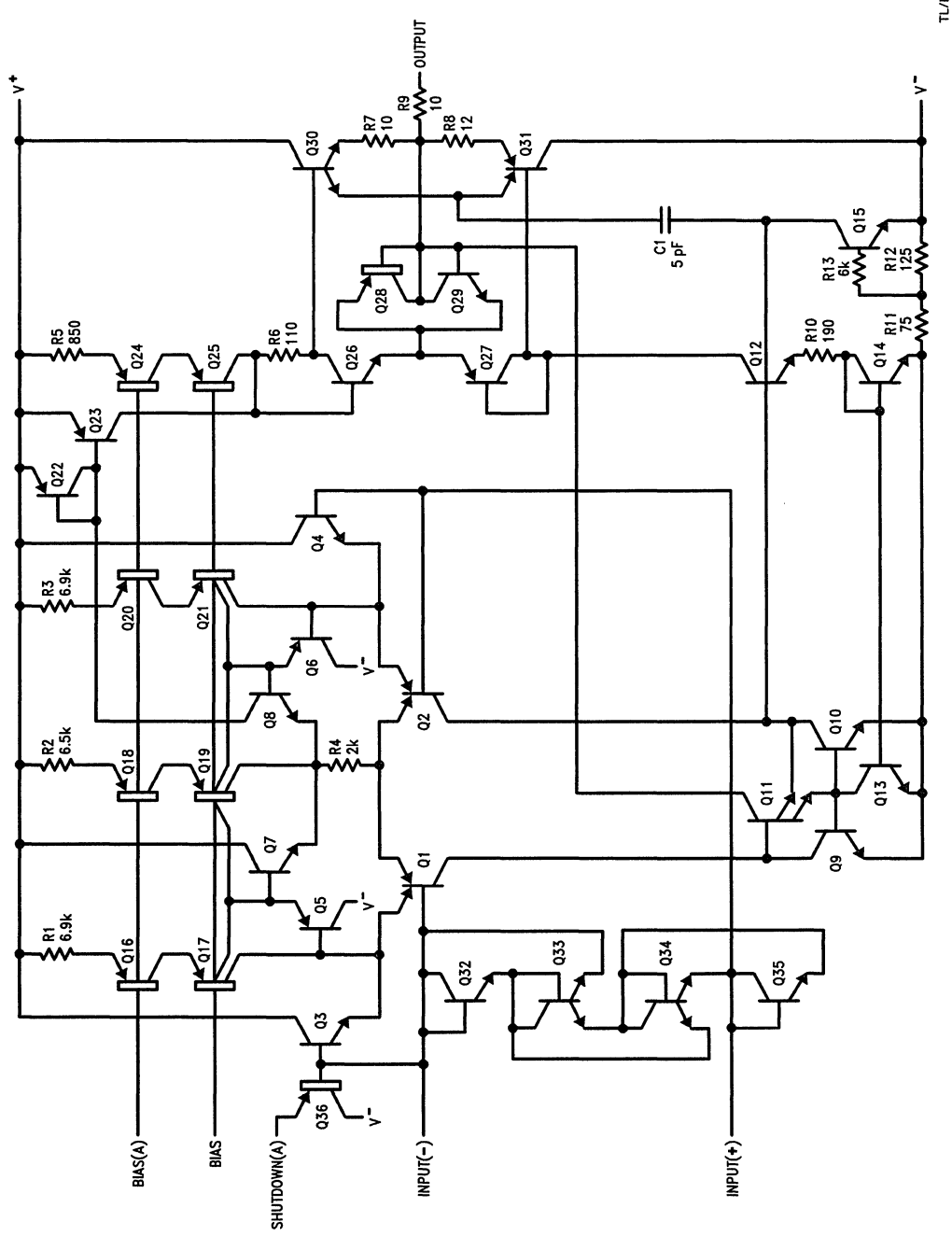
A_V = 100, $V_S = \pm 15V$,

Small signal BW ≈ 1.5 MHz

Large signal BW (20 V_{p-p}) ≈ 800 kHz

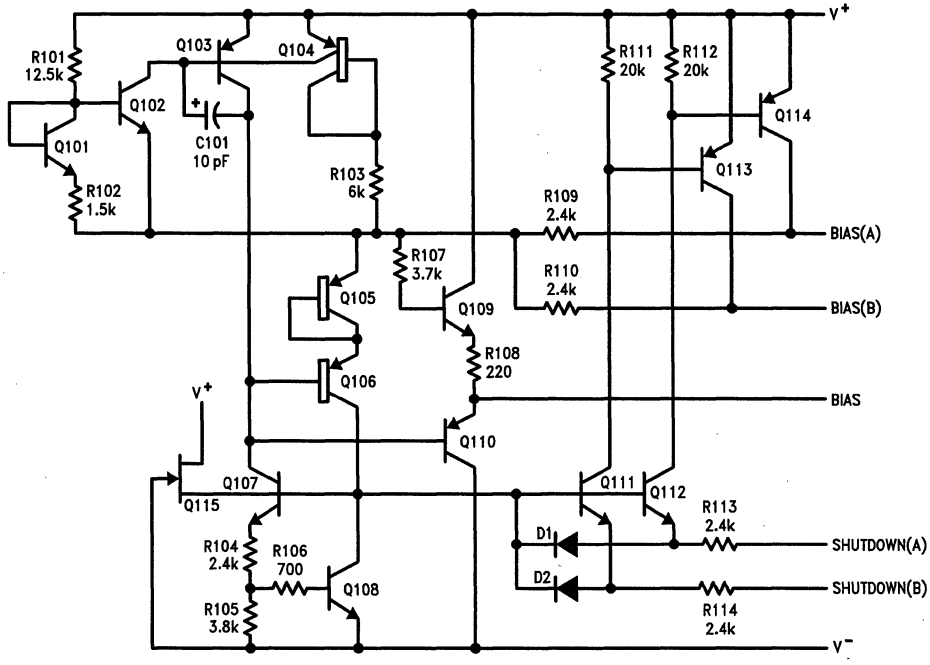
Schematic Diagram

½ LM6118 (Op Amp A)



Schematic Diagram (Continued)

Bias Circuit



TL/H/10254–22

National Semiconductor

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

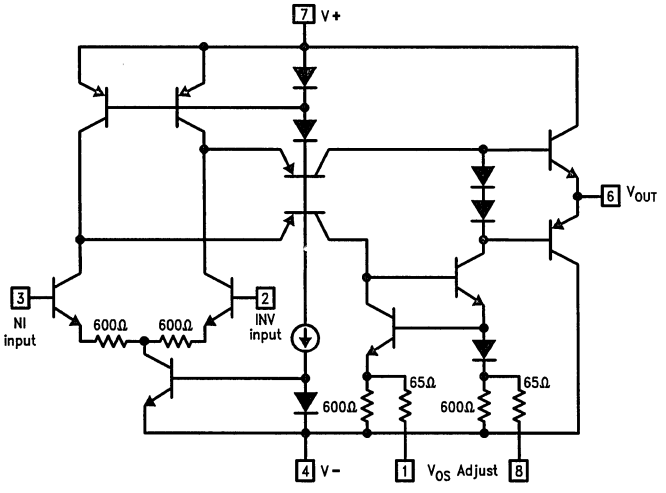
Features

■ High slew rate	300 V/μs
■ High unity gain freq	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

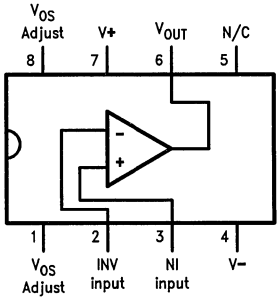
- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning

Simplified Schematic



TL/H/9057–3

Connection Diagram



TL/H/9057–5

Order Number LM6161J or LM6261J
See NS Package Number J08A

Order Number LM6261N or LM6361N
See NS Package Number N08E

Order Number LM6361M
See NS Package Number M08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 12)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 8 and 9)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		5	7 **10**		7	**9**	20	**22**	mV max
Input Offset Voltage Average Drift		10							µV/°C
Input Bias Current		2	3 **6**		3	**5**	5	**6**	µA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.4							nA/°C
Input Resistance	Differential	325							kΩ
Input Capacitance	Av = +1 @ 10 MHz	1.5							pF
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 11)	750	550 **300**		550	**400**	400	**350**	V/V min
	R_L = 10 kΩ	2900							V/V
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	Volts min
		−13.2	−12.9 **−12.7**		−12.9	**−12.7**	−12.8	**−12.7**	Volts min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	Volts min
		1.8	2.0 **2.2**		2.0	**2.2**	2.1	**2.2**	Volts max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**		80	**76**	72	**70**	dB min
Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	90	80 **74**		80	**76**	72	**70**	dB min

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	Volts min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	Volts min
	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	Volts min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	Volts max
Output Short Circuit Current	Souce	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6161		LM6261		LM6361		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	50	40 **30**		40	**35**	35	**32**	MHz min
	Supply = ±5V	35							MHz
Slew Rate	Av = +1 (Note 10)	300	200 **180**		200	**180**	200	**180**	V/μs min
	Supply = ±5V	200							V/μs
Power Bandwidth	V_{OUT} = 20 V_{pp}	4.5							MHz
Settling Time	10V Step to 0.1% Av = −1, R_L = 2 kΩ	120							ns
Phase Margin		45							Deg
Differential Gain	NTSC, Av = +4	<0.1							%
Differential Phase	NTSC, Av = +4	0.1							Deg
Input Noise Voltage	f = 10 kHz	15							$nV/\sqrt{Hz}$
Input Noise Current	f = 10 kHz	1.5							$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_j$ = 25°C with supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq$ 100 kΩ. **Boldface** limits apply over the range listed under "Operating Temperature Range" with $T_A = T_j$ in the "Absolute Maximum Ratings" section.

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are 100% production tested.

Note 5: All limits guaranteed at **temperature extremes (bold type face)** via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 7: $C_L \leq$ 5 pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

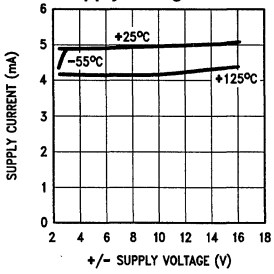
Note 10: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

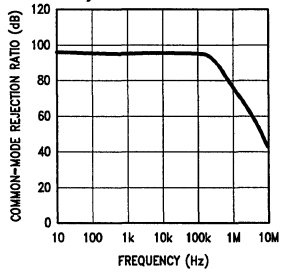
Note 12: The voltage between V^+ and either input pin must not exceed 36V.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

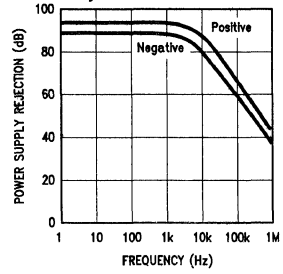
Supply Current vs Supply Voltage



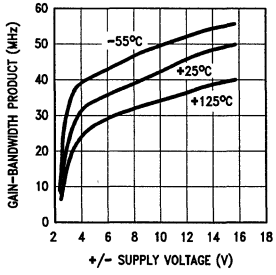
Common-Mode Rejection Ratio



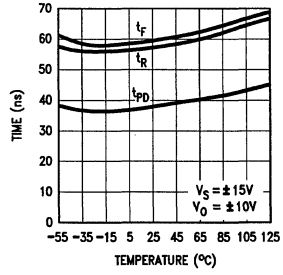
Power Supply Rejection Ratio



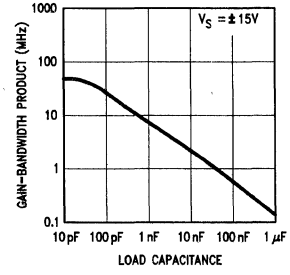
Gain-Bandwidth Product



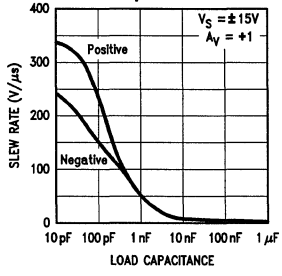
Propagation Delay Rise and Fall Times



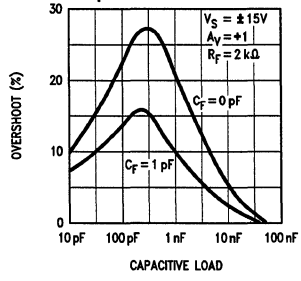
Gain-Bandwidth Product vs Load Capacitance



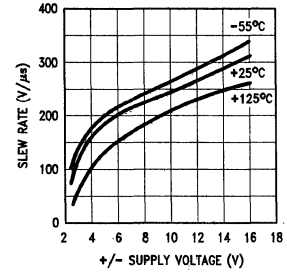
Slew Rate vs Load Capacitance



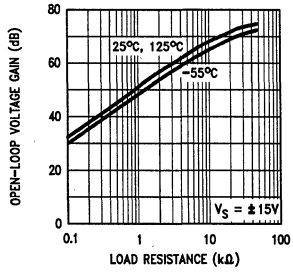
Overshoot vs Capacitive Load



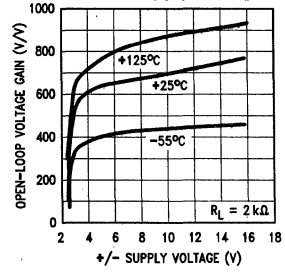
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage



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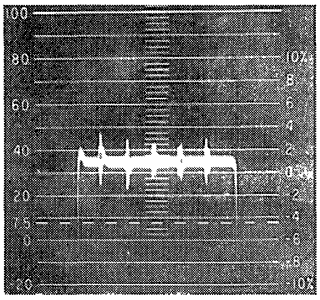
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



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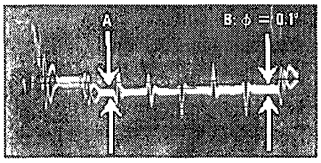
Differential Phase (Note)



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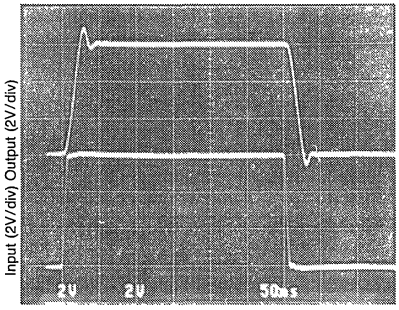
Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +1



(50 ns/div)

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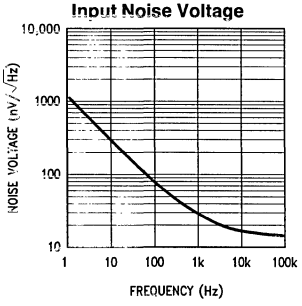
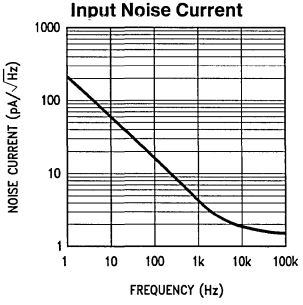
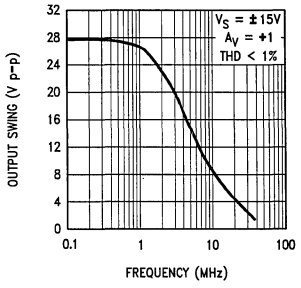
Input Noise Voltage



Input Noise Current



Power Bandwidth



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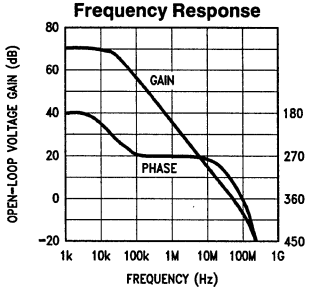
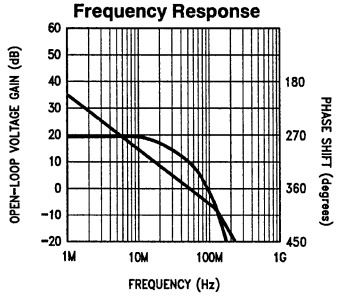
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

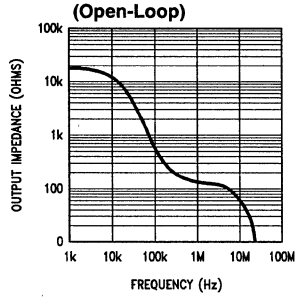
Open-Loop Frequency Response



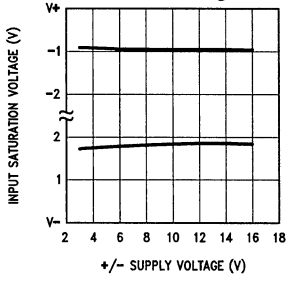
Open-Loop Frequency Response



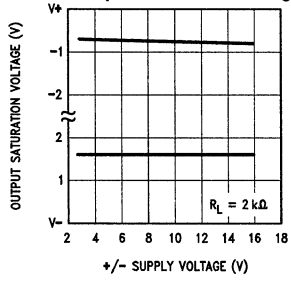
Output Impedence (Open-Loop)



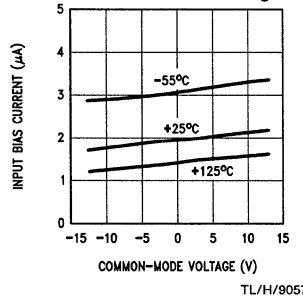
Common-Mode Input Saturation Voltage



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



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Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

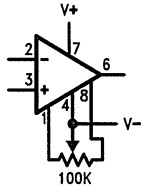
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

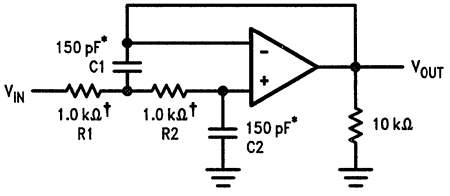
Typical Applications

Offset Voltage Adjustment



TL/H/9057–4

1 MHz Low-Pass Filter



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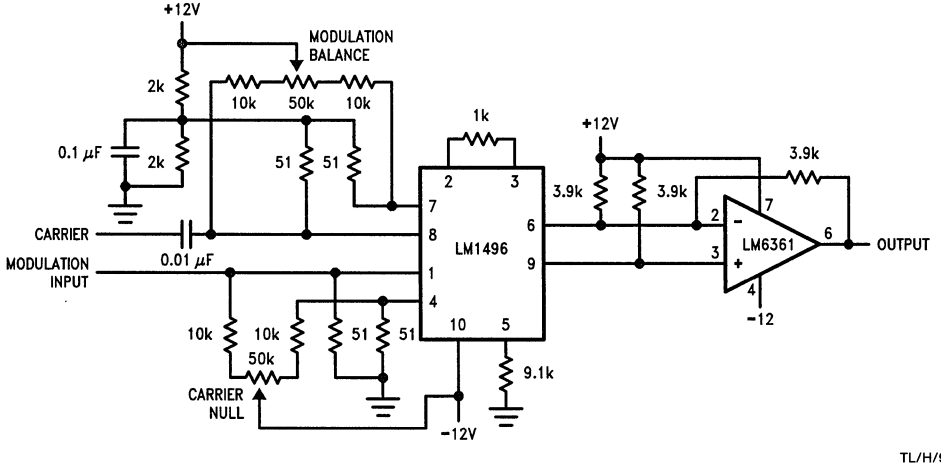
†1% tolerance

*Matching determines filter precision

$f_c = 2\pi\sqrt{(R1\ R2\ C1\ C2)}^{-1}$

Modulator with Differential-to-Single-Ended Converter



TL/H/9057–11

National Semiconductor

LM6164/LM6264/LM6364 High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

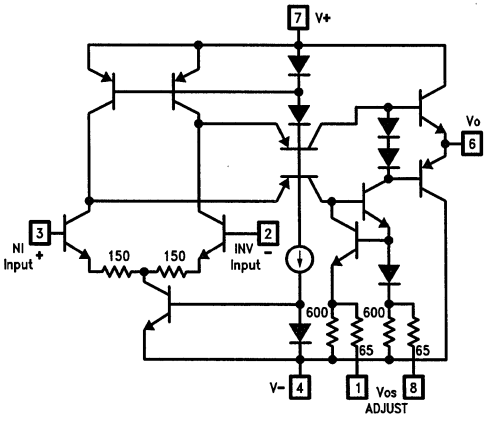
Features

■ High slew rate	300 V/μs
■ High GBW product	175 MHz
■ Low supply current	5 mA
■ Fast settling	100 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

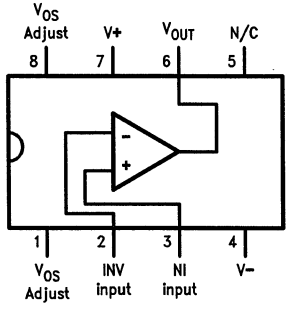
- Video amplifier
- Wide-bandwidth signal conditioning

Simplified Schematic



TL/H/9153–3

Connection Diagram



TL/H/9153–8

Order Number LM6164J or LM6264J
See NS Package Number J08A

Order Number LM6364M
See NS Package Number M08A

Order Number LM6264N or LM6364N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Input Voltage (Note 12)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to Gnd (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 8 & 9)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		2	4 **6**		4	**6**	9	**11**	mV max
Input Offset Voltage Average Drift		6							µV/°C
Input Bias Current		2.5	3 **6**		3	**5**	5	**6**	µA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	nA max
Input Offset Current Average Drift		0.3							nA/°C
Input Resistance	Differential	100							kΩ
Input Capacitance		3.0							pF
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\,k\Omega$ (Note 11)	2.5	1.8 **0.9**		1.8	**1.2**	1.3	**1.1**	V/mV min
	$R_L = 10\,k\Omega$	9							
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	V min
		−13.5	−13.3 **−13.1**		−13.3	**−13.1**	−13.2	**−13.1**	V min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	V min
		1.5	1.7 **1.9**		1.7	**1.9**	1.8	**1.9**	V max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	105	86 **80**		86	**82**	80	**78**	dB min
Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	96	86 **80**		86	**82**	80	**78**	dB min
Output Voltage Swing	Supply = ±15V and $R_L = 2\,k\Omega$	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	V min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	V min

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	V min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	V max
Output Short Circuit Current	Source	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6164		LM6264		LM6364		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	175	140 **100**		140	**120**	120	**100**	MHz min
	Supply = ±5V	120							
Slew Rate	A_V = +20 (Note 10)	300	200 **180**		200	**180**	200	**180**	V/μs min
	Supply = ±5V	200							
Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5							MHz
Setting Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100							ns
Phase Margin	A_V = +5	45							Deg
Differential Gain	NTSC, A_V = +10	<0.1							%
Differential Phase	NTSC, A_V = +10	<0.1							Deg
Input Noise Voltage	F = 10 kHz	8							nV/√Hz
Input Noise Current	F = 10 kHz	1.5							pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$ with supply voltage = ±15V, V_{CM} = 0V, and $r_l \geq 100$ KΩ **Boldface** limits apply over the range listed under "Operating Temperature Range".

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes.** All limits are 100% production tested.

Note 5: All limits guaranteed at room temperature (standard type face) and at **temperature extremes.** All limits are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 7: $C_L \leq 5$ pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

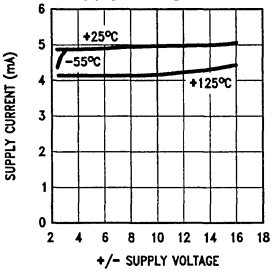
Note 10: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

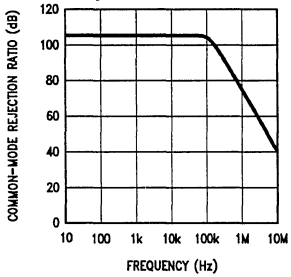
Note 12: The voltage between V^+ and either input pin must not exceed 36V.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

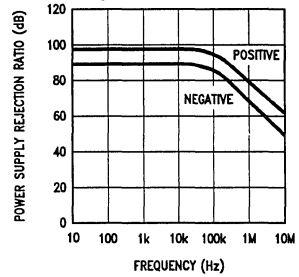
Supply Current vs Supply Voltage



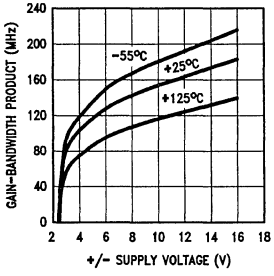
Common-Mode Rejection Ratio



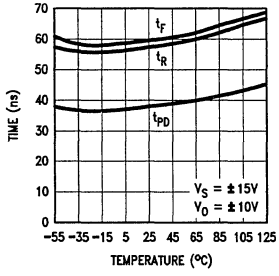
Power Supply Rejection Ratio



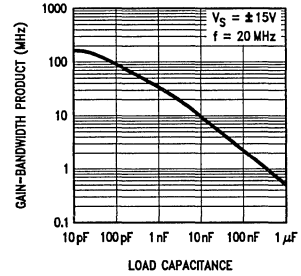
Gain-Bandwidth Product



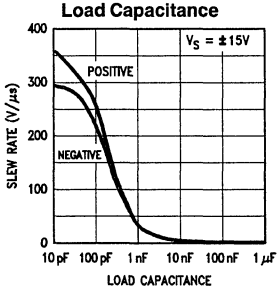
Propagation Delay Rise and Fall Time



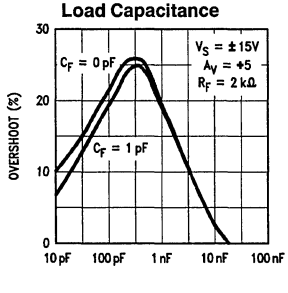
Gain-Bandwidth Product vs Load Capacitance



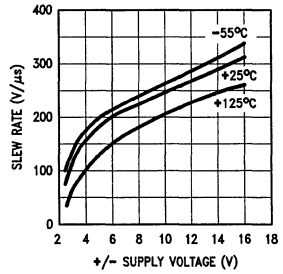
Slew Rate vs Load Capacitance



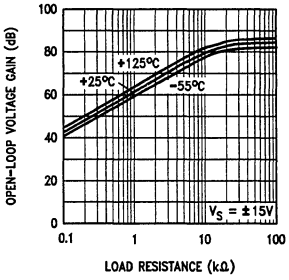
Overshoot vs Load Capacitance



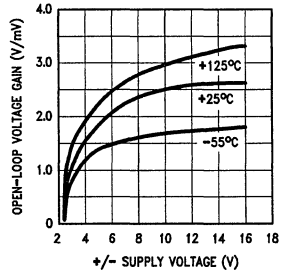
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

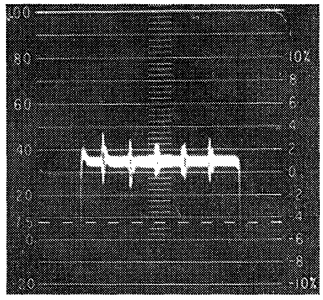


TL/H/9153–5

Typical Performance Characteristics

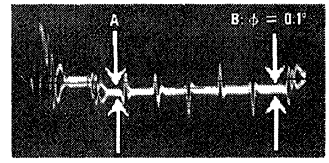
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9153–6

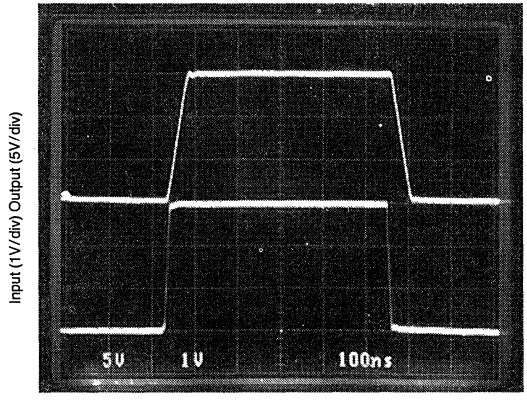
Differential Phase (Note)



TL/H/9153–7

Note: Differential gain and differential phase measured for four series LM6364 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

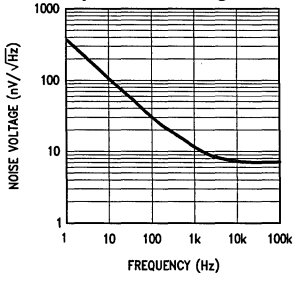
Step Response; Av = +5



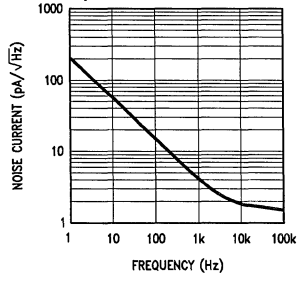
TL/H/9153–1

TIME (50 ns/div)

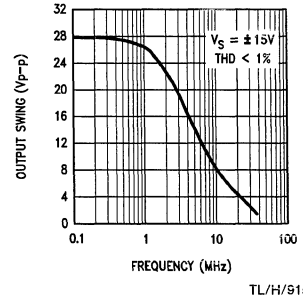
Input Noise Voltage



Input Noise Current



Power Bandwidth

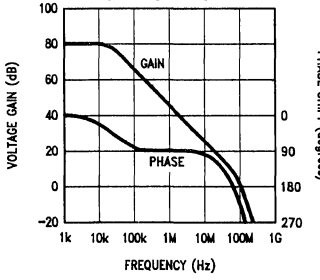


TL/H/9153–9

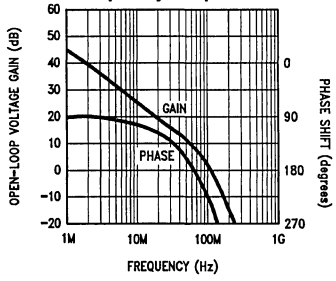
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

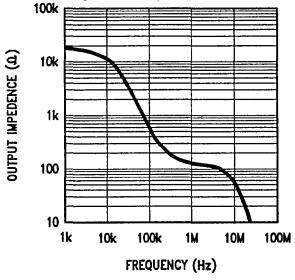
Open-Loop Frequency Response



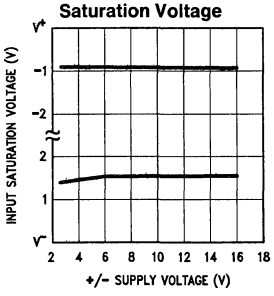
Open-Loop Frequency Response



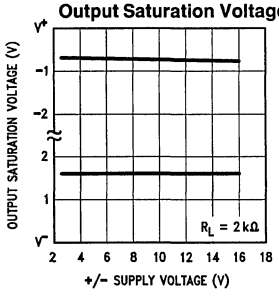
Output Resistance Open-Loop



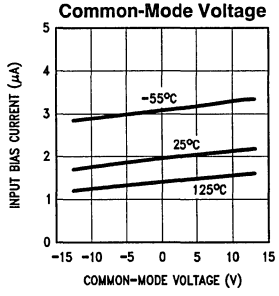
Common-Mode Input Saturation Voltage



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



TL/H/9153–13

3

Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/μs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

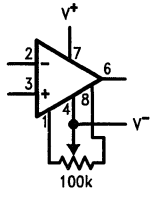
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

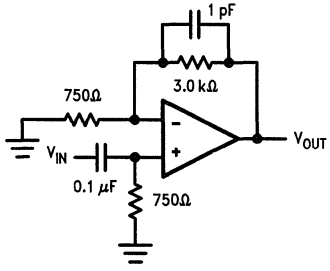
Typical Applications

Offset Voltage Adjustment



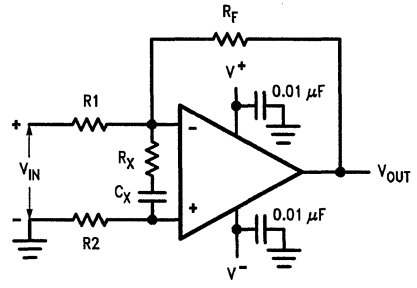
TL/H/9153–10

Video-Bandwidth Amplifier



TL/H/9153–12

Noise-Gain Compensation for Gains ≤5



TL/H/9153–11

$R_X C_X \geq (2\pi \cdot 25\ \text{MHz})^{-1}$

$5\ R_X = R_1 + R_F(1 + R_1/R_2)$

National Semiconductor

LM6165/LM6265/LM6365
High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

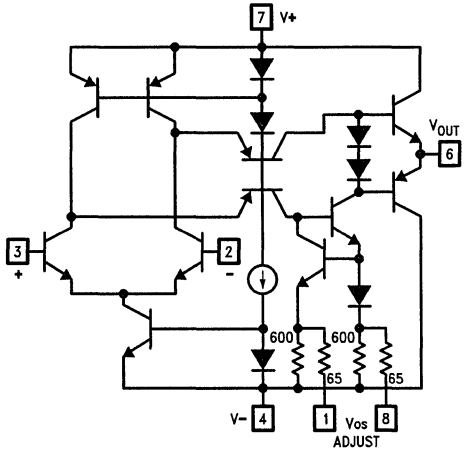
Features

■ High slew rate	300 V/μs
■ High GBW product	725 MHz
■ Low supply current	5 mA
■ Fast settling	80 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	<0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

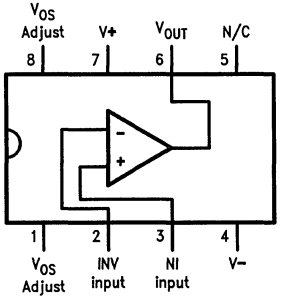
- Video amplifier
- Wide-bandwidth signal conditioning

Simplified Schematic



TL/H/9152-3

Connection Diagram



TL/H/9152-8

Order Number LM6165J or LM6265J
See NS Package Number J08A

Order Number LM6365M
See NS Package Number M08A

Order Number LM6265N or LM6365N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 12)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 8 and 9)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6165	$-55°C \le T_J \le +125°C$
LM6265	$-25°C \le T_J \le +85°C$
LM6365	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics (Note 3)

Parameter	Conditions	Typ	LM6165		LM6265		LM6365		Units
			Tested Limit	Design Limit	Tested Limit	Design Limit	Tested Limit	Design Limit	
			(Note 4)	(Note 5)	(Note 4)	(Note 5)	(Note 4)	(Note 5)	
Input Offset Voltage		1	3 **4**		3	**4**	6	**7**	mV max
Input Offset Voltage Average Drift		3							µV/°C
Input Bias Current		2.5	3 **6**		3	**5**	5	**6**	µA max
Input Offset Current		150	350 **800**		350	**600**	1500	**1900**	na max
Input Offset Current Average Drift		0.3							nA/°C
Input Resistance	Differential	20							kΩ
Input Capacitance		6.0							pF
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 11)	10.5	7.5 **5.0**		7.5	**6.0**	5.5	**5.0**	V/mV min
	$R_L = 10\ k\Omega$	38							
Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**		+13.9	**+13.8**	+13.8	**+13.7**	V min
		−13.6	−13.4 **−13.2**		−13.4	**−13.2**	−13.3	**−13.2**	V min
	Supply = +5V (Note 6)	4.0	3.9 **3.8**		3.9	**3.8**	3.8	**3.7**	V min
		1.4	1.6 **1.8**		1.6	**1.8**	1.7	**1.8**	V max
Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	102	88 **82**		88	**84**	80	**78**	dB min
Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	104	88 **82**		88	**84**	80	**78**	dB min
Output Voltage Swing	Supply = ±15V and $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**		+13.5	**+13.3**	+13.4	**+13.3**	V min
		−13.4	−13.0 **−12.7**		−13.0	**−12.8**	−12.9	**−12.8**	V min

DC Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	Typ	LM6165		LM6265		LM6365		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 6)	4.2	3.5 **3.3**		3.5	**3.3**	3.4	**3.3**	V min
		1.3	1.7 **2.0**		1.7	**1.9**	1.8	**1.9**	V max
Output Short Circuit Current	Source	65	30 **20**		30	**25**	30	**25**	mA min
	Sink	65	30 **20**		30	**25**	30	**25**	mA min
Supply Current		5.0	6.5 **6.8**		6.5	**6.7**	6.8	**6.9**	mA max

AC Electrical Characteristics (Notes 3 & 7)

Parameter	Conditions	Typ	LM6165		LM6265		LM6365		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Gain-Bandwidth Product	@ F = 20 MHz	725	575 **350**		575	**425**	500	**400**	MHz min
	Supply = ±5V	500							
Slew Rate	A_V = +25 (Note 10)	300	200 **180**		200	**180**	200	**180**	V/μs min
	Supply = ±5V	200							
Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5							MHz
Setting Time	10V Step to 0.1% A_V = −25, R_L = 2 kΩ	80							ns
Phase Margin	A_V = +25	45							Deg
Differential Gain	NTSC, A_V = +25	<0.1							%
Differential Phase	NTSC, A_V = +25	<0.1							Deg
Input Noise Voltage	F = 10 kHz	5							nV/√Hz
Input Noise Current	F = 10 kHz	1.5							pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, and the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Unless otherwise specified, all limits guaranteed for $T_a = T_j$ = 25°C with supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq$ 100 kΩ. **Boldface** limits apply over the range listed under "Operating Temperature Range".

Note 4: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face)**. All limits are 100% production tested.

Note 5: All limits guaranteed at room temperature (standard type face) and at **temperature extremes (bold type face).** All limits are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Note 6: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5C, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 7: $C_L \leq$ 5 pF.

Note 8: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exeeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 9: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

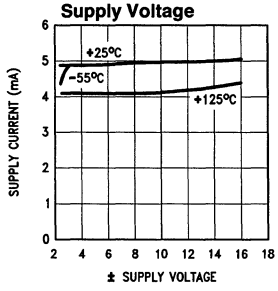
Note 10: V_{IN} = 0.7V step. For supply = ±5V, V_{IN} = 0.2V step.

Note 11: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

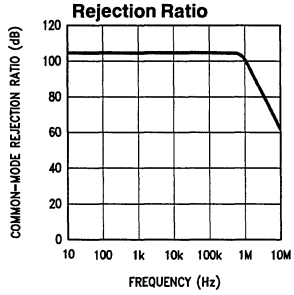
Note 12: The voltage between V+ and either input pin must not exceed 36V.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise specified

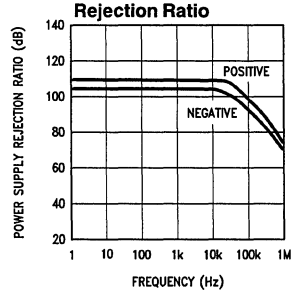
Supply Current vs Supply Voltage



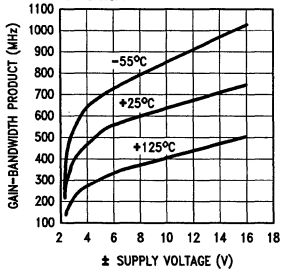
Common-Mode Rejection Ratio



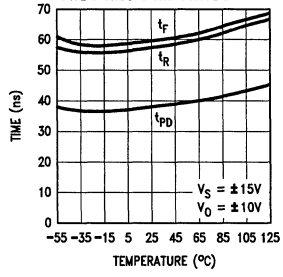
Power Supply Rejection Ratio



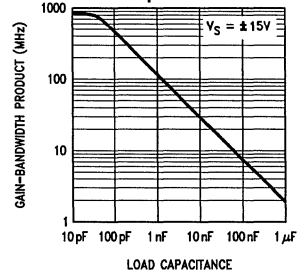
Gain-Bandwidth Product



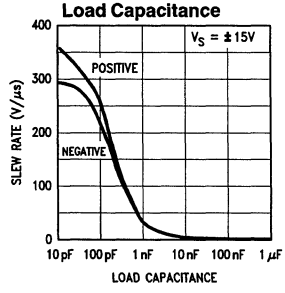
Propagation Delay, Rise and Fall Times



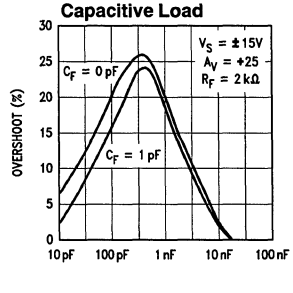
Gain-Bandwidth Product vs Load Capacitance



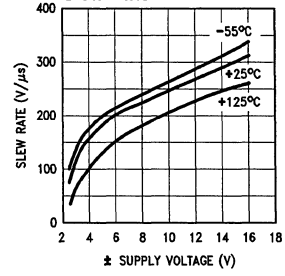
Slew Rate vs Load Capacitance



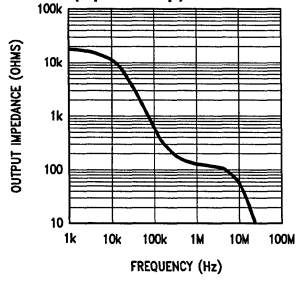
Overshoot vs Capacitive Load



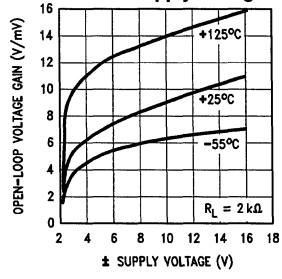
Slew Rate



Output Impedance (Open-Loop)



Gain vs Supply Voltage



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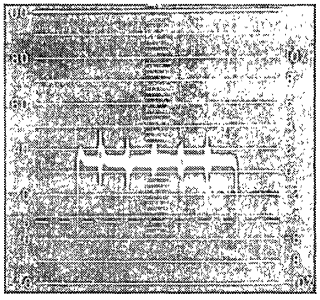
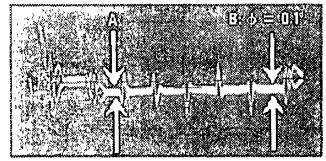
Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

Differential Gain (Note)



Differential Phase (Note)



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Note: Differential gain and differential phase measured for four series LM6365 op amps configured with gain of +25 (each output attenuated by 96%), in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

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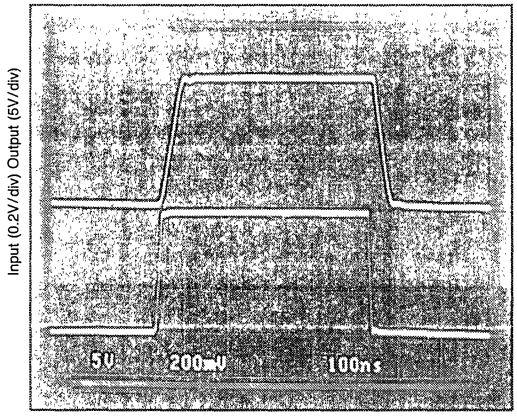
Step Response; Av = +1



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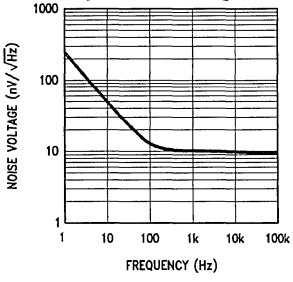
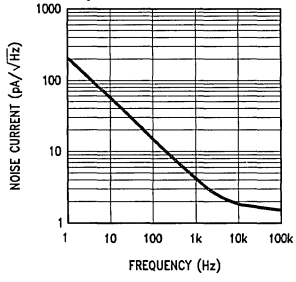
TIME (50 (ns/div)

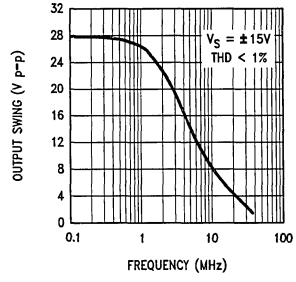
Input Noise Voltage



Input Noise Current



Power Bandwidth

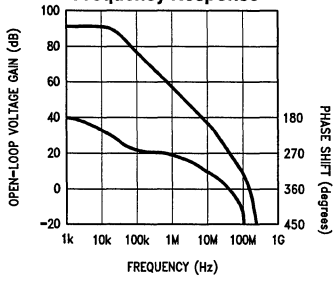


TL/H/9152-9

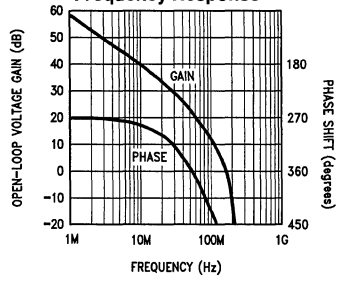
Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

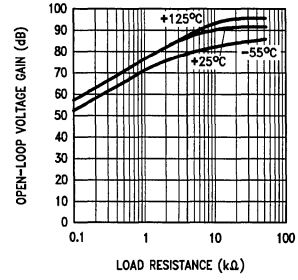
Open-Loop Frequency Response



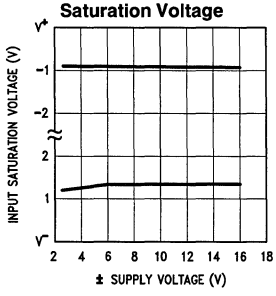
Open-Loop Frequency Response



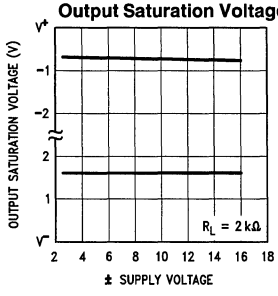
Voltage Gain vs Load Resistance



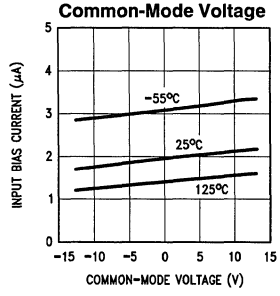
Common-Mode Input Saturation Voltage



Output Saturation Voltage



Bias Current vs Common-Mode Voltage



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Applications Tips

The LM6365 has no frequency compensation, but is stable for gains of 25 or greater (over the specified ranges of temperature, power supply voltage, and load). The LM6365 and LM6364, specified in separate datasheets, are compensated versions of the LM6365. The LM6361 is unity-gain stable, while the LM6364 is stable for gains as low as 5. The LM6361, and LM6364 have the same high slew rate as the LM6365, typically 300 V/μs.

To use the LM6365 for gains less than 25, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 25.

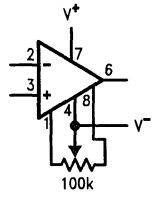
Power supply bypassing will improve stability and transient response of the LM6365, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

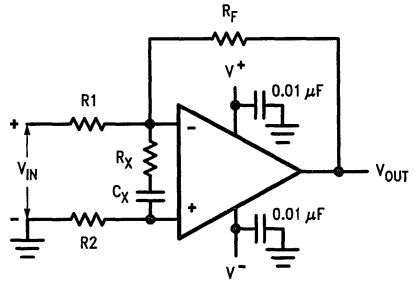
Typical Applications

Offset Voltage Adjustment



TL/H/9152–11

Noise-Gain Compensation



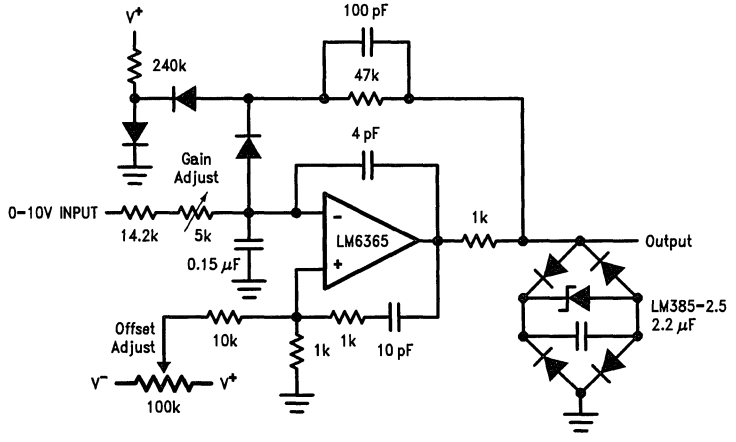
TL/H/9152–12

$R_XC_X \geq 1/2\pi \bullet 25$ MHz

$[R1 + R_F (1 + R1/R2)] = 25\ R_X$

1 MHz Voltage-to-Frequency Converter

(f_{OUT} = 1 MHz for V_{IN} = 10V)



TL/H/9152–13

National Semiconductor

LM6313 High Speed, High Power Operational Amplifier

General Description

The LM6313 is a high-speed, high-power operational amplifier. This operational amplifier features a 35 MHz small signal bandwidth, and 250 V/μs slew rate. A compensation pin is included for adjusting the open loop bandwidth. The input stage (A1) and output stage (A2) are pinned out separately, and can be used independently. The operational amplifier is designed for low impedance loads and will deliver ±300 mA. The LM6313 has both overcurrent and thermal shutdown protection with an error flag to signal both these fault conditions.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

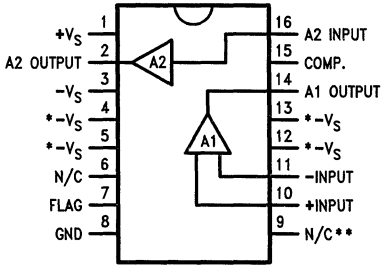
- High slew rate 250 V/μs
- Wide bandwidth 35 MHz
- Peak output current ±300 mA
- Input and output stages pinned out separately
- Single or dual supply operation
- Thermal protection
- Error flag warns of faults
- Wide supply voltage range ±5V to ±15V

Applications

- High speed ATE pin driver
- Data acquisition
- Driving capacitive loads
- Flash A-D input driver
- Precision 50Ω–75Ω video line driver
- Laser diode driver

Connection Diagram

Dual-In-Line Package



TL/H/10521–1

Top View

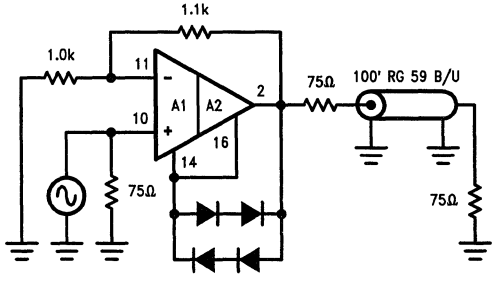
Order Number LM6313N
See NS Package Number N16A

*Heat sink pins

See Note 5 and Applications.

**Do not ground or otherwise connect to this pin.

Typical Application



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Absolute Maximum Ratings (Note 1)

Total Supply Voltage ($+V_S$ to $-V_S$)	36V (±18)
A1 Differential Input Voltage (Note 2)	±7V
A1 Input Voltage	$(V^+ - 0.7)$ to $(V^- - 7V)$
A2 Input to Output Voltage	±7V
A2 Input Voltage	$\pm V_S$
Flag Output Voltage	GND to $+V_S$
Short-Circuit to Ground	(Note 3)
Storage Temperature Range	$-65°C \le T \le +150°C$
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Tolerance (Note 4)	
Pins 10 and 11	±600V
All Other Pins	±1500V
Operating Temperature Range	
LM6313N	0°C to 70°C
Thermal Derating Information (Note 5)	
θ_{JA}	40°C/W
T_J (Max)	125°C

Operational Amplifier DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OS}	Input Offset Voltage		5	20	**22**	mV (Max)
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		10			µV/°C
I_b	Input Bias Current		2	5	**7**	µA (Max)
I_{OS}	Input Offset Current		0.15	1.5	**1.9**	µA (Max)
$\Delta I_{OS}/\Delta T$	Average Input Offset Current Drift		0.4			nA/°C
R_{IN}	Input Resistance	Differential	325			kΩ
C_{IN}	Input Capacitance	A_V = +1, f = 10 MHz	2.2			pF
V_{CM}	Common-Mode Voltage Range		+14.2 −13.2	+13.8 −12.8	**+13.7** **−12.7**	V (Min)
A_{V1} A_{V2}	Voltage Gain 1 Voltage Gain 2	R_L = 1 kΩ, V_O = ±10V R_L = 50Ω, V_O = ±8V	6000 5000	2500 2000	**2000** **1500**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm 5V \le V_S \le \pm 16V$	90	72	**70**	dB (Min)
V_{O1} V_{O2} V_{O3}	Output Voltage Swing 1 Output Voltage Swing 2 Output Voltage Swing 3	R_L = 1 kΩ R_L = 100Ω R_L = 50Ω	13.1 12.0 11.0	11.8 10.5 9.0	**11.2** **10.0** **8.5**	±V (Min)
I_S	Supply Current	T_J = 0°C T_J = 25°C T_J = 125°C	18	23	**24** **21**	mA (Max)
I_{SC}	Peak Short-Circuit Output	(See *Figure 3*)	300			mA

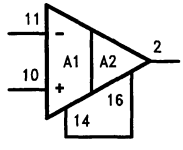

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FIGURE 1

Electrical Characteristics (Continued)

Operational Amplifier AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	Units
GBW	Gain-Bandwidth Product	@ f = 30 MHz	35	MHz
SR	Slew Rate	A_V = −1, R_L = 50Ω (Note 6)	250	V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	3.0	MHz
t_S	Settling Time	10V Step to 0.1% (See *Figure 2*)	200	ns
	Phase Margin	A_V = −1, R_L = 1 kΩ, C_L = 50 pF	53	Deg
	Differential Gain		0.1	%
	Differential Phase		0.1	Deg
e_n	Input Noise Voltage	f = 10 kHz	14	nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.8	pA/√Hz

A1 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ V_{OUT} = ±10V, R_L = ∞	650 6000	300 2500	**250** **2000**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	±5V ≤ ±V_S ≤ +16V	90	72	**70**	dB (Min)
I_{SC}	Output Short Circuit Current		±60	±30	**±25**	mA (Min)

A1 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
GBW	Gain-Bandwidth	f = 30 MHz	37	25	MHz (Min)
SR	Slew Rate	A_V = +1, R_L = 100 kΩ, ±4 V_{IN}, ±2 V_{OUT}	250	150	V/μs (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test condition listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors. Degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise) is proportional to the level of the externally limited breakdown current and the accumulated duration of the breakdown condition.

Note 3: Continuous short-circuit operation of A1 at elevated temperature can result in exceeding the maximum allowed junction temperature of 125°C. A2 contains current limit and thermal shutdown to protect against fault conditions. The device may be damaged by shorts to the supplies.

Note 4: Human body model, C = 100 pF, R_S = 1500Ω.

Electrical Characteristics (Continued)

A2 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_{IN} = ±10V	0.99	0.97	**0.95**	V/mV (Min)
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.9	0.85	**0.82**	V/V (Min)
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	70	**100**	mV (Max)
I_b	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	6	**8**	μA (Max)
R_{IN}	Input Resistance	R_L = 50Ω	5			MΩ
C_{IN}	Input Capacitance		3.5			pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3.5	5.0	**8.0**	Ω (Min)
V_O	Voltage Output Swing	R_L = 1 kΩ R_L = 100Ω R_L = 50Ω	13.7 12.5 11.0	13.0 10.5 9.0	**12.7** **10.0** **8.5**	V (Min)
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±16V	70	60	**50**	dB (Min)

A2 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
SR 1 SR 2	Slew Rate 1 Slew Rate 2	V_{IN} = ±11V, R_L = 1 kΩ V_{IN} = ±11V, R_L = 50Ω (Note 7)	1200 750	 550	V/μs (Min)
BW	−3 dB Bandwidth	V_{IN} = ±100 mVpp R_L = 50Ω, C_L ≤ 10 pF	65	30	MHz (Min)
t_r, t_f	Rise Time Fall Time	R_L = 1 kΩ, C_L ≤ 10 pF V_O = 100 mVpp	8		ns
P_D	Propagation Delay	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mVpp	4		ns
	Overshoot	R_L = 1 kΩ, C_L = 100 pF R_L = 50Ω, C_L = 1000 pF	13 21		%

Additional (A2) Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OL}	Flag Pin Output Low Voltage	I_{SINK} Flag Pin = 500 μA	220	340	**400**	mV (Max)
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 8)	0.01	10	**20**	μA (Max)

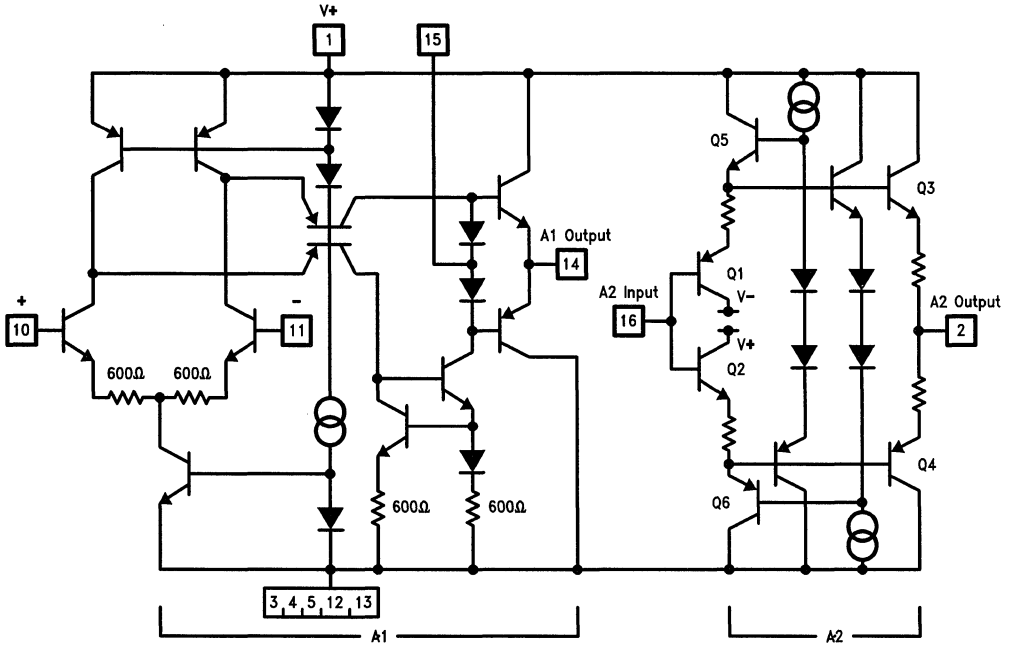
Note 5: For operation at elevated temperature, these devices must be derated to insure $T_J \leq 125°C$. $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} for the N package mounted flush to the PCB, is 40°C/W when pins 4, 5, 12 and 13 are soldered to a total of 2 in^2 of copper trace.

Note 6: Measured between ±5V.

Note 7: V_{IN} = ±9V step input, measured between ±5V out.

Note 8: The error flag is set during current limit or thermal shut-down. The flag is an open collector, low on fault.

Simplified Schematic



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Settling Time Test Circuit

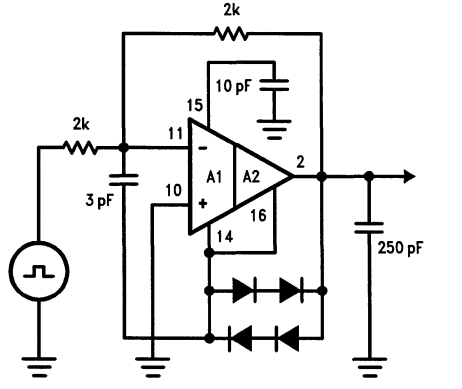

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FIGURE 2

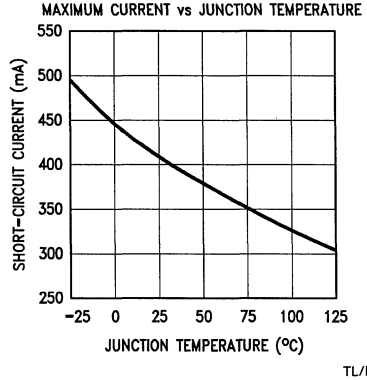

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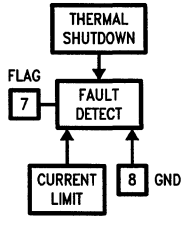
FIGURE 3

Protection Circuit Block Diagram



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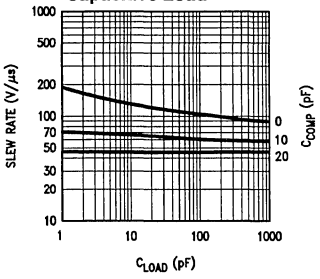
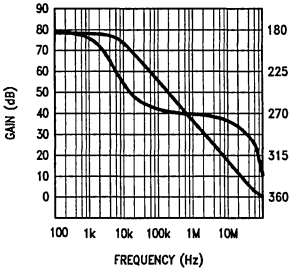
Typical Performance Characteristics Op Amp

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

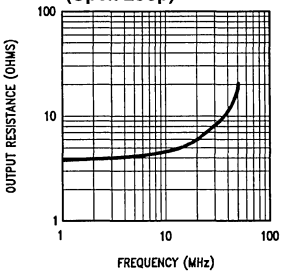
Slew Rate vs Capacitive Load



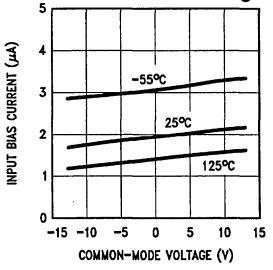
Bode Plot



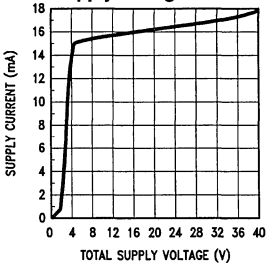
Output Resistance (Open Loop)



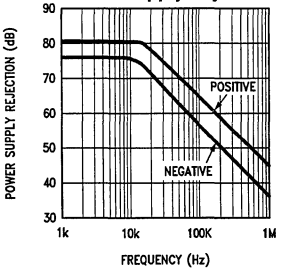
Bias Current vs Common-Mode Voltage



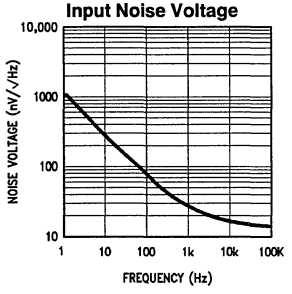
Supply Current vs Supply Voltage



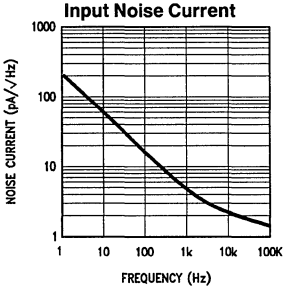
Power Supply Rejection



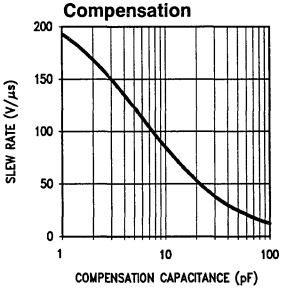
Input Noise Voltage



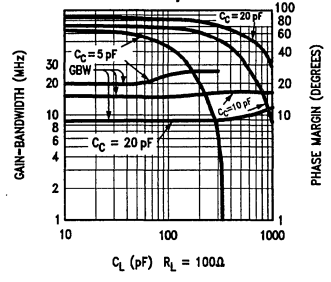
Input Noise Current



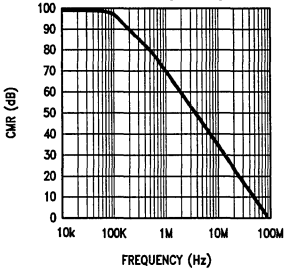
Slew Rate vs Compensation



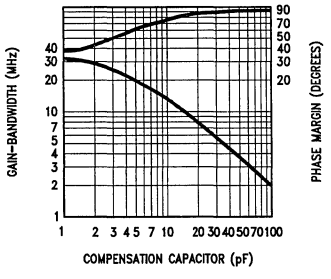
Gain-Bandwidth, Phase Margin vs Comp Cap and Load Cap



CMR vs Frequency



GBW and Phase Margin vs Comp Cap



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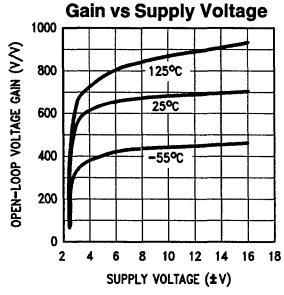
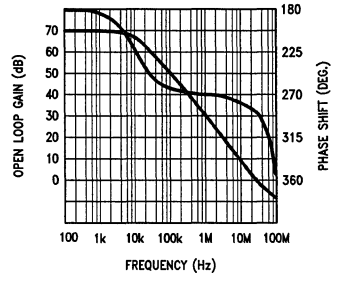
Typical Performance Characteristics A1 Only

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

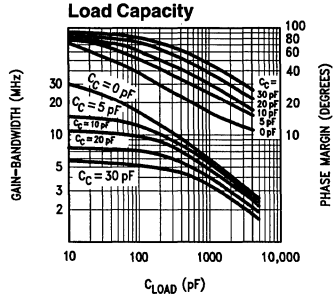
Gain vs Supply Voltage



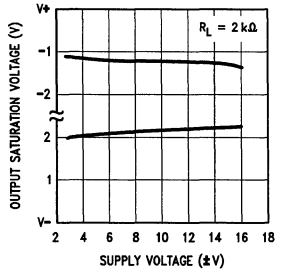
Bode Plot



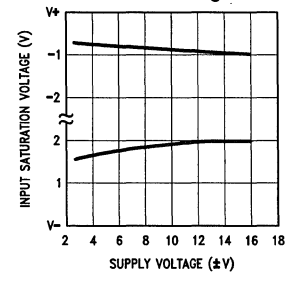
Gain-Bandwidth and Phase Margin vs Load Capacity



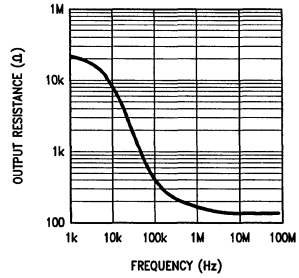
Output Saturation Voltage



Common-Mode Input Saturation Voltage



Output Resistance (Open Loop)



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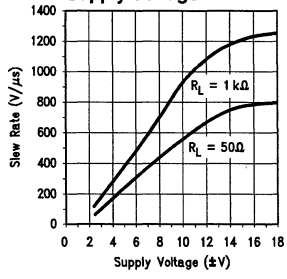
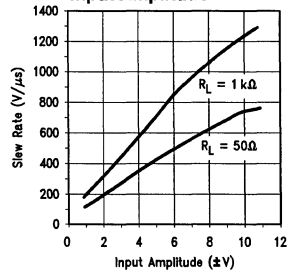
Typical Performance Characteristics A2 Only

(Unless otherwise specified, T_A = 25°C and V_S = ±15V.)

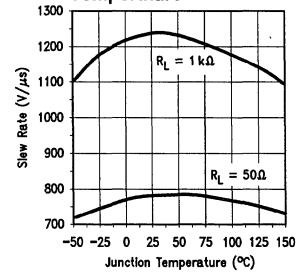
Slew Rate vs Supply Voltage



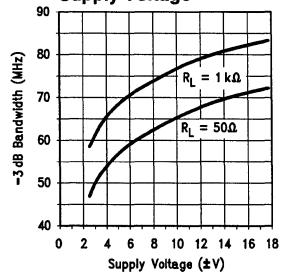
Slew Rate vs Input Amplitude



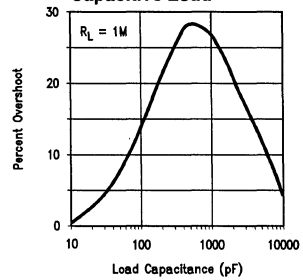
Slew Rate vs Temperature



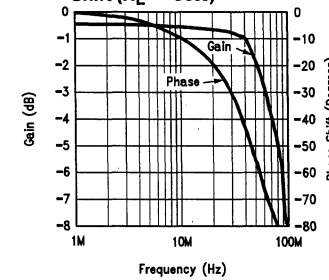
Bandwidth vs Supply Voltage



Overshoot vs Capacitive Load



Gain and Phase Shift (R_L = 50Ω)



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Application Hints

The LM6313 is a high-speed, high power operational amplifier that is designed for driving low-impedance loads such as 50Ω and 75Ω cables. Available in the standard, low cost, 16-pin DIP, this amplifier will drive back terminated video cables with up to 10 Vp-p. The ability to add additional compensation allows the LM6313 to drive capacitive loads of any size at bandwidths previously possible only with very expensive hybrid devices.

The LM6313 is excellent for driving high-speed flash A-to-D converters that require low-impedance drive at high frequencies. At 1 MHz, when used as a buffer, the LM6313 output impedance is below 0.1Ω. This very low output impedance also means that cables can be accurately back-terminated by just placing the characteristic impedance in series with the LM6313 output.

OVER-VOLTAGE PROTECTION

If the LM6313 is being operated on supply voltages of greater than ±5V, the possibility of damaging the output stage transistors exists. At higher supply voltages, if the output is shorted or excessive power dissipation causes the output stage to shut down, the maximum A2 input-to-output voltage, can be exceeded. This occurs when the input stage tries to drive the output while the output is at ground. To prevent this from happening, an easy solution is to place diodes around the output stage (See *Figure 4*). This will limit the maximum differential voltage to about 1.3V. Any signal diode, such as the 1N914 or the 1N4148 will work fine.

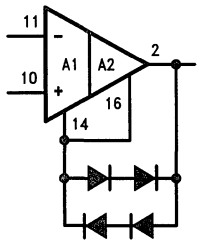

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FIGURE 4

HEAT SINKING

When driving a low impedance load such as 50Ω, and operating from ±15V supplies, the internal power dissipation of the LM6313 can rise above 3W. To prevent overheating of the chip, which would cause the thermal protection circuitry to shut the system down, the following guidelines should be followed:

1. Reduce the supply voltage. The LM6313 will operate with little change in performance, except output voltage swing, on ±5V supplies. This will reduce the dissipation to the level where no precautions against overheating are necessary for loads of 10Ω or more.
2. Solder pins 4, 5, 12 and 13 to copper traces which are at least 0.100 inch wide and have a total area of at least 2 square inches, to obtain a θ_{JA} of 40°C/W. These four pins are connected to the back of the chip and will be at V−. They should not be used as a V− connection unless pin 3 is also connected to this same point.

SUPPLY BYPASSING

Because of the large currents required to drive low-impedance loads, supply bypassing as close as possible to the I.C. is important. At 50 MHz, a few inches of wire or circuit trace can have 20Ω or 30Ω of inductive reactance. This inductance in series with a 0.1 μF bypass capacitor can resonate at 1 MHz to 2 MHz and just appear as an inductor at higher frequencies. A 0.1 μF and a 10μF to 15 μF capacitor connected in parallel and as close as possible to the LM6313 supply pins, from each supply to ground, will give best performance.

SELECTION OF COMPENSATION CAPACITOR

The compensation pin, pin 15, makes it possible to drive any load at any closed loop gain without stability problems. In most cases, where the gain is −1 or greater and the load is resistive, no compensation capacitor is required. When used at unity gain or when driving reactive loads, a small capacitor of 5 pF to 20 pF will insure optimum performance. The easiest way to determine the best value of compensation capacitor is to temporarily connect a trimmer capacitor (typical range of 2 pF to 15 pF) between pin 15, and ground, and adjust it for little or no overshoot at the output while driving the input with a square wave.

If the actual load capacitance is known, the typical graphs "Gain-Bandwidth and Phase Margin vs. Load Capacitance" can be used to select a value.

VIDEO CABLE DRIVER

The LM6313 is ideally suited for driving 50Ω or 75Ω cables. Unlike a buffer that requires a separate gain stage to make up for the losses involved in termination, the LM6313 gain can be set to 1 plus the line losses when the transmission line is end-terminated. If back-termination is needed, adding the line impedance in series with the output and raising the gain to 2 plus the expected line losses will provide a 0 dB loss system. *Figure 5* illustrates the back and end terminated video system including compensation for line losses. The excellent stability of the LM6313 with changes in supply voltages allow running the amplifier on unregulated supplies. The typical change in phase shift when the supplies are changed from ±5V to ±15V is less than 3° at 10 MHz.

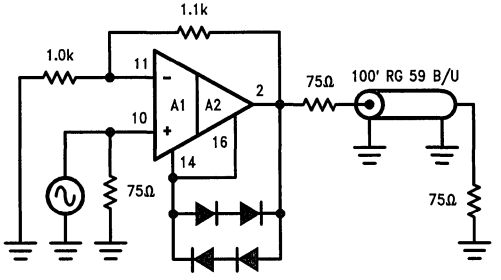

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FIGURE 5

Application Hints (Continued)

LASER DIODE MODULATOR

Figure 6 is a minimum component count example of a video modulator for a CW laser diode. This example biases the diode at 200 mA and modulates the current at ±200 mA per volt of signal. If it is desired to reduce power consumption and ±5V supplies are available, all that is necessary is to change R2 to 5 kΩ and R4 to 15Ω.

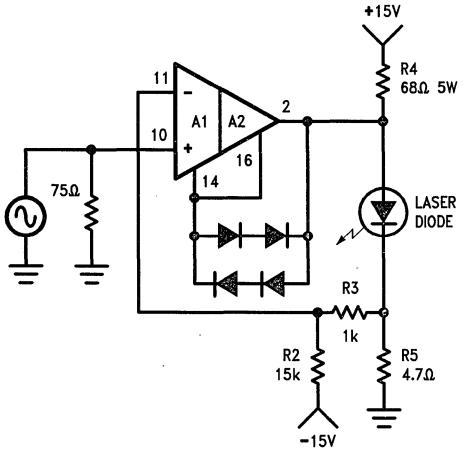

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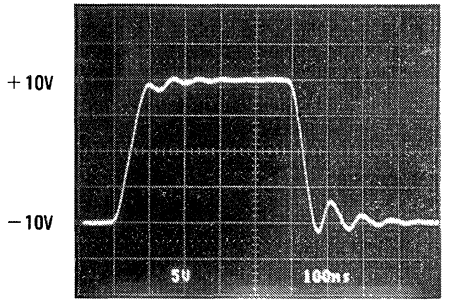
FIGURE 6

In photo 1, C_L is 1000 pF. The LM6313 is slewing at 250 V/μs, from −5V to +5V. The slew rate is 450 V/μs from +5V to −5V. This requires the op amp to deliver 450 mA into the load and remain stable.

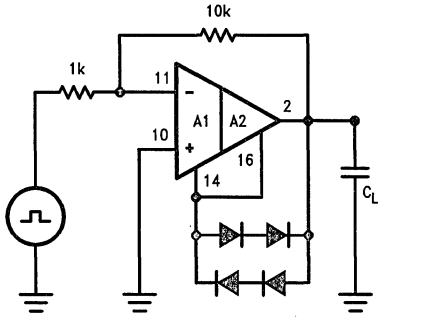


TL/H/10521–16

Photo 1

CAPACITIVE LOAD DRIVING

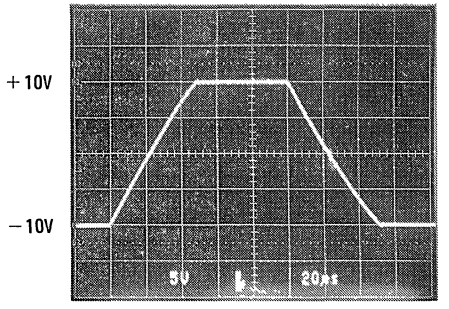
Figure 7 is the circuit used to demonstrate the ability of the LM6313 to drive capacitive loads at speeds not previously possible with monolithic op amps.



TL/H/10521–14

FIGURE 7

In photo 2, C_L is changed to 1 μF. Under these conditions, the op amp is forced into current limiting. Here the current is internally limited to about ±400 mA. Note the rapid and complete recovery to normal operation at the end of slewing.



TL/H/10521–15

Photo 2

National Semiconductor

LM13080
Programmable Power Operational Amplifier

General Description

The LM13080 is an internally compensated medium power operational amplifier designed for use in those applications requiring load currents of several hundred milliamperes. This amplifier has the added advantage of having an input stage programmed with an external resistor. The user is able to optimize the amplifier performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifiers, DC-to-DC converters, precision power comparators which can either sink or source current and motor speed controls.

The LM13080 may be powered from either single or dual power supplies, and will operate from as little as 3V.

As a power operational amplifier, the LM13080 is capable of delivering 0.25A to a load. This feature allows the system designer to fulfill his medium power circuit requirements without having to add external current boost transistors to the output of a standard operational amplifier.

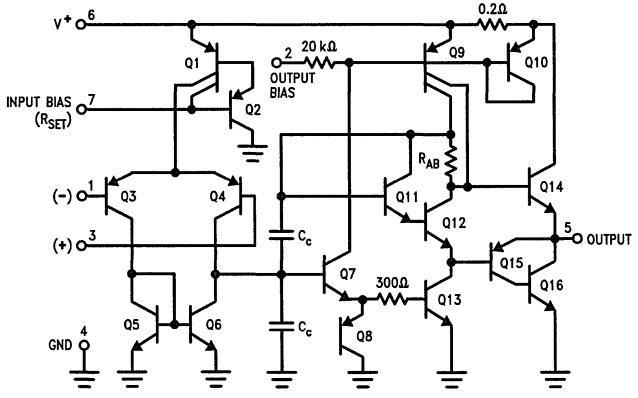
By selecting the proper input stage bias resistor it is possible to tailor the performance of the input stage to meet the needs of any particular system. Trade-offs between input offset voltage, input bias current and gain bandwidth are easily made.

An unusual feature of the LM13080 is an electronic shut-down capability.

Features

- High output current—250 mA
- Externally programmable input stage
- Low power supply operation—3V
- Electronic shut-down capability
- Internally compensated for unity gain
- Low input bias current

Schematic Diagram



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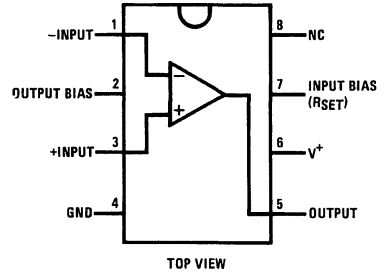
Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/7978–1

Order Number LM13080N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Operation Range	3V to 15V ±1.5V to ±7.5V
Power Dissipation (Note 1)	1250 mW
Differential Input Voltage (Note 2)	15V
Input Voltage Range (Note 3)	−0.3V to +15V
Input Current ($V_{IN} \leq -0.3V$) (Note 4)	20 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics $V_S = 12V$, $R_{SET} = 680k$, $0°C \leq T_A \leq 70°C$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 5)		±3	±7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		100	400	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±30	±75	nA
Supply Current	$R_L = \infty$, $T_A = 25°C$ (Note 6)		3	6	mA
Output Voltage Swing	$V_S = \pm 6V$, $T_A = 25°C$ (Note 1)				
V_{OH}	$R_L = 50\Omega$	4.5	5		V
	$R_L = 8\Omega$	2			V
V_{OL}	$R_L = 50\Omega$		−5	−4.5	V
	$R_L = 8\Omega$			−2	V
Large Signal Voltage Gain	$V_S = \pm 6V$, $R_L = 50\Omega$, $f = 100$ Hz, $T_A = 25°C$	3	10		V/mV
Input Common-Mode Voltage Range	$V_S \leq 15V$, $T_A = 25°C$ (Note 3)	1		$V_S - 1.5$	V
Input Offset Voltage	(Note 5)			±10	mV
Input Offset Voltage Drift			5		μV/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			600	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA
Input Offset Current Drift			50		pA/°C
Supply Current	$R_L = \infty$ (Note 6)			8	mA
Output Voltage Swing	$V_S = \pm 6V$ (Note 1)				
V_{OH}	$R_L = 50\Omega$			4	V
	$R_L = 8\Omega$			1.6	V
V_{OL}	$R_L = 50\Omega$	−4			V
	$R_L = 8\Omega$	−1.6			V

Electrical Characteristics V_S = 12V, R_{SET} = 680k, 0°C ≤ T_A ≤ 70°C, unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Large Signal Voltage Gain	V_S = ±6V, R_L = 50Ω, f = 100 Hz	1			V/mV
Input Common-Mode Voltage Range	V_S ≤ 15V (Note 3)	1.25		V_S − 1.75	V
Common-Mode Rejection Ratio	T_A = 25°C	63	85		dB
Total Harmonic Distortion	R_L = 8Ω, V_O = 2 Vrms, f = 1 kHz, T_A = 25°C		0.5	5	%

Note 1: For operation at high temperatures, the LM13080 must be derated based upon a maximum junction temperature of 150°C and a thermal resistance of 100°C/W. The thermal resistance values given are for a still air ambient with the package soldered into a printed circuit board.

Note 2: Differential input voltages up to the magnitude of the power supply voltage will not damage the input circuitry. However, input voltages outside the input common-mode voltage range will not be able to properly control the output of the amplifier.

Note 3: The input voltage applied to either input should not be allowed to go more than 0.3V below the potential applied to pin 4; however, either input can be taken as high as 15V without causing damage to the circuit. Input voltages below the minimum common-mode voltage range may cause a phase reversal in the output.

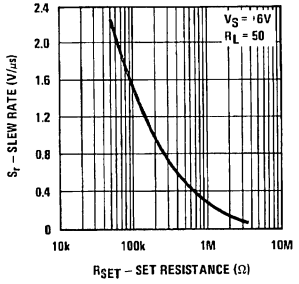
Note 4: This input current will exist only when the voltage at either input lead is driven negative. It is due to the base-isolation junction of the PNP transistor tub becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also lateral NPN parasitic action on the IC chip. This transistor action can cause the output to take an undefined state for the time duration that an input is driven negative.

Note 5: V_O = 6V, R_S = 0Ω, and over the full input common-mode voltage range.

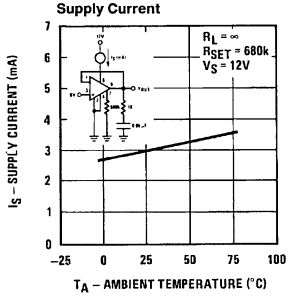
Note 6: Supply current is measured with the amplifier connected in a unity gain follower configuration and the positive input set to one-half of the supply voltage.

Typical Performance Characteristics

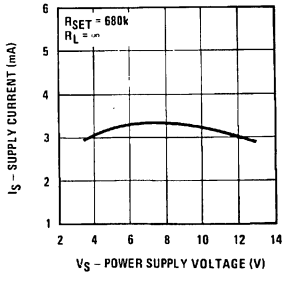
Slew Rate as Function of R_{SET}



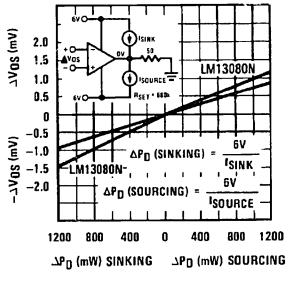
Supply Current



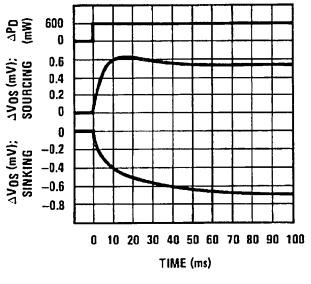
Supply Current



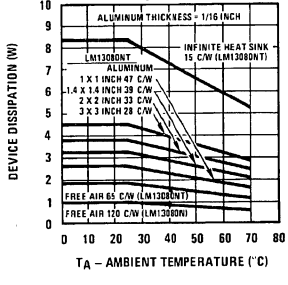
Offset Voltage Change vs Power Dissipation Due to Thermal Feedback



Thermal Feedback Time Constant



Device Dissipation vs Ambient Temperature



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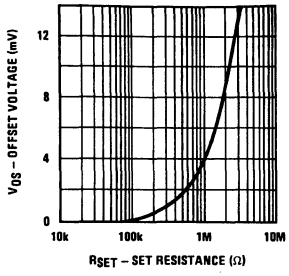
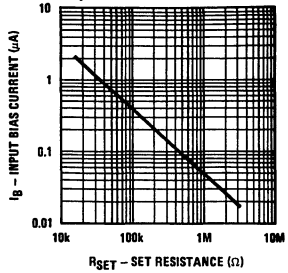
Typical Performance Characteristics (Continued)

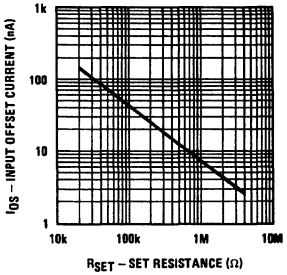
Offset Voltage



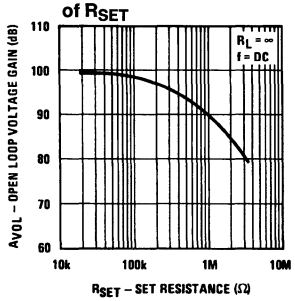
Input Bias Current



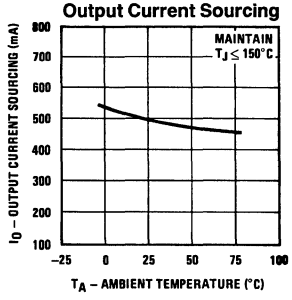
Offset Current



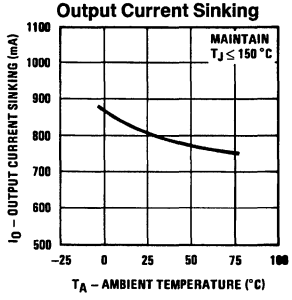
Voltage Gain as a Function of R_{SET}



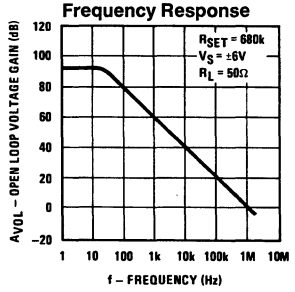
Output Current Sourcing



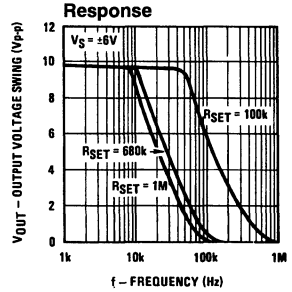
Output Current Sinking



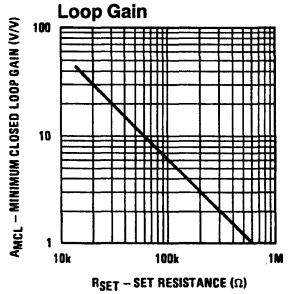
Small Signal Open Loop Frequency Response



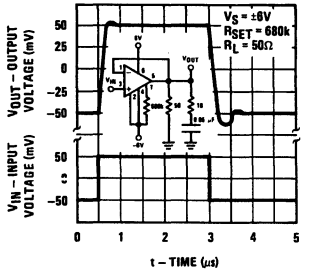
Large Signal Frequency Response



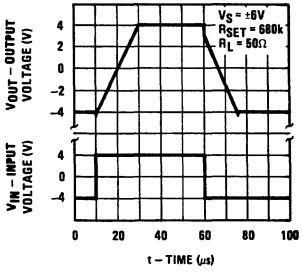
Minimum Stable Closed Loop Gain



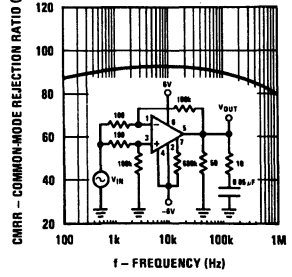
Voltage Follower Pulse Response (Small Signal)



Voltage Follower Pulse Response (Large Signal)



Common-Mode Rejection Ratio



TL/H/7978–3

Application Hints

The LM13080 is a power op amp capable of sourcing or sinking more than 250 mA and does not include internal current limit or thermal shut-down. Therefore, the user must make sure that his application will not cause the power dissipation rating of the package to be exceeded. The LM13080 is rated at a maximum dissipation of 1250 mW at 25°C. For operation at temperatures above 25°C, the maximum dissipation must be derated using the equation:

$$P_D = \frac{T_J - T_A}{\Theta_{JA}}$$

where P_D is the maximum allowable power dissipation, T_J is the maximum junction temperature (150°C), T_A is the ambient temperature and Θ_{JA} is the thermal resistance of the package operated in a still air environment. Θ_{JA} for the LM13080N is 100°C/W. For example, if the LM13080N is used in free air in a 70°C ambient, the maximum power that can be dissipated is:

$$P_D = \frac{150°C - 70°C}{100°C/W} = 800\ mW$$

The LM13080 derives its ability to sink current through the use of a composite NPN/PNP output configuration. This local loop must be compensated by the series connection of a 0.05 μF capacitor and a 10Ω resistor between the output of the op amp (pin 5) and the negative power supply (pin 4). The RC does not just filter out the oscillation from the output waveform but actually stabilizes the loop.

If the inputs of the LM13080 are driven below the input common-mode voltage range, it is possible that the output will experience a phase reversal. This is particularly true for the non-inverting input ($V_{IN(+)}$). If either input is driven to a voltage level 0.3V below the substrate (pin 4) a parasitic NPN transistor will be turned ON. The emitter of this parasitic transistor is the normal input transistor epi (N-type, base) region, the base is the substrate (P-type) and the collector is every other epi region on the die. Circuit operation in this mode is unpredictable. If an input is forced below the substrate, the current flowing out of that input should be limited to 20 mA to insure that the amplifier will not be destroyed.

Programming the LM13080 is accomplished by selecting the value of R_{SET}, the input stage bias resistor, to optimize the amplifier for each particular application. An example would be an application with low source resistance which requires a low offset voltage to make a precise DC measurement. By selecting an R_{SET} of 100 kΩ, the normal offset voltage would be reduced to approximately one-fourth the value it would be if a 680k resistor was used. By studying the curves, it can be seen that the bias current will increase but an increase here has very little effect due to the small source impedance. It should also be noted that with a 100k input set resistor the gain bandwidth product will also increase, and in fact, the amplifier must be operated with a closed loop voltage gain of 6 to assure stability.

The effect of R_{SET} on the total quiescent supply current will be very small ($\Delta I_S < 5\%\ I_S$) as long as R_{SET} is 100k or greater.

To employ electronic shut-down the output bias pin, pin 2, and the negative end of the input bias resistor, R_{SET}, are connected to the negative power supply (or ground in a single power system) through a saturated NPN transistor (or other electronic switch). When the transistor is turned OFF, all of the bias currents inside the op amp are turned OFF and all input and output terminals will float. When first turned ON, the output will take about 5 μs to reach the correct level. To insure that the LM13080 is OFF, leakage in the control device must be below the level that will allow pins 2 and 7 to fall to 0.4V below V^+.

Power supply rejection is a function of the change in voltage across the input bias resistor, R_{SET}. To improve the PSRR of the LM13080, the user must be careful to bypass pin 7 to pin 6 or to establish a floating voltage referenced to the positive power supply to serve as a connection point for R_{SET}. In applications where PSRR is important, it is imperative that a supply bypass capacitor(s) be used.

Typical Applications

LINE DRIVER

The line driver circuit in *Figure 1* is able to accept an unbalanced, high impedance input and convert it to a balanced output suitable for driving a low impedance line. This is particularly useful in an environment where magnetically induced hum or noise pickup is a problem.

The outputs of the 2 LM13080s are of opposite polarity; therefore, terminating the line with a balanced load (i.e., a differential amplifier or a transformer) will cause common-mode interference pickup to be cancelled.

This circuit will drive a 20 Vp-p signal into a 50Ω load for frequencies up to 10 kHz. Above 10 kHz the output signal is slew rate limited, but the line driver will still supply a 13 Vp-p signal at 20 kHz. The voltage gain of the network is 2, and the low frequency roll-off is determined by:

$$f_L = \frac{1}{2\pi RC}$$

It can be seen that if the load is connected directly between the outputs of the amplifiers, the line driver becomes a simple bridge amplifier capable of delivering 2W into a 16Ω load.

PIEZOELECTRIC ALARM

The piezoelectric alarm shown in *Figure 2* uses a 3-terminal transducer (Gulton 101FB or equivalent) to produce an 80 dB SPL alarm.

The transducer has a feedback terminal which is connected to the non-inverting input of the LM13080, causing oscillation at the resonant frequency of the piezoelectric crystal. The alarm can be controlled through the use of the electronic shut-down feature of the amplifier. The 100k resistor and 0.1 μF capacitor are used to provide a reference voltage at the inverting input and to keep the duty cycle of the crystal oscillation close to 50%. The RC time constant of this feedback network should be much greater than the time constant of the transducer.

Typical Applications (Continued)

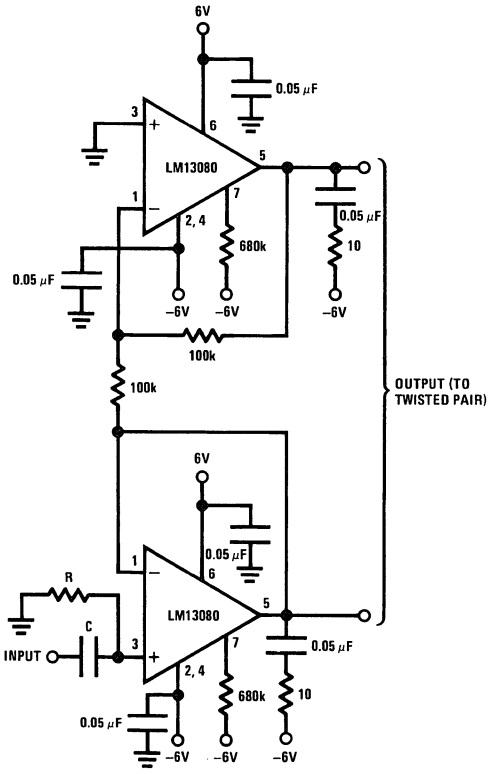


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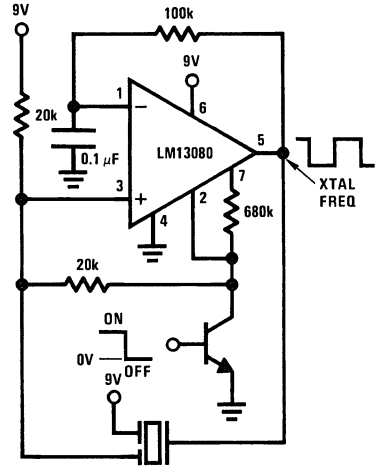
FIGURE 1. Line Driver—Unbalanced Input to Balanced Output



TL/H/7978–6

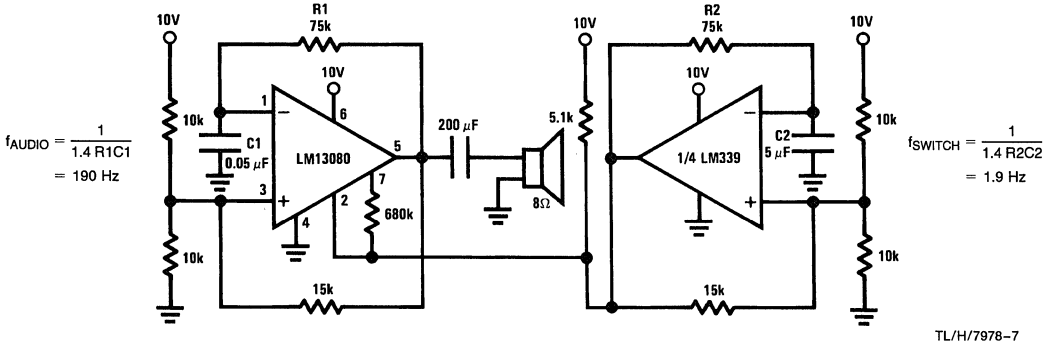
FIGURE 2. Piezoelectric Alarm

SIRENS

Two separate circuits for sirens are shown. The first, *Figure 3*, is a 2-state or ON-OFF type siren where the LM13080 oscillates at an audio frequency and drives an 8Ω speaker and the LM339 acts as a switch which controls the audio burst rate. The second siren, *Figure 4*, provides a constant audio output but alternates between 2 separate tones. The LM13080 is set to oscillate at one basic frequency and this frequency is changed by adding a 200 kΩ charging resistor in parallel with the feedback resistor, R2.

LAMP FLASHER—RELAY DRIVER

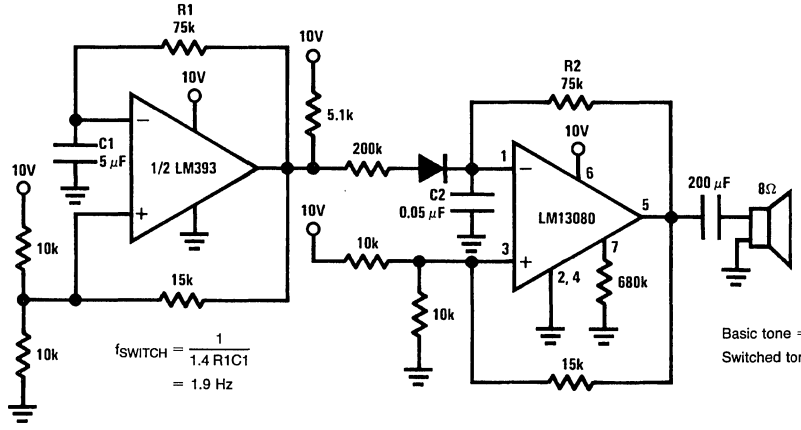
The LM13080 is easily adaptable to such applications as low frequency warning devices. The output of the oscillator is a squarewave that is used to drive lamps or small relays. As shown in *Figure 5*, the circuit alternately flashes 2 incandescent lamps.



TL/H/7978–7

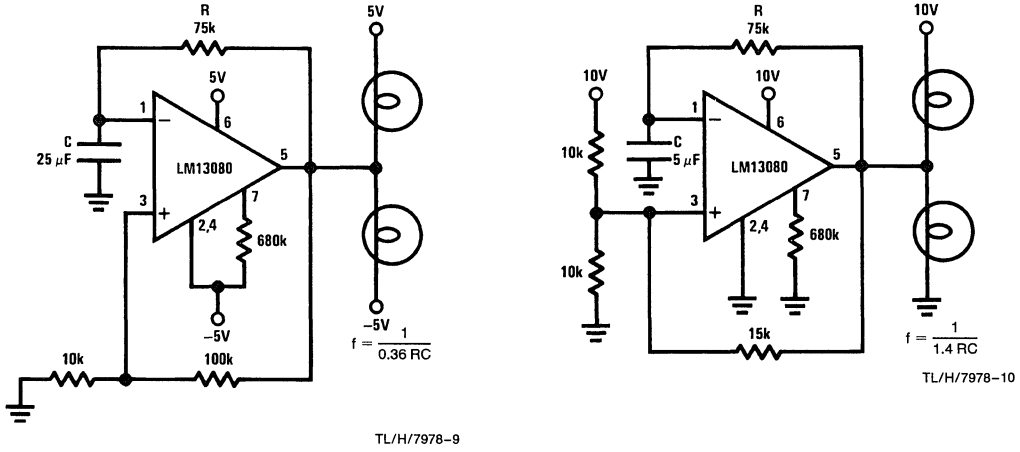
FIGURE 3. 2-State Siren

Typical Applications (Continued)



TL/H/7978–8

FIGURE 4. 2-Tone Siren



TL/H/7978–9

TL/H/7978–10

a) Split Supplies **b) Single Supply**

FIGURE 5. Low Frequency Lamp Flasher/Relay Driver

MOTOR SPEED CONTROL

The LM13080 can be used to construct a very simple speed control for small motors requiring less than 0.5A start current. This circuit operates by impressing the multiple of a reference voltage across the motor, and then varying the reference by means of a quasi-positive feedback to change the voltage across the motor any time the load on the motor changes.

To understand the circuit operation, it is easiest to let the voltage at the cathode of diode D1, *Figure 6*, be the input voltage, V_{IN}, to the system. Diode D1 is actually a level shift diode to bring V_{IN} into the common-mode range of the amplifier. A reference voltage is established by the combined voltage drop through the 10Ω potentiometer, R3 and the reference diode, D2 and is applied to the non-inverting input of the LM13080. Resistor R4 is a bias resistor used to keep D2 active. The 10k speed adjust potentiometer is 2 resistors in 1, where section R1 is the input resistance and section R2 is the negative feedback resistance. It can be seen that the voltage impressed across the motor is equal to:

$$V_{MOTOR} = \frac{(V_{BE2} + I_3R3)\,R2}{R1} + V_{BE}$$

Typical Applications (Continued)

The positive feedback is developed as a change in the voltage across R3 due to the change in the motor current caused by a variation in the motor's load. Resistor R3 is shown as a potentiometer so that the amount of positive feedback can be adjusted for smooth operation of the motor. Capacitor C1 and resistor R5 serve as a filter for the reference voltage at the non-inverting input of the amplifier.

VOLTAGE REGULATORS

In normal, positive or negative regulator application such as those shown in *Figure 7* and *Figure 8*, the LM13080 has 2 major advantages over standard operational amplifiers. The LM13080 has its own on-chip pass device and in addition can either sink or source 250 mA of load current.

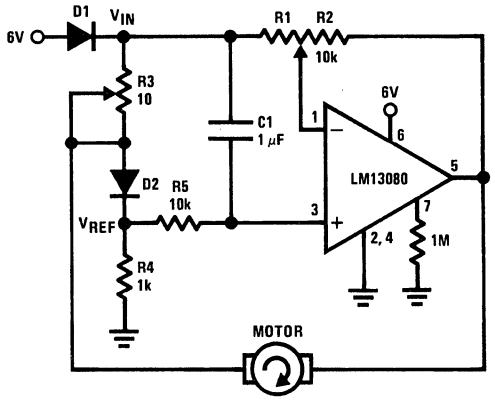


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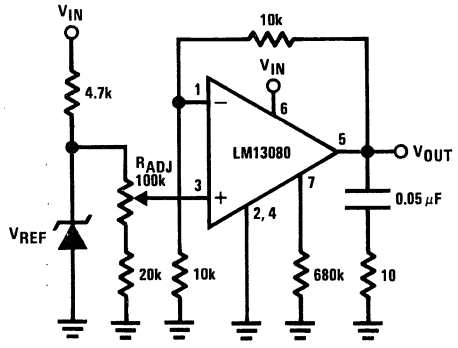
FIGURE 6. Motor Speed Control



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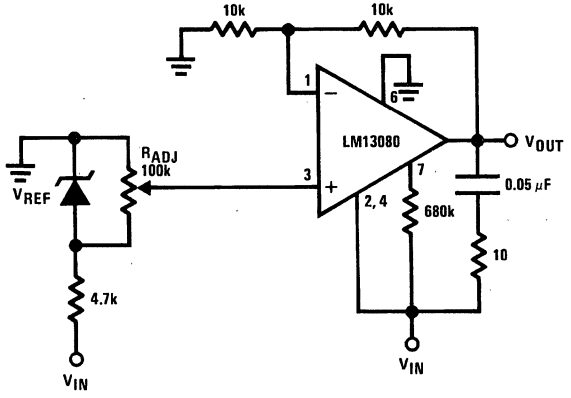
$2V \leq V_{OUT} \leq (V_{IN} - 2V)$

FIGURE 7. Positive Variable Voltage Regulator

Note: Pin numbers apply to miniDIP.



TL/H/7978–13

$-15V \geq V_{OUT} \geq -(V_{IN} - 2V)$

FIGURE 8. Negative Variable Voltage Regulator

National Semiconductor

LM13600/LM13600A
Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

Features

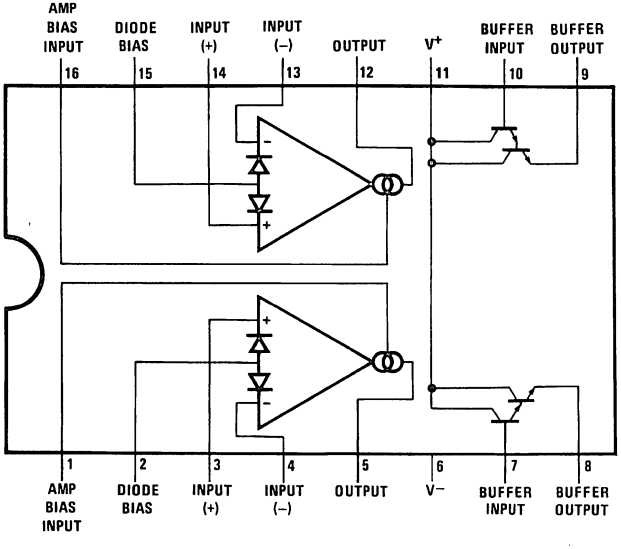
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio
- Wide supply range ±2V to ±22V

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7980–2

Top View

Order Number LM13600M, LM13600N or LM13600AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	
LM13600	36 V_{DC} or ±18V
LM13600A	44 V_{DC} or ±22V
Power Dissipation (Note 2) T_A = 25°C	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I_{ABC} = 5 μA		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			μmho
g_m Tracking			0.3			0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	R_L = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Supply Current	I_{ABC} = 500 μA, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100		0.2	5	nA

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Resistance		10	26		10	26		kΩ
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 5), Except I_{ABC} = 0 μA		0.2	0.4		0.2	0.4	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1: For selections to a supply voltage above ±22V, contact factory.

Note 2: For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

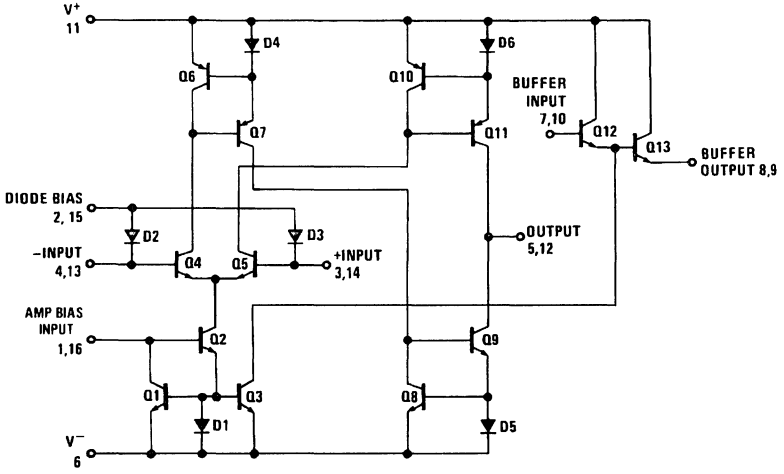
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for V_S = ±15V, I_{ABC} = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

One Operational Transconductance Amplifier



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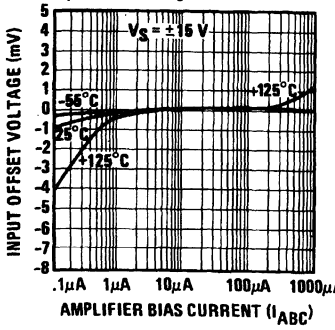
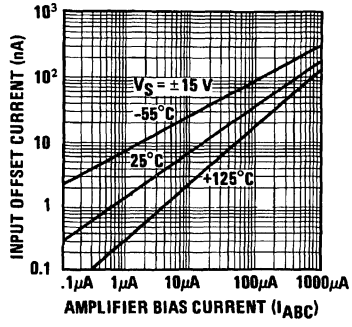
Typical Performance Characteristics

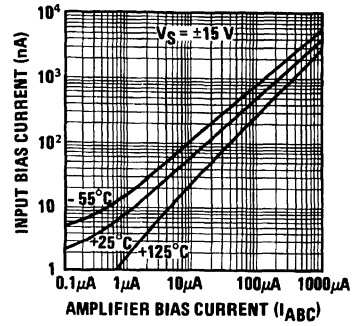
Input Offset Voltage



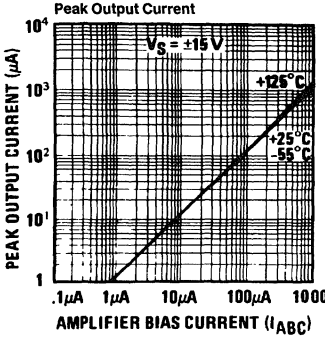
Input Offset Current



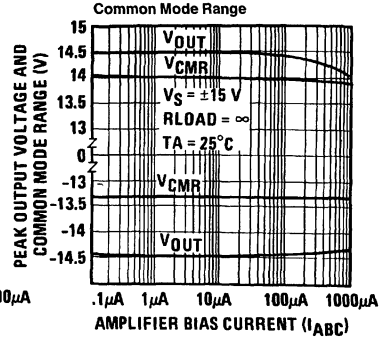
Input Bias Current



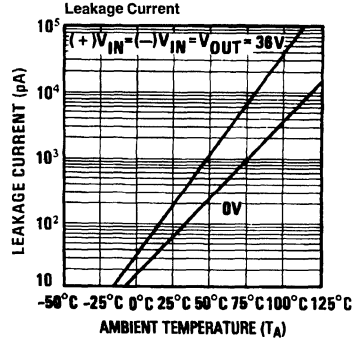
Peak Output Current



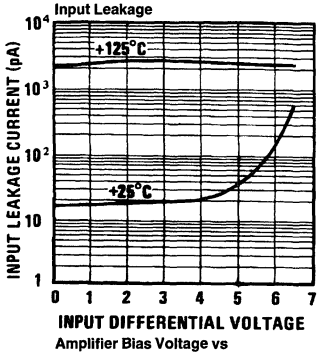
Peak Output Voltage and Common Mode Range



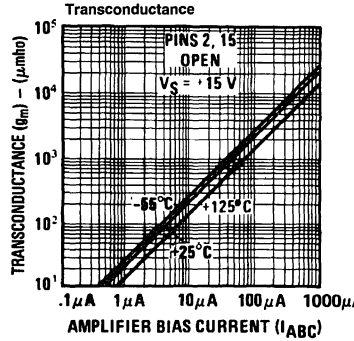
Leakage Current



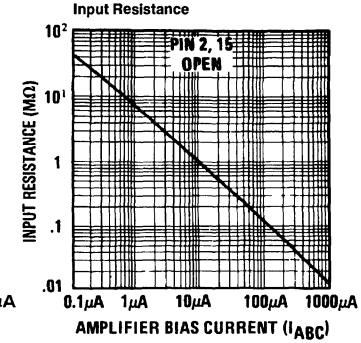
Input Leakage



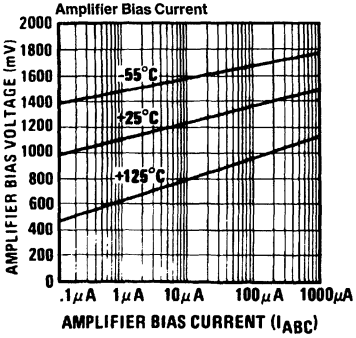
Transconductance



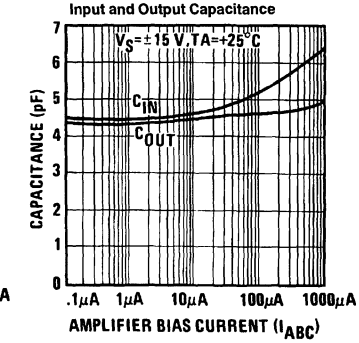
Input Resistance



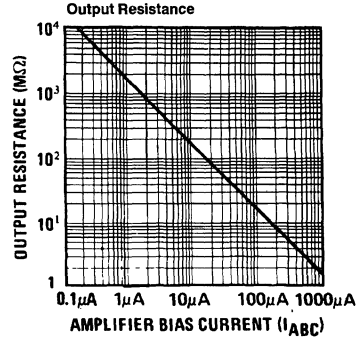
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance



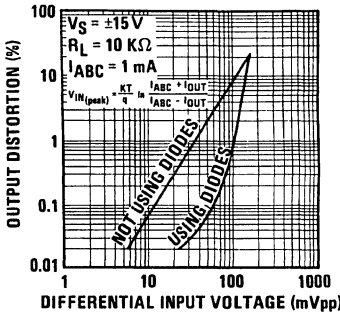
Output Resistance



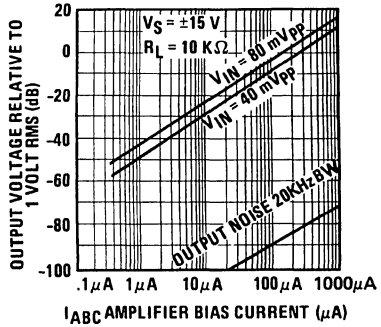
TL/H/7980–3

Typical Performance Characteristics (Continued)

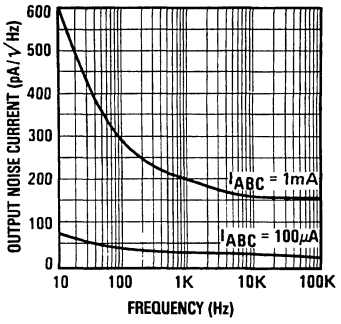
Distortion vs Differential Input Voltage



Voltage vs Amplifier Bias Current

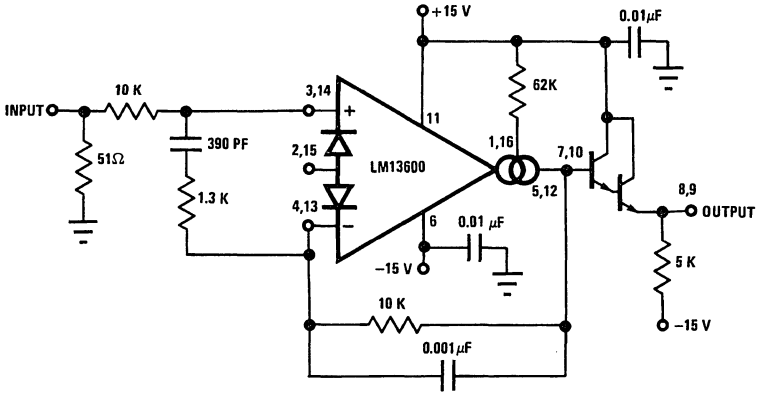


Output Noise vs Frequency



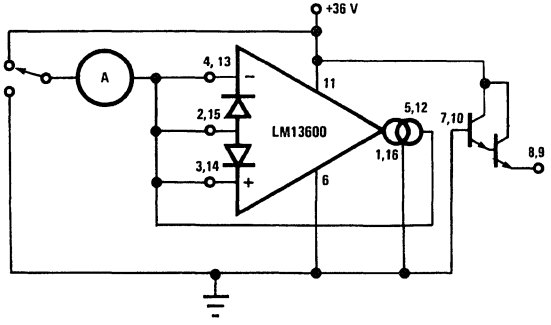
TL/H/7980–4

Unity Gain Follower

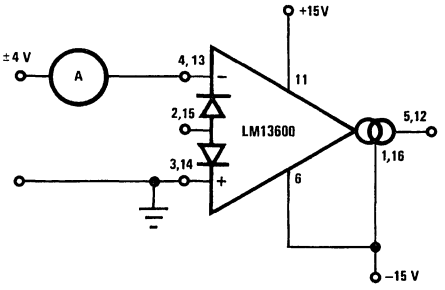


TL/H/7980–5

Leakage Current Test Circuit



Differential Input Current Test Circuit



TL/H/7980–7

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Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_5 - I_4 \quad (5)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \; I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \quad (6)$$

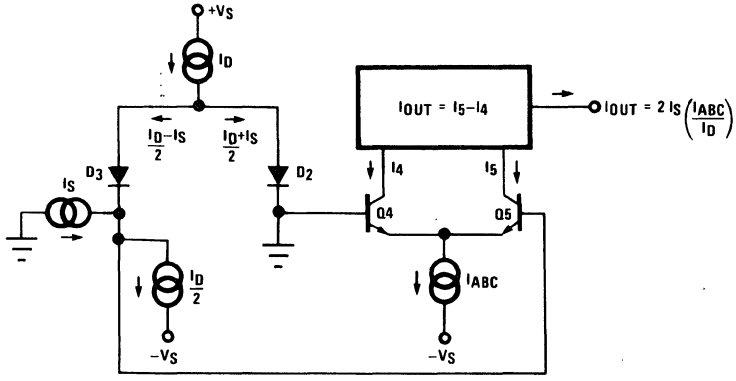

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FIGURE 1. Linearizing Diodes

Linearizing Diodes (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. An FET follower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC}, transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate. When I_{ABC} is changed, the DC level of the Darlington output buffer will shift. In audio applications where I_{ABC} is changed suddenly, this shift may produce an audible "pop". For these applications the LM13700 may produce superior results.

Applications—Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

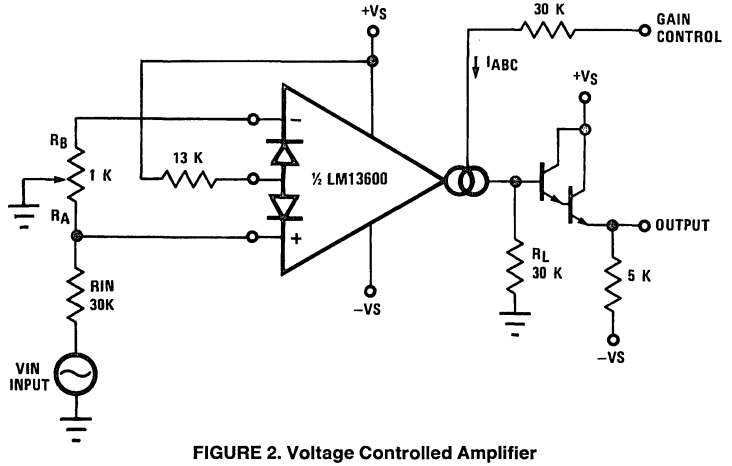


FIGURE 2. Voltage Controlled Amplifier TL/H/7980–9

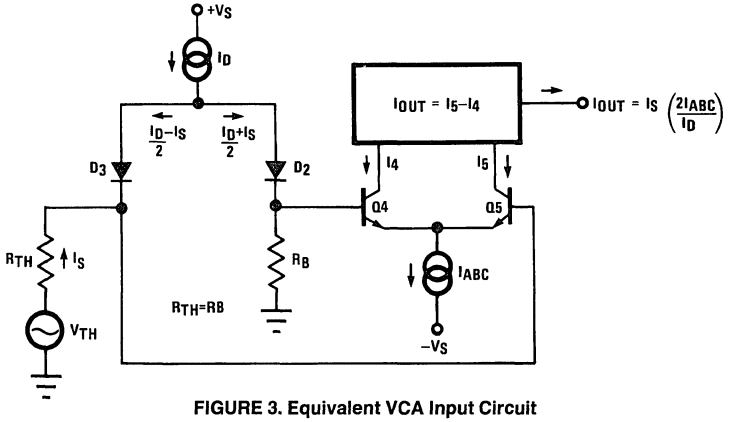


FIGURE 3. Equivalent VCA Input Circuit TL/H/7980–10

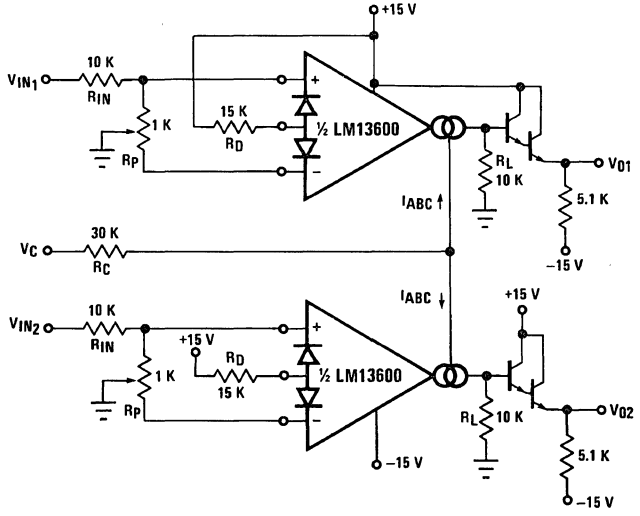
Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$



TL/H/7980–11

FIGURE 4. Stereo Volume Control

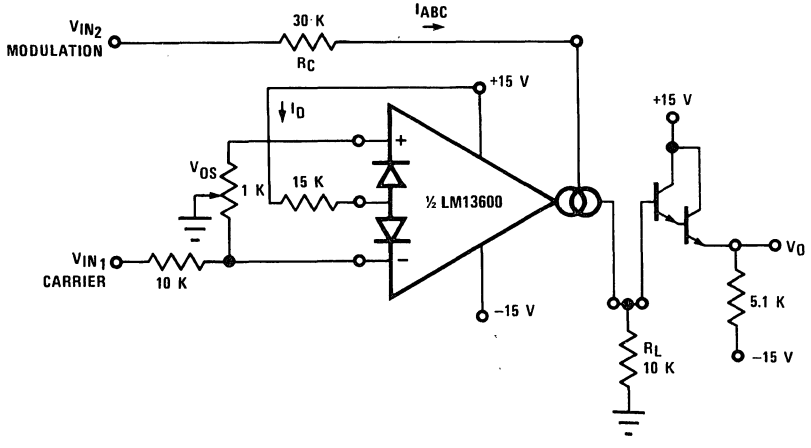


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FIGURE 5. Amplitude Modulator

Stereo Volume Control (Continued)

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2$ ($V^- + 1.4V$) into I_O. The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13600 amplifier of *Figure 3* may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, *Figure 7* shows as AGC Amplifier using this approach. As V_O reaches a high enough amplitude (3 V_{BE}) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2\, I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.

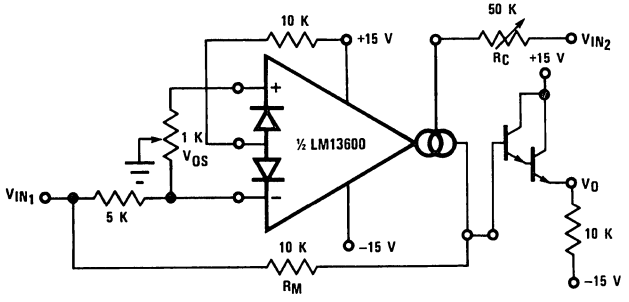

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FIGURE 6. Four-Quadrant Multiplier

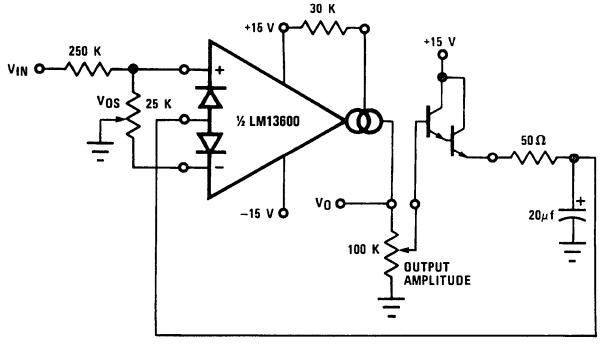

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FIGURE 7. AGC Amplifier

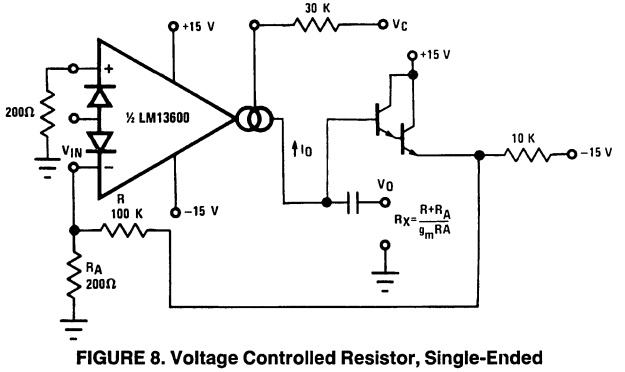

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FIGURE 8. Voltage Controlled Resistor, Single-Ended

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again $19.2 \times I_{ABC}$ at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

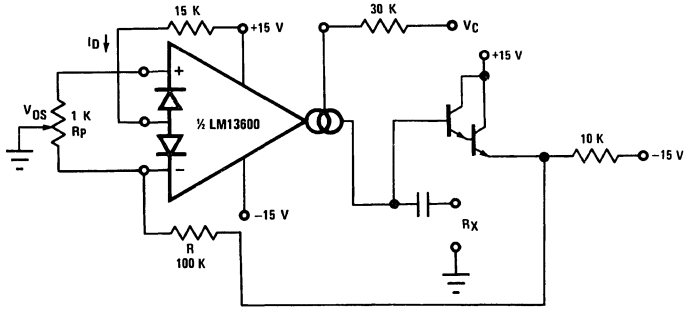

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FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

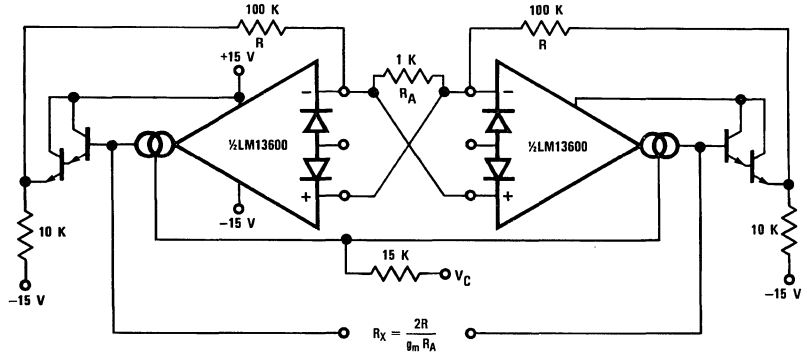

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FIGURE 10. Floating Voltage Controlled Resistor

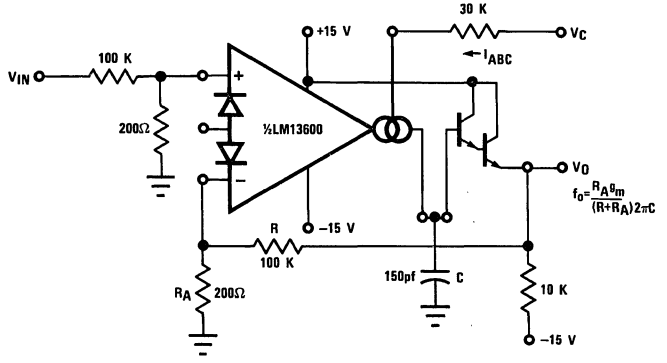

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FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)

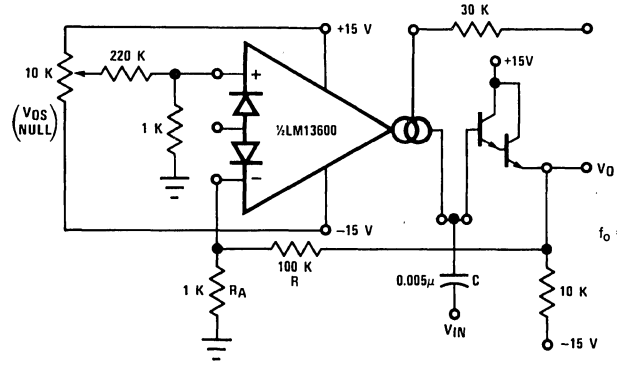

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FIGURE 12. Voltage Controlled Hi-Pass Filter

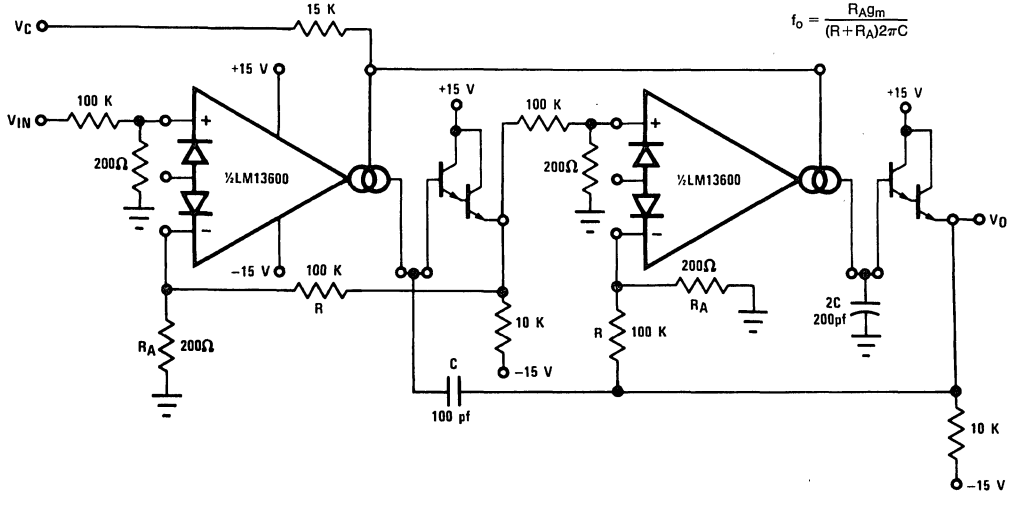

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FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

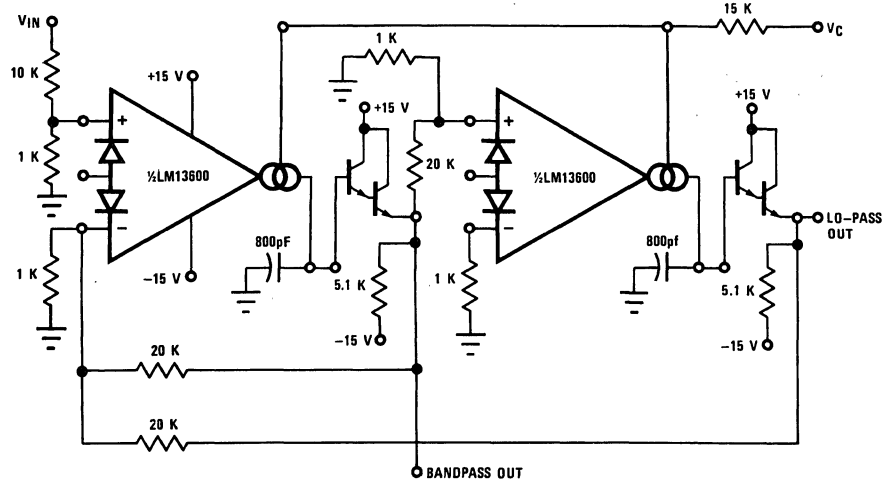

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FIGURE 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

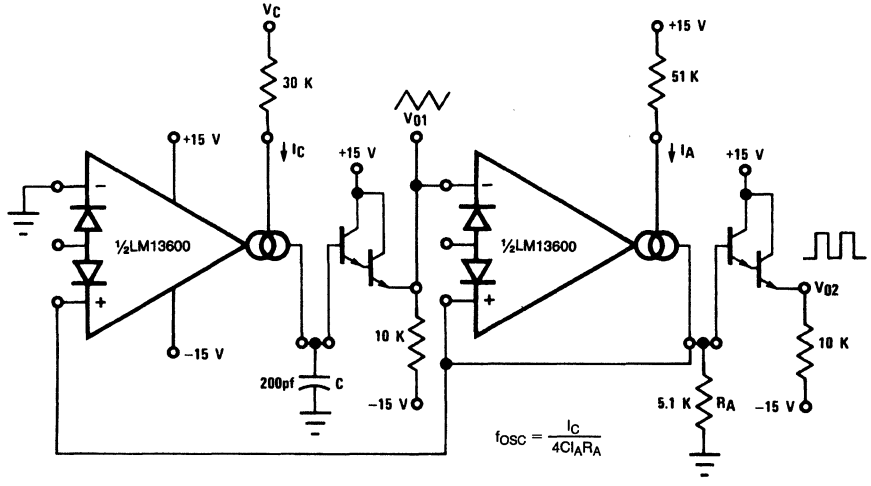

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FIGURE 15. Triangular/Square-Wave VCO

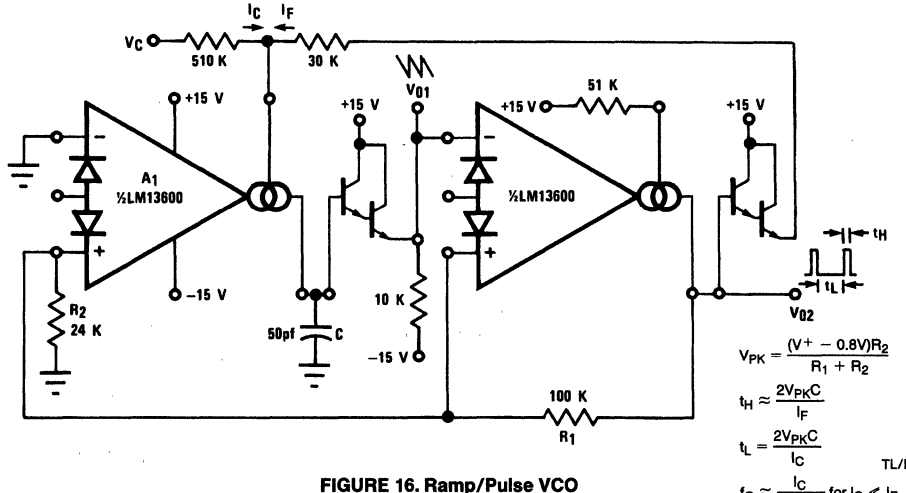

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FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)

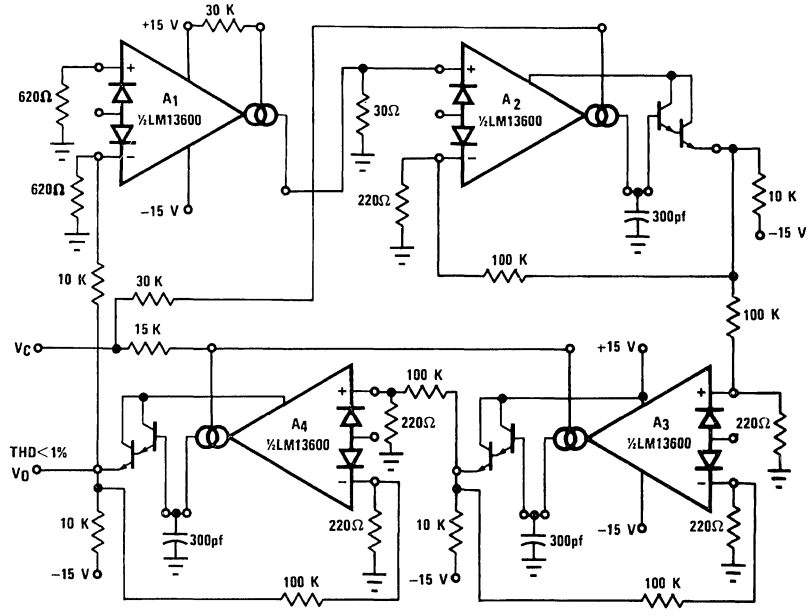

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FIGURE 17. Sinusoidal VCO

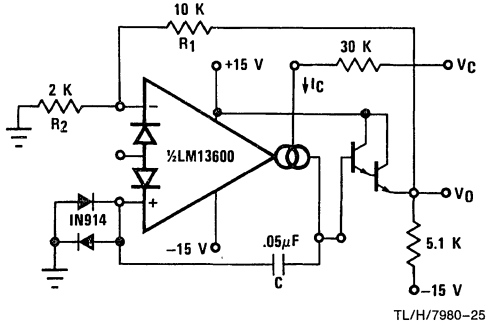

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FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so than an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13600 slew rate into 150 pF when the (V_{IN1}-V_{IN2}) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

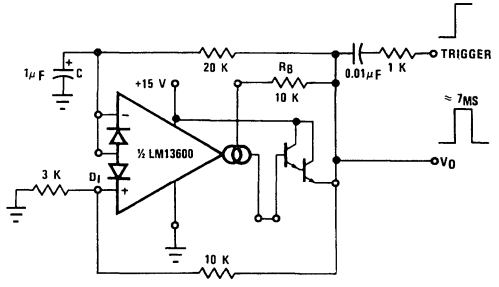

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FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)

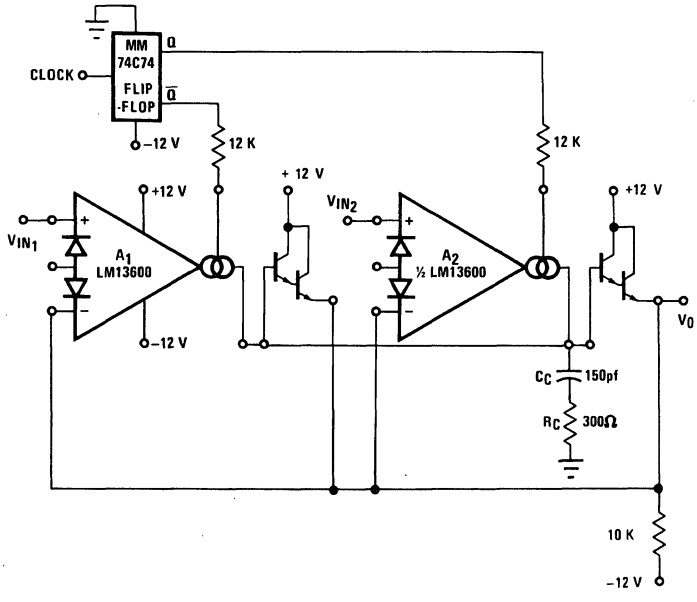

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FIGURE 20. Multiplexer

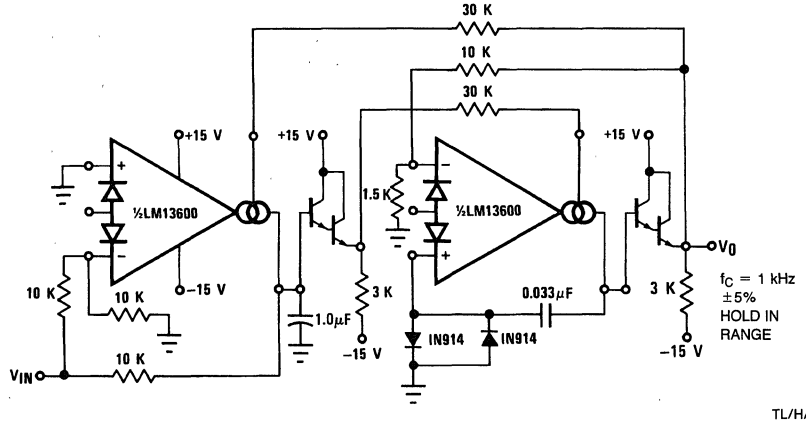

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FIGURE 21. Phase Lock Loop

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\, C_t$ is sourced into C_f and R_t. This once-per-cycle charge is then balanced by the current of V_O/R_t. The maximum f_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to $V_{IN}PK$. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)

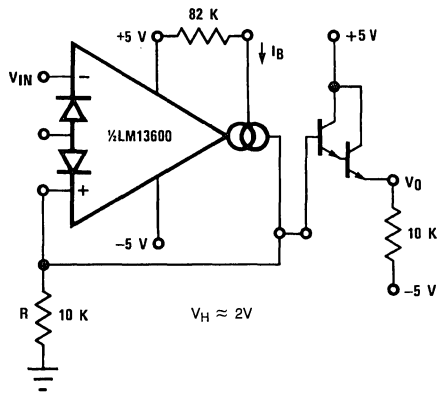

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FIGURE 22. Schmitt Trigger

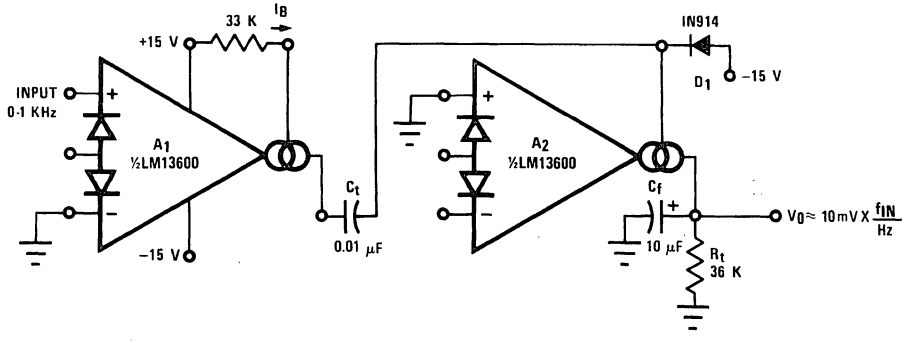

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FIGURE 23. Tachometer

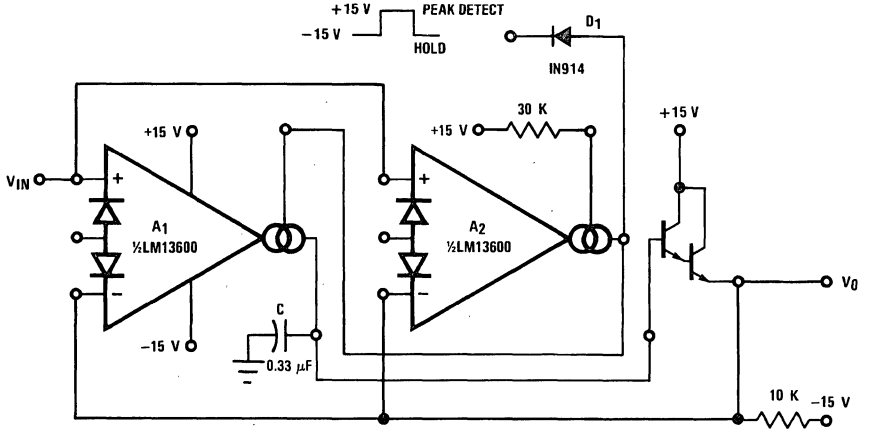

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FIGURE 24. Peak Detector and Hold Circuit

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Additional Applications (Continued)

The Sample-Hold circuit of *Figure 25* also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

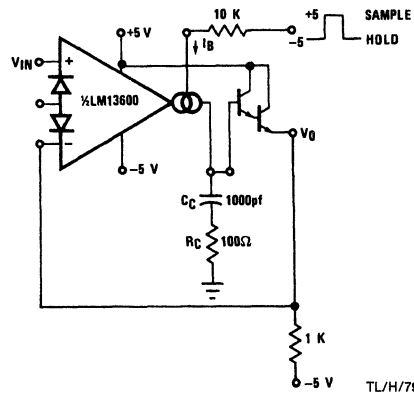

FIGURE 25. Sample-Hold Circuit

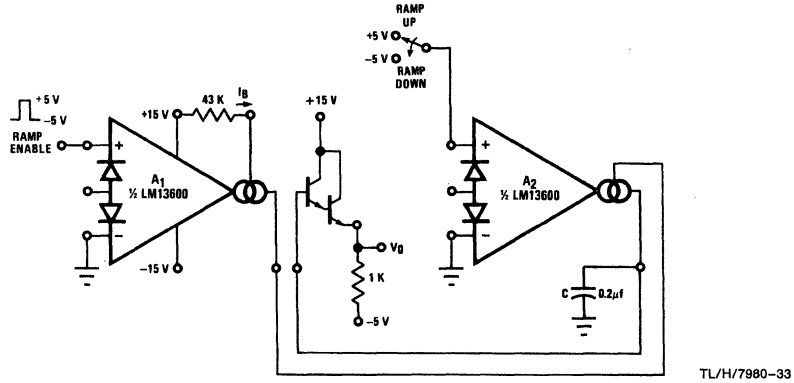

FIGURE 26. Ramp and Hold

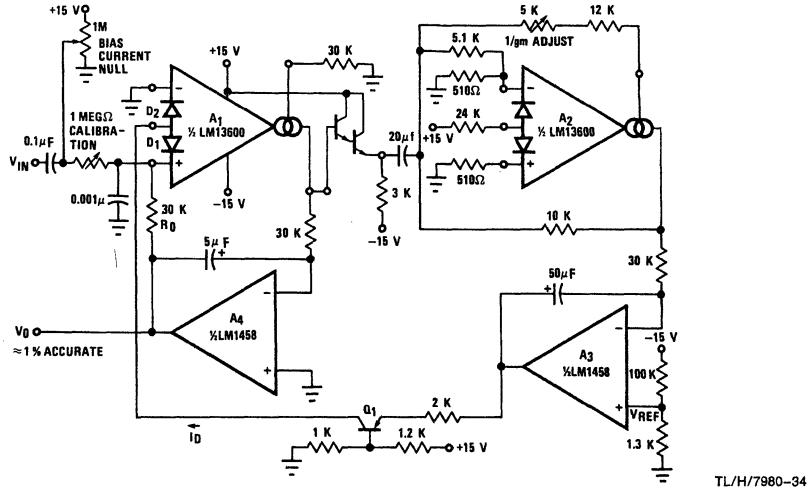

FIGURE 27. True RMS Converter

Additional Applications (Continued)

The circuit of *Figure 28* is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of *Figure 29* responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 30.*

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 31* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1+R_2)\,V_{IN}1}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_B1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp\left[\frac{2(R_1+R_2)\,V_C}{R_1I_2R_C}\right]$$

This logarithmic current can be used to bias the circuit of *Figure 4* provide a temperature independent stereo attenuation characteristic.

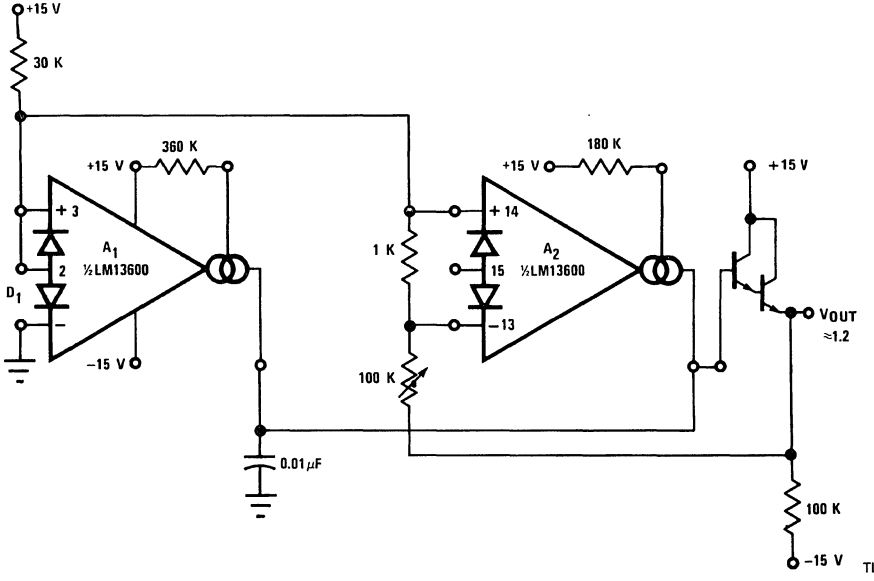

FIGURE 28. Delta VBE Reference

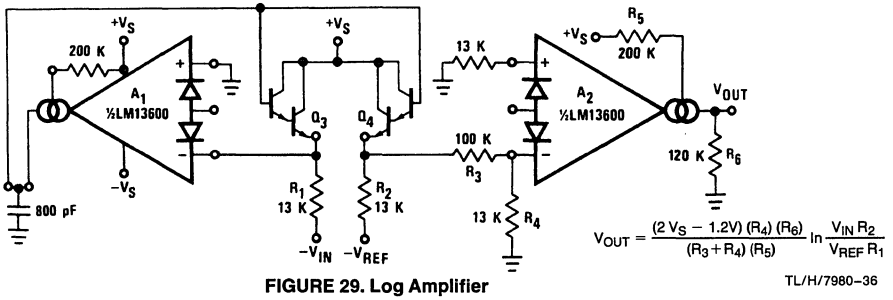

FIGURE 29. Log Amplifier

Additional Applications (Continued)

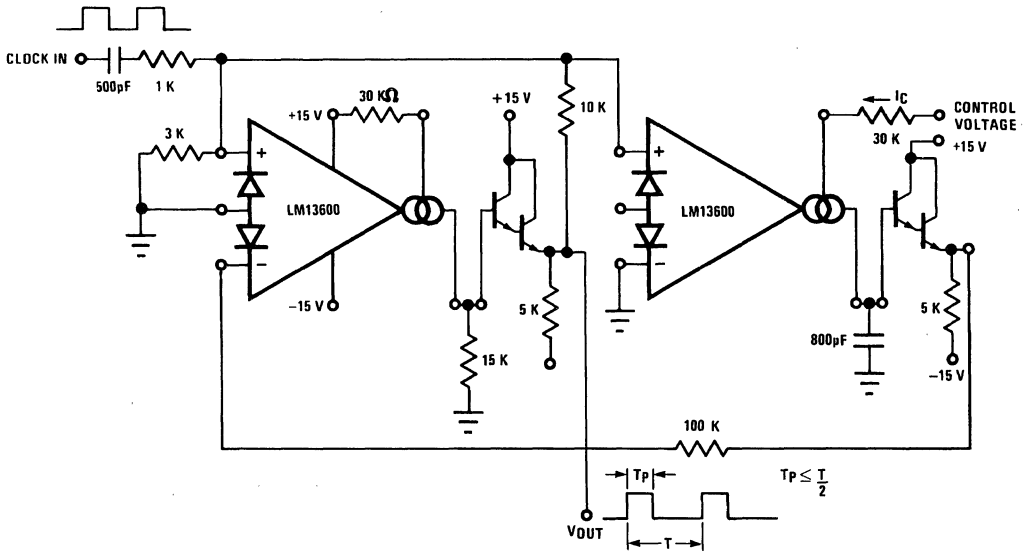

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FIGURE 30. Pulse Width Modulator

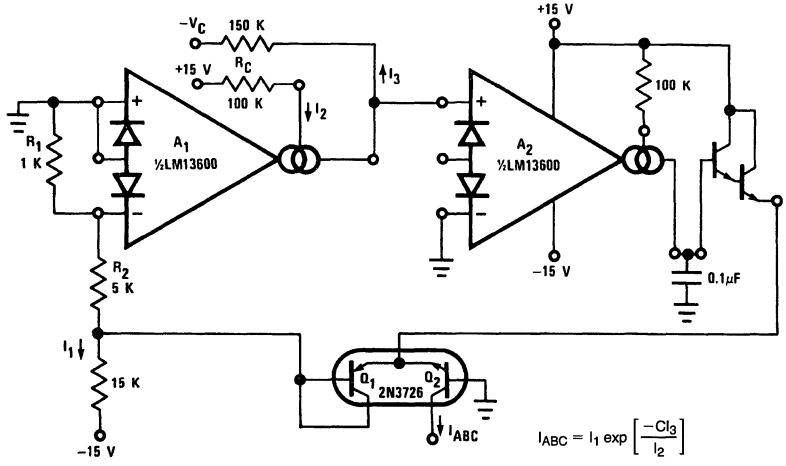

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FIGURE 31. Logarithmic Current Source

National Semiconductor

LM13700/LM13700A
Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of I_{ABC}. This may result in performance superior to that of the LM13600 in audio applications.

Features

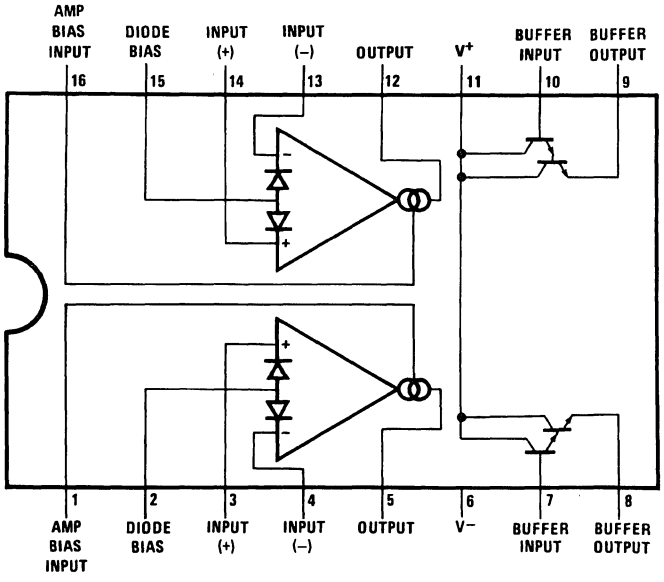
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio
- Wide supply range ±2V to ±22V

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

Connection Diagram

Dual In-Line and Small Outline Packages



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Top View

Order Number LM13700M, LM13700N or LM13700AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	
LM13700	36 V_{DC} or ±18V
LM13700A	44 V_{DC} or ±22V
Power Dissipation (Note 2) T_A = 25°C	
LM13700N, LM13700AN	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13700N, LM13700AN	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM13700			LM13700A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	
	I_{ABC} = 5 μA		0.3	4		0.3	1	
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current	Over Specified Temperature Range		0.4	5		0.4	5	μA
			1	8		1	7	
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			
g_m Tracking			0.3			0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	
	R_L = 0, Over Specified Temp Range	300			300			
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Supply Current	I_{ABC} = 500 μA, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V^+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V^-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		kΩ

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM13700			LM13700A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 5)		0.5	2		0.5	2	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1: For selections to a supply voltage above ±22V, contact factory.

Note 2: For operation at ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W; LM13700M, 110°C/W.

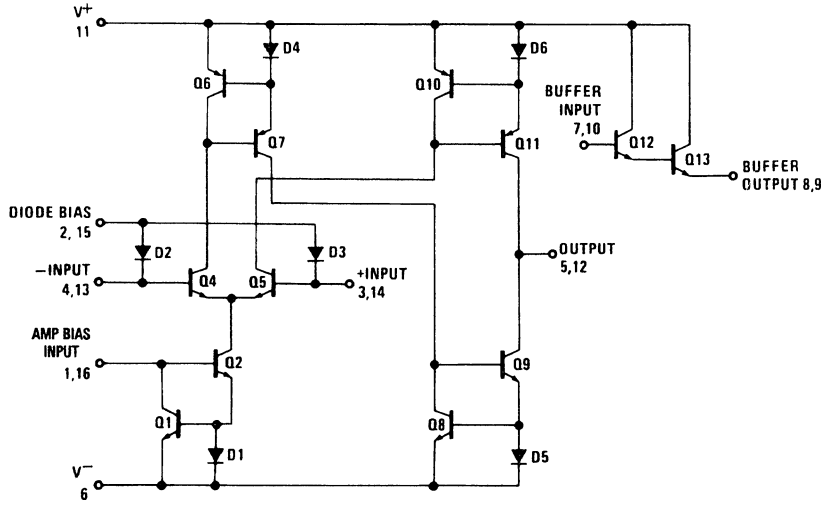
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500$ μA, $R_{OUT} = 5$ kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

One Operational Transconductance Amplifier



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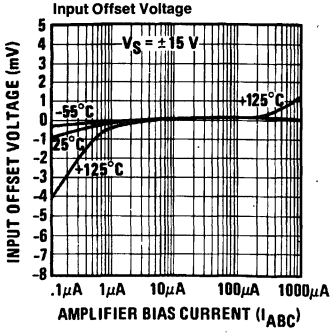
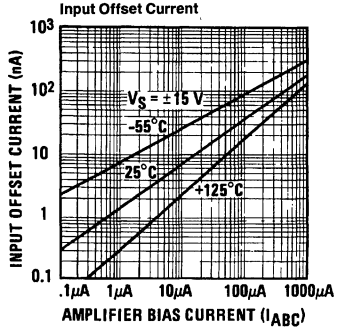
Typical Performance Characteristics

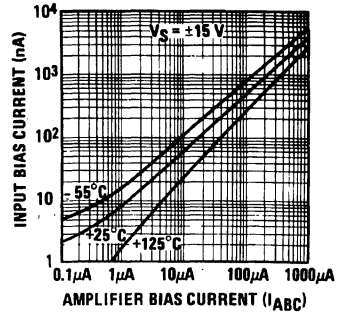
Input Offset Voltage



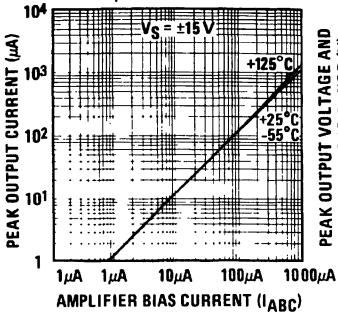
Input Offset Current



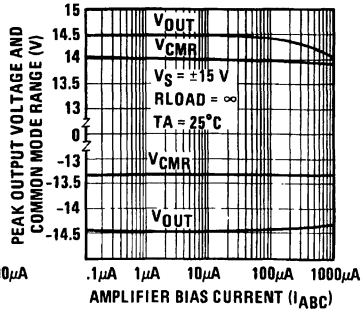
Input Bias Current



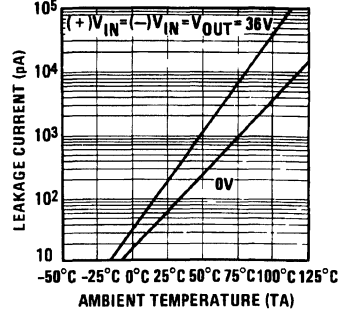
Peak Output Current



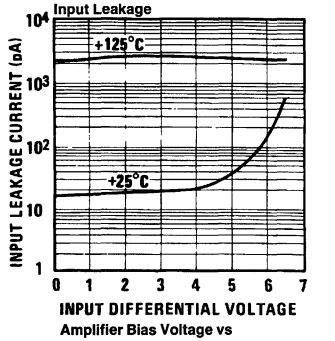
Peak Output Voltage and Common Mode Range



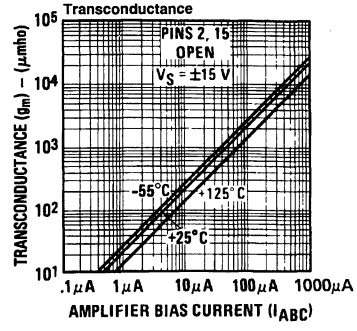
Leakage Current



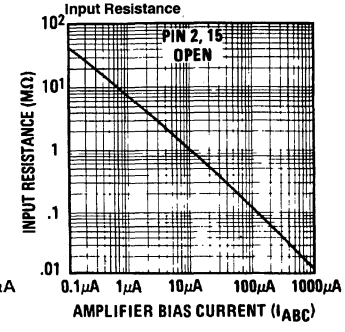
Input Leakage



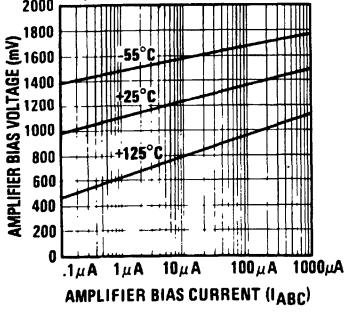
Transconductance



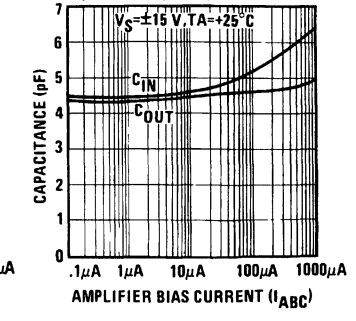
Input Resistance



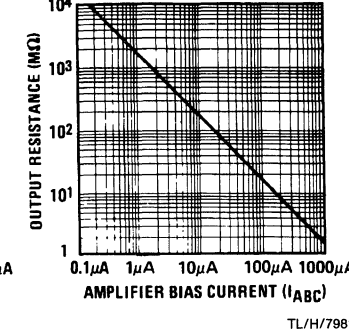
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance



Output Resistance



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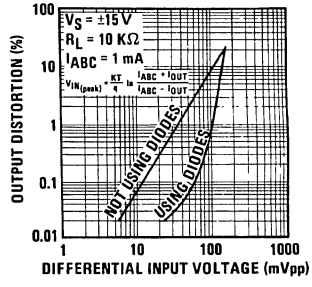
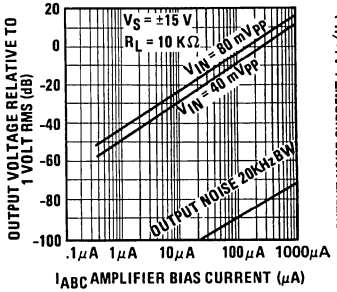
Typical Performance Characteristics (Continued)

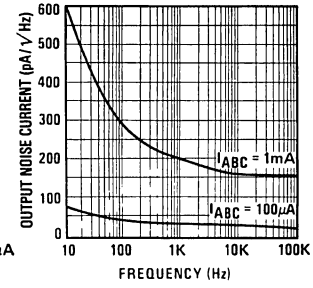
Distortion vs Differential Input Voltage



Voltage vs Amplifier Bias Current

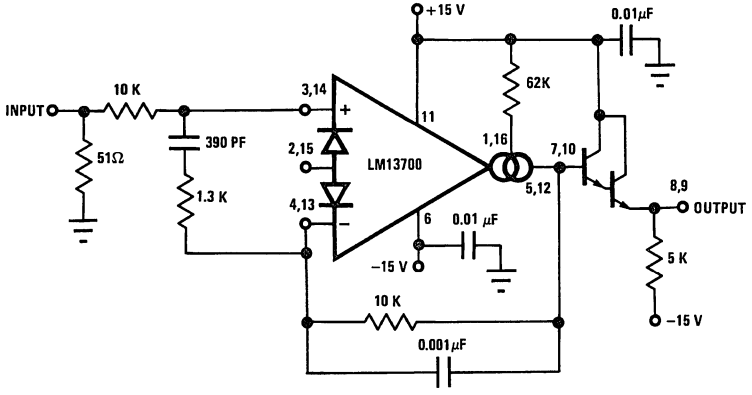


Output Noise vs Frequency



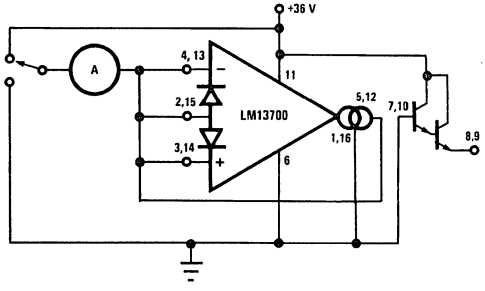
TL/H/7981–4

Unity Gain Follower



TL/H/7981–5

Leakage Current Test Circuit



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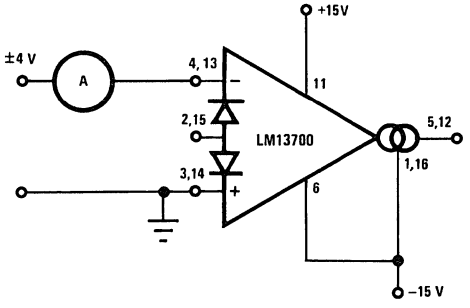
Differential Input Current Test Circuit



TL/H/7981–7

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{I_{ABC}q}{2kT}\right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

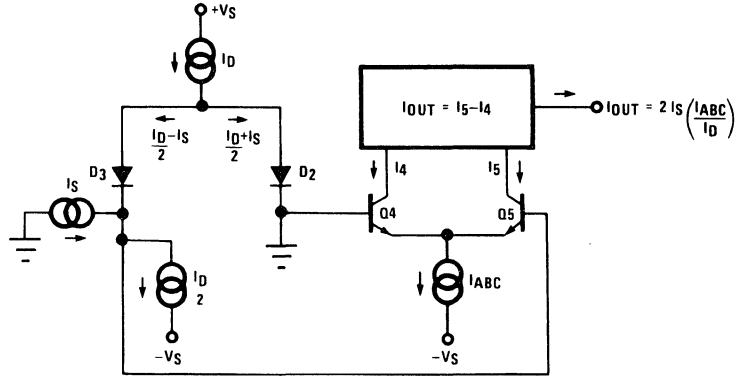
$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S\left(\frac{2I_{ABC}}{I_D}\right) \text{ for } |I_S| < \frac{I_D}{2} \quad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Applications: Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.



TL/H/7981–8

FIGURE 1. Linearizing Diodes

Applications:
Voltage Controlled Amplifiers (Continued)

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

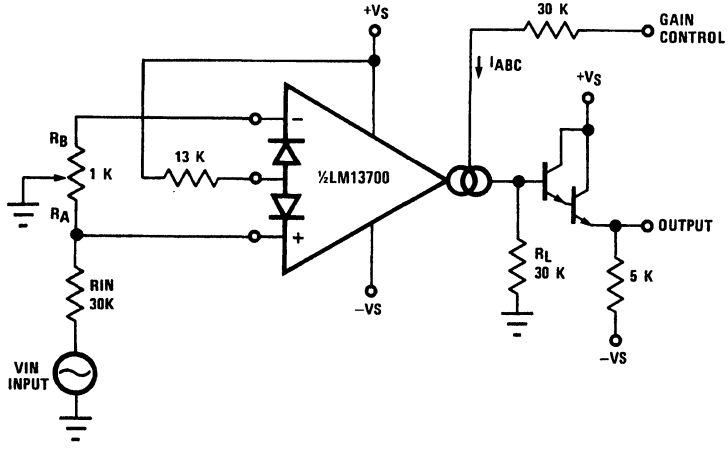


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FIGURE 2. Voltage Controlled Amplifier

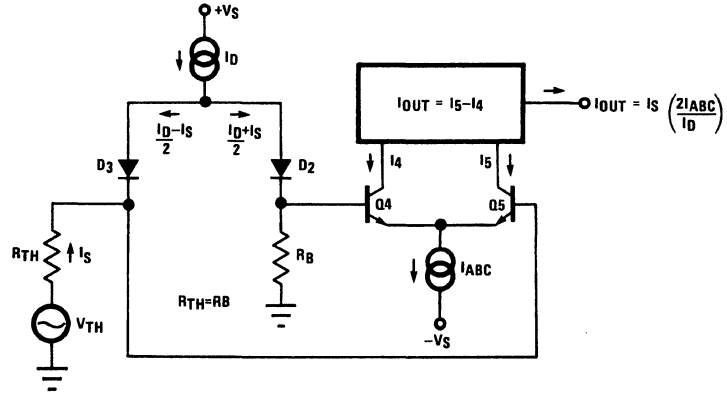

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FIGURE 3. Equivalent VCA Input Circuit

Stereo Volume Control

The circuit of *Figure 4* uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2(V^- + 1.4V)$ into I_O. The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

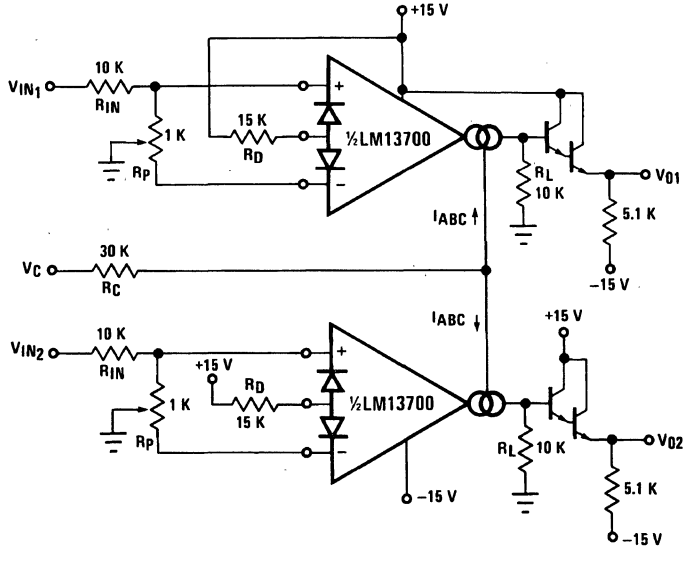

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FIGURE 4. Stereo Volume Control

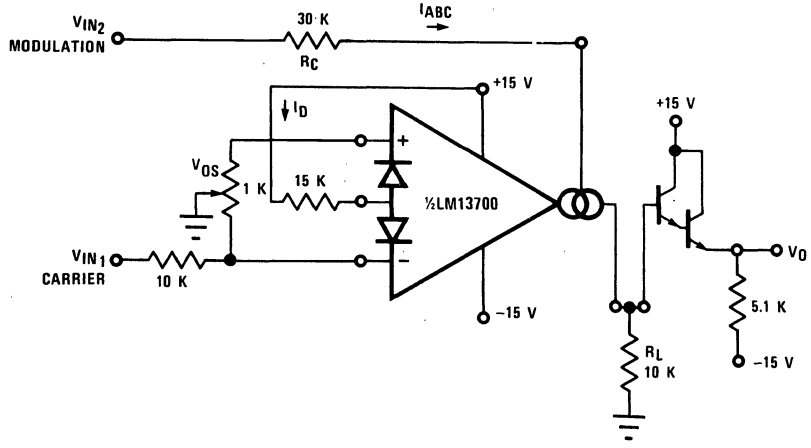

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FIGURE 5. Amplitude Modulator

Stereo Volume Control (Continued)

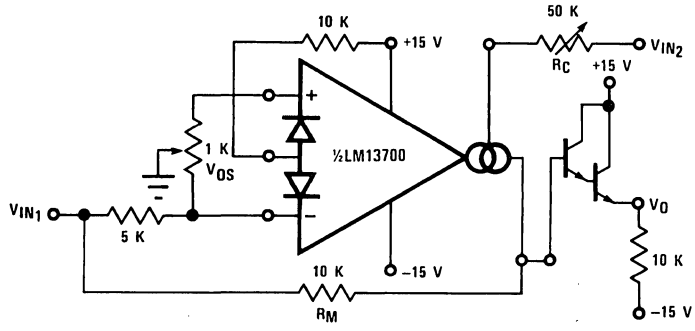

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FIGURE 6. Four-Quadrant Multiplier

Noting that the gain of the LM13700 amplifier of *Figure 3* may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, *Figure 7* shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at R_X generates a V_{IN} to the LM13700 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13700 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13700.

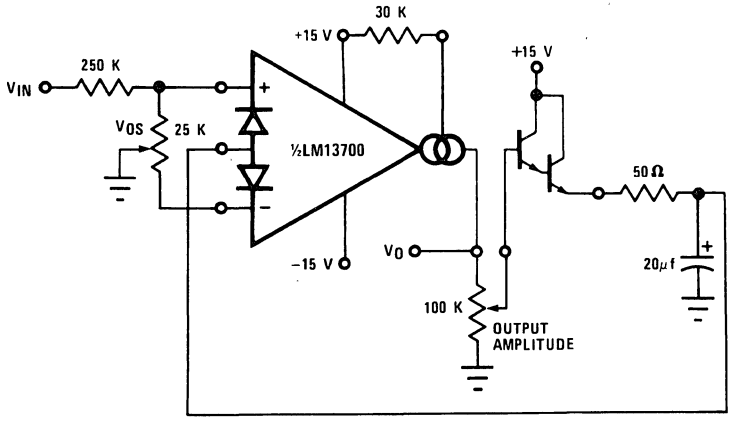

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FIGURE 7. AGC Amplifier

Voltage Controlled Resistors (Continued)

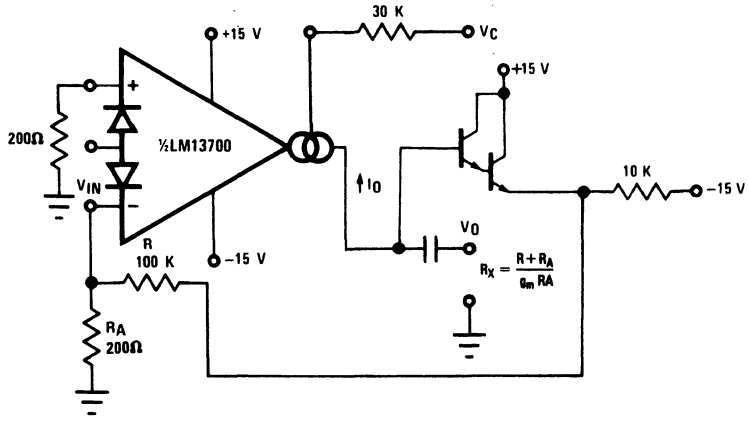

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FIGURE 8. Voltage Controlled Resistor, Single-Ended

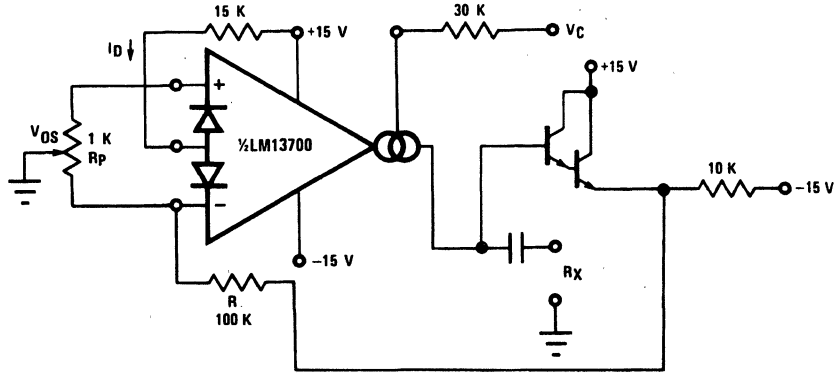

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FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again 19.2 × I_{ABC} at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent g_m tracking of the two amplifiers, these filters perform well over several decades of frequency.

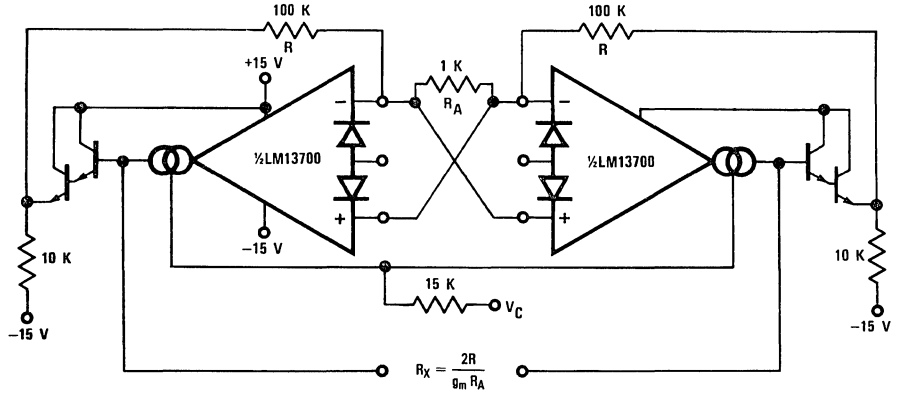

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FIGURE 10. Floating Voltage Controlled Resistor

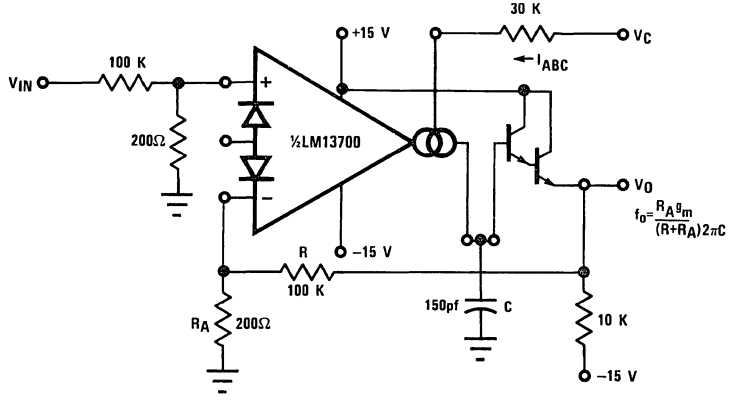

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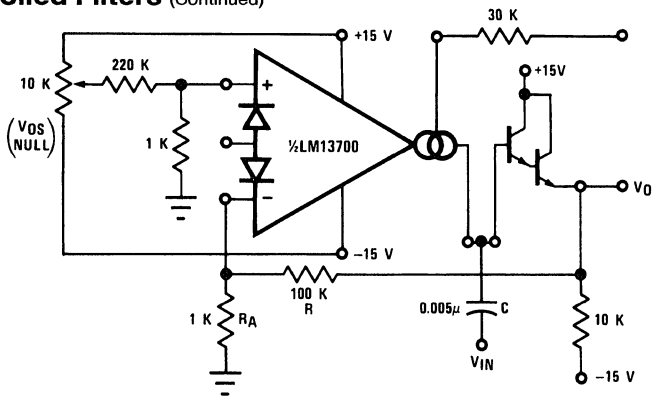
FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)



$$f_o = \frac{R_A g_m}{(R + R_A)\,2\pi C}$$

FIGURE 12. Voltage Controlled Hi-Pass Filter

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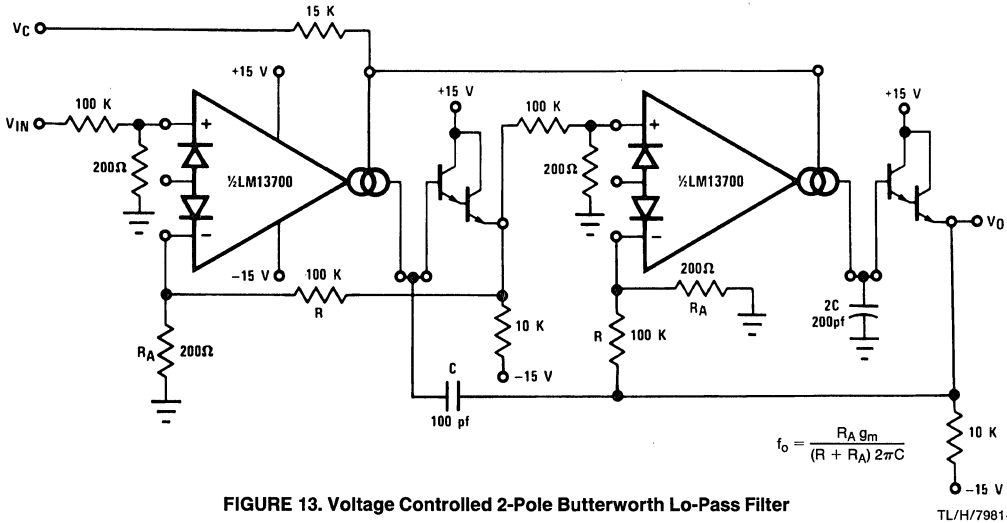

$$f_o = \frac{R_A g_m}{(R + R_A)\,2\pi C}$$

FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

TL/H/7981–20

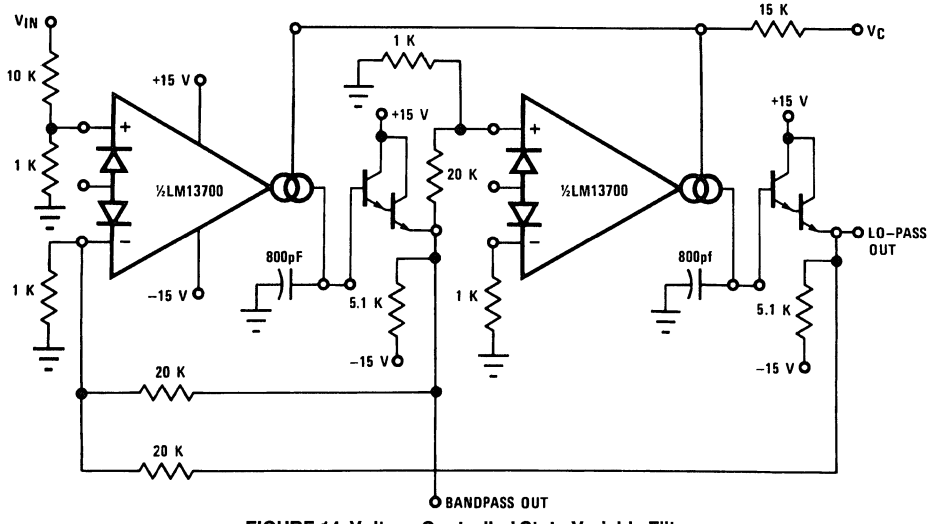

FIGURE 14. Voltage Controlled State Variable Filter

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Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

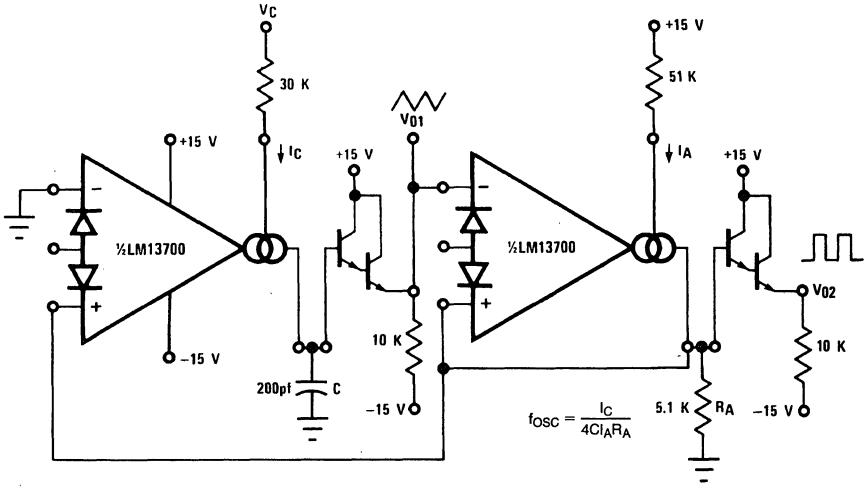

FIGURE 15. Triangular/Square-Wave VCO

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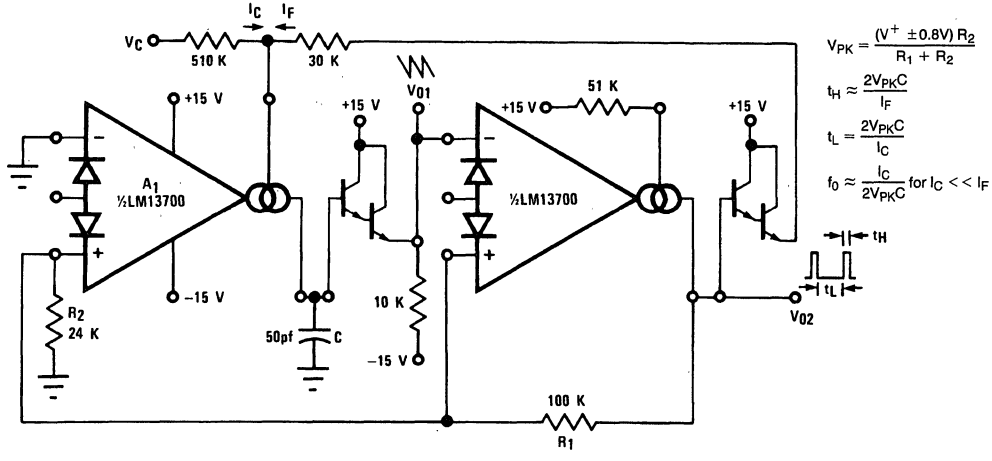

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FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)

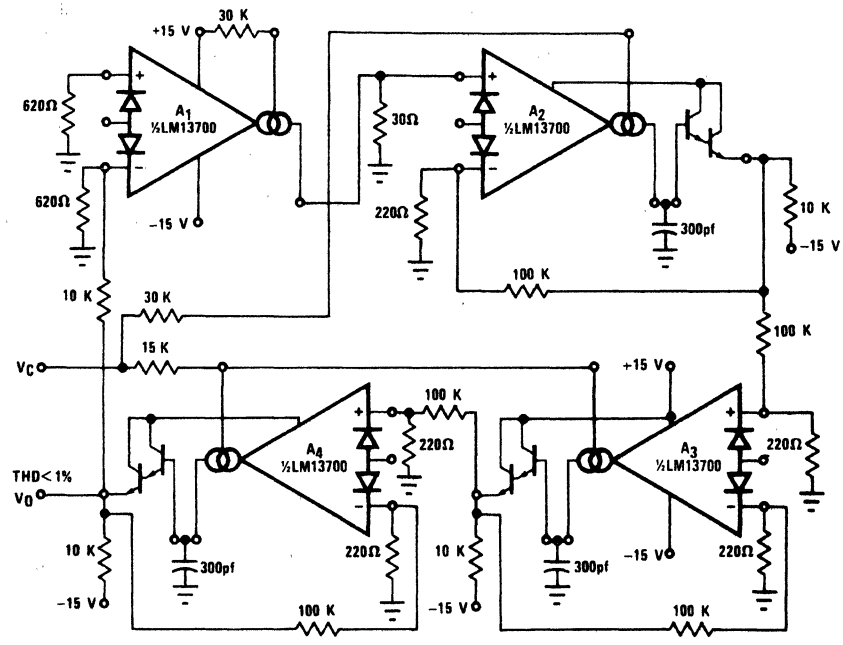

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FIGURE 17. Sinusoidal VCO

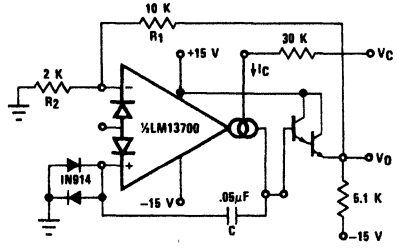

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FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

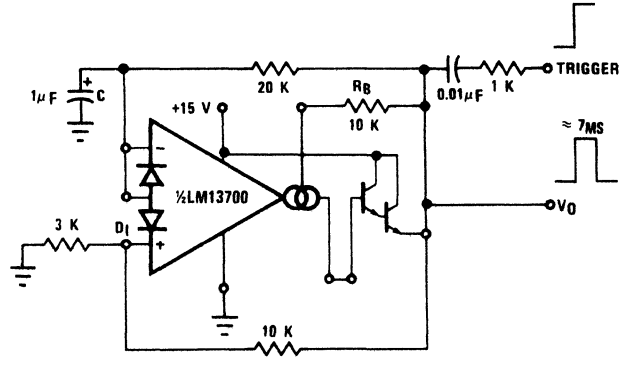

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FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the ($V_{IN1}-V_{IN2}$) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

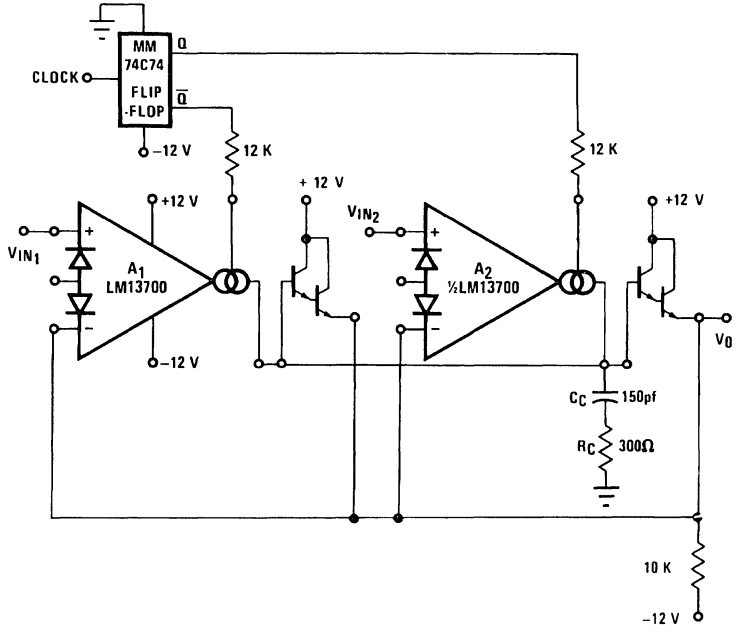

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FIGURE 20. Multiplexer

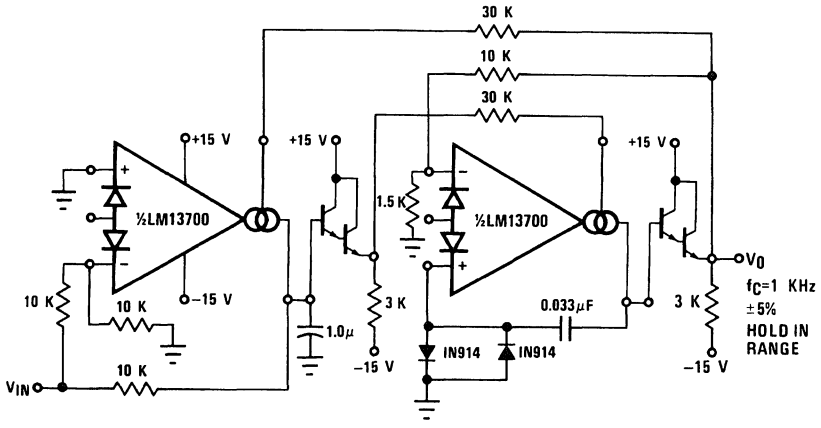

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FIGURE 21. Phase Lock Loop

Additional Applications (Continued)

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

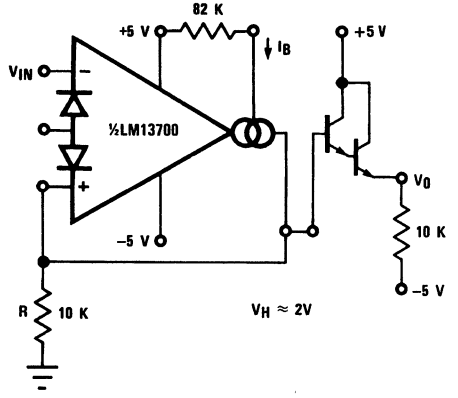

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FIGURE 22. Schmitt Trigger

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

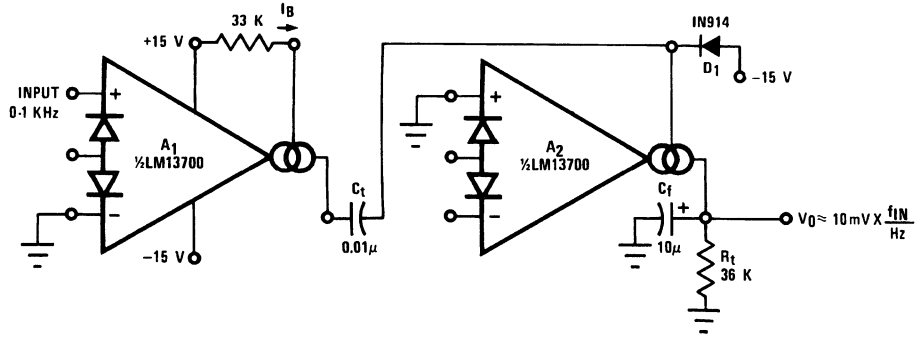

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FIGURE 23. Tachometer

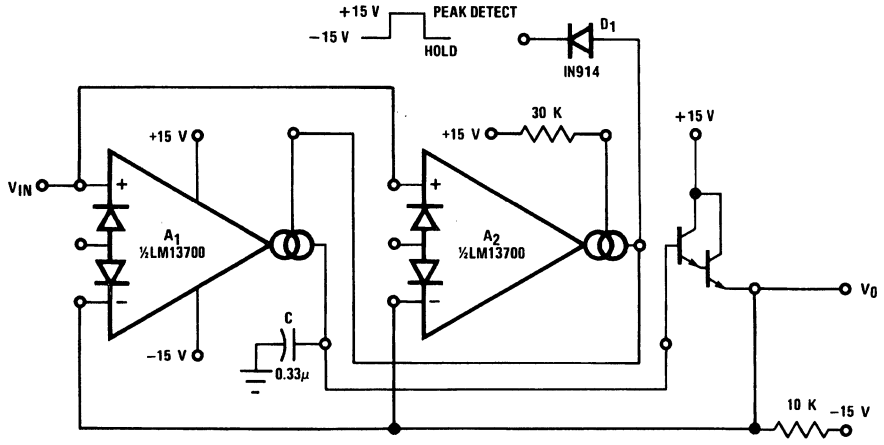

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FIGURE 24. Peak Detector and Hold Circuit

Additional Applications (Continued)

The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

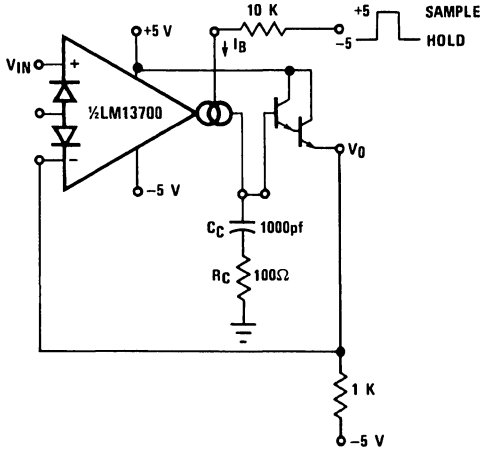

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FIGURE 25. Sample-Hold Circuit

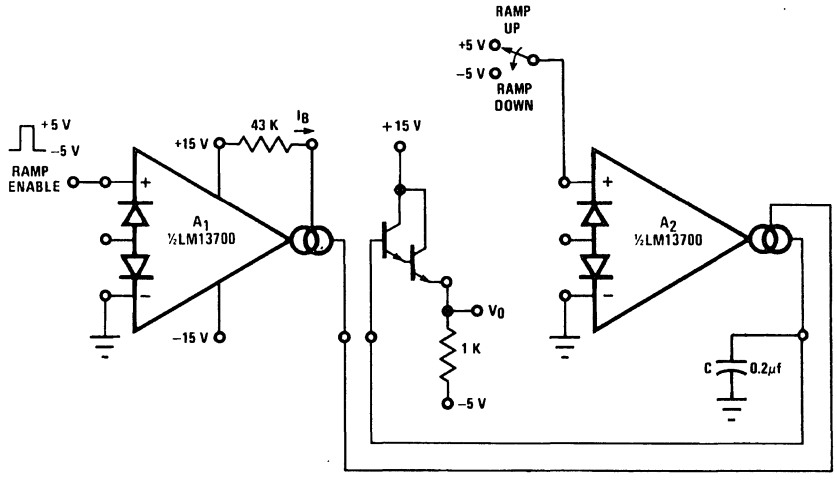

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FIGURE 26. Ramp and Hold

Additional Applications (Continued)

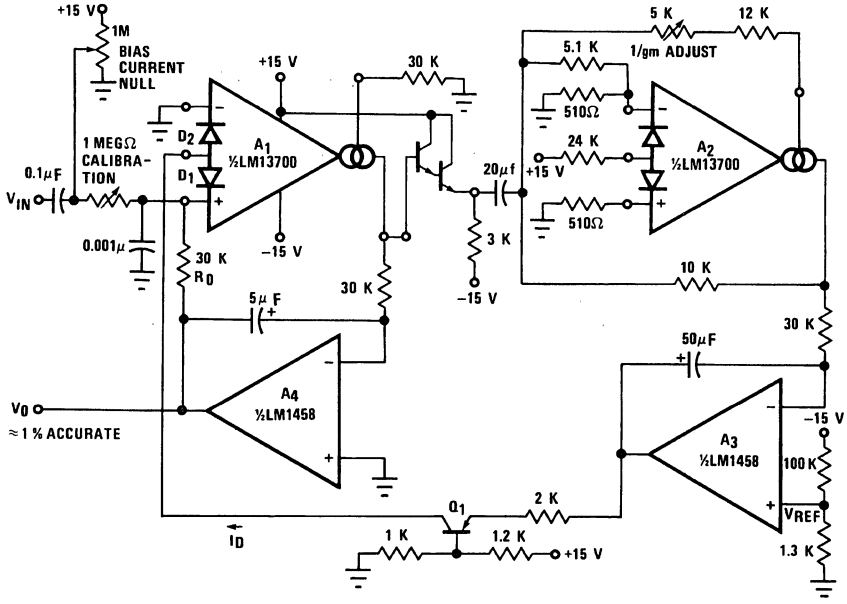

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FIGURE 27. True RMS Converter

The circuit of *Figure 28* is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 29*.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 30* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{-2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B}1 = \frac{(R_1 + R_2)\,V_{IN}1}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

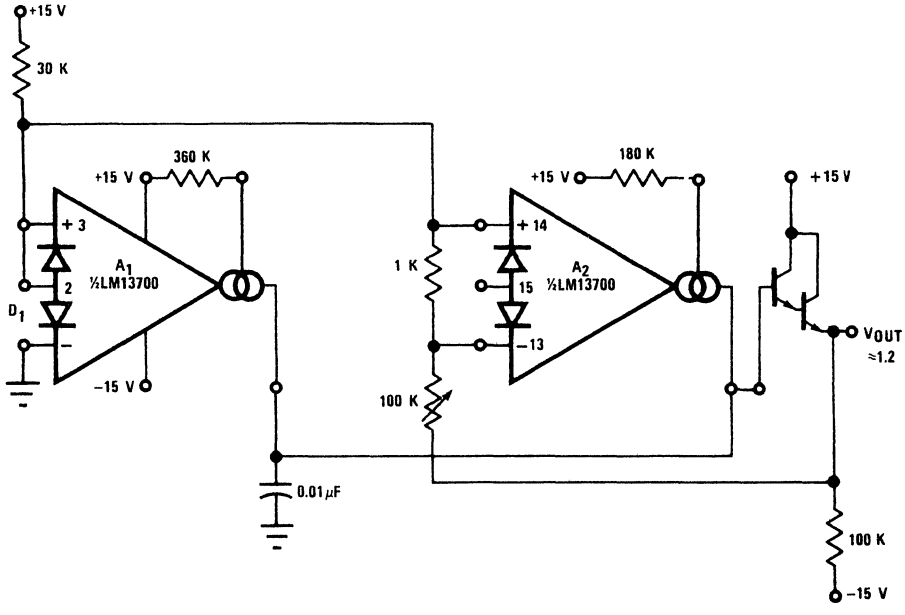
$$V_{B}1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp\frac{2(R_1 + R_2)\,V_C}{R_1\,I_2\,R_C}$$

This logarithmic current can be used to bias the circuit of *Figure 4* to provide temperature independent stereo attenuation characteristic.

Additional Applications (Continued)



TL/H/7981–35

FIGURE 28. Delta VBE Reference

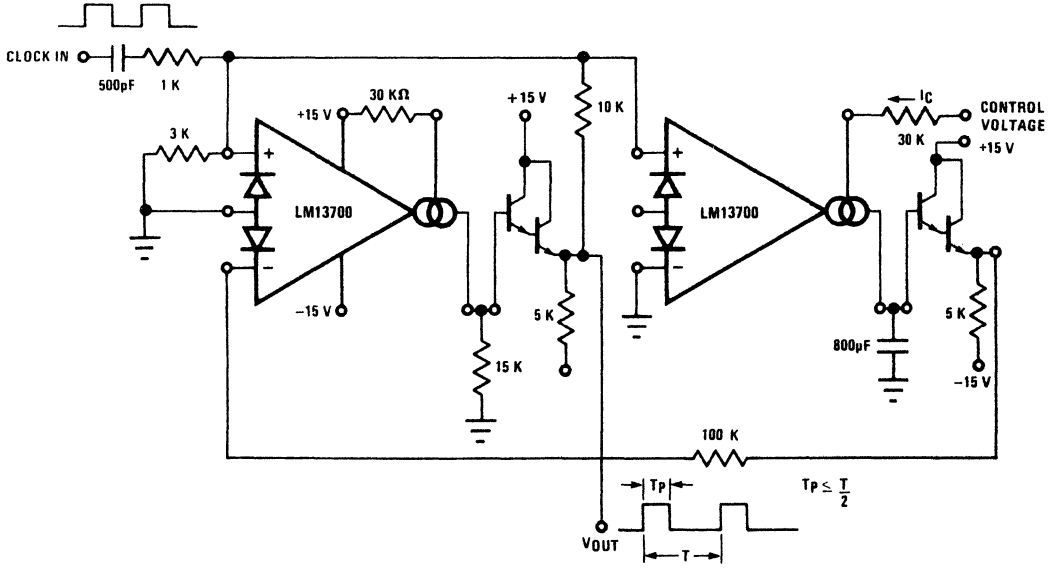


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FIGURE 29. Pulse Width Modulator

Additional Applications (Continued)

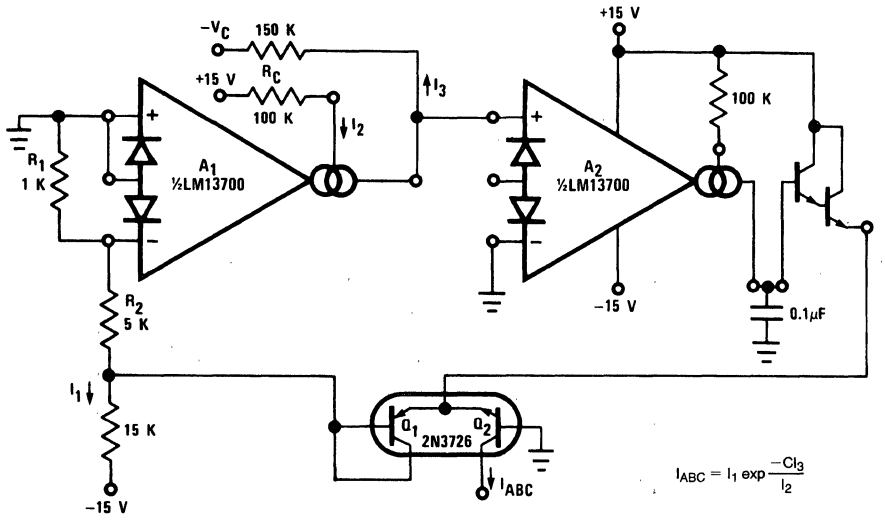

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FIGURE 30. Logarithmic Current Source

National Semiconductor

PRELIMINARY

LMC660AM /LMC660AI /LMC660C CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

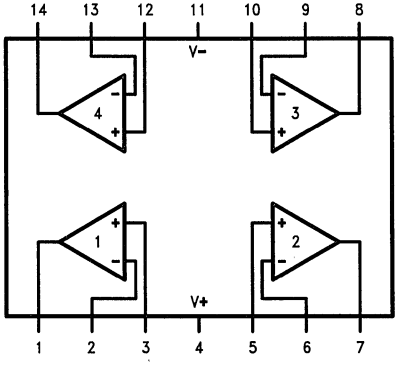
Features

- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV max
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Insensitive to latch-up
- Symmetrical gain when sourcing and sinking current

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Connection Diagram



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Ordering Information

Package	Temperature Range			NSC Drawing
	Military	Industrial	Commercial	
14-Pin Cavity DIP	LMC660AMD			D14E
14-Pin Small Outline		LMC660AIM	LMC660CM	M14A
14-Pin Molded DIP		LMC660AIN	LMC660CN	N14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD tolerance (Note 10)	500V

Operating Conditions

Temperature Range	
LMC660AM	$-55°C \le T_J \le +125°C$
LMC660AI	$-40°C \le T_J \le +85°C$
LMC660C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		1	3		3	**3.3**	6	**6.3**	mV max
			3.5						
Input Offset Voltage Average Drift		1.3							μV/°C
Input Bias Current	(Note 9)	0.04	20		20	**4**		**2**	pA max
			100						
Input Offset Current	(Note 9)	0.01	20		20	**2**		**1**	pA max
			100						
Input Resistance		>1							TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70		70	**68**	63	**62**	dB min
			68						
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70		70	**68**	63	**62**	dB min
			68						
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84		84	**83**	74	**73**	dB min
			82						
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1		−0.1	**0**	−0.1	**0**	V max
			0						
		$V^+ - 1.9$	$V^+ - 2.3$		$V^+ - 2.3$	$\mathbf{V^+ - 2.5}$	$V^+ - 2.3$	$\mathbf{V^+ - 2.4}$	V min
			$\mathbf{V^+ - 2.6}$						
Large Signal Voltage Gain	$R_L = 2k\Omega$ (Note 6)								
	Sourcing	2000	400		400	**440**	200	**300**	V/mV min
			300						
	Sinking	500	180		180	**120**	90	**80**	V/mV min
			70						
	$R_L = 600\Omega$ (Note 6)								
	Sourcing	1000	200		200	**220**	100	**150**	V/mV min
			150						
	Sinking	250	100		100	**60**	50	**40**	V/mV min
			35						

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Swing	$V^+ = 5V$ $R_L = 2 k\Omega$ to $V^+/2$	4.87	4.82		4.82	**4.79**	4.78	**4.76**	V min
			4.77						
		0.10	0.15		0.15	**0.17**	0.19	**0.21**	V max
			0.19						
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41		4.41	**4.31**	4.27	**4.21**	V min
			4.24						
		0.30	0.50		0.50	**0.56**	0.63	**0.69**	V max
			0.63						
	$V^+ = 15V$ $R_L = 2 k\Omega$ to $V^+/2$	14.63	14.50		14.50	**14.44**	14.37	**14.32**	V min
			14.40						
		0.26	0.35		0.35	**0.40**	0.44	**0.48**	V max
			0.43						
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35		13.35	**13.15**	12.92	**12.76**	V min
			13.02						
		0.79	1.16		1.16	**1.32**	1.45	**1.58**	V max
			1.42						
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16		16	**14**	13	**11**	mA min
			12						
	Sinking, $V_O = 5V$	21	16		16	**14**	13	**11**	mA min
			12						
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19		28	**25**	23	**21**	mA min
			19						
	Sinking, $V_O = 13V$	39	19		28	**24**	23	**20**	mA min
			19						
Supply Current	All Four Amplifiers $V_O = 1.5V$	1.5	2.2		2.2	**2.6**	2.7	**2.9**	mA min
			2.9						

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC660AM		LMC660AI		LMC660C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	(Note 7)	1.1	0.8		0.8	**0.6**		**0.7**	V/μs min
			0.5						
Gain-Bandwidth Product		1.4							MHz min
Phase Margin		50							Deg
Gain Margin		17							dB
Amp-to-Amp Isolation	(Note 8)	130							dB
Input Referred Voltage Noise	F = 1 kHz	22							$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002							$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\,k\Omega$, $V_O = 8\,V_{PP}$	0.01							%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 75°C/W., the molded plastic SO (M) package is 105°C/W., and the cavity DIP (D) package is 92°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: These limits are guaranteed, but are not used in calculating outgoing AQL.

Note 6: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 7: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

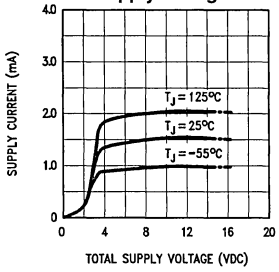
Note 8: Input referred. $V^+ = 15V$ and $R_L = 10\,k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\,V_{PP}$.

Note 9: The specifications in the Design Limit column reflect the true performance of the part, while those in the Tested Limit column are degraded to allow for the unavoidable inaccuracies involved in cost-effective high-speed automatic testing.

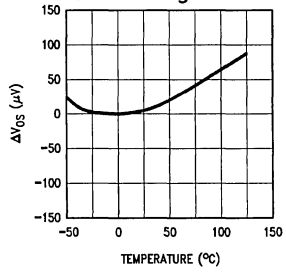
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

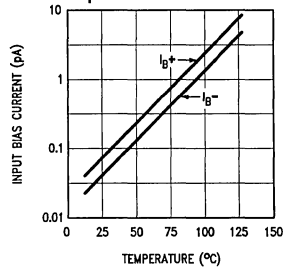
Supply Current vs Supply Voltage



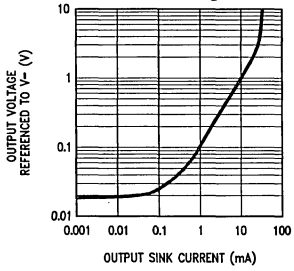
Offset Voltage



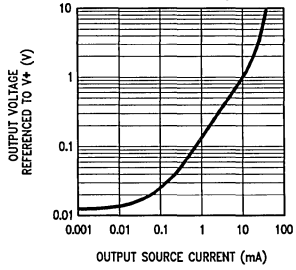
Input Bias Current



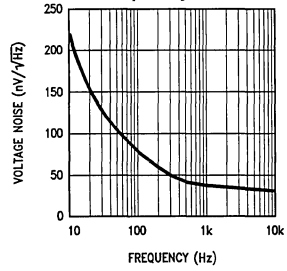
Output Characteristics Current Sinking



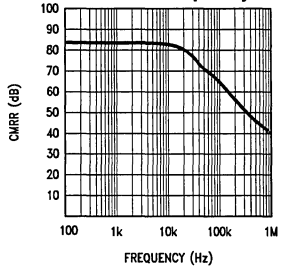
Output Characteristics Current Sourcing



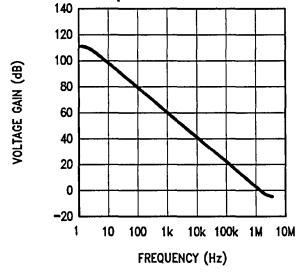
Input Voltage Noise vs Frequency



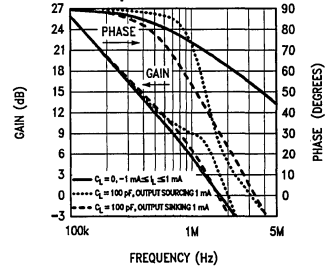
CMMR vs Frequency



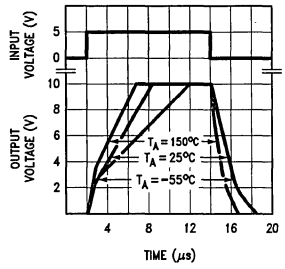
Open-Loop Frequency Response



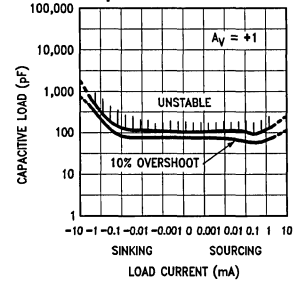
Frequency Response vs Capacitive Load



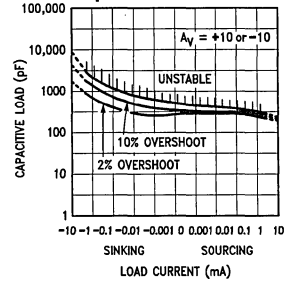
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/8767–3

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

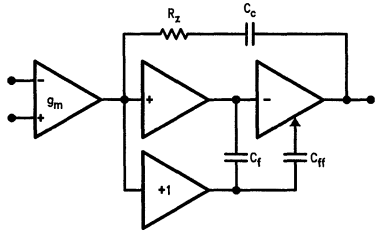
Applications Hint

Amplifier Topolgy

The topology chosen for the LMC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and Cff) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

LMC660 Circuit Topology (Each Amplifier)



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The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capcitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times 6BW \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

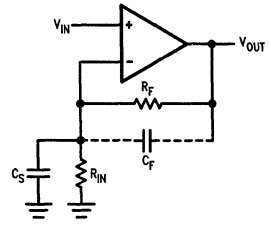
the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$

General Operational Amplifier Circuit



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C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Applications Hint (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Input Overdrive

Input overdrive protection has been built into the LMC660, so that no latching, "output phase changes", or activation of parasitic junctions occurs when the inputs are taken outside the power supply rails. In addition, this protection inhibits ESD damage whether or not the device is powered up, and even if the power supply pins are floating. The protection consists of 200Ω series input resistors and diodes connected from each input to each power supply rail.

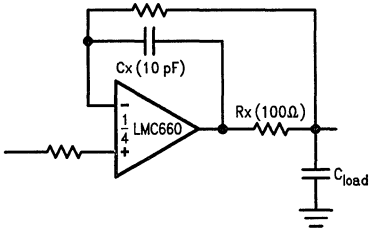
If the input to the LMC660 is set above the LMC660's input common-mode range, the LMC660's output will go to the positive supply rail. This output will stay at the positive supply rail until the input voltage is dropped back into the input common-mode range.

Capacitive Load Tolerance

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

Rx, Cx Improve Capacitive Load Tolerance

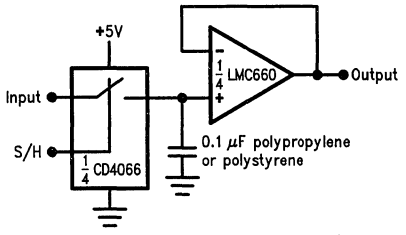


TL/H/8767–5

Typical Single-Supply Applications (V^+ = 5.0 VDC)

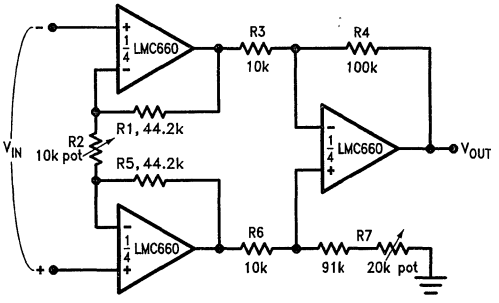
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



TL/H/8767–7

Instrumentation Amplifier



TL/H/8767–8

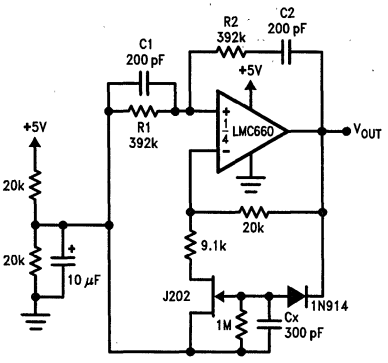
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3} \quad \begin{array}{l}\text{if } R1 = R5 \\ R3 = R6, \\ \text{and } R4 = R7.\end{array}$$

$$= 100 \text{ for circuit as shown.}$$

All resistors should be at least 1% tolerance. Matching of R1 to R5, R3 to R6, and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications (V^+ = 5.0 VDC)

Sine-Wave Oscillator



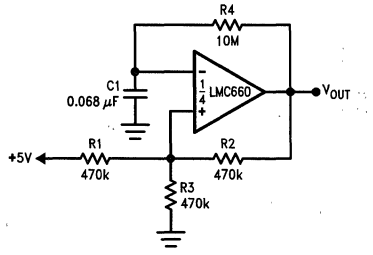
TL/H/8767–9

Oscillator frequency is determined by R1, R2, C1, and C2:

fosc = $1/2\pi RC$, where R = R1 = R2 and C = C1 = C2.

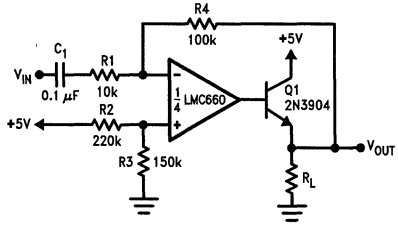
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



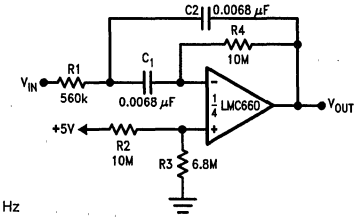
TL/H/8767–10

Power Amplifier



TL/H/8767–11

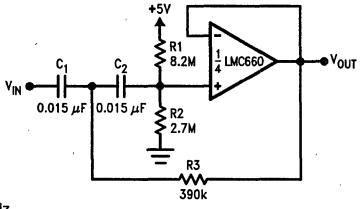
10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

TL/H/8767–12

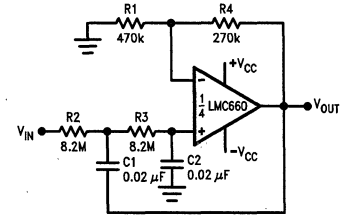
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

TL/H/8767–13

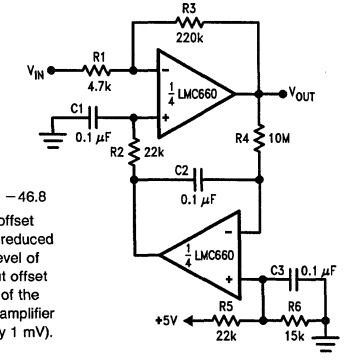
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



f_c = 1 Hz
d = 1.414
Gain = 1.57

TL/H/8767–14

High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

TL/H/8767–15

National Semiconductor

LMC662AM/LMC662AI/LMC662C CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

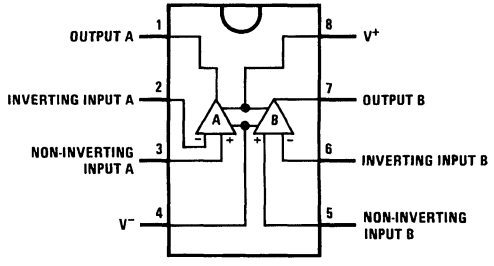
Features

- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV max
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Insensitive to latch-up
- Symmetrical gain when sourcing and sinking current

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-hold circuit
- Peak detector

Connection Diagram



TL/H/9763–1

Ordering Information

Package	Temperature Range			NSC Drawing
	Military	Industrial	Commercial	
8-Pin Cavity DIP	LMC662AMD	LMC662AID		D08C
8-Pin Small Outline		LMC662AIM	LMC662CM	M08A
8-Pin Molded DIP		LMC662AIN	LMC662CN	N08E

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD Tolerance (Note 10)	500V

Operating Conditions

Temperature Range	
LMC662AM	$-55°C \le T_J \le +125°C$
LMC662AI	$-40°C \le T_J \le +85°C$
LMC662C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V

DC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage		1	3		3	**3.3**	6	**6.3**	mV max
			3.5						
Input Offset Voltage Average Drift		1.3							µV/°C
Input Bias Current	(Note 9)	0.04	20		20	**4**		**2**	pA max
			100						
Input Offset Current	(Note 9)	0.01	20		20	**2**		**1**	pA max
			100						
Input Resistance		>1							Teraω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70		70	**68**	63	**62**	dB min
			68						
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70		70	**68**	63	**62**	dB min
			68						
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84		84	**83**	74	**73**	dB min
			82						
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1		−0.1	**0**	−0.1	**0**	V max
			0						
		$V^+ - 1.9$	$V^+ - 2.3$		$V^+ - 2.3$	**$V^+ - 2.5$**	$V^+ - 2.3$	**$V^+ - 2.4$**	V min
			$V^+ - 2.6$						
Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 6)								
	Sourcing	2000	400		400	**440**	200	**300**	V/mV min
			300						
	Sinking	500	180		180	**120**	90	**80**	V/mV min
			70						
	$R_L = 600\Omega$ (Note 6)								
	Sourcing	1000	200		200	**220**	100	**150**	V/mV min
			150						
	Sinking	250	100		100	**60**	50	**40**	V/mV min
			35						

DC Electrical Characteristics (Continued)

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Output Swing	$V^+ = 5V$ $R_L = 2 k\Omega$ to $V^+/2$	4.87	4.82		4.82	**4.79**	4.78	**4.76**	V min
			4.77						
		0.10	0.15		0.15	**0.17**	0.19	**0.21**	V max
			0.19						
	$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41		4.41	**4.31**	4.27	**4.21**	V min
			4.24						
		0.30	0.50		0.50	**0.56**	0.63	**0.69**	V max
			0.63						
	$V^+ = 15V$ $R_L = 2 k\Omega$ to $V^+/2$	14.63	14.50		14.50	**14.44**	14.37	**14.32**	V min
			14.40						
		0.26	0.35		0.35	**0.40**	0.44	**0.48**	V max
			0.43						
	$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35		13.35	**13.15**	12.92	**12.76**	V min
			13.02						
		0.79	1.16		1.16	**1.32**	1.45	**1.58**	V max
			1.42						
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16		16	**14**	13	**11**	mA min
			12						
	Sinking, $V_O = 5V$	21	16		16	**14**	13	**11**	mA min
			12						
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19		28	**25**	23	**21**	mA min
			19						
	Sinking, $V_O = 13V$	39	19		28	**24**	23	**20**	mA min
			19						
Supply Current	Both Amplifiers $V_O = 1.5V$	0.75	1.3		1.3	**1.5**	1.6	**1.8**	mA max
			1.8						

AC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LMC662AM		LMC662AI		LMC662C		Units
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	(Note 7)	1.1	0.8		0.8	**0.6**	0.8	**0.7**	V/μs min
			0.5						
Gain-Bandwidth Product		1.4							MHz
Phase Margin		50							Deg
Gain Margin		17							dB
Amp-to-Amp Isolation	(Note 8)	130							dB
Input Referred Voltage Noise	F = 1 kHz	22							$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002							$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\,k\Omega$, $V_O = 8\,V_{PP}$	0.01							%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 101°C/W, the molded plastic SO (M) package is 152°C/W, and the cavity DIP (D) package is 124°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: These limits are guaranteed, but are not used in calculating outgoing AQL.

Note 6: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 7: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

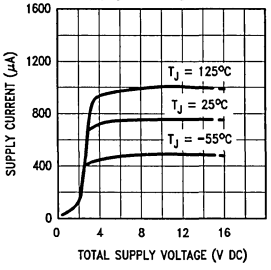
Note 8: Input referred. $V^+ = 15V$ and $R_L = 10\,k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\,V_{PP}$.

Note 9: The specifications in the Design Limit column reflect the true performance of the part, while those in the Tested Limit column are degraded to allow for the unavoidable inaccuracies involved in cost-effective high-speed automatic testing.

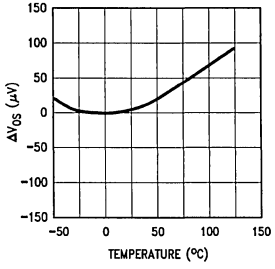
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

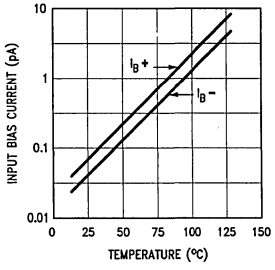
Supply Current vs Supply Voltage



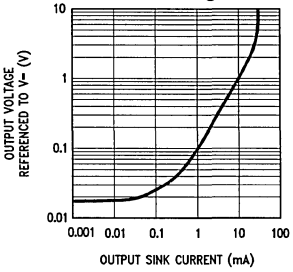
Offset Voltage



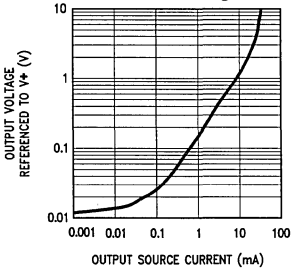
Input Bias Current



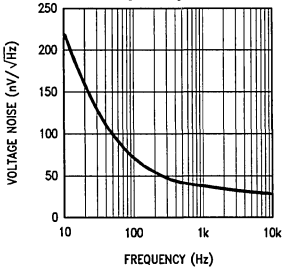
Output Characteristics Current Sinking



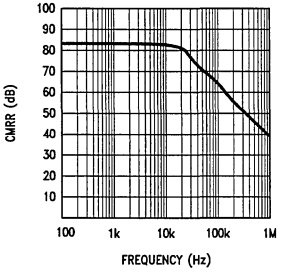
Output Characteristics Current Sourcing



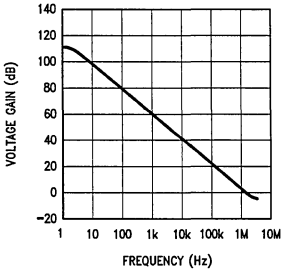
Input Voltage Noise vs Frequency



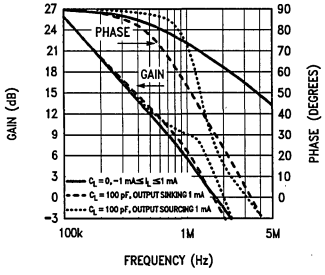
CMRR vs Frequency



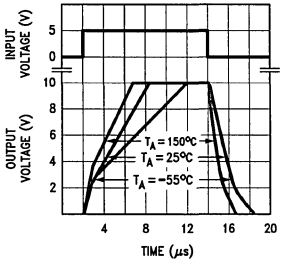
Open-Loop Frequency Response



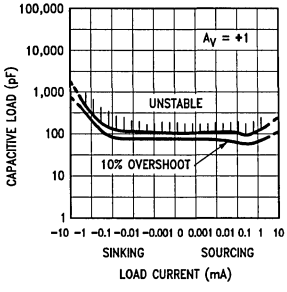
Frequency Response vs Capacitive Load



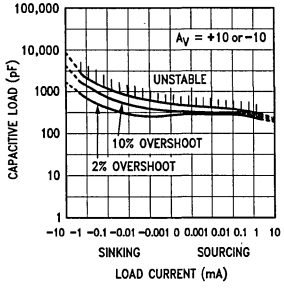
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/9763–3

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

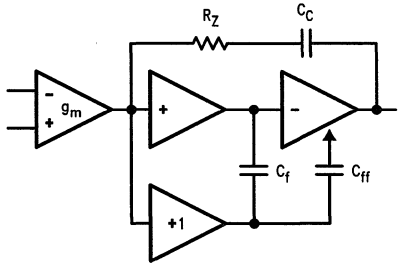
Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC662 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

LMC662 Circuit Topology (Each Amplifier)



TL/H/9763–4

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC662 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S},$$

the feedback capacitor should be:

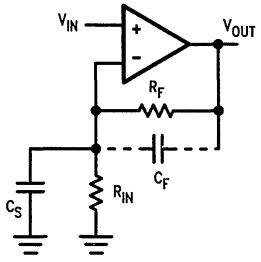
$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)

General Operational Amplifier Circuit



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C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

INPUT OVERDRIVE

Input overdrive protection has been built into the LMC662, so that no latching, "output phase changes", or activation of parasitic junctions occurs when the inputs are taken outside the power supply rails. In addition, this protection inhibits its ESD damage whether or not the device is powered up, and even if the power supply pins are floating. The protection consists of 200Ω series input resistors and diodes connected from each input to each power supply rail.

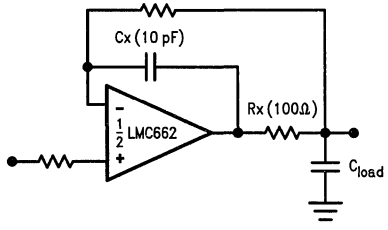
If the input to the LMC662 is set above the LMC662's input common-mode range, the LMC662's output will go to the positive supply rail. This output will stay at the positive supply rail until the input voltage is dropped back into the input common-mode range.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

Rx, Cx Improve Capacitive Load Tolerance



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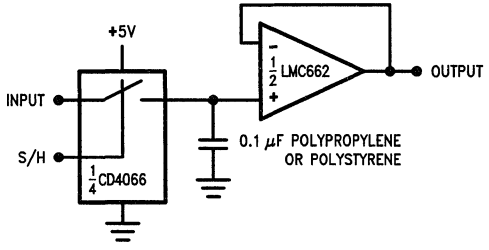
Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC662 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LM662 is smaller than that of the LM358.

Low-Leakage Sample-and-Hold



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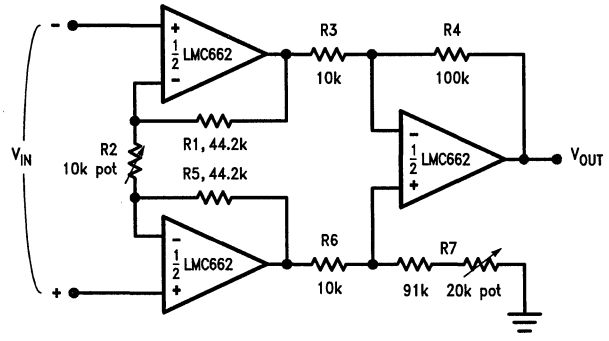
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Instrumentation Amplifier



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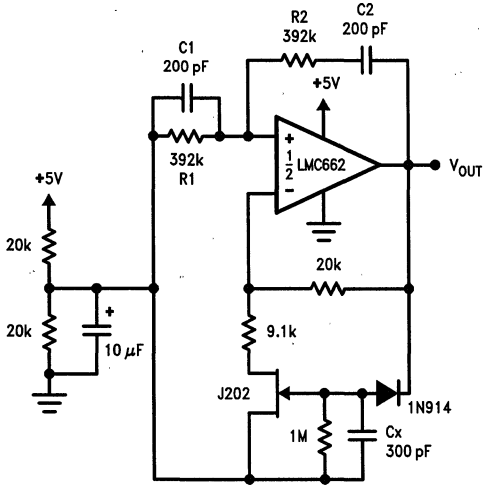
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

if R1 = R5; R3 = R6, and R4 = R7.

= 100 for circuit shown.

All resistors should be at least 1% tolerance. Matching of R1 to R5, R3 to R6, and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



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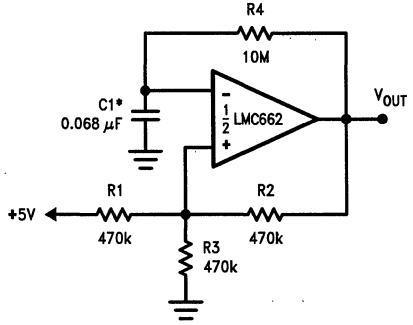
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



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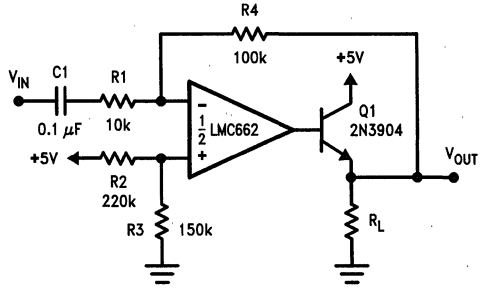
Power Amplifier



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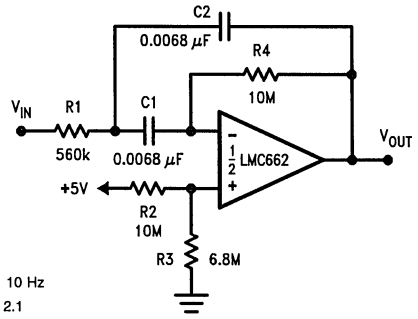
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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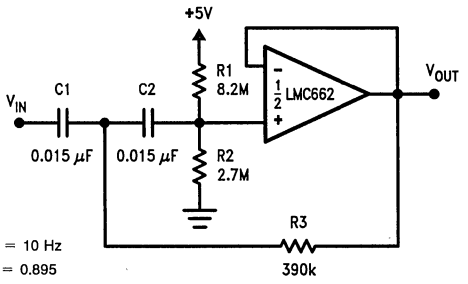
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

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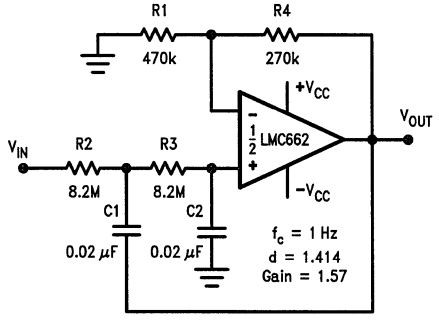
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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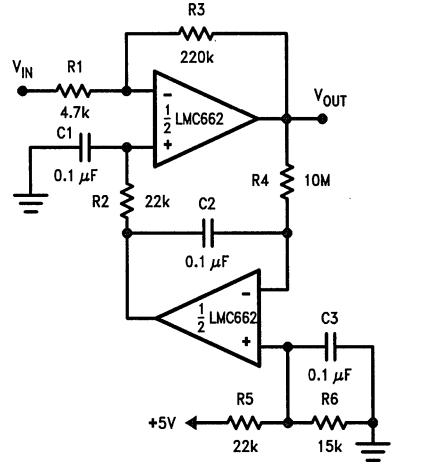
High Gain Amplifier with Offset Voltage Reduction



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Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

National Semiconductor

LMC669 Auto-Zero

General Description

The LMC669 uses sampled-data techniques to reduce the input offset voltage (V_{OS}) of an amplifier or system to approximately 5 μV. A four-stage comparator samples the summing node of an inverting-amplifier and generates a correction voltage that is applied to the amplifier's non-inverting input. The offset correction is independent of time, temperature, and supply voltage, and requires no initial or periodic user offset adjustments.

The user may also adjust clock frequency, sample rate, and the correction voltage's step size and magnitude.

The Auto-Zero operates on supply voltages of ±8V to ±20V with a quiescent current of 3 mA.

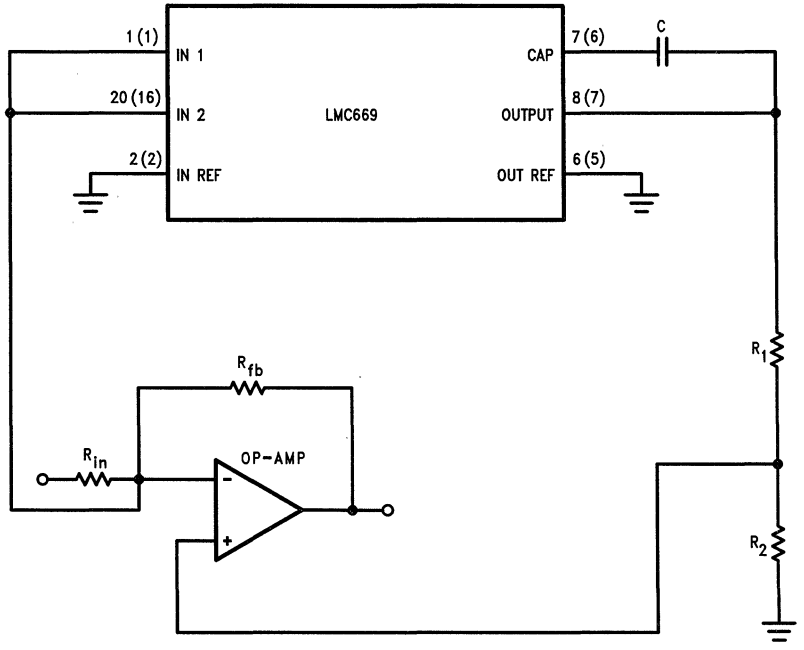
The use of the LMC669 does not limit the performance of the amplifier it is used with. Full use of the gain-bandwidth product, slew rate, and DC gain is retained.

The LMC669 can be used as a precision comparator with a latched, open drain output, or as a low-offset inverting operational amplifier for low-speed applications.

Features

- 5 microvolts typical offset voltage
- Temperature independent offset correction
- Internal or external clocking
- Automatic and continuous offset voltage correction
- High voltage CMOS—up to ±20V supplies

Typical Application



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Numbers in ( ) are for 16-pin packages

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage (V^+)	+22V
Negative Supply Voltage (V^-)	−22V
Voltage of Logic Pins T1, T2, $\overline{\text{RESET}}$, CLK	−0.2V to (V^+ + 0.2V)
Voltage at Inputs	−0.2V to (V^+ + 0.2V)
Input Current (Note 3) INREF, IN1 and IN2	20 mA
Power Dissipation (Note 4)	500 mW
Storage Temperature	−65°C to +150°C
Lead Temp. (soldering, 10 seconds)	300°C

Operating Ranges (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMC669D	−40°C ≤ T_A ≤ +85°C
Positive Supply Voltage	+8V to +20V
Negative Supply Voltage	−8V to −20V
INREF, IN1 and IN2 Voltage (Note 5)	−200 mV to +2V
ESD Susceptability (Note 10)	600V

Electrical Characteristics

The following specifications apply for V^+ = +15V, and V^- = − 15V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
V_{OS}	Maximum Input Offset Voltage (Note 9)	LMC669BIN, BIM LMC669BCN, BCM	Signal applied to both IN1 & IN2, T_{CLK} = 50 μs, V_{INREF} = 0V, 0.5V	±5	**±25** ±25		μV
		LMC669CIN, CIM LMC669CCN, CCM		±10	**±50** ±50		
		LMC669CD		±5	**±25**		
V_{OS}	Maximum Input Offset Voltage (Note 9)	LMC669BIN, BIM LMC669BCN, BCM	Signal applied only to IN1 or IN2, T_{CLK} = 50 μs, V_{INREF} = 0V	±10	**±50** ±50		μV
		LMC669CIN, CIM LMC669CCN, CCM		±20	**±100** ±100		
		LMC669CD		±10	**±50**		
I_b	Maximum Input Bias Current	IN2	Clock Off	1	100		pA
				400			pA
		IN1 or IN1 & IN2		5	100		pA
				40		**75**	nA
$\frac{\Delta V_{OS}}{\Delta T}$	Average Input Offset Drift			0.1			μV/°C
V_{IN1}, V_{IN2}	IN1 & IN2 Input Voltage Range (Note 5)	min		−200	0		mV
		max		+2.0	+0.5		V
$V_{IN\ REF}$	IN REF Input Voltage Range (Note 5)	min		−200	0		mV
		max		+2.0	+0.5		V
$V_{OUT\ REF}$	OUT REF Input Voltage Range	min		−100			mV
		max		+100			mV
PSRR	Power Supply Rejection Ratio			120			dB
V_{OUT}	Integrator Output Voltage Range			±14	±12	**±11**	V
V_{CO}	Comparator Open-Drain Output Voltage Range	Low (max)	Sink Current = 1.0 mA	0.25	**0.4**		V
		High (min)		25	20	**19**	
I_S^+	Maximum Positive Supply Current		$\overline{\text{RESET}}$ Low, T_{CLK} = 50 μs	3.2	6.0		mA
					10.0		

Electrical Characteristics The following specifications apply for $V^+ = +15V$, and $V^- = -15V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter			Conditions	Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
I_S-	Maximum Negative Supply Current			$\overline{RESET}$ Low, $T_{CLK} = 50\ \mu s$	2.0	5.0		mA
						7.0		
f_S	Maximum Sample Rate			$\overline{RESET}$ Low, Internal Clock	100	66.6	**56**	kHz
f_{CLK}	Clock Frequency Range		min		100		**100**	Hz
			max		100		**100**	kHz
T_R	Minimum $\overline{RESET}$ Pulse Width				80	150	**175**	ns
V_{TH}	Digital Input Threshold Voltage	T1, T2, $\overline{RESET}$	High (min)		2.9	3.5		V
			Low (max)		2.9	1.5		V
		CLK	High (min)		3.5	4.0		V
			Low (max)		1.5	1.0		V
$I_{D\ IN}$	T1, T2, $\overline{RESET}$, & CLK Maximum Digital Input Current		High		1.0			pA
						1.0		μA
			Low		1.0			pA
						1.0		μA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are with respect to AGND.

Note 3: This input current will exist only when an input is driven to a voltage greater than ($V^+ + 0.2V$) or less than $-0.2V$. It is due to internal diode clamps at the inputs turning on. If the current is limited to 20 mA, the overdrive will not be harmful to the LMC669.

Note 4: The typical junction-to-ambient thermal resistance (θ_{JA}) of the 16 pin J package is 80°C/W.

Note 5: If input currents are limited, input voltages may be driven beyond these limits and the device will still be functional. The comparator output will be correct as long as the voltage on either the INREF pin or the two input IN1 & IN2 pins is between -200 mV and $+2V$.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% tested.

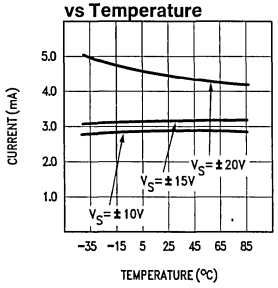
Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 9: The LMC669CD exhibits a warm-up drift of approximately 3 μV to 5 μV in the negative direction. There are two factors that work together to cause this. Firstly, as the die becomes warm, a temperature gradient forms between pin 2 and pins 1 and 16. Secondly, a thermocouple is created between the metal of the leadframe and the metal of the wire (usually copper) used to connect the IC to a circuit. It takes about 6 minutes for the drift to stabilize. The N and M packages do not exhibit this drift because their leadframes are 90% copper.

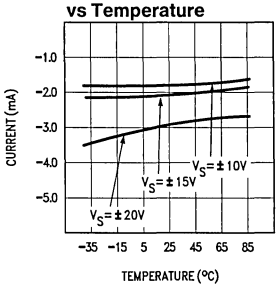
Note 10: Human body model, 100 pF discharged through 1.5 kΩ.

Typical Performance Characteristics

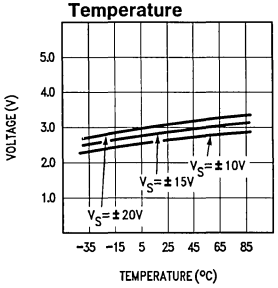
Positive Supply Current vs Temperature



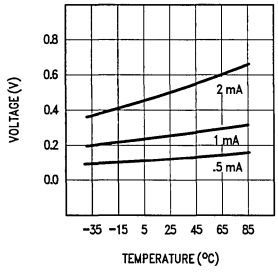
Negative Supply Current vs Temperature



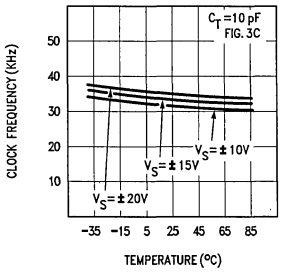
T1, T2 & $\overline{\text{RESET}}$ thresholds vs Temperature



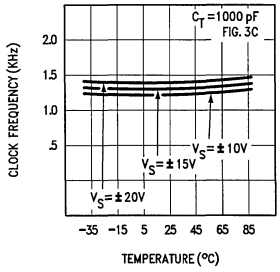
$V_{COMP\ OUT}$ vs Temperature



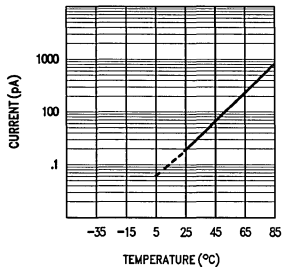
Clock Frequency vs Temperature



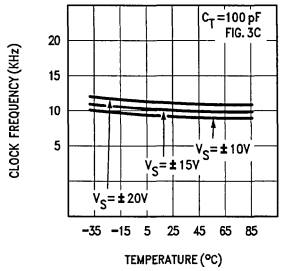
Clock Frequency vs Temperature



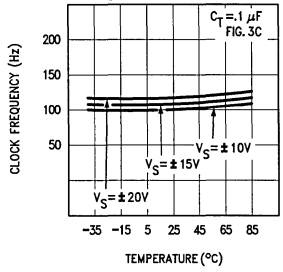
Integrator Summing Node Leakage Current



Clock Frequency vs Temperature



Clock Frequency vs Temperature



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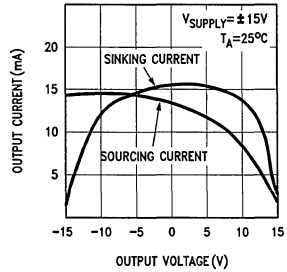
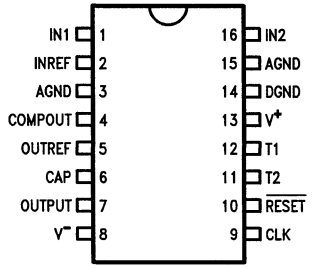
Output Current Limit vs Output Voltage



TL/H/8561–3

Connection Diagram

16-Pin Dual-In-Line Package



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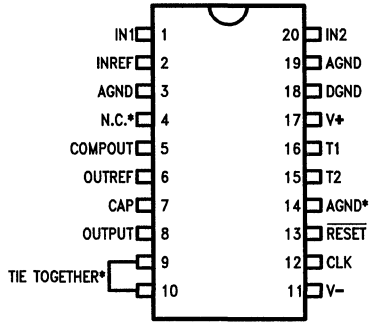
Top View

Order Number LMC669D
See NS Package Number D16C

20-Pin Dual-In-Line (N) Package
20-Pin Small-Outline (M) Package



TL/H/8561–17

Top View

*These pins must be connected as shown to ensure compatibility with future parts.

Pin Description LMC669 Numbers in ( ) are for 16-pin package

Pin	Description	Pin	Description
IN1, IN2 1, 20 (1, 16)	These are the inputs to the Auto Zero's comparator. They should be tied together and connected to the summing node of the host operational amplifier (op amp). One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V^+ (also refer to notes 3 and 5).	INREF 2 (2)	This is the input for the comparator's reference voltage. Correction of V_{OS} is accomplished by connecting this pin to a good clean system ground of its own. One set of inputs, either IN1 and IN2 or INREF, must be between +2 volts and ground while the other can go to V^+ (also refer to notes 3 and 5).

Pin Description 16-pin LMC669 (Continued)

Pin	Description
AGND 3,19 (3,15)	These act to shield the IN1, IN2, and INREF connections from stray capacitance and leakage which could degrade the part's performance. They should be connected to a high quality ground.
DGND 18 (14)	Provides a separate ground for the internal digital circuitry to prevent noise from corrupting the comparator inputs. It should have its own ground connection.
COMPOUT 5 (4)	This is the latched output from the internal comparator. It is an open drain which can be left unconnected if not needed. Its response time is equal to the sample rate's period. The rise time, from 10% to 90%, is nominally 500 ns with a 10 kΩ pull-up resistor. The output is typically capable of swinging from +0.25 (at 1 mA) to +25 volts.
OUTREF 6 (5)	Output reference; for proper integrator operation this input should be connected to a good system ground, such as the ground to which INREF is connected.
OUTPUT 8 (7)	This is the LMC669's integrator output. It can swing from −12 to +12 volts in 0.2 volt steps with a ≥10 KΩ load and no external integrating capacitor.
CAP 7 (6)	When a capacitor is used to decrease the correction voltage's step size, it is connected between CAP and OUTPUT. It parallels an internal 10 pF capacitor.
CLK 12 (9)	External clock input/internal adjust. The frequency of the internal clock (nominally 100 kHz) may be reduced with an external capacitor or an external clock connected to the CLK input. The logic thresholds for this input are 4 volts for a logic high and 1 volt for logic low. The internal clock can be stopped by applying a logic high, through a diode, to the CLK input. When a logic low is applied to the diode, the internal clock runs freely. (See Figure 3)
$\overline{\text{RESET}}$ 13 (10)	Comparator reset. At power-up, or when $\overline{\text{RESET}}$ is pulled low during normal operation, the Auto Zero will run at its fastest sample rate. This allows for the quickest V_{OS} nulling.
4	Leave this pin unconnected.
9, 10	Connect these pins together.
14	Connect to analog ground.

Pin	Description
T1, T2 16, 15 (12, 11)	These pins select one of five clock divider ratios. The ratio, hence the sample rate can be changed by applying V+ or ground to T1 and T2. The ratio chosen by these inputs is valid after the comparator's output changes state; i.e., a zero-crossing between the offset and correction voltage has taken place. These inputs can also be changed at any time to modify the LMC669's sample rate. Use the table below to determine the reduction in the clock's frequency for each combination of T1 and T2.

T1	T2	$\overline{\text{RESET}}$	÷
X	X	0	1
1	1	1	4
1	0	1	16
0	1	1	128
0	0	1	1024

V+, V− 17, 11 (13, 8)	Positive and negative power supply inputs. Typical supply voltages are ±15 volts, but operation will take place from ±8 to ±20 volts. Power supply current is typically 3 mA. Bypass capacitors (0.01 ~ 0.1 μF) should be connected to the power supply pins.

Application Hints

1.0 INTRODUCTION

In its standard application shown in *Figure 1*, the LMC669 continuously samples the summing node of an inverting amplifier and generates a correction voltage for the amplifier's non-inverting input, nulling the amplifier's input offset voltage (V_{OS}) to 5 μV. The offset correction is independent of time, temperature, and supply voltage. The LMC669 eliminates the need for initial or periodic offset adjustments, compensates for V_{OS} drift due to temperature changes, allows the use of greater DC gain, and increases immunity to changes in power supply voltages.

At the input of the LMC669 is a sampled-data differential comparator with very low offset voltage. When the comparator samples the summing node voltage and determines that it is not at ground, the LMC669's output generates a small voltage step in the opposite direction of the error. The size of the step and the sample rate are user-selectable. The correction voltage continues to step up or down until the summing node is within the V_{OS} of the LMC669—typically 5 μV. At this point the Auto Zero continues to monitor the summing node and perform any needed corrections. An internal divider generates five different sampling rates for any given clock frequency.

The only external parts needed for V_{OS} correction of most amplifiers are two resistors and one capacitor. Since the capacitor is in the feedback loop of an integrator, it should be a low leakage type (polycarbonate, polypropylene, polystyrene, mylar, etc.). The tolerance of the resistors and capacitor is not critical (10% components are satisfactory).

Application Hints (Continued)

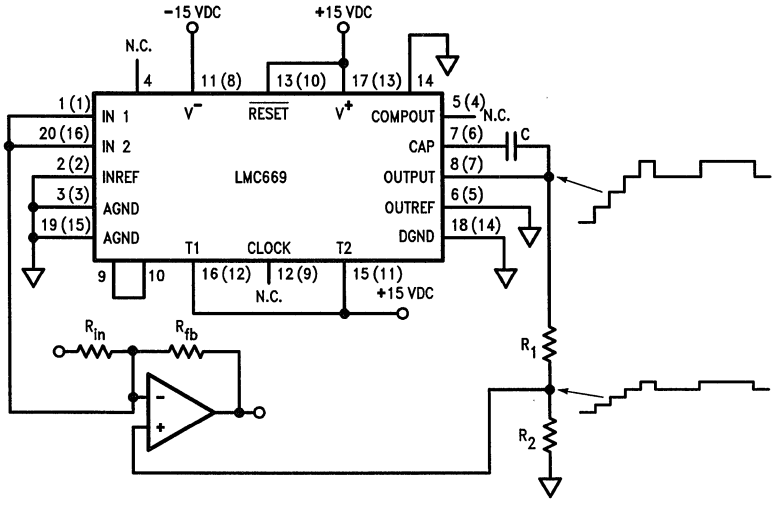


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FIGURE 1. Typical Application

1.1 CIRCUIT OPERATION

At the heart of the LMC669 is a four-stage precision sampled-data comparator, shown in *Figure 2.* The circuit operates by successively zeroing the offset of each stage, resulting in a very high gain amplifier with extremely low input offset voltage.

After a comparator decision is made, the latch is enabled and holds the comparator's output state. At the same time this state appears at COMPOUT. The latch also generates a ±1V signal that charges capacitor C_1 to ± 1V. C_1's charge is then transferred to the integrator's feedback capacitor C_2. Since C_2 is five times larger than C_1, a 200 mV step will appear at the integrator's output. Further reduction of the step size is possible with an external capacitor connected in parallel with C_2 (between OUTPUT and CAP). The integrator output is then attenuated by a resistive divider network before being applied to the external op amp's non-inverting input, completing the offset correction loop.

1.2 CLOCKS

In order to control the events that take place in the LMC669, an internal Schmitt trigger oscillator generates a 100 kHz clock. This oscillator's frequency can be lowered by connecting a capacitor between the CLK input and ground as in *Figure 3c.* It can also be overridden by applying an external clock source (≤ 100 kHz) to the CLK input (*Figure 3a*). Further, the clock can be halted with a diode connected as shown in *Figure 3(b).*

The clock signal drives the input of the divider (See *Figure 2*). Depending on the logic levels at inputs T1, T2, and $\overline{\text{RESET}}$, the clock can be divided by five different ratios (1, 4, 16, 128, and 1024). The output of the divider triggers the sequencer which controls the auto-zero function.

When the LMC669 is powered-up or reset the internal divider automatically divides by one. This allows the Auto-Zero to operate at maximum sampling rate so that large initial offsets can be rapidly corrected. When the comparator toggles for the first time, this indicates that input null has been achieved and that maximum sample rate is no longer required. The latch then switches the divider from ÷ 1 to the ratio programmed via T1 and T2. By employing this "two speed" approach the device can move quickly to handle turn-on transients and then shift to the optimum "gear" for long term offset correction. It is also possible to return to the maximum sample rate via the $\overline{\text{RESET}}$ input so that non-power-up transients can be dealt with as well.

1.3 INPUT RANGE

The IN1, IN2, and INREF inputs can accept signal levels between 0 and +2 V. However, as long as both IN1 and IN2, or INREF, is kept between 0 and 2V the other input (or inputs) can be taken to V^+ and, if input current limiting (≤20 mA) is provided, to V^-. In most auto-zero applications IN1 and IN2 will be able to go to these extended limits since INREF will normally be grounded.

Application Hints (Continued)

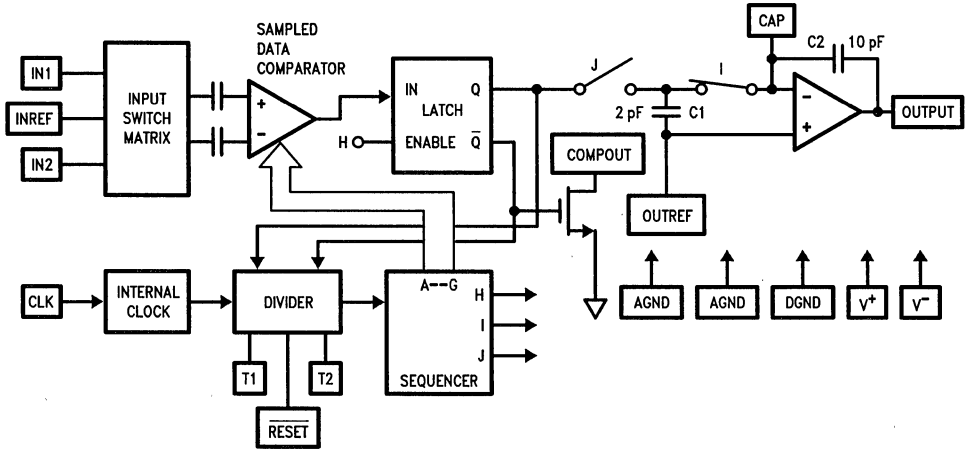

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FIGURE 2. Block Diagram

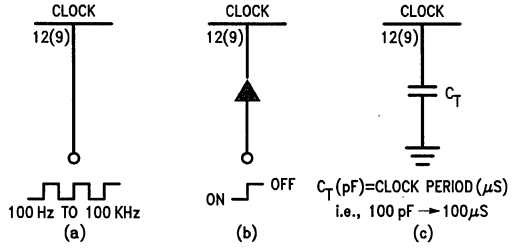

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FIGURE 3. Clock Input. External clock (a), controlling internal clock (b), reducing internal clock frequency (c).

Application Hints (Continued)

2.0 APPLICATION CIRCUITS

The most general application of the Auto-Zero is offset correction of an inverting op amp as shown in *Figure 1*. The example below shows how the integration capacitor and the resistor divider are chosen.

Determine the maximum expected offset voltage from the op amp characteristics and the requirements of the overall system. The correction voltage swing capability should be greater than or equal to this value. Also select the minimum system resolution and the time that can be allowed to null the initial offset. These will determine the correction voltage step size. The magnitude of the correction voltage (V_{corr}) and the step size (dv) are defined according to equations 1 and 2:

$$\text{Correction voltage} = V_{corr} = V_{out}\frac{R_2}{R_1 + R_2} \qquad (1)$$

V_o is typically ±12V for ±15V supplies.

$$R_2 = \frac{R_1 V_{corr}}{(V_o - V_{corr})} \qquad (1a)$$

$$= \frac{10K\, V_{corr}}{(12 - V_{corr})}$$

for $R_1 = 10\ k\Omega$ (For proper operation $R_1 + R_2$ should be greater than 10 kΩ.)

$$\text{step size} = dv = 1.0V\left(\frac{C_1}{C_2 + C}\right)\left(\frac{R_2}{R_1 + R_2}\right) \qquad (2)$$

$$C = \frac{C_1 R_2}{dv\,(R_1 + R_2)} - C_2 \qquad (2a)$$

with $C_1 = 2$ pF, $C_2 = 10$ pF, R_1 and R_2 from Eq. 1a. C_1 and C_2 are internal.

A further consideration regarding the selection of step size is resolution: the magnitude of the smallest significant signal. In the case of nulling the V_{os} of an op amp used with a digital-to-analog converter (DAC) the smallest signal is the voltage produced by the least-significant bit (LSB). Therefore, the correction voltage's step size would need to be much smaller than the magnitude of the DAC's LSB in order to retain the DAC's desired resolution.

Finally, for proper operation, the sampling period should be longer than the amplifier's settling time. 10 μs or more should be adequate for most contemporary amplifiers.

DESIGN EXAMPLE

As an example, assume that the offset of the op amp in *Figure 1* is expected to be no more than 15 mV and the system can tolerate a 1 μV square wave at a rate equal to the internal clock. Begin by using R_1 and R_2 to set the maximum correction voltage to 15 mV. The LMC669's output can swing to ±12 volts with a 10 KΩ load and a ±15 volt power supply. R_1 and R_2 should be chosen to reduce this to 15 mV:

$$R_2 = \frac{R_1 V_{corr}}{V_o - V_{corr}}$$

$$= \frac{(10K)\,(0.015)}{(12 - 0.015)}$$

$$= 12.5\Omega \approx 13\Omega$$

for ±15V supplies and $R_1 = 10K$.

Now choose C, the integrator's external feedback capacitor, to set the final step size to 1 μV. Using equation (2a):

$$C = \frac{C_1 R_2}{dv(R_1 + R_2)} - C_2$$

with $R_1 = 10\ k\Omega$, $R_2 = 13\Omega$, $C_1 = 2$ pF, and $C_2 = 10$ pF, yields

$$C \cong 2500\ pF$$

The null time for this example, with an amplifier offset of 15 mV, step size of 1 μV, and initial sample rate of 100 kHz, is

$$\text{Null time} = \frac{V_{os}}{(dv)(\text{sample rate})} \qquad (3)$$

$$= 150\ msec$$

If this is too slow, the step size can be increased.

OP AMP INPUT BIAS CURRENT

Input bias current should be considered when selecting an op amp that is nulled by the LMC669. If this current is too high, the result is a significant voltage drop across the feedback components and consequent output offset. The Auto Zero will not correct this error since it does not appear as a voltage at the summing node. Therefore, use low resistance feedback networks, or op amps with low input bias current such as the LF156, LF400, and LF411.

NOISE

Through careful selection of the sample rate and step size a compromise can be made between noise and null time. Low sample rates achieve low noise but take a long time to null an offset or correct it when a sudden change occurs. High sample rates can quickly null or correct changes in V_{os} but do so with an increase in noise. Step size directly affects the null time and the amount of noise introduced: small step sizes (< 100 nV) contribute almost no noise, but result in long null times.

Low noise LMC669 applications are beneficial to instrumentation and audio electronics. An LM833 low noise operational amplifier (4.5 nV / $\sqrt{Hz}$) with the LMC669 is shown in *Figure 4*. In this circuit the Auto Zero adds only 1 nV / $\sqrt{Hz}$ referred to the amplifier's input. To achieve this the step size is set to 100 nV. The sample rate, with the internal clock free-running, is set to 98 Hz (clock frequency ÷ 1024), and input and output filters are added to the LMC669. The input filter prevents switching transients from reaching the amplifier input and the output filter attenuates AC components of the steps at the Auto Zero's output. The filter at the op amp's input also introduces a pole at

$$F_p = \frac{1}{2\pi(R_{in} + R_f)\,C_f}$$

and a zero at

$$F_z = \frac{1}{2\pi R_f C_f}$$

The maximum V_{os} that can be corrected by the circuit in *Figure 4* is 12 mV. More offset correction can be obtained while retaining good noise performance by increasing the size of R_2 and C the same percentage. Increasing C compensates for the reduced attenuation caused by increasing R_2. This allows the step size to remain the same but increases the amount of correction voltage applied to the op amp.

Application Hints (Continued)

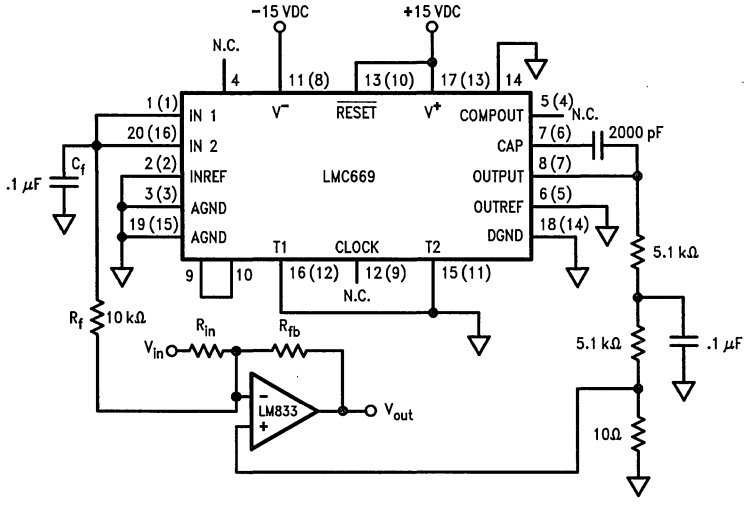

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FIGURE 4. Low Noise Application

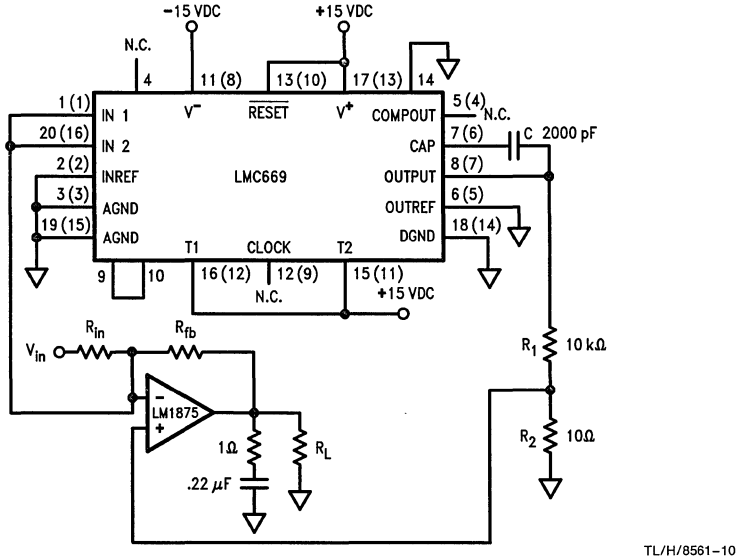

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FIGURE 5. Zeroing LM1875 Power Op-Amp

Application Hints (Continued)

POWER AMPLIFIERS

For applications such as motor control, automated servo systems, and power amplification the LMC669 can also be used with amplifiers other than standard small signal op amps. *Figure 5* shows how the Auto Zero can allow an LM1875 audio power amplifier to operate with very low offset. While the sample rate for this configuration is not critical, the LMC669's output step size should be set for less than 1 μV to ensure low system noise.

NON-INVERTING AMPLIFIERS AND SYSTEMS

A variation of the above circuit appears in *Figure 6* with the LMC669 operating as a DC-servo integrating feedback loop. This configuration is applicable when the Auto Zero is used with non-inverting op amps amplifying AC-only signals. The output error of the amplifier is reduced to the V_{OS} of the Auto Zero, typically 5 μV. A filter at the input of the LMC669 limits current and ensures that only DC and very low frequencies (< 0.6 Hz) are sampled. In this application the output of the op amp is sampled and compared with a reference ground. The correction output from the Auto Zero now replaces the ground reference for the feedback resistor connected to the inverting input.

Systems can also benefit from the Auto Zero. *Figure 7* shows how the V_{OS} of an MF6 Butterworth low-pass switched capacitor filter is nulled by the LMC669. The Auto Zero's IN1 and IN2 inputs are connected to the MF6's output while INREF is connected to its input. The correction signal is applied to the MF6's V_{OS} ADJ input. RC low-pass filters (R_{f1}, C_{f1} and R_{f2}, C_{f2}) are used to reduce AC signals at the LMC669's inputs and provide current limiting. It is important to set each passive RC filter's cutoff as low as possible, at most 0.1 of the MF6's f_o.

This correction makes the MF6 useful in applications calling for good DC accuracy. The MF6's typical 250 mV offset is decreased to 5 μV with a step size of 1 μV.

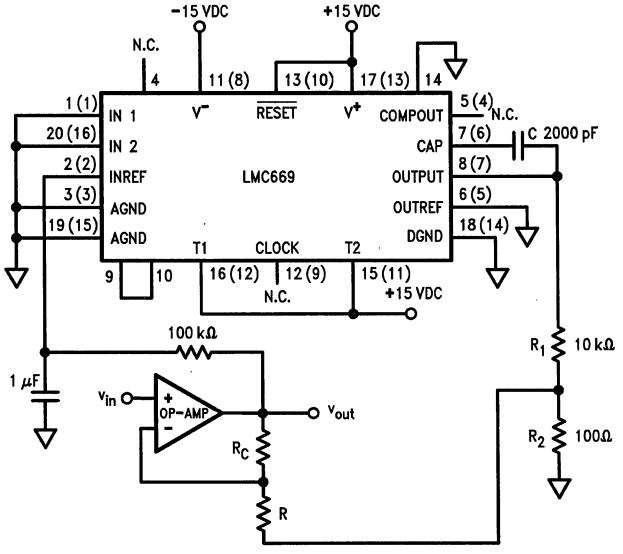

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FIGURE 6. DC Servo Loop

Application Hints (Continued)

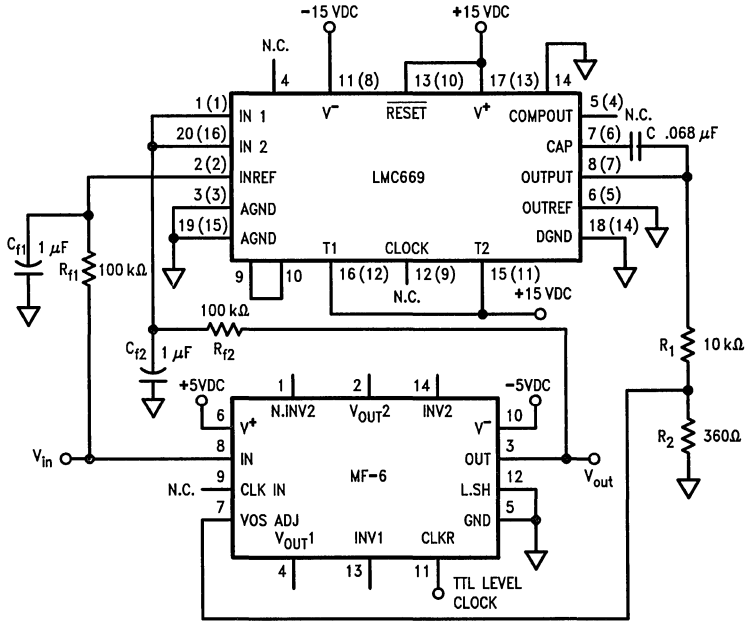

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FIGURE 7. Auto zeroing a system. In this case the 250 mV offset of a switched-capacitor low-pass filter is corrected by the LMC669.

MAINTAINING DAC LINEARITY

The LMC669 is particularly useful for zeroing the offset of an op amp used with a CMOS digital-to-analog converter (DAC). For good linearity the DAC's two outputs (I_{out} and $\overline{I_{out}}$) must be connected to identical ground potentials. The presence of op amp V_{os} (and its drift due to temperature) will degrade the DAC's linearity. Even though the effects of V_{os} can be corrected by trimming, a static trim will not be very helpful if the V_{os} changes with respect to temperature.

Figure 8 shows the DAC1208 with a 10V reference driving an LF357. The linearity of this DAC will degrade by 0.01% for each millivolt of op amp V_{os}. Therefore, the LF357's typical offset of 5 mV will turn the 12-bit DAC1208's 0.012% linearity error into 0.062%. What was a 12 bit linear device now has only 9 bits linearity. The original linearity specification can be retained by connecting an LMC669 to the inputs of the LF357, rendering the non-linearity due to V_{os} and temperature drift negligible. The DAC is now able to operate at its published linearity specifications independent of V_{os} and temperature.

Figure 9 shows the schematic of a unipolar power DAC. One use of the power DAC is as a digitally controlled power supply having the ability to sink current, in the case of inductive loads, as well as source current. The linearity of the DAC is preserved by the nulling action of the LMC669 connected to the inputs of the LM1875 power amplifier. The amplifier can generate an output voltage from 0 to 25 volts and a maximum current of 3 amperes. The actual output is determined by

$$V_{out} = \frac{-V_{ref}\,(D)}{4096}$$

("D" is the value of the digital code, base 10). The magnitude of each step is

$$1\ \text{LSB} = \frac{|V_{ref}|}{4096}$$

Stable operation of the LM1875 is ensured by the RC combination connected to the inverting input.

LMC669 AS A COMPARATOR

The LMC669's operation as a comparator is shown in *Figure 10*. Its input impedance is 5 kΩ with 160 pF to ground. For proper operation as a comparator IN1 and IN2, or IN-REF, should be kept between 0 and 2V while the other input (or inputs) can be taken to V^+. If input current limiting ($\leq$20 mA) is provided, the inputs can also go to V^-. (In addition, please refer to notes 3 and 5 under "Electrical Characteristics".)

The open collector output can be pulled-up to typically 25 volts. When the sink current is 1 mA the output can pull-down to 0.25V. Outputs closer to ground are possible with a larger pullup resistor.

Application Hints (Continued)

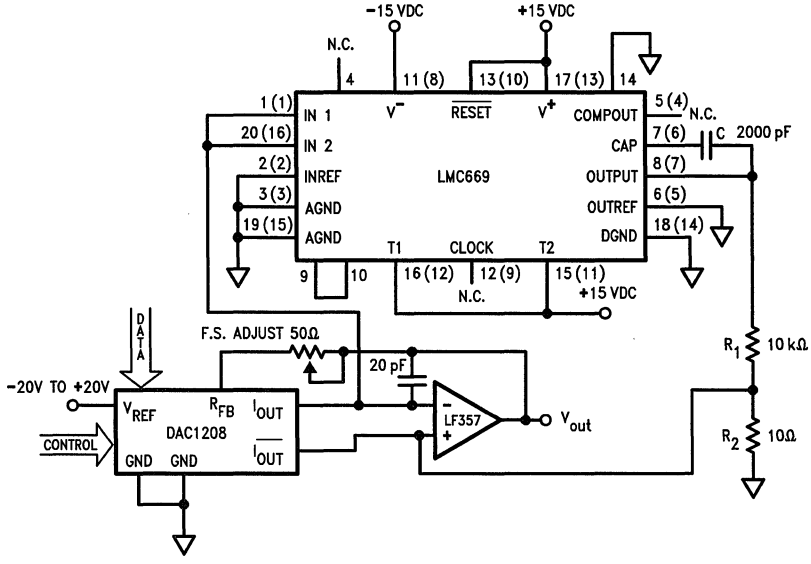

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FIGURE 8. Reducing V_{OS}-induced linearity errors in a 12-bit DAC by 0.01% /mV offset.

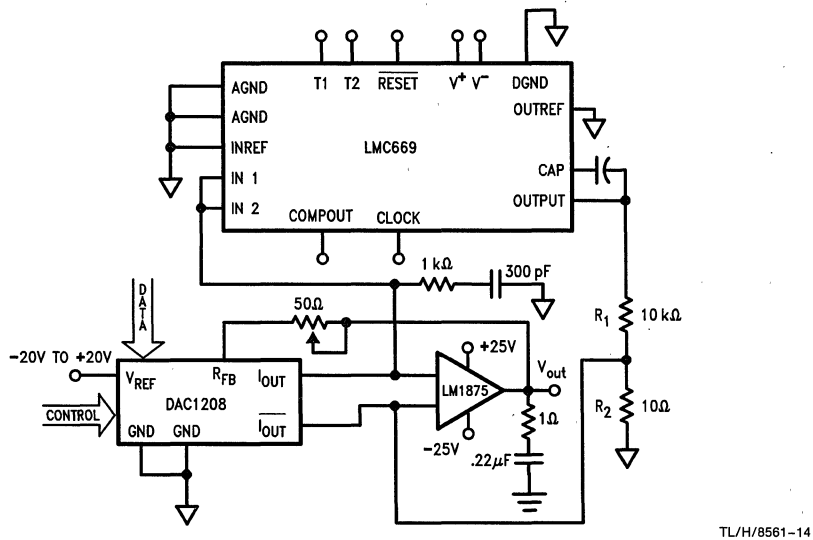

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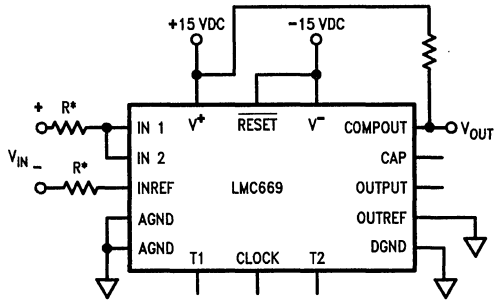
FIGURE 9. Power DAC with $\pm 20V_{p-p}$ and 3A output capabilities.

Application Hints (Continued)

LOW-FREQUENCY, HIGH-GAIN AMPLIFIER

For applications that require precision high-gain DC and low-frequency performance, the LMC669 can be connected as an amplifier as shown in *Figure 11*. For a closed-loop gain of −1000 the useful frequency range is typically

$$F_{max} = 20 \frac{Hz}{mV \text{ of step size}}$$



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*R = 10K. For inputs greater than 2 volts.

FIGURE 10. Low-Speed Precision Comparator

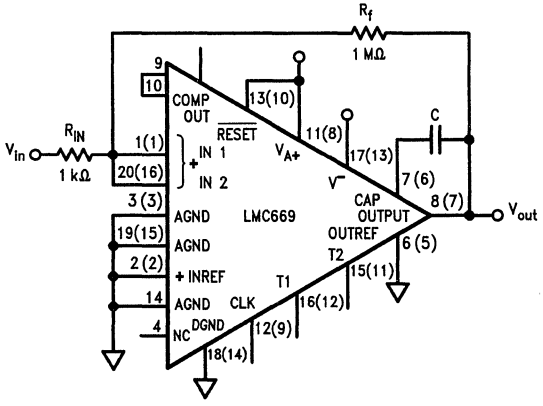

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FIGURE 11. Low Offset, High Gain, Low Frequency Op Amp.

Bandwidth ≅ $20 \frac{Hz}{mV \text{ of step size}}$, sample rate = 100 kHz.

National Semiconductor

LP124/LP2902/LP324 Micropower Quad Operational Amplifier

General Description

The LP124 series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP124 has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

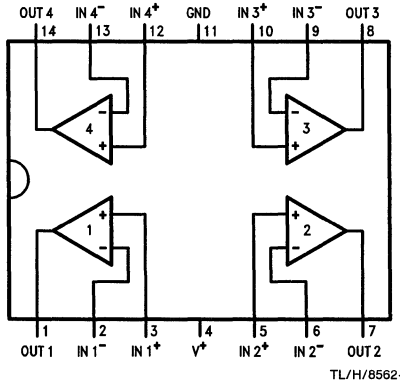
These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

Features

- Low supply current — 125 μA (max)
- Low offset voltage — 2 mV (max)
- Low input bias current — 4 nA (max)
- Input common mode to GND
- Interfaces to CMOS logic
- Wide supply range — $3V < V^+ < 32V$
- Small Outline Package available
- Pin-for-pin compatible with LM124

Connection Diagram

Dual-in-Line (J, N) and SO (M)



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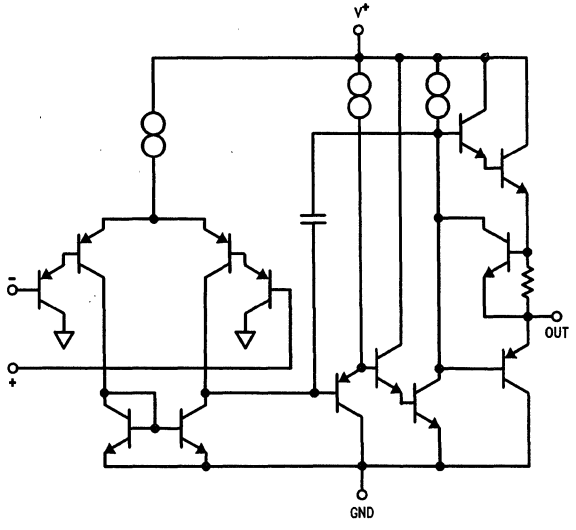
Order Number LP124J or LP324J
See NS Package Number J14A

Order Number LP324M or LP2902M
See NS Package Number M14A

Order Number LP324N or LP2902N
See NS Package Number N14A

Simplified Schematic



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	32V or ± 16V
LP2902	26V or ± 13V
Differential Input Voltage	32V
LP2902	26V
Input Voltage (Note 1)	−0.3V to 32V
LP2902	−0.3V to 26V
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous
ESD Susceptibility (Note 9)	±500V

Operating Conditions

	Package J	Package N	Package M
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
T_j Max	150°C	150°C	150°C
θ_{ja}	90°C/W	90°C/W	140°C/W
Operating Temp. Range	(Note 4)	(Note 4)	(Note 4)
Storage Temp. Range	−65°C ≤ T ≤ 150°C		
Soldering Information (10 sec.)	300°C	260°C	
Vapor Phase (60 sec.)			215°C
Infrared (15 sec.)			220°C

Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LP124 Typ	LP124 Tested Limit (Note 6)	LP124 Design Limit (Note 7)	LP2902 (Note 8) Typ	LP2902 (Note 8) Tested Limit (Note 6)	LP2902 (Note 8) Design Limit (Note 7)	LP324 Typ	LP324 Tested Limit (Note 6)	LP324 Design Limit (Note 7)	Units Limits
V_{os}	Input Offset Voltage		1	2 **4**	**7**	2	4	**10**	2	4	**9**	mV (Max)
I_b	Input Bias Current		1	4 **8**	**8**	2	20	**40**	2	10	**20**	nA (Max)
I_{os}	Input Offset Current		0.1	1 **2**	**2**	0.5	4	**8**	0.2	2	**4**	nA (Max)
A_{vol}	Voltage Gain	$R_L = 10k$ to GND $V^+ = 30V$	100	70 **60**	**60**	70	40	**30**	100	50	**40**	V/mV (Min)
CMRR	Common Mode Rej. Ratio	$V^+ = 30V$ $0V \leq V_{cm}$ $V_{cm} < V^+ - 1.5$	100	85 **80**	**75**	90	80	**75**	90	80	**75**	dB (Min)
PSRR	Power Supply Rej. Ratio	$V^+ = 5V$ to 30V	100	85 **80**	**75**	90	80	**75**	90	80	**75**	dB (Min)
I_s	Supply Current	$R_L = \infty$	85	125 **150**	**200**	85	150	**250**	85	150	**250**	μA (Max)
V_o	Output Voltage Swing	$I_L = 350\ \mu A$ to GND. $V_{cm} = 0V$	3.6	3.4 3.1	**$V^+ - 1.9V$**	3.6	3.4	**$V^+ - 1.9V$**	3.6	3.4	**$V^+ - 1.9V$**	V (Min)
		$I_L = 350\ \mu A$ to V^+ $V_{cm} = 0V$	0.7	0.8 **1.0**	**1.0**	0.7	0.8	**1.0**	0.7	0.8	**1.0**	V (Max)
I_{out} Source	Output Source Current	$V_o = 3V$ V_{in} (diff) = 1V	11	9 **4**	**4**	10	7	**4**	10	7	**4**	mA (Min)
I_{out} Sink	Output Sink Current	$V_o = 1.5V$ V_{in} (diff) = 1V	6	5 **4**	**4**	5	4	**3**	5	4	**3**	mA (Min)
I_{out} Sink	Output Sink Current	$V_o = 1.5V$ $V_{cm} = 0V$	5	3 **0.5**	**1.5**	4	2	**1**	4	2	**1**	mA (Min)
I_{source}	Output Short to GND	V_{in} (diff) = 1V	20	25 **35**	**35**	20	25 **35**	**35**	20	25 **35**	**35**	mA (Max)

Electrical Characteristics (Note 5) (Continued)

Symbol	Parameter	Conditions	LP124			LP2902 (Note 8)			LP324			Units Limits
			Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	
I_{sink}	Output Short to V^+	V_{in} (diff) = 1V	15	20 **25**	**35**	15	20	**35**	15	20	**35**	mA (Max)
V_{os} Drift			7			10			10			μV/C°
I_{os} Drift			5			10			10			pA/C°
GBW	Gain Bandwidth Product		100			100			100			KHz
S_r	Slew Rate		50			50			50			V/mS

Note 1: The input voltage is not allowed to go more than −0.3V below V^- (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V_{DC}, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{ja} and T_j max. $T_j = T_A + \theta_{ja}P_D$.

Note 4: The LP124 may be operated from $-55°C \le T_A \le +125°C$. The LP2902 may be operated from $-40°C \le T_A \le +85°C$, and the LP324 may be operated from $0°C \le T_A \le +70°C$.

Note 5: Boldface numbers apply at temperature extremes. All other numbers apply only at $T_A = T_j = 25°C$, $V^+ = 5V$, $V_{cm} = V/2$, and $R_L = 100k$ connected to GND unless otherwise specified.

Note 6: Guaranteed and 100% production tested.

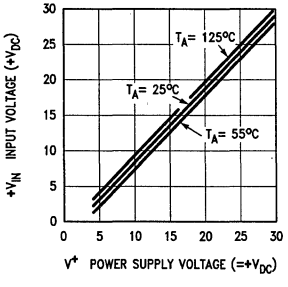
Note 7: Guaranteed (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP124, LP324, and 3.0V to 26V for the LP2902), and the common mode range (0V to $V^+ - 1.5V$), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

Note 8: The LP2902 operating supply range is 3V to 26V, and is not tested above 26V.

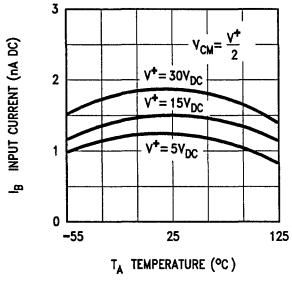
Note 9: The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Typical Performance Curves

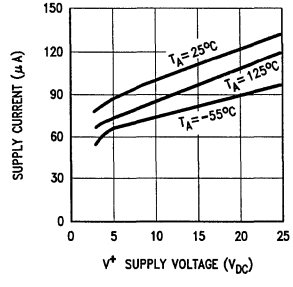
Input Voltage Range



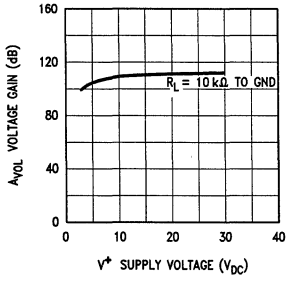
Input Current



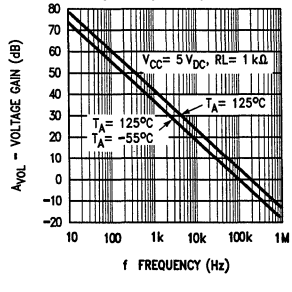
Supply Current



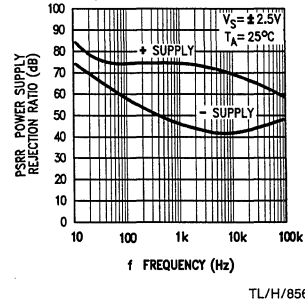
Voltage Gain



Open Loop Frequency Response



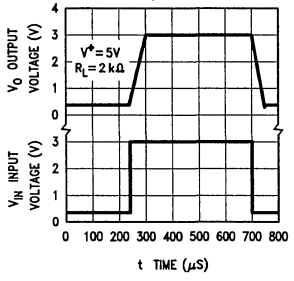
Power Supply Rejection Ratio



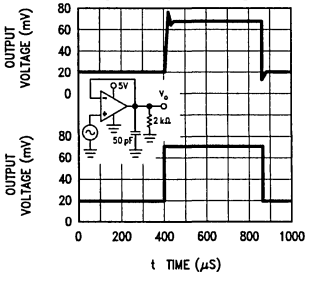
TL/H/8562–18

Typical Performance Curves (Continued)

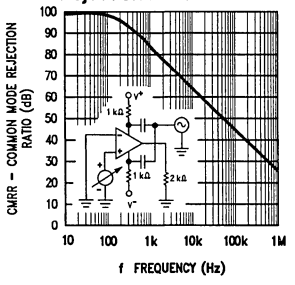
Voltage Follower Pulse Response



Voltage Follower Pulse Response (Small Signal)

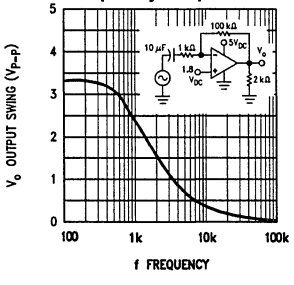


Common Mode Rejection Ratio

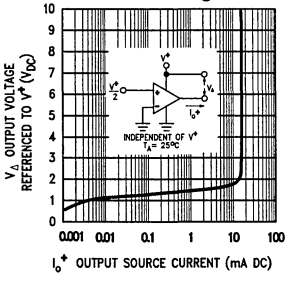


TL/H/8562–20

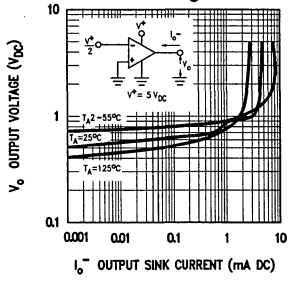
Large Signal Frequency Response



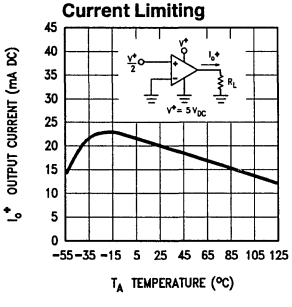
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



TL/H/8562–19

Application Hints

The LP124 series is a micro-power pin-for-pin equivalent to the LM124 op amps. Power supply current, input bias current, and input offset current have all been reduced by a factor of 10 over the LM124. Like its predecessor, the LP124 series op amps can operate on single supply, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or the unit is not inadvertently installed backwards in the test socket as an unlimited current surge through the resulting forward diode within the IC could destroy the unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

The amplifiers have a class B output stage which allows the amplifiers to both source and sink output currents. In applications where crossover distortion is undesirable, a resistor

Application Hints (Continued)

should be used from the output of the amplifier to ground. The resistor biases the output into class A operation.

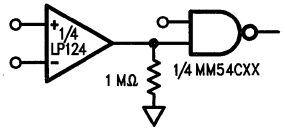
The LP124 has improved stability margin for driving capacitive loads. No special precautions are needed to drive loads in the 50 pF to 1000 pF range. It should be noted however that since the power supply current has been reduced by a factor of 10, so also has the slew rate and gain bandwidth product. This reduction can cause reduced performance in AC applications where the LM124 is being replaced by an LP124. Such situations usually occur when the LM124 has been operated near its power bandwidth.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example: If all four amplifiers were simultaneously shorted to ground on a 10V supply the junction temperature would rise by 110°C.

Exceeding the negative common-mode limit on either input will cause a reversal of phase to the output and force the amplifier to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a low state. In neither case does a latch occur since returning the input within the common mode range puts the input stage and thus the amplifier in a normal operating mode.

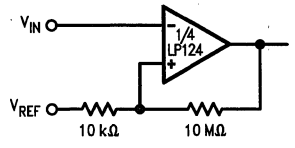
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference to $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Driving CMOS



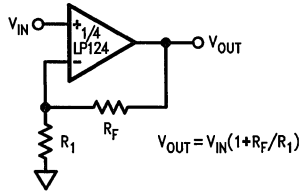
TL/H/8562–3

Comparator with Hysteresis



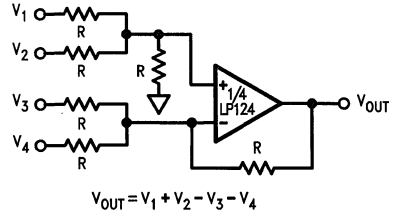
TL/H/8562–6

Non-Inverting Amplifier



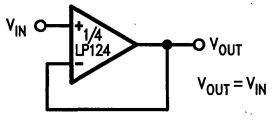
TL/H/8562–4

Adder/Subtractor



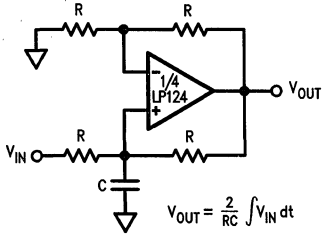
TL/H/8562–7

Unity Gain Buffer



TL/H/8562–5

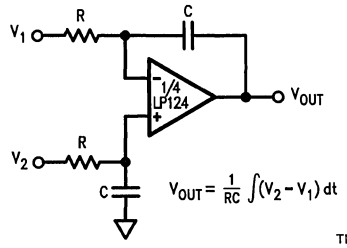
Positive Integrator



TL/H/8562–8

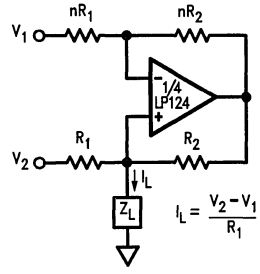
Application Hints (Continued)

Differential Integrator



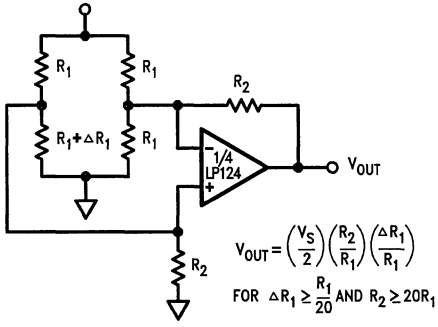
TL/H/8562–9

Howland Current Pump



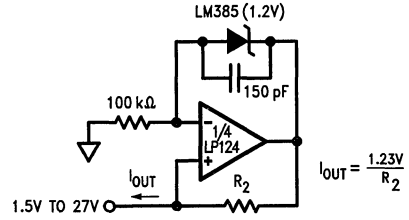
TL/H/8562–10

Bridge Current Amplifier



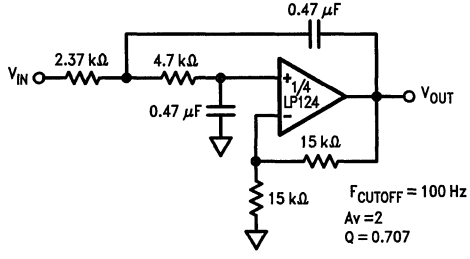
TL/H/8562–11

μ Power Current Source



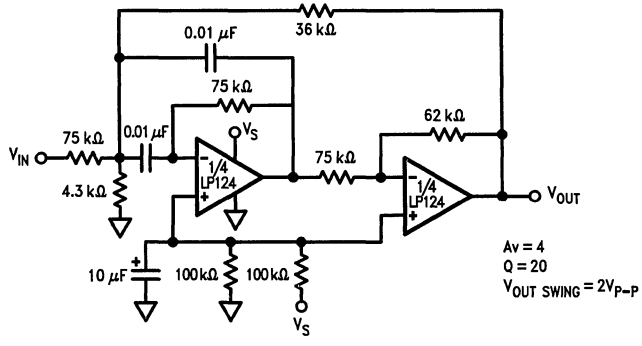
TL/H/8562–12

Lowpass Filter



TL/H/8562–13

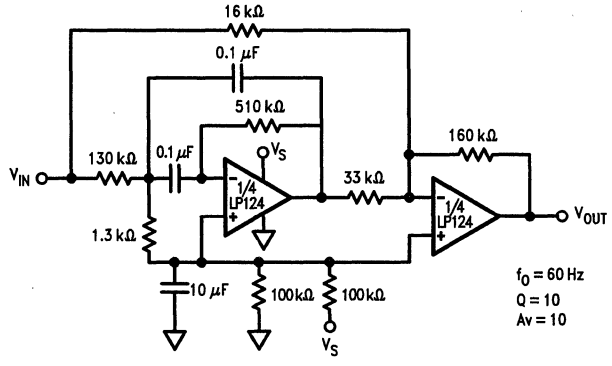
1 kHz Bandpass Active Filter



TL/H/8562–14

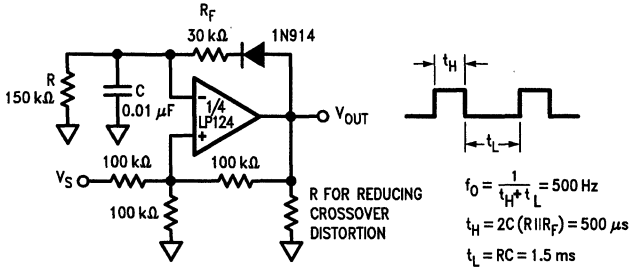
Application Hints (Continued)

Band-Reject Filter



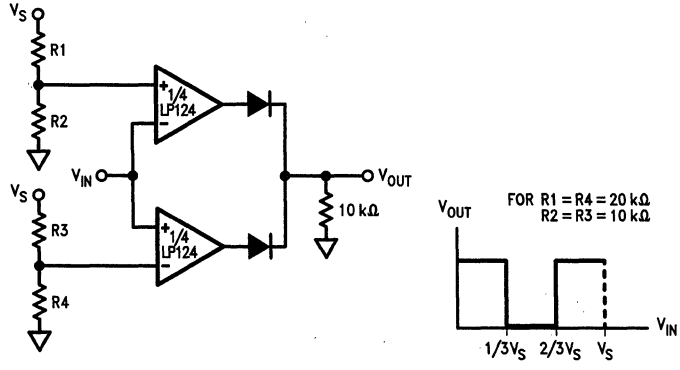
TL/H/8562–15

Pulse Generator



TL/H/8562–16

Window Comparator



TL/H/8562–17

National Semiconductor

LPC660AM/LPC660AI/LPC660I CMOS Quad Operational Amplifier

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier with these same features.

Applications

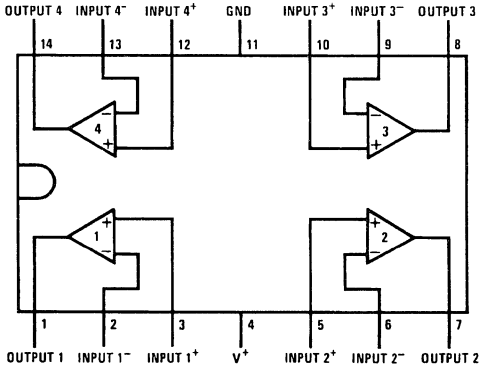
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (1 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain — 120 dB
- Low input offset voltage — 3 mV max
- Low offset voltage drift — 1.3 μV/°C
- Ultra low input bias current — 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- Low distortion — 0.01% at 1 kHz
- Slew rate — 0.11 V/μs
- Insensitive to latch-up

Connection Diagram

Dual-In-Line Package



TL/H/10547–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Industrial	
14-Pin Cavity DIP	LPC660AMD		D14E
14-Pin Small Outline		LPC660AIM or LPC660IM	M14A
14-Pin Molded DIP		LPC660AIN or LPC660IN	N14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C

ESD rating is to be determined.

Operating Ratings

Temperature Range	
LPC660AM	$-55°C \le T_J \le +125°C$
LPC660AI	$-40°C \le T_J \le +85°C$
LPC660I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM Limit (Note 4)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV max
			3.5	**3.3**	**6.3**	
Input Offset Voltage Average Drift		1.3				μV/°C
Input Bias Current	(Note 8)	0.04	20	20	20	pA max
			100	**4**	**4**	
Input Offset Current	(Note 8)	0.01	20	20	20	pA max
			100	**2**	**2**	
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB min
			68	**68**	**61**	
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70	70	63	dB min
			68	**68**	**61**	
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB min
			82	**83**	**73**	
Input Common Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR > 50 dB	−0.4	−0.1	−0.1	−0.1	V max
			0	**0**	**0**	
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V min
			$V^+ - 2.6$	**$V^+ - 2.5$**	**$V^+ - 2.5$**	
Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	$R_L = 5 k\Omega$ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC660AM Limit (Note 4)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 5V$ $R_L = 5\ k\Omega$ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 15V$ $R_L = 5\ k\Omega$ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, $V_O = 5V$	21	16	16	13	mA min
			12	**14**	**11**	
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, $V_O = 13V$	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	All Four Amplifiers $V_O = 1.5V$	160	200	200	240	μA max
			250	**230**	**270**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM Limit (Note 4)	LPC660AI Limit (Note 4)	LPC660I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs min
			0.04	**0.05**	**0.03**	
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 101°C/W, the molded plastic SO (M) package is 152°C/W, and the cavity DIP (D) package is 124°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

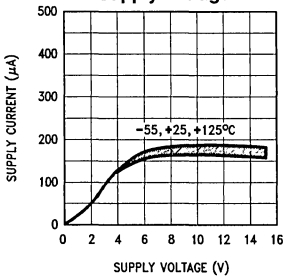
Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

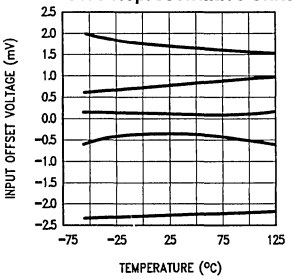
Note 8: The LPC660AI and the LPC660I input bias current and input offset current specifications over the temperature range are guaranteed through correlation techniques; these numbers reflect the true performance of the part. All other input bias and offset current specifications (other than the typical) are measured; these numbers are degraded in order to reduce the test time (and the cost of the part) taken in measuring these parameters.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

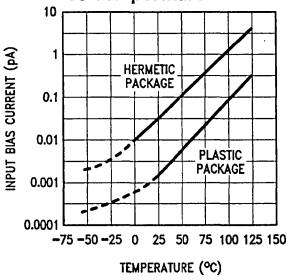
Supply Current vs Supply Voltage



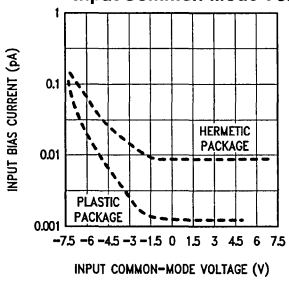
Offset Voltage vs Temperature of Five Representative Units



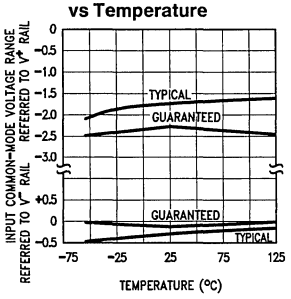
Input Bias Current vs Temperature



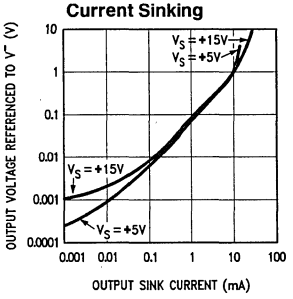
Input Bias Current vs Input Common-Mode Voltage



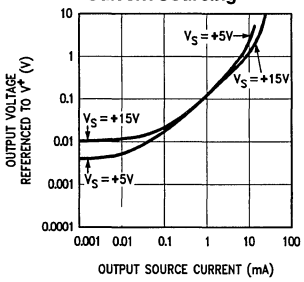
Common-Mode Voltage Range vs Temperature



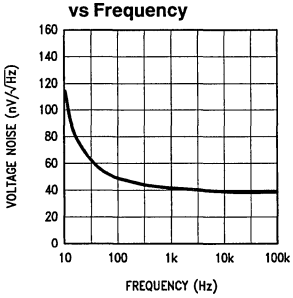
Output Characteristics Current Sinking



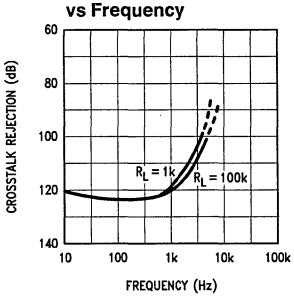
Output Characteristics Current Sourcing



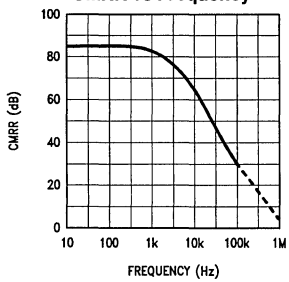
Input Voltage Noise vs Frequency



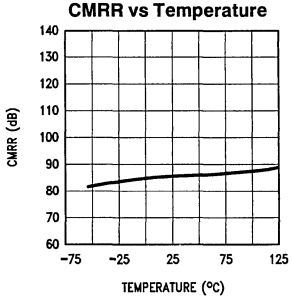
Crosstalk Rejection vs Frequency



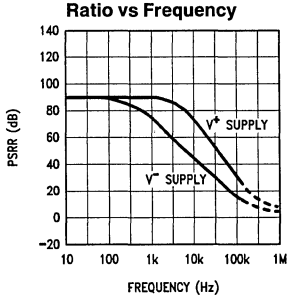
CMRR vs Frequency



CMRR vs Temperature



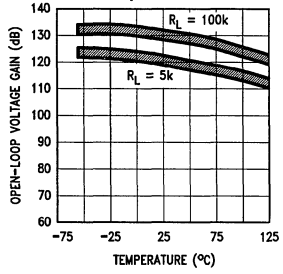
Power Supply Rejection Ratio vs Frequency



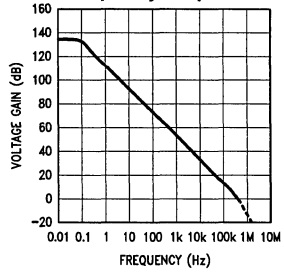
TL/H/10547–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

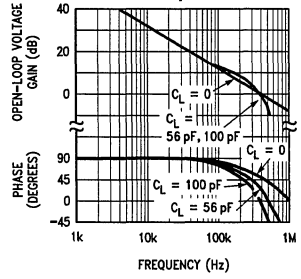
Open-Loop Voltage Gain vs Temperature



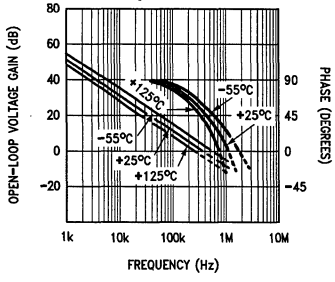
Open-Loop Frequency Response



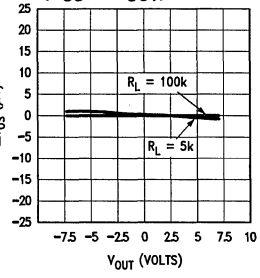
Gain and Phase Responses vs Load Capacitance



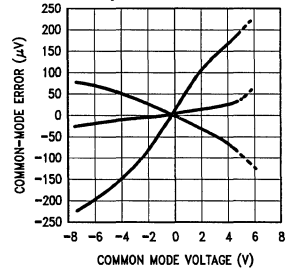
Gain and Phase Responses vs Temperature



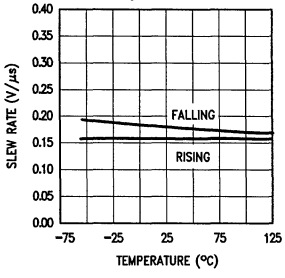
Gain Error (V_{OS} vs V_{OUT})



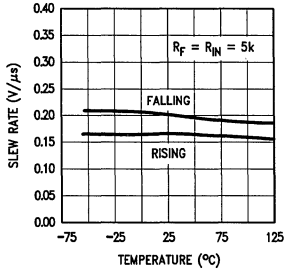
Common-Mode Error of 3 Representative Units



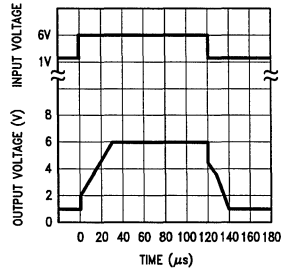
Non-Inverting Slew Rate vs Temperature



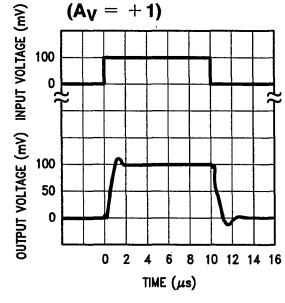
Inverting Slew Rate vs Temperature



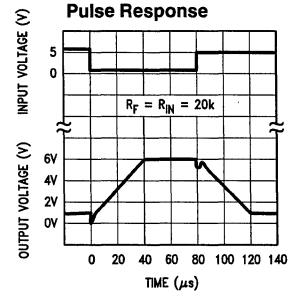
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



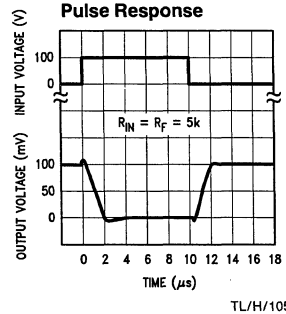
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



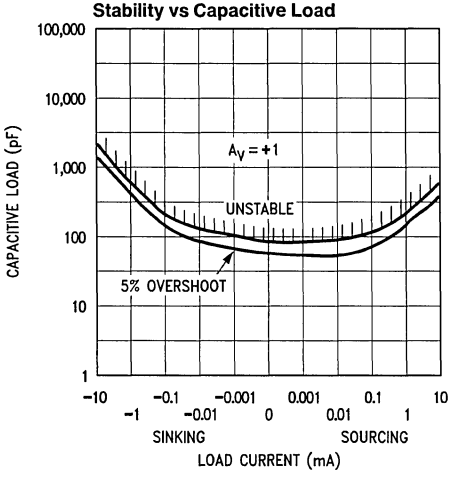
Inverting Small-Signal Pulse Response



TL/H/10547–3

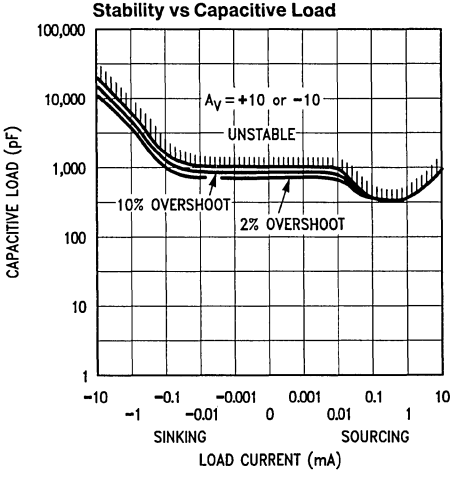
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)

Stability vs Capacitive Load



TL/H/10547–4

Stability vs Capacitive Load



TL/H/10547–5

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

3

National Semiconductor

LPC662AM/LPC662AI/LPC662I CMOS Dual Operational Amplifier

General Description

The LPC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It is fully specified for operation from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier with these same features.

Applications

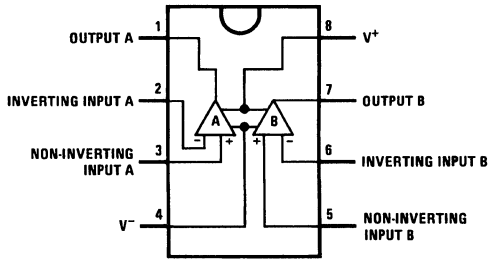
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (<0.5 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain — 120 dB
- Low input offset voltage — 3 mV max
- Low offset voltage drift — 1.3 μV/°C
- Ultra low input bias current — 40 fA
- Input common-mode includes GND
- Operation guaranteed from +5V to +15V
- Low distortion — 0.01% at 1 kHz
- Slew rate — 0.11 V/μs
- Insensitive to latch-up

Connection Diagram

8-Pin DIP



TL/H/10548–1

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Industrial	
8-Pin Cavity DIP	LPC662AMD		D08C
8-Pin Small Outline		LPC662AIM or LPC662IM	M08A
8-Pin Molded DIP		LPC662AIN or LPC662IN	N08E

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Either Input beyond V^+ or V^-	0.7V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to GND (Note 1)	Continuous
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C

ESD rating is to be determined.

Operating Ratings

Temperature Range	
LPC662AM	$-55°C \le T_J \le +125°C$
LPC662AI	$-40°C \le T_J \le +85°C$
LPC662I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM Limit (Note 4)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV max
			3.5	**3.3**	**6.3**	
Input Offset Voltage Average Drift		1.3				µV/°C
Input Bias Current	(Note 8)	0.04	20	20	20	pA max
			100	**4**	**4**	
Input Offset Current	(Note 8)	0.01	20	20	20	pA max
			100	**2**	**2**	
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB min
			68	**68**	**61**	
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70	70	63	dB min
			68	**68**	**61**	
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB min
			82	**83**	**73**	
Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB	−0.4	−0.1	−0.1	−0.1	V max
			0	**0**	**0**	
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V min
			$V^+ - 2.6$	**$V^+ - 2.5$**	**$V^+ - 2.5$**	
Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	$R_L = 5 k\Omega$ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC662AM Limit (Note 4)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Output Swing	$V^+ = 5V$ $R_L = 100 k\Omega$ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 5V$ $R_L = 5 k\Omega$ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	$V^+ = 15V$ $R_L = 100 k\Omega$ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	$V^+ = 15V$ $R_L = 5 k\Omega$ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, $V_O = 5V$	21	16	16	13	mA min
			12	**14**	**11**	
Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, $V_O = 13V$	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	Both Amplifiers $V_O = 1.5V$	86	120	120	140	μA max
			145	**140**	**160**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM Limit (Note 4)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs min
			0.04	**0.05**	**0.03**	
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/√Hz
Input Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 101°C/W, the molded plastic SO (M) package is 152°C/W, and the cavity DIP (D) package is 124°C/W. All numbers apply for packages soldered directly into a PC board.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: These limits are guaranteed and are used in calculating outgoing AQL.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

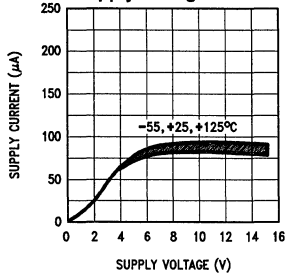
Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

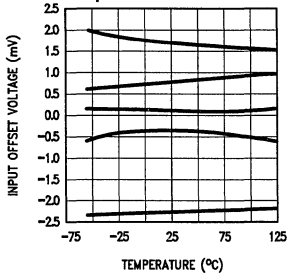
Note 8: The LPC662AI and the LPC662I input bias current and input offset current specifications over the temperature range are guaranteed through correlation techniques; these numbers reflect the true performance of the part. All other input bias and offset current specifications (other than the typical) are measured; these numbers are degraded in order to reduce the test time (and the cost of the part) taken in measuring these parameters.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

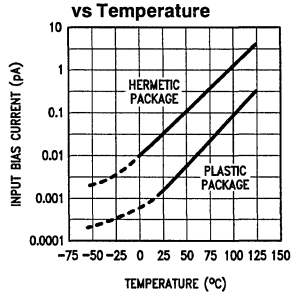
Supply Current vs Supply Voltage



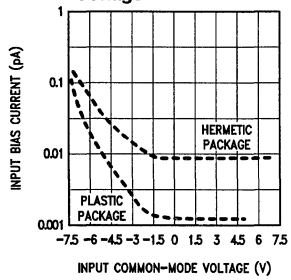
Offset Voltage vs Temperature of Five Representative Units



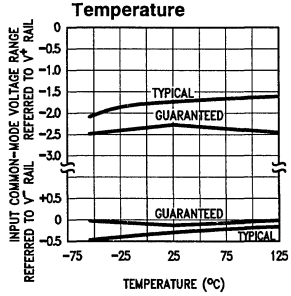
Input Bias Current vs Temperature



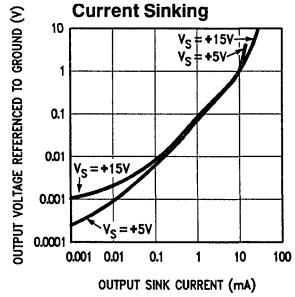
Input Bias Current vs Input Common-Mode Voltage



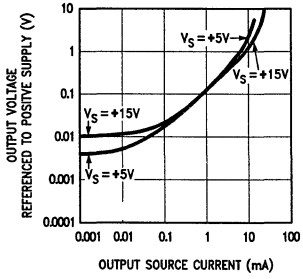
Input Common-Mode Voltage Range vs Temperature



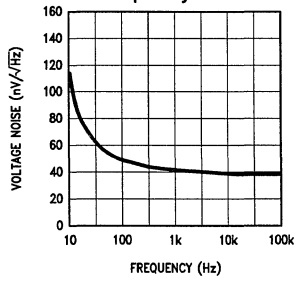
Output Characteristics Current Sinking



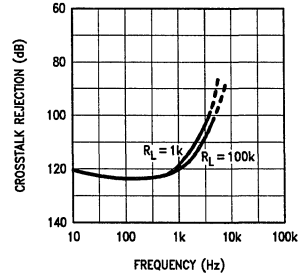
Output Characteristics Current Sourcing



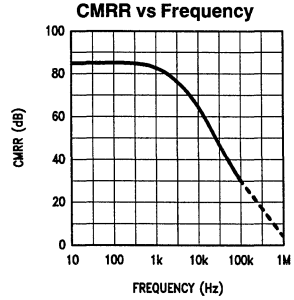
Input Voltage Noise vs Frequency



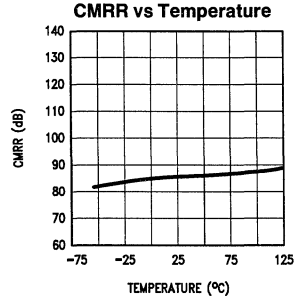
Crosstalk Rejection vs Frequency



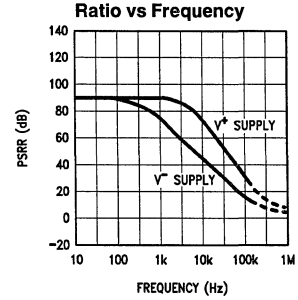
CMRR vs Frequency



CMRR vs Temperature



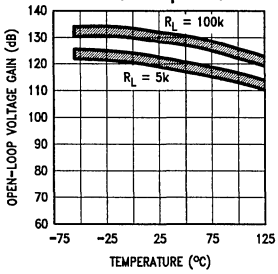
Power Supply Rejection Ratio vs Frequency



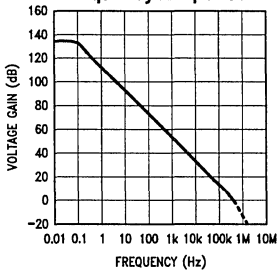
TL/H/10548–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

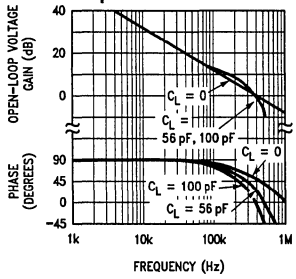
Open-Loop Voltage Gain vs Temperature



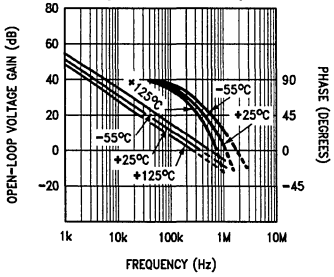
Open-Loop Frequency Response



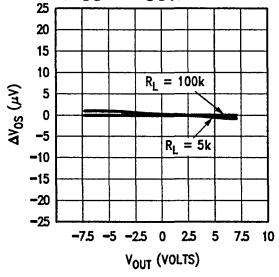
Gain and Phase Responses vs Load Capacitance



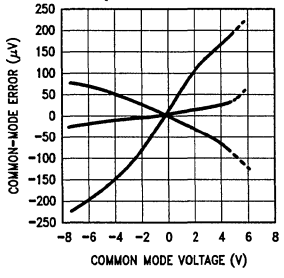
Gain and Phase Responses vs Temperature



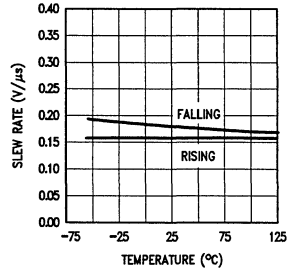
Gain Error (V_{OS} vs V_{OUT})



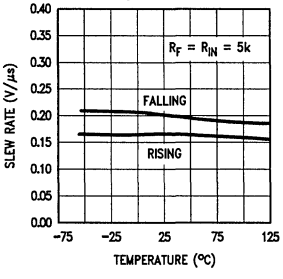
Common-Mode Error vs Common-Mode Voltage of 3 Representative Units



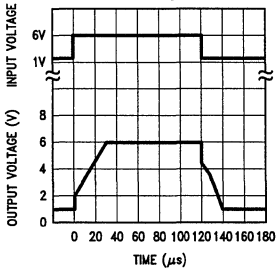
Non-Inverting Slew Rate vs Temperature



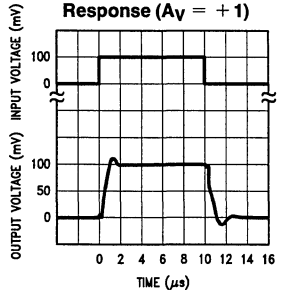
Inverting Slew Rate vs Temperature



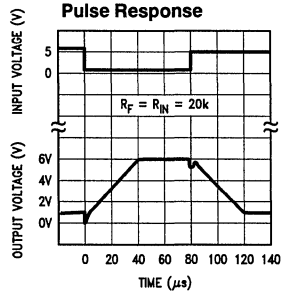
Non-Inverting Large-Signal Pulse Response (A_V = +1)



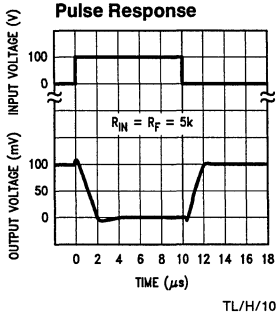
Non-Inverting Small-Signal Pulse Response (A_V = +1)



Inverting Large-Signal Pulse Response



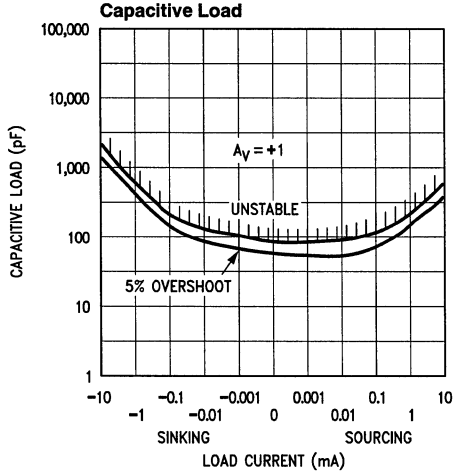
Inverting Small-Signal Pulse Response



TL/H/10548–3

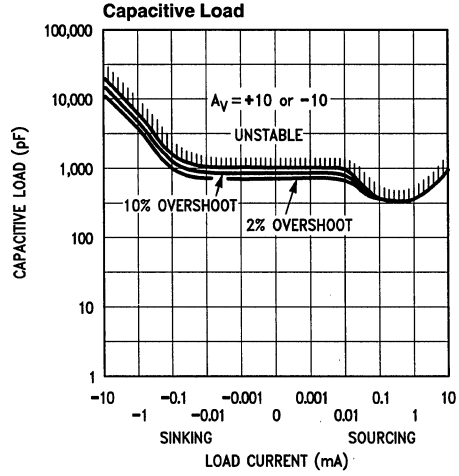
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)

Stability vs Capacitive Load



TL/H/10548–4

Stability vs Capacitive Load



TL/H/10548–5

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

National Semiconductor

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage (25 μV max. for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current (±2 nA for OP-07A) and high open-loop gain (300 V/mV for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

Features

Low V_{OS}	25 μV Max
Low V_{OS} Drift	0.6 μV/°C Max
Ultra-Stable vs Time	1.0 μV/Month Max
Low Noise	0.6 μVp-p Max
Wide Input Voltage Range	±14V
Wide Supply Voltage Range	±3V to ±18V

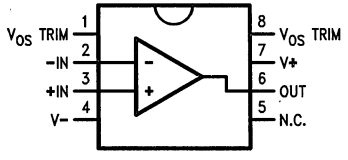
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the μA714

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagrams

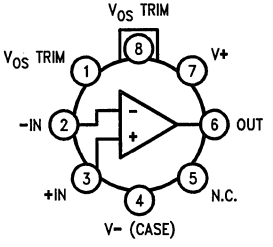
Dual-In-Line Package



TL/H/10550–1

See NS Package Number J08A or N08E

Metal Can Package



TL/H/10550–2

See NS Package Number H08C

Ordering Information

T_A = 25°C V_{OS}Max (μV)	H08C TO-99	Package J08A CERDIP	N08E Plastic	Operating Temperature Range
25	OP-07AJ*	OP-07AZ*		MIL
75	OP-07EJ	OP-07EZ	OP-07EP	COM
75	OP-07J*	OP-07Z*		MIL
150	OP-07CJ	OP-07CZ	OP-07CP	COM
150	OP-07DJ		OP-07DP	COM

*For devices processed in total compliance to military specifications refer to RETSOP07X for OP-07.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
J and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	−65°C to +150°C

Operating Temperature Range

OP-07A, OP-07,	−55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C

Electrical Characteristics

Unless otherwise specified, V_S = ±15V, T_A = 25°C. **Boldface** type refers to limits over −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	OP-07A			OP-07			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1) (Note 1)		10 **25**	25 **60**		30 **60**	75 **200**	μV
$\Delta V_{OS/t}$	Long-Term Input Offset Voltage Stability	(Note 2)		0.2	1.0		0.2	1.0	μV/Mo
I_{OS}	Input Offset Current			0.3 **0.8**	2.0 **4**		0.4 **1.2**	2.8 **5.6**	nA
I_B	Input Bias Current			±0.7 **±1**	±2.0 **±4**		±1.0 **±2**	±3.0 **±6**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.35	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		14	30	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	30	80		20	60		MΩ
R_{INCM}	Input Resistance Common-Mode			200			200		GΩ
IVR	Input Voltage Range		±13.0 **±13.0**	±14.0 **±13.5**		±13.0 **±13.0**	±14.0 **±13.5**		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	110 **106**	126 **123**		110 **106**	126 **123**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		4 **5**	10 **20**		4 **5**	10 **20**	μV/V
A_{VO}	Large-Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 500Ω, V_O = ±0.5V, V_S = ±3V (Note 4)	300 **200** 150	500 **400** 400		200 **150** 150	500 **400** 400		V/mV
V_O	Output Voltage Swing	R_L ≥ 10 kΩ R_L ≥ 2 kΩ R_L ≥ 2 kΩ R_L ≥ 1 kΩ	±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		V

Electrical Characteristics (Continued)

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $-55°C \leq T_A \leq +125°C$

Symbol	Parameter	Conditions	OP-07A			OP-07			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$R_L \geq 2\,k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Open-Loop Output Resistance	$V_O = 0, I_O = 0$		60			60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6		75 4	120 6	mW
	Offset Adj. Range	$R_P = 20\,k\Omega$		±4			±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 3)		**0.2**	**0.6**		**0.3**	**1.3**	μV/°C
TCV_{OSn}	With External Trim	$R_P = 20\,k\Omega$ (Note 4)		**0.2**	**0.6**		**0.3**	**1.3**	
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**5**	**25**		**8**	**50**	pA/°C
TCI_B	Average Input Bias Drift	(Note 3)		**8**	**25**		**13**	**50**	pA/°C

Note 1: OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 second after application of power.

Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

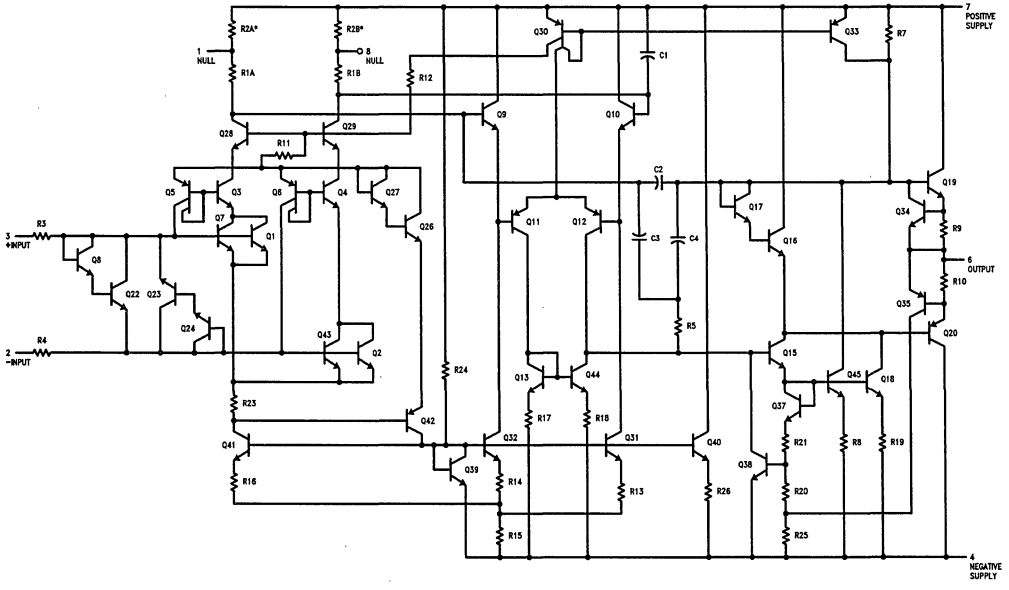
Note 3: Sample tested.

Note 4: Guaranteed by design.

Note 5: The typical θ_{JA} of the H08 (TO-99) package is 155°C/W, the J08 (CERDIP) package is 92° C/W and the N08 (Molded DIP) is 100° C/W. The typical θ_{JC} of the H08 package is 17.5° C/W. All numbers apply for packages soldered directly into an etched circuit board.

Note 6: For supply voltages of less than ±22V, the maximum input voltage is 0.5V beyond either supply.

Simplified Schematic



TL/H/10550–3

*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \le T_A \le 70°C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		30 **45**	75 **130**		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.3	1.5		0.4	2.0	μV/Mo
I_{OS}	Input Offset Current			0.5 **0.9**	3.8 **5.3**		0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±1.2 **±1.5**	±4.0 **±5.5**		±1.8 **±2.2**	±7.0 **±9.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		MΩ
R_{INCM}	Input Resistance Common-Mode			160			120		GΩ
IVR	Input Voltage Range		±13.0	±14.0		±13	±14		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	106 **103**	123 **123**		100 **97**	120 **120**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V V_S = ±3V to ±18V		5 **7**	20 **32**		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \ge 2$ kΩ, V_O = ±10V $R_L \ge 2$ kΩ $R_L \ge 500Ω$, V_O = ±0.5V, V_S = ±3V (Note 4)	200 **180** 150	500 **450** 400		120 **100** 100	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \ge 10$ kΩ $R_L \ge 2$ kΩ $R_L \ge 2$ kΩ $R_L \ge 1$ kΩ	±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \ge 2$ kΩ (Note 3)	0.1	0.3		0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	A_{VCL} = +1 (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Output Resistance	V_O = 0, I_O = 0		60			60		Ω
P_d	Power Consumption	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	R_P = 20 kΩ		±4			±4		mV
TCV_{OS} TCV_{OSn}	Average Input Offset Voltage Drift Without External Trim With External Trim	(Note 4) R_P = 20 kΩ (Note 4)		**0.3** **0.3**	**1.3** **1.3**		**0.5** **0.4**	**1.8** **1.6**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**35**		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**13**	**35**		**18**	**50**	pA/°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.5	3.0	μV/Mo
I_{OS}	Input Offset Current			0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±2.0 **±3.0**	±12.0 **±14.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	μVp-p
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pAp-p
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
R_{IN}	Input Resistance Differential-Mode	(Note 4)	7	31		MΩ
R_{INCM}	Input Resistance Common-Mode			120		GΩ
IVR	Input Voltage Range		±13	±14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	94 **94**	110 **106**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to ±18V		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \leq 2 k\Omega$, $V_O = \pm 10V$ $R_L = 2 k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, V_S ±3V (Note 4)	120 **100**	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$	±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \geq 2 k\Omega$ (Note 3)	0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
RO	Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20 k\Omega$		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 4)		**0.7**	**2.5**	μV/°C
TCV_{OSn}	With External Trim	$R_P = 20 k\Omega$ (Note 4)		**0.7**	**2.5**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**18**	**50**	pA/°C

Note 1: OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 second after application of power.

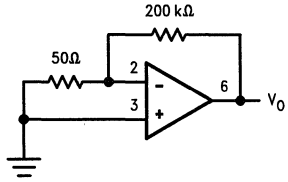
Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample Tested.

Note 4: Guaranteed by design.

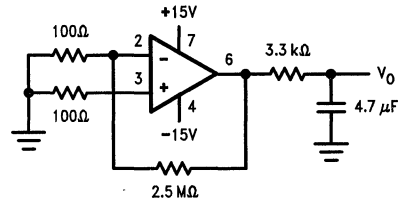
Test Circuits

Offset Voltage Test Circuit



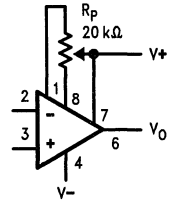
TL/H/10550–4

Low Frequency Noise Test Circuit



TL/H/10550–5

Optional Offset Nulling Circuit



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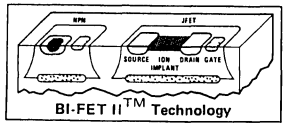
National Semiconductor



TL081CP Wide Bandwidth JFET Input Operational Amplifier

General Description

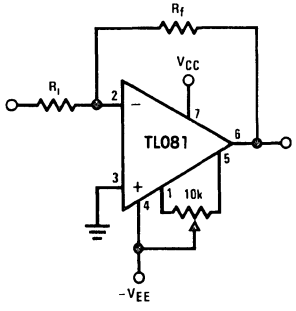
The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

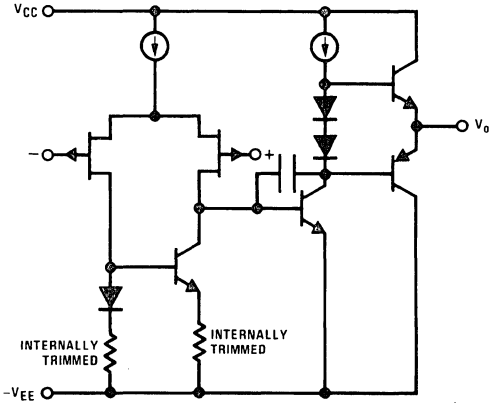
Internally trimmed offset voltage	15 mV
Low input bias current	50 pA
Low input noise voltage	25 nV/$\sqrt{\text{Hz}}$
Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
Wide gain bandwidth	4 MHz
High slew rate	13 V/μs
Low supply current	1.8 mA
High input impedance	$10^{12}\Omega$
Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz	<0.02%
Low 1/f noise corner	50 Hz
Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/8358–1

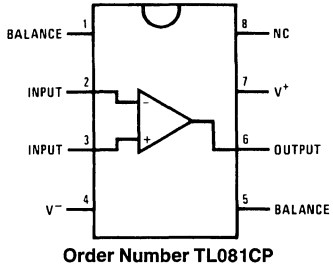
Simplified Schematic



TL/H/8358–2

Connection Diagram

Dual-In-Line Package



TL/H/8358–4

Order Number TL081CP
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
θ_{jA}	120°C/W

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	2.8	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 120°C/W junction to ambient for N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

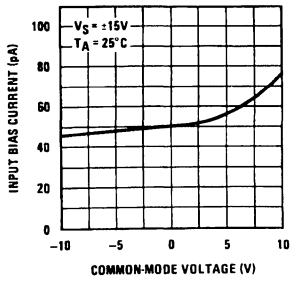
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ±5V to ±15V.

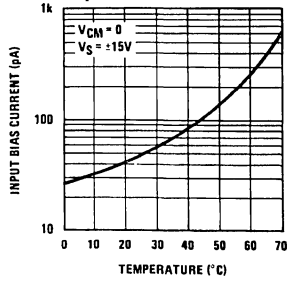
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

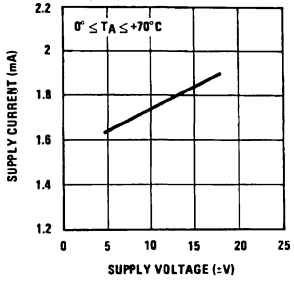
Input Bias Current



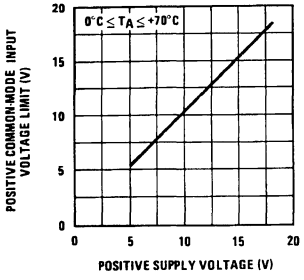
Input Bias Current



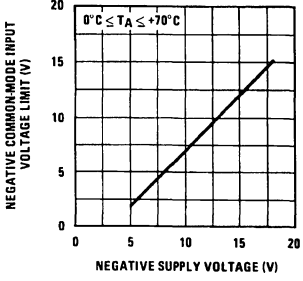
Supply Current



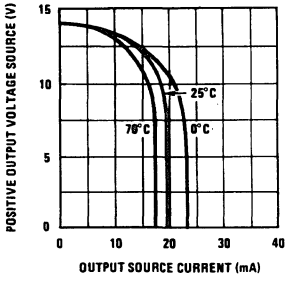
Positive Common-Mode Input Voltage Limit



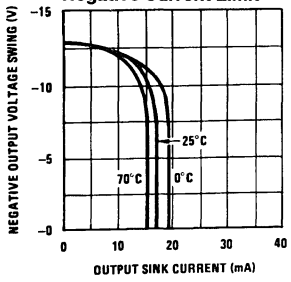
Negative Common-Mode Input Voltage Limit



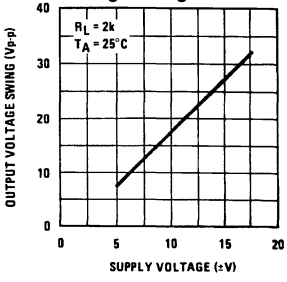
Positive Current Limit



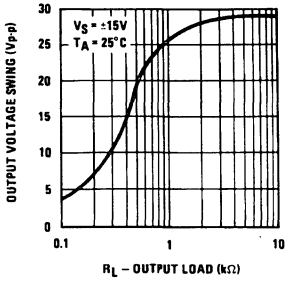
Negative Current Limit



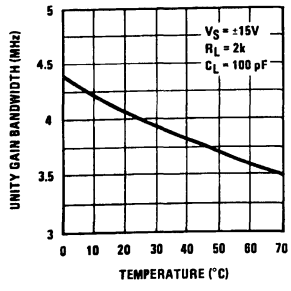
Voltage Swing



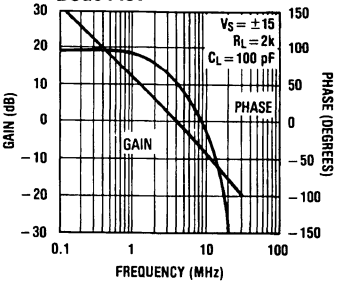
Output Voltage Swing



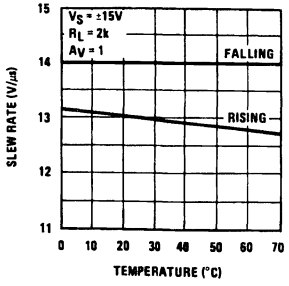
Gain Bandwidth



Bode Plot



Slew Rate

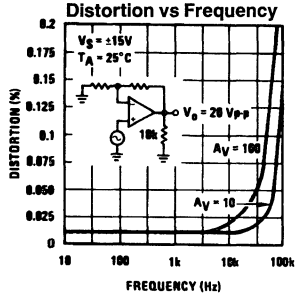


TL/H/8358–5

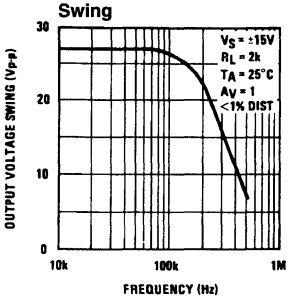
3

Typical Performance Characteristics (Continued)

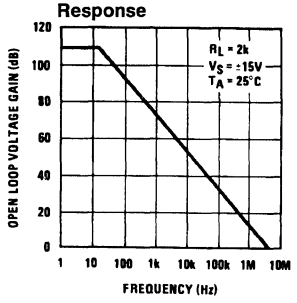
Distortion vs Frequency



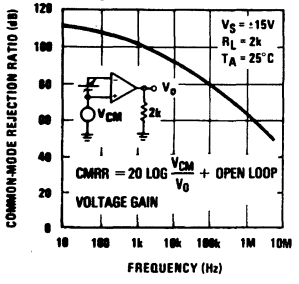
Undistorted Output Voltage Swing



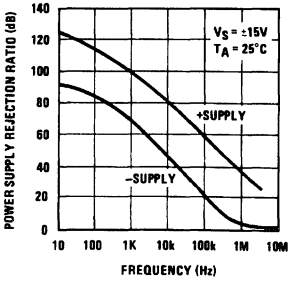
Open Loop Frequency Response



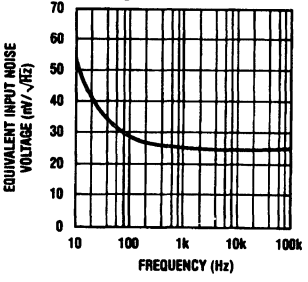
Common-Mode Rejection Ratio



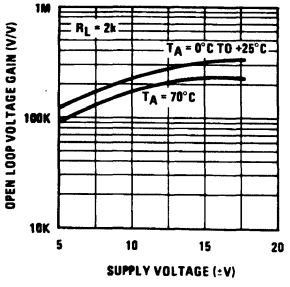
Power Supply Rejection Ratio



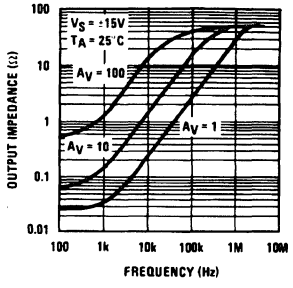
Equivalent Input Noise Voltage



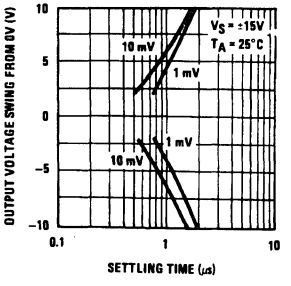
Open Loop Voltage Gain (V/V)



Output Impedance



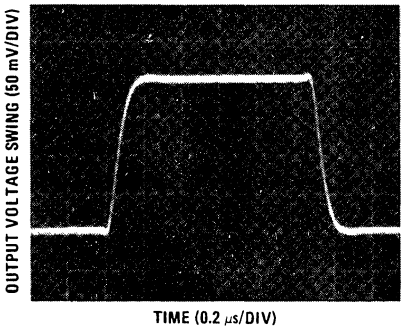
Inverter Settling Time



TL/H/8358–6

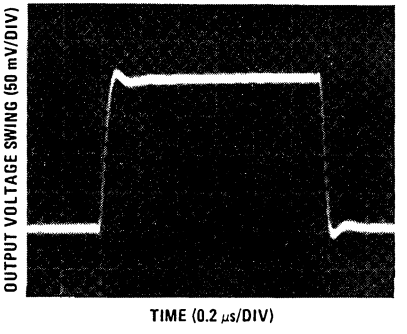
Pulse Response

Small Signal Inverting



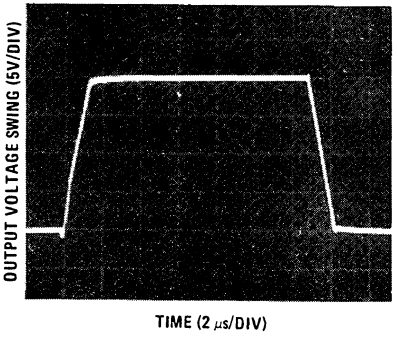
TL/H/8358–7

Small Signal Non-Inverting



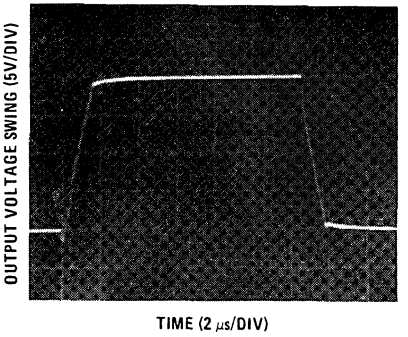
TL/H/8358–13

Large Signal Inverting



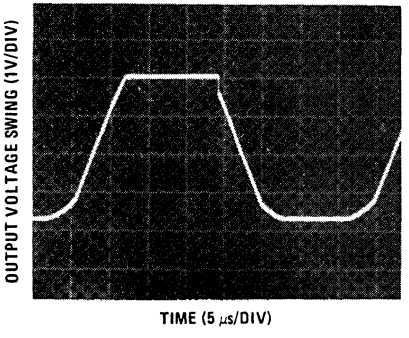
TL/H/8358–14

Large Signal Non-Inverting



TL/H/8358–15

Current Limit (R_L = 100Ω)



TL/H/8358–16

Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

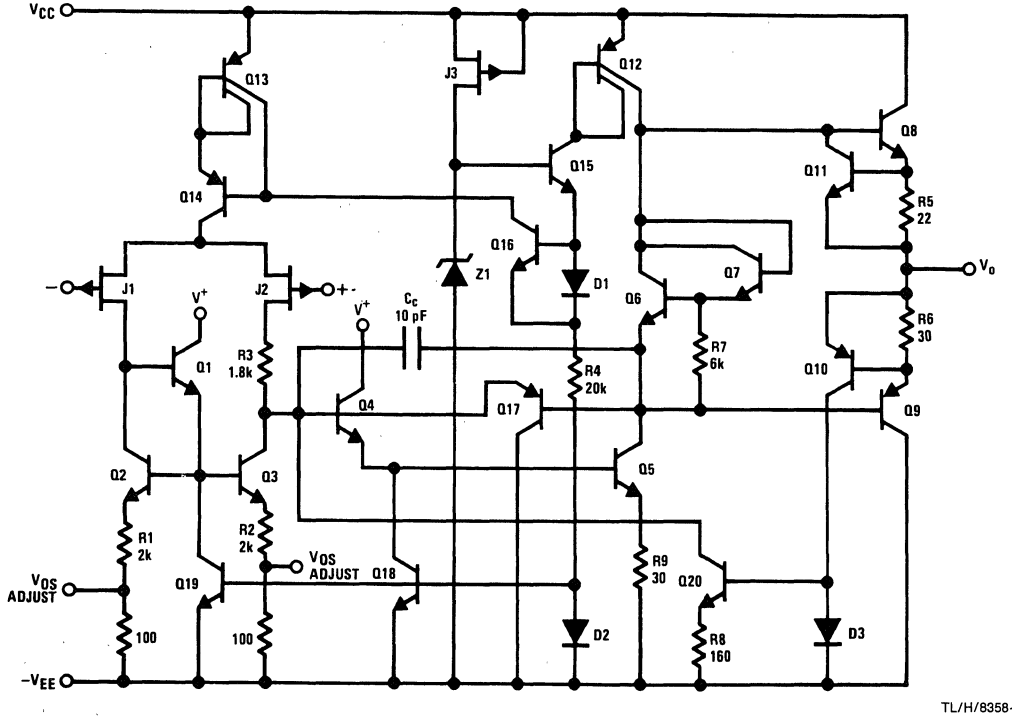
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

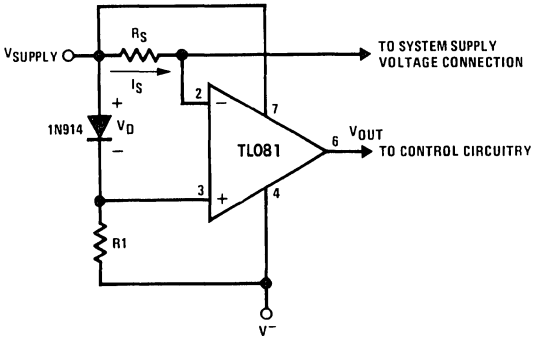
Detailed Schematic



TL/H/8358–8

Typical Applications

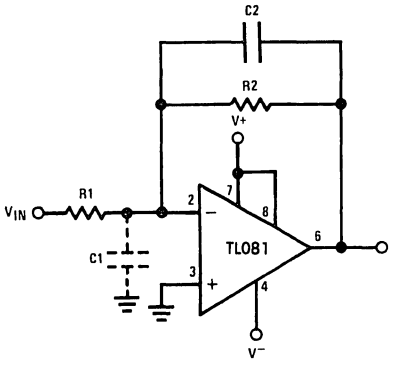
Supply Current Indicator/Limiter



TL/H/8358–9

• V_{OUT} switches high when $R_S I_S > V_D$

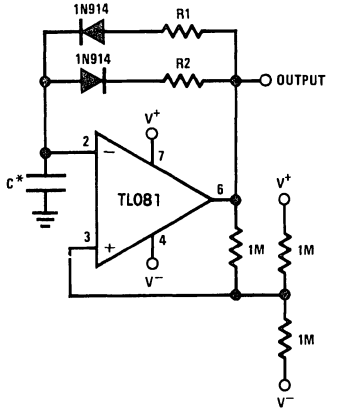
Hi-Z_{IN} Inverting Amplifier



TL/H/8358–10

Parasitic input capacitance C1 ≅ (3 pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



TL/H/8358–11

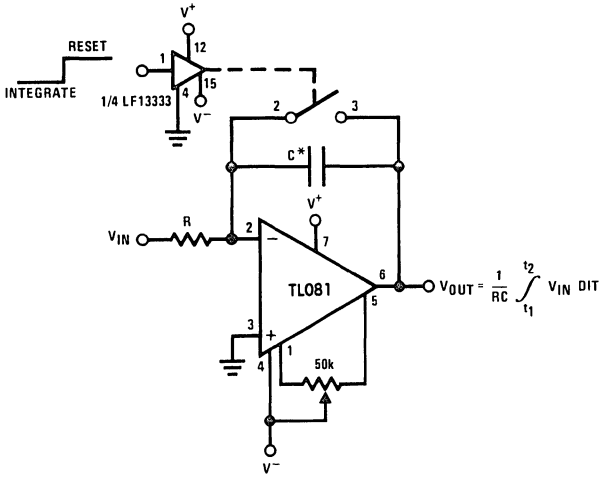
• $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$

• $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V-|$

*low leakage capacitor

Long Time Integrator

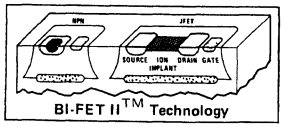


TL/H/8358–12

* Low leakage capacitor

• 50k pot used for less sensitive V_{OS} adjust

National Semiconductor



TL082CP Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

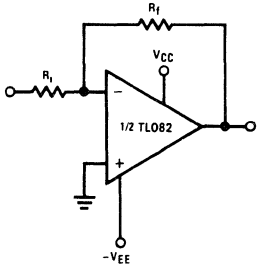
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp − p, BW = 20 Hz−20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

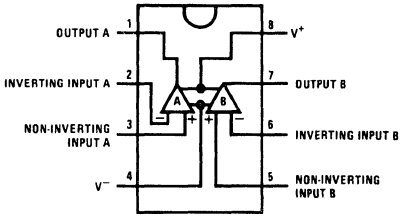
Typical Connection



TL/H/8357–1

Connection Diagram

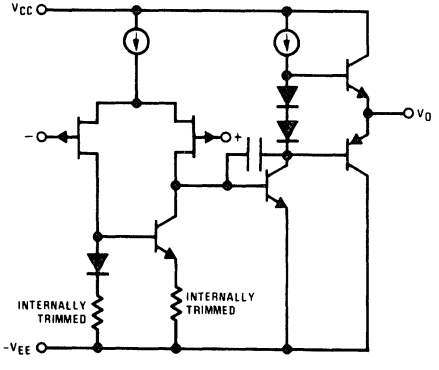
Dual-In-Line Package (Top View)



TL/H/8357–3

Order Number TL082CP
See NS Package Number N08E

Simplified Schematic



TL/H/8357–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5) $T_j \leq$ 70°C		25	200 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5) $T_j \leq$ 70°C		50	400 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1Hz- 20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	8	13		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

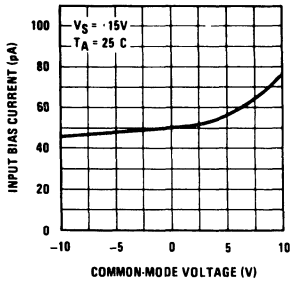
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

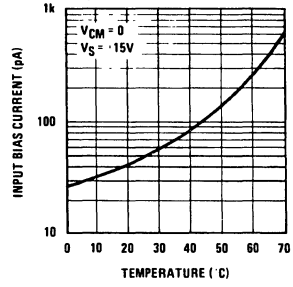
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Typical Performance Characteristics

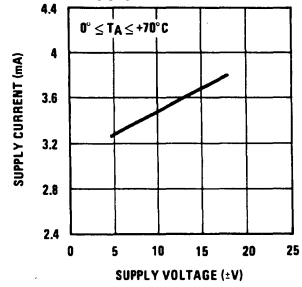
Input Bias Current



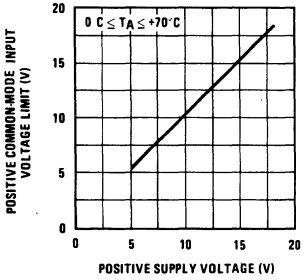
Input Bias Current



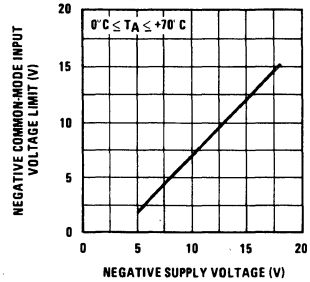
Supply Current



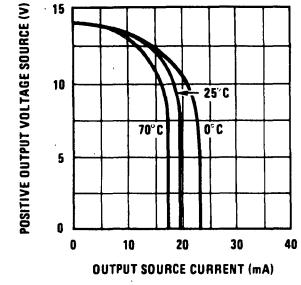
Positive Common-Mode Input Voltage Limit



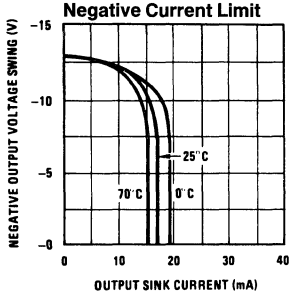
Negative Common-Mode Input Voltage Limit



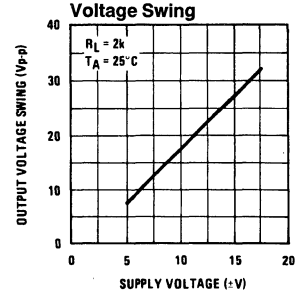
Positive Current Limit



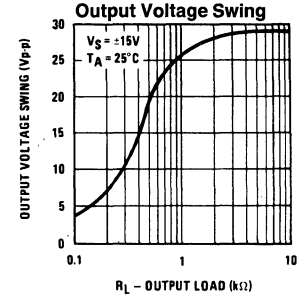
Negative Current Limit



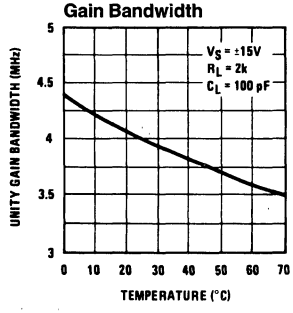
Voltage Swing



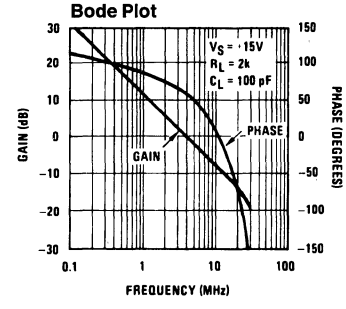
Output Voltage Swing



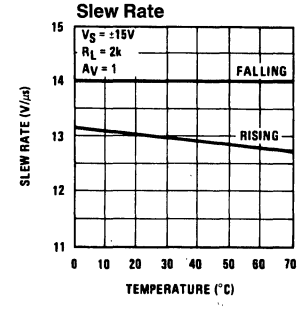
Gain Bandwidth



Bode Plot



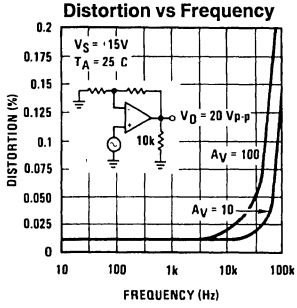
Slew Rate



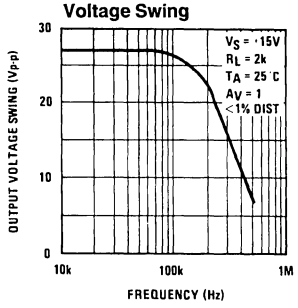
TL/H/8357–4

Typical Performance Characteristics (Continued)

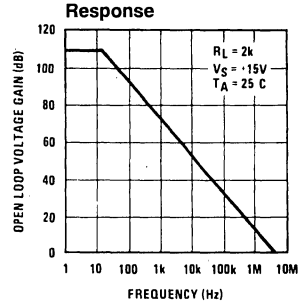
Distortion vs Frequency



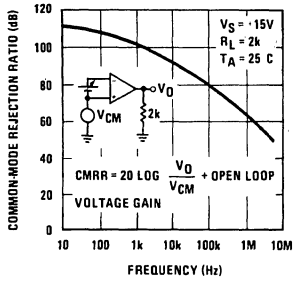
Undistorted Output Voltage Swing



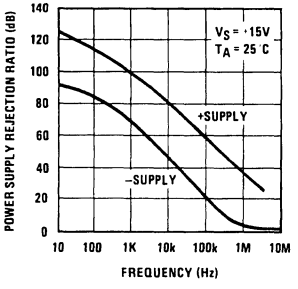
Open Loop Frequency Response



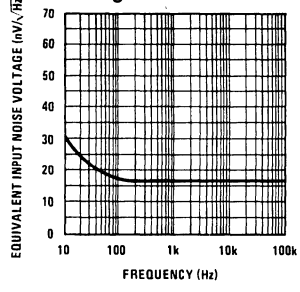
Common-Mode Rejection Ratio



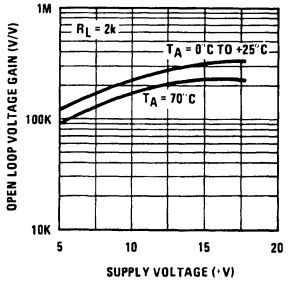
Power Supply Rejection Ratio



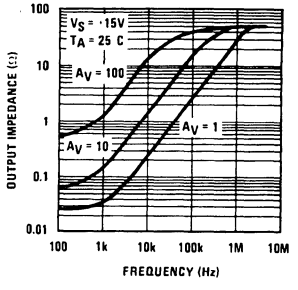
Equivalent Input Noise Voltage



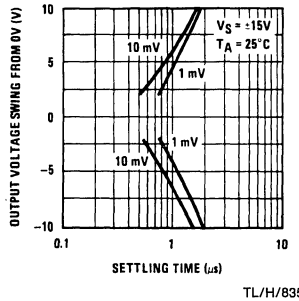
Open Loop Voltage Gain (V/V)



Output Impedance



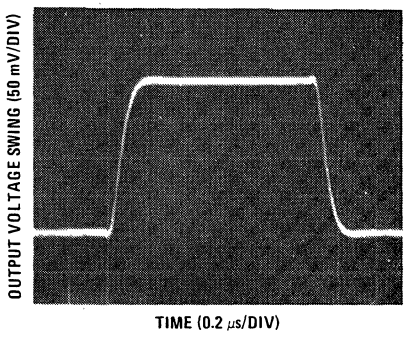
Inverter Settling Time



TL/H/8357–5

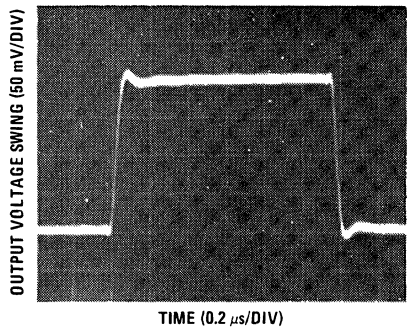
Pulse Response

Small Signal Inverting



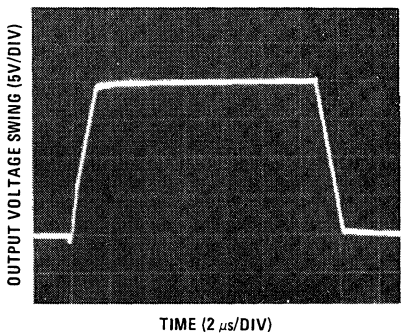
TL/H/8357–6

Small Signal Non-Inverting



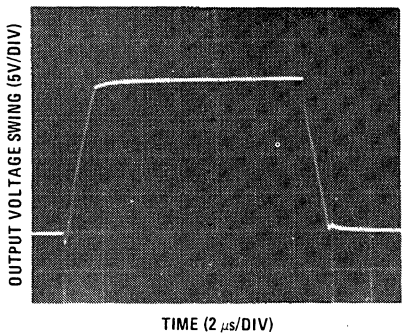
TL/H/8357–7

Large Signal Inverting



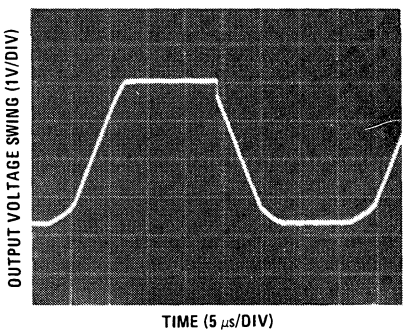
TL/H/8357–8

Large Signal Non-Inverting



TL/H/8357–9

Current Limit (R_L = 100Ω)



TL/H/8357–10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

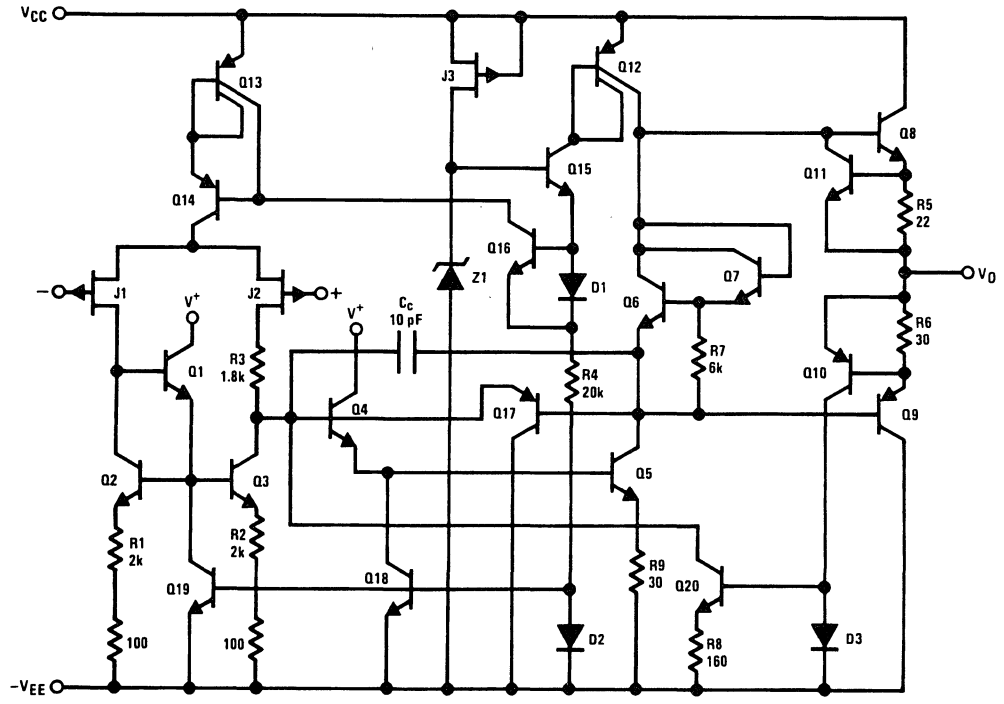
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

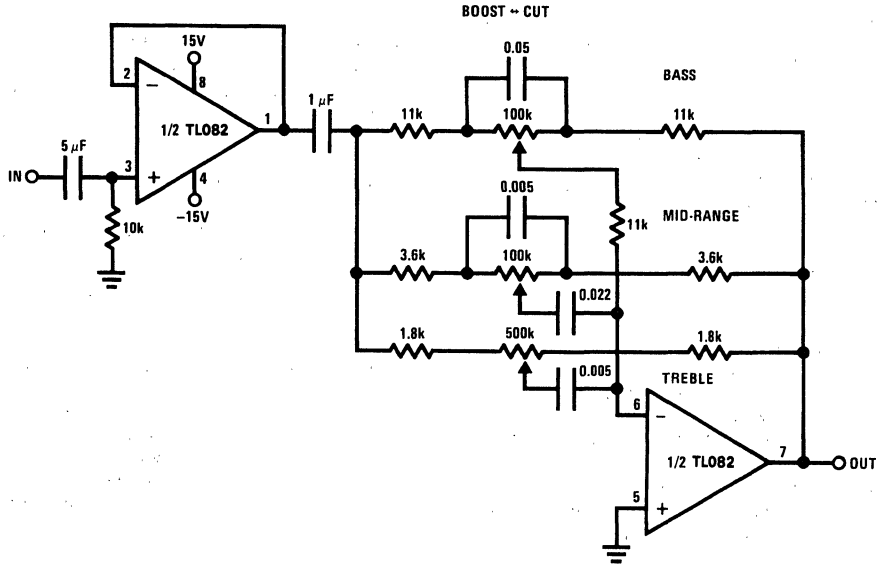
Detailed Schematic



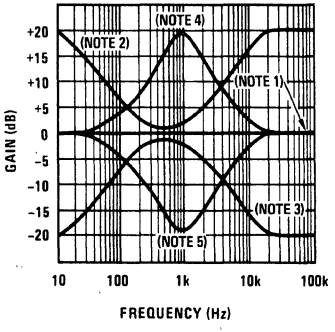
TL/H/8357–11

Typical Applications

Three-Band Active Tone Control



TL/H/8357–12



TL/H/8357–13

Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

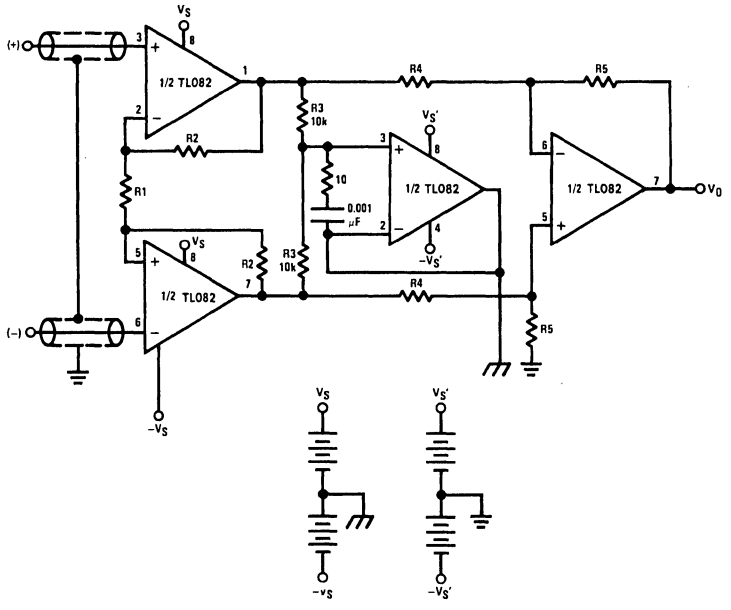
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



TL/H/8357–14

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

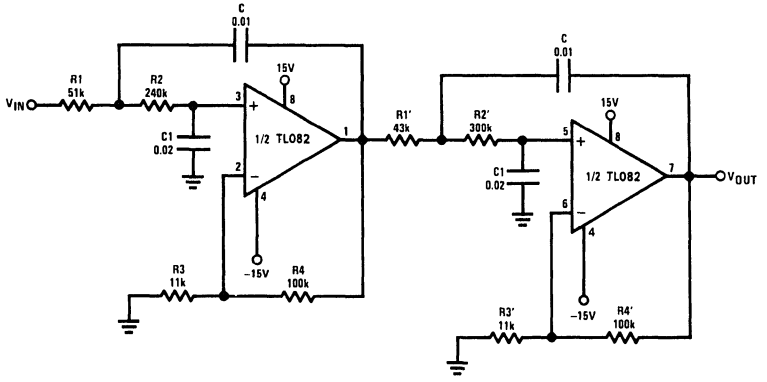
⫽ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

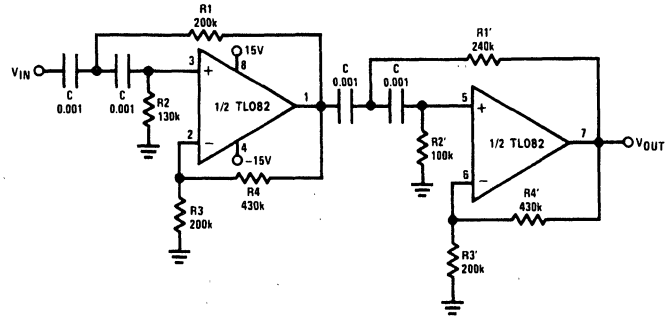


TL/H/8357–15

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Typical Applications (Continued)

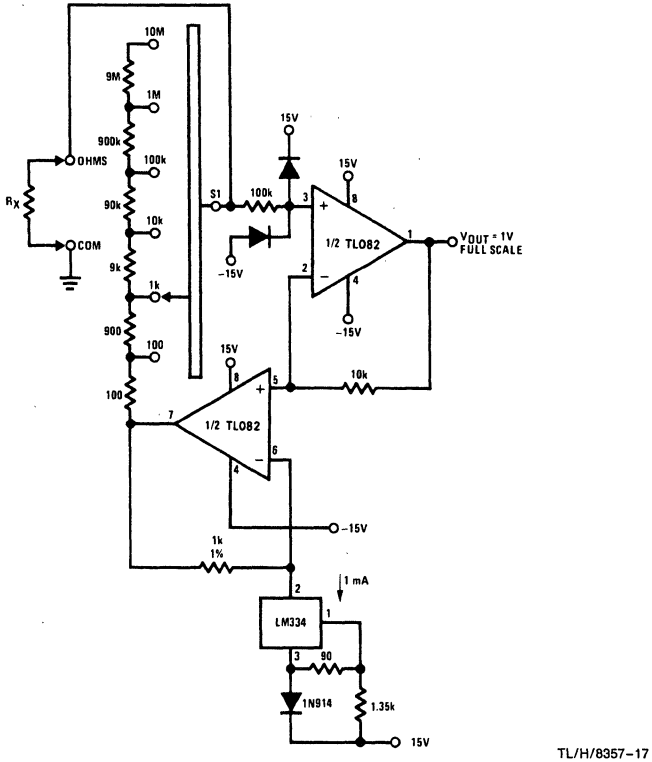
Fourth Order High Pass Butterworth Filter



TL/H/8357–16

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



TL/H/8357–17

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Section 4

Buffers

Section 4 Contents

National Semiconductor

Buffers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\%\ \text{harmonic distortion} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

Buffers Selection Guide (Notes 1 and 2)

Device Type	Key Features	Slew Rate (V/μs)	Bandwidth −3 dB (MHz)	Gain (A_V)	Output (V, mA)	Full Power BW (MHz @ V_{PP}, R_L)	Test Conditions
LH4012	Super Fast, High Current	11,500	460	0.93	±11.4, ±230	180 @ 20, 50	R_L = 50 , V_S = ±15V
LH4009	LH4008 Type with Short Circuit Protection	8000	190	0.87	±11, ±220	130 @ 20, 50	R_L = 50, V_S = ±15V
LH4008	FET Input, High Current, Ultra Fast	7000	180	0.94	±12, ±240	110 @ 20, 50	R_L = 50, V_S = ±15V
LH4011	Very Fast, High Current	5000	160	0.94	±11.4, ±230	80 @ 20, 50	R_L = 50, V_S = ±15V
LH4010	FET Input, High Speed	2500	200	0.97	±9, ±90	80 @ 10, 1k	R_L = 1k, V_S = ±15V
LH0063	FET Input, Very Fast	2400	200	0.93	±13, ±260	40 @ 20, 50	R_L = 50, V_S = ±15V
LH4063	Low Cost LH0063	2400	200	0.93	±13, ±260	40 @ 20, 50	R_L = 50, V_S = ±15V
LH0033	FET Input, High Speed	1500	100	0.98	±9, ±90	24 @ 20, 1k	R_L = 1k, V_S = ±15V
LH4033	Low Cost LH0033	1400	100	0.98	±9, ±90	20 @ 20, 1k	R_L = 1k, V_S = ±15V
LH4002	Wideband Video Buffer	1250	200	0.97	±2.2, ±44	100 @ 4, 50	R_L = 50, V_S = ±5V
LH4003	Precision Buffer	1000	250	0.98	±3, ±60	80 @ 4, 50	R_L = 50, V_S = ±6V
LH4006	Precision Buffer	1000	350	0.98	±3, ±60	80 @ 4, 50	R_L = 50, V_S = ±6V
LM6121/6125	High Speed VIP™ Buffer	800	50	0.90	±12, ±240	10.6 @ 12, 50	R_L = 50, V_S = ±15V
LH4004	Current Feedback Buffer	600	125	0.98	±4.5, ±90	40 @ 5, 50	R_L = 50, V_S = ±12V
LH0002	Medium Speed	200	30	0.97	±10, ±100	3 @ 20, 1k	R_L = 1k, V_S = ±12V
LH4001	Low Cost LH0002	125	25	0.97	±10, ±100	4 @ 10, 100	R_L = 100, V_S = ±12V
LH2110	Dual Voltage Follower	30	20	0.999	±10, ±10	0.5 @ 20, 10k	R_L = 10k, V_S = ±15V
LM110, 210, 310	Voltage Follower	30	20	0.9999	±10, ±10	0.5 @ 20, 10k	R_L = 10k, V_S = ±15V

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.

National Semiconductor

LH0002/LH0002C Current Amplifier

General Description

The LH0002/LH0002C is a general purpose current amplifier.

Features

- High input impedance 400 kΩ
- Low output impedance 6Ω
- High power efficiency
- Low harmonic distortion
- DC to 30 MHz bandwidth
- Output voltage swing that approaches supply voltage
- 400 mA pulsed output current
- Slew rate is typically 200 V/μs
- Operation from ±5V to ±20V

These features make it ideal to integrate with an operational amplifier inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

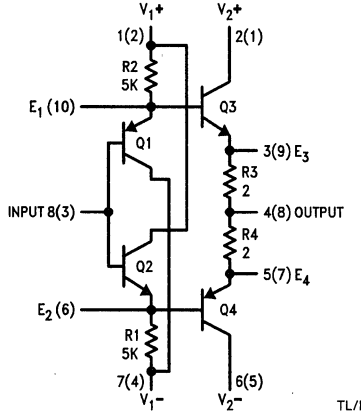
The LH0002 is available in an 8-lead low-profile TO-5 header and a 20-pin leadless chip carrier; the LH0002C is also available in an 8-lead TO-5, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

Applications

- Line driver
- 30 MHz buffer
- High speed D/A conversion
- Instrumentation buffer
- Precision current source

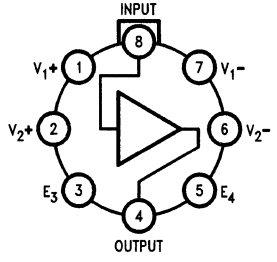
Schematic and Connection Diagrams



TL/H/5560–1

Pin numbers in parentheses denote pin connections for dual-in-line package.

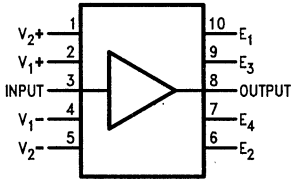
Metal Can Package



TL/H/5560–3

Order Number LH0002H or LH0002CH
See NS Package Number H08D

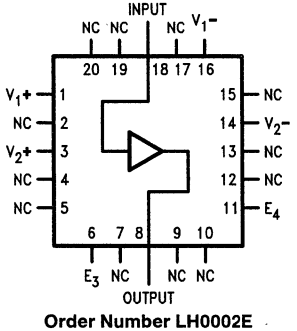
Dual-In-Line Package



TL/H/5560–2

Order Number LH0002CN
See NS Package Number N10A

Leadless Chip Carrier



TL/H/5560–6

Order Number LH0002E
See NS Package Number E20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±22V
Power Dissipation Ambient	600 mW
Input Voltage	(Equal to Power Supply Voltage)
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LH0002	−55°C to +125°C
LH0002C	0°C to +85°C
Steady State Output Current	±100 mA
Pulsed Output Current (50 ms On/1 sec. Off)	±400 mA
Lead Temperature Soldering (10 seconds)	
Metal Can	300°C
Plastic	260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

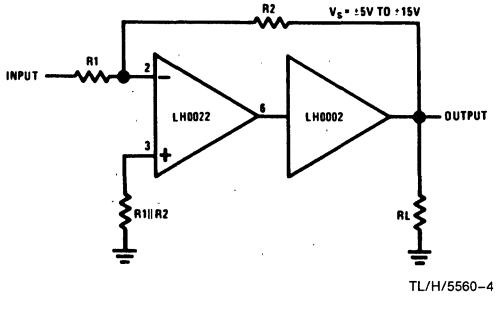
Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ, V_{IN} = ±10V	0.95	0.97		
AC Current Gain	V_{IN} = 1.0 Vrms, f = 1.0 kHz		40		A/mA
Input Impedance	R_S = 200 kΩ, V_{IN} = ±1.0V, R_L = 1.0 kΩ	180	400		kΩ
Output Impedance	V_{IN} = ±1.0V, R_L = 50Ω, R_S = 10 kΩ		6.0	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, V_{IN} = ±12V	±10	±11		V
Output Voltage Swing	V_S = ±15V, V_{IN} = ±12V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C	±10			V
DC Output Offset Voltage	R_S = 300Ω, R_L = 1.0 kΩ		±10	±30	mV
DC Input Offset Current	R_S = 10 kΩ, R_L = 1.0 kΩ		±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 Vrms, f = 1.0 kHz		0.1		%
Rise Time	R_L = 50Ω, ΔV_{IN} = 100 mV		7.0	12	ns
Positive Supply Current	R_S = 10 kΩ, R_L = 1.0 kΩ		+6.0	+10	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1.0 kΩ		−6.0	−10	mA

Note 1: Specification applies for T_A = 25°C with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to +125°C unless otherwise specified.

Note 2: Refer to RETS0002X for LH0002 military specifications.

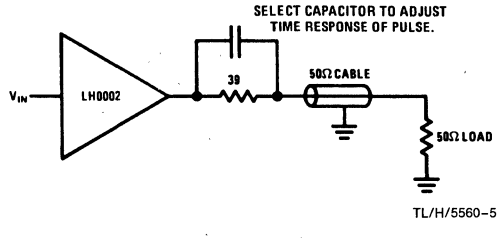
Typical Applications

High Current Operational Amplifier



TL/H/5560–4

Line Driver

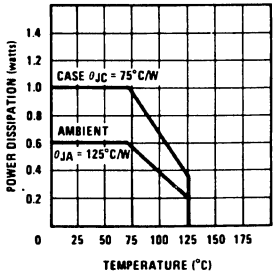


TL/H/5560–5

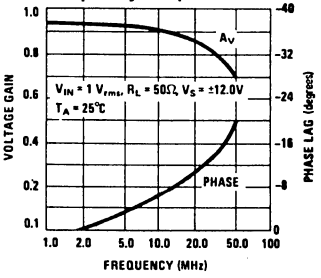
*Previously called NH0002/NH0002C

Typical Performance Characteristics

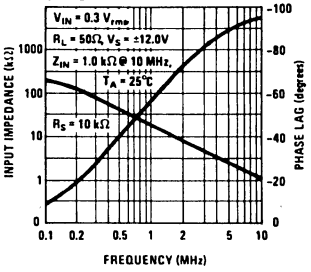
Maximum Power Dissipation



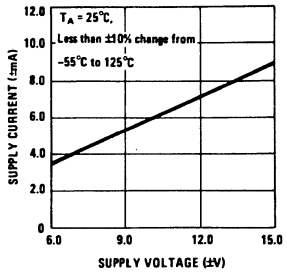
Frequency Response



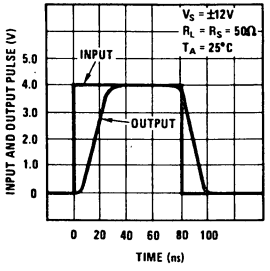
Input Impedance (Magnitude & Phase)



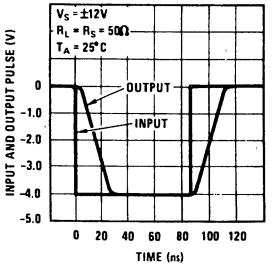
Supply Current



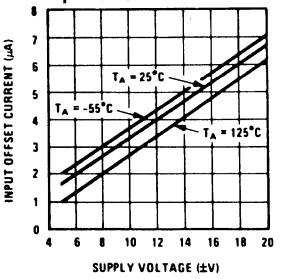
Positive Pulse



Negative Pulse



Input Offset Current



TL/H/5560–7

4

National Semiconductor

LH0033/LH0033A/LH0033C/LH0033AC/LH0063/ LH0063C Fast and Ultra Fast Buffer Amplifiers

General Description

The LH0033/LH0033A and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033A will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063 will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033/LH0033A and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C/LH0033AC and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033A is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

Features

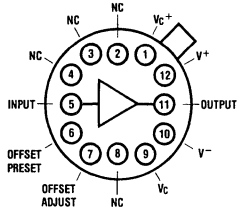
- Ultra fast (LH0063): 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ±10V with 50Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High current gain: 120 dB
- High input resistance: $10^{10}\Omega$

Advantages

- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

Connection Diagrams

LH0033G
Metal Can Package



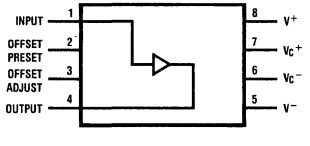
TOP VIEW

TL/K/5507–1

Case is electrically isolated

Order Number LH0033G, LH0033AG, LH0033CG, LH0033ACG, LH0063K, LH0063CK, LH0033J or LH0033CJ
See NS Package Number G12B, HY08A or K08A

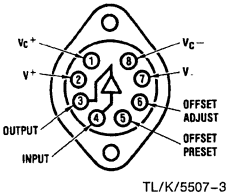
LH0033J
Dual-In-Line Package



TOP VIEW

TL/K/5507–2

LH0063K
Metal Can Package

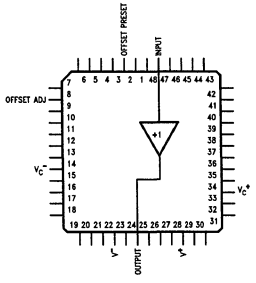


TL/K/5507–3

Top View

Case is electrically isolated

Leadless Chip Carrier



TL/K/5507–27

Order Number LH0033E
See NS Package Number E48B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Notes 5 & 7)

Supply Voltage ($V^+ - V^-$) 40V

Maximum Power Dissipation (See Curves)
- LH0063/LH0063C 5W
- LH0033A/LH0033AC/LH0033/LH0033C 1.5W

Maximum Junction Temperature 175°C

Input Voltage $\pm V_S$

Continuous Output Current
- LH0063/LH0063C ±250 mA
- LH0033A/LH0033AC/LH0033/LH0033C ±100 mA

Peak Output Current
- LH0063/LH0063C ±500 mA
- LH0033A/LH0033AC/LH0033/LH0033C ±250 mA

Operating Temperature Range
- LH0033A/LH0033 and LH0063 −55°C to +125°C
- LH0033AC/LH0033C and LH0063C −25°C to +85°C

Storage Temperature Range −65° to +150°C

Lead Temp. (Soldering, 10 seconds) 300°C

ESD rating to be determined.

DC Electrical Characteristics

$V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified, (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2)		1	5		6	15		5.0	10		12	20	mV
	$R_S = 100\Omega$			10			20			15			25	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$													
	$T_J = 25°C$ (Note 2)			100			250			250			500	pA
	$T_A = 25°C$ (Note 4)			1.5			2.5			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			7.5			10			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$	±12			±12			±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720		600	660		630	720	mW

AC Electrical Characteristics

$T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ K\Omega$ (Note 6)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		1000	1500		1000	1400		V/µs
Bandwidth	$V_{IN} = 1.0$ Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2			2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1			<0.1			<0.1		%

Note 1: LH0033 and LH0033A are 100% production tested as specified at 25° C, 125°C, and −55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033 and LH0033A are 100% production tested for this parameter. LH0033AC/C are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Note 7: Refer to RETS0033AG for the LH0033AG and RETS0033G for the LH0033G military specifications.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0063			LH0063C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S \leq 100k\Omega$, $T_J = 25°C$, $R_L = 100\Omega$ (Note 2)		10	25		10	50	mV
				100			100	mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$		300			300		$\mu V/°C$
Input Bias Current	$T_J = 25°C$ (Note 2)		10	30		10	30	nA
				100			100	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 1\ k\Omega$	0.94	0.96	1.0	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$ $T_J = 25°C$	0.92	0.93	0.98	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0			8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$		1.0	4.0		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	0.2	0.25		0.2	0.25		A
Output Voltage Swing	$R_L = 50\Omega$	± 10	± 13		± 10	± 13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.0	7.0		5.09	7.0		Vp-p
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm$ 15V (Note 3)		35	65		35	65	mA
Supply Current	$V_S = \pm 5.0V$ (Note 3)		50			50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95		1.05	1.95	W
Power Consumption	$V_S = \pm 5.0V$		500			500		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 4)

Parameter	Conditions	LH0063			LH0063C			Units
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000			6000		$V/\mu s$
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		2000	2400		$V/\mu s$
Bandwidth	$V_{IN} = 1.0$ Vrms		200			200		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.6			1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.9			2.1		ns
Harmonic Distortion			<0.1			<0.1		%

Note 1: LH0063 is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B ans I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs temperature graph for expected values.

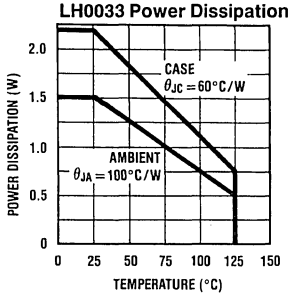
Note 3: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 4: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

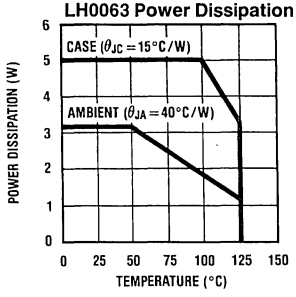
Note 5: Refer to RETS0063K for the LH0063K military specifications.

Typical Performance Characteristics

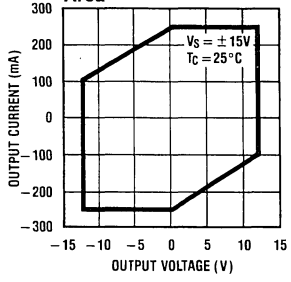
LH0033 Power Dissipation



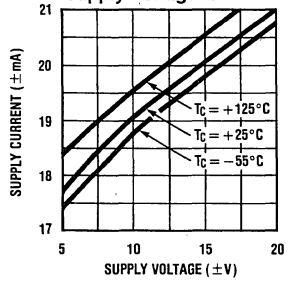
LH0063 Power Dissipation



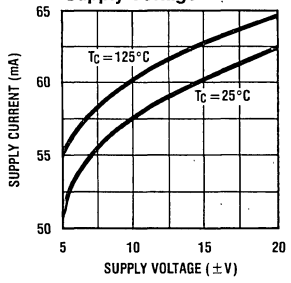
LH0063 DC Safe Operating Area



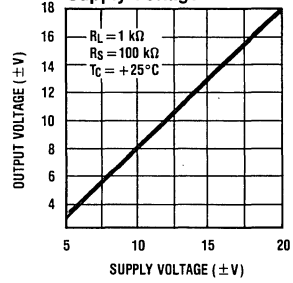
LH0033 Supply Current vs Supply Voltage



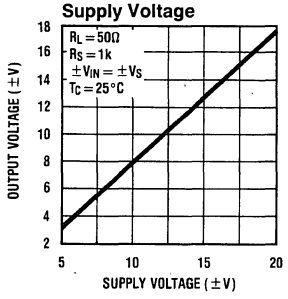
LH0063 Supply Current vs Supply Voltage



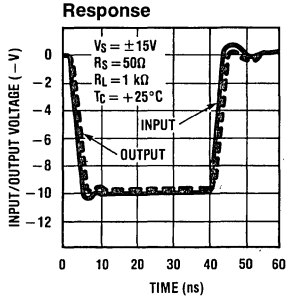
LH0033 Output Voltage vs Supply Voltage



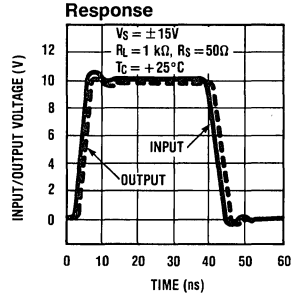
LH0063 Output Voltage vs Supply Voltage



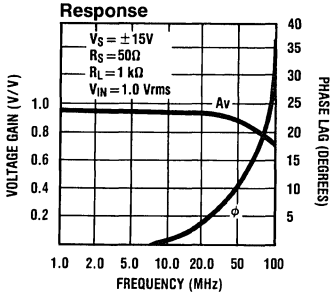
LH0033 Negative Pulse Response



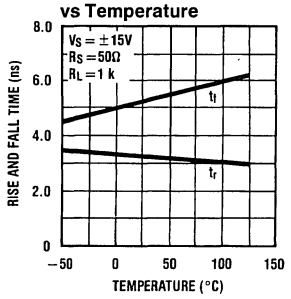
LH0033 Positive Pulse Response



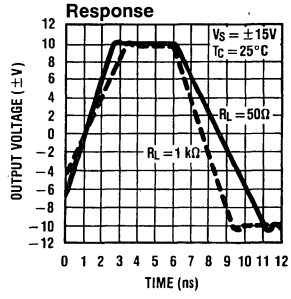
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature



LH0063 Large Signal Pulse Response



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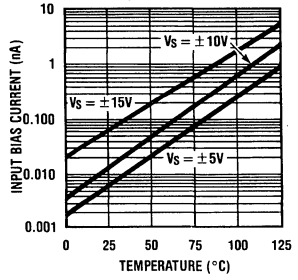
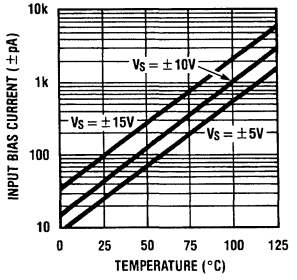
4

Typical Performance Characteristics (Continued)

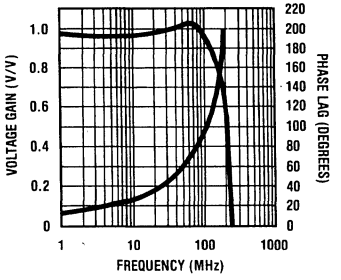
LH0033 Input Bias Current vs Temperature



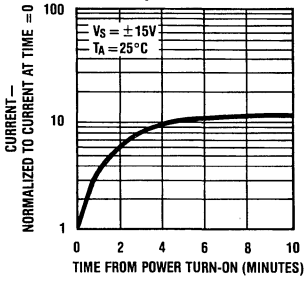
LH0063 Input Current



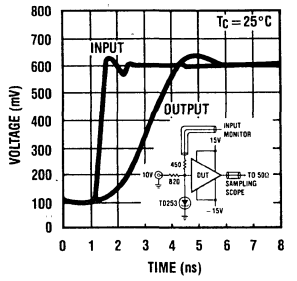
LH0063 Frequency Response



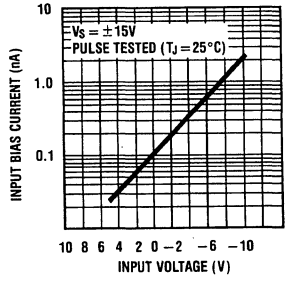
LH0033 Normalized Input Bias Current During Warm-Up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



TL/K/5507–5

Application Hints

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^-, as illustrated in *Figures 1* and *2*.

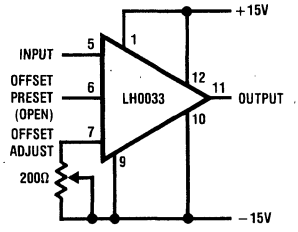


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FIGURE 1. Offset Zero Adjust for LH0033 (Pin numbers shown for TO-8)

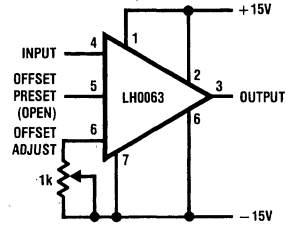

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FIGURE 2. Offset Zero Adjust for LH0063

Application Hints (Continued)

OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be $-35mV$. This may be adjusted to zero as described in *Figure 2.* For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

SHORT CIRCUIT PROTECTION

In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3 and 4.* Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where:

$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

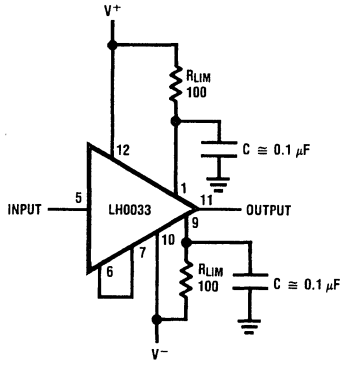

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FIGURE 3. LH0033 Using Resistor Current Limiting

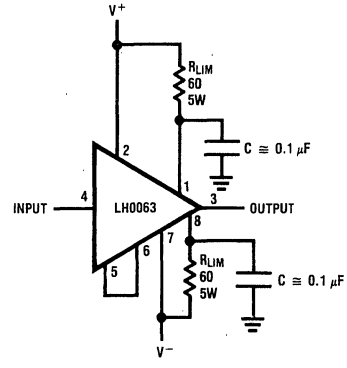

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FIGURE 4. LH0063 Using Resistor Current Limiting

Application Hints (Continued)

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5* and *6*. In *Figures 5* and *6*, the current sources are saturated during normal operation, thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

For *Figure 5:*

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\ mA} = 10\Omega$$

In *Figure 6,* quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200\ mA)} = 8.2\Omega$$

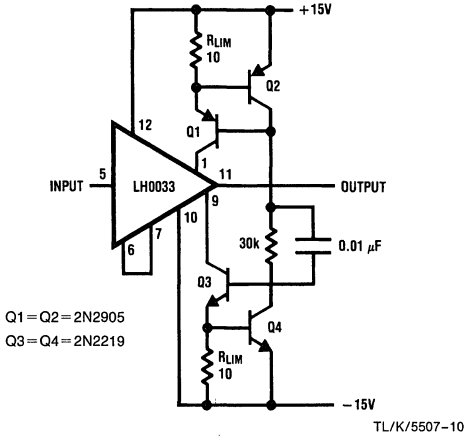

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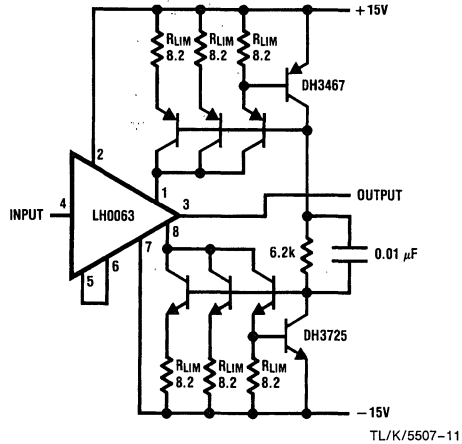
FIGURE 5. LH0033 Current Limiting Using Current Sources



TL/K/5507–11

FIGURE 6. LH0063 Current Limiting Using Current Sources

CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times dV/dt)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$P_D pkg. \geq P_{DC} + P_{AC}$

$P_D pkg. \geq (V^+ - V^-) \times I_S + P_{AC}$

$P_{AC} \cong (Vp\text{-}p)^2 \times f \times C_L$

where:

Vp-p = Peak-to-peak output voltage swing

f = Frequency

C_L = Load Capacitance

OPERATION WITHIN AN OP AMP LOOP

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE

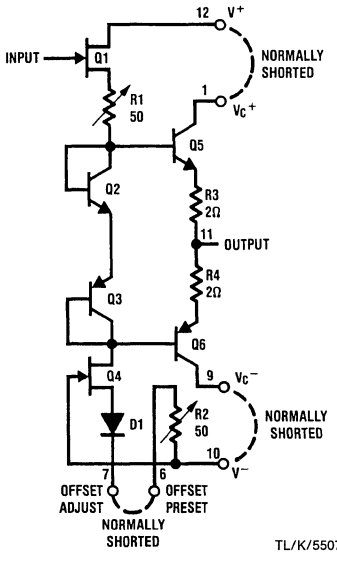
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within $<1/4$ to $1/2$" of the device package) to a ground plane. Capacitors should be one or two 0.1 µF in parallel for the LH0033; adding a 4.7 µF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1 µF ceramic and one 4.7 µF solid tantalum capacitors in parallel will be necessary on each supply lead.

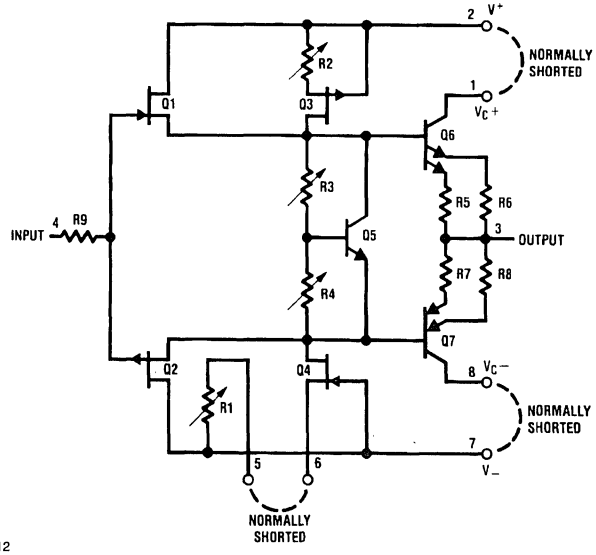
Schematic Diagrams

LH0033/LH0033A



TL/K/5507–12

LH0063

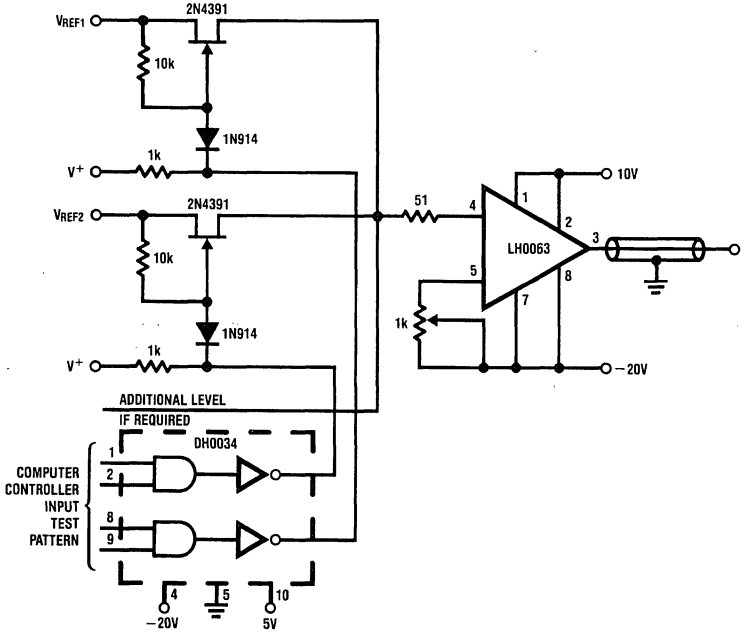


TL/K/5507–13

Pin numbers shown for TO-8 ("G") package.

Typical Applications

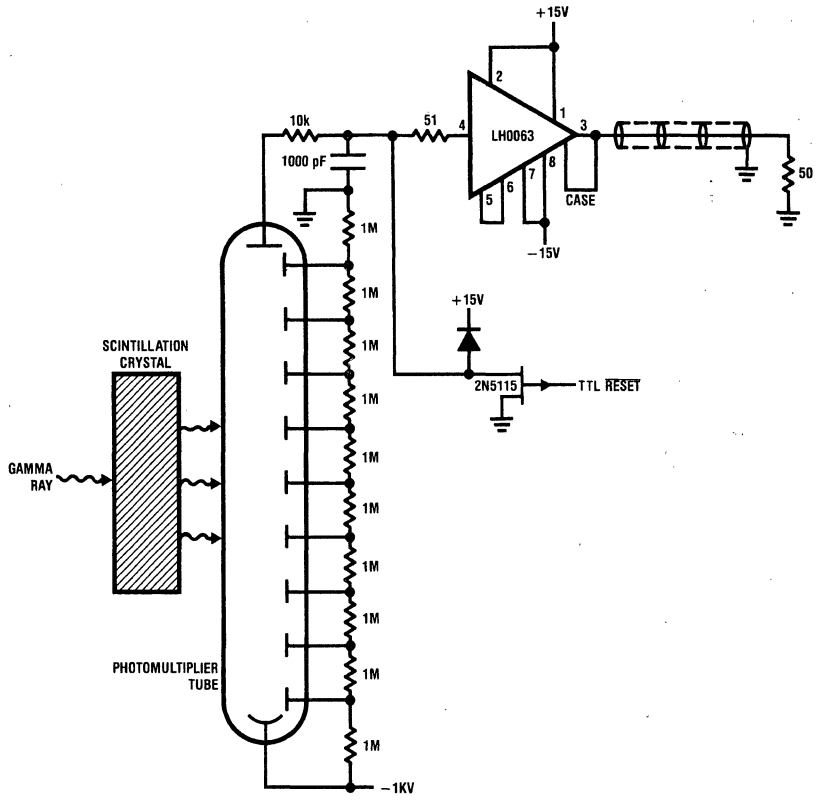
High Speed Automatic Test Equipment
Forcing Function Generator



TL/K/5507–14

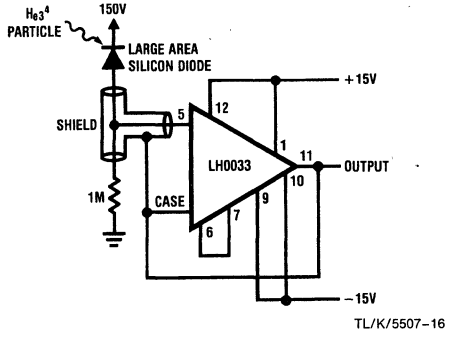
Typical Applications (Continued)

Gamma Ray Pulse Integrator



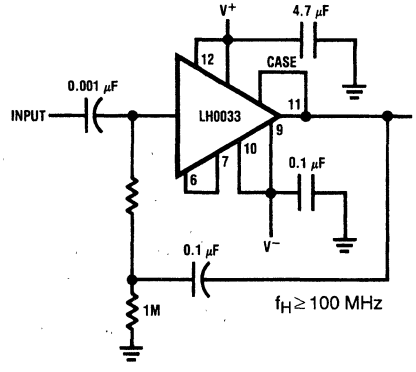
TL/K/5507–15

Nuclear Particle Detector



TL/K/5507–16

High Input Impedance AC Coupled Amplifier



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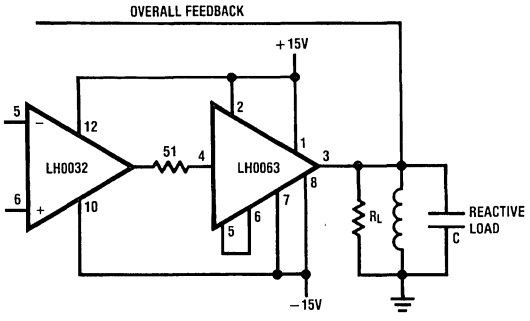
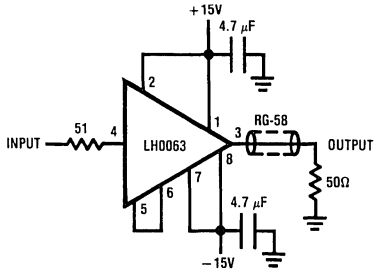
Typical Applications (Continued)

Isolation Buffer



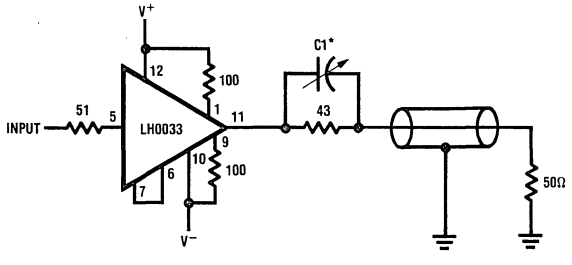
TL/K/5507–18

Coaxial Cable Driver



TL/K/5507–19

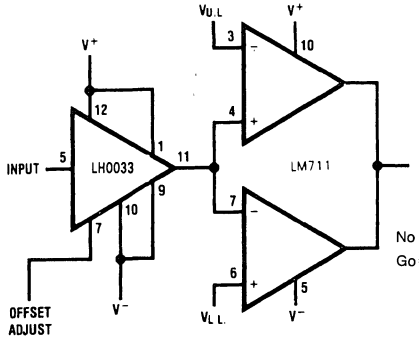
Coaxial Cable Driver



TL/K/5507–20

*Select C1 for optimum pulse response

High Input Impedance Comparator with Offset Adjust



No go = logic "1"
Go = logic "0"

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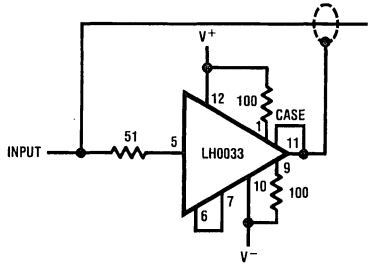
Instrumentation Shield/Line Driver

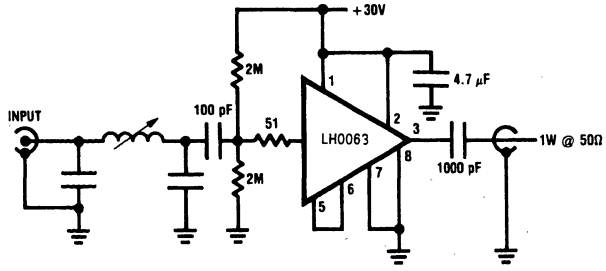


TL/K/5507–22

4

Typical Applications (Continued)

1W CW Final Amplifier



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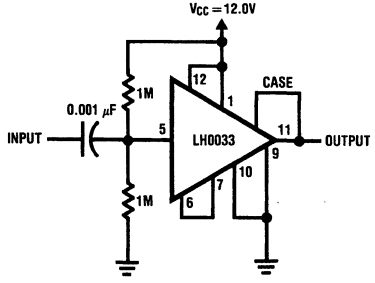
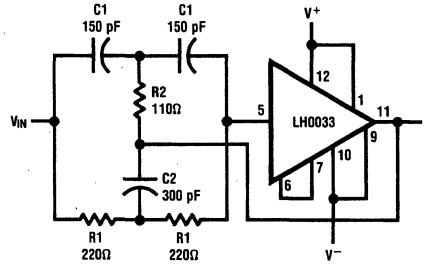
Single Supply AC Amplifier



TL/K/5507-24

4.5 MHz Notch Filter



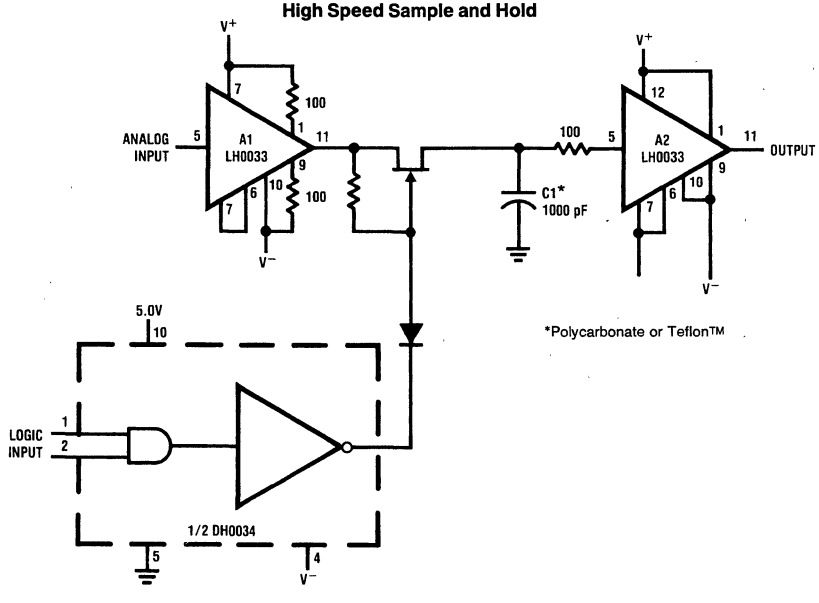
$$f_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\ R2$$

$$C1 = \frac{C2}{2}$$

TL/K/5507-25

High Speed Sample and Hold



*Polycarbonate or Teflon™

TL/K/5507-26

National Semiconductor

LH2110/LH2210/LH2310 Dual Voltage Followers

General Description

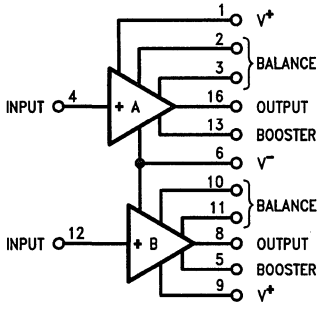
The LH2110 series of dual voltage followers are two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information, see the LM110 data sheet and National's Linear Applications Handbook.

The LH2110 is specified for operation over the −55°C to +125°C military temperature range. The LH2210 is specified for operation over the −25°C to +85°C temperature range. The LH2310 is specified for operation over the 0°C to +70°C temperature range.

Features

■ Low input current	1 nA
■ High input resistance	$10^{10}\Omega$
■ High slew rate	30V/μs
■ Wide bandwidth	20 MHz
■ Wide operating supply range	±5V to ±18V
■ Output short circuit proof	

Connection Diagram

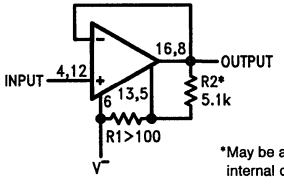


TL/K/10119–1

Order Number LH2110D, LH2210D or LH2310D
See NS Package Number D16C

Auxiliary Circuits

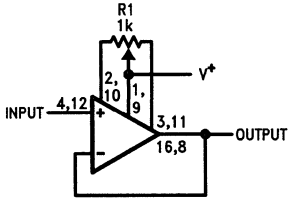
Increasing Negative Swing Under Load



*May be added to reduce internal dissipation.

TL/K/10119–2

Offset Balancing Circuit



TL/K/10119–3

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range LH2110	−55°C to +125°C
LH2210	−25°C to +85°C
LH2310	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics Each Side (Note 4)

Parameter	Conditions	Limits			Units
		LH2110	LH2210	LH2310	
Input Offset Voltage	$T_A = 25°C$	4.0	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10^{10}	10^{10}	10^{10}	Ω Min
Input Capacitance		1.5	1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L = 8\ k\Omega$	0.999	0.999	0.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	5.5	mA Max
Input Offset Voltage		6.0	6.0	10	mV Max
Offset Voltage	$-55°C \le T_A \le 85°C$	6	6	10	μV/°C Typ
Temperature Drift	$T_A = 125°C$	12	12		
Input Bias Current		10	10	10	nA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L = 10\ k\Omega$	0.999	0.999	0.999	μV/V Min
Output Voltage Swing (Note 5)	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±10	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	4.0		mA Max
Supply Voltage Rejection Ratio	$\pm 5V \le V_S \le \pm 18V$	70	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2210 is 100°C and that of the LH2310 is 85°C. For operating devices in the flat package at elevated temperatures, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 18V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified. With the LM210, however, all temperature specifications are limited to $-25°C \le T_A \le 85°C$, and for the LH2310, all temperature specifications are limited to $0°C \le T_A \le 70°C$.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals.

National Semiconductor

LH4001 Wideband Current Buffer

General Description

The LH4001 is a high speed unity gain buffer designed to provide high current drive capability at frequencies from DC to over 25 MHz. It is capable of providing a continuous output current of ±100 mA and a peak of ±200 mA.

The LH4001 is designed to fulfill a wide range of applications such as impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high speed line drivers. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased to ±100 mA.

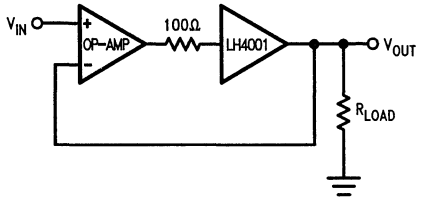
Features

- DC to 25 MHz bandwidth
- 125 V/μs slew rate
- Drives ±10V into 50Ω
- Operates from ±5 to ±20V supplies
- Output swing approaches supply voltage

Applications

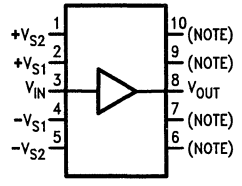
- Boost op amp output
- Buffer amplifiers
- Isolate capacitive loads
- Drive long cables

Typical Applications and Connection Diagram



TL/K/8628–1

Dual-In-Line Package



TL/K/8628–2

Top View

***Note:** Electrically connected internally. No connection should be made to these pins.

Order Number LH4001CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±22V
Continuous Output Current, I_O	±100 mA
Peak Output Current, $I_{O(peak)}$ (50 ms On/1 Sec Off)	±200 mA
Input Voltage Range, V_{IN}	$\pm V_S$
Power Dissipation Ambient	500 mW
Storage Temperature Range, T_{STG}	−65°C to +150°C
Operating Temperature Range, T_A	0°C to +70°C
Maximum Junction Temperature, T_J	150°C
Lead Temp. (Soldering, <10 seconds)	260°C

ESD rating is to be determined.

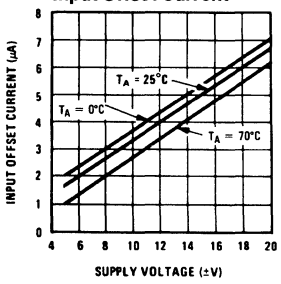
Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_V	Voltage Gain	R_S = 10 kΩ, R_L = 1 kΩ V_{IN} = ±10V	0.95	0.97	1	V/V
R_{IN}	Input Impedance	R_S = 200 kΩ, R_L = 1 kΩ V_{IN} = ±1.0V	180	400		kΩ
R_{OUT}	Output Impedance	R_S = 10 kΩ, R_L = 50Ω V_{IN} = ±1.0V		6	10	Ω
V_O	Output Swing	V_S = ±15V, R_S = 50Ω R_L = 1 kΩ, V_{IN} = ±12V	±10	±11		V
I_B	Input Bias Current	R_S = 10 kΩ, R_L = 1 kΩ		±10	±50	μA
t_r	Rise Time	R_L = 100Ω, ΔV_{IN} = 100 mV		7		ns
SR	Slew Rate	V_{IN} = ±5V, R_L = 100Ω		125		V/μs
I_S	Supply Current	R_S = 10 kΩ		±6	±10	mA
V_{OS}	DC Output Offset Voltage	R_S = 300Ω, R_L = 1 kΩ		±10	±50	mV

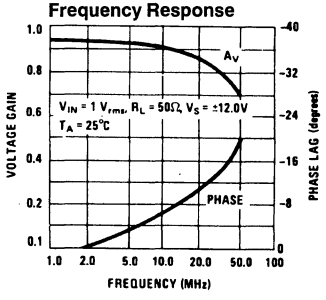
Note 1: Specification applies for T_A = 25°C with +12V on Pins 1 & 2; −12V on Pins 4 & 5 unless otherwise specified.

Typical Performance Characteristics

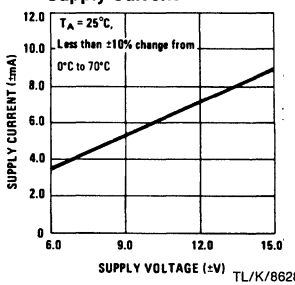
Input Offset Current



Frequency Response

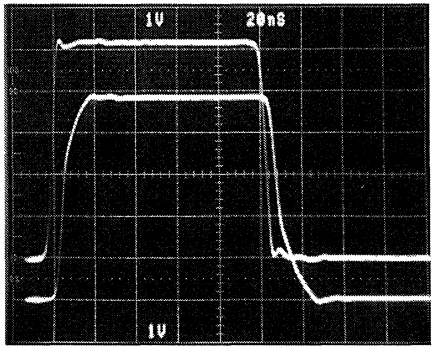


Supply Current



TL/K/8628–3

Pulse Response



TOP TRACE = INPUT

BOTTOM TRACE = OUTPUT

TL/K/8628–10

V_{IN} = ±2.5V, R_S = R_L = 50Ω

Applications Information

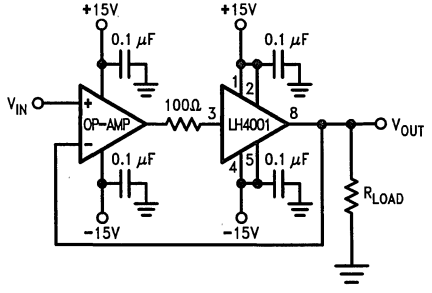
Figure 1 shows a simple implementation of a non-inverting buffer amplifier of unity gain. Popular industry standard operational amplifiers such as LF156, LF351, LF411, LF441, LM11, LM741, etc. can be used in this configuration. Due to the high bandwidth of the LH4001, it is suitable for use with most monolithic op amps.

Figure 2 shows an implementation of an inverting amplifier with output current capability in excess of ±100 mA. The gain of this amplifier is determined by the values of R_F and R_{IN}. The resistor between the non-inverting input and ground is used to minimize the output offset voltage resulting from the input bias current.

Because of its high current drive capability, the LH4001 buffer amplifier is suitable for driving terminated or unterminated co-axial cables, and high current or reactive loads.

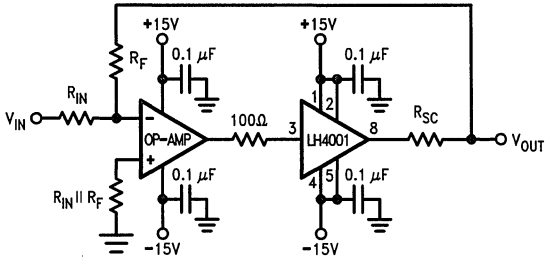
Figure 3 shows a co-axial cable drive circuit. The 43Ω resistor matches the driving source to the cable, however, its inclusion rarely will result in substantial improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

Figure 4 shows a non-inverting amplifier with gain and output current capability in excess of ±100 mA. It is capable of providing ±10 mA into a 1 kΩ load or ±100 mA into a 100Ω load (±10V swing). *Figures 5* and *6* show two different methods of providing current limit or short circuit protection for the LH4001. In *Figure 6,* the 10Ω resistor limits the output current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to occur.



TL/K/8628–4

FIGURE 1. Non-Inverting Buffer Amplifier

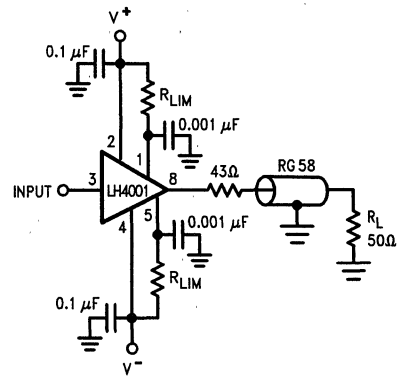


$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$$

TL/K/8628–6

FIGURE 2. Inverting Buffer Amplifier with Current Limit

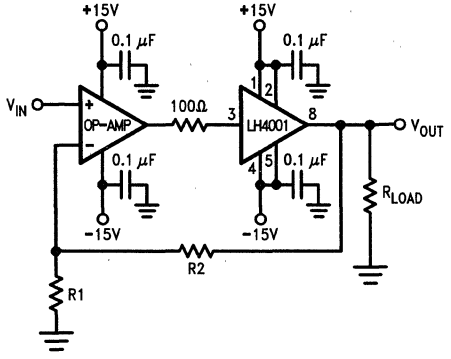
Applications Information (Continued)



$R_{LIM} = 100\Omega$, 1W

TL/K/8628–7

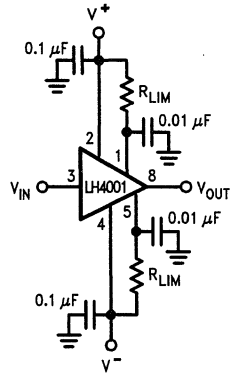
FIGURE 3. Coaxial Cable Drive Circuit



TL/K/8628–5

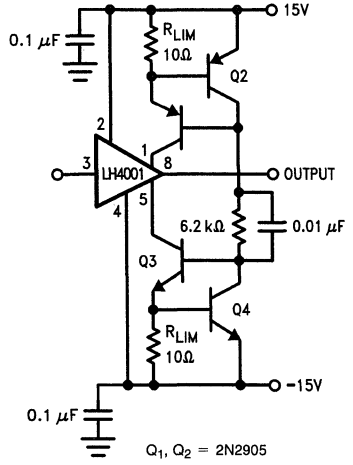
$$V_{OUT} = V_{IN}\left(1 + \frac{R2}{R1}\right)$$

FIGURE 4. Non-Inverting Buffer Amplifier with Gain



TL/K/8628–8

FIGURE 5. LH4001 Using Resistor Current Limiting



Q_1, Q_2 = 2N2905
Q_3, Q_4 = 2N2219

TL/K/8628–9

FIGURE 6. Current Limit Using Current Sources

National Semiconductor

LH4002 Wideband Video Buffer

General Description

The LH4002 is a high speed voltage follower designed to drive video signals from DC up to 200 MHz. At voltage supplies of ±5V, the LH4002 will provide up to 40 mA into 50Ω at slew rates in excess of 1000 V/μs.

The device is intended to fulfill a wide range of high speed applications including video distribution, impedance transformation, and load isolation. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased.

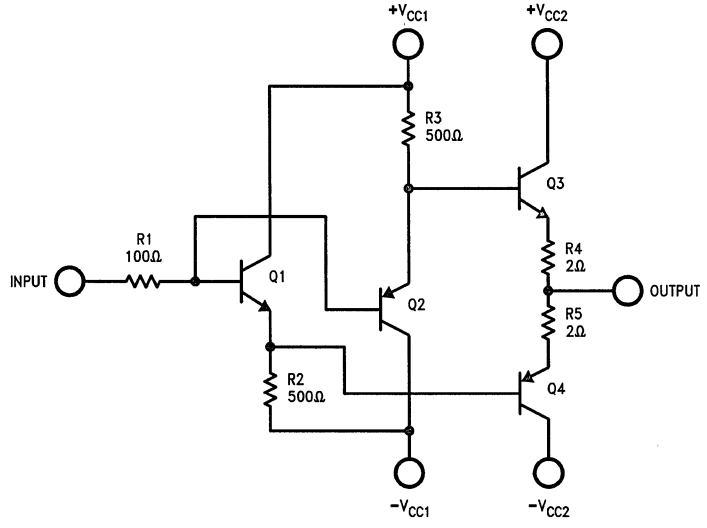
Features

- DC to 200 MHz Bandwidth with V_S = ±5V
- 1250 V/μs Slew Rate into 50Ω
- 150 MHz Bandwidth with V_S = ±5V, R_L = 50Ω and Voltage Swing = 2 V_{P-P}

Applications

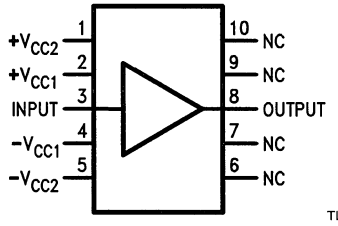
- Wideband Buffer Amplifiers
- Wideband Line Driver

Schematic and Connection Diagrams



TL/K/8686-15

Dual-In-Line Package

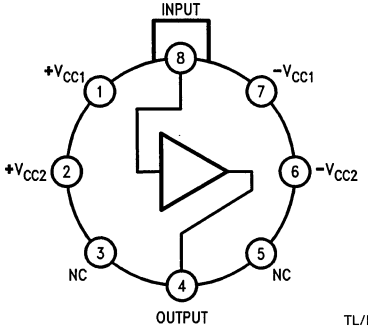


TL/K/8686-2

Top View

Order Number LH4002CN
See NS Package Number N10A

Metal Can Package



TL/K/8686-3

Top View

Order Number LH4002CH or LH4002H
See NS Package Number H08D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±6V
Input Voltage Range, V_{IN}	±V_S
Continuous Output Current, I_O	±60 mA
Storage Temperature Range, T_{STG}	−65°C to +150°C
Operating Temperature Range, T_A	
LH4002	−55°C to +125°C
LH4002C	−25°C to +85°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering, 10 sec)	300°C

ESD rating is to be determined.

DC Electrical Characteristics V_{CC} = ±5V, $T_{min} \le T_A \le T_{max}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$T_A = T_J = 25°C$ $R_S = 150\Omega, R_L = 50\Omega$			20	50	mV
I_B	Input Bias Current	$R_S = 1\ k\Omega, R_L = 50\Omega$			100	200	μA
A_V	DC Voltage Gain	$R_S = 10\ k\Omega, R_L = 1.0\ k\Omega, V_{IN} = \pm 2V$		0.95	0.97		V/V
V_O	Output Voltage Swing	$R_S = 150\Omega, V_{IN} = \pm 2.5V$	$R_L = 1\ k\Omega$	±2.2	±2.4		V
			$T_A = 25°C, R_L = 50\Omega$	±2.0	±2.2		V
I_S	Supply Current	$R_S = 10\ k\Omega, V_{IN} = 0V, R_L = 1\ k\Omega, T_A = T_J = 25°C$			20	35	mA
R_{OUT}	Output Resistance	$R_S = 10\ k\Omega, R_L = 50\Omega$			6	10	Ω
R_{IN}	Input Resistance	$R_S = 10\ k\Omega, R_L = 50\Omega$		10	18		kΩ

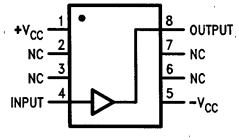
AC Electrical Characteristics V_{CC} = ±5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$R_L = 50\Omega, R_S = 50\Omega$ $V_{IN} = \pm 2V$		1000	1250		V/μs
f_{3dB}	Bandwidth, −3 dB	$R_S = 50\Omega$ $R_L = 50\Omega$	$V_{OUT} = 4V_{P-P}$		125		MHz
			$V_{OUT} = 2V_{P-P}$	100	150		MHz
		(Note 2)	$V_{OUT} = 100\ mV_{P-P}$		200		MHz
	Phase Non-Linearity	BW = 1.0–20 MHz			2.0		degrees
t_r	Rise Time	$\Delta V_{IN} = 0.5V$			3		ns
t_d	Propagation Delay	$\Delta V_{IN} = 0.5V$			1.2		ns
THD	Harmonic Distortion	f = 1 kHz			0.1		%

Note 1: Under normal operating conditions $+V_{CC1}$ and $+V_{CC2}$ should be connected together, and $-V_{CC1}$ and $-V_{CC2}$ should be connected together.

Note 2: Guaranteed by design. This parameter is sample tested.

Connection Diagrams (Continued)

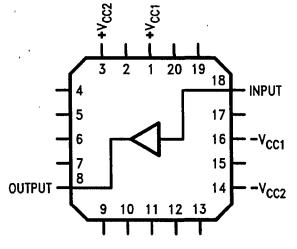


TL/K/8686-16

Top View

Order Number LH4002CN-8
See NS Package Number N08E

Note: $+V_{CC1}$ and $+V_{CC2}$ pins and $-V_{CC1}$ and $-V_{CC2}$ pins are internally connected.



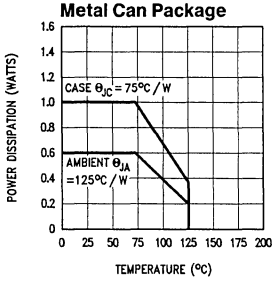
TL/K/8686-17

Top View

Order Number LH4002E
See NS Package Number E20A

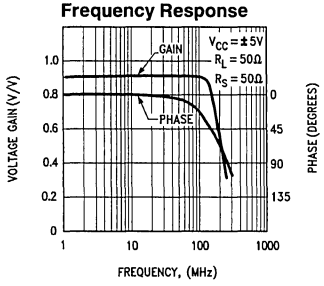
Typical Performance Characteristics

Maximum Power Dissipation Metal Can Package



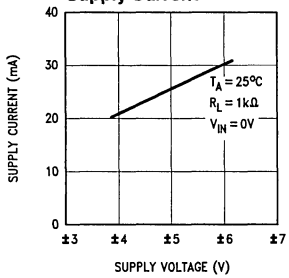
TL/K/8686-4

Frequency Response



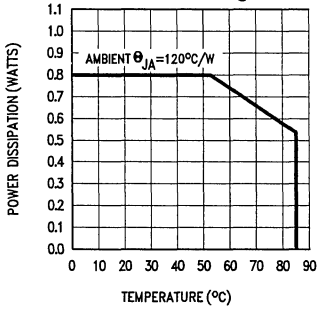
TL/K/8686-5

Supply Current



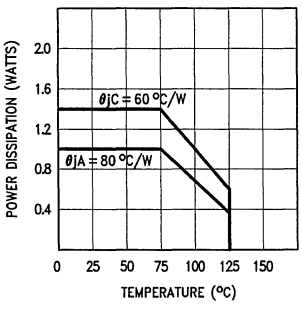
TL/K/8686-6

Maximum Power Dissipation Dual-In-Line Package



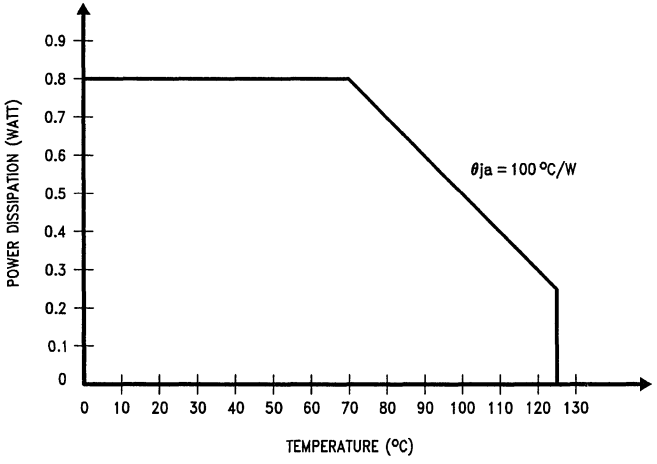
TL/K/8686-12

Maximum Power Dissipation E20A Package



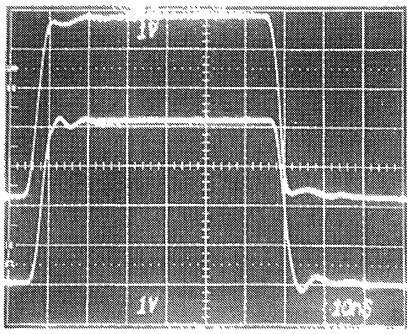
TL/K/8686-18

Maximum Power Dissipation For N08E Package



TL/K/8686-19

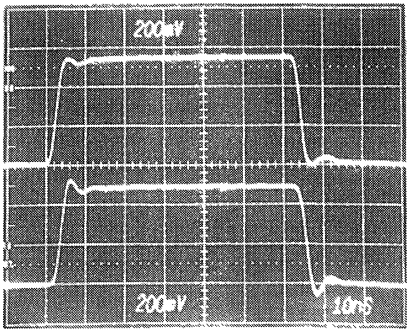
Pulse Response



TOP TRACE
= INPUT

BOTTOM TRACE
= OUTPUT

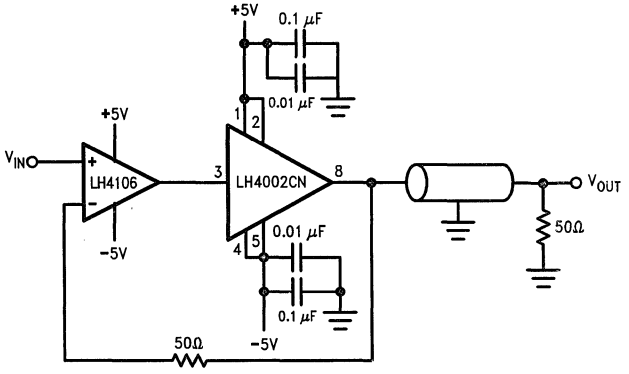
$V_S = \pm 5V$
$R_L = 50\Omega$



TL/K/8686–7

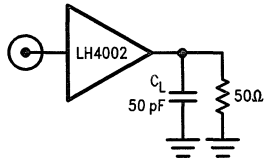
TL/K/8686–8

Typical Applications



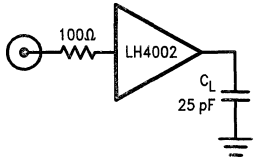
TL/K/8686–11

FIGURE 1. Wideband Unity Gain Amplifier Using LH4002CN



TL/K/8686–9

FIGURE 2. Compensation for Capacitive Loads



TL/K/8686–10

FIGURE 3. Compensation for Capacitive Loads

Applications Information

The high speed performance of the LH4002 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.01 μF in parallel with 0.1 μF should be connected with the shortest practical lead length between device supply leads and a ground plane. Failure to follow these rules can result in oscillations. When driving a capacitive load such as inputs to flash converters, the circuits in *Figure 2* and *3* can be used to minimize the amount of overshoot and ringing at the outputs. *Figure 2* indicates that a 50Ω should be placed in parallel with the load and *Figure 3* recommends that a 100Ω resistor be placed in series with the input to the LH4002.

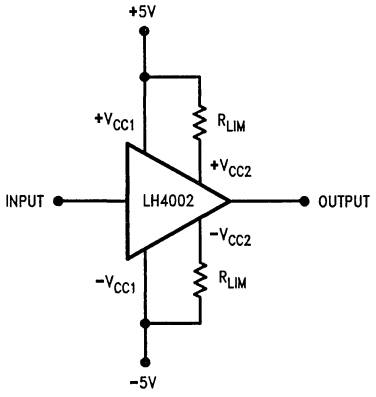
Short Circuit Protection

In order to optimize transient response and output swing, output current limits have been omitted from the LH4002. Short circuit protection may be added by inserting appropriate value resistors between $+V_{CC1}$ and $+V_{CC2}$ pins and between $-V_{CC1}$ and $-V_{CC2}$ pins as illustrated in *Figure 4*. Resistor values may be predicted by:

$$R_{LIM} = \frac{+V_{CC1}}{I_{SC}} = \frac{-V_{CC1}}{I_{SC}}$$

where $I_{SC} \leq 100$ mA. The inclusion of 50Ω limiting resistors in the collectors of the output transistors limits the short circuit current to approximately 100 mA without reducing the output voltage swing.

Short Circuit Protection (Continued)



TL/K/8686-20

FIGURE 4. LH4002 Using Resistor Current Limiting

National Semiconductor

PRELIMINARY

LH4003/LH4003C Precision RF Closed Loop Buffer

General Description

The LH4003 is a precision RF buffer optimized for unity gain applications. The LH4003 features a small signal bandwidth of 250 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4003 is useful in applications such as video buffering, cable driving, and flash converter input conditioning.

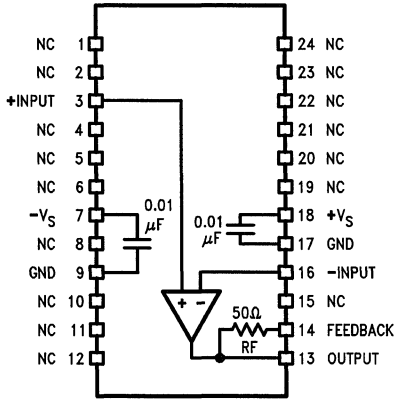
Features

- Operation from ±6V supplies
- Drive 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.97 gain accuracy into 50Ω

Applications

- Line drivers
- Video buffers

Block and Connection Diagram



Note 1: NC = No Connection

Note 2: Pins 9 & 17 Internally Connected

TL/K/9243-1

Top View

Order Number LH4003D, LH4003CD
See NS Package Number D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, Vs	±8V
Power Dissipation, P_D	
T_A = 25°C, derate linearly at 62.5°C/W	2W
T_C = 25°C, derate linearly at 33.3°C/W	3.75W
Input Common Mode Voltage Range, V_{CM}	±Vs
Output Current, I_O	±100 mA
Output Short Circuit Duration	Continuous
Operating Temperature Range, T_A	
LH4003CD	−25°C to +85°C
LH4003D	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted. (Notes 1, 6)

Symbol	Parameter	Conditions		LH4003C			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset Voltage	T_A = T_J = 25°C (Note 4)		5	15		mV
$V_{OS/\Delta T}$	Offset Voltage Drift			100			µV/°C
I_B	Input Bias Current	R_S = 300Ω, T_A = T_J = 25°C (Note 4)		100	200		µA
A_V	Voltage Gain	V_{IN} = 2 V_{PP}, f = 1 kHz	R_L = 50Ω	0.98	0.95		V/V(Min)
			R_L = 1 kΩ	0.98	0.95		
V_O	Output Voltage Swing				±3		$V_{(Min)}$
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±8V		55	45		$dB_{(Min)}$
I_S	Supply Current	R_L = 1 kΩ (Note 7)		55	65		mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions		LH4003C			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time	ΔV_{IN} = 0.5V		2			ns
t_s	Settling Time to 0.1%	V_{IN} = ±3V		80			
SR	Slew Rate	V_{IN} = −3V to +3V	10%–90%	1000		800	V/µs (Min)
		V_{IN} = +3V to −3V	10%–90%	1200		1000	
$f_{-3\,dB}$	Small Signal Bandwidth	V_{OUT} = 100 mVp-p		250	200		MHz (Min)
	Full Power Bandwidth	V_{IN} = ±2V, (Note 5)		65			MHz
	Harmonic Distortion	Second Order, V_{OUT} = 4V p-p, f_{IN} = 10 MHz		−60			dB

DC Electrical Characteristics $V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Notes 1, 6)

Symbol	Parameter	Conditions		LH4003			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset Voltage	$T_A = T_J = 25°C$ (Note 4)		2	15		mV
					20		
$V_{OS/\Delta T}$	Offset Voltage Drift			100			μV/°C
I_B	Input Bias Current	$R_S = 300\Omega$	$T_A = T_J = 25°C$, (Note 4)	100	200		μA
					200		
A_V	Voltage Gain	$V_{IN} = 2\ V_{PP}$, $f = 1$ kHz	$R_L = 50\Omega$	0.98	0.95	**0.93**	$V/V_{(Min)}$
			$R_L = 1\ k\Omega$	0.98	0.95		
					0.93		
V_O	Output Voltage Swing	$A_V = +1$			±3	**±3**	V (Min)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 8V$		55	45		dB (Min)
					40		
I_S	Supply Current	$R_L = 1\ k\Omega$ (Note 7)		55	65	**80**	mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics $V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted. (Note 1)

Symbol	Parameter	Conditions		LH4003			Units (Max Unless Otherwise Stated)
				Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$		2			ns
t_s	Settling Time to 0.1%	$V_{IN} = \pm 3V$		80			ns
SR	Slew Rate	$V_{IN} = -3V$ to $+3V$	10%–90%	1000		800	$V/\mu s$ (Min)
		$V_{IN} = +3V$ to $-3V$	10%–90%	1200		1000	
$f_{-3\ dB}$	Small Signal Bandwidth	$V_{OUT} = 100$ mVp-p		250	200		MHz (Min)
	Full Power Bandwidth	$V_{IN} = \pm 2V$, (Note 5)		65			MHz
	Harmonic Distortion	Second Order, $V_{OUT} = 4V$ p-p, $f_{IN} = 10$ MHz		−60			dB

Note 1: These measurements are taken with the LH4003 strapped for a gain of +1.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$. See Typical Performance Characteristics for more information.

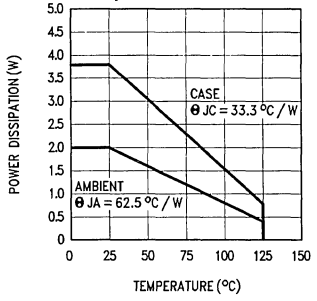
Note 5: Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate / ($2\pi V$ peak).

Note 6: Boldface limits are guaranteed over full temperature. Operating ambient temperature range of LH4003C is −25°C to +85°C, and LH4003 is −55°C to +125°C.

Note 7: When the LH4003 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S of ±6V is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

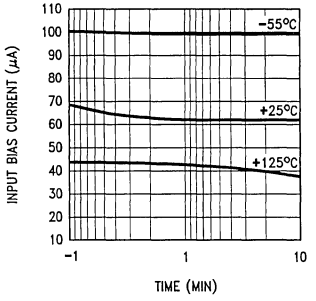
Typical Performance Characteristics

Maximum Power Dissipation



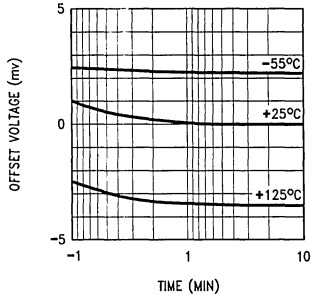
TL/K/9243-2

Input Bias Current vs Time



TL/K/9243-10

Offset Voltage (Typical) vs Time



TL/K/9243-11

Application Information

The unity gain follower configuration shown in *Figure 1,* offers a 250 MHz small signal bandwidth to the −3dB point and the minimum slew rate of 800 V/μs insures a full power bandwidth of 65 MHz for a 4V peak-to-peak signal, according to the formula:

$$B = SR/2\pi Vp$$

Where SR is the slew rate in μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.

DRIVING CAPACITIVE LOADS

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4003 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time of 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).

LAYOUT CONSIDERATIONS

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz required special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4003 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 μF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5.*

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.

INPUT CAPACITANCE

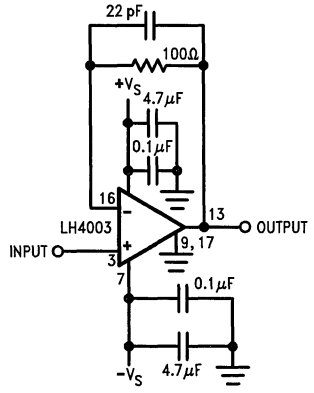
The input capacitance of the LH4003 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500 ohms should not be utilized in the feedback network and high source impedance should be avoided.

BIAS CURRENT

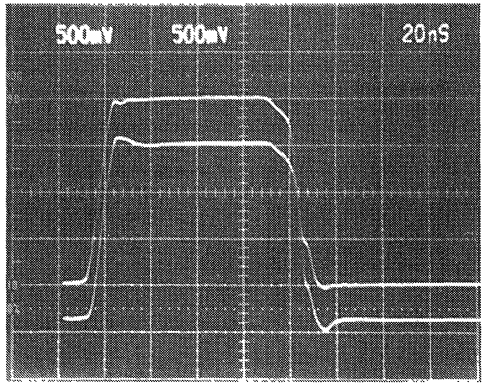
The input bias current is typically 100 μA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.

Typical Applications



TL/K/9243-3

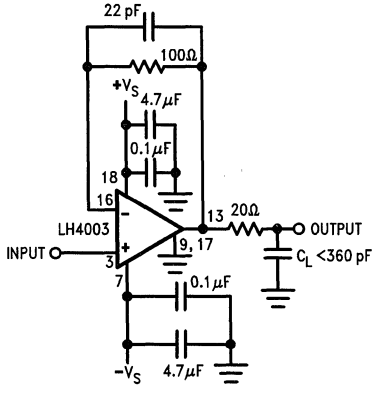
FIGURE 1. Unity Gain Follow, Typical BW 3dB = 250 MHz



TL/K/9243-4

Note: Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = R_L = 50\Omega$.

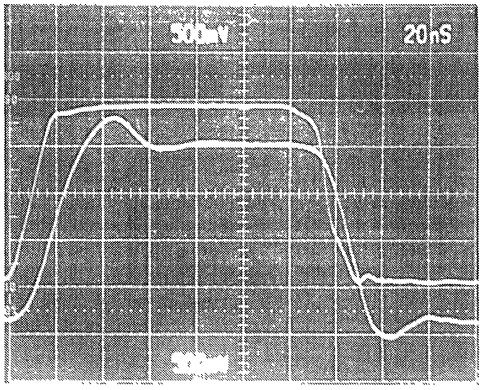
FIGURE 2. Pulse Response of Follower



TL/K/9243-6

FIGURE 3. Driving Capacitance

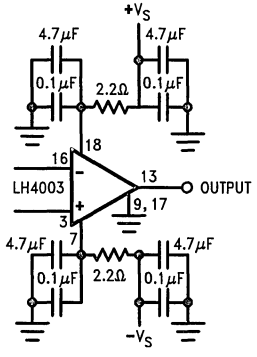
Typical Applications (Continued)



TL/K/9243–7

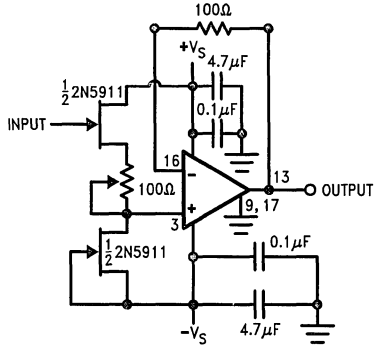
Note: Top trace is input and bottom trace is output. $V_{CC} = \pm 6V$, $R_S = 50\Omega$, $R_{ISO} = 20\Omega$ and $C_L = 300$ pF.

FIGURE 4. Pulse Response when Driving Capacitance.



TL/K/9243–8

FIGURE 5. Dual Stage Decoupling



TL/K/9243–9

FIGURE 6. FET Buffer Reduces Bias Current

National Semiconductor

PRELIMINARY

LH4004/LH4004C Wideband FET-Input Buffer/Amplifier

General Description

The LH4004 is an FET input, high speed differential amplifier optimized for unity gain applications. It eliminates most of the drawbacks of conventional open loop buffers and does not require compensation for unity and other low gain operations. It is an ideal choice for video distribution, driving flash converters, and summing amplifiers. Furthermore, the bandwidth does not decrease with increasing gain. At a closed loop gain of 4, the LH4004 still offers a 75 MHz bandwidth.

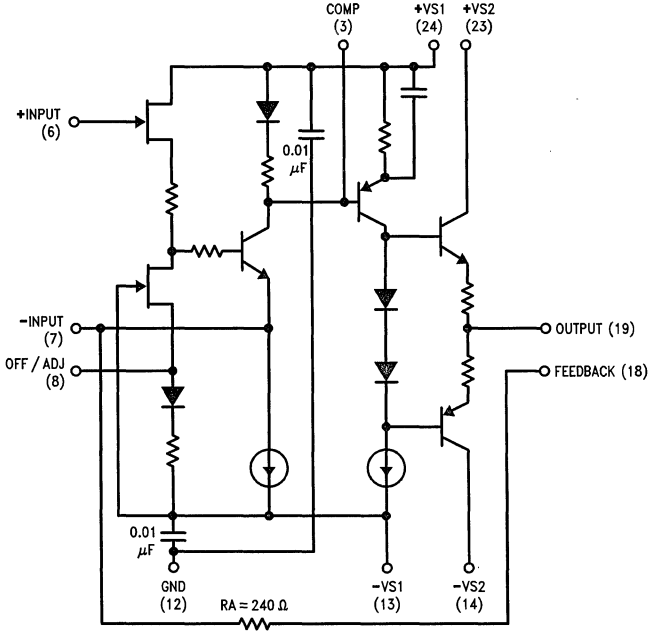
Features

- ±0.5 dB gain flatness
- 500 V/μs slew rate
- Drives 50Ω directly
- 140 MHz bandwidth
- No external components required for unity gain operation
- Internal power supply bypassing

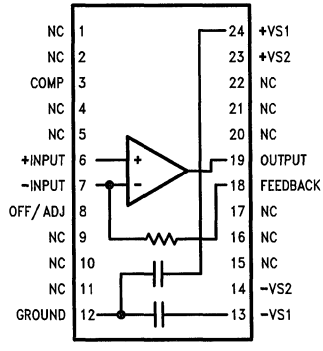
Applications

- Unity gain buffer
- Low gain op amp

Simplified Schematic and Connection Diagram



TL/K/8831-1



TL/K/8831-2

Top View

Order Number
LH4004CD or LH4004D
See NS Package Number D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S ±15V

Power Dissipation, P_D
T_A = 25°C, derate linearly at 80°C/W 1.8W
T_C = 25°C, derate linearly at 40°C/W 3.75W

Input Voltage Range, V_{IN} ±V_S

Operating Temperature Range, T_A
LH4004CD −25°C to +85°C
LH4004D −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_J 150°C

Lead Temperature (Soldering, <10 sec) 300°C

ESD rating is to be determined.

DC Electrical Characteristics V_S = ±12V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted (Note 1)

Symbol	Parameter	Conditions		LH4004C Typ	LH4004C Tested Limit (Note 2)	LH4004C Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_{OS}	Input Offset Voltage	V_{IN} = 0V, T_A = T_J = 25°C (Note 4)		8	15		mV
$V_{OS}/\Delta T$	Offset Voltage Drift			300			µV/°C
I_B	Input Bias Current	T_J = 25°C, Pin 6 (Note 4)			400		pA
	Gain Accuracy	V_{IN} = ± 1V, A_V = +1	R_L = 500Ω	0.98	0.96	**0.93**	V/V (Min)
			R_L = 50Ω	0.98	0.96	**0.93**	
V_O	Output Voltage Swing	V_{IN} = ±10V	R_L = 500Ω	9.6	9.2	9.2	V (Min)
V_O	Output Voltage Current Swing	V_{IN} = ±5V, R_L = 50Ω		±4.5	±4		V (Min)
I_S	Supply Current			35	40		mA
PSRR	Power Supply Rejection Ratio	± V_S = ±11V to ±15V			40		dB (Min)

AC Electrical Characteristics V_S = ±12V, R_S = R_L = 50Ω, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions		LH4004C Typ	LH4004C Tested Limit (Note 2)	LH4004C Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
t_r	Small Signal Rise Time	ΔV_{IN} = 0.5V		3			ns
t_s	Settling Time to 0.5%	V_{IN} = −2.5V to +2.5V		30			ns
f_{-3dB}	Small Signal Bandwidth	V_{IN} = −10 dBm	A_V = +1	140	125		MHz (Min)
			A_V = +4	85	75		
	Large Signal Bandwidth	V_{OUT} = ±2.5V	A_V = +1		70		MHz
	Gain Flatness	V_{IN} = −10 dBm, A_V = +1, f = 0–50 MHz			±0.5		dB
	Harmonic Distortion	Second Order, V_{IN} = 4Vp-p, f_{IN} = 10 MHz					dB
SR	Slew Rate	V_{IN} = −2.5V to +2.5V		1500		1200	V/µs (Min)
		V_{IN} = +2.5V to −2.5V		600		500	

DC Electrical Characteristics

$V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted (Notes 1 & 5)

Symbol	Parameter	Conditions		LH4004 Typ	LH4004 Tested Limit (Note 2)	LH4004 Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
V_{OS}	Input Offset Voltage	$T_A = T_J = 25°C$ (Note 4)		8	15		mV
$V_{OS}/\Delta T$	Offset Voltage Drift			300			μV/°C
I_B	Input Bias Current	$T_A = T_J = 25°C$, Pin 6 (Note 4)			400		pA
					400		nA
	Gain Accuracy	$V_{IN} = \pm 1V$, $A_V = +1$	$R_L = 500\Omega$	0.98	0.96		V/V (Min)
					0.93		
			$R_L = 50\Omega$	0.98	0.96		
					0.93		
V_O	Output Voltage Swing	$V_{IN} = \pm 10V$	$R_L = 500\Omega$	9.6	9.2		V (Min)
V_O	Output Voltage Swing	$V_{IN} = \pm 5V$, $R_L = 50\Omega$		±4.5	**±4**		V (Min)
I_S	Supply Current			35	40		
PSRR	Power Supply Rejection Ratio				**40**		dB (Min)

AC Electrical Characteristics $V_S = \pm 12V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions		LH4004 Typ	LH4004 Tested Limit (Note 2)	LH4004 Design Limit (Note 3)	Units (Max Unless Otherwise Stated)
t_r	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$		3			ns
t_s	Settling Time to 0.5%	$V_{IN} = -2.5V$ to $+2.5V$		30			ns
f_{-3dB}	Small Signal Bandwidth	$V_{IN} = -10$ dBm	$A_V = +1$		125		MHz (Min)
			$A_V = +4$		75		
	Large Signal Bandwidth	$V_{OUT} = \pm 2.5V$	$A_V = +1$		70		MHz
	Gain Flatness	$V_{IN} = 100$ mV p-p, $A_V = +1$, $f = 0$–50 MHz			±0.5		dB
	Harmonic Distortion	Second Order, $V_{IN} = 4V$ p-p, $f_{IN} = 10$ MHz					dB
SR	Slew Rate	$V_{IN} = -2.5V$ to $+2.5V$		1500		1200	V/μs (Min)
		$V_{IN} = +2.5V$ to $-2.5V$		600		500	

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4004C is −25°C to +85°C, and LH4004 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality levels.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

Note 5: When the LH4004 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S of ±12V is 960 mW, whereas the package is only rated to 800 mW without a heatsink at 125°C.

Application Hints

The front page figure shows the simplified schematic which includes the feedback resistor and the decoupling capacitors.

The essential difference from other op amps is that both inputs are radically different, the non-inverting input goes to a FET buffer follower and the inverting input is connected to the second stage emitter node. This topology is responsible for the unique bandwidth characteristic and transfer function of the amplifier.

Let's consider the connection diagram of *Figure 1.* The typical transfer function in the case of a classical op amp would be:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K(s)}{1 + K(s)/B}$$

where $B = \frac{R_A + R_B}{R_B}$ and K(s) is the open loop gain of the amplifier and is frequency dependent. By rearranging the formula, we find;

$$(1) \quad \frac{V_{OUT}}{V_{IN}} = B * \frac{K(s)}{K(s) + B}$$

For the LH4004, a small signal analysis shows that the difference between the two inputs turns the previous typical equation into:

$$(2) \quad \frac{V_{OUT}}{V_{IN}} = B * \frac{K(s)}{K(s) + B + m R_A}$$

where m is an internal parameter to the device and K(s) is approximately 70 dB at DC with a 50Ω load.

In both equations, the second term is negligible when the open loop gain of the amplifier, K(s), approaches infinity, but in equation (1), when the signal frequency reaches a point where K(s) is small, say K(s) = 10 or less, then the term will be very sensitive to the value of the closed loop gain B and V_{OUT}/V_{IN} will fall earlier as B increases.

In equation (2), m is approximately 0.19 and R_A is provided inside the package, with a value which has been chosen to be 240Ω. The term mR_A is therefore equal to 46 and will dominate the term B as long as it is kept below 5. The result is that V_{OUT}/V_{IN} will not be as dependent on B as with traditional topologies. The gain will still fall with the open loop gain K(s) as the frequency increases, but the roll off will be virtually independent of the closed loop gain B.

Resistor R_B sets the overall closed loop gain, but has very little effect on stability and bandwidth. Another peculiarity of the LH4004 is that the loop compensation can be accomplished by changing the value of resistor R_A *(Figure 2).* Even though this such as settling time, overshoot and phase margin, it will not affect the slew rate. Although this resistive compensation scheme is adequate in most cases, an alternate method is to place a capacitor between pins 3 and 19 *(Figure 3).* This method of compensation also reduces the device slew rate *(Figure 4).*

Low Gain Operation

The small amount of stray capacitance present at the inverting input can cause peaking which increases with decreasing gain. The gain set resistor R_B (in *Figure 1*) is effectively in parallel with this capacitance and so a frequency domain pole results. With a small R_B, this pole is at a high frequency and it affects the closed loop gain of the LH4004 only slightly. At lower values of gain, this pole becomes significant. For example, at a gain of +2, the gain may peak as much as 1.5 dB to 2 dB at 100 MHz.

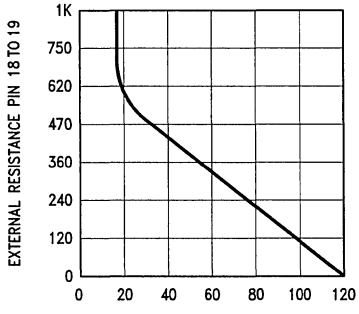


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FIGURE 2. Bandwidth vs R_{ext}

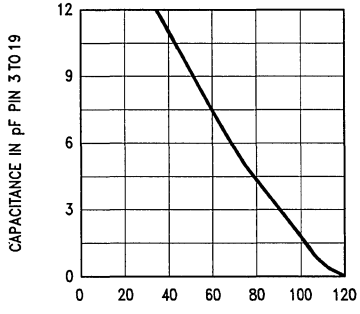

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FIGURE 3. Bandwidth vs C_{ext}

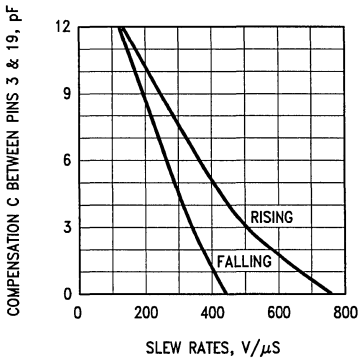

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FIGURE 4. Slew Rates vs Compensation C

Typical Applications

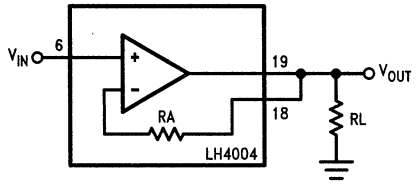

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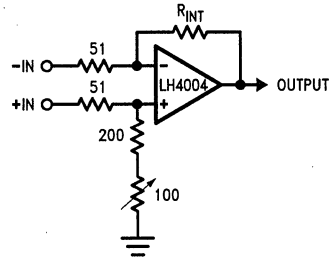
FIGURE 5. Unity Gain Buffer



Note: Adjust pot for best CMRR.

TL/K/8831–12

FIGURE 6. Differential Amplifier

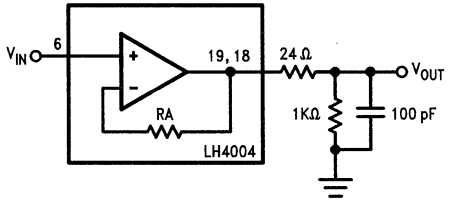


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FIGURE 7. Driving Capacitive Loads

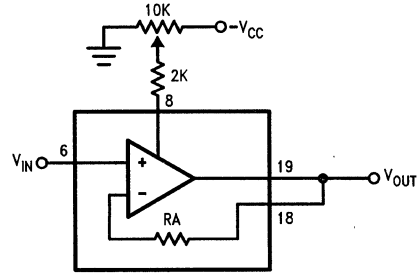

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FIGURE 8. Offset Adjust

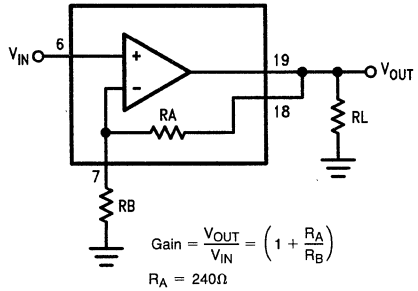

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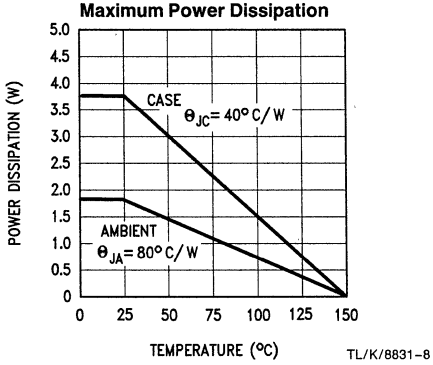
FIGURE 9. LH4004 Used in Amplifier Applications

Typical Performance Characteristics



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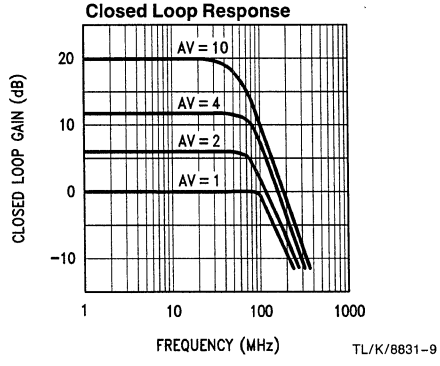

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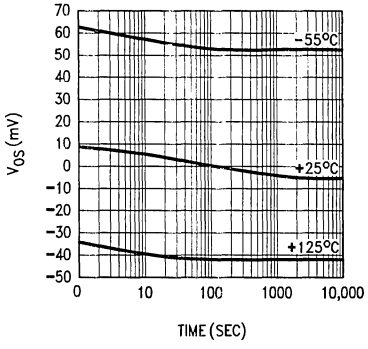
Typical Performance Characteristics (Continued)

Input Offset Voltage vs Time



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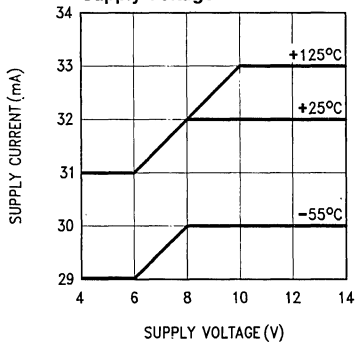
Supply Current vs Supply Voltage



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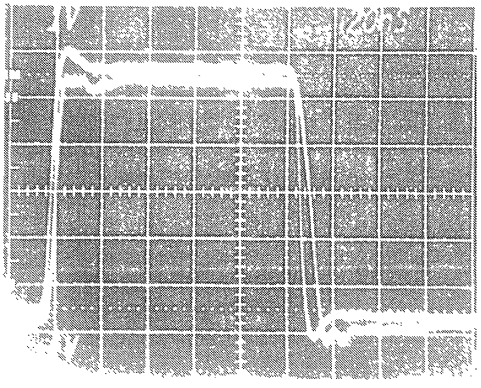
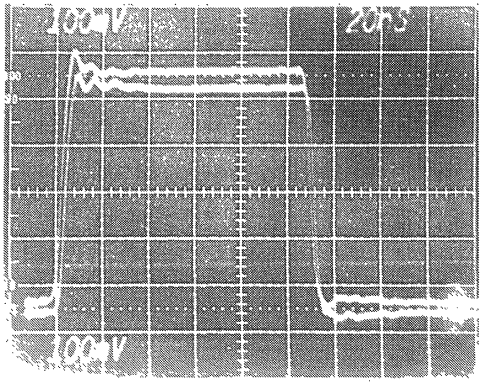
Large Signal Pulse Response



TL/K/8831–16

Top Trace = Input
Bottom Trace = Output

Small Signal Pulse Response



TL/K/8831–17

Top Trace = Input
Bottom Trace = Output

National Semiconductor

PRELIMINARY

LH4006/LH4006C Precision RF Closed Loop Buffer

General Description

The LH4006 is a precision RF buffer optimized for unity gain applications. It features a small signal bandwidth of 350 MHz. The buffer is internally compensated to be unity gain stable and has internal short circuit protection. The LH4006 is useful in applications such as video buffering, cable driving, and flash converter input conditioning. The high bandwidth also allows the LH4006 to be used in RF/IF signal conditioning such as amplification or down conversion.

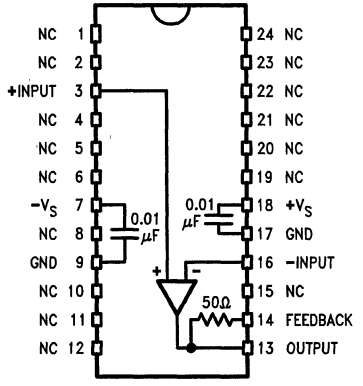
Features

- Operation from ±6V supplies
- Drives 50Ω directly
- Internal power supply bypassing
- Short circuit protection
- 1000 V/μs slew rate
- 0.95 gain accuracy into 50Ω

Applications

- Line drivers
- Video buffers
- Pulse amplifiers

Connection Diagram



TL/K/9255–1

Top View

Note 1: NC = not connected.

Note 2: Pins 9 & 17 are internally connected.

Order Number LH4006D & LH4006CD
See NS Package Number D24D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S ±8V

Power Dissipation, P_D
- T_C = 25°C, Derate Linearly at 33.3°C/W 3.75W
- T_A = 25°C, Derate Linearly at 62.5°C/W 2W

Input Common Mode Voltage Range, V_{CM} ±V_S

Output Current, I_O ±100 mA

Output Short Circuit Duration Continuous

Operating Temperature Range, T_A
- LH4006CD −25°C to +85°C
- LH4006D −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_J 150°C

Lead Temperature (Soldering < 10 sec.) 300°C

ESD Rating to be determined.

DC Electrical Characteristics (Notes 1 & 6)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006C Typ	LH4006C Tested Limit (Note 2)	LH4006C Design Limit (Note 3)	Units (Max unless otherwise stated)
V_{OS}	Output Offset Voltage	T_A = T_J = 25°C, Note 4		5	15		mV
$V_{OS/\Delta T}$	Offset Voltage Drift			100			µV/°C
I_B	Input Bias Current	R_S = 300Ω, Note 4		100	300		µA
A_V	Voltage Gain	V_{IN} = 2 Vp-p, f = 1 kHz	R_L = 50Ω	0.98	0.95		V/V (min)
			R_L = 1 kΩ	0.98	0.95		
V_O	Output Voltage Swing	A_V = +1			±3		V (min)
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±8V, R_L = 1 kΩ		55	45		dB (min)
I_S	Supply Current	V_{IN} = 0V, R_L = 1 kΩ, Note 7		55	65		mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics (Note 1)

V_S = ±6V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		LH4006C Typ	LH4006C Tested Limit (Note 2)	LH4006C Design Limit (Note 3)	Units (Max unless otherwise stated)
tr	Small Signal Rise Time	ΔV_{IN} = 0.5V		2			ns
ts	Settling Time to 0.1%	V_{IN} = ±3V		80			
SR	Slew Rate	V_{IN} = −3V to +3V	10%–90%	1000			V/µs (min)
		V_{IN} = +3V to −3V	10%–90%	1200			
$f_{-3\,dB}$	Small Signal Bandwidth	V_{OUT} = 100 mVp-p	A_V = +1	350	300		MHz (min)
	Full Power Bandwidth	V_{IN} = ±2V, Note 5		80			
	Second Order Harmonic Distortion	V_{OUT} = 4 Vp-p, f_{IN} = 10 MHz		−60			dB

4

DC Electrical Characteristics (Notes 1 & 6)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions		LH4006 Typ	LH4006 Tested Limit (Note 2)	LH4006 Design Limit (Note 3)	Units (Max unless otherwise stated)
V_{OS}	Output Offset Voltage	$T_A = T_J = 25°C$		2	15		mV
					25		
$V_{OS/\Delta T}$	Offset Voltage Drift	$V_{IN} = 0V$		100			μV/°C
I_B	Input Bias Current	$R_S = 300\Omega$ $T_A = T_J = 25°C$, Note 4		100	300		μA
					400		
A_V	Voltage Gain	$V_{IN} = 2$ Vp-p, f = 1 kHz	$R_L = 50\Omega$	0.98	0.95 **0.93**		V/V (min)
			$R_L = 1$ kΩ	0.98	0.95 **0.93**		
V_O	Output Voltage Swing	$A_V = +1$			±3	**±3**	V (min)
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $+8V$		55	45		dB (min)
					40		
I_S	Supply Current	$V_{IN} = 0V$, $R_L = 1$ kΩ (Note 7)		55	65	**80**	mA
P_D	Power Dissipation					780	mW

AC Electrical Characteristics (Note 1)

$V_S = \pm 6V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions		LH4006 Typ	LH4006 Tested Limit (Note 2)	LH4006 Design Limit (Note 3)	Units (Max unless otherwise stated)
tr	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$		2			ns
ts	Settling Time to 0.1%	$V_{IN} = \pm 3V$		80			
SR	Slew Rate	$V_{IN} = -3V$ to $+3V$	10%–90%	1000			V/μs (min)
		$V_{IN} = +3V$ to $-3V$	10%–90%	1200			
$f_{-3\,dB}$	Small Signal Bandwidth	$V_{OUT} = 100$ mVp-p	$A_V = +1$	350	300		MHz (min)
	Full Power Bandwidth	$V_{IN} = \pm 2V$, Note 5		80			
	Second Order Harmonic Distortion	$V_{OUT} = 4$ Vp-p, $f_{IN} = 10$ MHz		−60			dB

Note 1: These measurements are taken with the LH4006 strapped for a gain of +1.

Note 2: Tested limits are guaranteed and 100% tested in production.

Note 3: Design limits are guaranteed (but not 100% production tested) over indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual value may be higher at operating junction temperature.

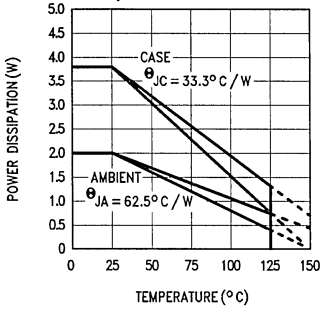
Note 5: Full power bandwidth is calculated based on slew rate measurement using FPBW = slew rate/(2 πV peak).

Note 6: Boldface limits are guaranteed over full temperature. Operating ambient temperature range of LH4006C is −25°C to +85°C, and LH4006 is −55°C to +125°C.

Note 7: When the LH4006 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S of ±6V is 780 mW, whereas the package is rated to 750 mW without a heatsink at 125°C.

Typical Performance Characteristics

Maximum Power Dissipation



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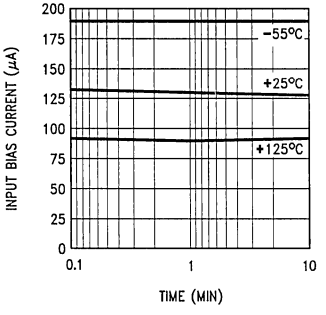
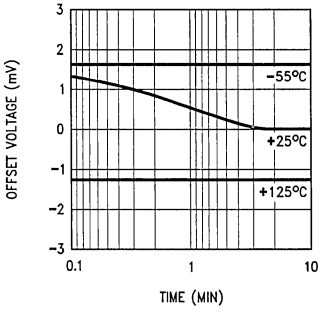
Input Bias Current vs Time



TL/K/9255–10

Offset Voltage (Typical) vs Time



TL/K/9255–11

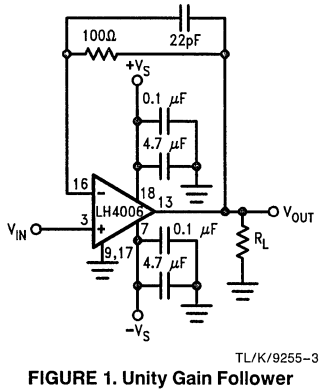
Application Information

The unity gain follower configuration shown in *Figure 1*, offers a 350 MHz small signal bandwidth to the −3 dB point and the minimum slew rate of 1000 V/μs insures a full power bandwidth of 80 MHz for a 4V peak to peak signal, according to the formula:

$$B = \frac{SR}{2\pi Vp}$$

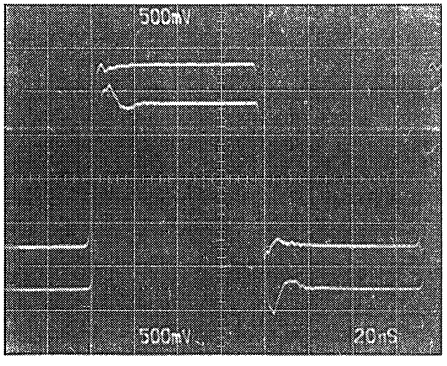
Where SR is the slew rate in V/μs, B is the bandwidth of the device in MHz for a peak sine wave voltage Vp.

The unity gain follower/buffer is therefore an excellent choice for wideband sinewave buffering or pulse amplification. *Figure 2* shows the typical pulse response for such a configuration.



TL/K/9255–3

FIGURE 1. Unity Gain Follower



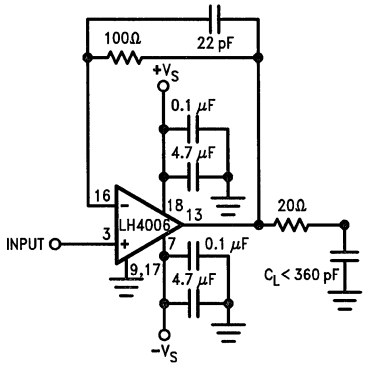
TL/K/9255–5

$V_{CC} = \pm 6V, R_S = R_L = 50\Omega$.

FIGURE 2. Follower/Buffer Pulse Response

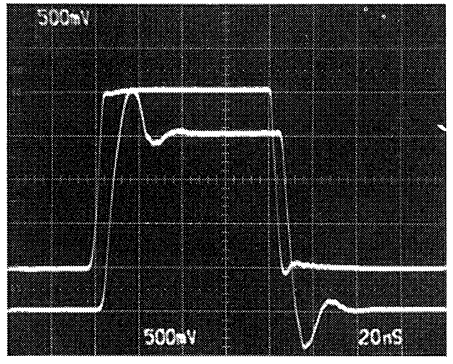
Driving Capacitive Loads

Flash A/D, unterminated cables, etc, can exhibit up to 300 pF of capacitance, thus creating stability or settling problems. *Figure 3* shows the compensation scheme for driving such capacitive loads while still insuring optimum settling. The output current limit of the LH4006 is a considerable help for driving capacitive loads, the charging current is kept in control and the damping resistor can be small without overloading the output stage. A 20Ω resistor in series with the capacitance is required for insuring an optimum settling time to 0.5% in less than 20 ns which is suitable for driving a 7 bit flash A to D converter in video applications at a sampling rate of 20 MSPS (see *Figure 4*).



TL/K/9255–6

FIGURE 3. Driving Capacitance



TOP = Input

BOTTOM = Output

TL/K/9255–7

V_{CC} = ±6 Volts

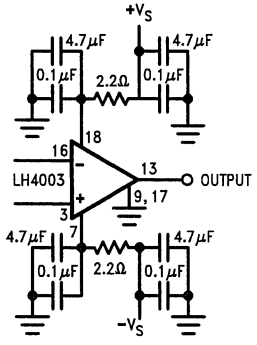
C_L = 360 pF

FIGURE 4. Pulse Response When Driving Capacitance

Layout Considerations

The layout of a RF/Video PC board where the signal frequency is beyond 100 MHz requires special attention. All the traces or connections must be as short and as wide as possible in order to keep their parasitic inductance to a minimum. This is especially critical for the supply lines where the current can reach over 100 mA in a few nanoseconds.

Although the LH4006 contains internal decoupling, it still requires some external bypassing capacitors, which have to be located as close to the supply pins as possible. A 4.7 μF in parallel with a 100 nF low inductance capacitor will insure good filtering. In some cases of noisy environment, or when the power supply is located far from the circuit, it may be necessary to use a dual stage decoupling as shown in *Figure 5.*



TL/K/9255–8

FIGURE 5. Dual Stage Decoupling

Ground can also become a considerable problem. It is assumed to be uniformly zero volts and considered as a reference. In practice, if the ground is poorly laid out, every single point may be at a different potential and at a different phase, which is a source of instability or signal distortion.

The most reliable solution to this problem is to have a ground plane that will minimize the parasitic inductance and therefore, potential and phase differences.

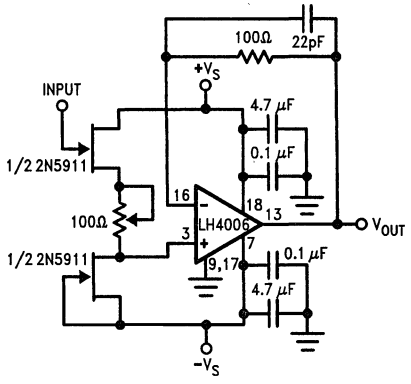
Input Capacitance

The input capacitance of the LH4006 is typically 8 pF and will slightly increase with frequency. A large source resistance value in front of this will form a pole, which may substantially reduce the bandwidth of the circuit and affect stability.

This is the reason why resistor values higher than 500Ω should not be used in the feedback network and high source impedance should be avoided.

Bias Current

The input bias current is typically 100 μA and may create an undesirable output offset voltage when the source impedance is high. An internal 50Ω resistor is provided for matching with a 50Ω source impedance in order to minimize the output offset voltage. *Figure 6* shows a circuit that uses a FET transistor pair for the input stage in order to reduce the input bias current to the sub-nanoampere region.



TL/K/9255–9

FIGURE 6. FET Input Follower Buffer

National Semiconductor

LH4008/LH4008C Fast Buffer

General Description

The LH4008 is a very high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 180 MHz. The LH4008/LH4008C will provide ±200 mA into 50Ω loads (±500 mA peak) at slew rates of 10,000 V/μs. In addition, it exhibits excellent phase linearity.

The LH4008 is intended to fulfill a wide range of buffer applications. Due to its high speed it does not degrade the system performance. Its high output current makes it adequate for most loads. Only a single +10V supply is needed for a 5 V_{PP} video signal. In addition, the LH4008 can continuously drive 50Ω coaxial cables.

These devices are constructed using specially selected junction FET's and active laser trimming to achieve guaranteed performance specifications. The LH4008K is specified for operation from −55°C to +125°C; whereas, the LH4008CK and LH4008CT are specified from −25°C to +85°C. LH4008K and LH4008CK are available in an 8-pin TO-3 package. The LH4008CT is available in an 11-pin TO-220 package.

Features

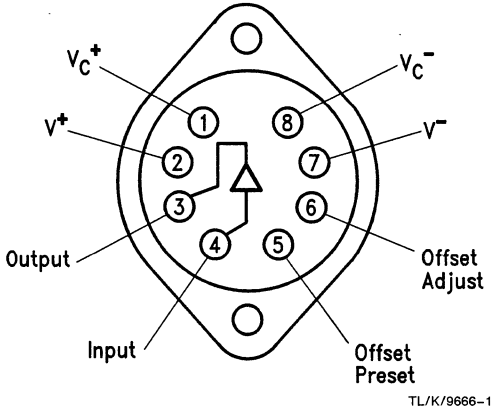
■ Fast	10,000 V/μs
■ Wide range single or dual supply operation	
■ Wide power bandwidth	DC to 130 MHz
■ High output drive	±10V with 50Ω load
■ Low phase non-linearity	< 2 degrees
■ Fast rise times	< 1.6 ns
■ High input resistance	> 10^{10}Ω
■ Pin compatible with LH0063	

Applications

- High speed line drivers
- Video impedance transformation
- Op amp isolation buffers
- Yoke driver for high resolution CRT
- High impedance input buffer

Connection Diagram

Metal Can Package (TO-3), 8 Pin



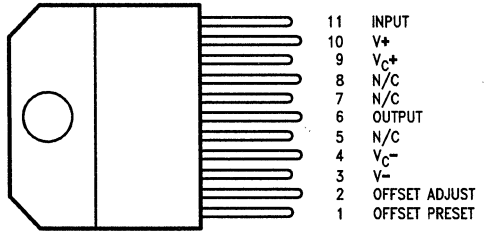
TL/K/9666–1

Note: Case is electrically isolated.

Top View

Order Number LH4008K or LH4008CK
See NS Package Number K08A

Plastic Package (TO-220), 11 Leads



TL/K/9666–18

Note: Metal tab is electrically isolated.

Top View

Order Number LH4008CT
See NS Package Number TA11B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curves)	3.2W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	±200 mA
Peak Output Current	±500 mA
Operating Temperature Range	
LH4008	−55°C to +125°C
LH4008C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD	TBD

DC Electrical Characteristics

V_S = ±15V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4008			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	(Note 4)	10	25		mV
				100		
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Output Offset Voltage	R_S < 100 kΩ	200			µV/°C
I_B	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$ (Note 4)	10	30		nA
				100		
A_V	Voltage Gain	V_{IN} = ±10V, R_L = 1 kΩ	0.95	0.94		V/V (Min)
				0.92		
A_V	Voltage Gain	V_{IN} = ±10V	0.94	0.90		V/V (Min)
				0.88		
C_{IN}	Input Capacitance	Case Shorted to Output	8			pF
R_{OUT}	Output Impedance	V_{OUT} = ±10V	1.8	**4**		Ω
V_O	Output Current Swing	V_{IN} = ±10V, R_S < 100 kΩ	0.25	**0.2**		Amps (Min)
V_O	Output Voltage Swing		11.9	±10.5		V (Min)
			11.1	**10.0**		
LSV_O	Low Supply Output Voltage Swing	V_S = ± 5.0V	±3.2	±2.5		V (Min)
I_S	Supply Current	R_L = ∞, V_S = ±15V	60	70		mA
I_S	Supply Current	R_L = ∞, V_S = ±15V, T_A = +125°C	52	70		mA
I_S	Supply Current	R_L = ∞, V_S = ±15V, T_A = −55°C	88	135		mA
I_S	Supply Current	V_S = ±5.0V	45			mA
P_D	Power Consumption	R_L = ∞, V_S = ±15V	1.8	2.1		W
P_D	Power Consumption	V_S = ±5.0V	450			mW

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4008C is −25°C to +85°C, and LH4008 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_J = 25°C.

DC Electrical Characteristics

V_S = ±15V, R_S = R_L = 50Ω, T_A = 25°C unless otherwise specified (Note 1) (Continued)

Symbol	Parameter	Conditions	LH4008C			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	(Note 4)	10	50		mV
$\Delta V_{OS}/\Delta T$	Avererage Temperature Coefficient of Output Offset Voltage	R_S < 100 kΩ	200			μV/°C
I_B	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$ (Note 4)	10	30		nA
A_V	Voltage Gain	V_{IN} = ±10V, R_L = 1 kΩ	0.95	0.92		V/V
A_V	Voltage Gain	V_{IN} = ±10V	0.94	0.9		V/V
C_{IN}	Input Capacitance	Case Shorted to Output	8			pF
R_{OUT}	Output Impedance	V_{OUT} = ±10V	1.8	4		Ω
V_O	Output Current Swing	V_{IN} = ±10V, R_S < 100 kΩ	0.25	0.2		Amps
V_O	Output Voltage Swing		11.9	±10.5		V
LSV_O	Low Supply Output Voltage Swing	V_S = ± 5.0V	±3.2	±2.5		V (Min)
I_S	Supply Current	R_L = ∞, V_S = ±15V	60	70		mA
I_S	Supply Current	V_S = ±5.0V	45			mA
P_D	Power Consumption	R_L = ∞, V_S = ±15V	1.8	2.1		W
P_D	Power Consumption	V_S = ±5.0V	450			mW

AC Electrical Characteristics LH4008 (T_J = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 50Ω)

Symbol	Parameter	Conditions	LH4008C/LH4008			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
S_R	Slew Rate Rising Edge	V_{IN} = 20 V_{P-P} 20%–80%	10000			V/μs
S_R	Slew Rate Falling Edge	V_{IN} = 20 V_{P-P} 20%–80%	7000			V/μs
BW	Bandwidth	V_{IN} = 1.0 Vrms	180	160		MHz
PBW	Power Bandwidth	V_{IN} = 20 V_{P-P}	130	110		MHz
	Phase Non-Linearity	BW = 1.0 to 50 MHz	2			degrees
t_r	Rise Time	ΔV_{IN} = 20 V_{P-P}	1.6			ns
t_p	Propagation Delay	ΔV_{IN} = 20 V_{P-P}	1.2			ns
	Harmonic Distortion		< 0.1			%

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4008C is −25°C to +85°C, and LH4008 is −55°C to +125°C.

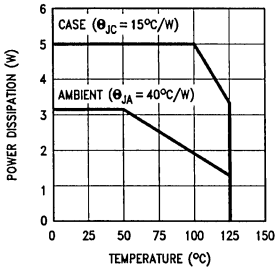
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality level.

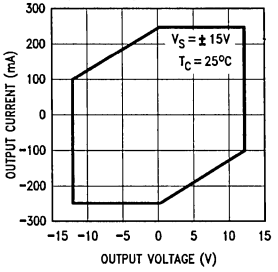
Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_J = 25°C.

Typical Performance Characteristics

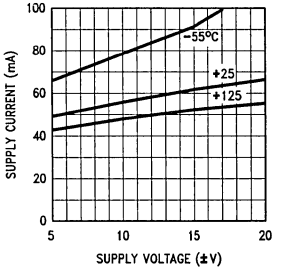
Maximum Power Dissipation vs Temperature



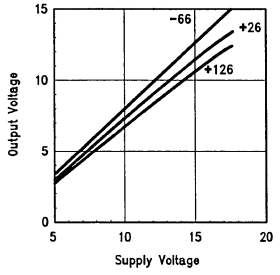
DC Safe Operating Area



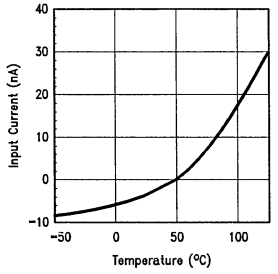
Supply Current vs Supply Voltage



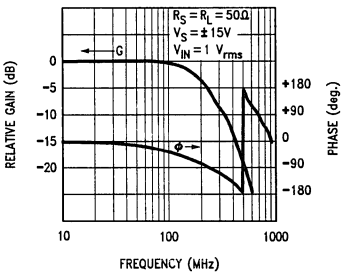
Output Swing vs Supply Voltage



Input Bias Current vs Temperature

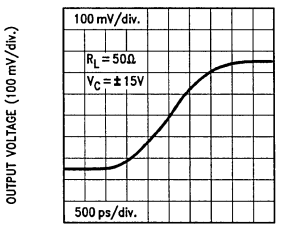


Gain Phase vs Frequency



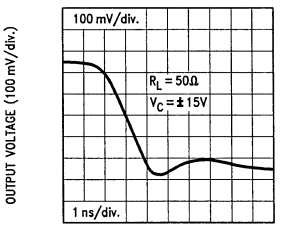
TL/K/9666-5

Small Signal Rise Time



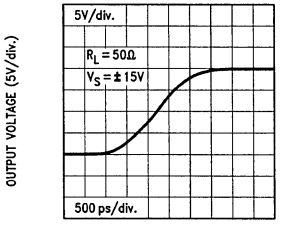
TL/K/9666-12

Small Signal Fall Time



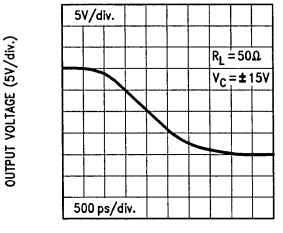
TL/K/9666-13

Large Signal Rise Time



TL/K/9666-14

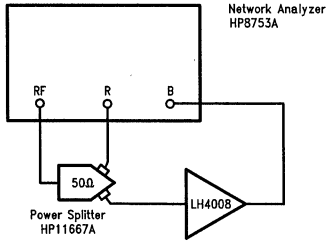
Large Signal Fall Time



TL/K/9666-15

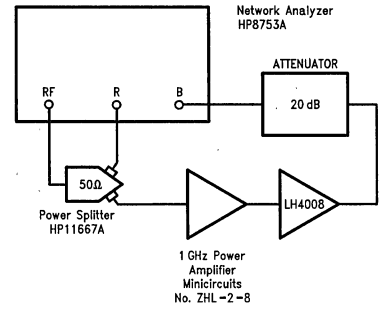
4

Bandwidth Test Circuit



TL/K/9666-3

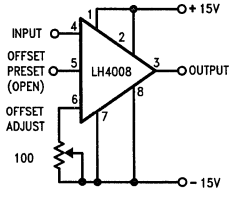
Power Bandwidth Test Circuit



TL/K/9666-4

Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4008 since it will provide power gain to frequencies over 180 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.



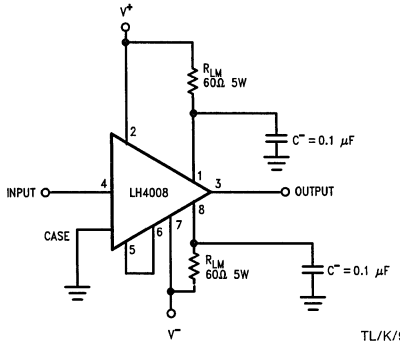
TL/K/9666-6

FIGURE 2. Offset Zero Adjust

Short Circuit Protection: Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 2* and *3*. Resistor values may be predicted by:

$$R_{LIM} = \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses.



TL/K/9666-7

FIGURE 3. Using Resistor Current Limiting

Capacitive Loading: The LH4008 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (C × dV/dt), should be limited below absolute maximum peak current ratings for the devices.

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below package power rating:

$$P_{diss} \geq P_{DC} + P_{AC}$$
pkg.

$$P_{diss} \geq (V^+ - V^-) \times I_S + P_{AC}$$
pkg.

$$P_{AC} = (V_{p\text{-}p})^2 \times f \times C_L$$

where

$V_{p\text{-}p}$ = Peak-to-peak output voltage swing

f = frequency

C_L = Load Capacitance

Operation within an Op Amp Loop: The device may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6161, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4008. The wide bandwidth and high slew rate of the LH4008 assures that the loop has the characteristics of the op amp and that additional rolloff is not required.

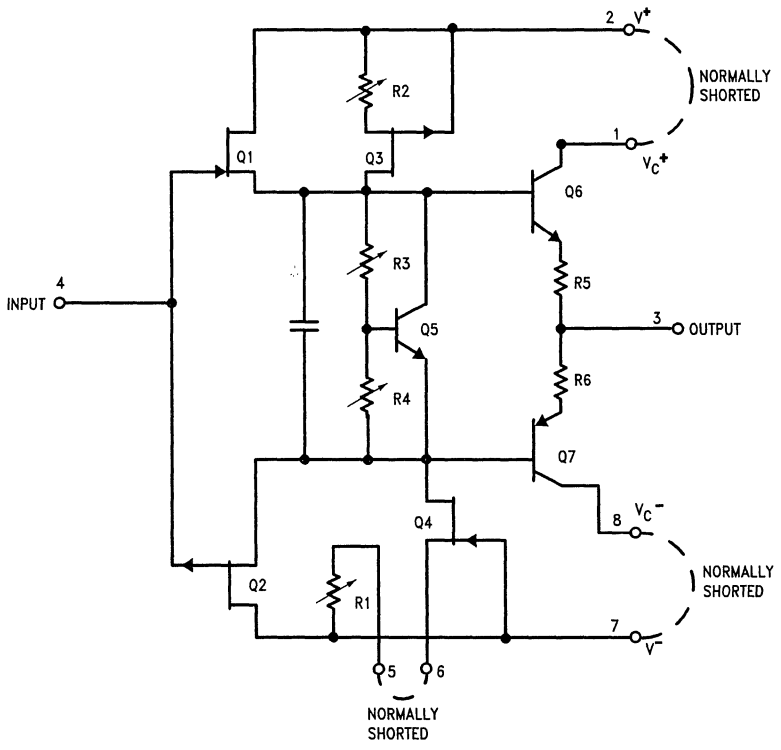
Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ATTENTION!

Power supply bypassing is necessary to prevent oscillation in all circuits. Low inductance ceramic disc capacitance with the shortest practical lead lengths must be connected from each supply lead (within < ¼ to ½" of the device package) to a ground plane. Capacitors should be two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel on each supply lead.

Schematic Diagram

LH4008/LH4008C

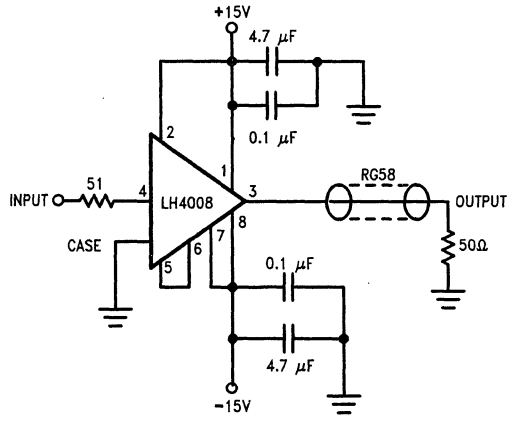


TL/K/9666-2

FIGURE 1

Typical Applications

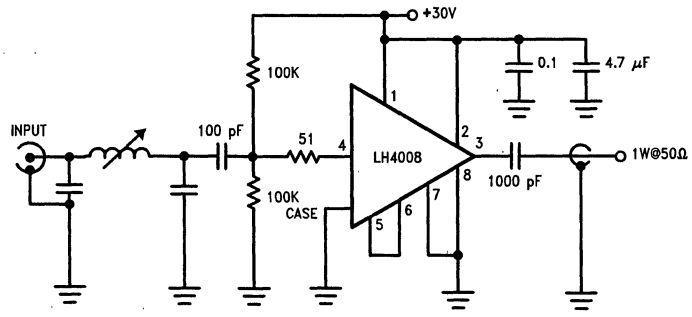
Coaxial Cable Driver



TL/K/9666-8

Typical Applications (Continued)

1W CW Final Amplifier



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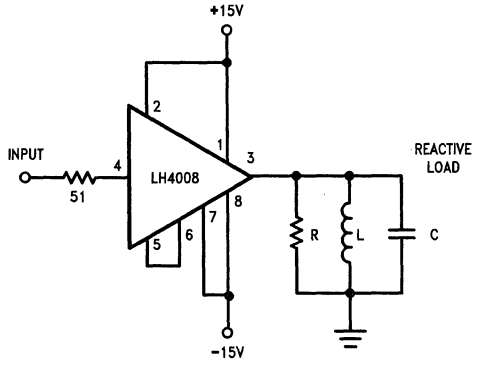
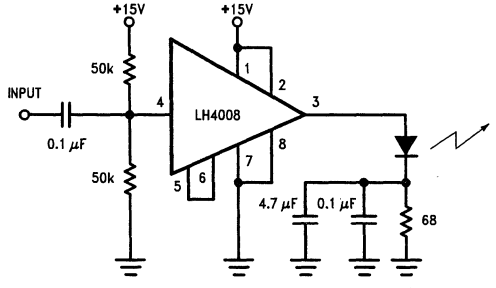
Isolation Buffer



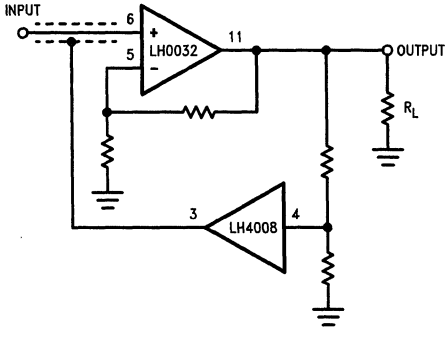
TL/K/9666-11

Laser Diode Transmitter



TL/K/9666-16

Guard Driver



TL/K/9666-17

National Semiconductor

LH4009/LH4009C Fast Buffer

General Description

The LH4009 is a very high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 190 MHz. The LH4009/LH4009C will provide ±200 mA into 50Ω loads (±250 mA peak) at slew rates of 10000V/μs. In addition, it exhibits excellent phase linearity.

The LH4009 is intended to fulfill a wide range of buffer applications. Due to its high speed it does not degrade the system performance. Its high output current makes it adequate for most loads. Only a single +10V supply is needed for a 5 V_{PP} video signal. In addition, the LH4009 can continuously drive 50Ω coaxial cables.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH4009K is specified for operation from −55°C to +125°C; whereas, the LH4009CK is specified from −25°C to +85°C. LH4009K and LH4009CK are available in an 8-pin TO-3 package. LH4009CT is available in an 11-pin TO-220 package and is specified from −25°C to +85°C.

Features

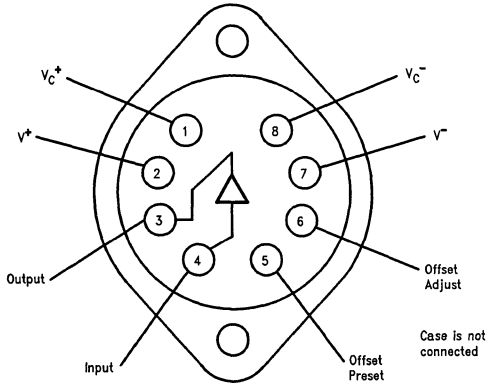
Fast	10000V/μs
Wide range single or dual supply operation	
Wide power bandwidth	DC to 150 MHz
High output drive	±10V with 50Ω load
Low phase non-linearity	2 degrees
Fast rise times	2 ns
High input resistance	$10^{10}\Omega$
Pin compatible with LH0063	
Built in short circuit protection	

Applications

- High speed line drivers
- Video impedance transformation
- Op amp isolation buffers
- Yoke driver for high resolution CRT
- High impedance input buffer

Connection Diagrams

Metal Can Package (TO-3), 8-Pin

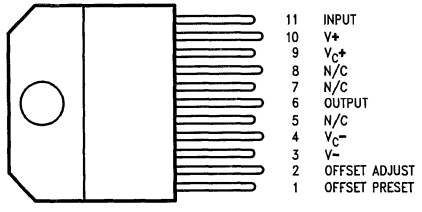


TL/K/9405–2

Top View

Order Number LH4009K or LH4009CK
See NS Package Number K08A

Plastic Package (TO-220), 11 Pin



TL/K/9405–18

Top View

Metal Tab is Electrically Isolated

Order Number LH4009CT
See NS Package Number TA11B

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (see Curves)	3W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	±200 mA
Peak Output Current	±250 mA
Duration of Short Circuit Protection	30 sec
Operating Temperature Range	
LH4009	−55°C to +125°C
LH4009C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD	TBD

DC Electrical Characteristics $V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	LH4009			Units (Max unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	(Note 4)	10	25 **150**		mV
I_B	Input Bias Current	(Note 4)	5	30 **100**		nA
Av	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.92	0.9 **0.85**		V/V (Min)
Av	Voltage Gain	$V_{IN} = \pm 10V$	0.87	0.85 **0.8**		V/V (Min)
C_{IN}	Input Capacitance		10			pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$		**5**		Ω
V_O	Output Voltage Swing		±11	±10 **±8**		V (Min)
LSV_O	Low Supply Output Voltage Swing	$V_S = \pm 5.0V$		±2.5		V (Min)
I_S	Supply Current	$V_S = \pm 15V$, $R_L = \infty$,	47	60 **75**		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5.0V$	45	60		mA
P_D	Power Consumption	$V_S = \pm 15V$, $R_L = \infty$	1.26	1.8		W
P_D	Power Consumption	$V_S = \pm 5.0V$, $R_L = \infty$		600		mW

DC Electrical Characteristics $V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = 25°C$ unless otherwise specified

Symbol	Parameter	Conditions	LH4009C			Units (Max unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	(Note 4)	10	50		mV
I_B	Input Bias Current	(Note 4)	5	30		nA
Av	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.92	0.9		V/V (Min)
Av	Voltage Gain	$V_{IN} = \pm 10V$	0.87	0.85		V/V (Min)
C_{IN}	Input Capacitance					pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$		5		Ω
V_O	Output Voltage Swing		±11	±10		V (Min)
V_O	Output Voltage Swing	$V_S = \pm 5.0V$		±2.5		V (Min)
I_S	Supply Current	$V_S = \pm 15V$, $R_L = \infty$	42	60		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5.0V$	45	60		mA
P_D	Power Consumption	$V_S = \pm 15V$, $R_L = \infty$	1.26	1.8		W
P_D	Power Consumption	$V_S = \pm 5.0V$, $R_L = \infty$		600		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$

Symbol	Parameter	Conditions	LH4009			Units (Max unless otherwise noted)
			Typical	Tested Limit (Note 2)	Design LImit (Note 3)	
SR	Slew Rate Rising Edge	$V_{IN} = 20\ V_{PP}$ 20%–80%	11,000			V/μs (Min)
SR	Slew Rate Falling Edge	$V_{IN} = 20\ V_{PP}$ 20%–80%	8000			V/μs (Min)
BW	Bandwidth	$V_{IN} = 1.0$ Vrms	190	160		MHz (Min)
PBW	Power Bandwidth	$V_{IN} = 20\ V_{PP}$	150	130		MHz (Min)
	Rise Time	$\Delta V_{IN} = 20\ V_{PP}$	1.2			ns
	Propagation Delay	$\Delta V_{IN} = 20\ V_{PP}$	1.3			ns

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4009C is −25°C to +85°C, and LH4009 is −55°C to +125°C.

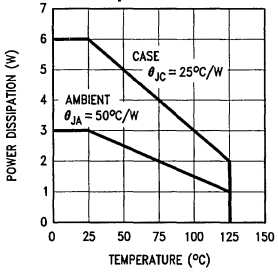
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

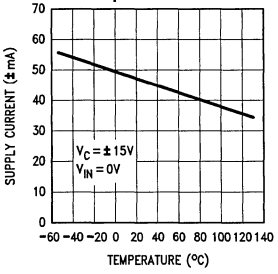
Note 4: Specifications are at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

Typical Performance Characteristics

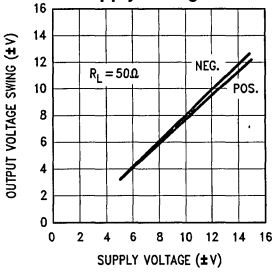
Maximum Power Dissipation vs Temperature



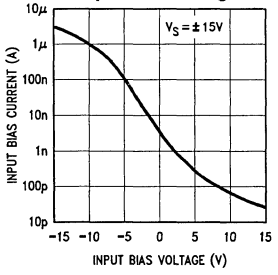
Supply Current vs Temperature



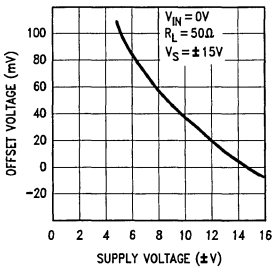
Output Voltage Swing vs Supply Voltage



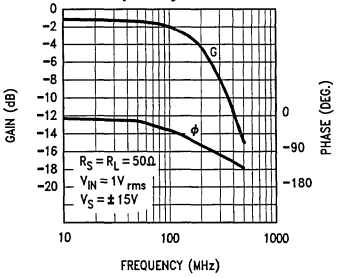
Input Bias Current vs Input Bias Voltage



Offset Voltage vs Supply Voltage



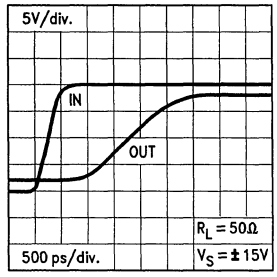
Gain and Phase vs Frequency



TL/K/9405–9

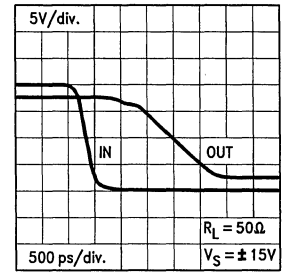
Typical Performance Characteristics (Continued)

Large Signal Rise Time



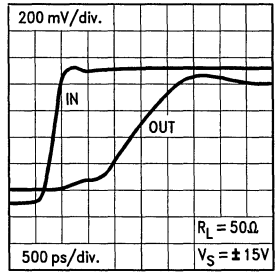
TL/K/9405–10

Large Signal Fall Time



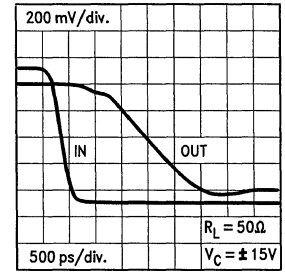
TL/K/9405–11

Small Signal Rise Time



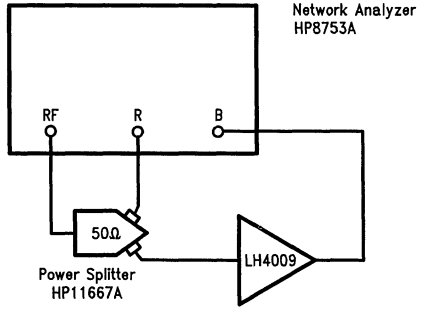
TL/K/9405–12

Small Signal Fall Time



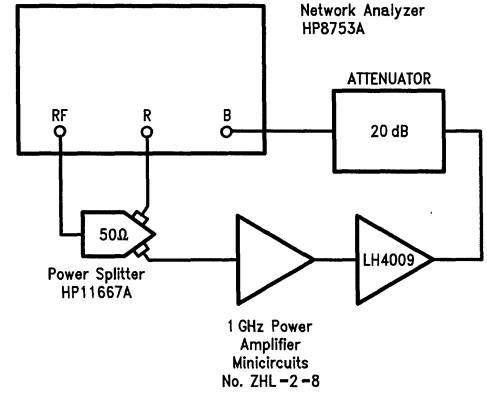
TL/K/9405–13

Bandwidth Test Circuit



TL/K/9405–14

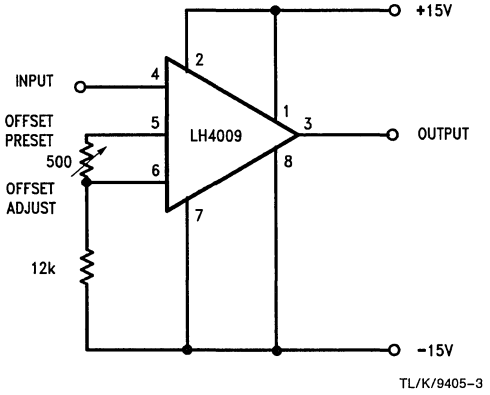
Power Bandwidth Test Circuit



TL/K/9405–15

Application Hints

RECOMMENDED LAYOUT PRECAUTIONS: RF/video printed circuit board layout rules should be followed when using the LH4009 since it will provide power gain to frequencies over 200 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.



TL/K/9405–3

FIGURE 1. Offset Zero Adjust

SHORT CIRCUIT PROTECTION: The LH4009 features built-in short circuit protection. It will protect the device against output shorts to ground for up to 30 seconds. Beyond that the device may get degraded.

CAPACITIVE LOADING: The LH4009 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (C × dV/dt), should be limited below absolute maximum peak current ratings for the devices.

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

In addition, power dissipation resulting from driving capactive loads plus standby power should be kept below package power rating:

$$P_{diss} \geq P_{DC} + P_{AC}$$
$$\text{pkg.}$$

$$P_{diss} \geq (V^+ - V^-) \times I_S + P_{AC}$$
$$\text{pkg.}$$

$$P_{AC} = (Vp\text{-}p)^2 \times f \times C_L$$

where $Vp\text{-}p$ = Peak-to-peak output voltage swing

f = frequency

C_L = Load Capacitance

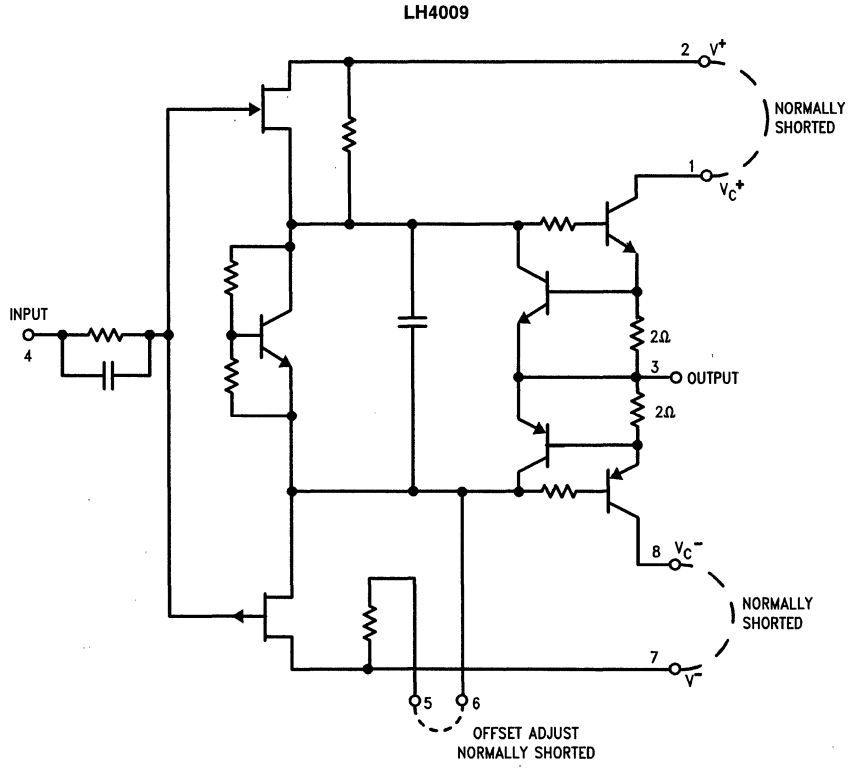
OPERATION WITHIN AN OP AMP LOOP: The device may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6161, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4009. The wide bandwidth and high slew rate of the LH4009 assures that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ATTENTION!

POWER SUPPLY BYPASSING is necessary to prevent oscillation in all circuits. Low inductance ceramic disc capacitance with the shortest practical lead lengths must be connected from each supply lead (within <¼ to ½" of the device package) to a ground plane. Capacitors should be two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel on each supply lead.

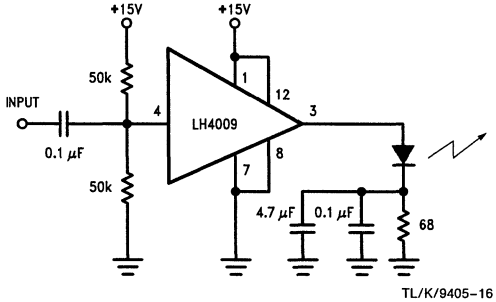
Schematic Diagram



TL/K/9405–1

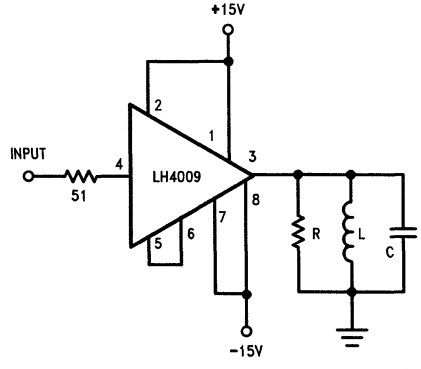
Typical Applications

Laser Diode Transmitter



TL/K/9405–16

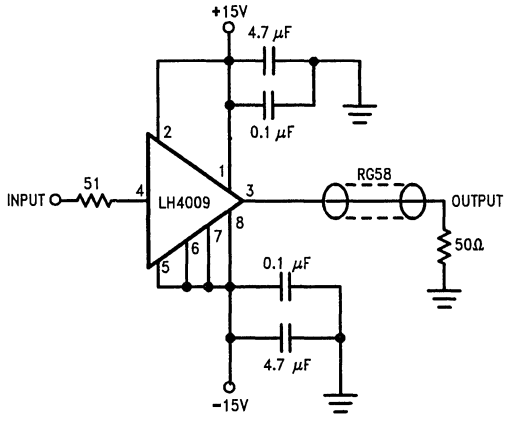
Isolation Buffer



TL/K/9405–6

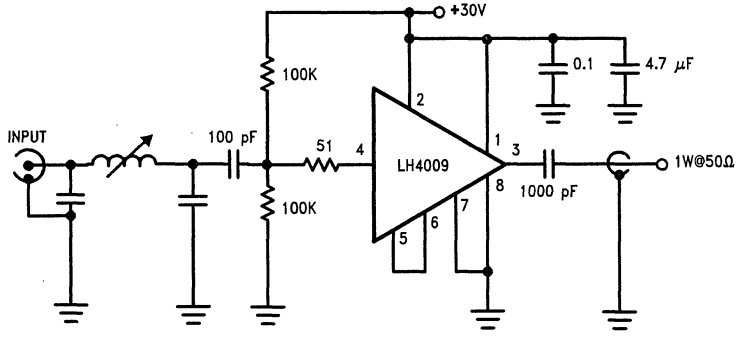
Typical Applications (Continued)

Coaxial Cable Driver



TL/K/9405-7

1W CW Final Amplifier



TL/K/9405-8

National Semiconductor

LH4010/LH4010C Fast FET Buffer

General Description

The LH4010/LH4010C is a high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 100 MHz. LH4010 will provide ±100 mA into 50Ω loads (±250 mA peak) at slew rates of 2500 V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

The LH4010 is intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed ADCs and comparators.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH4010 is specified for operation from −55°C to +125°C; whereas, the LH4010C is specified from −25°C to +85°C. The LH4010/LH4010C is available in a 1.5W metal TO-8 package or a 16 lead dual-in-line package, N16A.

Features

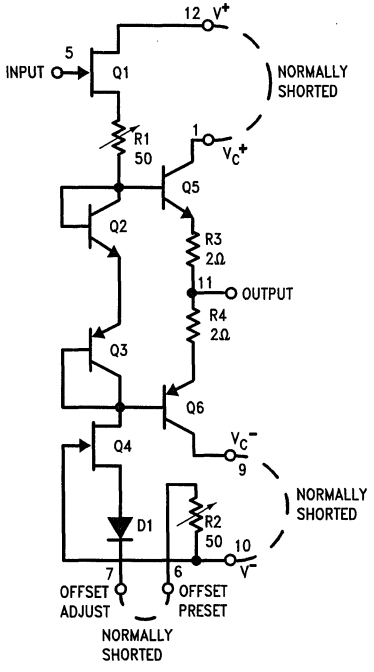
- Slew rate 2500 V/μs
- Wide range single or dual supply operation
- Power bandwidth DC to 20 MHz
- High output drive ±10V with 100Ω load
- Low phase non-linearity 2°
- Fast rise times 2 ns
- High current gain 120 dB
- High input resistance $10^{10}\Omega$
- Pin compatible with LH0033

Applications

- High speed cable driver
- Isolation buffer
- ADC input buffer
- Op amp current booster

Schematic and Connection Diagram

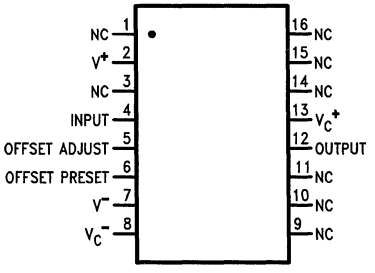
LH4010/LH4010C



TL/K/9349–16

Pin numbers shown for TO-8 ("G") package.

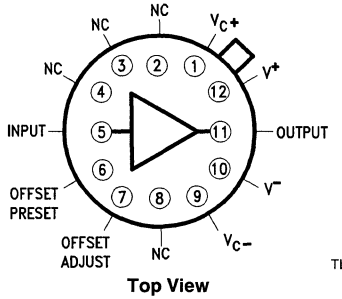
Top View



TL/K/9349–24

Order Number LH4010CN
See NS Package Number N16A

Metal Can Package (TO-8)



TL/K/9349–1

Top View

Case is Electrically Isolated.

Order Number LH4010G or LH4010CG
See NS Package Number H12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Maximim Power Dissipation (See Curves)	1.5W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Output Current, Continuous	±100 mA
Pulsed	±250 mA
Operating Temperature Range	
LH4010C	−25°C to +85°C
LH4010	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

V_S = ±15V, V_{IN} = 0V, R_L = 1k, T_A = 25°C unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4010C			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V, T_A = T_J = 25°C (Note 4)	5	10	**20**	mV
I_B	Input Bias Current	T_J = 25°C (Note 1)	0.5	1	**50**	nA
V_O	Output Voltage Swing	V_{IN} = ±14V (Note 1)		±12	**±12**	V (Min)
		V_{IN} = ±10.5, R_L = 100Ω		±9		V (Min)
R_{IN}	Input Impedance	T_J = 25°C, V_{IN} = ±1V	10^{10}			Ω
I_S	Supply Current		22	26		mA
R_{OUT}	Output Impedance	V_{IN} = $\pm V_{DC}$, ΔR_L = 100Ω to ∞		10		Ω
A_V	Voltage Gain	V_{IN} = ±10V		0.96	**0.96**	V/V (Min)
		V_{IN} = ±10V, R_L = 100Ω		0.90	**0.90**	V/V (Min)

DC Electrical Characteristics $V_S = \pm 15V$, $V_{IN} = 0V$, $R_L = 1k$, $T_A = 25°C$ otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4010			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset	$V_{IN} = 0V$, $T_A = T_J = 25°C$ (Notes 1, 4)	5	10		mV
				25		
I_B	Input Bias Current	$T_J = 25°C$ (Notes 1, 4)	200	500		pA
				10		nA
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$		**±12**		V (Min)
		$V_{IN} = \pm 10.5$, RL = 100Ω, $T_A = 25°C$		±9		V (Min)
R_{IN}	Input Impedance	$T_J = 25°C$, $V_{IN} = \pm 1V$	10^{10}			Ω
I_S	Supply Current		22	**26**		mA
R_{OUT}	Output Impedance	$V_{IN} = \pm V_{DC}$ (Note 4) $\Delta R_L = 100\Omega$ to ∞		**8**		Ω
A_V	Voltage Gain	$V_{IN} = \pm 10V$		**0.97**		V/V (Min)
		$V_{IN} = \pm 10V$, RL = 100Ω		**0.92**		V/V (Min)

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, $R_S = 50\Omega$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH4010/LH4010C			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
t_r	Small Signal Rise Time (Note 5)	$\Delta V_{IN} = 0.5V$	1.5			ns
		$R_L = 50\Omega$, $V_{IN} = 0.5V$		2.5		
t_p	Propagation Delay (Note 5)	$\Delta V_{IN} = 0.5V$	2.0			ns
BW	Small Signal Bandwidth (Note 7)		200			MHz (Min)
		$R_L = 50\Omega$			140	
SR	Slew Rate (Note 6)	$V_{IN} = \pm 5V$	2500	2000		V/μs (Min)

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4010C is −25°C to +85°C, and LH4010 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications are at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

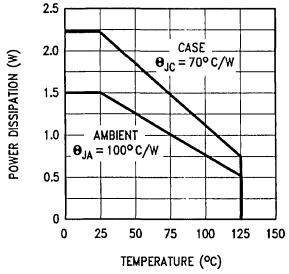
Note 5: See AC Test Circuit.

Note 6: Slew rate is measured between +2.5V and −2.5V. See AC Test Circuit.

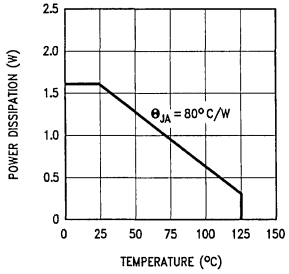
Note 7: Bandwidth is calculated from rise time with $f = t_r/\pi$.

Typical Characteristics

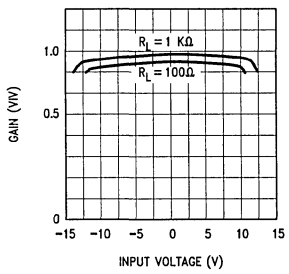
Maximum Power Dissipation for TO-8 ("G") Package



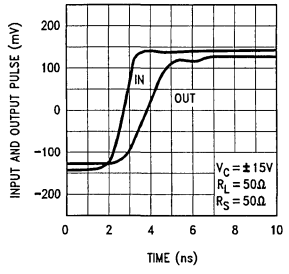
Maximum Power Dissipation for N16A Package



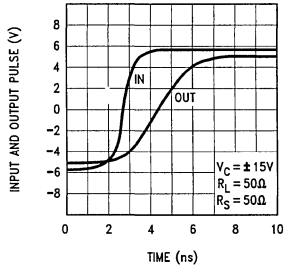
Gain vs Input Voltage



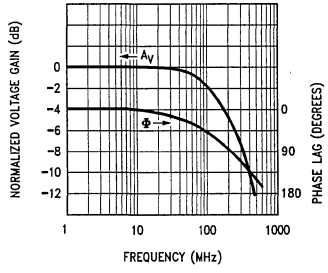
Small Signal Pulse



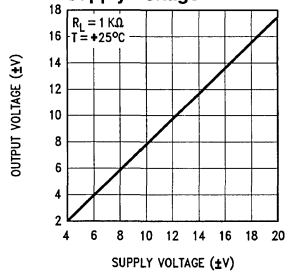
Large Signal Pulse



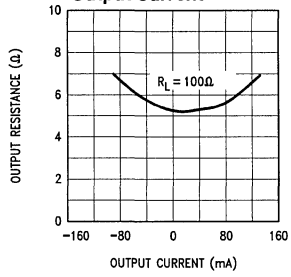
Frequency Response



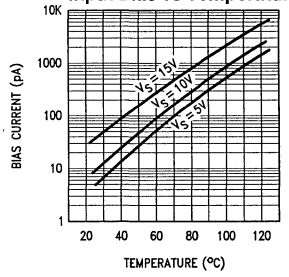
Output Voltage vs Supply Voltage



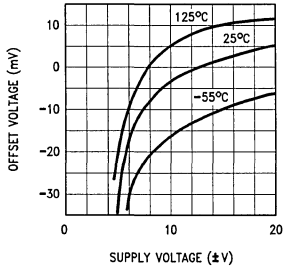
Output Resistance vs Output Current



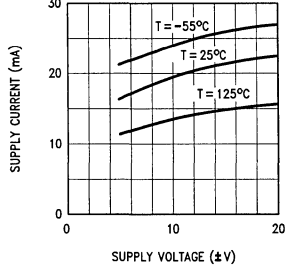
Input Bias vs Temperature



Offset Voltage vs Supply Voltage



Supply Current vs Supply Voltage



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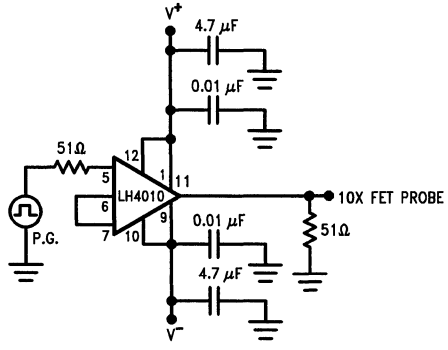
AC Test Circuit



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Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4010 and LH4010C since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment: Both the LH4010 and LH4010C offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω between the offset adjust pin and V^- as illustrated in *Figure 1*.

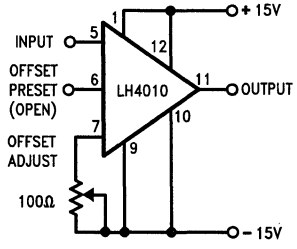

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FIGURE 1. Offset Zero Adjust for LH4010

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in application where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be −35 mV. This may be adjusted to zero as discussed above. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH4010 and LH4010C. Short circuit protection may be added by inserting appropriate value resistors between V^+ and $V_C{}^+$ pins and V^- and $V_C{}^-$ pins as illustrated in *Figure 2*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{-V^-}{I_{SC}}$$

where:

$$I_{SC} \leq 100\ mA$$

The inclusion of limiting resistors in the collectors of the output transitors reduces output voltage swing. Decoupling $V_C{}^+$ and $V_C{}^-$ pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing is shown in *Figure 3*.

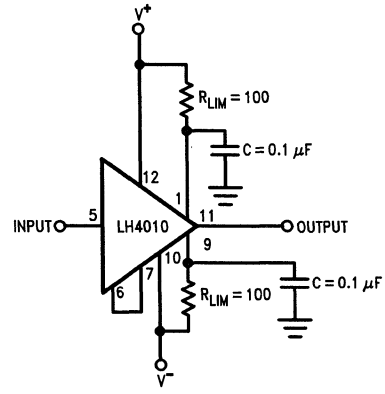

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FIGURE 2

Applications Hints (Continued)

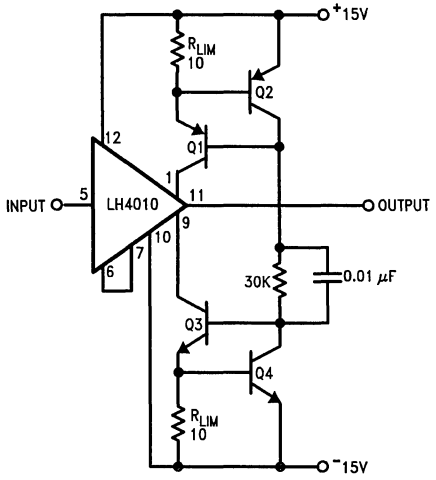

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FIGURE 3. LH4010 Current Limiting Using Current Sources

Capacitive Loading: The LH4010 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without being susceptible to oscillation. However, peak current resulting from (C × dV/dt) should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\left\{\frac{\Delta V_{IN}}{\Delta t}\right\} \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

In addition, power dissipation resulting from driving capcitative loads plus standby power should be kept below total package power rating:

$$P_{\substack{diss \\ pkg}} \geq P_{DC} + P_{AC}$$

$$P_{\substack{diss \\ pkg}} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{PP})^2 \times f \times C_L$$

where: V_{PP} = Peak-to-peak output voltage swing
f = frequency
C_L = Load Capacitance

Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6361, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4010. The wide bandwidths and high slew rates of the LH4010 assure that loop has the characteristics of the op amp and that additional rolloff is not required.

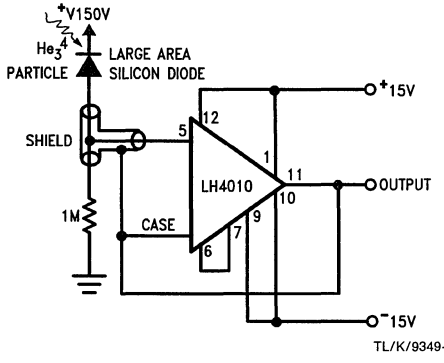
Hardware: In order to utilize the full drive capabilities of the device, it should be mounted with a heat sink particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

ATTENTION!

Power supply bypassing is necessary to prevent oscillation in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within < ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

Typical Applications

Nuclear Particle Detector



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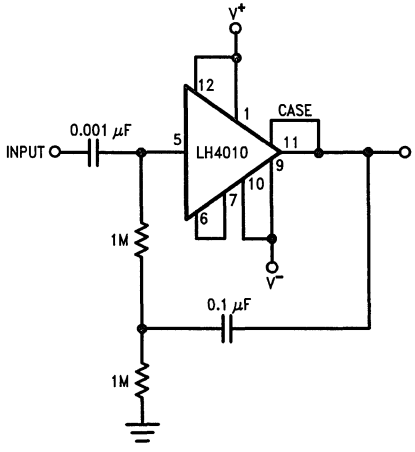
High Input Impedance AC Coupled Amplifier



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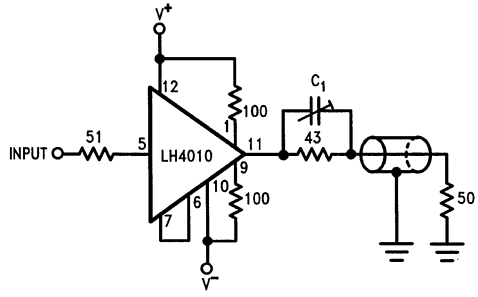
Typical Applications (Continued)

Coaxial Cable Driver



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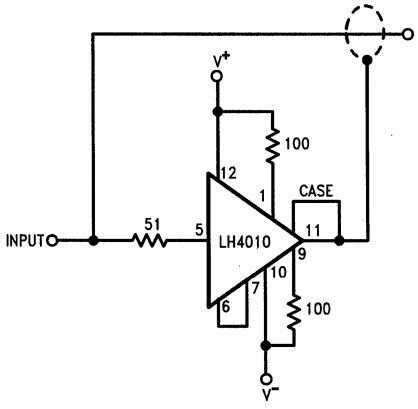
*Select C_1 for optimum pulse response.

Instrumentation Shield/Line Driver



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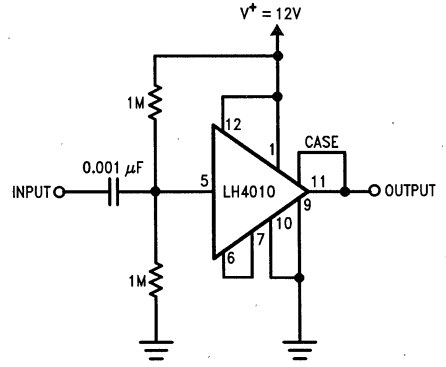
Single Supply AC Amplifier



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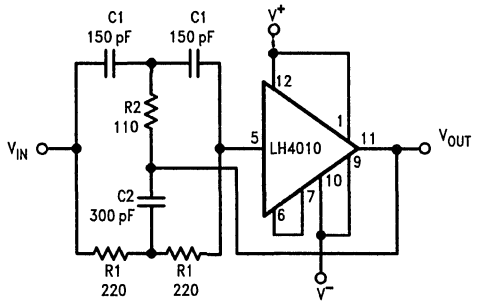
Typical Applications (Continued)

4.5 MHz Notch Filter



$$f_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\,R2$$

$$C1 = \frac{C2}{2}$$

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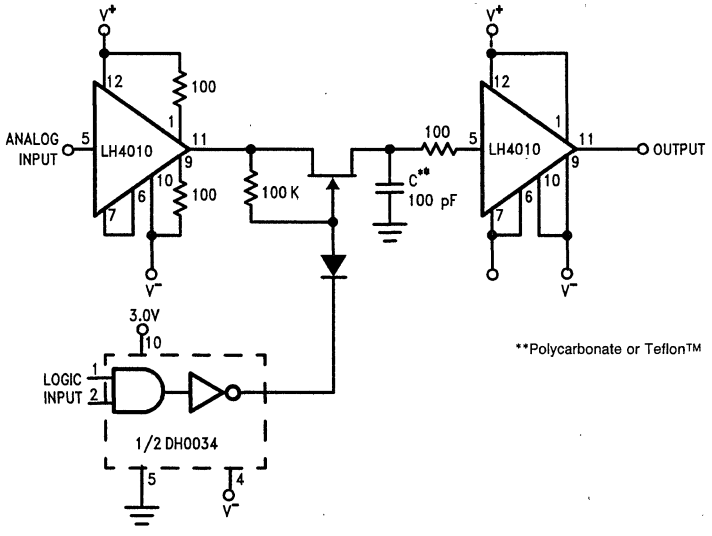
High Speed Sample and Hold



**Polycarbonate or Teflon™

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*Pin numbers shown for TO-8 ("G") package.

National Semiconductor

LH4011/LH4011C Fast Open Loop Buffer

General Description

The LH4011 is a very high speed, FET input, voltage follower/buffer designed to provide high current drive at frequencies from DC to over 150 MHz. The LH4011/LH4011C will provide ±200 mA into 50Ω loads (±500 mA peak) at slew rates of 5000 V/μs. In addition, it exhibits excellent phase linearity.

The LH4011 is intended to fulfill a wide range of buffer applications. Due to its high speed it does not degrade the system performance. Its high output current makes it adequate for most loads. Only a single +10V supply is needed for a 5 V_{PP} video signal. In addition, the LH4011 can continuously drive 50Ω coaxial cables.

These devices are constructed using specially selected junction FET's and active laser trimming to achieve guaranteed performance specifications. The LH4011K is specified for operation from −55°C to +125°C; whereas, the LH4011CK is specified from −25°C to +85°C. LH4011K and LH4011CK are available in a 5W 8-pin TO-3 package.

The LH4011CT is specified for operation from −25°C to +85°C and is available in an 11-pin TO-220 package.

Features

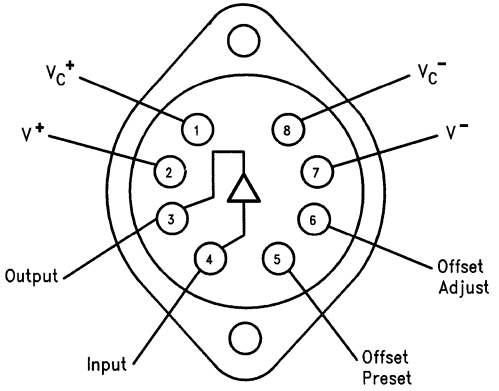
- Fast 5000V/μs
- Wide range single or dual supply operation
- Wide bandwidth DC to 160 MHz
- High output drive ±10V with 50Ω load
- Low phase non-linearity <2°
- Fast rise times <2 ns
- High input resistance $>10^{10}\Omega$
- Pin compatible with LH0063

Applications

- High speed line drivers
- Video impedance transformation
- Op amp isolation buffers
- Yoke driver for high resolution CRT
- High impedance input buffer

Connection Diagrams

Metal Can Package (TO-3), 8-Pin



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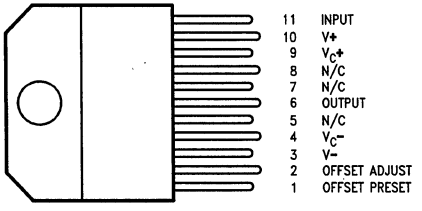
Top View

Note: Case is Electrically Isolated

Order Number LH4011K or LH4011CK

See NS Package Number K08A

Plastic Package (TO-220), 11-Pin



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Top View

Note: Metal Tab is Electrically Isolated

Order Number LH4011CT

See NS Package Number TA11B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Maximum Power Dissipation (See Curves)	3.2W
Maximum Junction Temperature	175°C
Input Voltage	Equal to Supplies
Continuous Output Current	±200 mA
Peak Output Current	±500 mA
Operating Temperature Range	
LH4011	−55°C to +125°C
LH4011C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD	TBD

DC Electrical Characteristics

V_S ±15V, RS = RL = 50Ω, T_A = 25°C unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4011			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	R_L = 50Ω R_S < 100 kΩ (Note 4)	10	25 **100**		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	R_S < 100 KΩ $T_{MIN} < T_A < T_{MAX}$	300			μV/°C
I_B	Input Bias Current	(Note 4)	10	30 **100**		nA
A_V	Voltage Gain	V_{IN} ±10V, R_L = 1 kΩ R_S < 100 kΩ	0.95	0.94 **0.92**		V/V (Min)
A_V	Voltage Gain	V_{IN} = ±10V, R_L = 50Ω R_S < 100 kΩ	0.94	0.92		V/V (Min)
C_{IN}	Input Capacitance	Case Shorted to Output	8			pF
R_{OUT}	Output Impedance	V_{OUT} = ±10V		**4**		Ω
V_O	Output Current Swing	V_{IN} = ±10V, R_S < 100 kΩ	0.25	**0.2**		Amps (Min)
V_O	Output Voltage Swing	R_L = 50Ω	11.4	**±10**		V (Min)
V_O	Output Voltage Swing	V_S = ±5.0V, R_L = 50Ω	±2.7	±2.5		V (Min)
I_S	Supply Current	R_L = ∞, V_S = ±15V	60	68		mA
I_S	Supply Current	V_S = ±5.0V	50			mA
P_D	Power Consumption	R_L = ∞, V_S = ±15V	1.8			W
P_D	Power Consumption	V_S = ±5.0V	0.5			W

DC Electrical Characteristics

V_S ±15V, RS = RL = 50Ω, T_A = 25°C unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4011C			Units (Max Unless Otherwise Noted
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset	T_J = 25°C, R_L = 50Ω R_S < 100 kΩ (Note 4)	10	50		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	R_S < 100 kΩ T_{MIN} < T_A < T_{MAX}	300			µV/°C
I_B	Input Bias Current	(Note 4)	10	30		nA
A_v	Voltage Gain	V_{IN} = ±10V, R_L = 1 kΩ R_S < 100 kΩ	0.95	0.92		V/V (Min)
A_v	Voltage Gain	V_{IN} = ±10V, R_L = 50Ω, T_J = 25°C R_S < 100 kΩ	0.94	0.9		V/V (Min)
C_{IN}	Input Capacitance	Case Shorted to Output	8			pF
R_{OUT}	Output Impedance	V_{OUT} = ±10V		4		Ω
V_O	Output Current Swing	V_{IN} = ±10V, R_S < 100 kΩ	0.25	0.2		Amps (Min)
V_O	Output Voltage Swing	R_L = 50Ω	11.4	±10		V (Min)
V_O	Output Voltage Swing	V_S = ±5.0V, R_L = 50Ω	±2.7	±2.5		V (Min)
I_S	Supply Current	R_L = ∞, V_S = ±15V	60	68		mA
I_S	Supply Current	V_S = ±5.0V	50			mA
P_D	Power Consumption	R_L = ∞, V_S = ±15V	1.8			W
P_D	Power Consumption	V_S = ±5.0V	0.5			W

AC Electrical Characteristics

T_J = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 50Ω

Symbol	Parameter	Conditions	LH4011C/LH4011			Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
SR	Slew Rate	R_L = 50Ω, V_{IN} = 20 V_{PP}, 20% to 80%	5000			V/µs
BW	Bandwidth	V_{IN} = 1.0 Vrms	160	140		MHz
PBW	Power Bandwidth	ΔV_{IN} = 20 V_{PP}	80	60		MHz (Min)
	Phase Non-Linearity	BW = 1.0 MHz to 50 MHz	2			deg.
	Rise Time	Δ V_{IN} = 1 V_{PP}	1.6			ns
	Propagation Delay	ΔV_{IN} = 1 V_{PP}	1.9			ns
	Harmonic Distortion		<0.1			%

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4011C is −25°C to +85°C, and LH4011 is −55°C to 125°C.

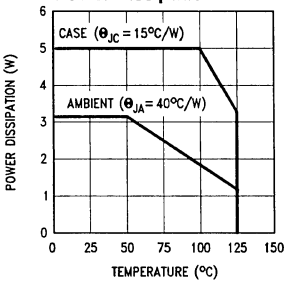
Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature range. These limtis are not used to calculate outgoing quality level.

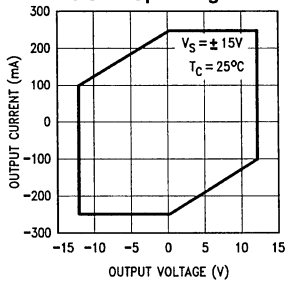
Note 4: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_J = 25°C.

Typical Performance Characteristics

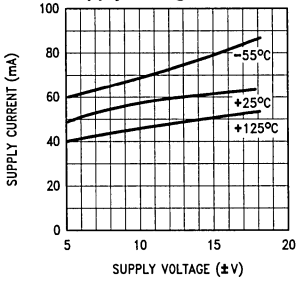
Power Dissipation



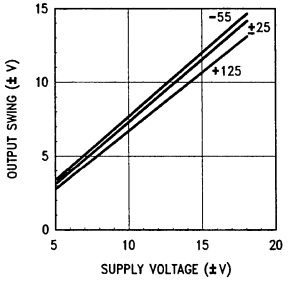
DC Safe Operating



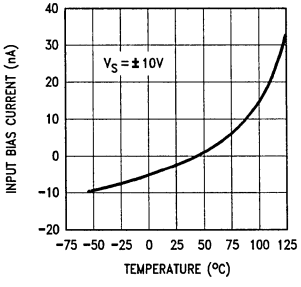
Supply Current vs Supply Voltage



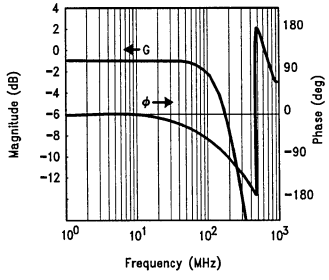
Output Swing vs Supply Voltage



Input Bias Current



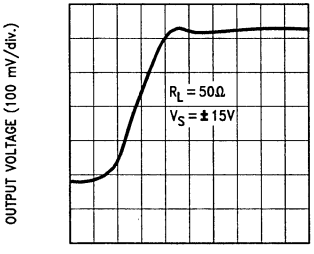
Frequency Response



TL/K/9423-3

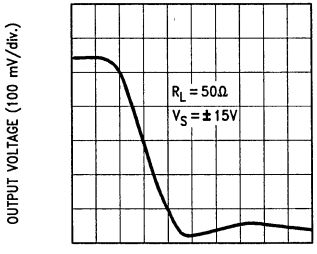
TL/K/9423-6

Small Signal Rise Time



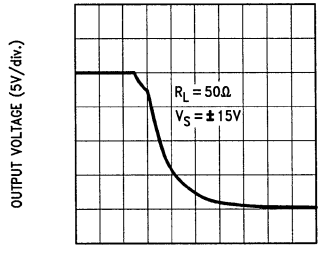
TL/K/9423-4

Small Signal Fall Time



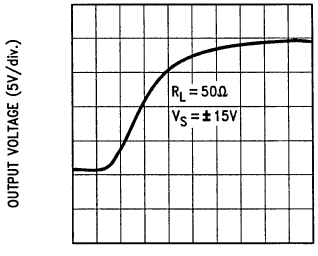
TL/K/9423-15

Large Signal Fall Time



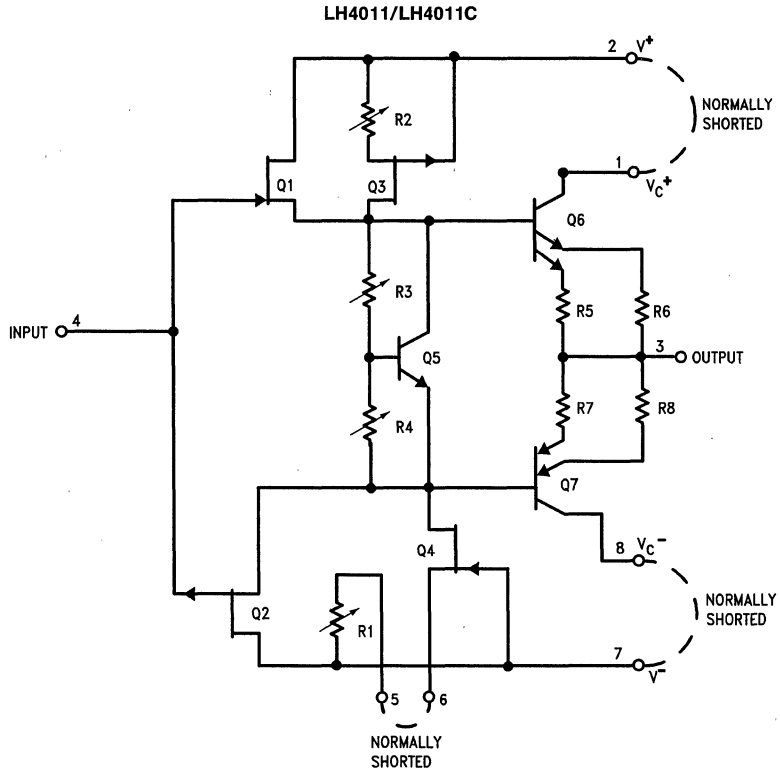
TL/K/9423-16

Large Signal Rise Time



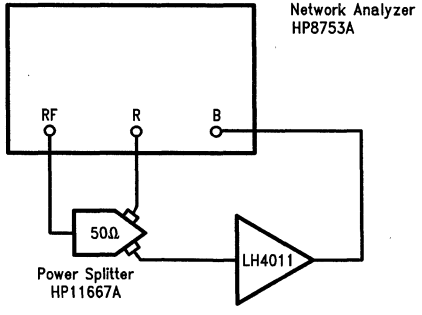
TL/K/9423-5

Schematic Diagram



TL/K/9423–2

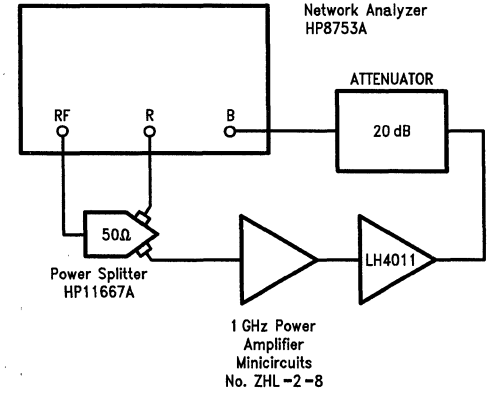
Bandwidth Test Circuit



TL/K/9423–13

FIGURE 1. Bandwidth Test Circuit

Power Bandwidth Test Circuit



TL/K/9423–14

FIGURE 2. Power Bandwidth Test Circuit

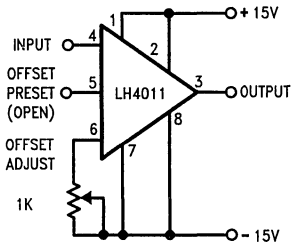
Application Hints

Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4011 since it will provide gain to frequencies over 160 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Short Circuit Protection: Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figure 4.* Resistor values may be predicted by:

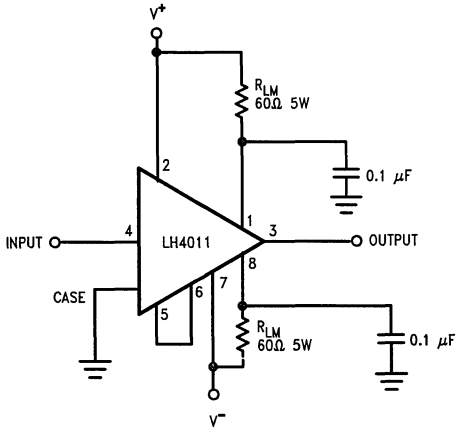
$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses.



TL/K/9423-7

FIGURE 3. Offset Zero Adjust



TL/K/9423-8

FIGURE 4. Using Resistor Current Limiting

Application Hints (Continued)

Capacitive Loading: The LH4011 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (C × dV/dt), should be limited below absolute maximum peak current ratings for the devices.

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the package power rating.

$$P_{\substack{diss \\ pkg.}} \geq P_{DC} + P_{AC}$$

$$P_{\substack{diss \\ pkg.}} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} = (V_{p\text{-}p})^2 \times f \times C_L$$

where $V_{p\text{-}p}$ = Peak-to-peak output voltage swing

f = frequency

C_L = Load Capacitance

Operation Within an Op Amp Loop: The device may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6161, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4011. The wide bandwidth and high slew rate of the LH4011 assures that the loop has the characteristics of the op amp and that additional compensation is not required.

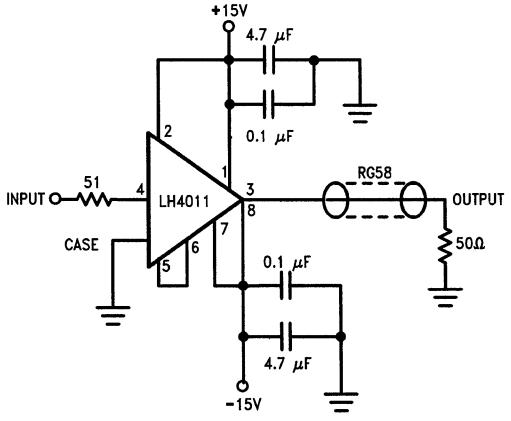
Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to system chassis.

ATTENTION!

Power supply bypassing is necessary to prevent oscillation in all circuits. Low inductance ceramic disc capacitance with the shortest practical lead lengths must be connected from each supply lead (within ¼ to ½" of the device package) to a ground plane. Capacitors should be two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel on each supply lead.

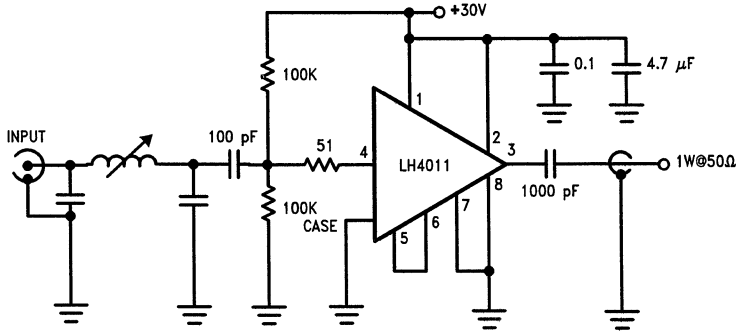
Typical Applications

Coaxial Cable Driver



TL/K/9423–9

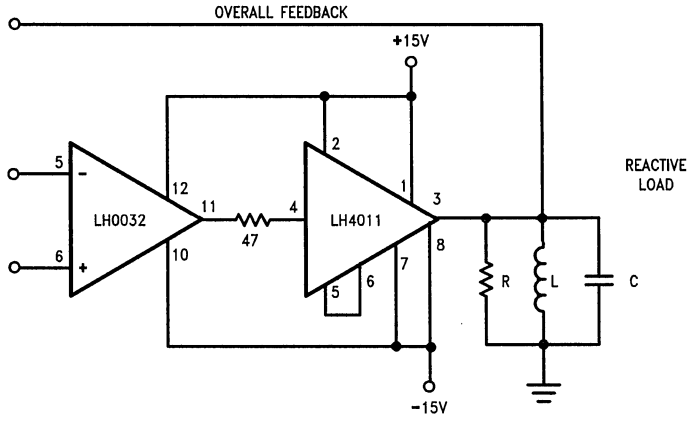
1W CW Final Amplifier



TL/K/9423–10

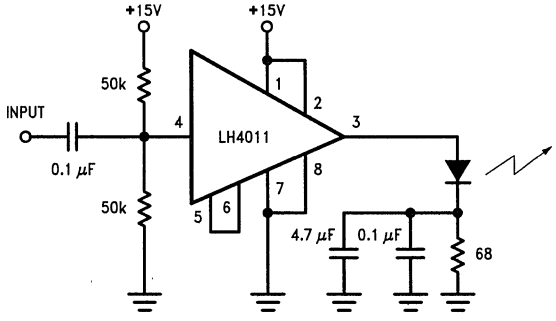
Typical Applications (Continued)

Isolation Buffer



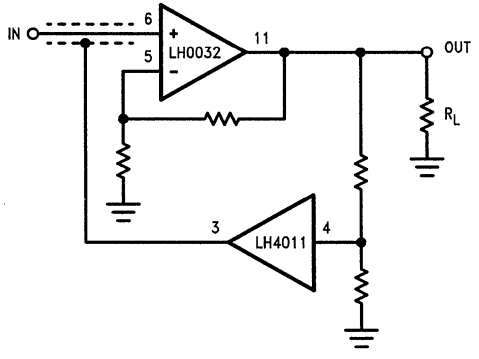
TL/K/9423–12

Laser Diode Transmitter



TL/K/9423–17

Guard Driver



TL/K/9423–18

National Semiconductor

LH4012/LH4012C Wideband Buffer

General Description

The LH4012 is a very high speed buffer designed to provide high current drive at frequencies from DC to over 400 MHz. The LH4012/LH4012C will provide ±200 mA into 50Ω loads at slew rates of 11500 V/μs. In addition, it exhibits excellent phase linearity.

The LH4012 is intended to fulfill a wide range of buffer applications. Due to its high speed it does not degrade the system performance. Its high output current makes it adequate for most loads. Only a single +10V supply is needed for a 5 V_{PP} video signal.

These devices are constructed using specially selected bipolar transistors to achieve guaranteed performance specifications. The LH4012K is specified for operation from −55°C to +125°C; the LH4012CK is specified from −25°C to +85°C. Both devices are available in an 8-pin TO-3 package.

Features

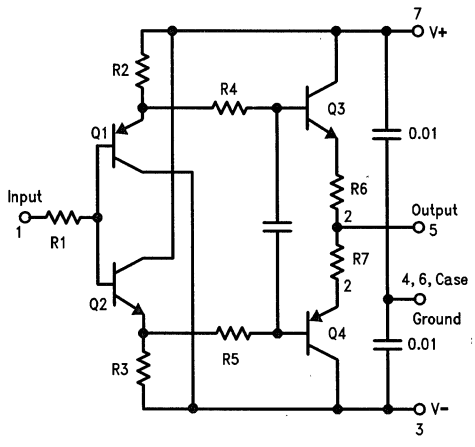
- Internal supply bypass capacitors
- Ultra fast slewing 11500 V/μs
- Wide range single or dual supply operation
- Wide bandwidth DC to 490 MHz
- High output drive ±10V with 50Ω load
- Low phase non-linearity 1 deg.
- Fast rise times 1.2 ns

Applications

- High speed line drivers
- Video impedance transformation
- Op amp isolation buffers
- Yoke driver for high resolution CRT

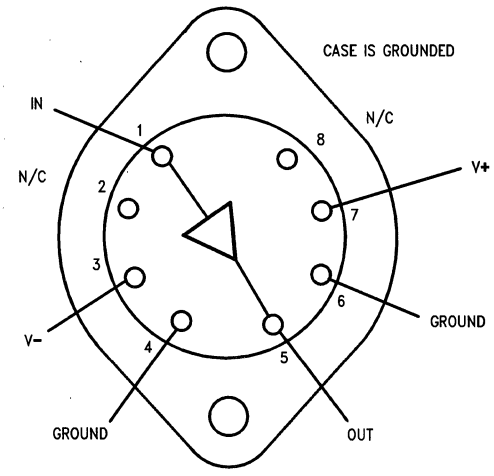
Schematic Diagram

LH4012



TL/K/9720–1

Metal Can Package (TO-3)



TL/K/9720–2

Top View

Case is Electrically Tied to Pins 4 and 6 (Ground)

Order Number LH4012K or LH4012CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V^+, $-V^-$)	40V
Maximum Power Dissipation (See Curves)	3W
Maximum Junction Temperature	175°C
Input Voltage	$\lvert V_{OUT} \pm V_{IN} \rvert < 3V$
Output Current, Continuous	±200 mA
Peak	±400 mA
Operating Temperature Range	
LH4012	−55°C to +125°C
LH4012C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD	TBD

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = +25°C$, unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4012			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset		±20	±50 **±55**		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	$T_{MIN} < T_A < T_{MAX}$	30			µV/°C
I_B	Input Bias Current (Note 4)		0.2	0.7		mA
A_V	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.98	0.95		V/V (Min)
A_V	Voltage Gain	$V_{IN} = \pm 10V$	0.93	0.9 **0.9**		V/V (Min)
C_{IN}	Input Capacitance		7			pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$	2.3	4.5		Ω
V_O	Output Voltage Swing		11.4	10 **9**		V (Min)
PSRR	Power Supply Rejection Ratio		70			dB
LSA_V	Low Supply Voltage Gain	$V_S = \pm 5V$, $V_{IN} = \pm 2.5V$	0.92	0.85 **0.85**		V/V (Min)
LSV_O	Low Supply Output Voltage Swing	$V_S = \pm 5V$	3.4	2.5		V (Min)
I_S	Supply Current	$R_L = \infty$, $V_S = \pm 15V$	65	75 **80**		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5V$	21	30		mA
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 15V$	1.95	2.25		W
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 5.0V$	0.21	0.3		W

DC Electrical Characteristics

$V_S = \pm 15V$, $R_S = R_L = 50\Omega$, $T_A = +25°C$, unless otherwise specified (Note 1)

Symbol	Parameter	Conditions	LH4012C			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Output Offset		±20	±50		mV
$\Delta V_{OS}/\Delta T$	Aver. Temp. Coeffic. of Output Offset Voltage	$T_{MIN} < T_A < T_{MAX}$	30			μV/°C
I_B	Input Bias Current (Note 4)		0.2	0.7		mA
A_V	Voltage Gain	$V_{IN} = \pm 10V$, $R_L = 1\ k\Omega$	0.98	0.95		V/V (Min)
A_V	Voltage Gain	$V_{IN} = \pm 10V$	0.93	0.9		V/V (Min)
C_{IN}	Input Capacitance		7			pF
R_{OUT}	Output Impedance	$V_{OUT} = \pm 10V$	2.3	4.5		Ω
V_O	Output Voltage Swing		11.4	10		V (Min)
PSRR	Power Supply Rejection Ratio		70			db (Min)
LSA_V	Low Supply Voltage Gain	$V_S = \pm 5V$, $V_{IN} = \pm 2.5V$	0.92	0.85		V/V (Min)
LSV_O	Low Supply Output Voltage Swing	$V_S = \pm 5V$	3.4	2.5		V (Min)
I_S	Supply Current	$R_L = \infty$, $V_S = \pm 15V$	65	75		mA
LVI_S	Low Voltage Supply Current	$V_S = \pm 5V$	21	30		mA
P_D	Power Consumption	$R_L = \infty$, $V_S = \pm 15V$	1.95	2.25		W
P_D	Power Consumption	$V_S = \pm 5.0V$	0.21	0.3		W

AC Electrical Characteristics

$T_J = +25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 5)

Symbol	Parameter	Conditions	LH4012/LH4012C			Units (Max unless Otherwise Noted)
			Typical	Tested Limit (Note 2)	Design Limit (Note 3)	
SR	Slew Rate	$V_{IN} = 20\ V_{P-P}$	11500			V/μs
SSBW	Small Signal Bandwidth	$V_{IN} = 0.223$ Vrms	460	400		MHz (Min)
PBW	Power Bandwidth	$R_L = 50\Omega$, $V_{IN} = 10\ V_{P-P}$	230	200		MHz
	Phase Non-Linearity	BW = 1.0 MHz to 100 MHz	1			Degrees
	Rise Time	$V_{IN} = 20\ V_{P-P}$, $t_r = 500$ ps	1.2			ns
	Propagation Delay	$V_{IN} = 20\ V_{P-P}$	1			ns
	Harmonic Distortion	$V_{IN} = 10\ V_{P-P}$, f = 100 MHz	0.5			%

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4012C is −25°C to +85°C, and LH4012 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

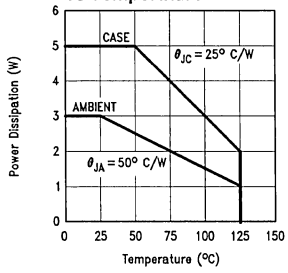
Note 3: Design limits are guaranteed (but not production tested) over the indicated temperature or temperature range. These limits are not used to calculate outgoing quality level.

Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_J = 25°C$.

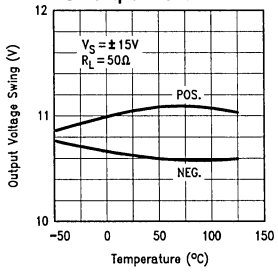
Note 5: For test circuits see *Figures 1, 2.*

Typical Performance Characteristics

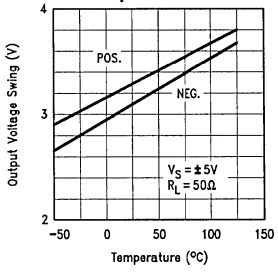
Power Dissipation vs Temperature



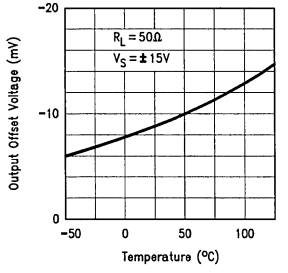
Output Voltage Swing vs Temperature



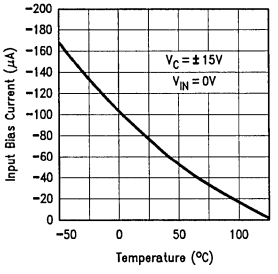
Output Voltage Swing vs Temperature



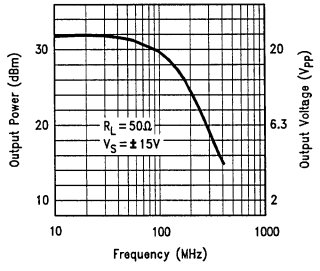
Output Offset Voltage vs Temperature



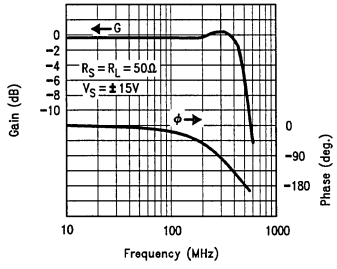
Input Bias Current vs Temperature



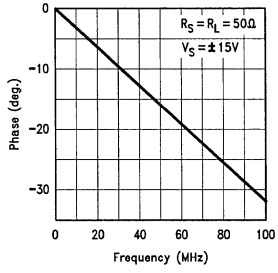
1 dB Compression vs Frequency



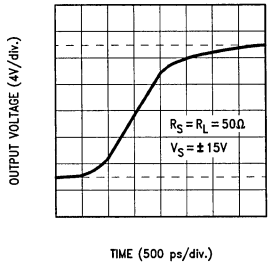
Gain and Phase vs Frequency



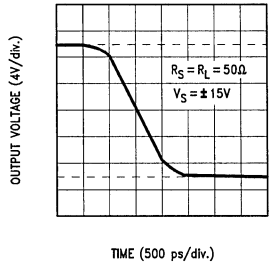
Phase vs Frequency



Rise Time



Fall Time



TL/K/9720–3

Typical S Parameters $V_S = \pm 15V$, $R_L = R_S = 50\Omega$

f	S11		S21		S12		S22	
MHz	Mag	Ang	dB	Ang	dB	Ang	Mag	Ang
10	0.99	−3	5.27	−3.7	−60	54	0.87	176
100	0.99	−26	5.20	−33	−32	129	0.92	167
250	1.0	−82	5.15	−94	−14	69	0.94	138
500	0.80	−170	1.20	−182	−10	−22	0.60	96

Small Signal Bandwidth Test Circuit

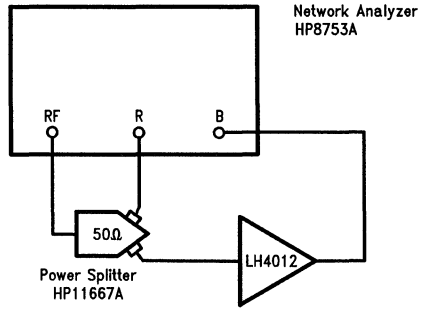


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FIGURE 1. Small Signal Bandwidth Test Circuit

Power Bandwidth Test Circuit

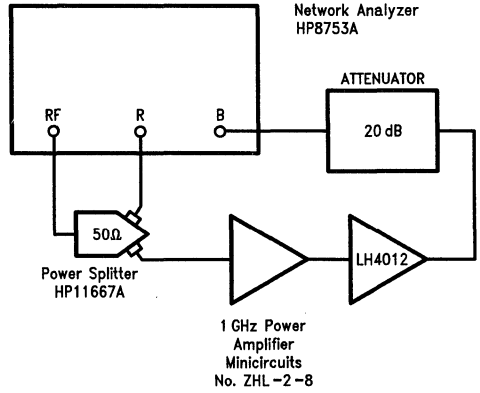

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FIGURE 2. Power Bandwidth Test Circuit

Application Information

LAYOUT: Breadboards should have a solid ground plane and short point-to-point wiring. Do not use wire wrap boards or techniques. PC boards should have short connections and as much ground plane as possible.

It is best to have a layout without sockets, but sockets with shortpins and receptacles do not significantly degrade the performance.

The LH4012 has built-in 0.01 μF power supply bypass capacitors, but additional 4.7 μF tantalum capacitors are needed a maximum of 1" distant from the pins.

Input and output signals should be fed by coax or microstrip if the distances are more than a few inches to avoid impedance mismatches and resulting reflections. However, inside a feedback loop all connections should be short to avoid time delays and the associated phase shifts.

SOURCE RESISTANCE: The LH4012 is designed to work from a 50Ω or higher source impedance. If driven from a low source impedance, especially if it is inductive, a series input resistor is recommended that brings the source impedance to 50Ω, or instabilities could result.

CAPACITIVE LOADING: As with all buffers, capacitive loading can lead to instabilities. This can be minimized by reducing the phase angle of the load with a resistor either in series or in parallel with the capacitor or with a combination of both.

The charge current of the load capacitor,

$$C\ Load \times \frac{dV}{dT}$$

should be considered when the load current is checked against its absolute maximum limit.

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the package power rating.

$P_{AC} + P_{DC} < P_{Pkg.\ Diss.}$

$P_{AC} = (V_{PP})^2 \times f \times C\ load$

$P_{DC} = (V^+ - V^-) \times I_S$

where V_{PP} = output voltage swing
f = Frequency

OPERATION WITHIN AN OP AMP LOOP: The device may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LM6161, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of the LH4012. The wide bandwidth and high slew rate of the LH4012 assures that the loop has the characteristics of the op amp and that additional frequency compensation is not required.

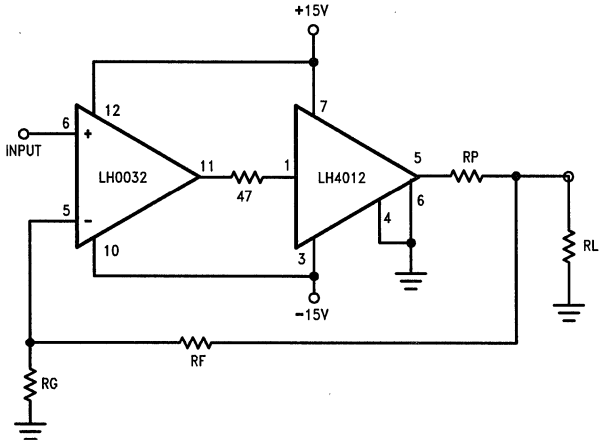
HEATSINK: In order to utilize the full drive capabilities of both the LH4012K or the LH4012CK, the device should be mounted with a heatsink, particularly for extended temperature operation.

VOLTAGE SWING: Input voltage is allowed to swing between positive and negative supply voltage levels, but it must be within $\pm$3V of the output voltage. If the voltage differential from input to output is greater than $\pm$3V the base-to-emitter diode of one of the input transistors will be broken down in reverse and the transistor will be degraded and could be destroyed.

SHORT CIRCUIT PROTECTION: In the interest of high performance the LH4012 has been designed without built-in protection. The simplest protection is a series resistor in the output. This approach has the advantage that input and output voltage of the buffer stay close together even during a shorted load. The main disadvantage is that the output voltage swing is reduced. Accuracy is normally not a problem, since the voltage drop across the protection resistor can be compensated for by more gain somewhere else in the circuit. This is especially true if the buffer is used within the feedback loop of an opamp.

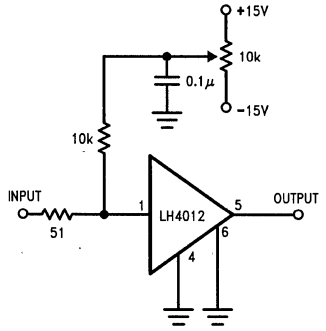
Application Information (Continued)

Output Short Circuit Protection Using a Series Resistor



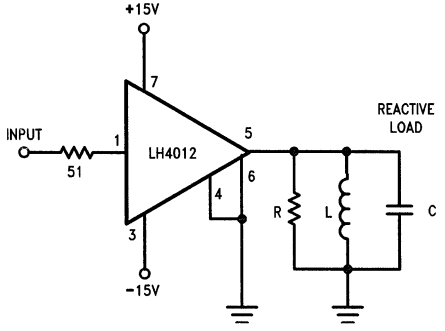
TL/K/9720-6

Offset Adjust



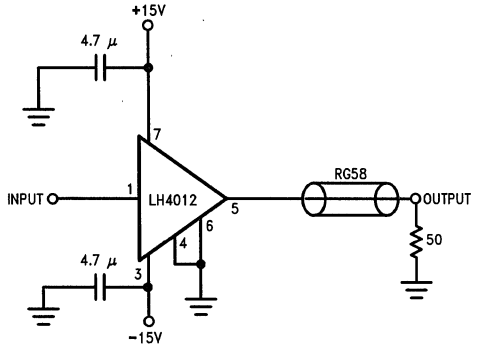
TL/K/9720-7

Isolation Buffer



TL/K/9720-8

Coaxial Cable Driver



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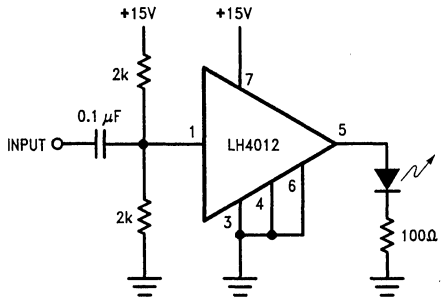
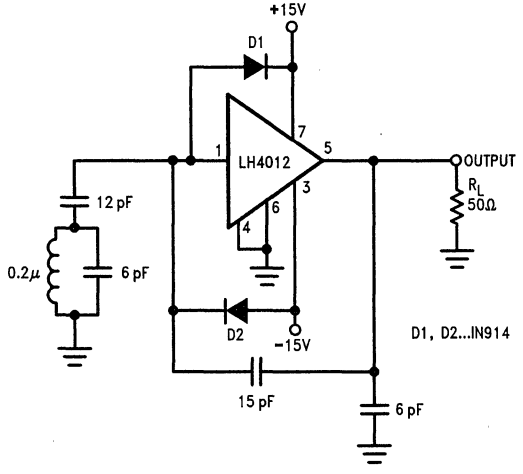
Application Information (Continued)

Laser Diode Transmitter



TL/K/9720–12

VHF Power Oscillator 100 MHz 1W



TL/K/9720–11

National Semiconductor

LH4033C/LH4063C Fast and Ultra Fast Buffer Amplifiers

General Description

The LH4033C and LH4063C are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH4033C will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500 V/μs. The LH4063C will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates of up to 6000 V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffer for driving reactive loads and high impedance input buffers for high speed ADCs and comparators. In addition, the LH4063C can continuously drive 50Ω coaxial cables or be used as a diddle yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH4033C and LH4063C are specified from −25°C to +85°C. The LH4033C is available in a 16-pin plastic DIP. The LH4063C is available in an 11-lead TO-220 package.

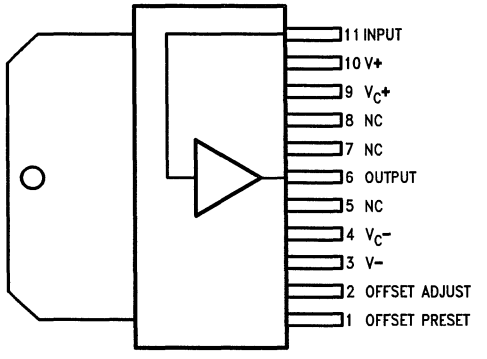
Features

- Fast (LH4063) 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth DC to 100 MHz
- High output drive ±10V with 50Ω load
- Low phase non-linearity 2°
- Fast rise times 2 ns
- High current gain 120 dB
- High input resistance $10^{10}\Omega$

Applications

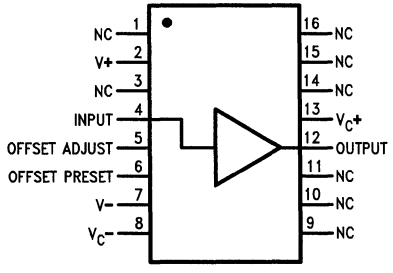
- High speed ATE
- Coaxial cable driver
- Isolation buffer
- High speed S/H amplifier
- High frequency filter
- Flash A/D buffer

Connection Diagrams



TL/K/10008-1

11-Lead TO-220
Order Number LH4063CT
See NS Package Number TA11A



TL/K/10008-2

16-Lead Molded Dual-In-Line Package
Order Number LH4033CN
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) 40V

Maximum Power Dissipation (See Curves)
- LH4063C 5W
- LH4033C 1.5W

Maximum Junction Temperature 175°C

Input Voltage $\pm V_S$

Continuous Output Current
- LH4063C ±250 mA
- LH4033C ±100 mA

Peak Output Current
- LH4063C ±500 mA
- LH4033C ±250 mA

Operating Temperature Range
- LH4033C and LH4063C −25°C to +85°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	Limits LH4033C Min	Limits LH4033C Typ	Limits LH4033C Max	Units
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ $R_S = 100\Omega$ (Note 2)		12	20 25	mV mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$ $T_J = 25°C$ (Note 2) $T_A = 25°C$ (Note 4) $T_J = T_A = T_{MAX}$			500 5.0 20	pA nA nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0\ k\Omega$	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$ $V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±12 ±9.0			V V
Supply Current	$V_{IN} = 0V$ (Note 5), No Load		21	24	mA
Power Consumption	$V_{IN} = 0V$ (No Load)		630	720	mW

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ k\Omega$ (Note 6)

Parameter	Conditions	Limits LH4033C Min	Limits LH4033C Typ	Limits LH4033C Max	Units
Slew Rate	$V_{IN} = \pm 10V$	1000	1400		V/µs
Bandwidth	$V_{IN} = 1.0\ V_{rms}$		100		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1		%

Note 1: LH4033C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.

Note 3: LH4033C is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{max}.

Note 4: Measured in still air 7 minutes after application of Power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	Limits			Units
		LH4063C			
		Min	Typ	Max	
Output Offset Voltage	$R_S \leq 100\ k\Omega$, $T_J = 25°C$ $R_L = 100\Omega$ (Note 2)		10	50 100	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$		300		$\mu V/°C$
Input Bias Current	$T_J = 25°C$ (Note 2)		10	30 100	nA nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S = 100\ k\Omega$, $R_L = 1.0\ k\Omega$	0.94	0.96	1.0	V/V
	$V_{IN} = \pm 10V$, $R_S = 100\ k\Omega$, $R_L = 50\Omega$, $T_J = 25°C$	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\ k\Omega$ $R_L = 50\Omega$		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	0.2	0.25		Amps
Output Voltage Swing	$R_L = 50\Omega$	± 10	± 13		V
	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.09	7.0		V_{P-P}
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$ (Note 3)		35	65	mA
	$V_S = \pm 5.0V$ (Note 3)		50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95	W
	$V_S = \pm 5.0V$		500		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_L = 50\Omega$ (Note 4), $R_S = 50\Omega$

Parameter	Conditions	Limits			Units
		LH4063C			
		Min	Typ	Max	
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000		$V/\mu s$
	$V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		$V/\mu s$
Bandwidth	$V_{IN} = 1.0\ V_{rms}$		200		MHz
Phase Non-Linearity	BW = 1.0 to 20 MHz		2.0		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		2.1		ns
Harmonic Distortion			<0.1		%

Note 1: LH4063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

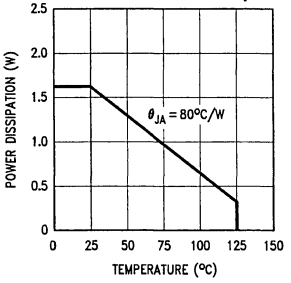
Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 3: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

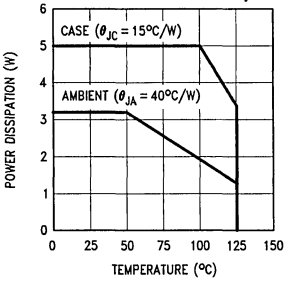
Note 4: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

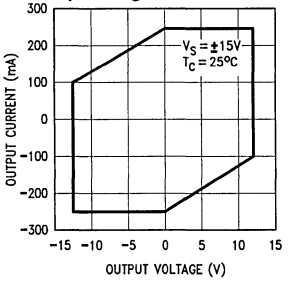
LH4033C Power Dissipation



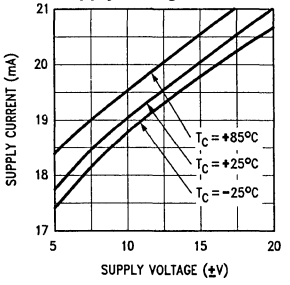
LH4063C Power Dissipation



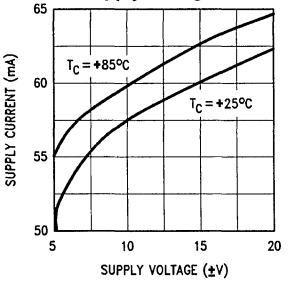
LH4063C DC Safe Operating Area



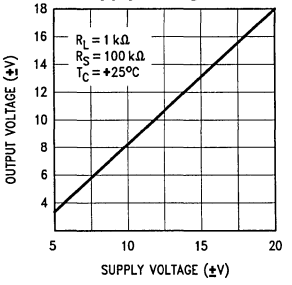
LH4033C Supply Current vs Supply Voltage



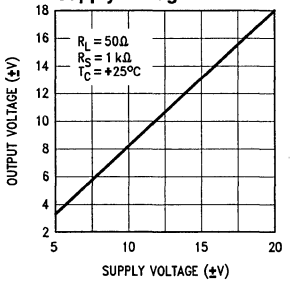
LH4063C Supply Current vs Supply Voltage



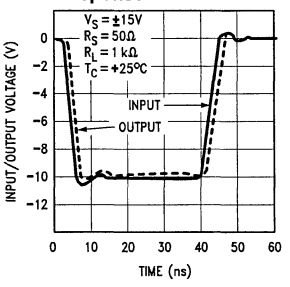
LH4033C Output Voltage vs Supply Voltage



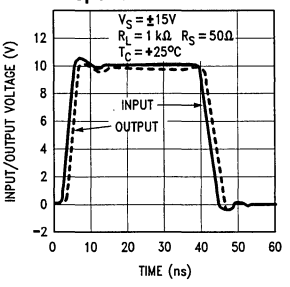
LH4063C Output Voltage vs Supply Voltage



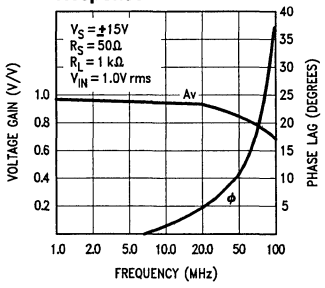
LH4033C Negative Pulse Response



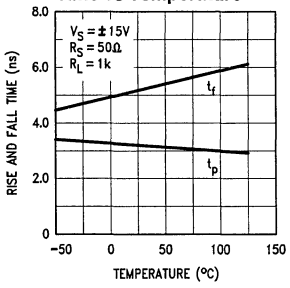
LH4033C Positive Pulse Response



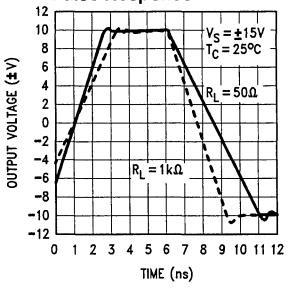
LH4033C Frequency Response



LH4033C Rise and Fall Time vs Temperature



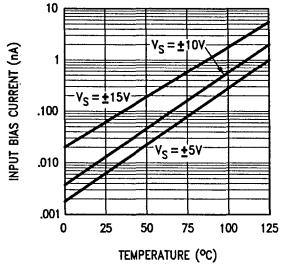
LH4063C Large Signal Pulse Response



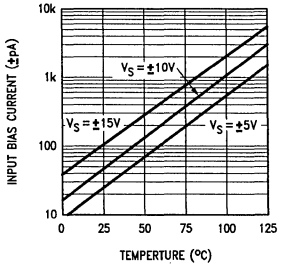
TL/K/10008–3

Typical Performance Characteristics (Continued)

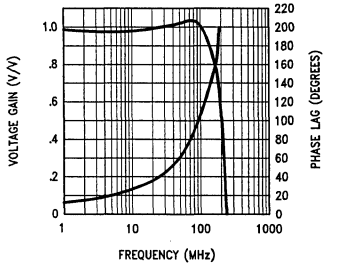
LH4033C Input Bias Current vs Temperature



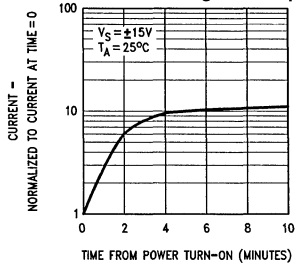
LH4063C Input Current vs Temperature



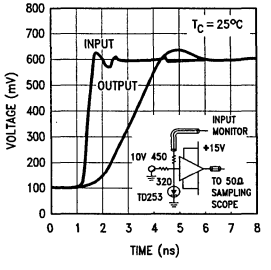
LH4063C Frequency Response



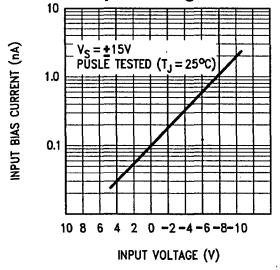
LH4033C Normalized Input Bias Current During Warm-Up



LH4063C Small Signal Rise Time



LH4033C Input Bias Current vs Input Voltage

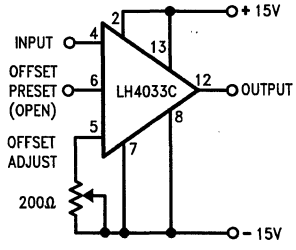


TL/K/10008–4

Application Hints

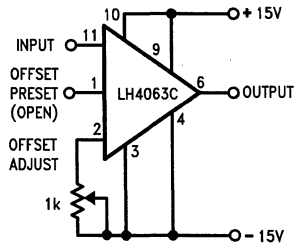
Recommended Layout Precautions: RF/video printed circuit board layout rules should be followed when using the LH4033C and LH4063C since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors.

Offset Voltage Adjustment: Both the LH4033C's and LH4063C's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 200Ω for the LH4033C or 1 kΩ for the LH4063C between the offset adjust pin and V^- as illustrated in *Figures 1* and *2*.



TL/K/10008–5

FIGURE 1. Offset Zero Adjust for LH4033C



TL/K/10008–6

FIGURE 2. Offset Zero Adjust for LH4063C

Application Hints (Continued)

Operation from Single or Asymmetrical Power Supplies: Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where:

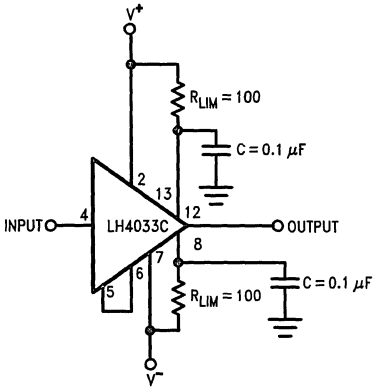
A_V = No load voltage gain, typically 0.99
V^+ = Positive supply voltage
V^- = Negative suply voltage

For the above example, ΔV_O would be -35 mV. This may be adjusted to zero by offset voltage adjustment described earlier. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection: In order to optimize transient response and output swing, output current limit has been omitted from the LH4033 and LH4063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3* and *4*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for LH4033C
$I_{SC} \leq 250$ mA for LH4063C



TL/K/10008–7

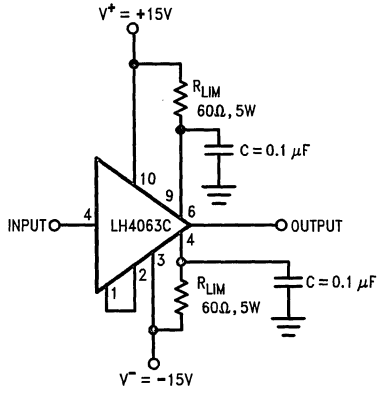
FIGURE 3. LH4033C Using Resistor Current Limiting

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5, 6* and *7*. In *Figures 5* and *6*, the current sources are saturated during normal operation thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload. For *Figure 5*:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

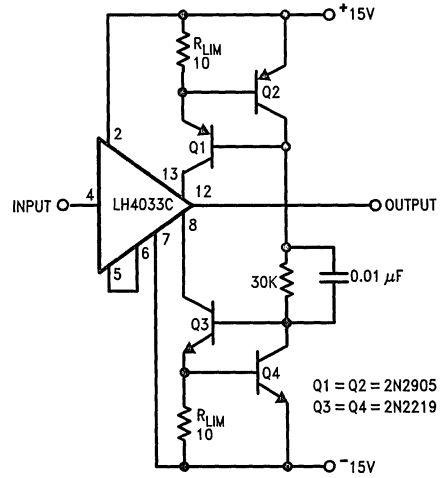
In *Figure 6*, quad transistor arrays are used to minimize part count and:

$$R_{LIM} = \frac{V_{BE}}{1/3\,(I_{SC})} = \frac{0.6V}{1/3\,(200\text{ mA})} = 8.2\Omega$$



TL/K/10008–8

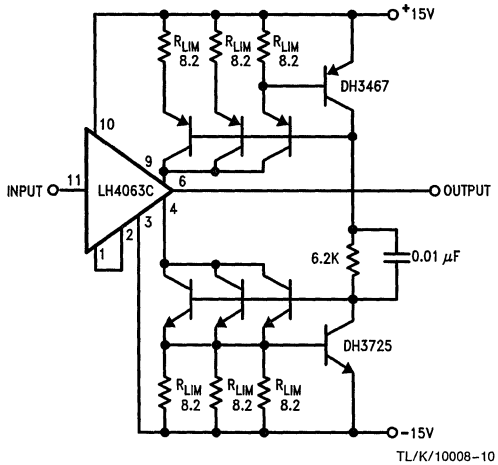
FIGURE 4. LH4063C Using Resistor Current Limiting



TL/K/10008–9

FIGURE 5. LH4033C Current Limiting Using Current Sources

Application Hints (Continued)



TL/K/10008–10

FIGURE 6. LH4063C Current Limiting Using Current Sources

Capacitance Loading: Both the LH4033C and LH4063C are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (CdV/dt) should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH4033C:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH4063C:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_{diss\ pkg} \geq P_{DC} + P_{AC}$$

$$\geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

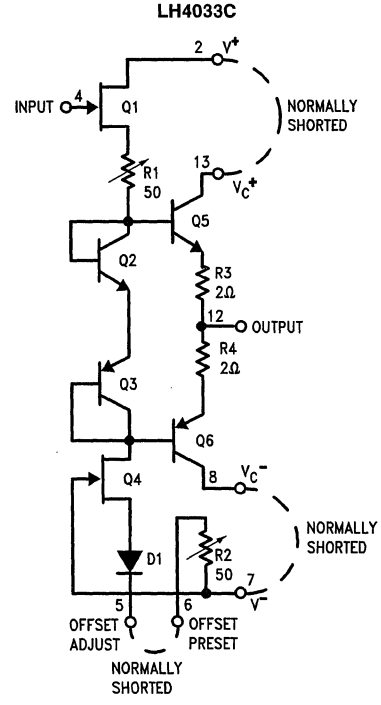
Operation Within an Op Amp Loop: Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH4033C. The wide bandwidths and high slew rates of the LH4033C and LH4063C assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Hardware: In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH4033C and LH4063C in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within <¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel for the LH4033C; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances. For the LH4063C, two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel will be necessary on each supply lead.

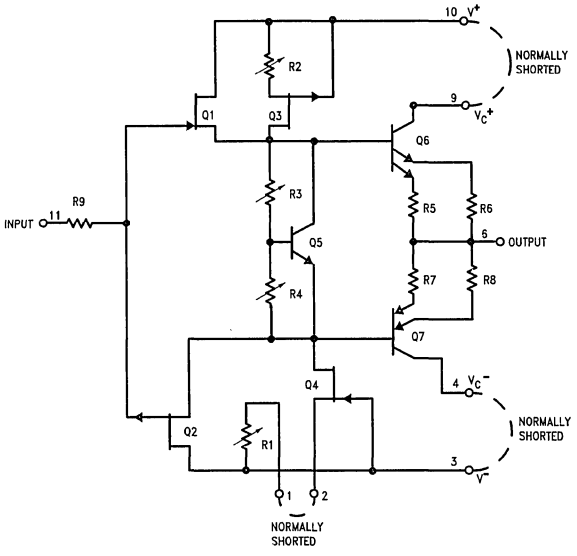
Schematic Diagrams



TL/K/10008–11

Schematic Diagrams (Continued)

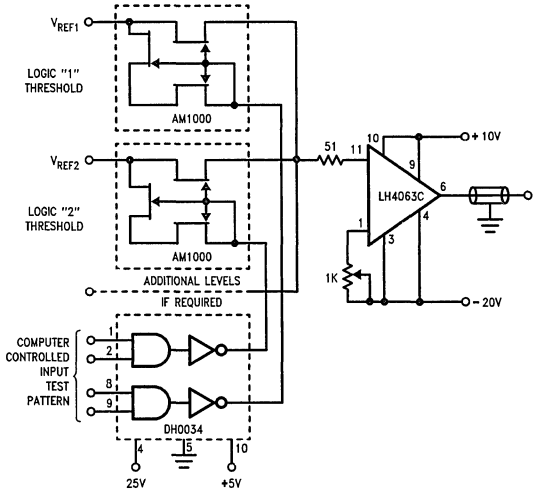
LH4063C



TL/K/10008–12

Typical Applications

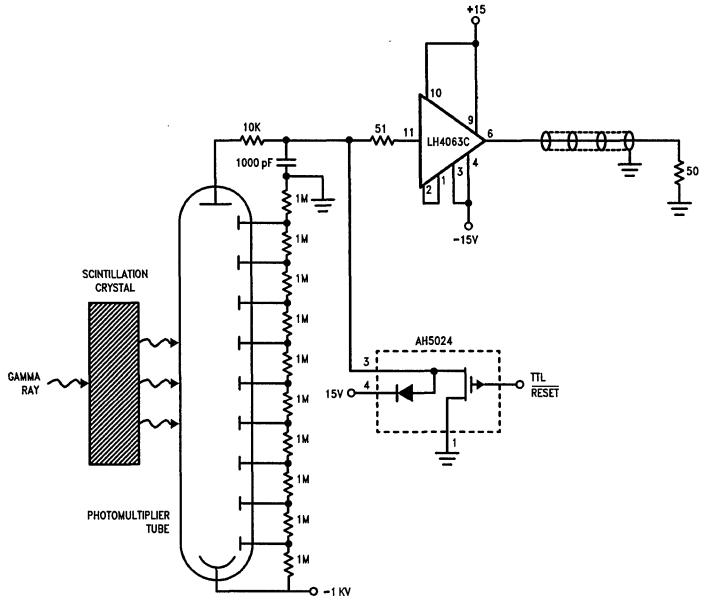
High Speed Automatic Test Equipment
Forcing Function Generator



TL/K/10008–13

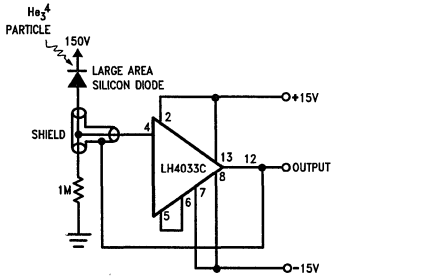
Typical Applications (Continued)

Gamma Ray Pulse Integrator



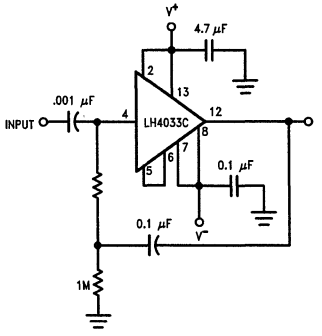
TL/K/10008–14

Nuclear Particle Detector



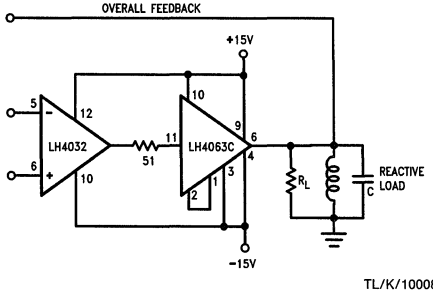
TL/K/10008–15

High Input Impedance AC Coupled Amplifier



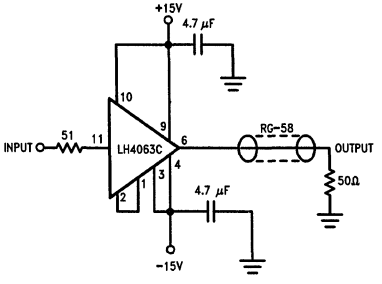
fH > 100 MHz TL/K/10008–16

Isolation Buffer



TL/K/10008–17

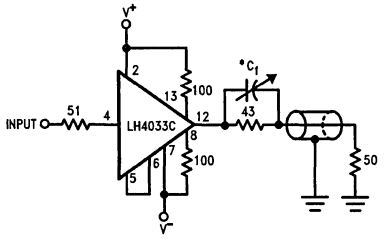
Coaxial Cable Driver



TL/K/10008–18

Typical Applications (Continued)

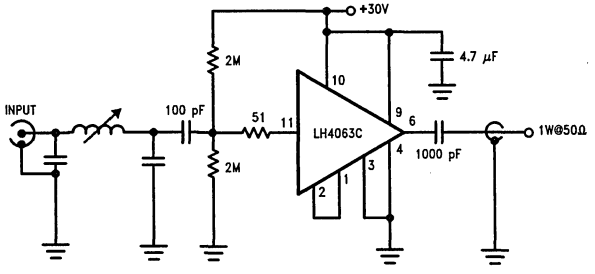
Coaxial Cable Driver



*Select C_1 For Optimum Pulse Response.

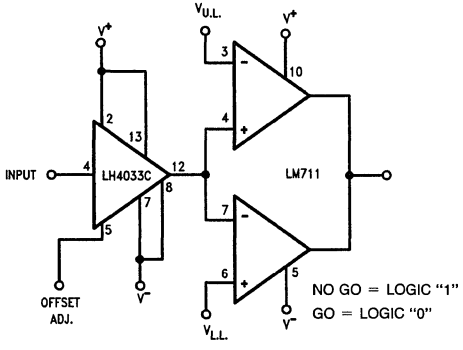
TL/K/10008–19

1W CW Final Amplifier



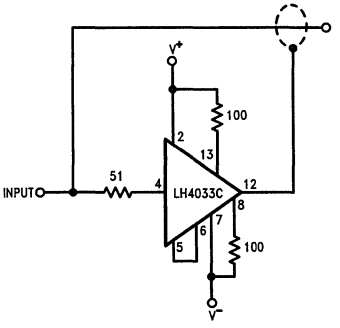
TL/K/10008–20

High Input Impedance Comparator With Offset Adjust



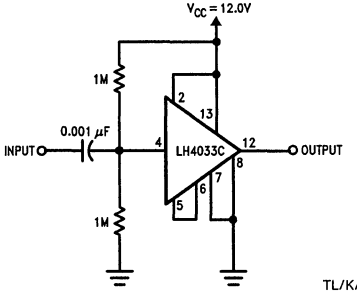
TL/K/10008–21

Instrumentation Shield/Line Driver



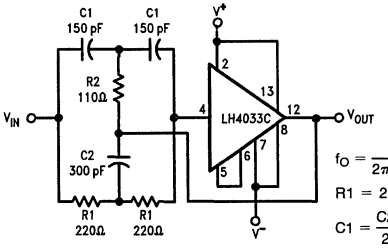
TL/K/10008–22

Single Supply AC Amplifier



TL/K/10008–23

4.5 MHz Notch Filter



$$f_O = \frac{1}{2\pi R1C1}$$

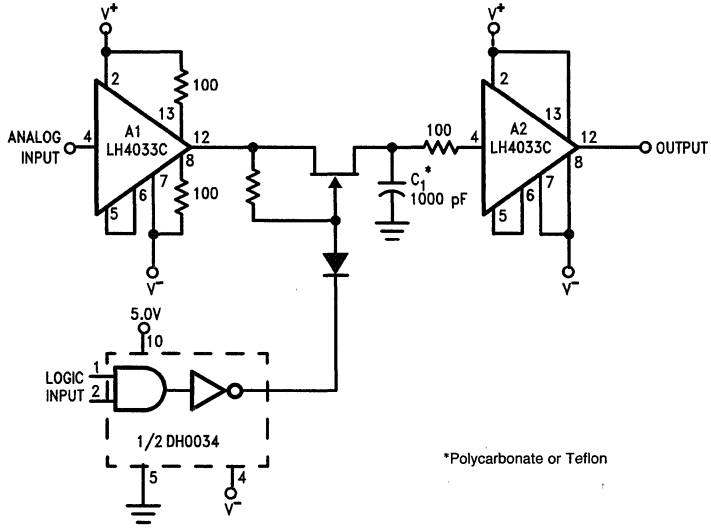
$$R1 = 2\,R2$$

$$C1 = \frac{C2}{2}$$

TL/K/10008–24

Typical Applications (Continued)

High Speed Sample & Hold



*Polycarbonate or Teflon

TL/K/10008–25

National Semiconductor

LM102/LM302 Voltage Followers

General Description

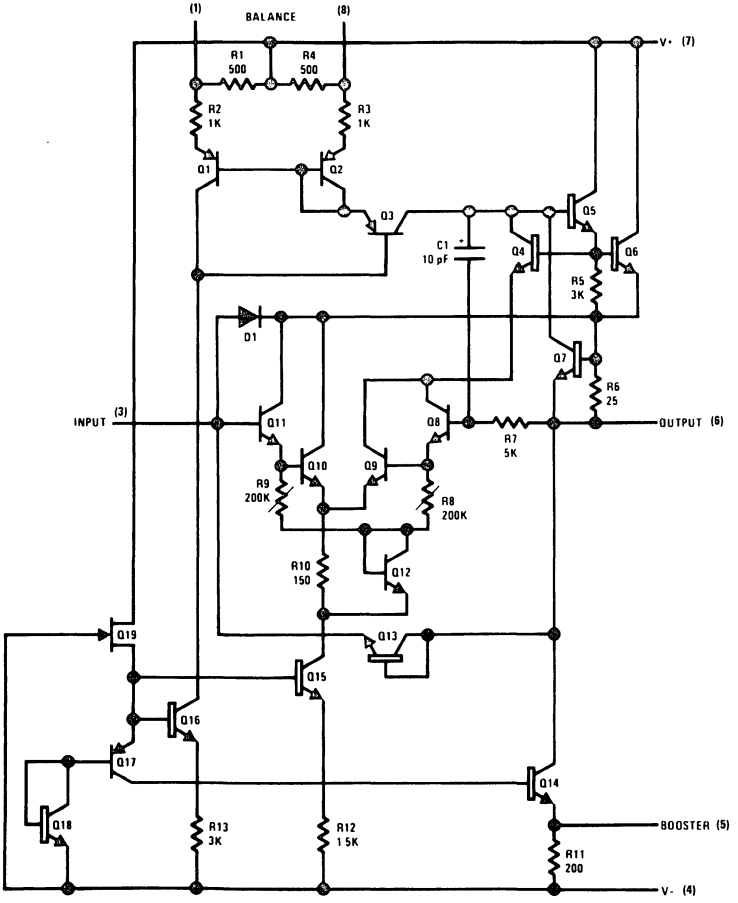
The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift.

The LM102, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response—all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

Features

- Fast slewing — 10V/μs
- Low input current — 10 nA (max)
- High input resistance — 10,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1K potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications

Schematic Diagram



TL/H/7753–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite

Operating Free Air Temperature Range	
LM102	−55°C to +125°C
LM302	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM102			LM302			Units
		Min	Typ	Max	Min	Type	Max	
Input Offset Voltage	$T_A = 25°C$		2	5		5	15	mV
Input Bias Current	$T_A = 25°C$		3	10		10	30	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^9	10^{12}		Ω
Input Capacitance				3.0		3.0		pF
Large Signal Voltage Gain	$T_A = 25°C$, V_S ±15V, V_{OUT} = ±10V, R_L = 8 kΩ	0.999	0.9996		0.9985	0.9995	1.0	V/V
Output Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5	Ω
Supply Current	$T_A = 25°C$		3.5	5.5		3.5	5.5	mA
Input Offset Voltage				7.5			20	mV
Offset Voltage Temperature Drift			6			20		μV/°C
Input Bias Current	$T_A = T_A$MAX $T_A = T_A$MIN		3 30	10 100		3.0 20	15 50	nA nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 10 kΩ	0.999						
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ (Note 5)	±10			±10			V
Supply Current	$T_A = 125°C$		2.6	4.0				mA
Supply Voltage Rejection Ratio	$±12V \le V_S \le ±15V$	60			60			dB

Note 1: The maximum junction temperature of the LM102 is 150°C, while that of the LM302 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: It is necessary to insert a resistor (at least 5k and preferably 10k) in series with the input pin when the amplifier is driven from low impedance sources to prevent damage when the output is shorted and to ensure stability.

Note 4: These specifications apply for $±12V \le V_S \le ±15V$ and $-55°C \le T_A \le 125°C$ for the LM102 and $0°C \le T_A \le 70°C$ for the LM302 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

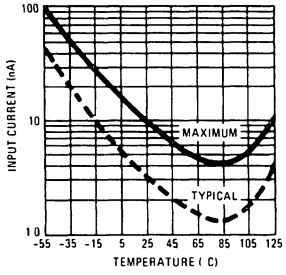
Note 6: Refer to RETS102X for the LM102H military specifications.

APPLICATION HINT

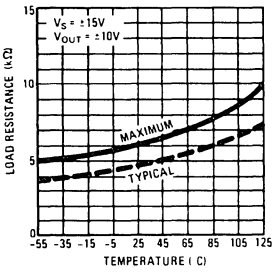
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ Min) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Guaranteed Performance Characteristics LM102

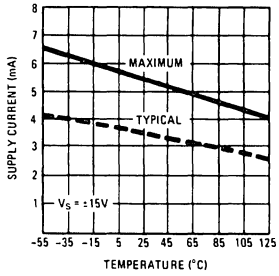
Input Current



Output Swing



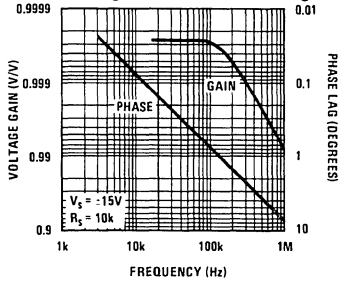
Supply Current



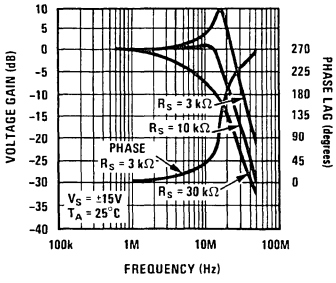
TL/H/7753–7

Typical Performance Characteristics LM102

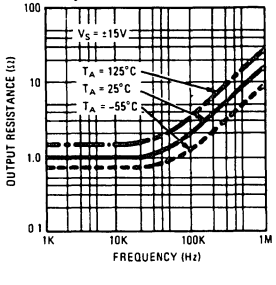
Voltage Gain and Phase Lag



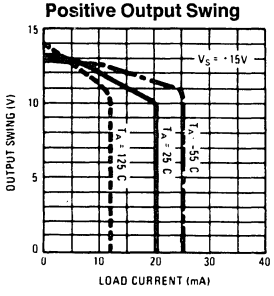
Voltage Gain and Phase Lag



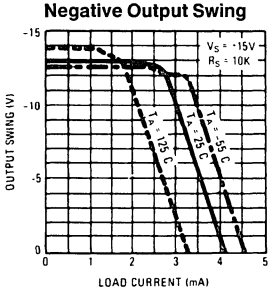
Output Resistance



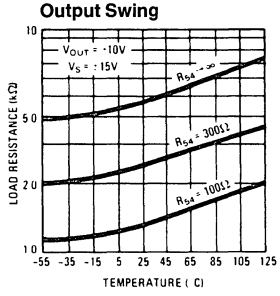
Positive Output Swing



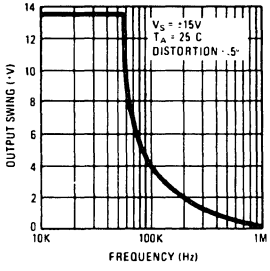
Negative Output Swing



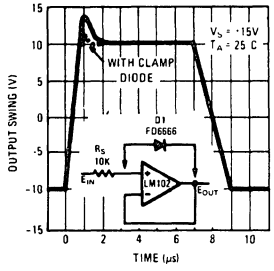
Output Swing



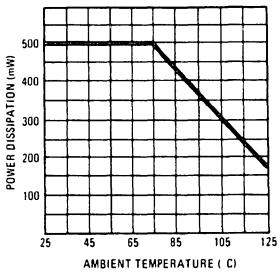
Large Signal Frequency Response



Large Signal Pulse Response

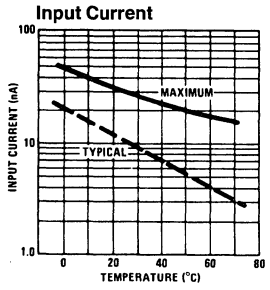


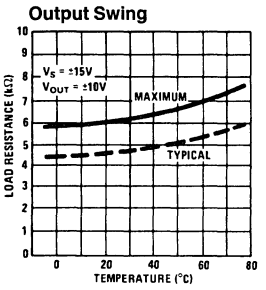
Maximum Power Dissipation

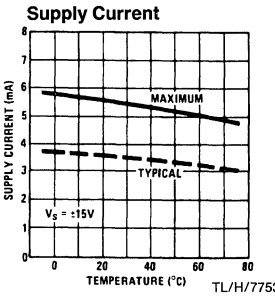


TL/H/7753–8

Guaranteed Performance Characteristics LM302

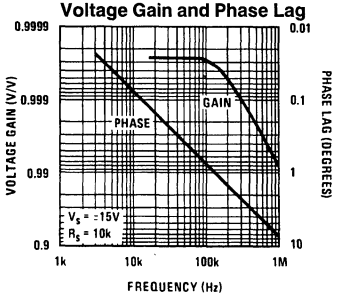


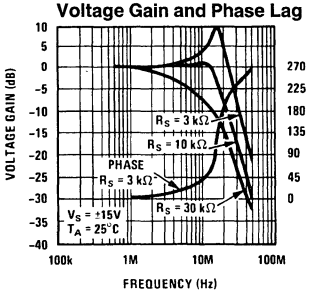


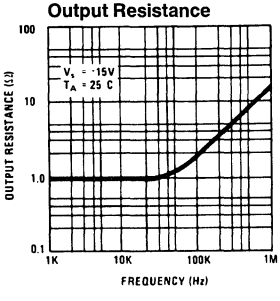


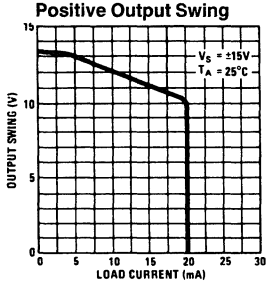
TL/H/7753–9

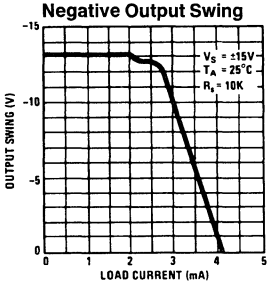
Typical Performance Characteristics LM302

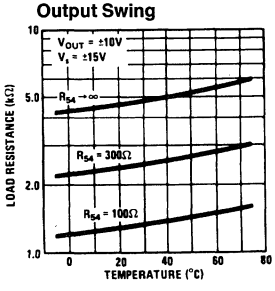


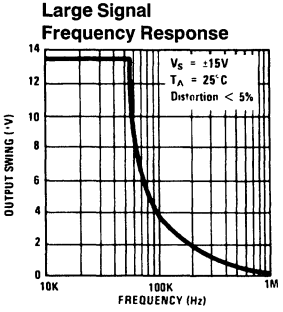


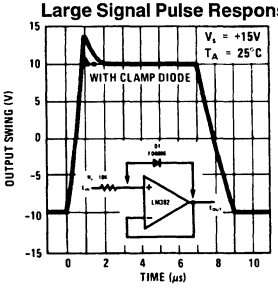


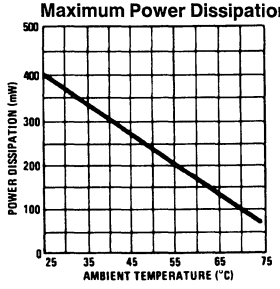








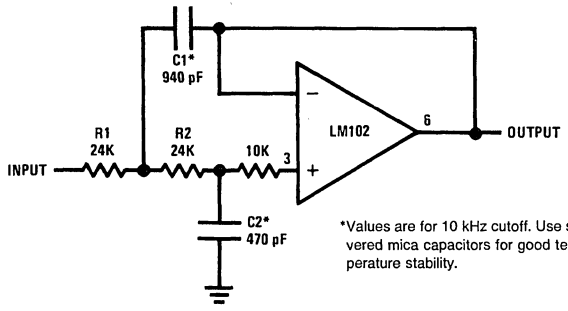




TL/H/7753–10

Typical Applications

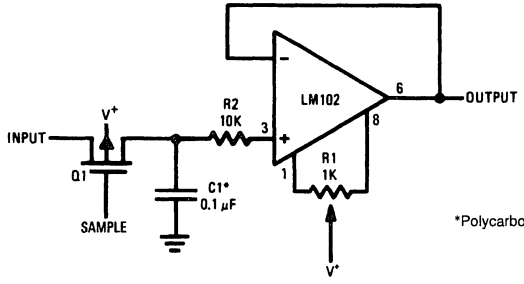
Low Pass Active Filter



*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

TL/H/7753–3

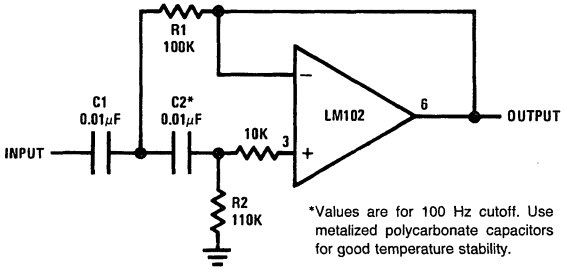
Sample and Hold with Offset Adjustment



*Polycarbonate-dielectric capacitor.

TL/H/7753–4

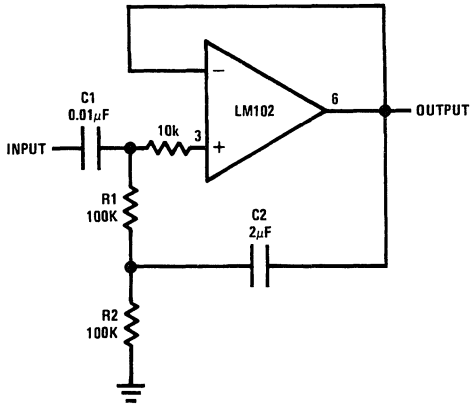
High Pass Active Filter



*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

TL/H/7753–5

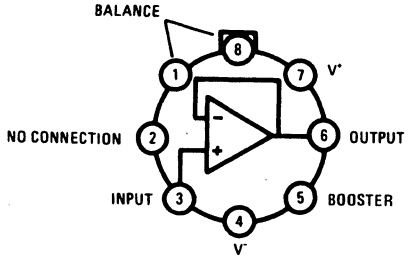
High Input Impedance AC Amplifier



TL/H/7753–6

Connection Diagram

Metal Can Package
Top View



TL/H/7753–2

Order Number LM102H or LM302H
See NS Package Number H08C

National Semiconductor

LM110/LM210/LM310 Voltage Follower

General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

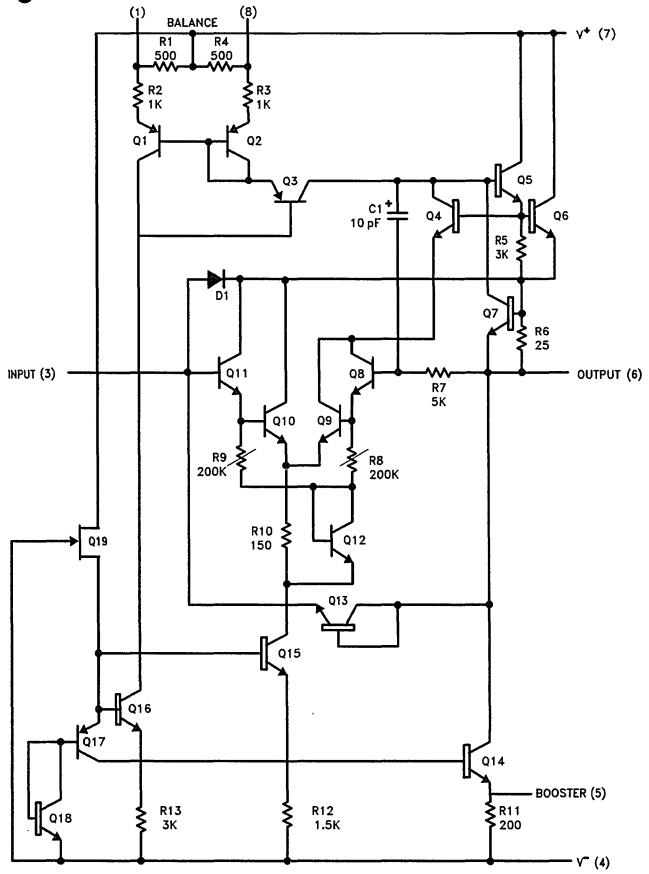
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55°C \leq T_A \leq +125°C$, the LM210 from $-25°C \leq T_A \leq +85°C$ and the LM310 from $0°C \leq T_A \leq +70°C$.

Features

■ Input current	10 nA max over temperature
■ Small signal bandwidth	20 MHz
■ Slew rate	30 V/μs
■ Supply voltage range	±5V to ±18V

Schematic Diagram



TL/H/7761–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM110	−55°C to +125°C
LM210	−25°C to +85°C
LM310	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM110			LM210			LM310			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L = 8\ k\Omega$	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift	$-55°C \le T_A \le +85°C$ $+85 \le T_A \le 125°C$ $0°C \le T_A \le +70°C$		6 12			6			 10		μV/°C μV/°C μV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L = 10\ k\Omega$	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 5)	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±10			±10			±10			V
Supply Current	$T_A = 125°C$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$\pm 5V \le V_S \le \pm 18V$	70	80		70	80		70	80		dB

Note 1: The maximum junction temperature of the LM110 is 150°C, of the LM210 is 100°C, and of the LM310 is 85°C. For operating at elevated temperatures, devices in the HO8 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 22°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to 125°C and ambient temperatures to 70°C, and for the LM310, 70°C case temperature or 55°C ambient temperature. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted. R_S = 5k min, 10k typical is recommended for dynamic stability in all applications.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 18V$ and $-55°C \le T_A$ 125°C for the LM110, $-25°C \le T_A \le 85°C$ for the LM210, and $0°C \le T_A \le 70°C$ for the LM310 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

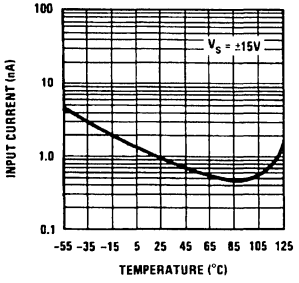
Note 6: Refer to RETS110X for LM110H, LM110J military specifications.

Application Hint

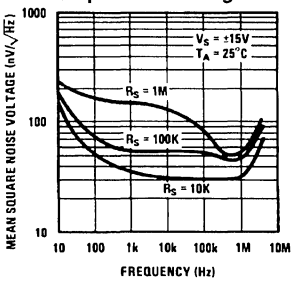
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ min.) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Typical Performance Characteristics (LM110/LM210)

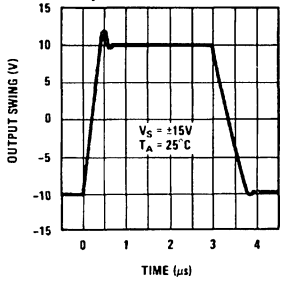
Input Current



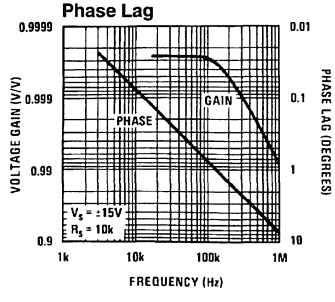
Output Noise Voltage



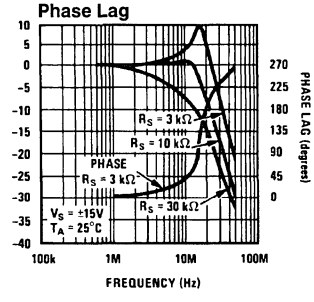
Large Signal Pulse Response



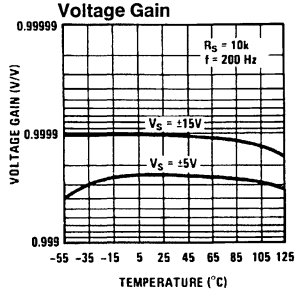
Voltage Gain and Phase Lag



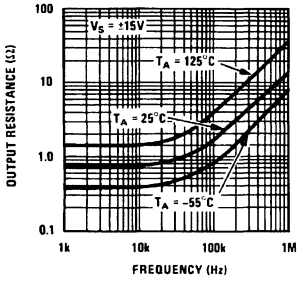
Voltage Gain and Phase Lag



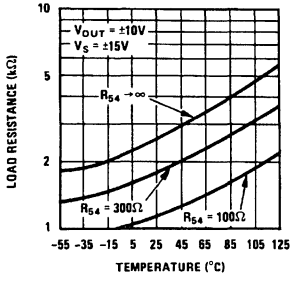
Voltage Gain



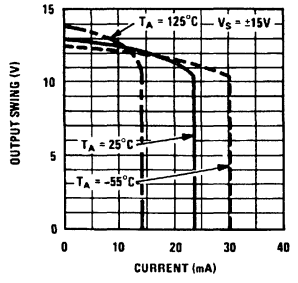
Output Resistance



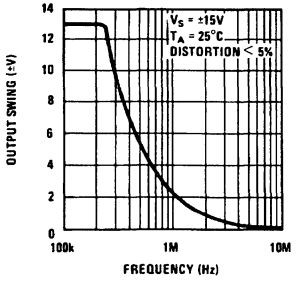
Symmetrical Output Swing



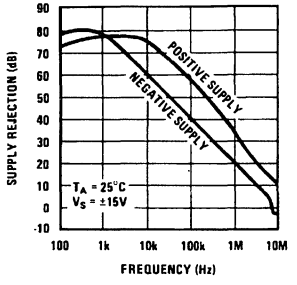
Positive Output Swing



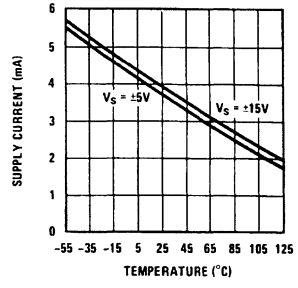
Large Signal Frequency Response



Power Supply Rejection



Supply Current

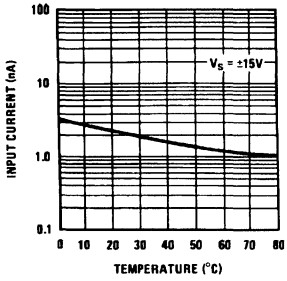


TL/H/7761–28

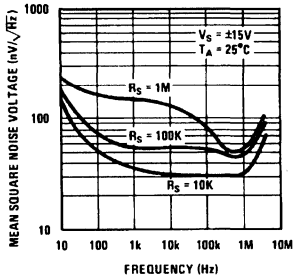
4

Typical Performance Characteristics (LM310)

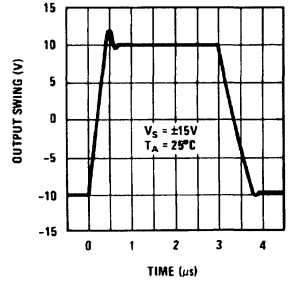
Input Current



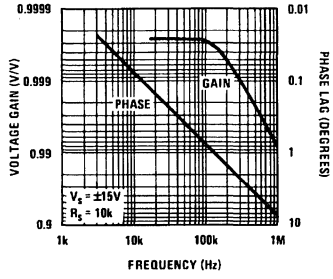
Output Noise Voltage



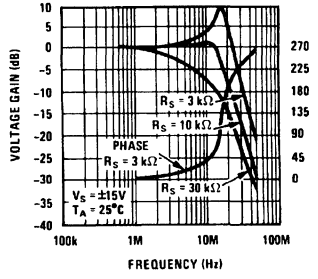
Large Signal Pulse Response



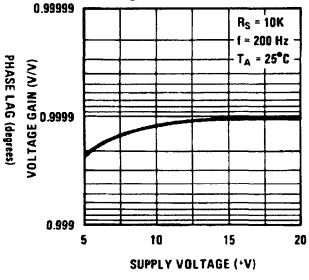
Voltage Gain and Phase Lag



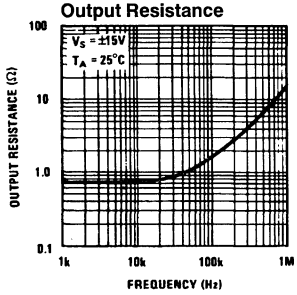
Voltage Gain and Phase Lag



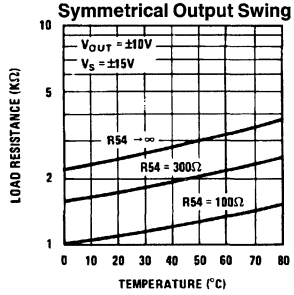
Voltage Gain



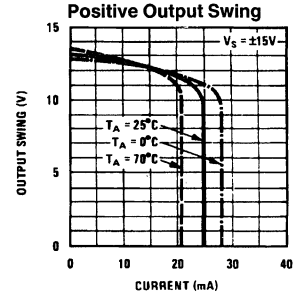
Output Resistance



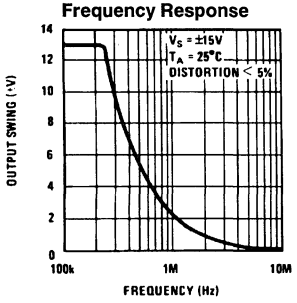
Symmetrical Output Swing



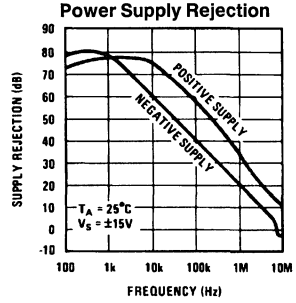
Positive Output Swing



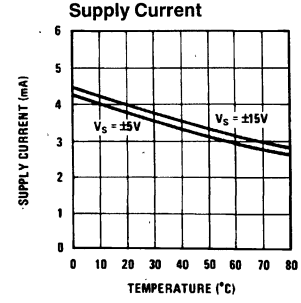
Large Signal Frequency Response



Power Supply Rejection



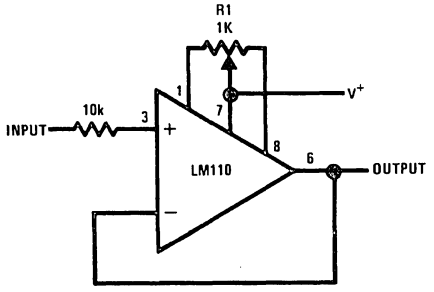
Supply Current



TL/H/7761–29

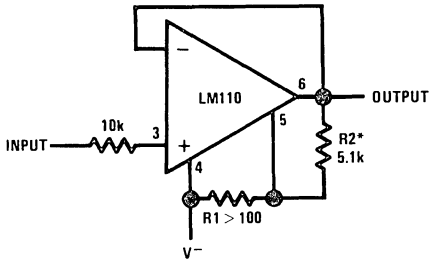
Auxiliary Circuits

Offset Balancing Circuit



TL/H/7761-2

Increasing Negative Swing Under Load

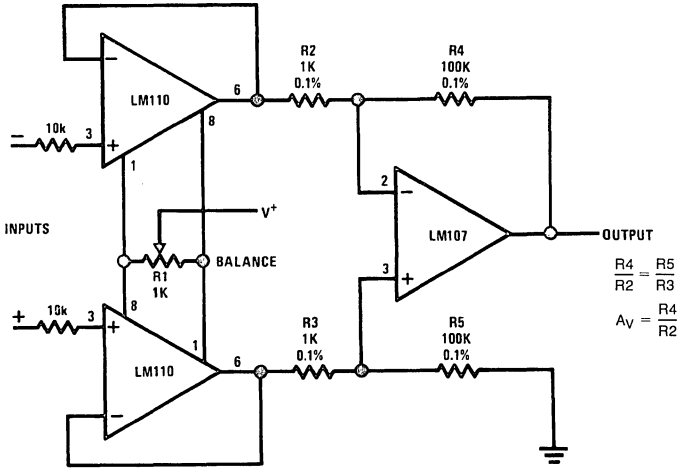


TL/H/7761-3

*May be added to reduce internal dissipation

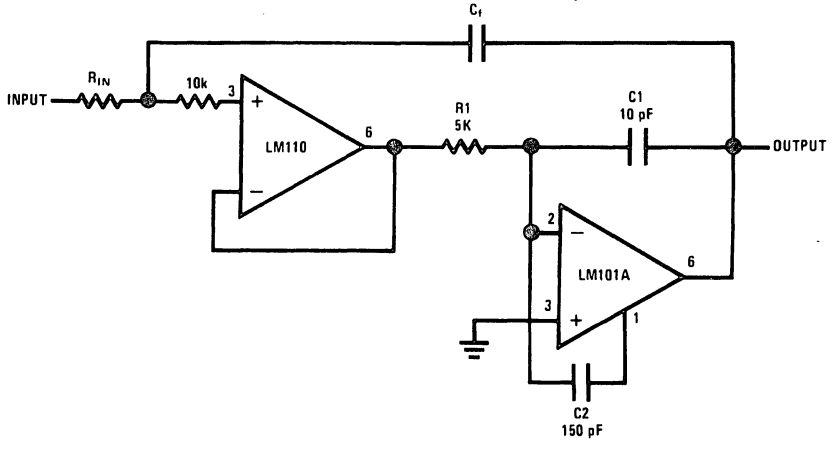
Typical Applications

Differential Input Instrumentation Amplifier



TL/H/7761-4

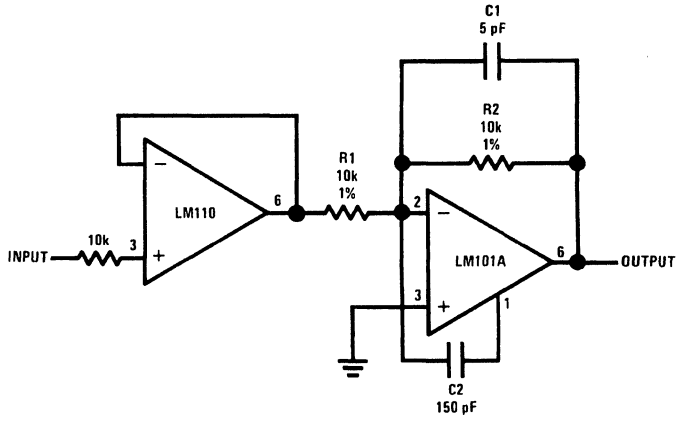
Fast Integrator with Low Input Current



TL/H/7761-5

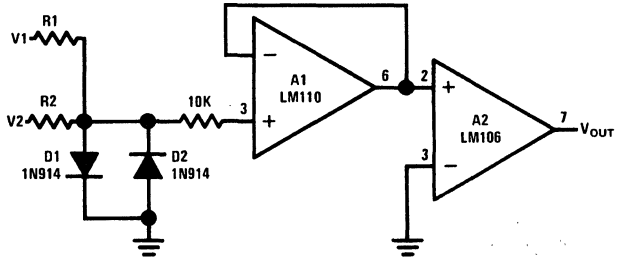
Typical Applications (Continued)

Fast Inverting Amplifier with High Input Impedance



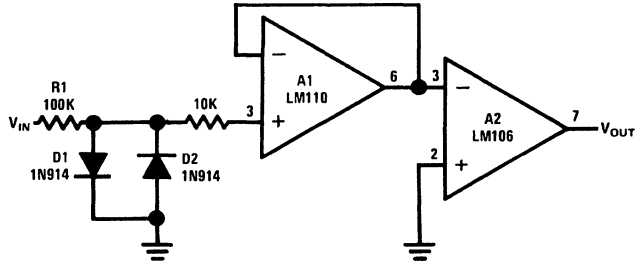
TL/H/7761–6

Comparator for Signals of Opposite Polarity



TL/H/7761–7

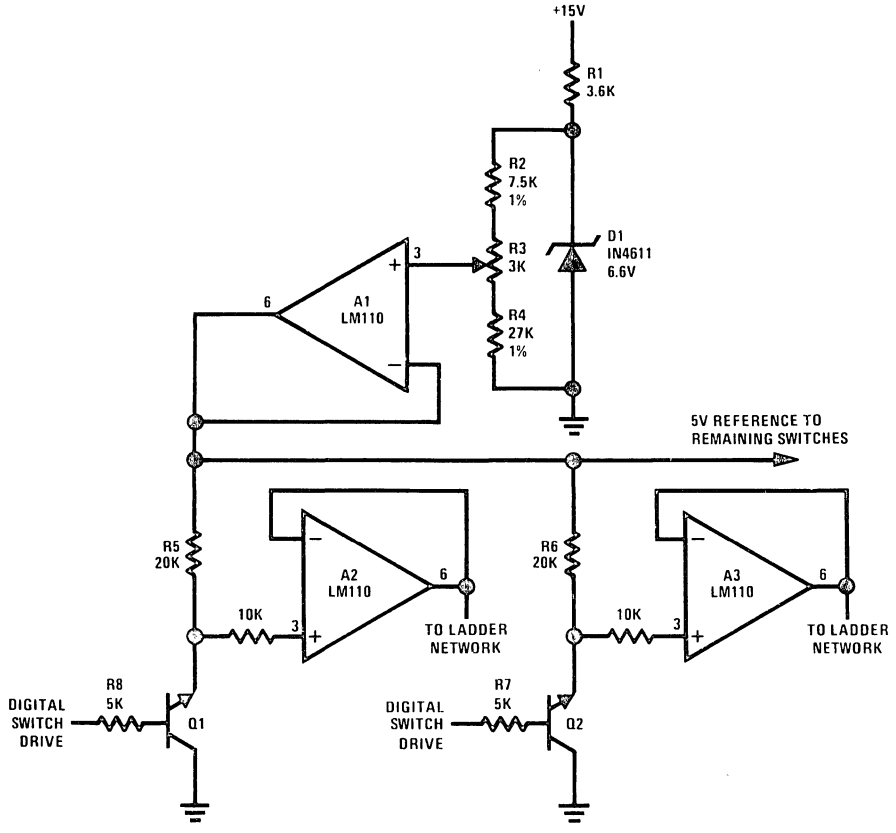
Zero Crossing Detector



TL/H/7761–9

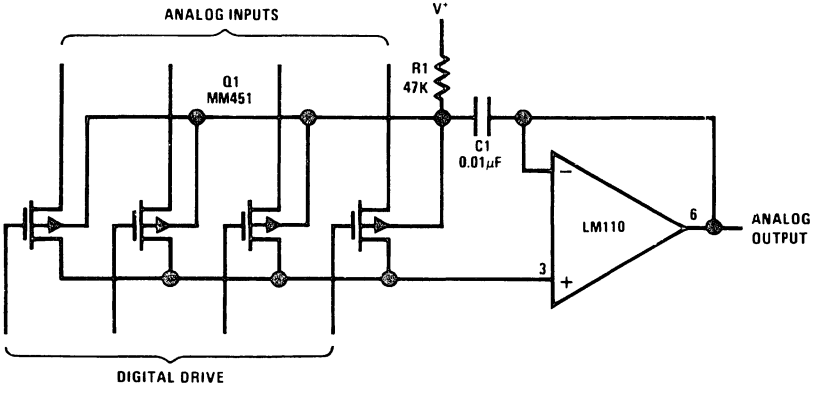
Typical Applications (Continued)

Driver for A/D Ladder Network



TL/H/7761–8

Buffer for Analog Switch*

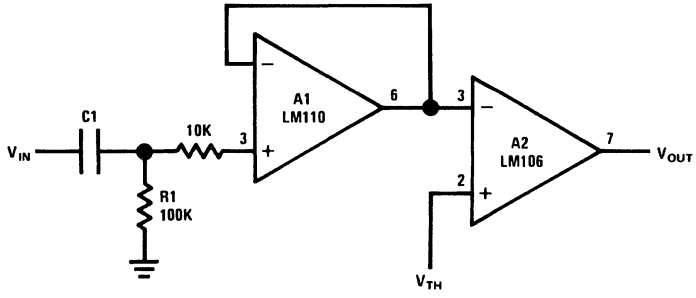


TL/H/7761–10

*Switch substrates are boot-strapped to reduce output capacitance of switch.

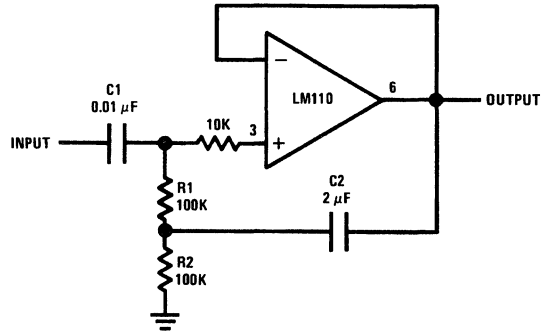
Typical Applications (Continued)

Comparator for AC Coupled Signals



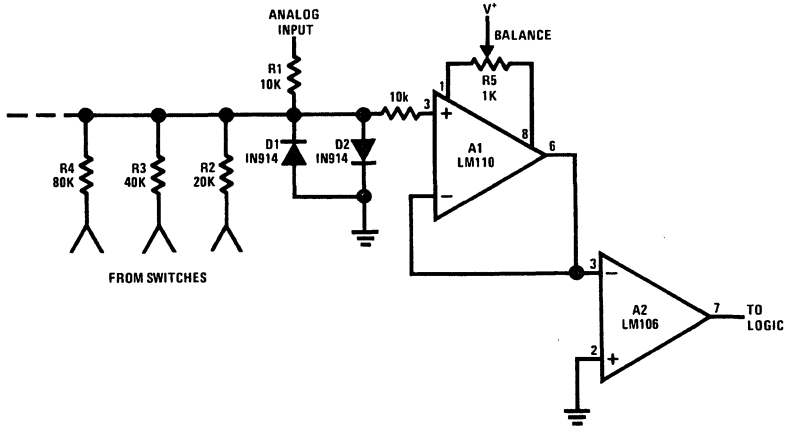
TL/H/7761–11

High Input Impedance AC Amplifier



TL/H/7761–12

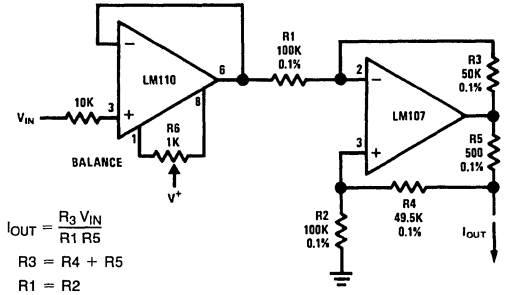
Comparator for A/D Converter Using a Binary-Weighted Network



TL/H/7761–13

Typical Applications (Continued)

Bilateral Current Source



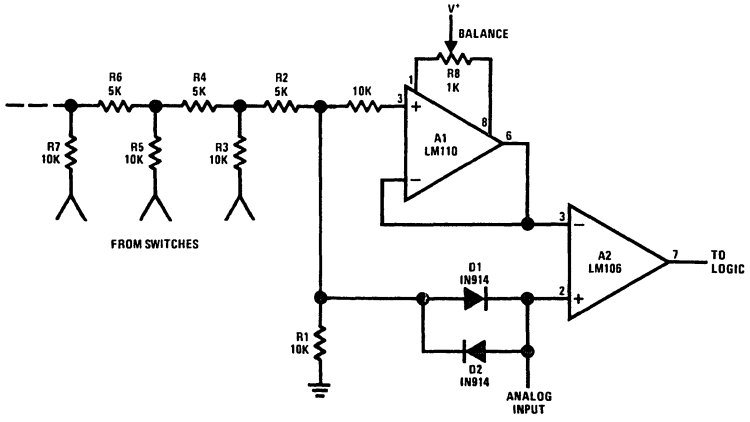
$$I_{OUT} = \frac{R_3 V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

$R1 = R2$

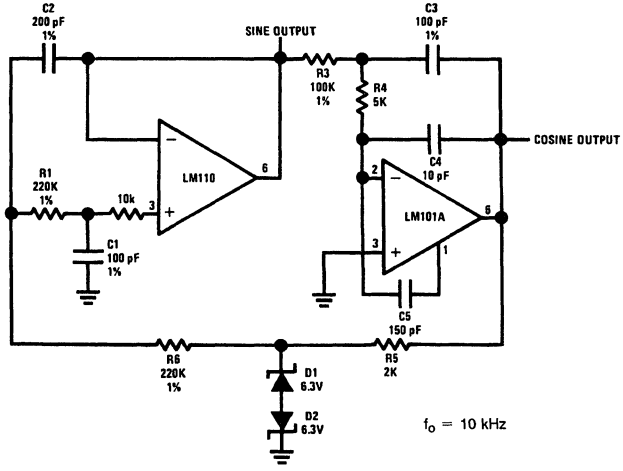
TL/H/7761–14

Comparator for A/D Converter Using a Ladder Network



TL/H/7761–15

Sine Wave Oscillator

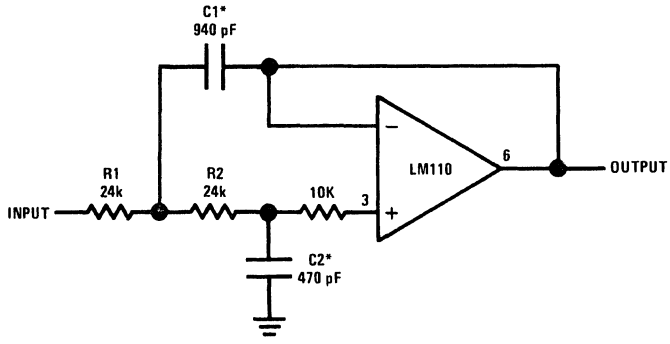


f_o = 10 kHz

TL/H/7761–16

Typical Applications (Continued)

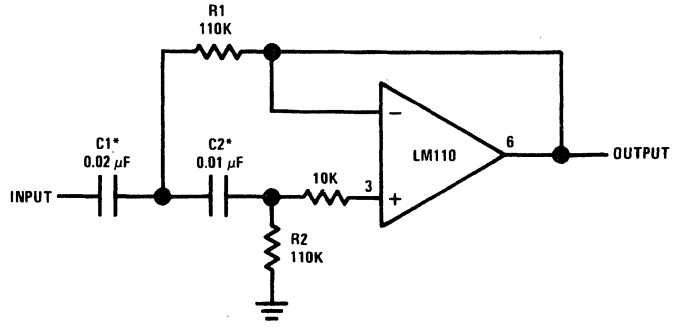
Low Pass Active Filter



TL/H/7761–18

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

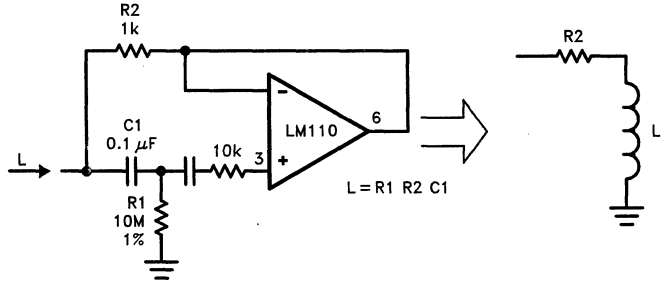
High Pass Active Filter



TL/H/7761–19

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

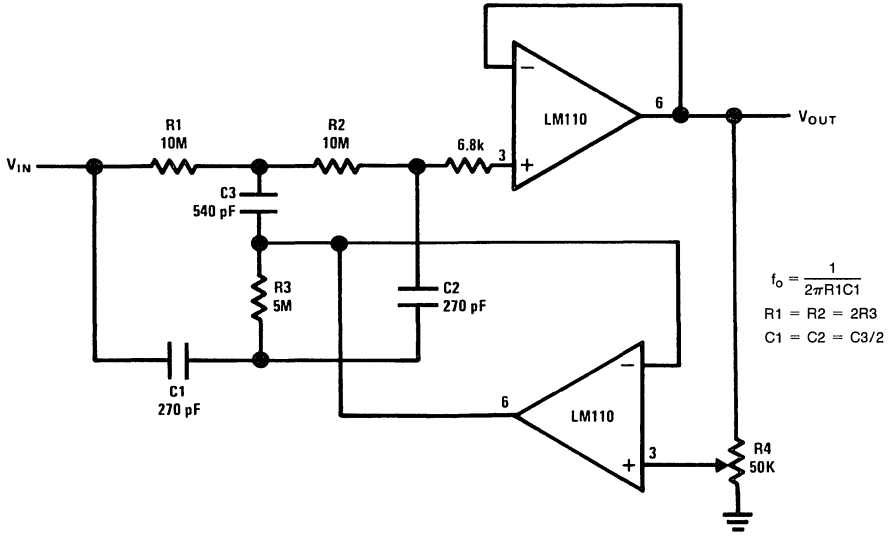
Simulated Inductor



TL/H/7761–21

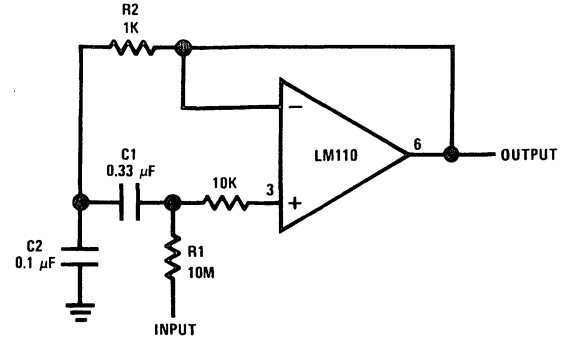
Typical Applications (Continued)

Adjustable Q Notch Filter



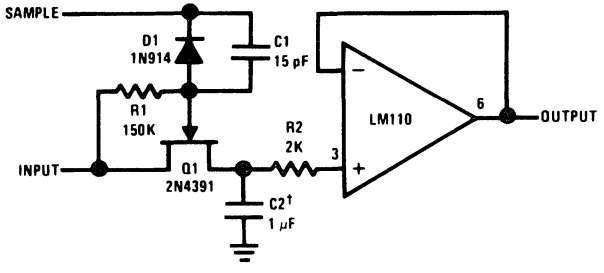
TL/H/7761–22

Bandpass Filter



TL/H/7761–23

Sample and Hold

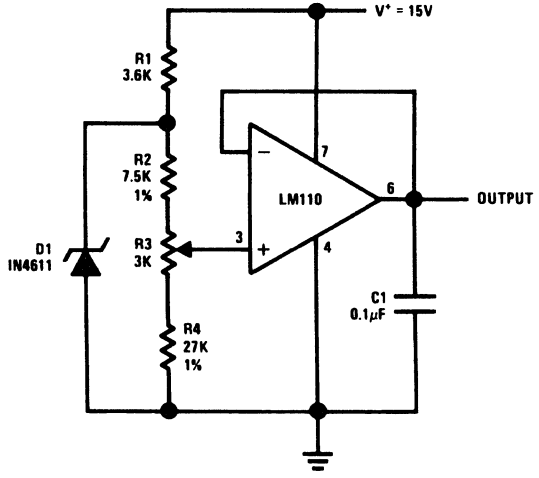


TL/H/7761–24

†Use capacitor with polycarbonate teflon or polythylene dietetric

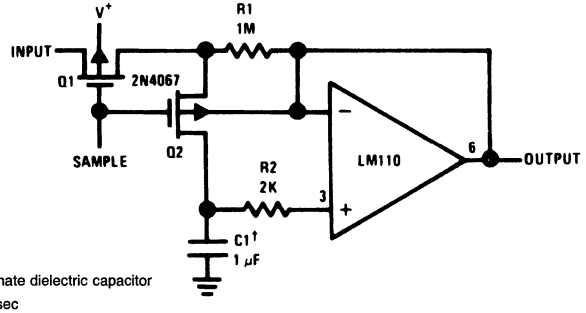
Typical Applications (Continued)

Buffered Reference Source



TL/H/7761–25

Low Drift Sample and Hold*



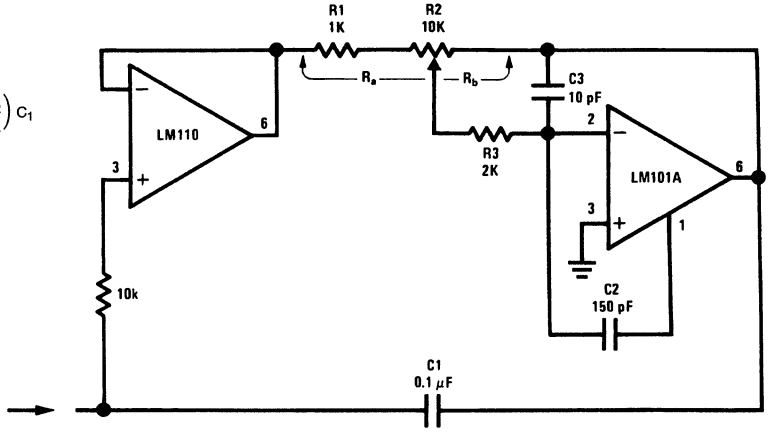
†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV/sec

TL/H/7761–26

Variable Capacitance Multiplier

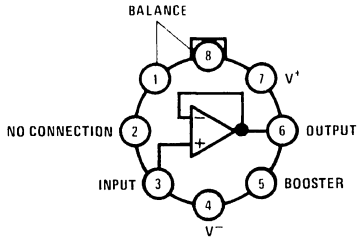
$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$



TL/H/7761–27

Connection Diagrams

Metal Can Package



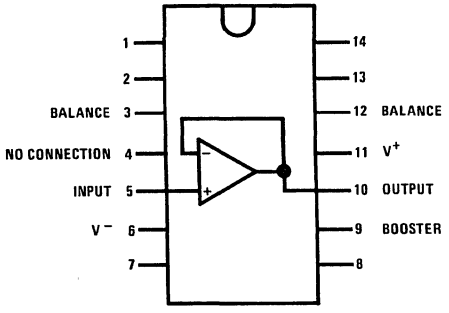
TL/H/7761–30

Package is connected to Pin 4 (V^-)

Top View

Order Number LM110H, LM210H or LM310H
See NS Package Number H08C

Dual-In-Line Package

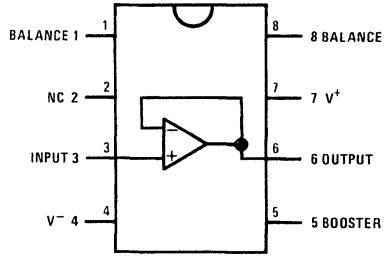


TL/H/7761–31

Top View

Order Number LM110J, LM210J or LM310J
See NS Package Number J14A

Dual-In-Line Package



TL/H/7761–32

Top View

Order Number LM310M or LM310N
See NS Package Number M08A or N08E

National Semiconductor

LM6121/LM6221/LM6321 High Speed Buffer

General Description

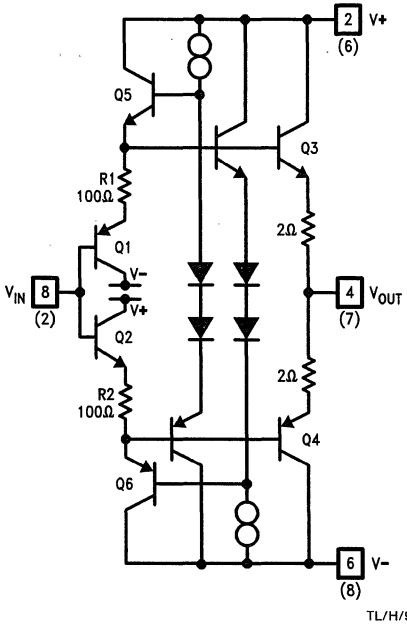
These high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

- High slew rate — 800 V/μs
- Wide bandwidth — 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current — ±300 mA
- High input impedance — 5 MΩ
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to ±15V operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

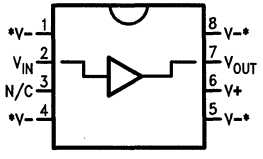
Simplified Schematic



TL/H/9223–1

Numbers in ( ) are for 8-pin N DIP.

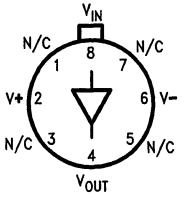
Pin Configurations



TL/H/9223–2

*Heat-sinking pins.

Order Number LM6221N or LM6321N
See NS Package Number N08E



TL/H/9223–3

Top View

Note: Pin 6 connected to case.

Order Number LM6121H or LM6221H
See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 10)	±2000V

	Package H	Package N
θ_{JA} (Note 4)	150°C/W	47°C/W
Maximum Junction Temp. (T_j)	150°C	150°C
Operating Temperature Range		
LM6121	−55°C to +125°C	
LM6221	−40°C to +85°C	
LM6321	0°C to +70°C	
Operating Supply Range	4.75 to ±16V	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6121 Tested Limit (Note 6)	LM6121 Design Limit (Note 7)	LM6221 Tested Limit (Note 6)	LM6221 Design Limit (Note 7)	LM6321 Tested Limit (Note 6)	LM6321 Design Limit (Note 7)	Units
A_{V1}	Voltage Gain 1	R_L = 1k, V_{IN} = ±10V	0.990	0.980 **0.970**		0.980	**0.950**	0.970	**0.950**	
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860 **0.800**		0.860	**0.820**	0.850	**0.820**	V/V Min
A_{V3}	Voltage Gain 3 (Note 8)	R_L = 50Ω V_{IN} = 2 V_{pp} V^+ = 5V **(1.5 V_{pp})**	0.840	0.780 **0.750**		0.780	**0.700**	0.750	**0.700**	
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30 **50**		30	**60**	50	**100**	mV Max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	4 **7**		4	**7**	5	**7**	μA Max
R_{IN}	Input Resistance	R_L = 50Ω	5							MΩ
C_{IN}	Input Capacitance		3.5							pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5 **10**		5	**10**	5	**6**	Ω Max
I_{S1}	Supply Current 1	R_L = ∞	15	18 **20**		18	**20**	20	**22**	mA Max
I_{S2}	Supply Current 2	R_L = ∞, V^+ = 5V	14	16 **18**		16	**18**	18	**20**	
V_{O1}	Output Swing 1	R_L = 1k	13.5	13.3 **13**		13.3	**13**	13.2	**13**	
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5 **10**		11.5	**10**	11	**10**	±V Min
V_{O3}	Output Swing 3	R_L = 50Ω	12	11 **9**		11	**9**	10	**9**	
V_{O4}	Output Swing 4	R_L = 50Ω V^+ = 5V (Note 8)	1.8	1.6 **1.3**		1.6	**1.4**	1.6	**1.5**	V_{pp} Min
PSSR	Power Supply Rejection Ratio	$V^{\pm}$ = ±5V to ±15V	70	60 **55**		60	**50**	60	**50**	dB Min

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6121		LM6221		LM6321		Units
				Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
SR_1	Slew Rate 1	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$	1200							
SR_2	Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 9)	800	550		550		550		V/μs Min
SR_3	Slew Rate 3	$V_{IN} = 2\ V_{pp}$, $R_L = 50\Omega$, $V^+ = 5V$ (Note 8)	50							
BW	−3 dB Bandwidth	$V_{IN} = \pm 100\ mV_{pp}$, $R_L = 50\Omega$, $C_L \leq 10\ pF$	50	30		30		30		MHz Min
t_r, t_f	Rise Time, Fall Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	7.0							ns
t_{pd}	Propagation Delay Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	4.0							ns
	Overshoot	$R_L = 50\Omega$, $C_L \leq 10\ pF$, $V_O = 100\ mV_{pp}$	10							%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, with $T_J = T_A + \theta_{JA}PD$. θ_{JC} for the LM6121H and LM6221H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 47°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 84°C/W.

Note 5: $R_S = 50\Omega$, $V_S = \pm 15V$, unless otherwise specified. **Boldface** numbers apply over the operating temperature range. Numbers in standard typeface apply at $T_A = 25°C$. Electrical tests are performed with high-speed automated test equipment, so that $T_J = T_A$, unless otherwise noted.

Note 6: Guaranteed and 100% production tested.

Note 7: Guaranteed over the operating temperature range (but not 100% tested).

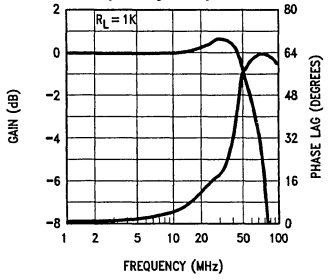
Note 8: The input is biased to 2.5V and V_{IN} swings V_{pp} about this value. The input swing is 2 V_{pp} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{pp}.

Note 9: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

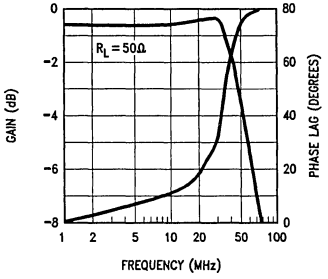
Note 10: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Typical Performance Characteristics T_J = 25°C, unless otherwise specified

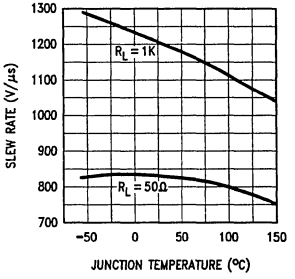
Frequency Response



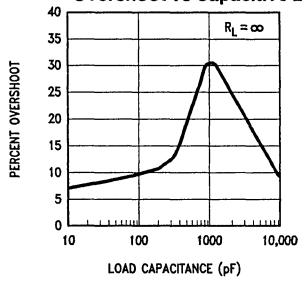
Frequency Response



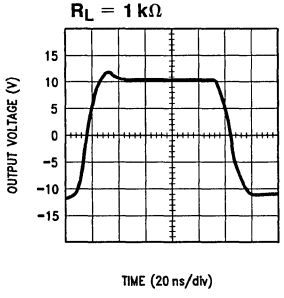
Slew Rate vs Temperature



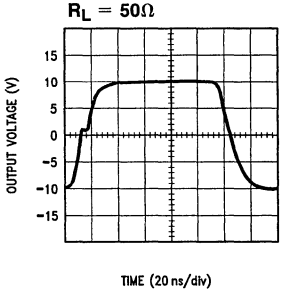
Overshoot vs Capacitive Load



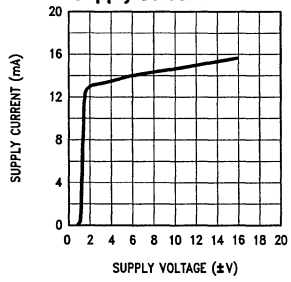
Large Signal Response
R_L = 1 kΩ



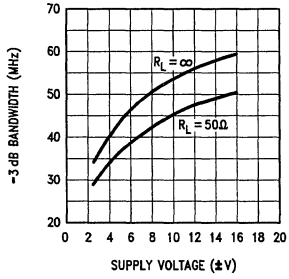
Large Signal Response
R_L = 50Ω



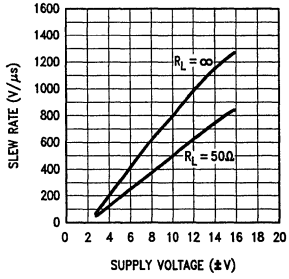
Supply Current



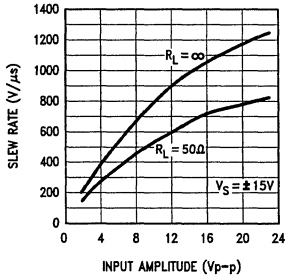
−3 dB Bandwidth



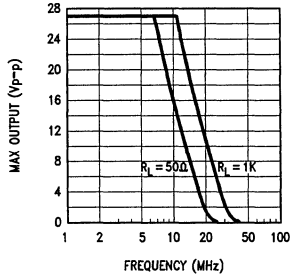
Slew Rate



Slew Rate

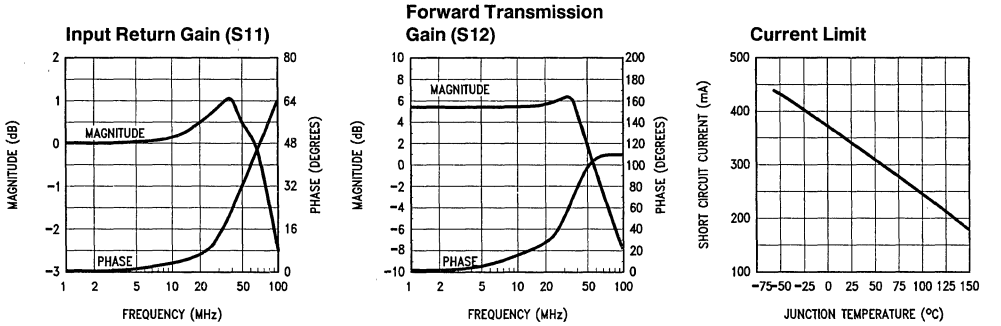


Power Bandwidth



TL/H/9223–4

Typical Performance Characteristics T_J = 25°C, unless otherwise specified (Continued)



TL/H/9223–5

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

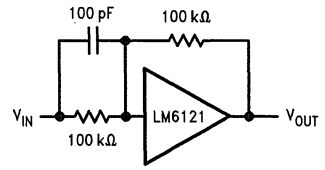
Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.



TL/H/9223–6

FIGURE 1. LM6121 with Overvoltage Protection

National Semiconductor

LM6125/LM6225/LM6325 High Speed Buffer

General Description

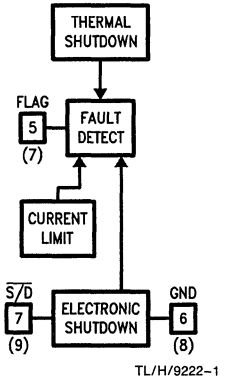
The LM6125 family of high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

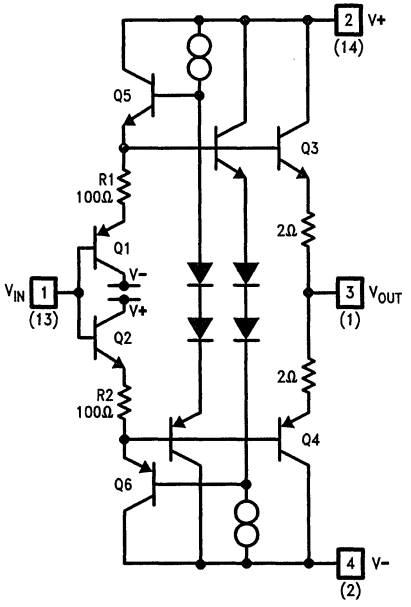
Features

- High slew rate — 800 V/μs
- Wide bandwidth — 50 MHz
- Peak output current — ±300 mA
- High input impedance — 5 MΩ
- No oscillations with capacitive loads
- Current and thermal limiting
- Electronic shutdown
- "Bi-state" output
- Error flag warns of faults
- Slew rate and bandwidth 100% tested
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

Simplified Schematic and Block Diagram



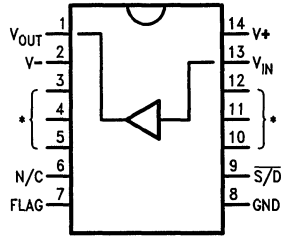
TL/H/9222-1



TL/H/9222-2

Numbers in ( ) are for 14-pin N DIP.

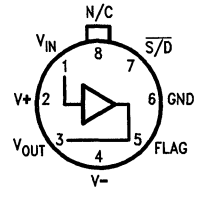
Pin Configurations



TL/H/9222-3

*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N or LM6325N
See NS Package Number N14A



TL/H/9222-4

Top View

Note: Pin 4 connected to case

Order Number LM6125H or LM6225H
See NS Package Number H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18V)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Flag Output Voltage	GND ≤ Vflag ≤ +Vsupply
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 11)	±1500V

	Package H	Package N
θ_{JA} (Note 4)	150°C/W	40°C/W
Maximum Junction Temp. (T_J)	150°C	150°C
Operating Temperature Range		
LM6125	−55°C to +125°C	
LM6225	−40°C to +85°C	
LM6325	0°C to +70°C	
Operating Supply Voltage Range	4.75V to ±16V	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6125 Tested Limit (Note 6)	LM6125 Design Limit (Note 7)	LM6225 Tested Limit (Note 6)	LM6225 Design Limit (Note 7)	LM6325 Tested Limit (Note 6)	LM6325 Design Limit (Note 7)	Units
A_{V1}	Voltage Gain 1	R_L = 1kΩ, V_{IN} = ±10V	0.990	0.980 **0.970**		0.980	**0.950**	0.970	**0.950**	
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.900	0.860 **0.800**		0.860	**0.820**	0.850	**0.820**	V/V min
A_{V3}	Voltage Gain 3 (Note 8)	R_L = 50Ω, V_{IN} = 2 V_{PP} V^+ = 5V **(1.5 V_{PP})**	0.840	0.780 **0.750**		0.780	**0.700**	0.750	**0.700**	
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	30 **50**		30	**60**	50	**100**	mV max
I_B	Input Bias Current	R_L = 1 kΩ, R_S = 10kΩ	1	4 **7**		4	**7**	5	**7**	μA max
R_{IN}	Input Resistance	R_L = 50Ω	5							MΩ
C_{IN}	Input Capacitance		3.5							pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3	5 **10**		5	**10**	5	**6**	Ω max
I_{S1}	Supply Current 1	R_L = ∞	15	18 **20**		18	**20**	20	**22**	
I_{S2}	Supply Current 2	R_L = ∞, V^+ = 5V	14	16 **18**		16	**18**	18	**20**	mA max
$I_{S/D}$	Supply Current in Shutdown	R_L = ∞, V± = ±15V	1.1	1.5 **2.0**		1.5	**2.0**	1.5	**2.0**	
V_{O1}	Output Swing 1	R_L = 1 kΩ	13.5	13.3 **13**		13.3	**13**	13.2	**13**	
V_{O2}	Output Swing 2	R_L = 100Ω	12.7	11.5 **10**		11.5	**10**	11	**10**	±V min
V_{O3}	Output Swing 3	R_L = 50Ω	12	11 **9**		11	**9**	10	**9**	
V_{O4}	Output Swing 4	R_L = 50Ω V^+ = 5V (Note 8)	1.8	1.6 **1.3**		1.6	**1.4**	1.6	**1.5**	V_{PP} min
PSRR	Power Supply Rejection Ratio	V± = ±5V to ±15V	70	60 **55**		60	**50**	60	**50**	dB min
V_{OL}	Flag Pin Output Low Voltage	I_{SINK} Flag Pin = 500 μA (Note 9)		300 **400**		300	**400**	340	**400**	mV max
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V $V_{S/D}$ = 0V (Note 9)	0.01	10 **20**		10	**20**	10	**20**	μA max

DC Electrical Characteristics (Note 5) (Continued)

Symbol	Parameter	Conditions	Typ	LM6125		LM6225		LM6325		Units
				Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{TH}	Shutdown Threshold		1.4							V
V_{IH}	Shutdown Pin Trip Point High			2.0 **2.0**		2.0	**2.0**	2.0	**2.0**	V min
V_{IL}	Shutdown Pin Trip Point Low			0.8 **0.8**		0.8	**0.8**	0.8	**0.8**	V max
I_{IL}	Shutdown Pin Input Low Current	$V_{S/D}$ = 0V	−0.07	−10 **−20**		−10	**−20**	−10	**−20**	μA max
I_{IH}	Shutdown Pin Input High Current	$V_{S/D}$ = 5V	−0.05	−10 **−20**		−10	**−20**	−10	**−20**	μA max
I_O	Bi-State Output Current	Shutdown Pin = 0V V_{OUT} = +5V or −5V	1	50 **2000**		50	**100**	100	**200**	μA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	Typ	LM6125		LM6225		LM6325		Units
				Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	Tested Limit (Note 6)	Design Limit (Note 7)	
SR_1 SR_2 SR_3	Slew Rate 1 Slew Rate 2 Slew Rate 3	V_{IN} = ±11V, R_L = 1 kΩ V_{IN} = ±11V, R_L = 50Ω (Note 10) V_{IN} = 2 V_{PP}, R_L = 50Ω V^+ = 5V (Note 8)	1200 800 50	550		550		550		V/μs min
BW	−3 dB Bandwidth	V_{IN} = 100 mV_{PP} R_L = 50Ω C_L ≤ 10 pF	50	30		30		30		MHz min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mV_{PP}	8.0							ns
t_{PD}	Propagation Delay Time	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mV_{PP}	4.0							ns
	Overshoot	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mV_{PP}	10							%
V_{FT}	V_{IN}, V_{OUT} Feedthrough in Shutdown	Shutdown Pin = 0V V_{IN} = 4 V_{P-P}, 1 MHz R_L = 50Ω	−50							dB
C_{OUT}	Output Capacitance in Shutdown	Shutdown Pin = 0V	30							pF
t_{SD}	Shutdown Response Time		700							ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 40°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60°C/W.

Note 5: $R_S = 50\Omega$, $V_S = \pm 15V_{shutdown} = V^+$, unless otherwise specified. **Boldface** numbers apply over the operating temperature range. Numbers is standard typeface apply at $T_A = 25°C$. Electrical tests are performed with high-speed automated test equipment, so that $T_J = T_A$, unless otherwise noted.

Note 6: Guaranteed and 100% production tested.

Note 7: Guaranteed over the Operating Temperature Range (but not 100% tested).

Note 8: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{PP}.

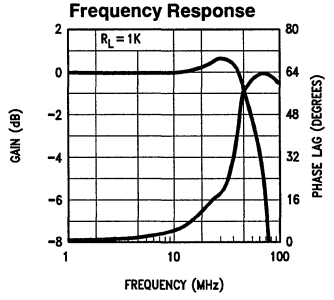
Note 9: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

Note 10: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

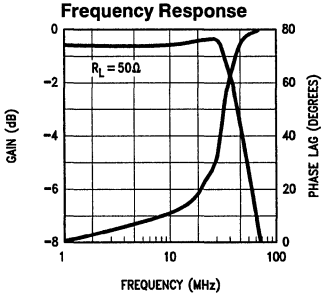
Note 11: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Typical Performance Characteristics $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified

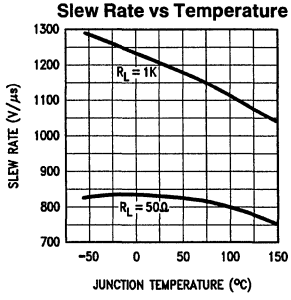
Frequency Response



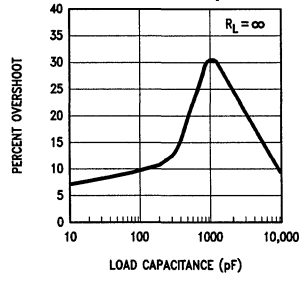
Frequency Response



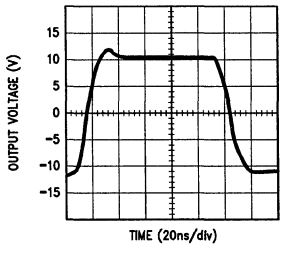
Slew Rate vs Temperature



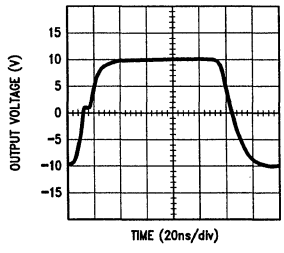
Overshoot vs Capacitive Load



Large Signal Response (R_L = 1 kΩ)



Large Signal Response (R_L = 50Ω)



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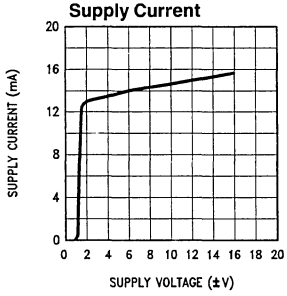
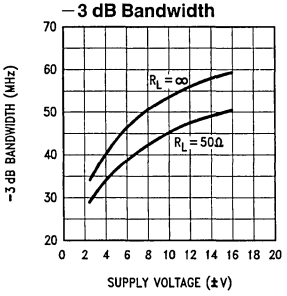
Typical Performance Characteristics $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified (Continued)

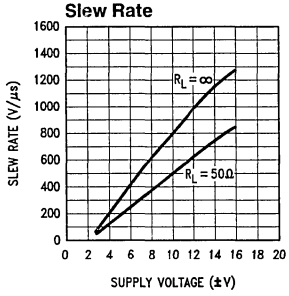
Supply Current



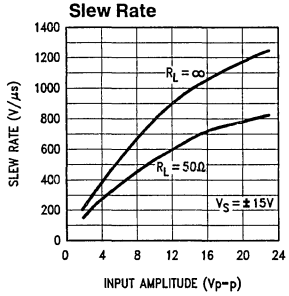
−3 dB Bandwidth



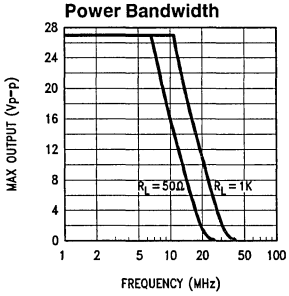
Slew Rate



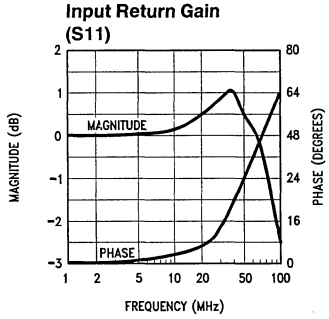
Slew Rate



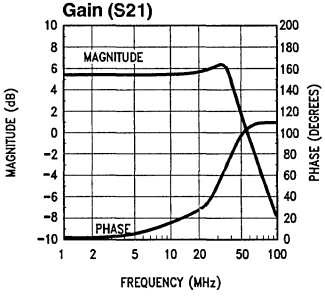
Power Bandwidth



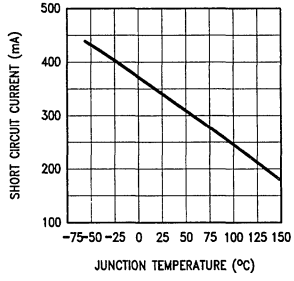
Input Return Gain (S11)



Forward Transmission Gain (S21)



Current Limit



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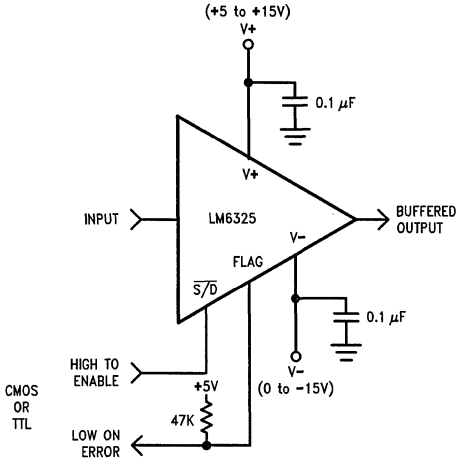
Typical Connection Diagram



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Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH results in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

If the S/D pin is not to be used, it should be connected to V^+.

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

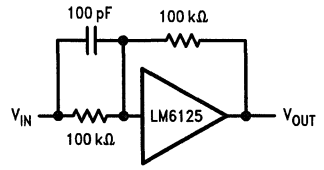

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FIGURE 1. LM6125 with Overvoltage Protection

Section 5

Voltage Comparators

Section 5 Contents

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Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

National Semiconductor

Voltage Comparators Selection Guide

	Response Time (Typ) ns	V_{OS} mV(Max)	I_S mA(Max)	I_B nA(Max)	Comments
T_A = 25°C (Notes 1 and 2)					
LM361	12	5	25	30,000	High Speed w/Strobes
LM360	16	5	32	20,000	High Speed, Complementary Outputs
LM306	40	5	10	25,000	High Speed, High Drive
LM319	80	8	12.5	1000	High Speed Dual
LF311	200	10	7.5	0.15	FET Input
LM311	200	10	7.5	300	General Purpose Single
LH2311	200	7.5	7.5	250	Dual LM311
LM339	1300	5	2	400	General Purpose Quad
LM392	1300	10	1	400	One Comparator Plus One Op Amp (Note 3)
LM393	1300	5	2.5	250	General Purpose Dual
LM2903	1300	5	2.5	250	Automotive Dual
LM2901	1300	7	2	400	Automotive Quad
LM613	1500	5	1	35	Dual Comparator, Dual Op Amp and Adjustable Reference (Note 3)
LP365	4000	9	0.30	200	Programmable Quad
LP311	4000	10	0.3	150	Low Power Single
LP339	5000	9	0.1	40	Low Power Quad

*Not Specified

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

Note 3: Refer to data sheet in Op Amp chapter of this databook.

National Semiconductor

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

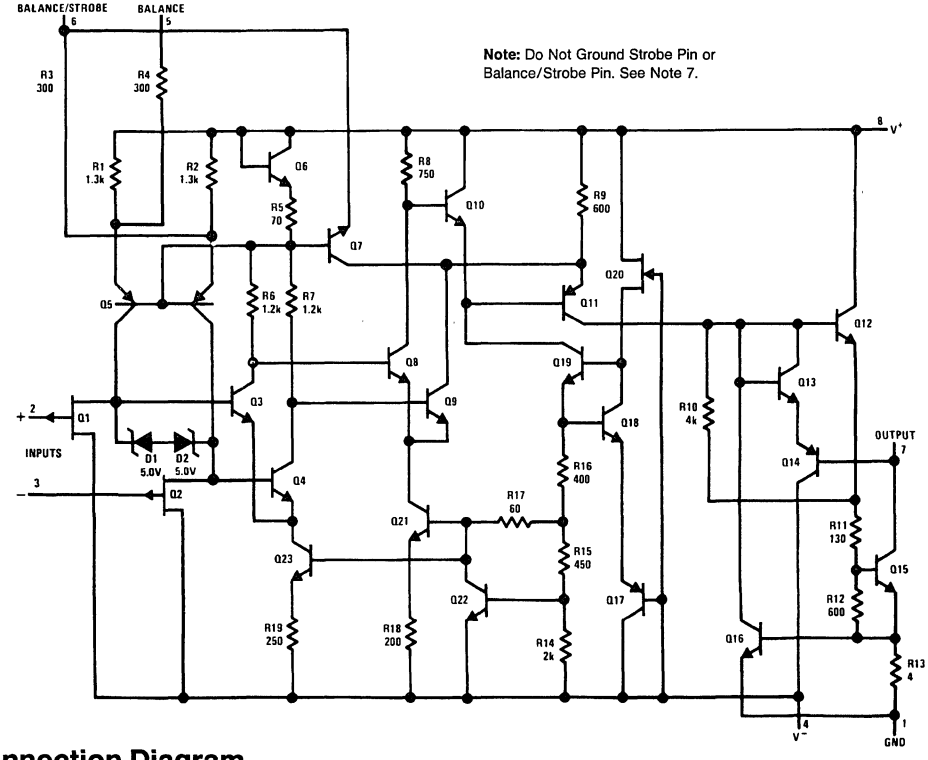
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Features

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Schematic Diagram



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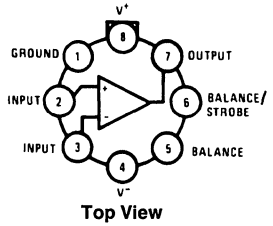
Connection Diagram

Metal Can Package



TL/H/5703–1

Top View
Order Number LF111H, LF211H or LF311H
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds

	LF111/LF211	LF311
Operating Temp. Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C	260°C

ESD rating to be determined.

Electrical Characteristics (LF111/LF211) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \leq 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			6.0	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range		−13.5	±14	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0$ mV, $I_{OUT} \leq 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +65°C/W junction to ambient (in 400 linear feet/min air flow), +165°C/W junction to ambient (in static air), or +20°C/W junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq \pm 85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 8: Refer to RETSF111X for LF111H military specifications.

Electrical Characteristics (LF311) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = 15V$, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +165°C/W, junction to ambient, or +20°C/W, junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

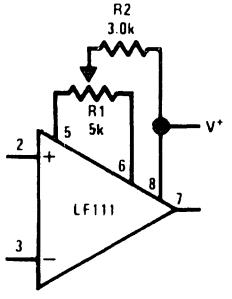
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

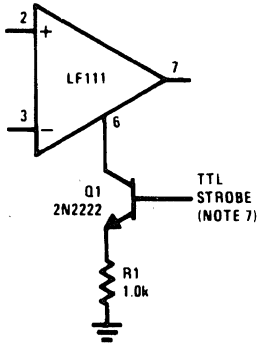
Auxiliary Circuits

Offset Balancing



TL/H/5703–13

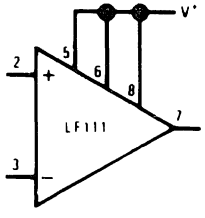
Strobing



TL/H/5703–14

Note: Do Not Ground Strobe Pin.

Increasing Input Stage Current*

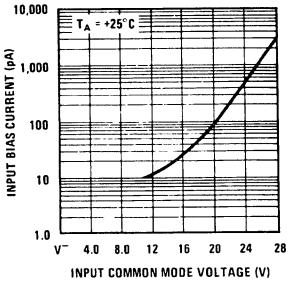


TL/H/5703–15

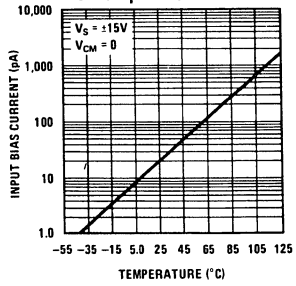
*Increases typical common mode slew from 7.0V/μs to 18V/μs

Typical Performance Characteristics

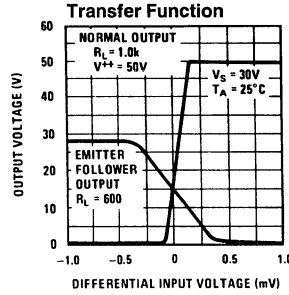
Input Bias Current vs Common Mode



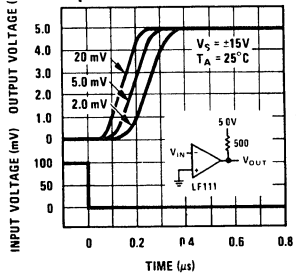
Input Bias Current vs Temperature



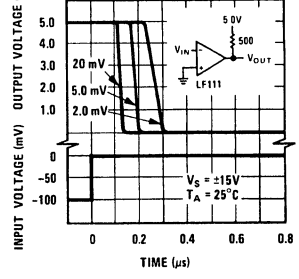
Transfer Function



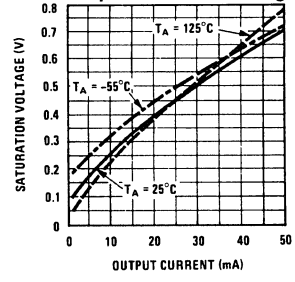
Response Time for Various Input Overdrives



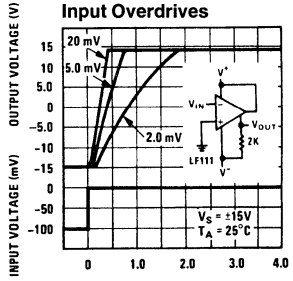
Response Time for Various Input Overdrives



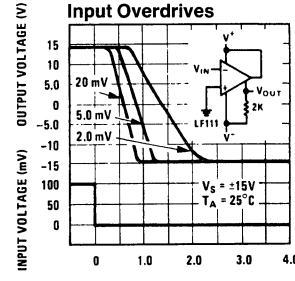
Output Saturation Voltage



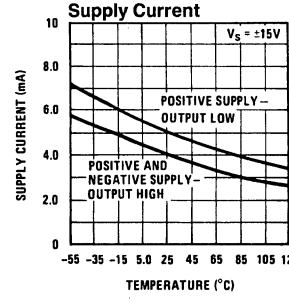
Response Time for Various Input Overdrives



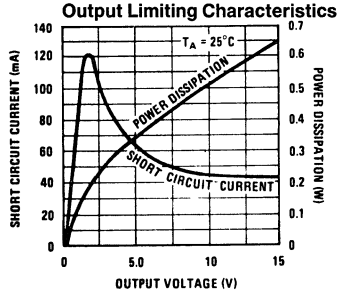
Response Time for Various Input Overdrives



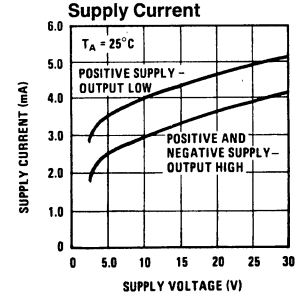
Supply Current



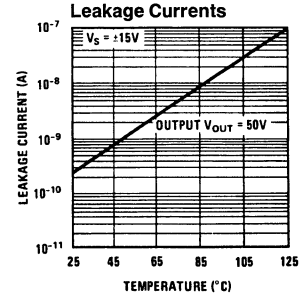
Output Limiting Characteristics



Supply Current



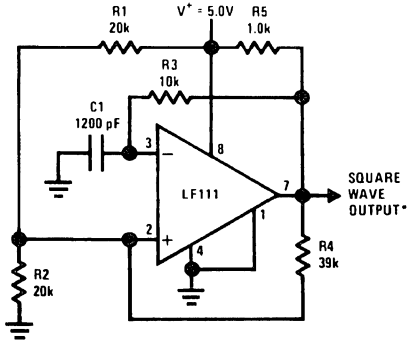
Leakage Currents



TL/H/5703–4

Typical Applications

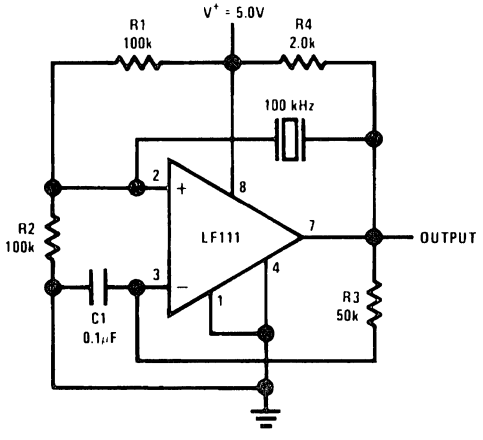
100 kHz Free Running Multivibrator



TL/H/5703–7

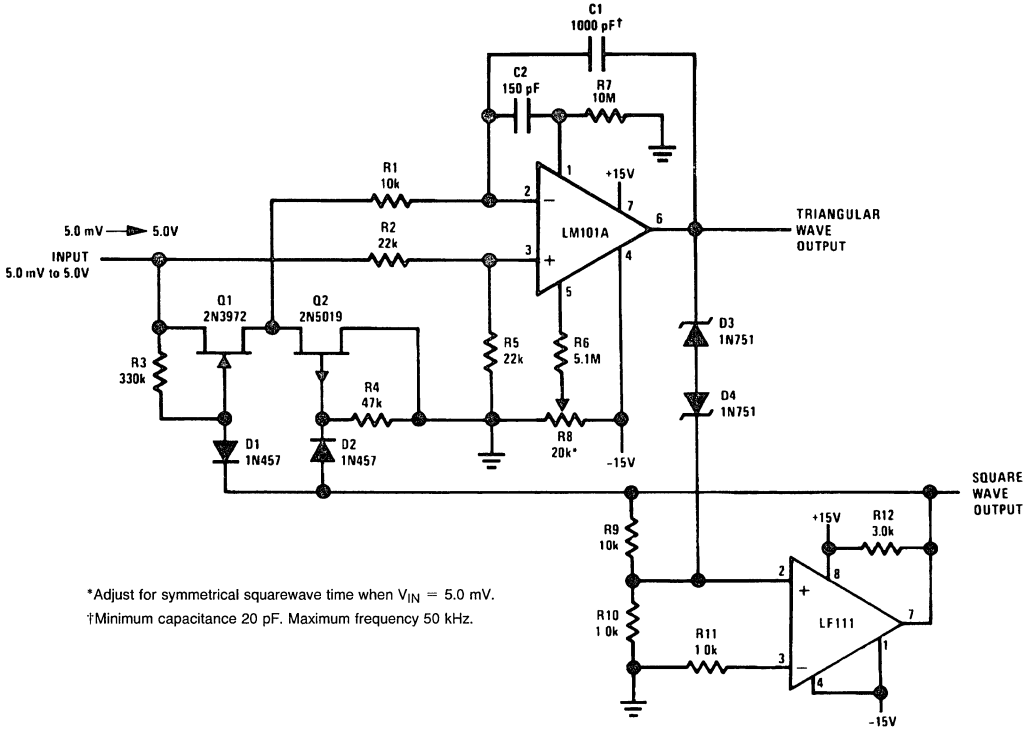
*TTL or DTL fanout of two.

Crystal Oscillator



TL/H/5703–3

10 Hz to 10 kHz Voltage Controlled Oscillator



*Adjust for symmetrical squarewave time when V_{IN} = 5.0 mV.

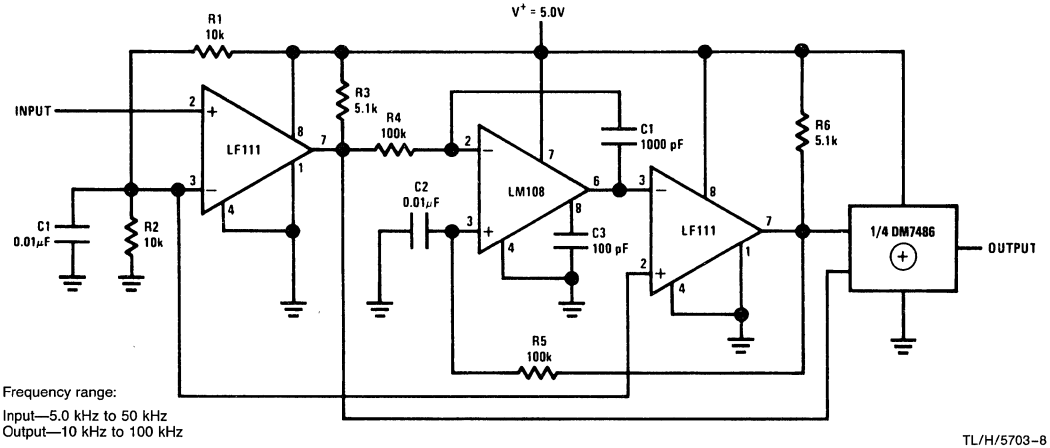
†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

TL/H/5703–5

5

Typical Applications (Continued)

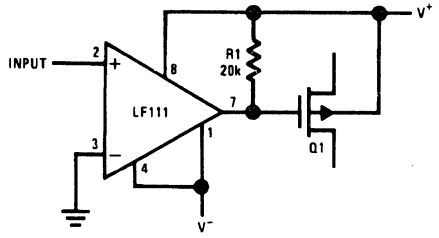
Frequency Doubler



Frequency range:
Input—5.0 kHz to 50 kHz
Output—10 kHz to 100 kHz

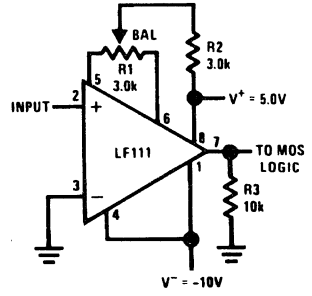
TL/H/5703–8

Zero Crossing Detector Driving MOS Switch



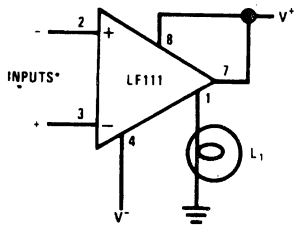
TL/H/5703–9

Zero Crossing Detector Driving MOS Logic



TL/H/5703–10

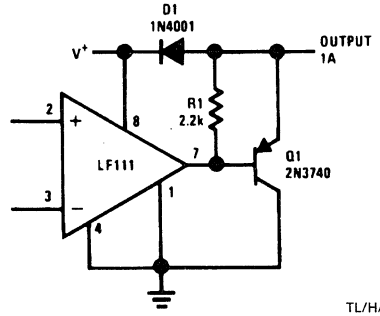
Driving Ground-Referred Load



TL/H/5703–11

*Input polarity is reversed when using pin 1 as output.

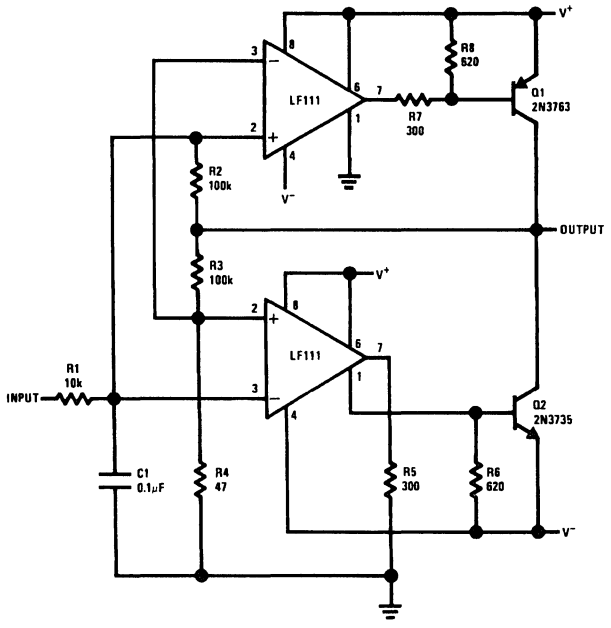
Comparator and Solenoid Driver



TL/H/5703–12

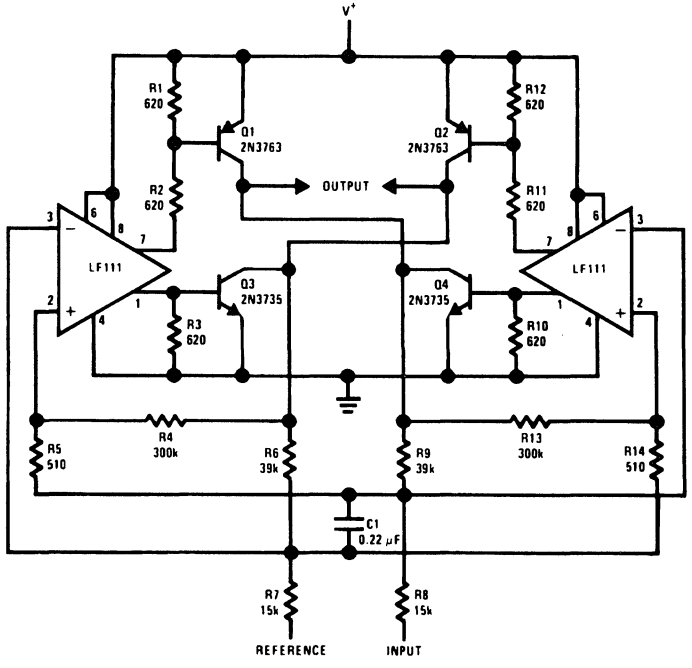
Typical Applications (Continued)

Switching Power Amplifier



TL/H/5703–16

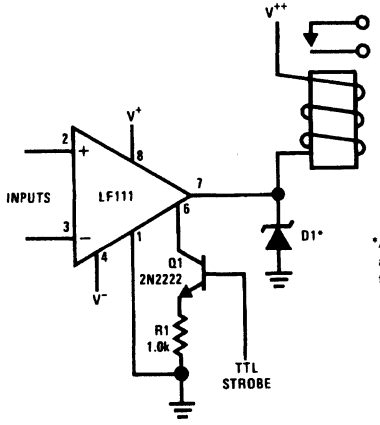
Switching Power Amplifier



TL/H/5703–17

Typical Applications (Continued)

Relay Driver with Strobe

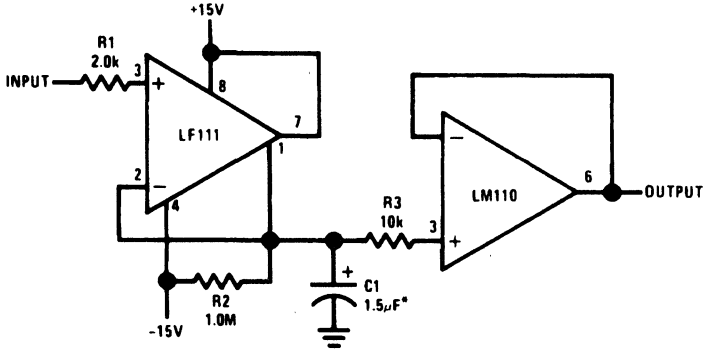


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

TL/H/5703–18

Note: Do Not Ground Strobe Pin.

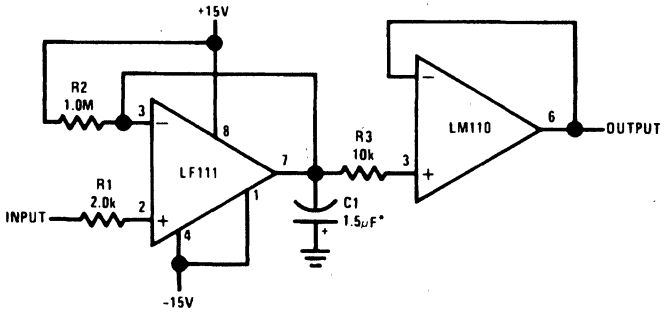
Positive Peak Detector



*Solid tantalum

TL/H/5703–19

Negative Peak Detector

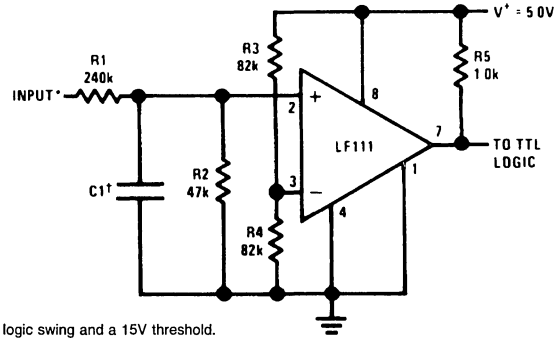


*Solid tantalum

TL/H/5703–20

Typical Applications (Continued)

TTL Interface with High Level Logic

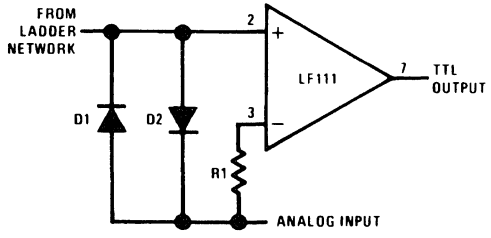


*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes

TL/H/5703–21

Using Clamp Diodes to Improve Response



TL/H/5703–6

National Semiconductor

LH2111/LH2211/LH2311
Dual Voltage Comparators

General Description

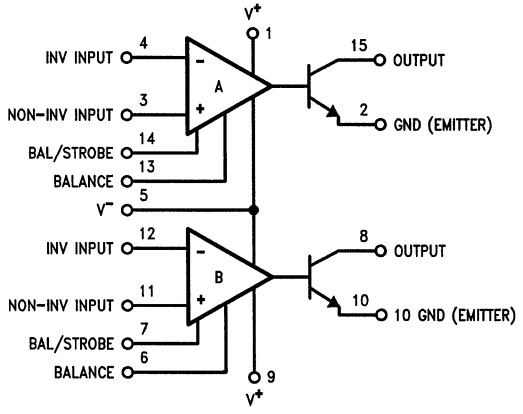
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2211 is specified for operation over the −25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

■ Wide operating supply range	±15V to a single +5V
■ Low input currents	6 nA
■ High sensitivity	10 μV
■ Wide differential input range	±30V
■ High output drive	50 mA, 50V

Connection Diagram



TL/K/10116–1

Order Number LH2111D, LH2211D or LH2311D
See NS Package Number D16C

Order Number LH2111J, LH2211J or LH2311J
See NS Package Number J16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V
Ground to Negative Supply Voltage (GND $- V^-$)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	−55°C to +125°C
LH2211	−25°C to +85°C
LH2311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 3)

Parameter	Conditions	Limits			Units
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$, $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

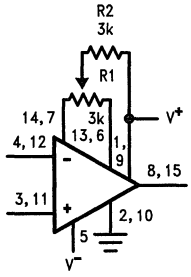
Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

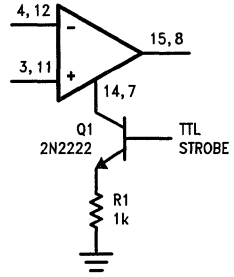
Auxiliary Circuits

Offset Balancing



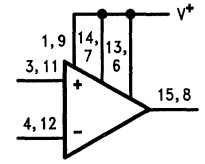
TL/K/10116–2

Strobing



TL/K/10116–3

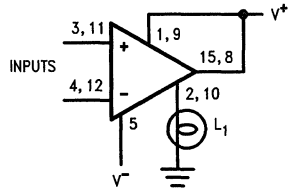
Increasing Input Stage Current*



TL/K/10116–4

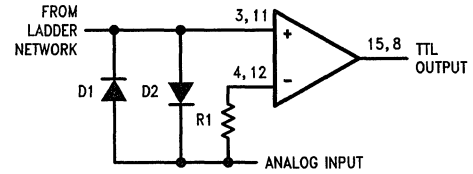
*Increases typical common mode slew from 7.0 V/μs to 18 V/μs

Driving Ground-Referred Load



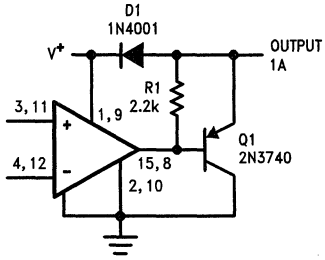
TL/K/10116–5

Using Clamp Diodes to Improve Responses



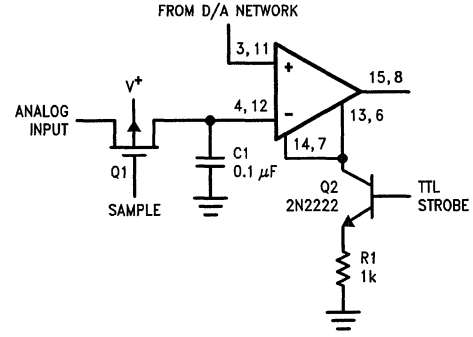
TL/K/10116–6

Comparator and Solenoid Driver



TL/K/10116–7

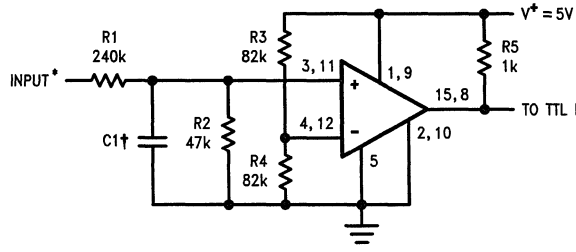
Strobing off Both Input* and Output Stages



TL/K/10116–8

*Typical input current is 50 pA with inputs strobed off

TTL Interface with High Level Logic



*Values shown are for a 0V to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TL/K/10116–9

National Semiconductor

LM106/LM206/LM306 Voltage Comparator

General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 10 mA.

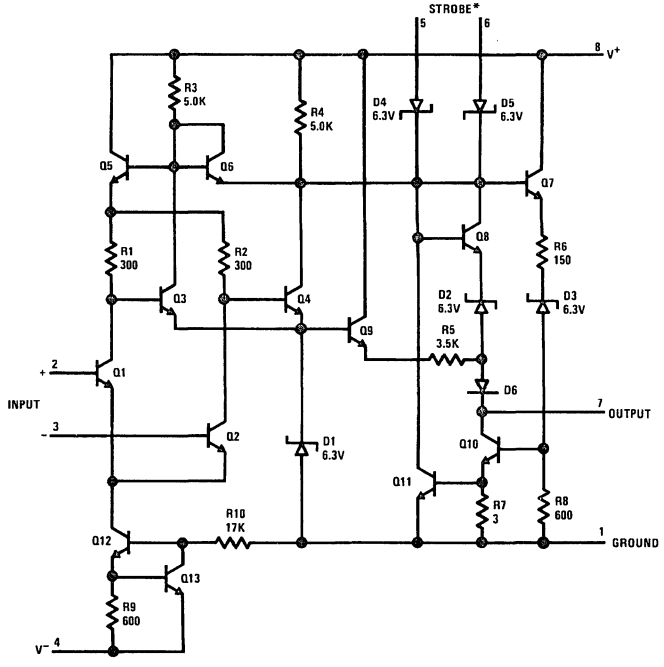
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM206 is specified for operation over the −25°C to +85°C temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

Features

- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

Schematic and Connection Diagrams**

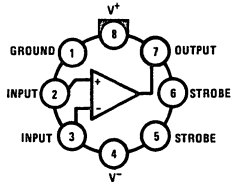


TL/H/7756-1

*Grounding either strobe forces the output to −0.5V (typ.). To disable strobe function, connect strobes to V^+ or leave open.

**Pin connections shown are for TO-5 package.

Metal Can



TL/H/7756-2

Top View

Note: Pin 4 connected to case.

Order Number LM106H, LM206H or LM306H
See NS Package Number H08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Positive Supply Voltage	15V
Negative Supply Voltage	−15V
Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V

Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 seconds
Operating Temperature Range	T_{MIN} T_{MAX}
LM106	−55°C to +125°C
LM206	−25°C to +85°C
LM306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating to be determined.	

Electrical Characteristics (Note 2)

Parameter	Conditions	LM106/LM206			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 3)		0.5	2.0		1.6	5.0	mV
Input Offset Current	(Note 3)		0.7	3.0		1.8	5.0	μA
Input Bias Current			10	20		16	25	μA
Response Time	R_L = 390Ω to 5V C_L = 15 pF, (Note 4)		28	40		28	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 100 mA $V_{IN} \leq -7$ mV, I_{OUT} = 100 mA		1.0	1.5		 0.8	 2.0	V V
Output Leakage Current	$V_{IN} \geq 5$ mV, 8V ≤ V_{OUT} ≤ 24V $V_{IN} \geq 7$ mV, 8V ≤ V_{OUT} ≤ 24V		0.02	1.0		 0.02	 2.0	μA μA
THE FOLLOWING SPECIFICATIONS APPLY FOR $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 5)								
Input Offset Voltage	(Note 3)			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	10		5	20	μV/°C
Input Offset Current	$T_L \leq T_A \leq 25°C$, (Note 3) $25°C \leq T_A \leq T_H$		1.8 0.25	7.0 3.0		2.4	7.5 5.0	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$ $T_L \leq T_A \leq 25°C$		5.0 15	25 75		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$ $25°C \leq T_A \leq T_H$			45 20		25	40 25	μA μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 50 mA $V_{IN} \leq -8$ mV For LM306			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 16 mA $V_{IN} \leq -8$ mV For LM306			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = -400\mu A$ $V_{IN} \geq 8$ mV For LM306	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, 8V ≤ V_{OUT} ≤ 24V $V_{IN} \geq 8$ mV For LM306 $T_L \leq T_A \leq 25°C$ $25°C < T_A \leq T_H$			1.0 100			2.0 100	μA μA
Strobe Current	V_{STROBE} = 0.4V		−1.7	−3.2		−1.7	−3.2	mA

Electrical Characteristics (Note 2) (Continued)

Parameter	Conditions	LM106/LM206			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Strobe "ON" Voltage		0.9	1.4		0.9	1.4		V
Strobe "OFF" Voltage	$I_{SINK} \leq 16$ mA		1.4	2.2		1.4	2.2	V
Positive Supply Current	$V_{IN} = -5$ mV $V_{IN} = -8$ mV for LM306		5.5	10		5.5	10	mA
Negative Supply Current			−1.5	−3.6		−1.5	−3.6	mA

Note 1: The maximum junction temperature of LM106 is 150°C, LM206 is 110°C, LM306 is 85°C. For operating at elevated temperatures, devices in the HO8 package must be derated based on a thermal resistance of 170°C/W, junction to ambient, or 23°C/W, junction to case.

Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, $V^+ = 12V$ and $T_A = 25°C$ unless otherwise specified. All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

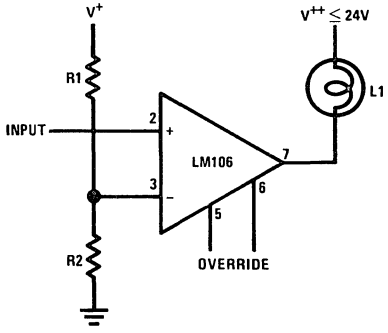
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 5: All currents into device pins are considered positive.

Note 6: Refer to RETS106X for LM106 military specifications.

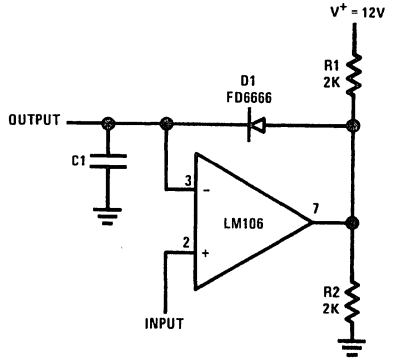
Typical Applications**

Level Detector and Lamp Driver



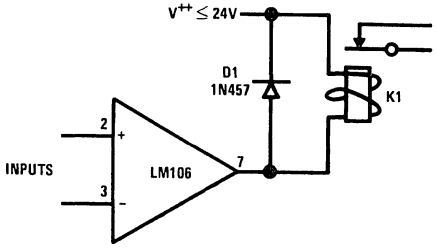
TL/H/7756–4

Fast Response Peak Detector



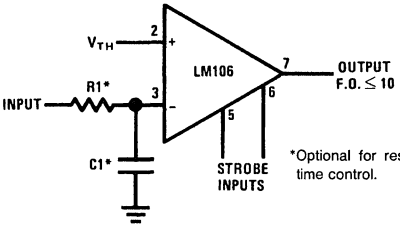
TL/H/7756–5

Relay Driver



TL/H/7756–6

Adjustable Threshold Line Receiver



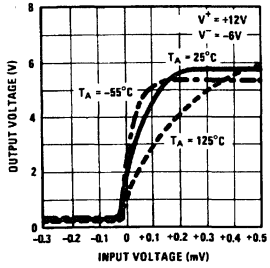
*Optional for response time control.

TL/H/7756–7

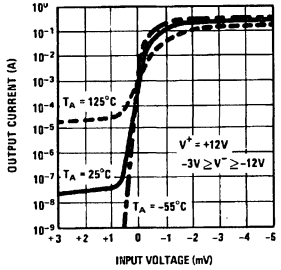
**Pin connections shown are for metal can package.

Typical Performance Characteristics

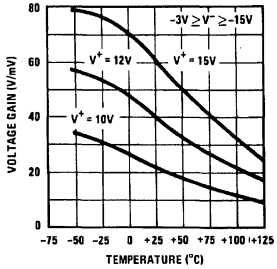
Transfer Function



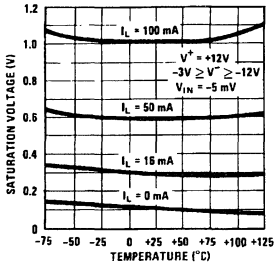
Transconductance



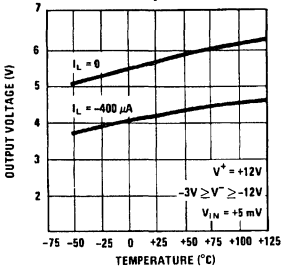
Voltage Gain



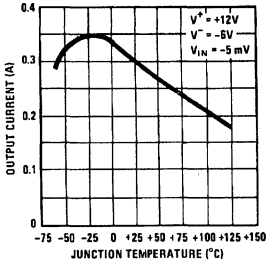
Saturation Voltage



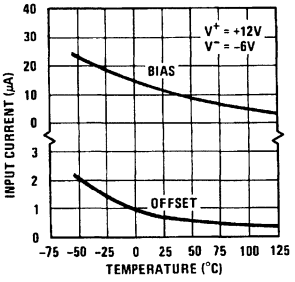
Positive Output Level



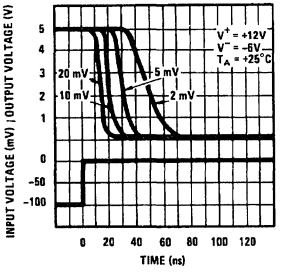
Short Circuit Output Current



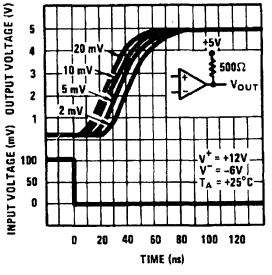
Input Current



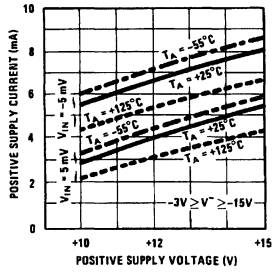
Response Time for Various Input Overdrives



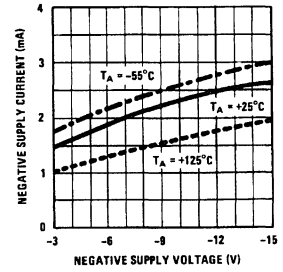
Response Time for Various Input Overdrives



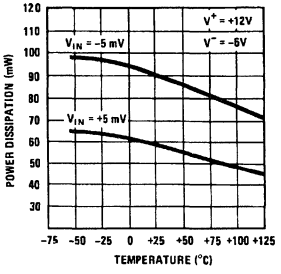
Positive Supply Current



Negative Supply Current



Power Consumption



TL/H/7756–8

National Semiconductor

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

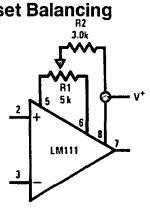
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

Features

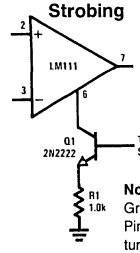
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Typical Applications**

Offset Balancing



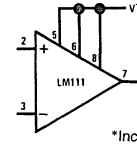
Strobing



Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

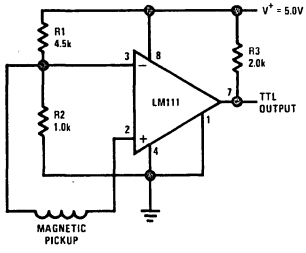
Note: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

Increasing Input Stage Current*

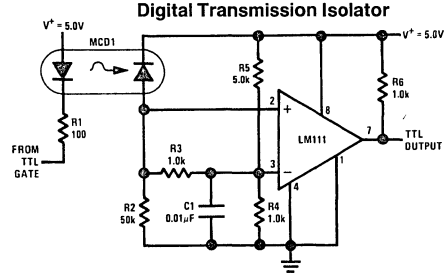


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

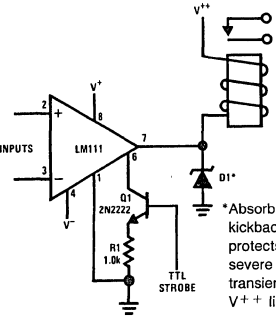
Detector for Magnetic Transducer



Digital Transmission Isolator



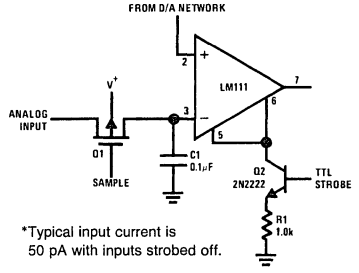
Relay Driver with Strobe



*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input* and Output Stages



*Typical input current is 50 pA with inputs strobed off.

Note: Do Not Ground Strobe Pin.

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Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec

Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ..... 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ..... 215°C
  - Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 8) 300V

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$	2.0	3.0	5.0	mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ k			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Absolute Maximum Ratings for the LM311

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage V_{74})	40V
Ground to Negative Supply Voltage V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
ESD Rating (Note 7)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ..... 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ..... 215°C
  - Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics for the LM311 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$	1.5	3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA $V^- = V_{GRND} = -5V$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

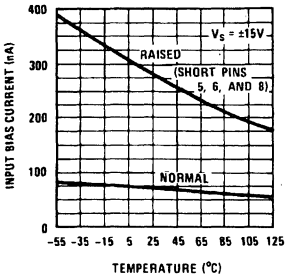
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

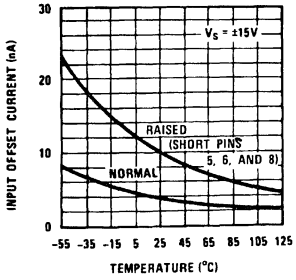
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

LM111/LM211 Typical Performance Characteristics

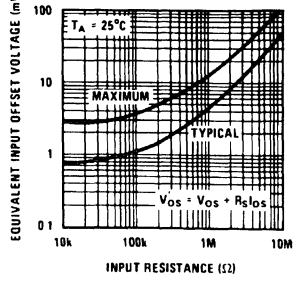
Input Bias Current



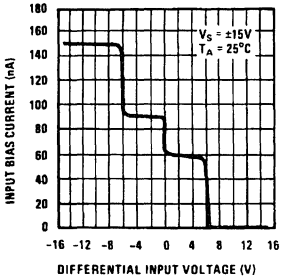
Input Offset Current



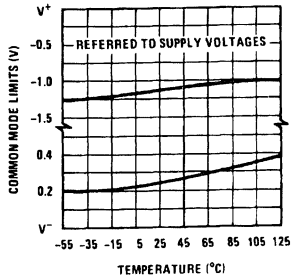
Offset Error



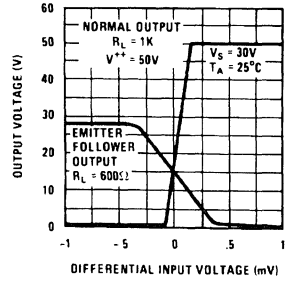
Input Characteristics



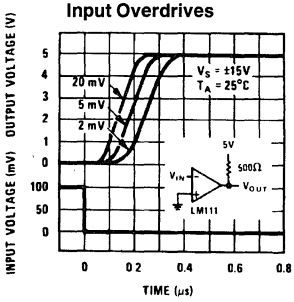
Common Mode Limits



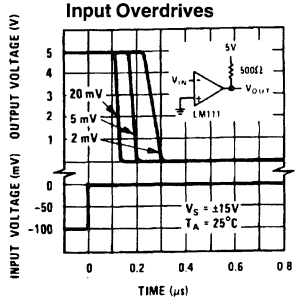
Transfer Function



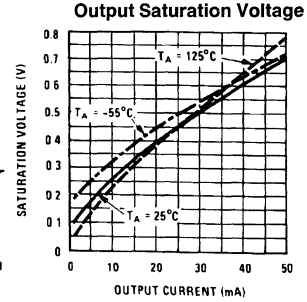
Response Time for Various Input Overdrives



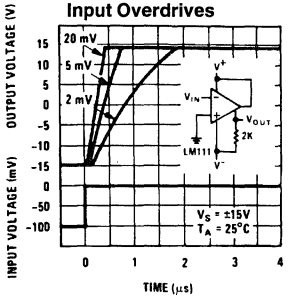
Response Time for Various Input Overdrives



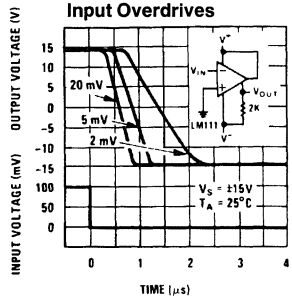
Output Saturation Voltage



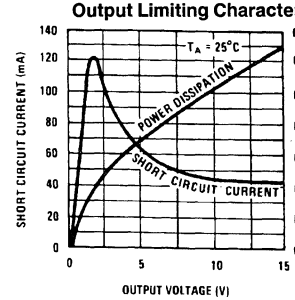
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



Output Limiting Characteristics



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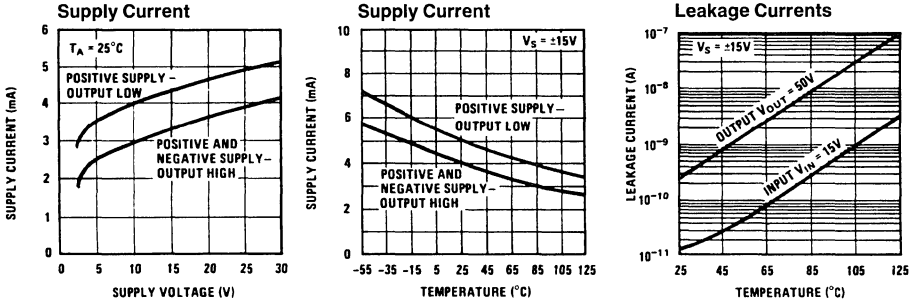
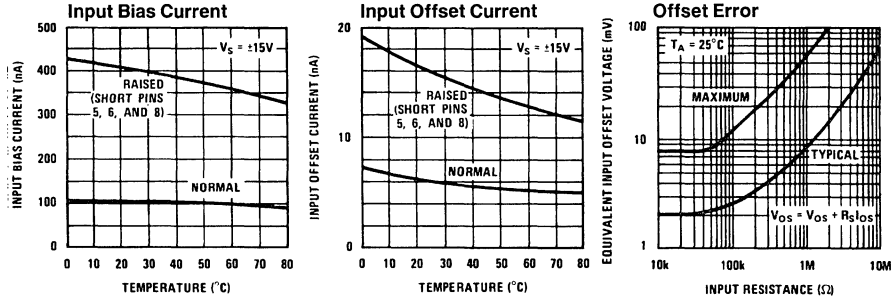
LM111/LM211 Typical Performance Characteristics (Continued)

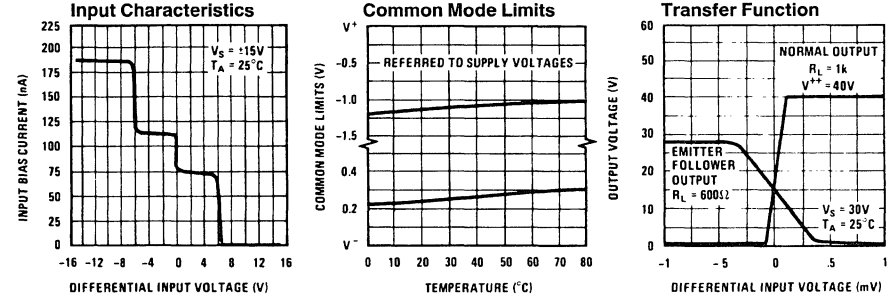


TL/H/5704–3

LM311 Typical Performance Characteristics



TL/H/5704–8



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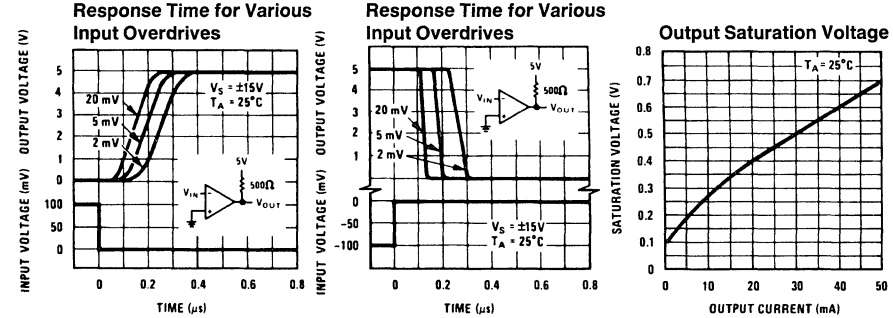

TL/H/5704–10

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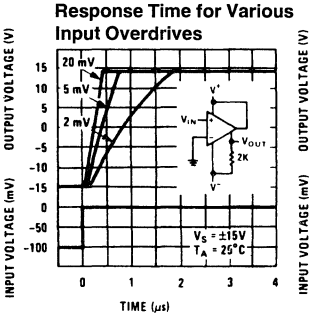
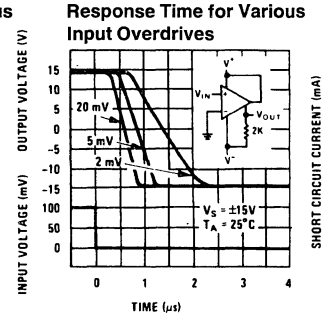
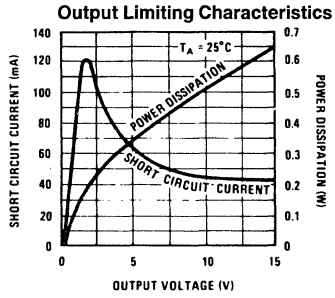
LM311 Typical Performance Characteristics (Continued)







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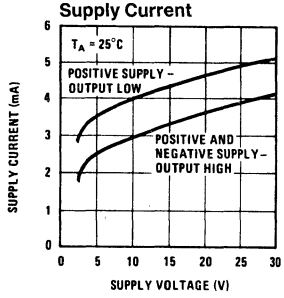

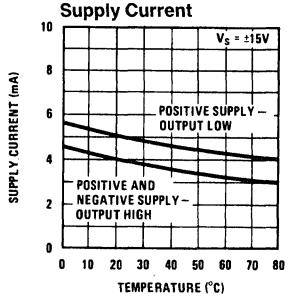

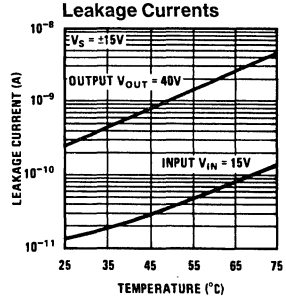

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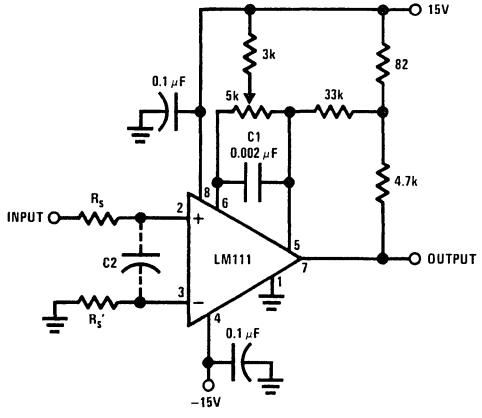
Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10$ kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



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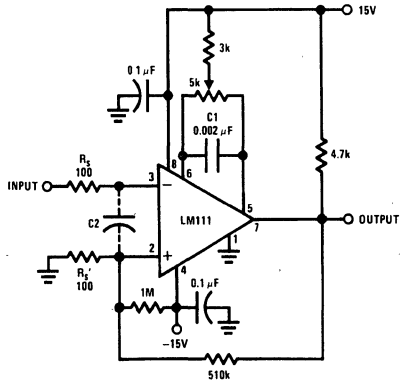
Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

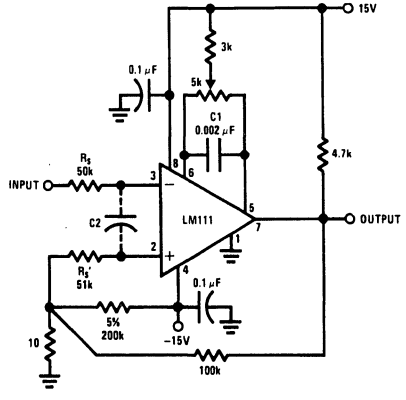
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. the circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



TL/H/5704–30

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

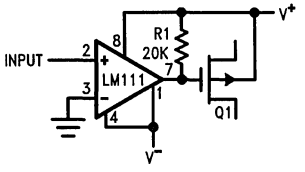


TL/H/5704–31

FIGURE 3. Positive Feedback with High Source Resistance

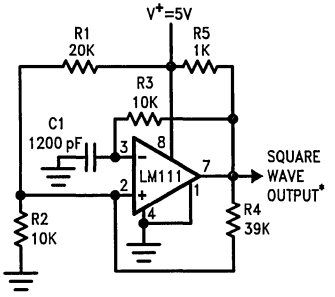
Typical Applications (Continued) (Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch



TL/H/5704–13

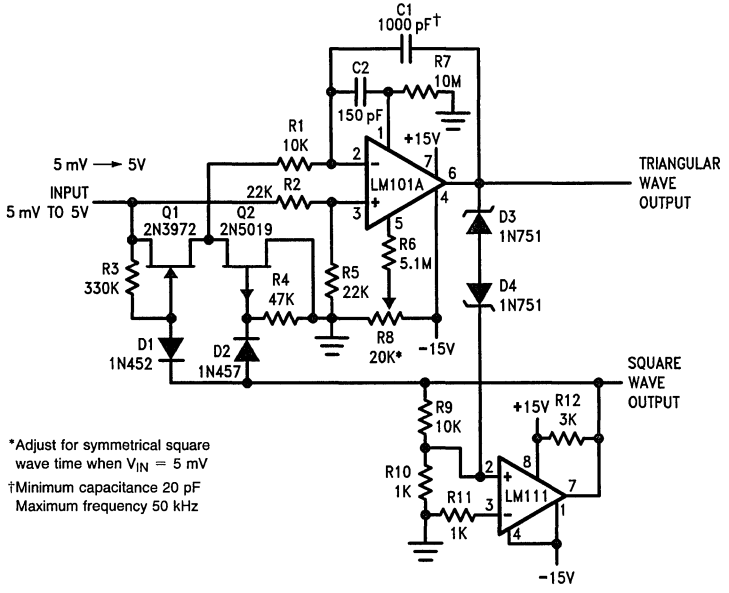
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two

TL/H/5704–14

10 Hz to 10 kHz Voltage Controlled Oscillator

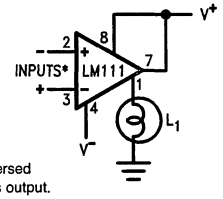


*Adjust for symmetrical square wave time when V_{IN} = 5 mV

†Minimum capacitance 20 pF
Maximum frequency 50 kHz

TL/H/5704–15

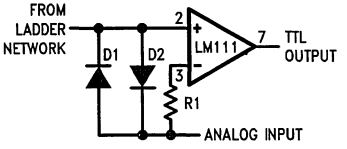
Driving Ground-Referred Load



*Input polarity is reversed when using pin 1 as output.

TL/H/5704–16

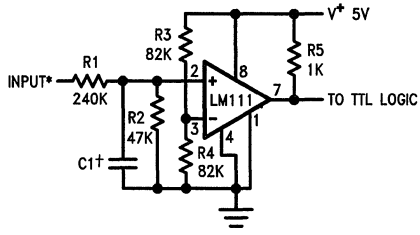
Using Clamp Diodes to Improve Response



TL/H/5704–17

Typical Applications (Continued) (Pin numbers refer to H08 package)

TTL Interface with High Level Logic

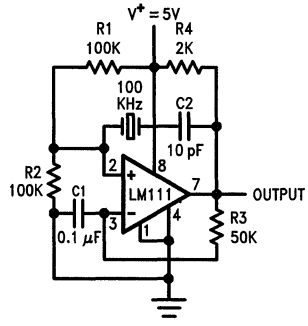


*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

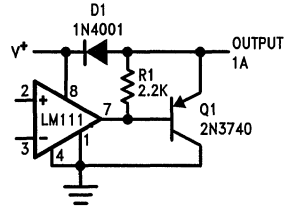
TL/H/5704–18

Crystal Oscillator



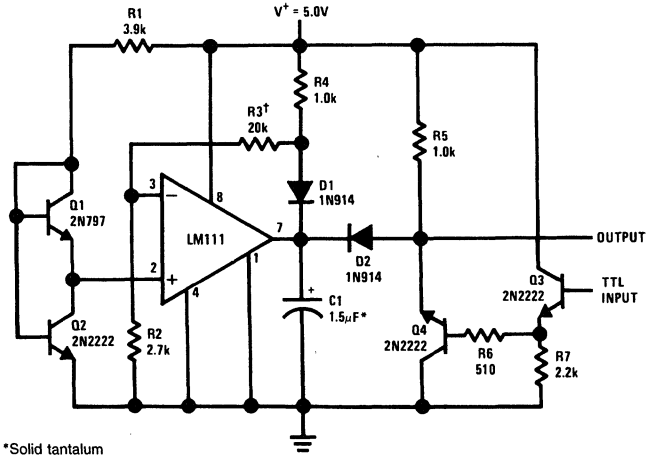
TL/H/5704–19

Comparator and Solenoid Driver



TL/H/5704–20

Precision Squarer

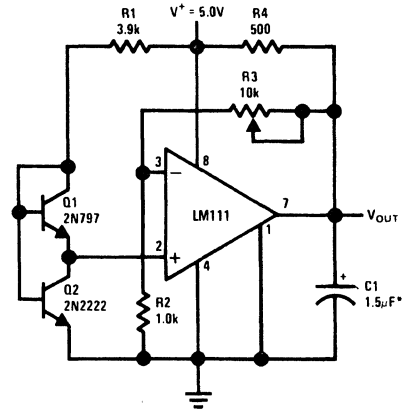


*Solid tantalum

†Adjust to set clamp level

TL/H/5704–21

Low Voltage Adjustable Reference Supply

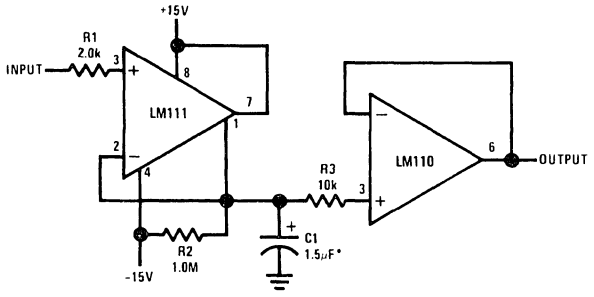


*Solid tantalum

TL/H/5704–22

Typical Applications (Continued) (Pin numbers refer to H08 package)

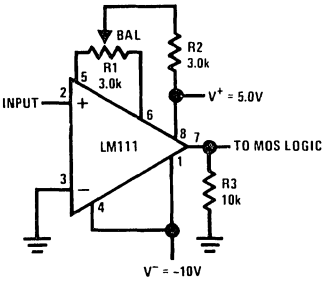
Positive Peak Detector



*Solid tantalum

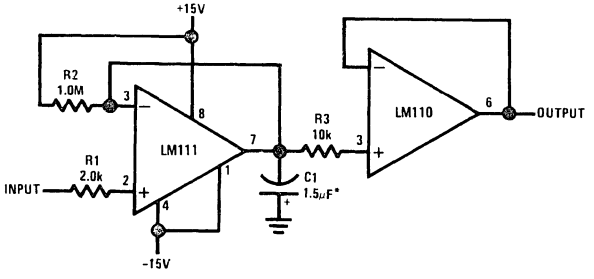
TL/H/5704–23

Zero Crossing Detector Driving MOS Logic



TL/H/5704–24

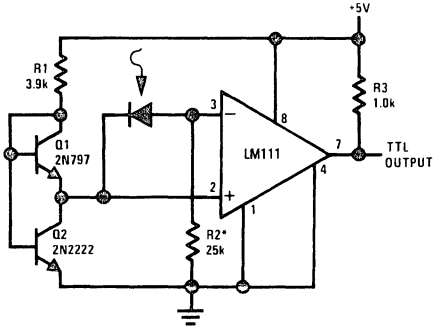
Negative Peak Detector



*Solid tantalum

TL/H/5704–25

Precision Photodiode Comparator

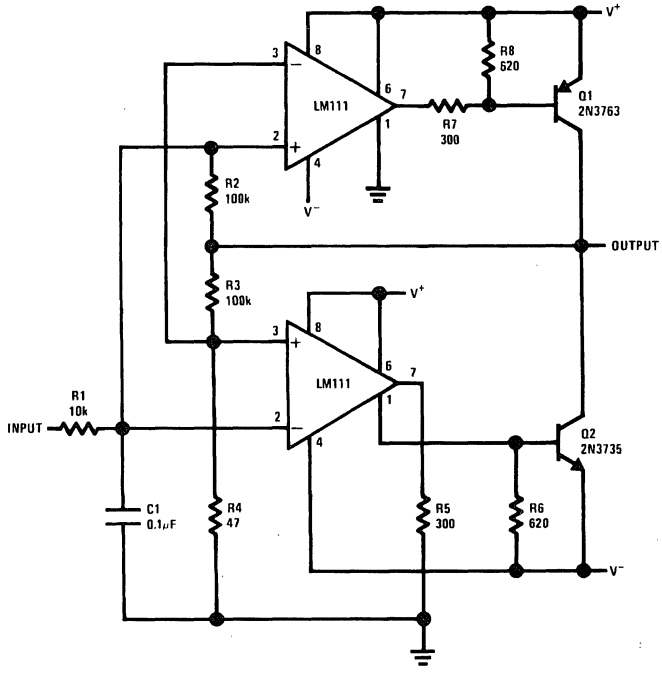


TL/H/5704–26

*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

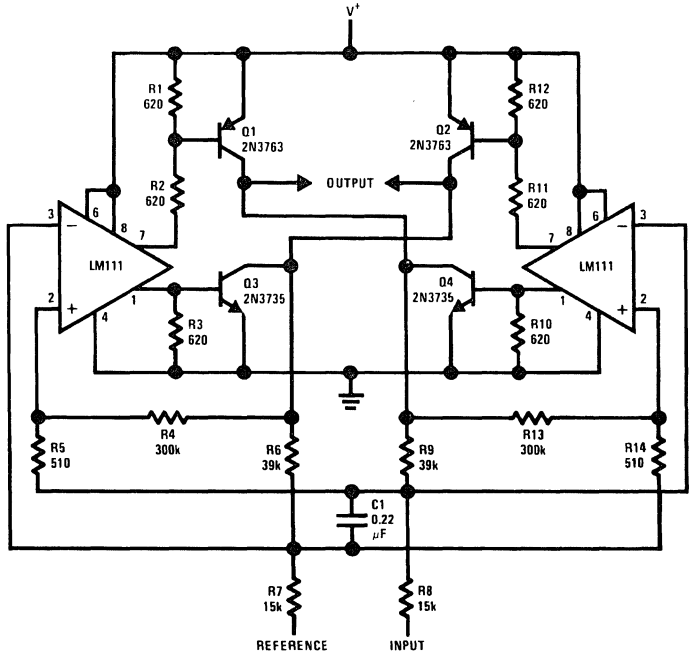
Typical Applications (Continued) (Pin numbers refer to H08 package)

Switching Power Amplifier



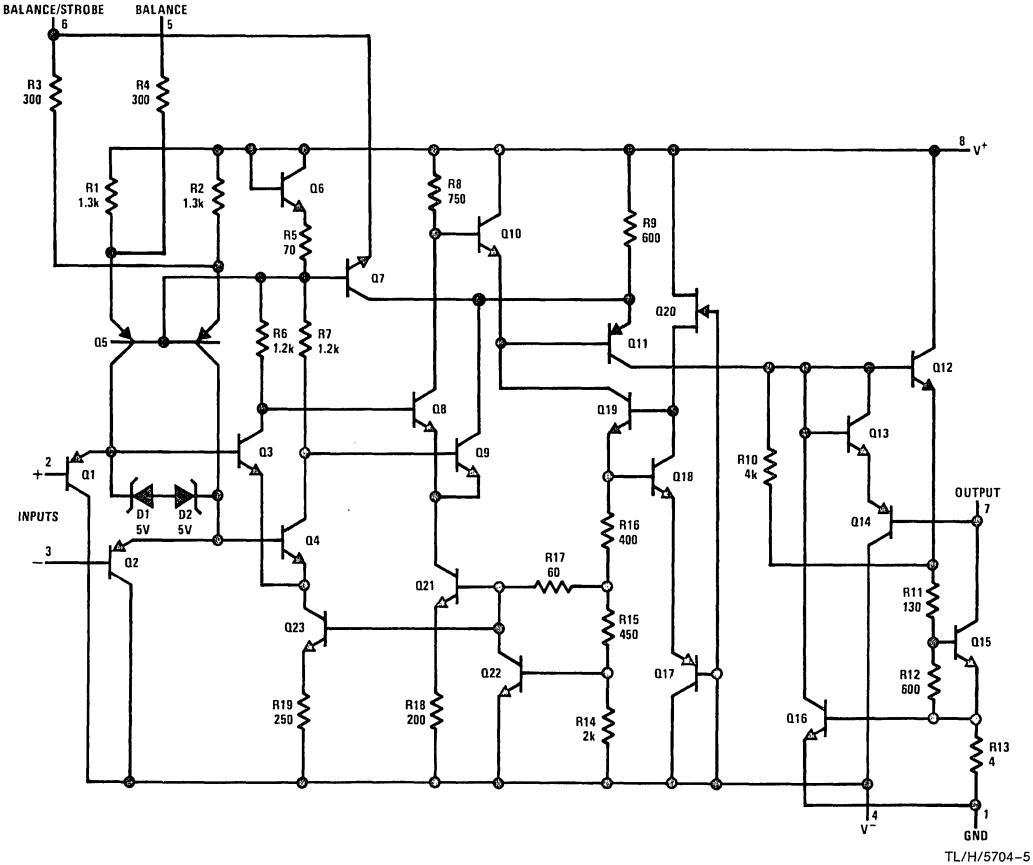
TL/H/5704–27

Switching Power Amplifier



TL/H/5704–28

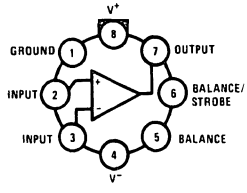
Schematic Diagram*



TL/H/5704–5

Connection Diagrams*

Metal Can Package

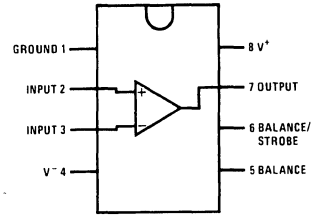


TOP VIEW

NOTE: Pin 4 connected to case.

Order Number LM111H, LM211H or LM311H
See NS Package Number H08C

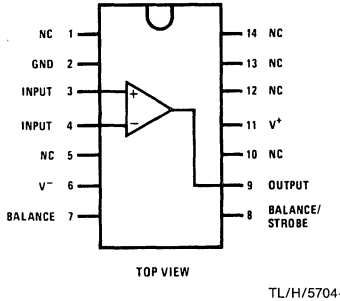
Dual-In-Line Package



TOP VIEW

Order Number LM111J-8, LM211J-8, LM311J-8, LM311M or LM311N
See NS Package Number J08A, M08A or N08E

Dual-In-Line Package



TOP VIEW

TL/H/5704–6

Order Number LM111J, LM211J, LM311J or LM311N-14
See NS Number Package J14A or N14A

*Pin connections shown on schematic diagram are for H08 package.

National Semiconductor

LM119A/LM119/LM219/LM319A/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

The LM119A and LM319A offer improved precision over the standard LM119 and LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Features

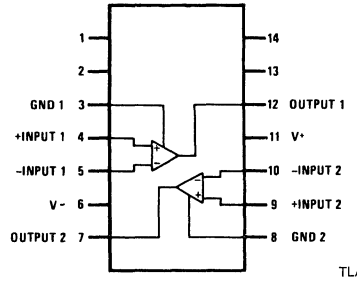
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119A and LM119 are specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319A and LM319 are specified from 0°C to +70°C.

Connection Diagrams

Dual-In-Line-Package

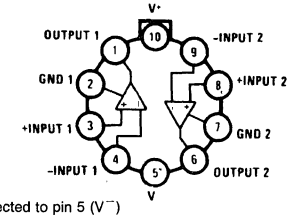


TL/H/5705–4

Top View

Order Number LM119AJ, LM119J, LM219J, LM319AJ, LM319J, LM319AM, LM319M, LM319AN or LM319N
See NS Package Number J14A, M14A or N14A

Metal Can Package



Case is connected to pin 5 (V^-)

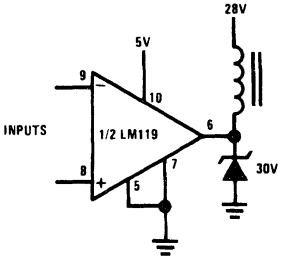
TL/H/5705–7

Top View

Order Number LM119AH, LM119H, LM319AH or LM319H
See NS Package Number H10C

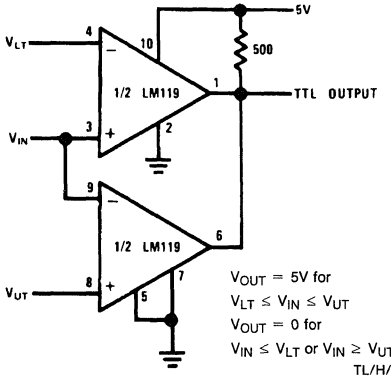
Typical Applications*

Relay Driver



TL/H/5705–5

Window Detector



TL/H/5705–6

*Pin numbers are for metal can package.

Absolute Maximum Ratings LM119A/119/219

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
ESD rating (1.5 kΩ in series with 100 pF)	800V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec

Operating Temperature Range	
LM119A, LM119	−55°C to 125°C
LM219	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM119A			LM119/LM219			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.5	1.0		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		20	40		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500		150	500	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	20	40		10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80			80		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	2		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$		1.2	2.0			7	mV
Input Offset Current (Note 4)				75			100	nA
Input Bias Current				1000			1000	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	−12 1	±13	+12 3	−12 1	±13	+12 3	V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA $T_A \geq 0°C$ $T_A \leq 0°C$		0.23	0.4 0.6		0.23	0.4 0.6	V V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$		1	10		1	10	μA
Differential Input Voltage				±5			±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	11.5		8	11.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	4.5		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119A and LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the J14 package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Note 7: Refer to RETS119X for LM119H/883 and LM119J/883 specifications, RETS119AX for LM119AH/883 and LM119AJ/883 specifications.

Absolute Maximum Ratings LM319A/319

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
ESD rating (1.5 kΩ in series with 100 pF)	800V

Operating Temperature Range LM319A, LM319	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM319A			LM319			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.5	1.0		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		20	40		80	200	nA
Input Bias Current	$T_A = 25°C$		150	500		250	1000	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	20	40		8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80			80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10			10	mV
Input Offset Current (Note 4)				300			300	nA
Input Bias Current				1000			1200	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	1	±13	3	1	±13	3	V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA		0.3	0.4		0.3	0.4	V
Differential Input Voltage				±5			±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	12.5		8	12.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	5		3	5	mA

Note 1: For supply voltages less than ±15 the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319A and LM319 is 85°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the N14 and J14 package is 100°C/W, junction to ambient. The thermal resistance of the M14 package is 115°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and $0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

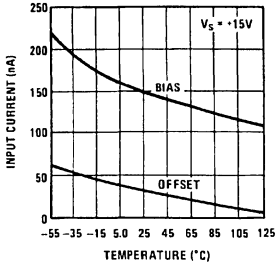
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

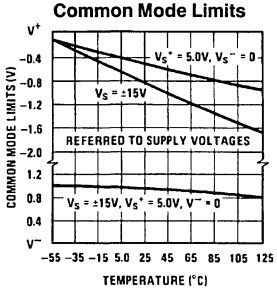
Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Typical Performance Characteristics LM119A/LM119/LM219

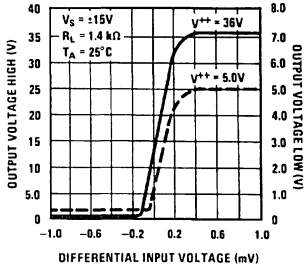
Input Currents



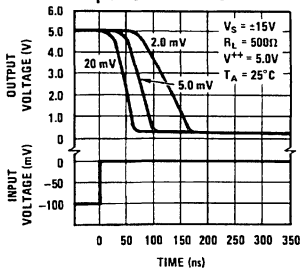
Common Mode Limits



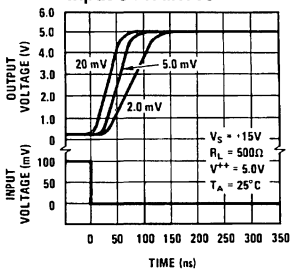
Transfer Function



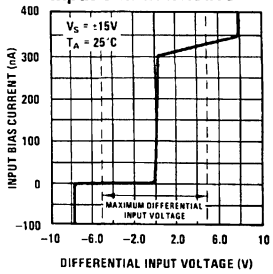
Response Time for Various Input Overdrives



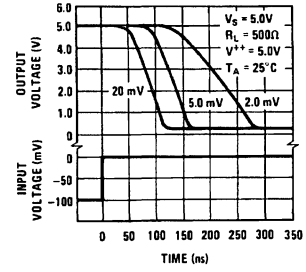
Response Time for Various Input Overdrives



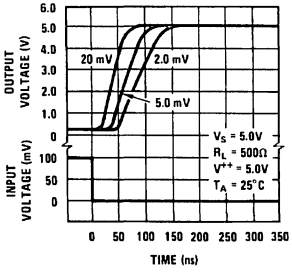
Input Characteristics



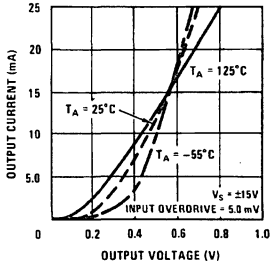
Response Time for Various Input Overdrives



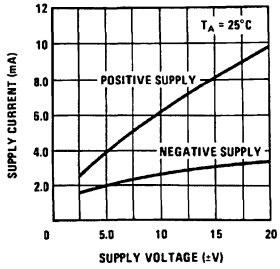
Response Time for Various Input Overdrives



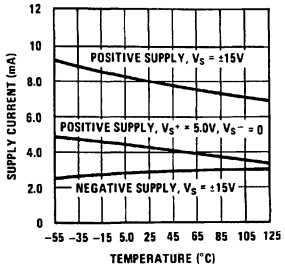
Output Saturation Voltage



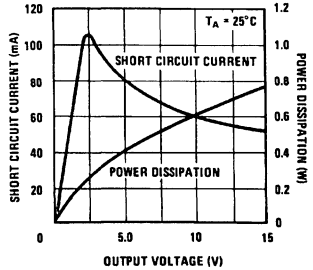
Supply Current



Supply Current



Output Limiting Characteristics



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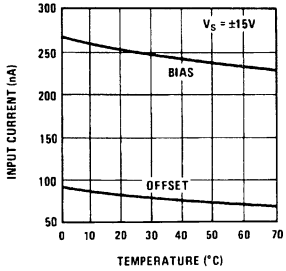
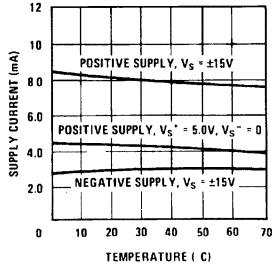
5

Typical Performance Characteristics LM319A, LM319

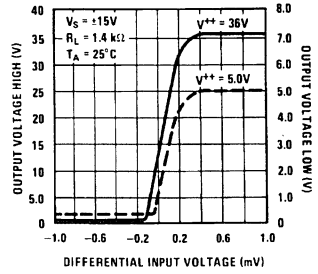
Input Currents



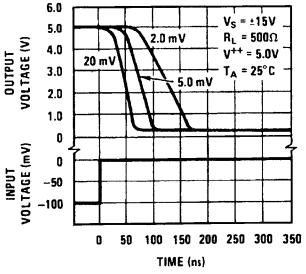
Supply Currents



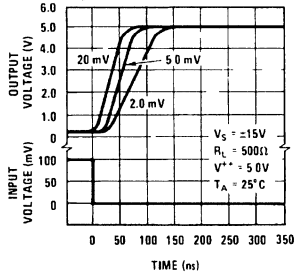
Transfer Function



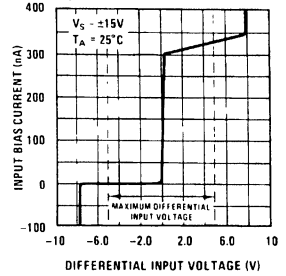
Response Time for Various Input Overdrives



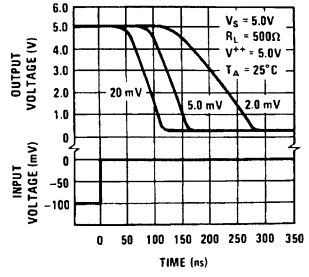
Response Time for Various Input Overdrives



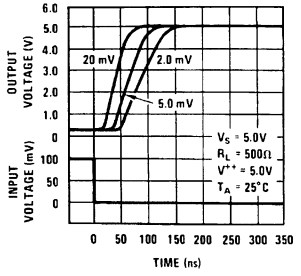
Input Characteristics



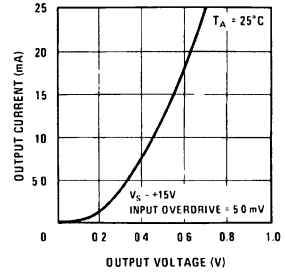
Response Time for Various Input Overdrives



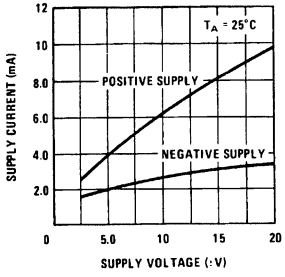
Response Time for Various Input Overdrives



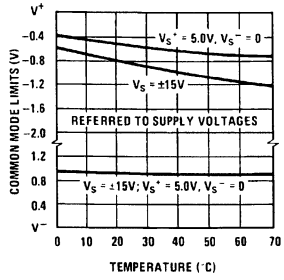
Output Saturation Voltage



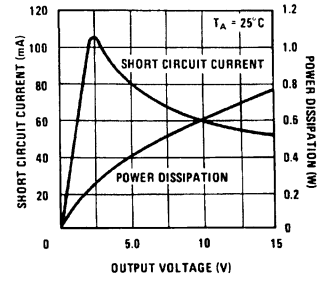
Supply Current



Common Mode Limits



Output Limiting Characteristics



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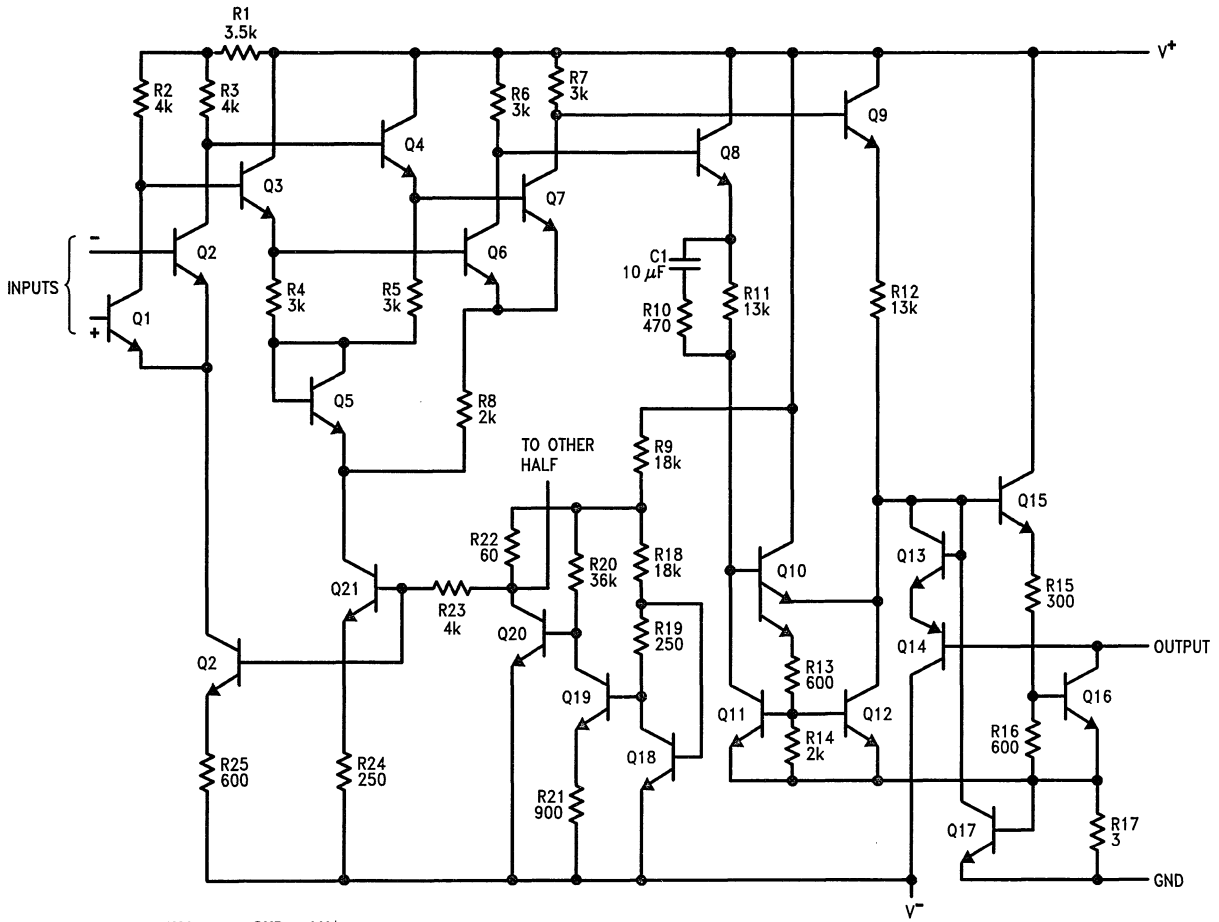


*Do not operate the LM119 with more than 16V between GND and V+

TL/H/5705–1

National Semiconductor

LM139/LM239/LM339/LM139A/LM239A/LM339A/ LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

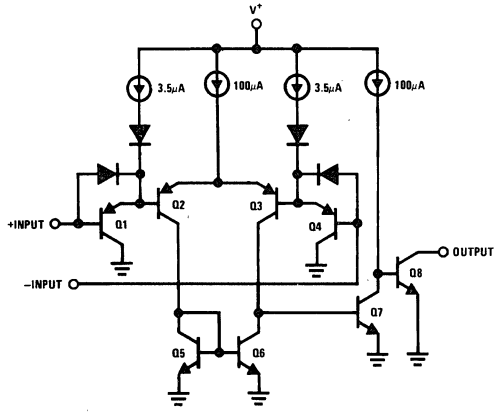
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide single supply voltage range of dual supplies
  LM139 series, 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ± 1 V_{DC} to ± 18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC}
  or ± 1 V_{DC} to ± 14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ± 5 nA
  and offset voltage ± 3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



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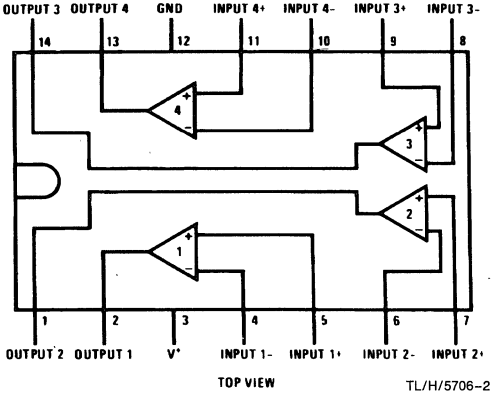
Dual-In-Line Package



TOP VIEW TL/H/5706–2

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 600V 600V

Electrical Characteristics ($V^+ = 5$ V_{DC}, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30$ V_{DC} (LM3302, $V^+ = 28$ V_{DC}) (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	$R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ V_{DC})					1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5	mA_{DC}
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15$ V_{DC}, $V_O = 1$ V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ,		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} = 1$ V_{DC}, $V_{IN(+)} = 0$, $V_O \leq 1.5$ V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}

Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			±4.0			±4.0			±9.0			±9.0		±9	±15			±40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±100			±150			±100			±150		±50	±200			±300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$			$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a valve greater than $-0.3\ V_{DC}$ (at 25°)C.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

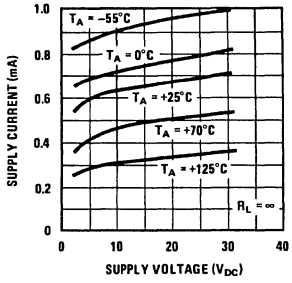
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, V^+ from $5\ V_{DC}$ to $28\ V_{DC}$.

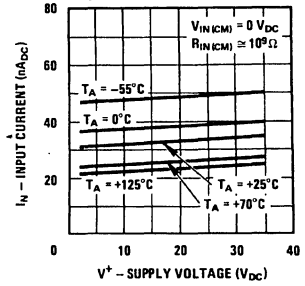
Note 10: Refer to RETS139AX for LM139AJ military specifications and to RETS139X for LM139J military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

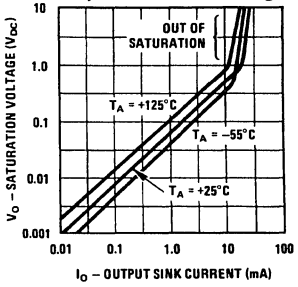
Supply Current



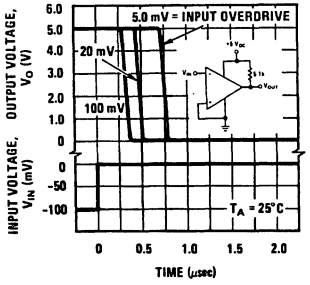
Input Current



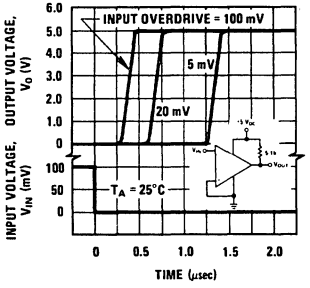
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



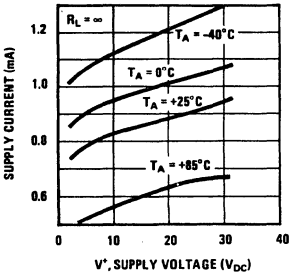
Response Time for Various Input Overdrives—Positive Transition



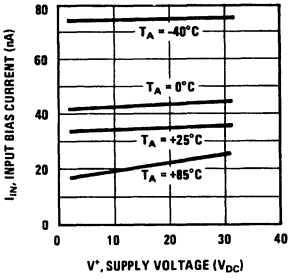
TL/H/5706–6

Typical Performance Characteristics LM2901

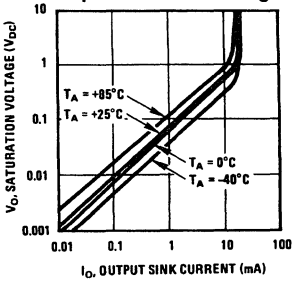
Supply Current



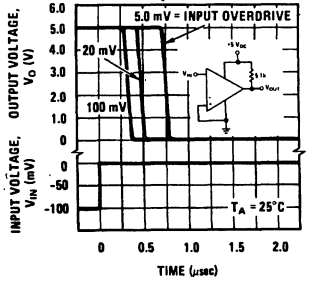
Input Current



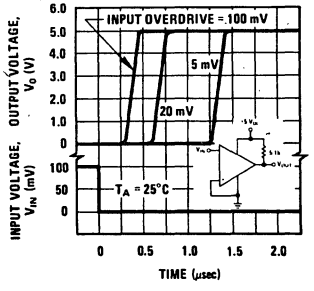
Output Saturation Voltage



Response Time for Various Input Overdrives-Negative Transition



Response Time for Various Input Overdrives-Positive Transition



TL/H/5706–7

5

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

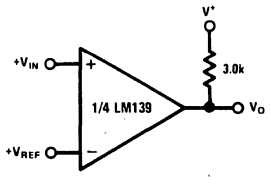
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

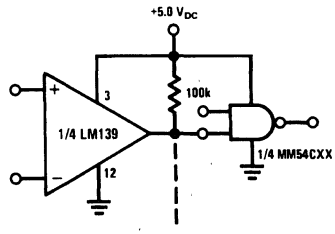
Typical Applications ($V^+ = 5.0\ V_{DC}$)

Basic Comparator



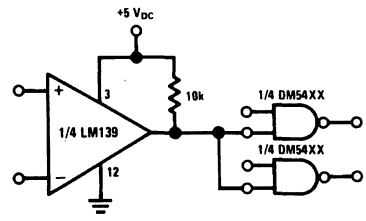
TL/H/5706–3

Driving CMOS



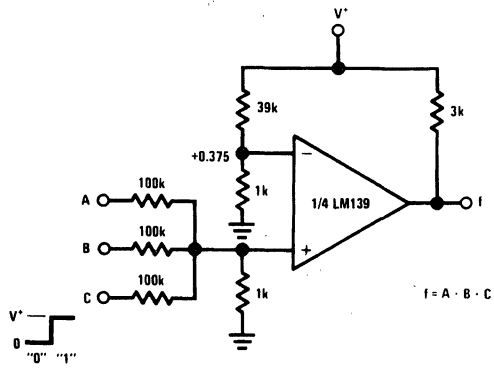
TL/H/5706–4

Driving TTL



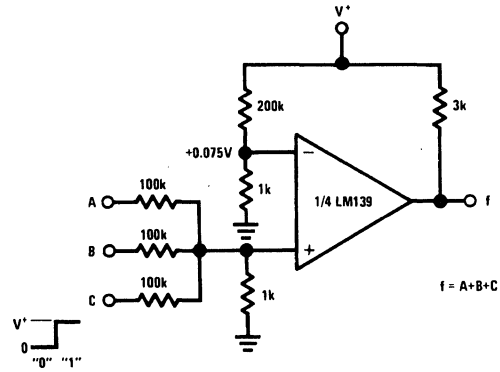
TL/H/5706–5

AND Gate



TL/H/5706–8

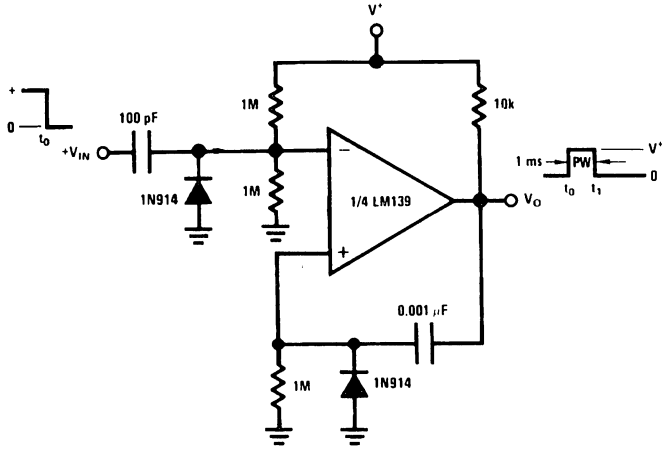
OR Gate



TL/H/5706–9

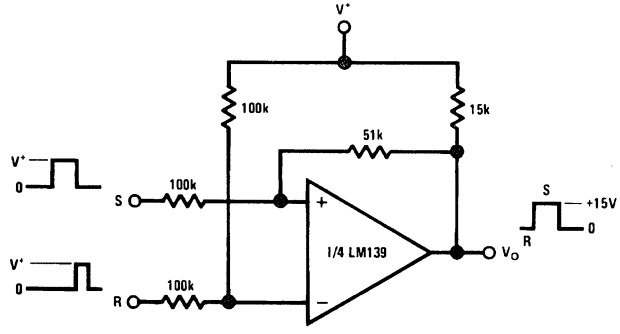
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

One-Shot Multivibrator



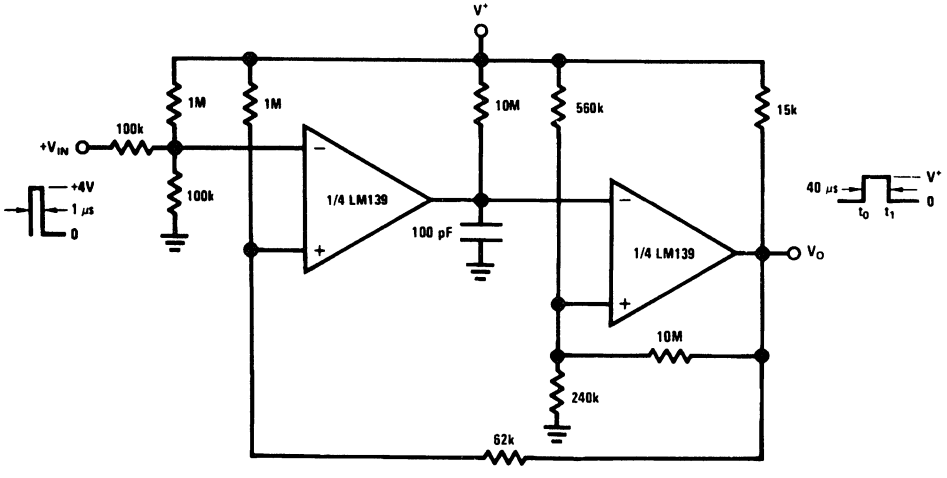
TL/H/5706–10

Bi-Stable Multivibrator



TL/H/5706–11

One-Shot Multivibrator with Input Lock Out

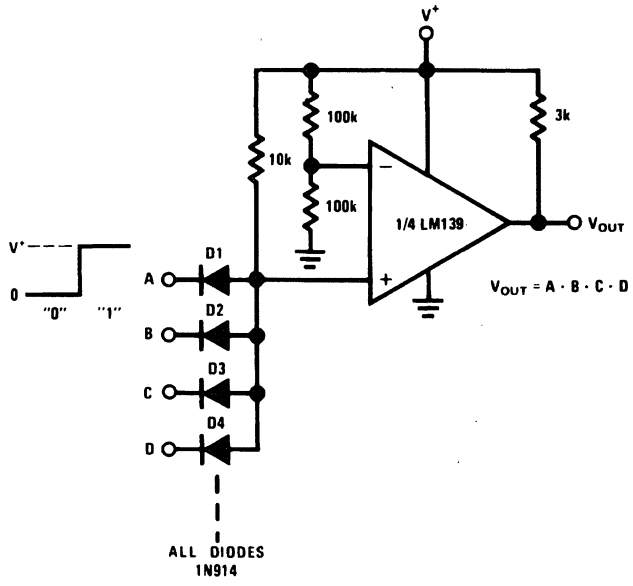


TL/H/5706–12

5

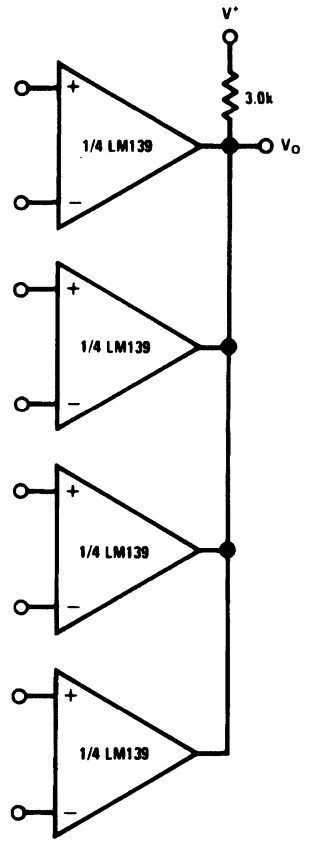
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Large Fan-In AND Gate



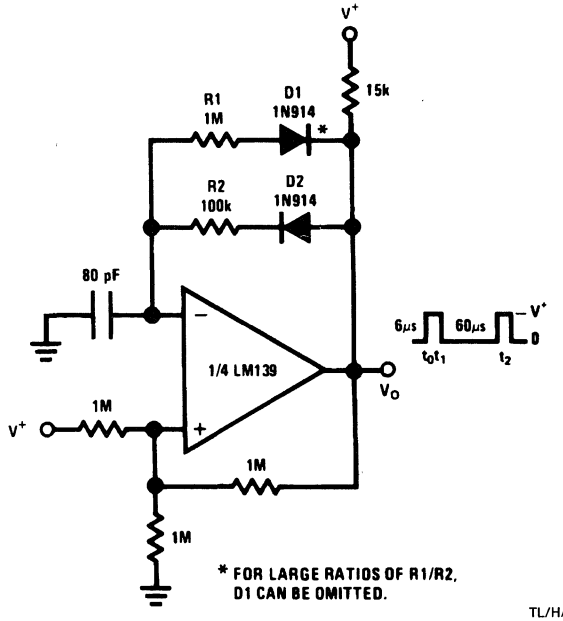
TL/H/5706–13

ORing the Outputs



TL/H/5706–15

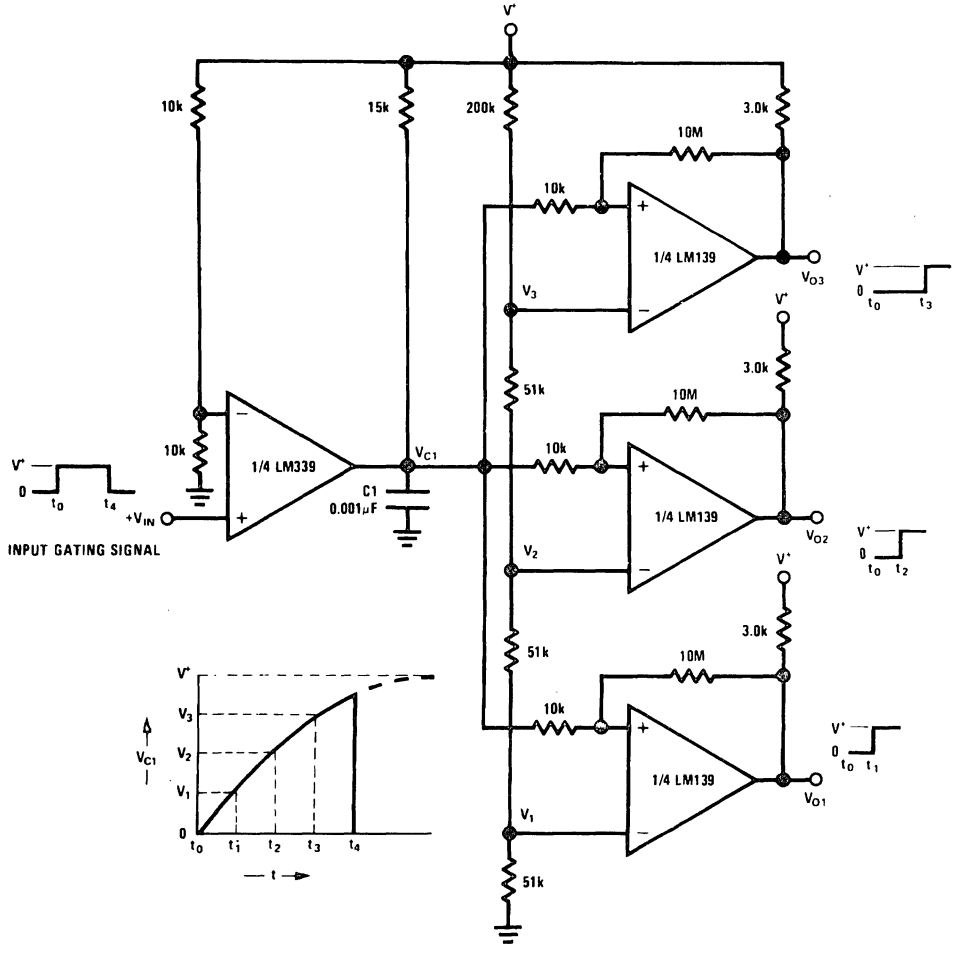
Pulse Generator



TL/H/5706–17

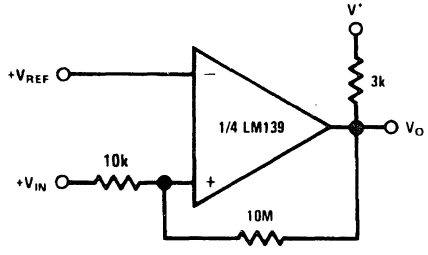
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Time Delay Generator



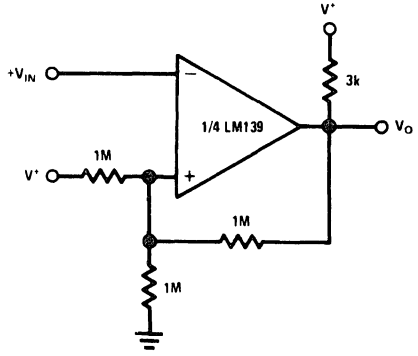
TL/H/5706–14

Non-Inverting Comparator with Hysteresis



TL/H/5706–18

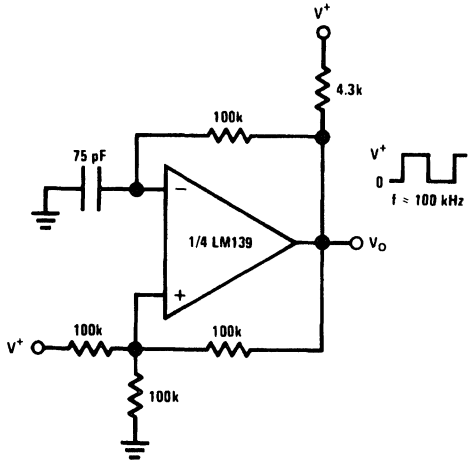
Inverting Comparator with Hysteresis



TL/H/5706–19

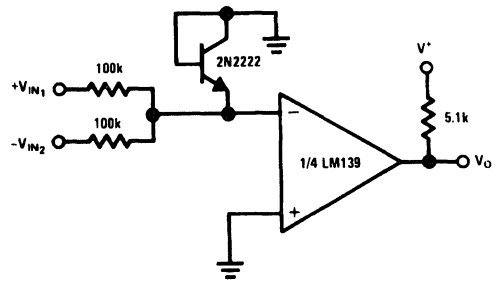
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Squarewave Oscillator



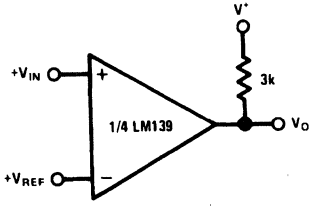
TL/H/5706–16

Comparing Input Voltages of Opposite Polarity



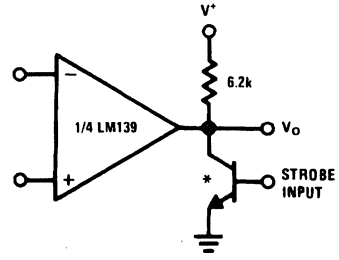
TL/H/5706–20

Basic Comparator



TL/H/5706–21

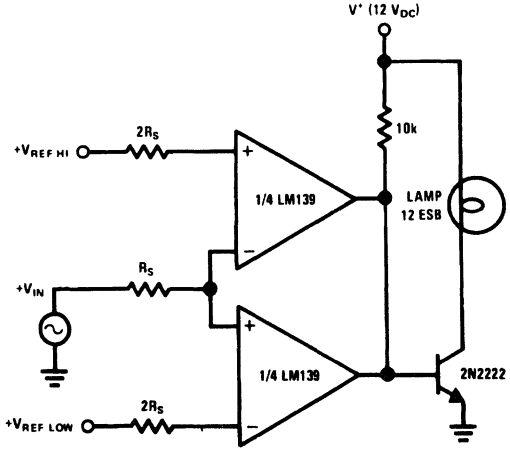
Output Strobing



TL/H/5706–22

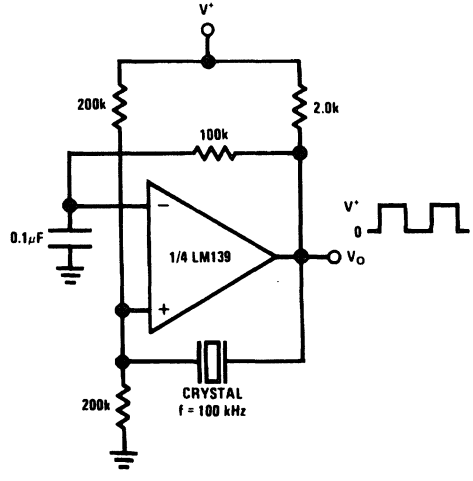
*Or open-collector logic gate without pull-up resistor

Limit Comparator



TL/H/5706–24

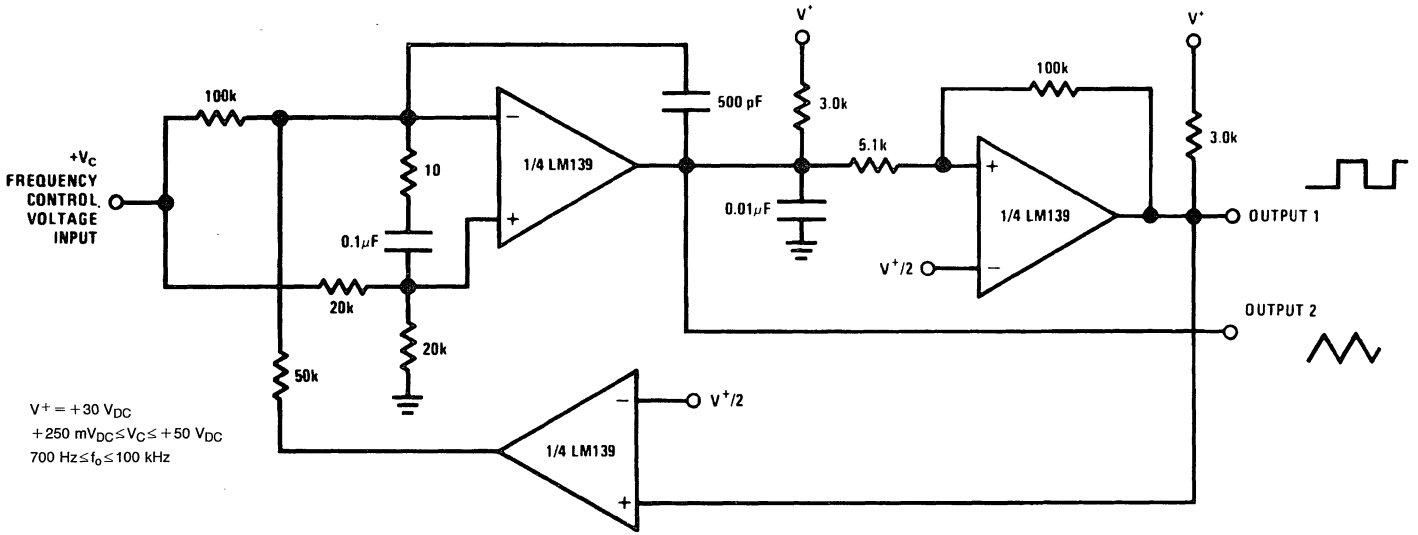
Crystal Controlled Oscillator



TL/H/5706–25

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

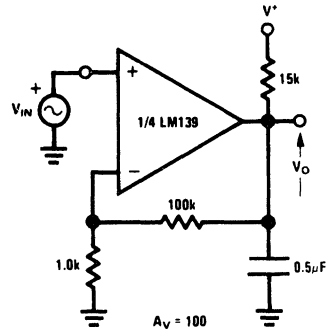
Two-Decade High-Frequency VCO



TL/H/5706–23

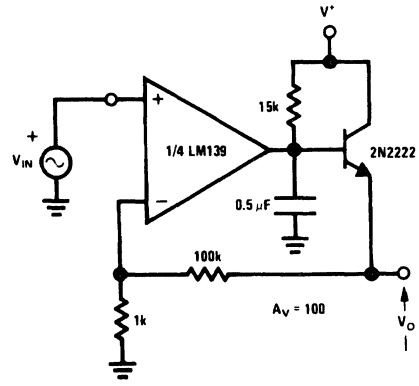
Typical Applications ($V^+ = 5\ V_{DC}$) (Continued)

Low Frequency Op Amp



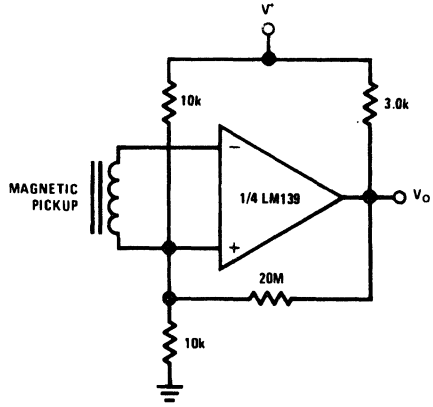
TL/H/5706–26

Low Frequency Op Amp
(V_O = 0V for V_{IN} = 0V)



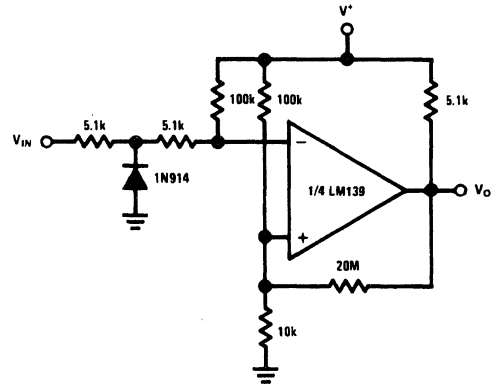
TL/H/5706–27

Transducer Amplifier



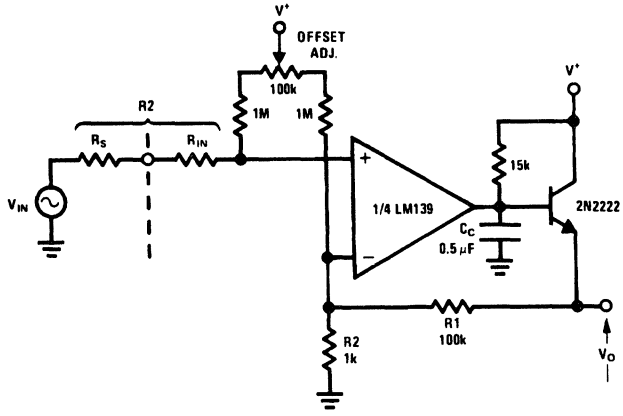
TL/H/5706–28

Zero Crossing Detector (Single Power Supply)



TL/H/5706–30

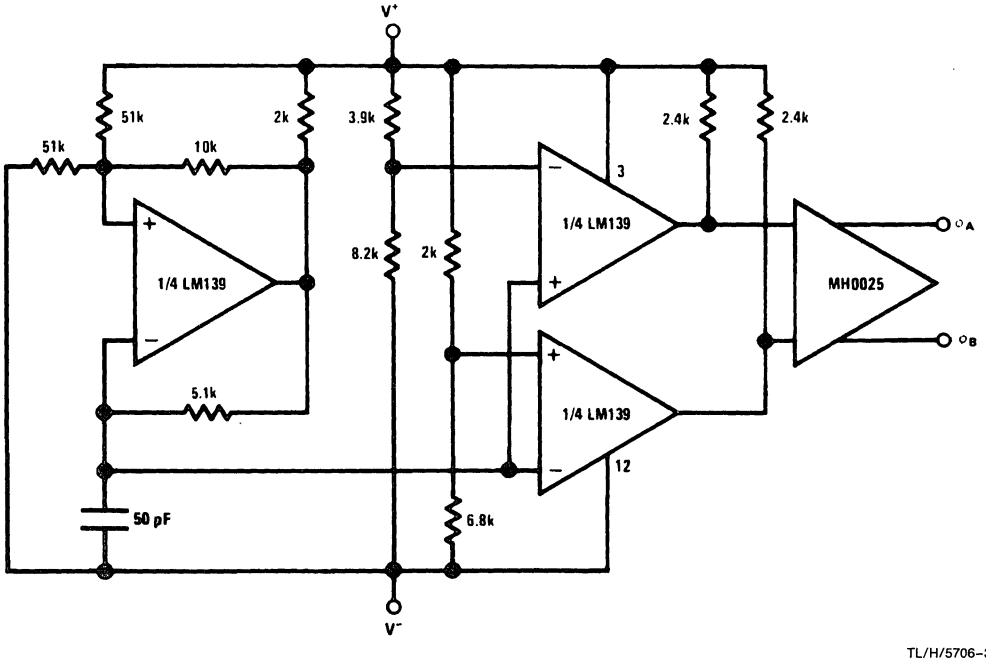
Low Frequency Op Amp with Offset Adjust



TL/H/5706–29

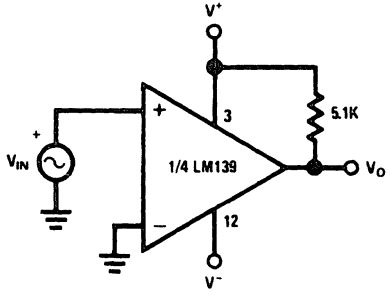
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

MOS Clock Driver



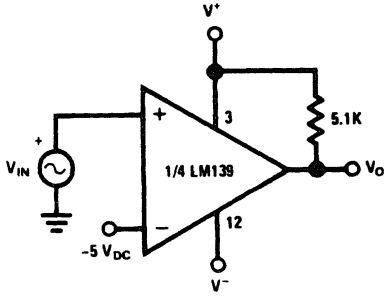
TL/H/5706–31

Zero Crossing Detector



TL/H/5706–32

Comparator With a Negative Reference



TL/H/5706–33

5

National Semiconductor

LM160/LM260/LM360 High Speed Differential Comparator

General Description

The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

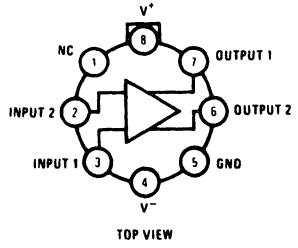
Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

Features

- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Connection Diagrams

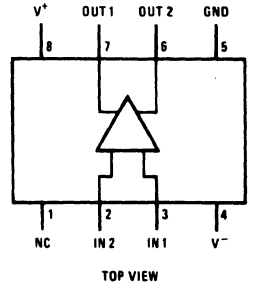
Metal Can Package



TL/H/5707–4

Order Number LM160H, LM260H or LM360H
See NS Package Number H08C

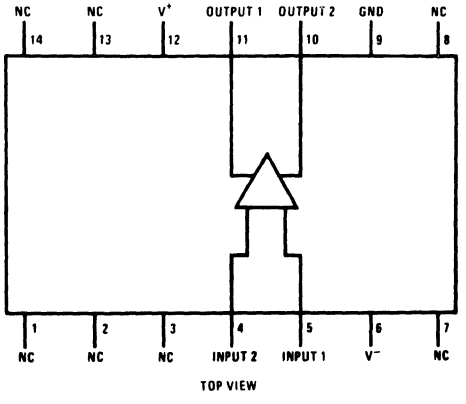
Dual-In-Line Package



TL/H/5707–5

Order Number LM360M or LM360N
See NS Package Number M08A or N08E

Dual-In-Package



TL/H/5707–6

Order Number LM160J-14, LM360J-14 or LM360N-14
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 7)

Positive Supply Voltage	+8V
Negative Supply Voltage	−8V
Peak Output Current	20 mA
Differential Input Voltage	±5V
Input Voltage	$V^+ \geq V_{IN} \geq V^-$
ESD rating is to be determined.	

Operating Temperature Range	
LM160	−55°C to +125°C
LM260	−25°C to +85°C
LM360	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			0.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 1, 6)		13	25	ns
	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 2, 6)		12	20	ns
	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 3, 6)		14		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm 6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\ \mu A$, $V_S = \pm 4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm 6.5V$		−9	−16	mA

Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Note 4: Typical thermal impedances are as follows:

Cavity DIP (J):	θ_{jA}	135°C/W	Header (H)	θ_{jA}	165°C/W	(Still Air)
Molded DIP (N):	θ_{jA}	130°C/W			67°C/W	(400 LF/min Air Flow)
				θ_{jC}	25°C/W	

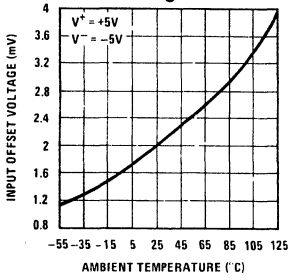
Note 5: The device may be damaged if used beyond the maximum ratings.

Note 6: Measurements are made in AC Test Circuit, Fanout = 1

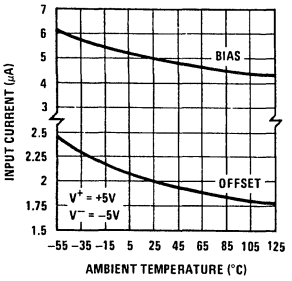
Note 7: Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

Typical Performance Characteristics

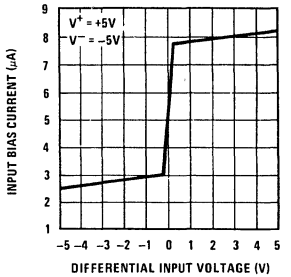
Offset Voltage



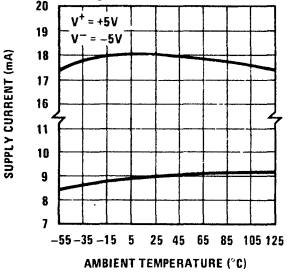
Input Currents vs Ambient Temperature



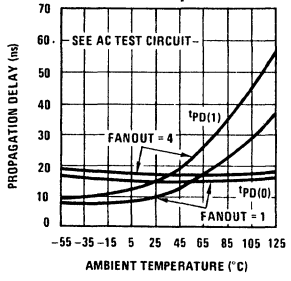
Input Characteristics



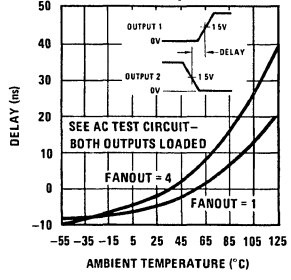
Supply Current vs Ambient Temperature



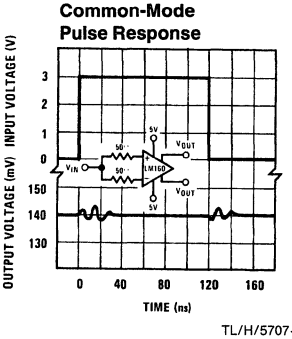
Propagation Delay vs Ambient Temperature



Delay of Output 1 With Respect to Output 2 vs Ambient Temperature

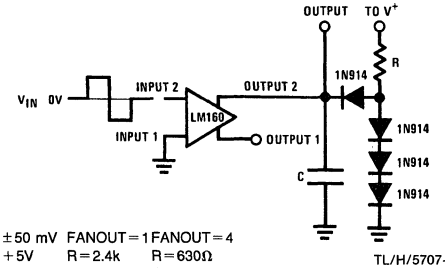


Common-Mode Pulse Response



TL/H/5707–2

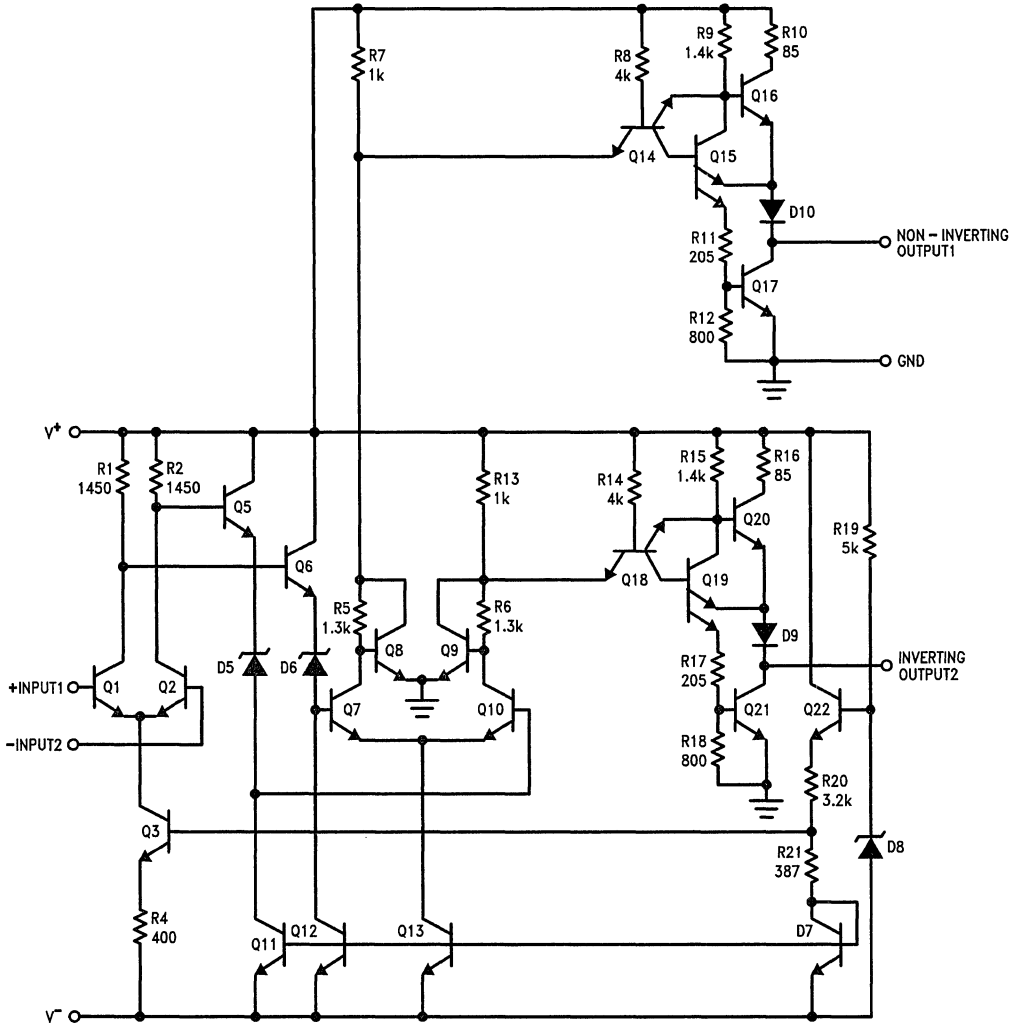
AC Test Circuit



V_{IN} = ±50 mV	FANOUT = 1	FANOUT = 4
V^+ = +5V	R = 2.4k	R = 630Ω
V^- = −5V	C = 15 pF	C = 30 pF

TL/H/5707–3

Schematic Diagram



TL/H/5707–1

National Semiconductor

LM161/LM261/LM361
High Speed Differential Comparators

General Description

The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

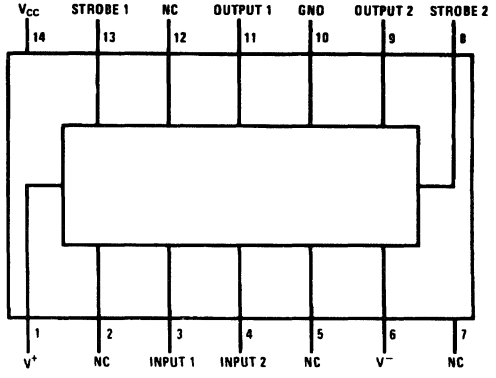
Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

- Independent strobes
- Guaranteed high speed — 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies — ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Connection Diagrams

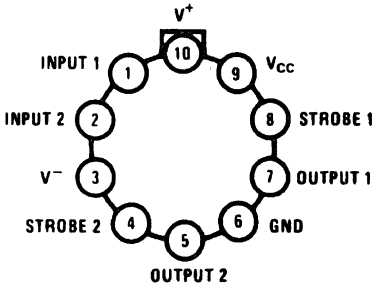
Dual-In-Line Package



TL/H/5708–2

Top View
Order Number LM161J, LM261J, LM361J, LM361M or LM361N
See NS Package Number J14A, M14A or N14A

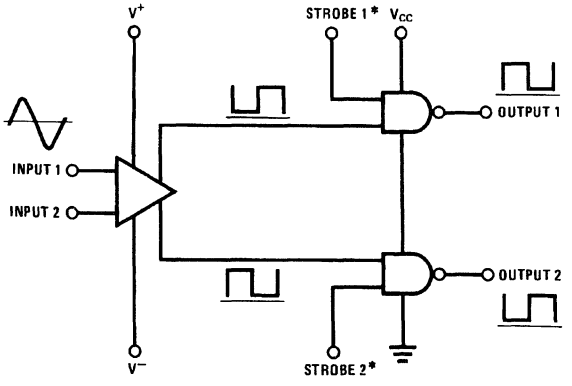
Metal Can Package



TL/H/5708–3

Order Number LM161H, LM261H or LM361H
See NS Package H10C

Logic Diagram



*Output is low when current is drawn from strobe pin.

TL/H/5708–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	−55°C to +125°C
LM261	−25°C to +85°C
LM361	0°C to +70°C
Lead Temp. (Soldering, 10 seconds)	260°C
For Any Device Lead Below V^-	0.3V

Operating Conditions

	Min	Typ	Max
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V

ESD rating to be determined.

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5	20		10	30	μA μA
Input Offset Current	$T_A = 25°C$		2	3		2	5	μA μA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -0.5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			0.4			0.4	V
Strobe Input "1" Current (Output Enabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	μA
Strobe Input "0" Current (Output Disabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 0.4V$			−1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			0.8			0.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	−18		−55	−18		−55	mA

Electrical Characteristics (Continued)

($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						20	mA
Transient Response	V_{IN} = 50 mV overdrive (Note 3)							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

Note 1: The device may be damaged by use beyond the maximum ratings.

Note 2: Typical thermal impedances are as follows:

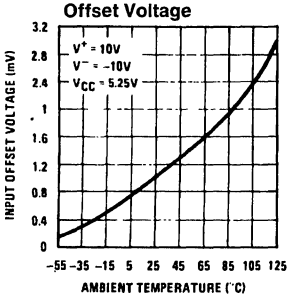
	H Package	J Package	N Package
θ_{jA}	165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow)	112°C/W	105°C/W
θ_{jC}	25°C/W		

Note 3: Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

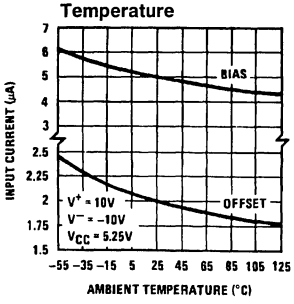
Note 4: Refer to RETS161X for LM161H and LM161J military specifications.

Typical Performance Characteristics

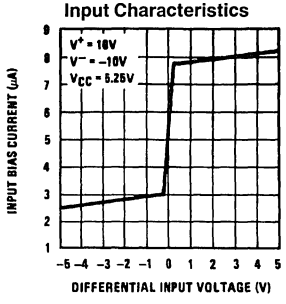
Offset Voltage



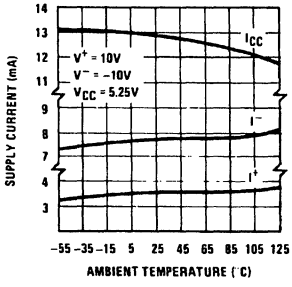
Input Currents vs Ambient Temperature



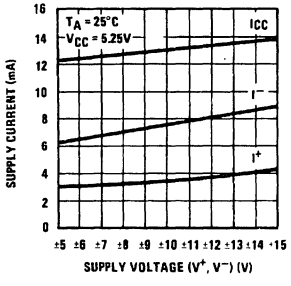
Input Characteristics



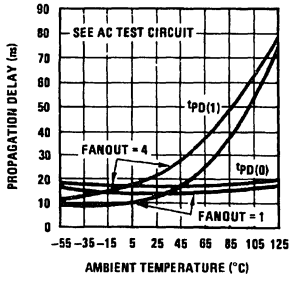
Supply Current vs Ambient Temperature



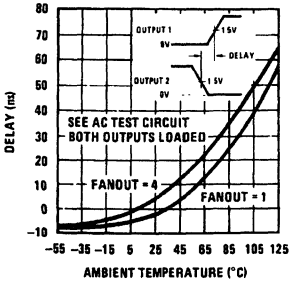
Supply Current vs Supply Voltage



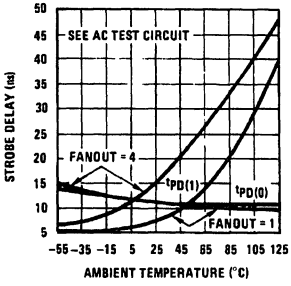
Propagation Delay vs Ambient Temperature



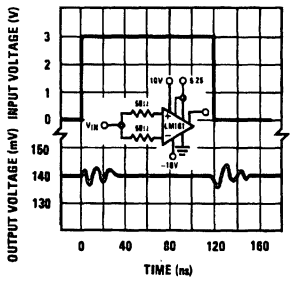
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Strobe Delay vs Ambient Temperature

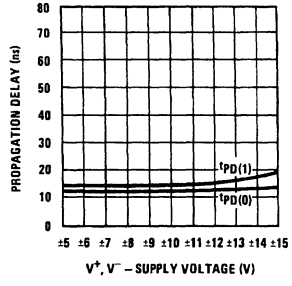


Common-Mode Pulse Response



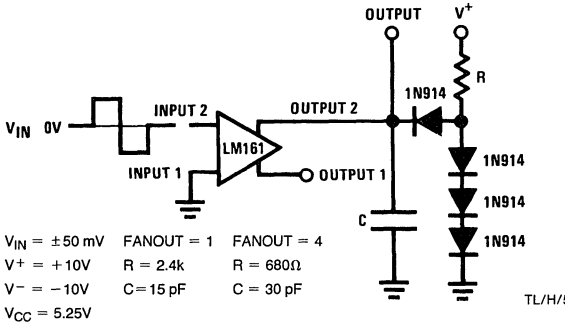
TL/H/5708–5

Propagation Delay vs Supply Voltage



TL/H/5708–7

AC Test Circuit

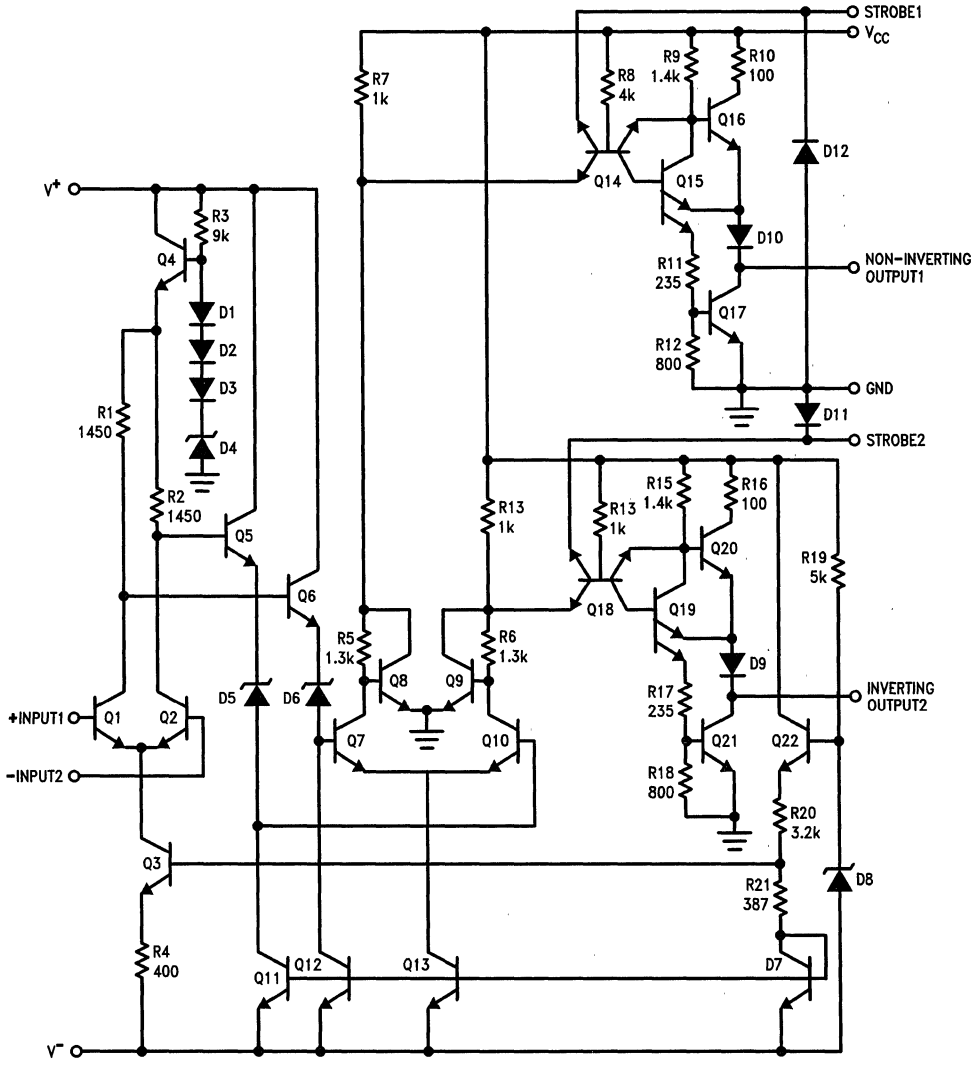


V_{IN} = ±50 mV	FANOUT = 1	FANOUT = 4
V+ = +10V	R = 2.4k	R = 680Ω
V− = −10V	C = 15 pF	C = 30 pF
V_{CC} = 5.25V		

TL/H/5708–6

Schematic Diagram

LM161



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R10, R16: 85
R11, R17: 205

National Semiconductor

LM193/LM293/LM393, LM193A/LM293A/LM393A, LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

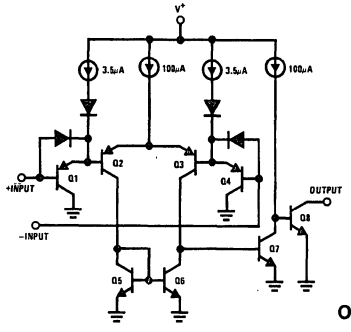
Features

- Wide single supply
  Voltage range 2.0 V_{DC} to 36 V_{DC}
  or dual supplies ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and maximum offset voltage ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

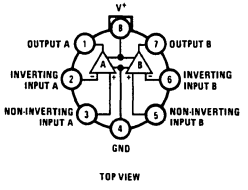
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature

Schematic and Connection Diagrams

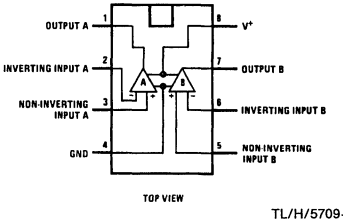


Metal Can Package



Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package



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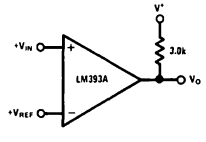
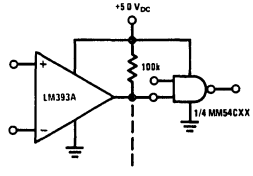
Order Number LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM393AN or LM2903N
See NS Package Number J08A, M08A or N08E

Typical Applications ($V^+ = 5.0\ V_{DC}$)

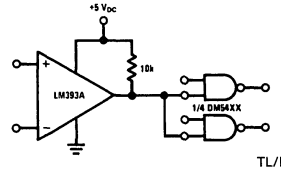
Basic Comparator



Driving CMOS



Driving TTL



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5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Input Current ($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous

Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 1300V

Electrical Characteristics ($V^+ = 5$ V_{DC}, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±1.0	±2.0		±1.0	±5.0		±1.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (Note 5)		25	100		25	250		25	100		25	250		25	250	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ V_{CM} = 0V		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5.0	±50	nA_{DC}
Input Common Mode Voltage Range	V^+ = 30 V_{DC} (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on All Comparators, $R_L = \infty$ on All Amps, $V^+ = 36$ V_{DC}		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1.0 2.5	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15$ V_{DC} V_O = 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC} V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ		300			300			300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ (Note 7)		1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O \leq 1.5$ V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1$ V_{DC}, $V_O = 5$ V_{DC}		0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5\ V_{DC}$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			±4.0			±4.0			±9			±9		±9	±15	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±100			±150			±100			±150		±50	±200	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA_{DC}
Input Common Mode Voltage Range	$V^+ = 30\ V_{DC}$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA,			700			700			700			700		400	700	mV_{DC}
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN(+)} = 1\ V_{DC}$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V_{DC}

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36 V_{DC} without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

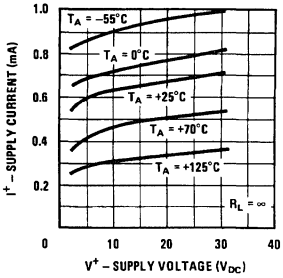
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$), at 25°C.

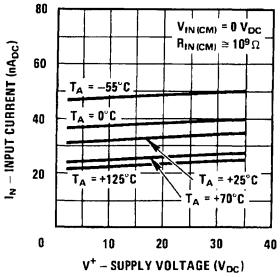
Note 10: Refer to RETS193AX for LM193AH/military specifications and to RETS193X for LM193H/military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

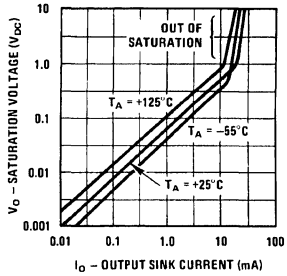
Supply Current



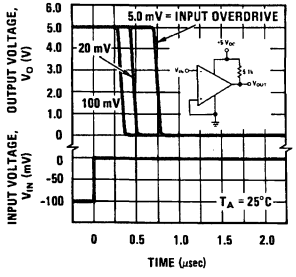
Input Current



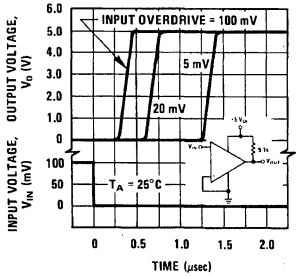
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



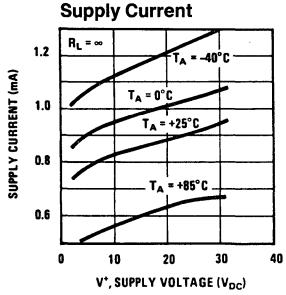
Response Time for Various Input Overdrives—Positive Transition



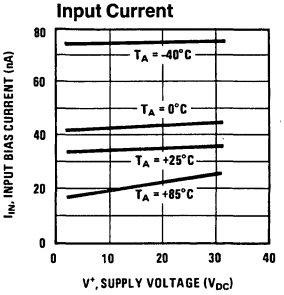
TL/H/5709–3

Typical Performance Characteristics LM2903

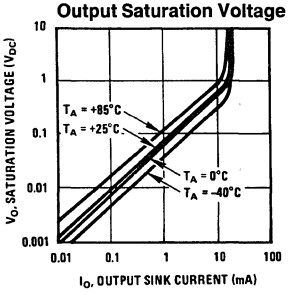
Supply Current



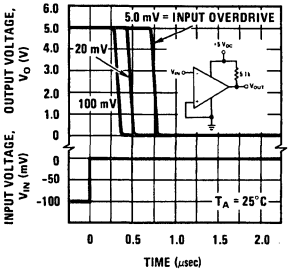
Input Current



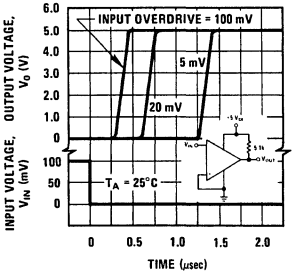
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

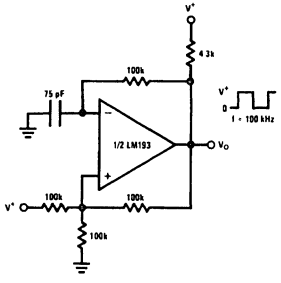
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

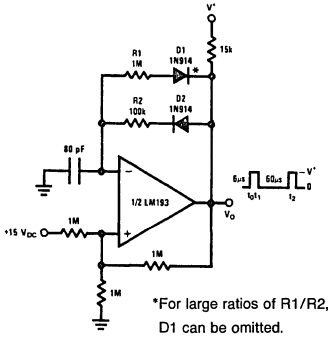
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\Omega\ r_{SAT}$ of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Squarewave Oscillator

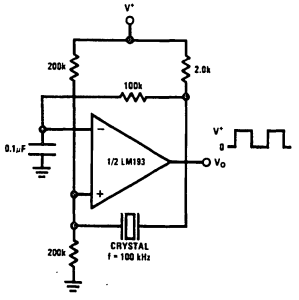


Pulse Generator

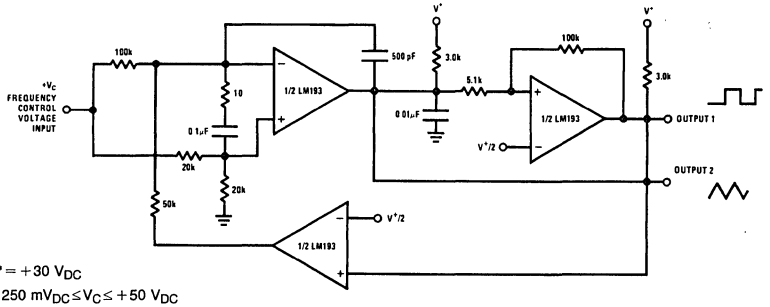


*For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator



Two-Decade High-Frequency VCO



$V^+ = +30\ V_{DC}$

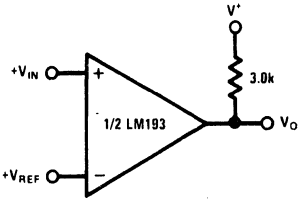
$+250\ mV_{DC} \leq V_C \leq +50\ V_{DC}$

$700\ Hz \leq f_o \leq 100\ kHz$

TL/H/5709–5

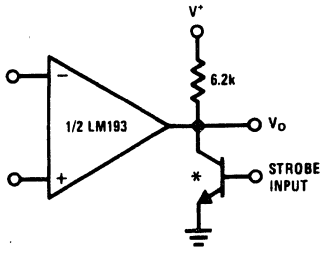
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Basic Comparator



TL/H/5709–6

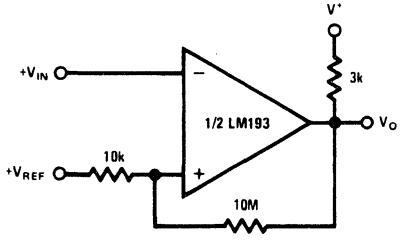
Output Strobing



* OR LOGIC GATE WITHOUT PULL-UP RESISTOR

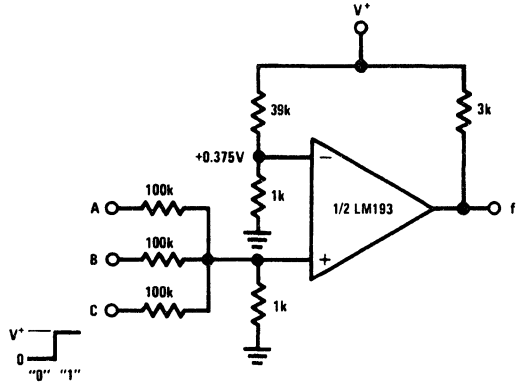
TL/H/5709–11

Non-Inverting Comparator with Hysteresis



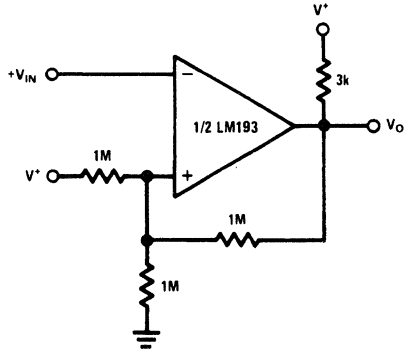
TL/H/5709–9

AND Gate



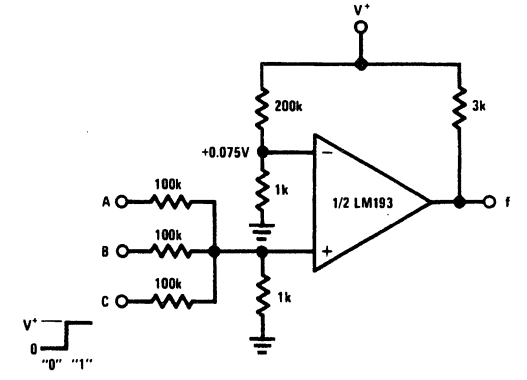
TL/H/5709–12

Inverting Comparator with Hysteresis



TL/H/5709–10

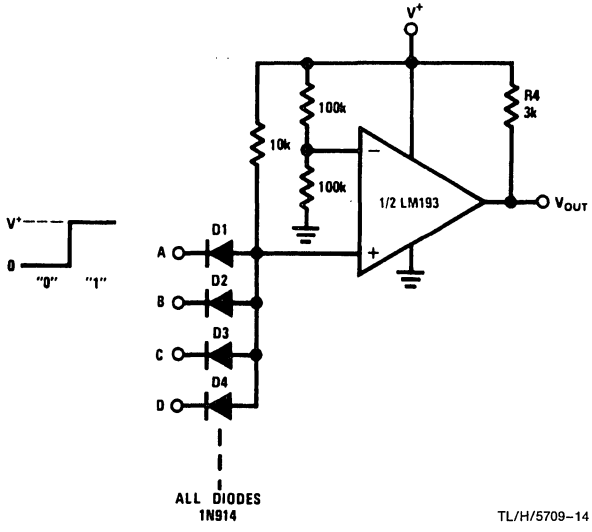
OR Gate



TL/H/5709–13

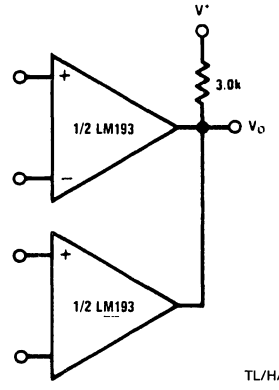
Typical Applications (Continued) ($V^+ = V_{DC}$)

Large Fan-in AND Gate



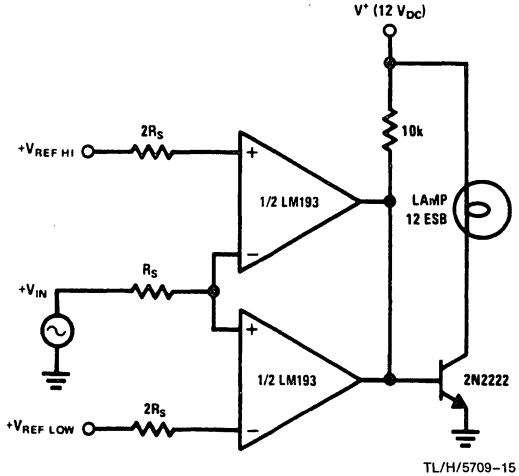
TL/H/5709–14

ORing the Outputs



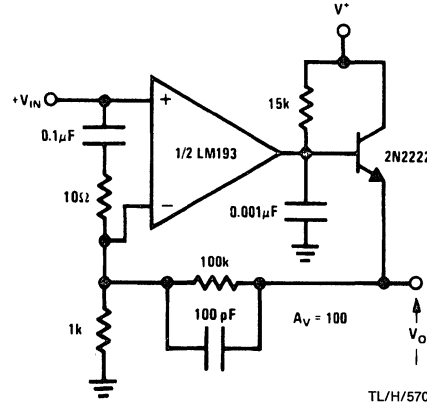
TL/H/5709–17

Limit Comparator



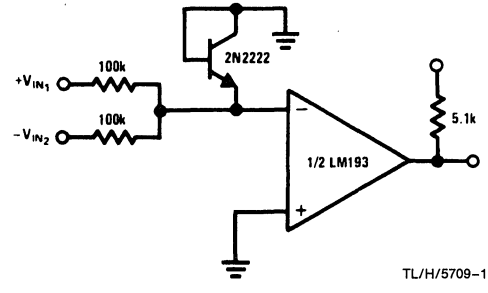
TL/H/5709–15

Improved Op Amp



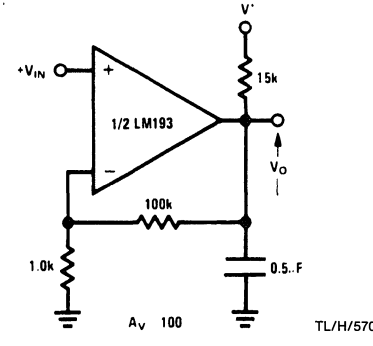
TL/H/5709–18

Comparing Input Voltages of Opposite Polarity



TL/H/5709–16

Low Frequency Op Amp

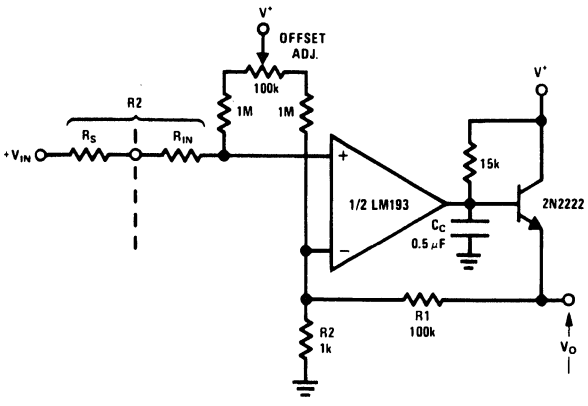


TL/H/5709–19

5

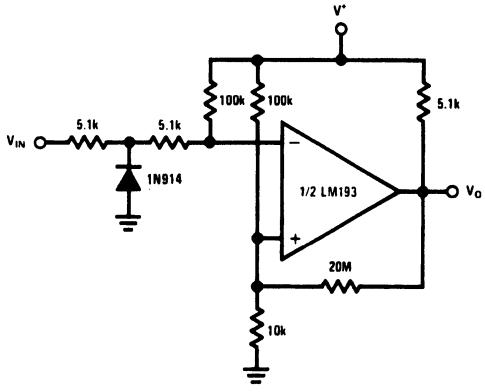
Typical Applications (Continued) ($V^+ = V_{DC}$)

Low Frequency Op Amp with Offset Adjust



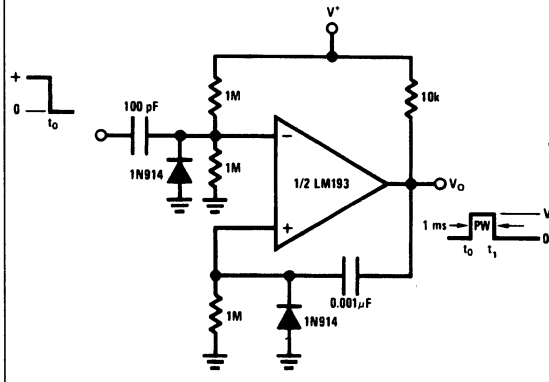
TL/H/5709–20

Zero Crossing Detector (Single Power Supply)



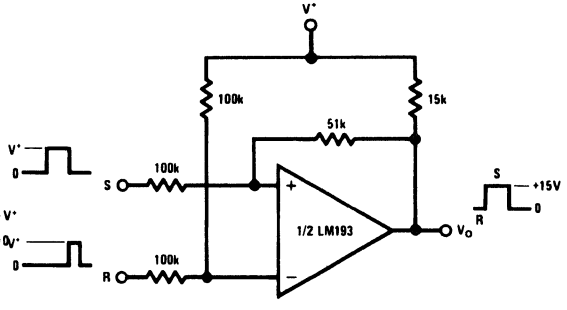
TL/H/5709–21

One-Shot Multivibrator



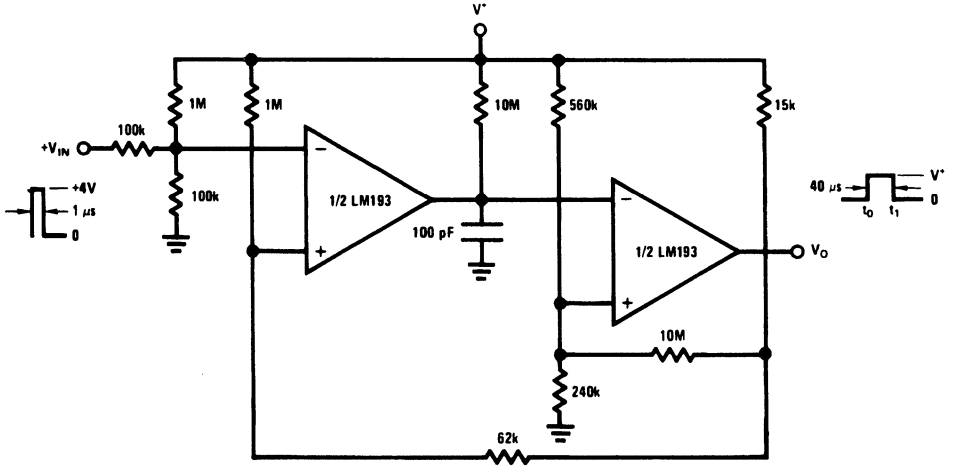
TL/H/5709–22

Bi-Stable Multivibrator



TL/H/5709–24

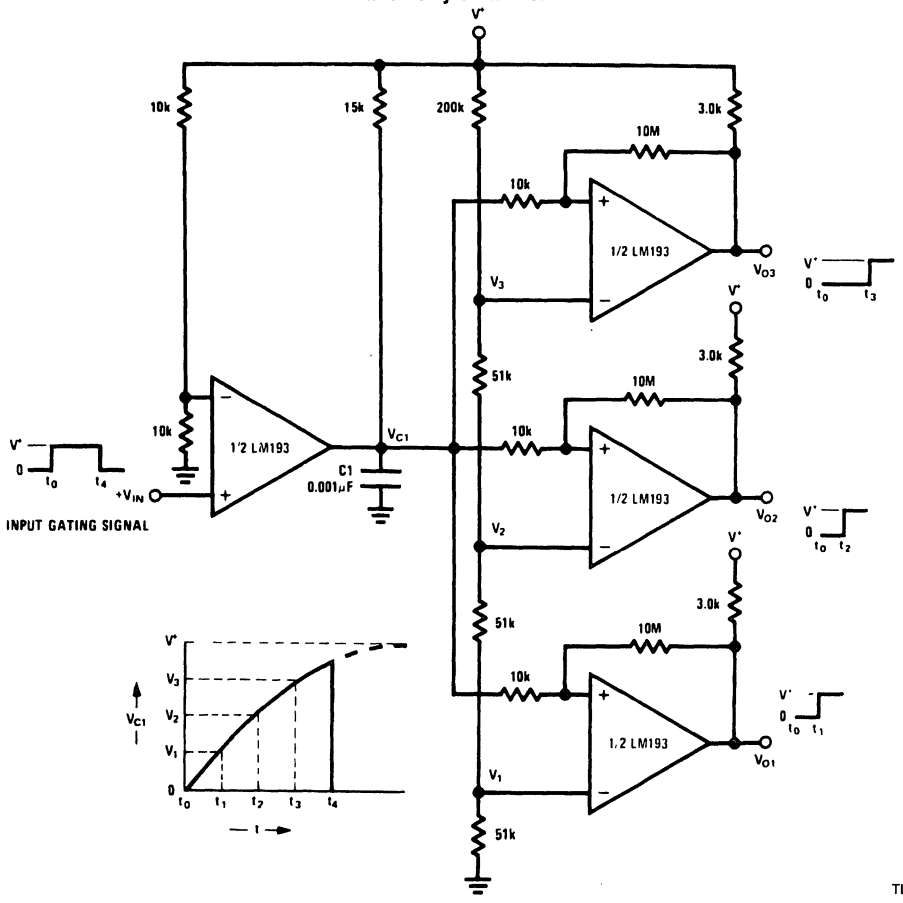
One-Shot Multivibrator with Input Lock Out



TL/H/5709–23

Typical Applications (Continued) ($V^+ = V_{DC}$)

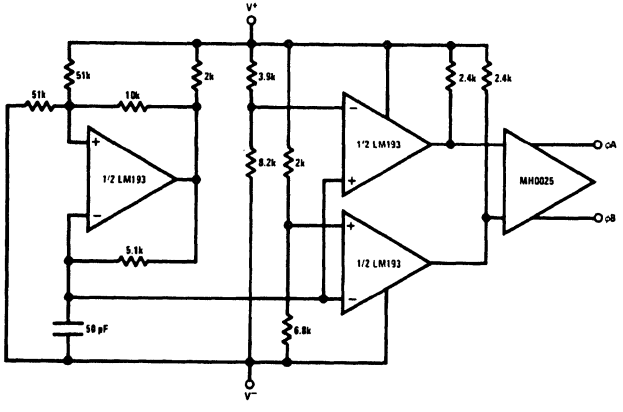
Time Delay Generator



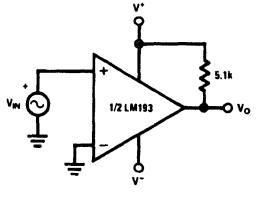
TL/H/5709–7

Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

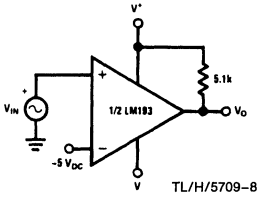
MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference



TL/H/5709–8

National Semiconductor

LM710/LM710C Voltage Comparator

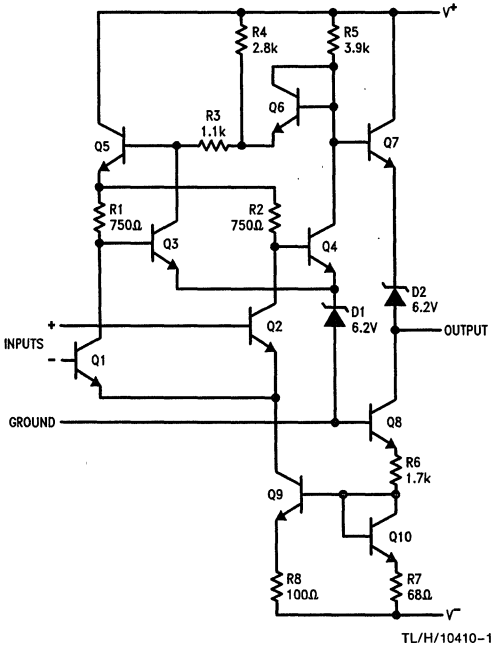
General Description

The LM710 series are high-speed voltage comparators intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

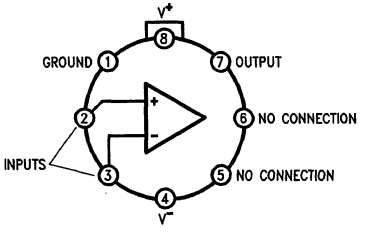
The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A/D converters or go, no-go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the units suggests them for applications replacing relatively simple discrete component circuitry.

Schematic and Connection Diagrams



TL/H/10410–1

Metal Can Package



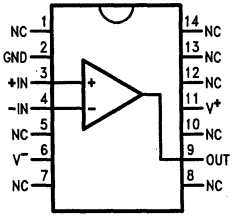
TL/H/10410–2

Top View

Note: Pin 4 is connected to case.

Order Number LM710H or LM710CH
See NS Package Number H08C

Dual-In-Line Package



TL/H/10410–3

Top View

Order Number LM710CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage	+14V
Negative Supply Voltage	−7V
Peak Output Current	10 mA
Output Short Circuit Duration	10 seconds
Differential Input Voltage	±5V
Input Voltage	±7V

Power Dissipation	
TO-99 (Note 1)	700 mW
Plastic Dual-In-Line Package (Note 2)	950 mW
Operating Temperature Range	
LM710	−55°C to +125°C
LM710C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $T_A = 25°C$		0.6	2.0		1.6	5.0	mV
Input Offset Current	$V_{OUT} = 1.4V$, $T_A = 25°C$		0.75	3.0		1.8	5.0	μA
Input Bias Current	$T_A = 25°C$		13	20		16	25	μA
Voltage Gain	$T_A = 25°C$	1250	1700		1000	1500		
Output Resistance	$T_A = 25°C$		200			200		Ω
Output Sink Current	$V_{OUT} = 0$, $T_A = 25°C$ $\Delta V_{IN} \geq 5$ mV $\Delta V_{IN} \geq 10$ mV	2.0	2.5		1.6	2.5		mA mA
Response Time	$T_A = 25°C$ (Note 4)		40			40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$ $R_S \leq 50\Omega$		3.0	10		5.0	20	μV/°C
Input Offset Current	$T_A = T_{A\,MAX}$ $T_A = T_{A\,MIN}$		0.25 1.8	3.0 7.0			7.5 7.5	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		5.0 15	25 75		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = T_{MIN}$		27	45		25	40	μA
Input Voltage Range	$V^- = -7V$	±5.0			±5.0			V
Common-Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			V/V
Positive Output Level	-5 mA $\leq I_{OUT} \leq 0$ $V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	2.5	3.2	4.0	2.5	3.2	4.0	V V
Negative Output Level	$V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	−1.0	−0.5	0	−1.0	−0.5	0	V V
Output Sink Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 0$ $T_A = 125°C$ $T_A = -55°C$	0.5 1.0	1.7 2.3					mA mA
	$V_{IN} \geq 10$ mV, $V_{OUT} = 0$ $0°C \leq T_A \leq +70°C$				0.5			mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Positive Supply Current	$V_{IN} \geq 5$ mV		5.2	9.0				mA
	$V_{IN} \geq 10$ mV					5.2	9.0	mA
Negative Supply Current	$V_{IN} \geq 5$ mV		4.6	7.0				mA
	$V_{IN} \geq 10$ mV					4.6	7.0	mA
Power Consumption	$I_{OUT} = 0$							
	$V_{IN} \geq 5$ mV		90	150				mW
	$V_{IN} \geq 10$ mV						150	mW

Note 1: Rating applies for ambient temperatures of 25°C; derate linearly at 5.6 mW/°C for ambient temperatures above 25°C.

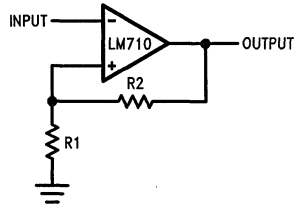
Note 2: Derate linearly at 9.5 mW/°C for ambient temperatures above 25°C.

Note 3: These specifications appy for $V^+ = 12V$, $V^- = -6V$, $-55°C \leq T_A \leq +125°C$ for LM710 and $0°C \leq T_A \leq +70°C$ for LM710C unless otherwise specified: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at 25°C, and 1V at 125°C for LM710 and 1.5V at 0°C, 1.4V at 25°C, and 1.2V at 70°C for LM710C.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive (LM710) or a 10 mV overdrive (LM710C).

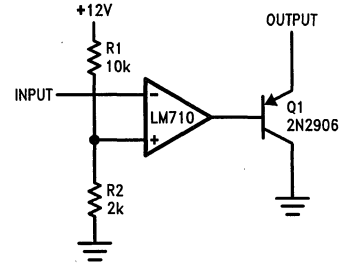
Typical Applications

Schmitt Trigger



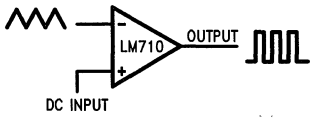
TL/H/10410–4

Line Receive with Increased Output Sink Current



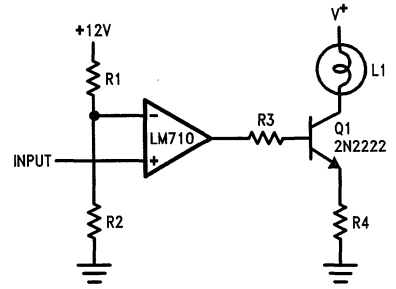
TL/H/10410–5

Pulse Width Modulator



TL/H/10410–6

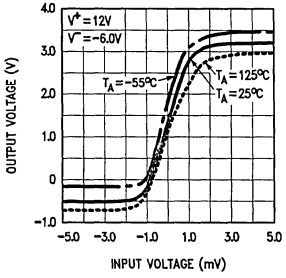
Level Detector with Lamp Driver



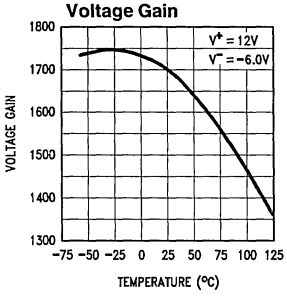
TL/H/10410–7

Typical Performance Characteristics

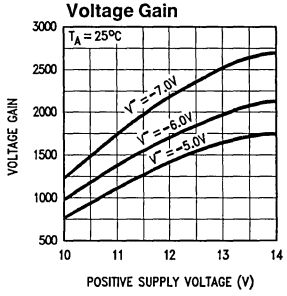
Transfer Function



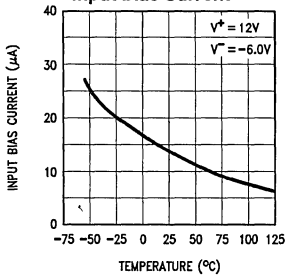
Voltage Gain



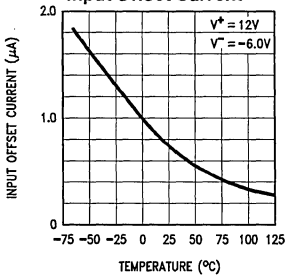
Voltage Gain



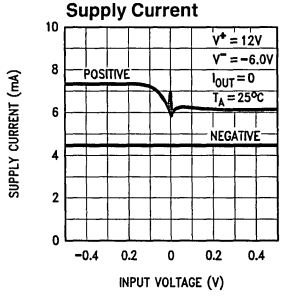
Input Bias Current



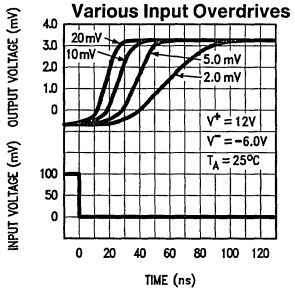
Input Offset Current



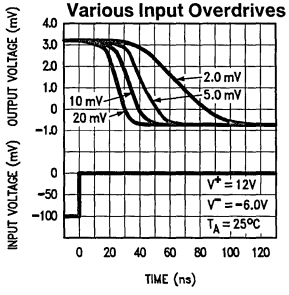
Supply Current



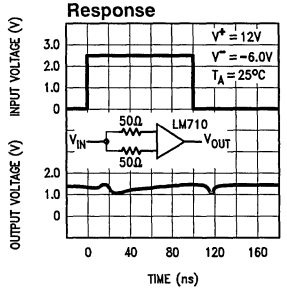
Response Time for Various Input Overdrives



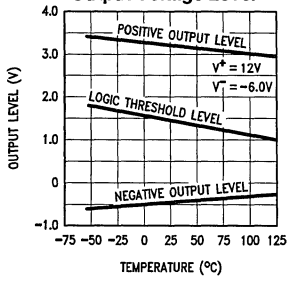
Response Time for Various Input Overdrives



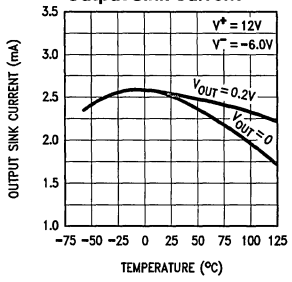
Common Mode Pulse Response



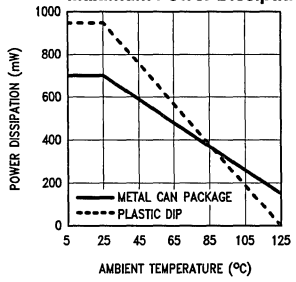
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



TL/H/10410–8

National Semiconductor

LM1514/LM1414
Dual Differential Voltage Comparator

General Description

The LM1514/LM1414 is a dual differential voltage comparator intended for applications requiring high accuracy and fast response times. The device is constructed on a single monolithic silicon chip.

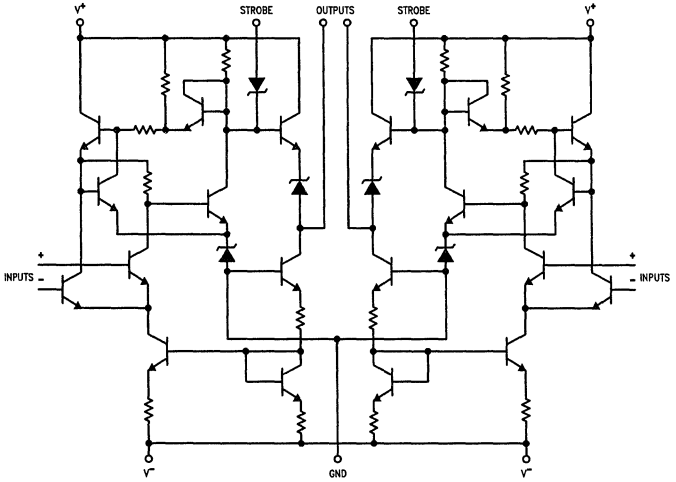
The LM1514/LM1414 is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. The LM1514/LM1414 meet or exceed the specifications for the MC1514/MC1414 and are pin-for-pin replacements. The LM1514 is available in the ceramic dual-in-line package. The LM1414 is available in either the ceramic or molded dual-in-line package.

The LM1514 is specified for operation over the −55°C to +125°C military temperature range. The LM1414 is specified for operation over the 0°C to +70°C temperature range.

Features

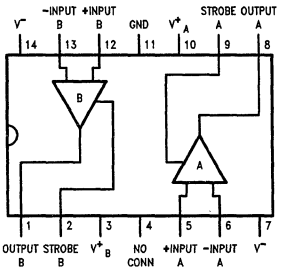
- Two totally separate comparators per package
- Independent strobe capability
- High speed 30 ns typ
- Low input offset voltage and current
- High output sink current over temperature
- Output compatible with TTL/DTL logic
- Molded or ceramic dual-in-line package

Schematic and Connection Diagrams



TL/H/10411–1

Dual-In-Line Package



TL/H/10411–2

Order Number LM1414J or LM1514J
See NS Package Number J14A

Order Number LM1414N
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation (Note 2)	1000 mW
Operating Temperature Range	
LM1514	−55°C to +125°C
LM1414	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics for $T_A = 25°C$, $V^+ = +12V$, $V^- = -6V$, unless otherwise specified

Parameter	Conditions	LM1514			LM1414			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$		0.6	2.0		1.0	5.0	mV
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.4V$		0.8	3.0		1.2	5.0	μA
Input Bias Current				20			25	μA
Voltage Gain		1250			1000			
Output Resistance			200			200		Ω
Differential Input Voltage Range		±5.0			±5.0			V
Input Voltage Range	$V^- = -7.0V$	±5.0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$, $V^- = -7.0V$	80	100		70	100		dB
Positive Output Voltage	$V_{IN} \geq 7.0$ mV, $0 \leq I_{OUT} \leq -5.0$ mA	2.5	3.2	4.0	2.5	3.2	4.0	V
Negative Output Voltage	$V_{IN} \leq -7.0$ mV	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobed Output Voltage	$V_{STROBE} \leq 0.3V$	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobe "0" Current	$V_{STROBE} = 100$ mV		−1.2	−2.5		−1.2	−2.5	mA
Positive Supply Current	$V_{IN} \leq -7$ mV			18			18	mA
Negative Supply Current	$V_{IN} \leq -7$ mV			−14			−14	mA
Power Consumption			180	300		180	300	mW
Response Time	(Note 3)		30			30		ns
LM1514/LM1414: The following apply for $T_L \leq T_A < T_H$ (Note 4) unless otherwise specified								
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{OUT} = 1.8V$ for $T_A = T_L$ $V_{CM} = 0V$, $V_{OUT} = 1.0V$ for $T_A = T_H$			3.0 3.0			6.5 6.5	mV mV
Input Bias Current				45			40	μA
Temperature Coefficient of Input Offset Voltage			3.0			5.0		μV/°C
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.8V$, $T_A = T_L$ $V_{CM} = 0V$, $V_{OUT} = 1.0V$, $T_A = T_H$			7.0 3.0			7.5 7.5	μA μA
Voltage Gain		1000			800			
Output Sink Current	$V_{IN} \leq -9.0$ mV, $V_{OUT} \geq 0V$	2.8	4.0		1.6	2.5		mA

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: LM1514 ceramic package: The maximum junction temperature is +150°C, for operating at elevated temperatures, devices must be derated linearly at 12.5 mW/°C. LM1414 ceramic package: The maximum junction temperature is +125°C for operating at elevated temperatures, devices must be derated linearly at 12.5 mW/°C. LM1414 molded package: The maximum junction temperature is +125°C, for operating at elevated temperatures, devices must be derated linearly at 10 mW/°C.

Note 3: The response time specified (see definitions) for a 100 mV input step with 5 mV overdrive.

Note 4: For LM1514, $T_L = -55°C$, $T_H = +125°C$. For LM1414, $T_L = 0°C$, $T_H = +70°C$.

National Semiconductor

LP265/LP365 Micropower Programmable Quad Comparator

General Description

The LP365 consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

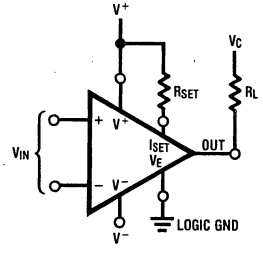
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ± 2.0 V_{DC} to ± 18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator) @ $I_{SET} = 0.5\ \mu A$ $V_{CC} = 5 V_{DC}$
- Uncommitted output stage—selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

Typical Connection



TL/H/5023–1

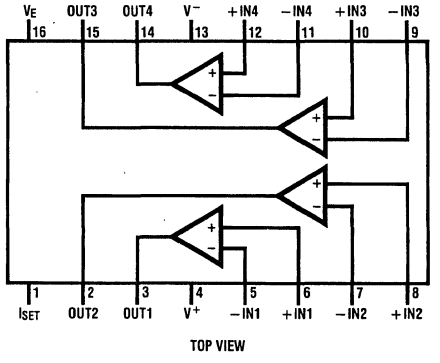
Programming Equation

$$I_{SET} = \frac{(V^+) - (V^-) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5023–2

Order Number LP365M, LP265N, LP365AN or LP365N
See NS Package Numbers M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ± 18 V_{DC}
Differential Input Voltage	± 36 V_{DC}
Input Voltage (Note 1)	−0.3V to +36 V_{DC}
Output Short Circuit to V_E (Note 2)	Continuous
V_{OUT} with Respect to V_E	$V_E - 7V \le V_{OUT} \le V_E + 36V$
ESD Tolerance (Note 10)	2000V

	M Package	N Package
Power Dissipation (Note 3)	500 mW	500 mW
T_j Max	115°C	115°C
θ_{jA}	115°C/W	90°C/W
Lead Temp.		
(Soldering—10 sec.)		260°C
(Vapor Phase—60 sec.)	215°C	
(Infrared—15 sec.)	220°C	

Operating Temp. Range LP365: $0°C \le T_A \le +70°C$

LP265: $-40°C \le T_A \le +85°C$

Storage Temp. Range $-40°C \le T_A \le +150°C$

Electrical Characteristics (Note 4) Low power $V_S = 5V$, $I_{SET} = 10\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP265/LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$ LP265	2	20	**50**	4	25	**75**	nA (Max)
						4	25	**150**	
I_B	Input Bias Current	$V_{CM} = 0V$ LP265	10	50	**125**	15	75	**200**	nA (Max)
						15	75	**300**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 100k$	500	50	**50**	300	25	**25**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			0	**0**		0	**0**	V (Max)
				3	**3**		3	**3**	V (Min)
CMRR	Common-Mode Rejection Ratio	$0 \le V_{CM} \le 3V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 2.5V \le V_S \le \pm 3.5V$	75	65	**65**	70	65	**65**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$	215	250	**300**	225	275	**300**	μA (Max)
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	2.4	1.2	**0.6**	2.0	0.8	**0.4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 5V$, $V_E = 0V$	2	50	**5000**	2	100	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 7)	4			4			μs

Electrical Characteristics (Continued) (Note 8) High power $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP265/LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$ LP265	5	50	**100**	10	90	**200**	nA (Max)
						10	90	**500**	
I_B	Input Bias Current	$V_{CM} = 0V$ LP265	60	200	**500**	80	300	**500**	nA (Max)
						80	300	**800**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 15k$	500	100	**100**	500	100	**100**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			-15	$-$**15**		-15	$-$**15**	V (Max)
				13	**13**		13	**13**	V (Min)
CMRR	Common-Mode Rejection Ratio	$-15V \le V_{CM} \le 13V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 10V \le V_S \le \pm 15V$	80	70	**70**	75	70	**70**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$, LP265	2.6	3	**3.3**	2.8	3.5	**3.7**	mA (Max)
						2.8	3.5	**4.3**	
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	10	8	**5.5**	7.5	6	**4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 15V$, $V_E = -15V$	5	50	**5000**	5	50	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 7)	1.0			1.0			μs

Note 1: The input voltage is not allowed to go 0.3V above V^+ or $-0.3V$ below V^- as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to V^+ may cause excessive heating and eventual destruction. The current in the output leads and the V_E lead should not be allowed to exceed 30 mA. The output should not be shorted to V^- if $V_E \le (V^-) + 7V$.

Note 3: For operating at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{jA} and T_j max. $T_j = T_A + \theta_{jA} P_D$.

Note 4: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = 5V$, $V^- = 0V$, $I_{SET} = 10\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate out-going quality levels.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive.

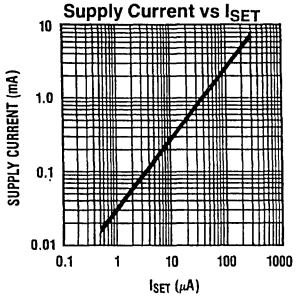
Note 8: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = +15V$, $V^- = -15V$, $I_{SET} = 100\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 9: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

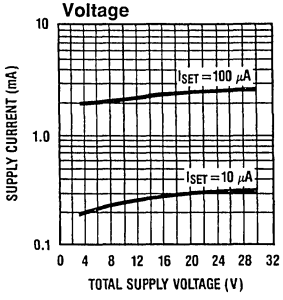
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

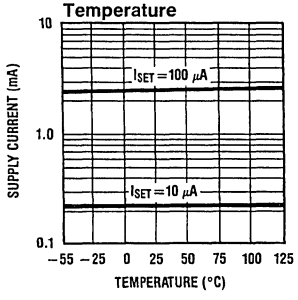
Supply Current vs I_{SET}



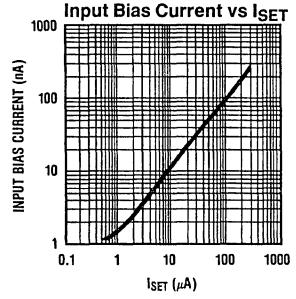
Supply Current vs Supply Voltage



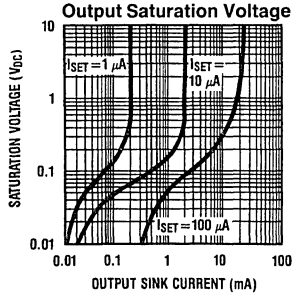
Supply Current vs Temperature



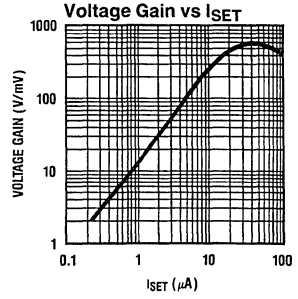
Input Bias Current vs I_{SET}



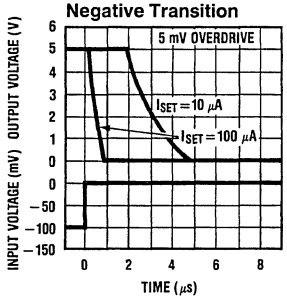
Output Saturation Voltage



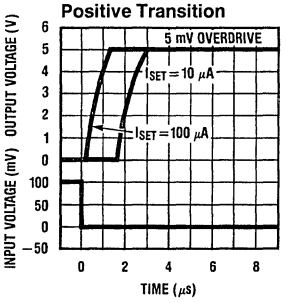
Voltage Gain vs I_{SET}



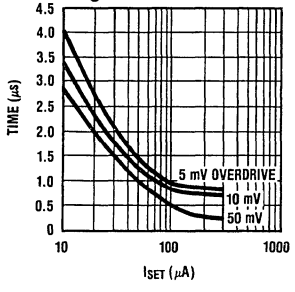
Response Time Negative Transition



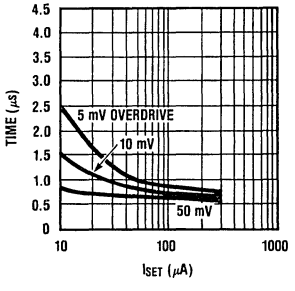
Response Time Positive Transition



Response Time Negative Transition



Response Time Positive Transition

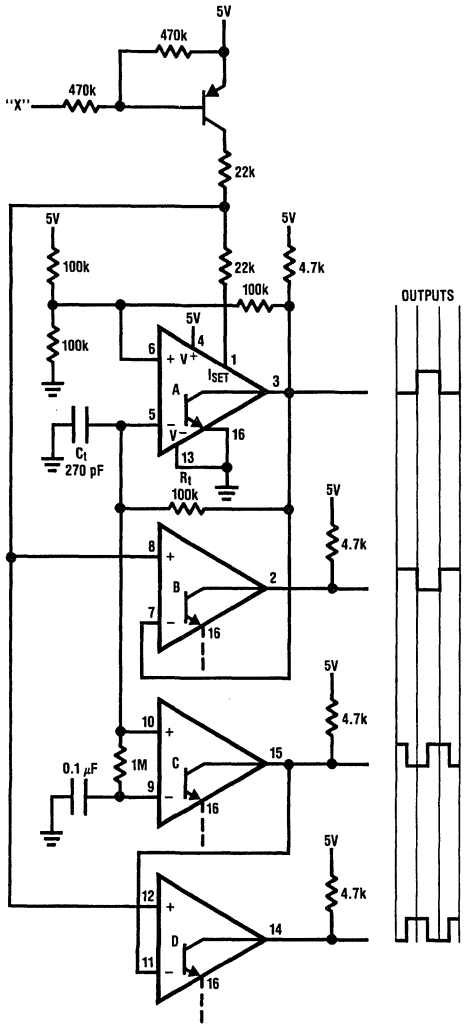


TL/H/5023–3

5

Typical Applications

Gated 4-Phase Oscillator



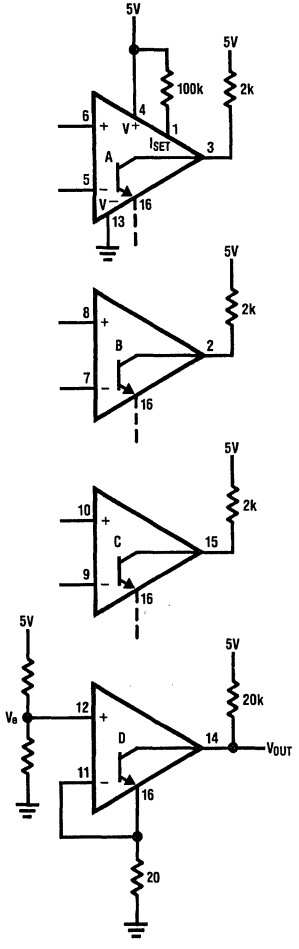
TL/H/5023–4

f = 20 kHz

$$f = \frac{1}{1.6 \bullet R_t \bullet C_t}$$

All four phases run when X is low. When X is high, oscillation stops and power drain is zero.

"Voting" Comparator

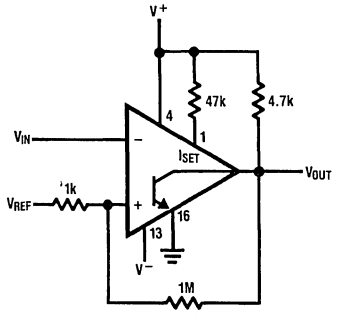


TL/H/5023–5

If V_E = 0.25V, then V_{OUT} will be low if 1 of the 3 other outputs are low. Choice of V_E = 0.50V causes V_{OUT} to be low if 2 of the 3 other outputs are low; V_E = 0.75V will cause V_{OUT} to be low if all 3 other outputs are low.

Typical Applications (Continued)

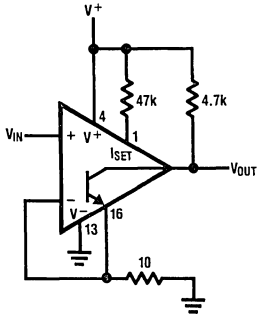
Ordinary Hysteresis



TL/H/5023–6

It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

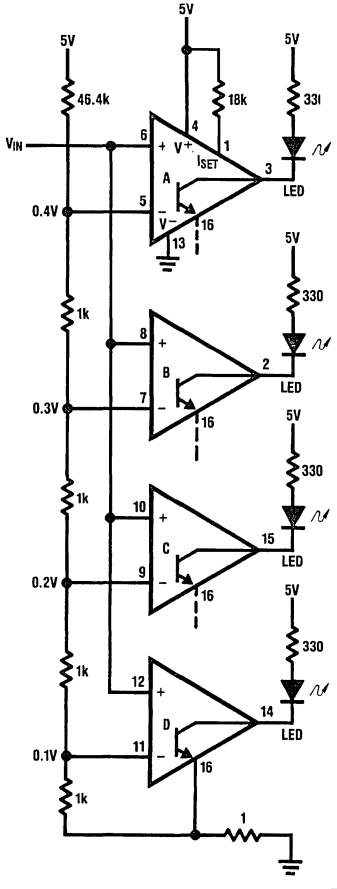
Hysteresis from Emitter



TL/H/5023–7

Positive feedback from the emitter can also prevent oscillations when V_{IN} is near the threshold.

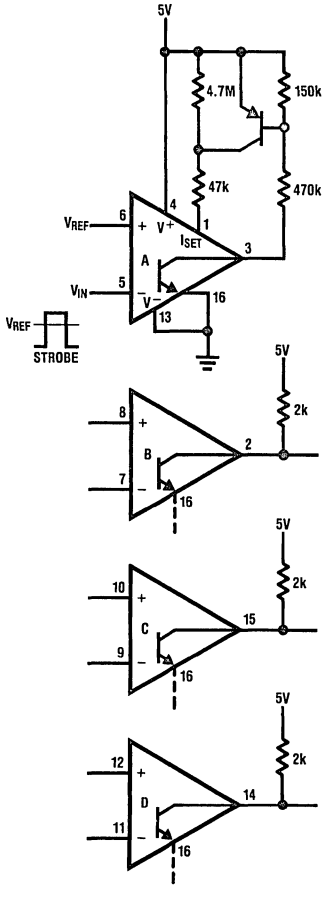
Bar-Graph Display



TL/H/5023–8

The positive feedback from pin 16 provides hysteresis.

Level-Sensitive Strobe

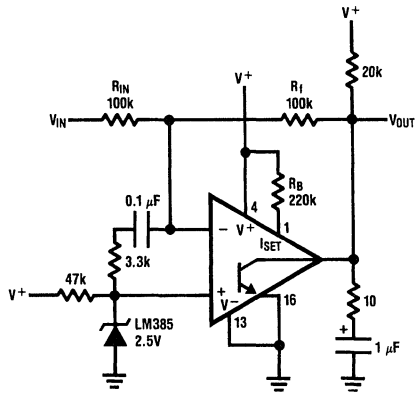


TL/H/5023–9

Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

Typical Applications (Continued)

Slow Op Amp (Inverter)

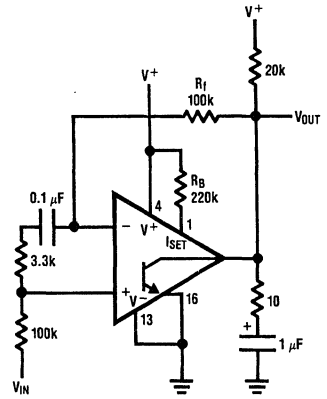


TL/H/5023–10

$R_B = V^+/20\ \mu A$

Unlike most comparators, the LP365 can be used as an op amp, if suitable R-C damping networks are used.

Slow Op Amp (Unity-Gain Follower)

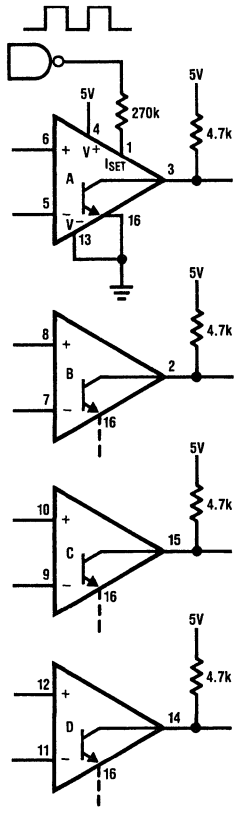


TL/H/5023–11

$R_B = V^+/20\ \mu A$

The LP365 can also be used as a high-input-impedance follower-amplifier with the damping components shown.

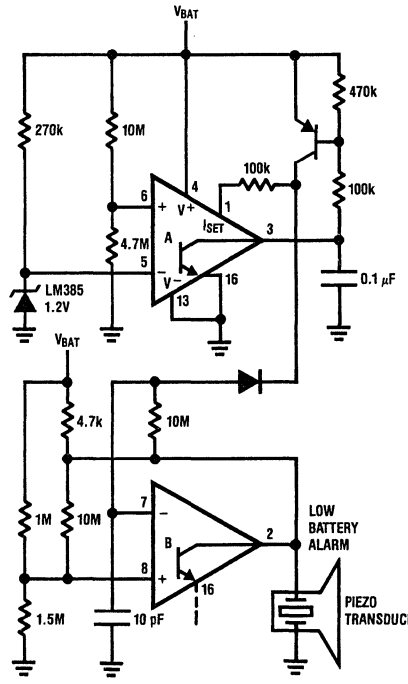
Chopping Outputs



TL/H/5023–12

Chopping the outputs by modulating the I_{SET} current allows data to be transmitted via opto-couplers, transformers, etc.

Low Battery Detector



TL/H/5023–13

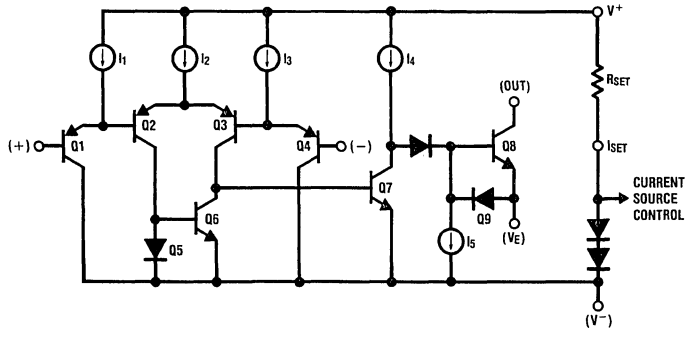
I_S @ 6V = 45 µA

I_S @ 3.8V = 1 µA

f = 3 kHz

Comparator A detects when the supply voltage drops to 4V and enables comparator B to drive a piezoelectric alarm.

Simplified Schematic



TL/H/5023–14

Current sources are programmed by I_{SET}

V_E is common to all 4 comparators

National Semiconductor

LP311 Voltage Comparator

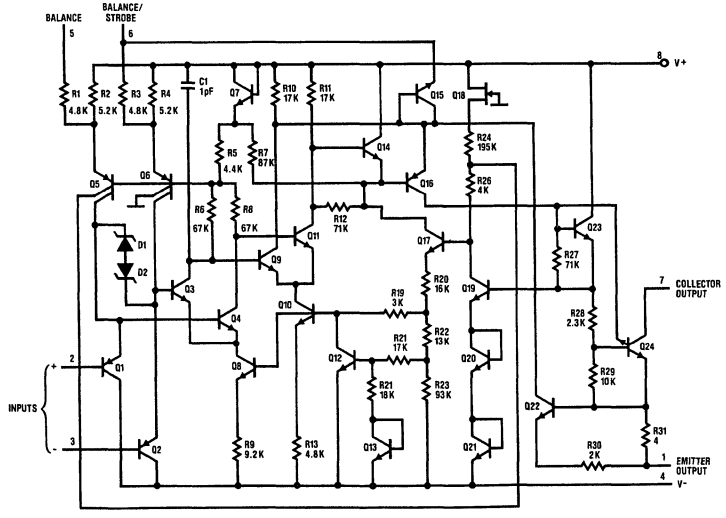
General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. (See the LM311 section of the Linear Databook.)

Features

- Low power drain, 900 μW on 5V supply
- Operates from ±15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: −14.6V to 13.6V with ±15V supply

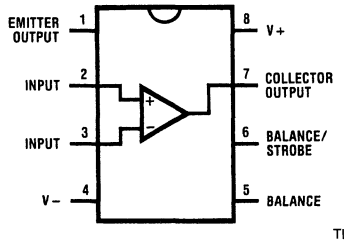
Schematic Diagram



TL/H/5711–7

Connection Diagrams

Dual-In-Line Package

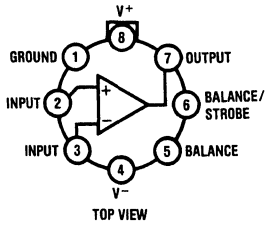


TL/H/5711–4

Top View

Order Number LP311N
See NS Package Number N08E

Metal Can Package



TOP VIEW

TL/H/5711–3

Note: Pin 4 connected to case.

Order Number LP311H
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{8-4})	36V
Collector Output to Negative Supply Voltage (V_{7-4})	40V
Collector Output to Emitter Output	40V
Emitter Output to Negative Supply Voltage (V_{1-4})	±30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 100k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		2.0	25	nA
Input Bias Current	$T_A = 25°C$		15	100	nA
Voltage Gain	$T_A = 25°C$, $R_L = 5k$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		1.2		μs
Saturation Voltage (Note 6)	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.4	1.5	V
Strobe Current (Note 7)	$T_A = 25°C$	100	200	300	μA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	100	nA
Input Offset Voltage (Note 4)	$R_S \leq 100k$			10	mV
Input Offset Current (Note 4)				35	nA
Input Bias Current				150	nA
Input Voltage Range		$V^- + 0.5$	+13.7, −14.7	$V^+ - 1.5$	V
Saturation Voltage (Note 6)	$V^+ \geq 4.5V$, $V^- = 0V$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 1.6$ mA		0.1	0.4	V
Positive Supply Current	$T_A = 25°C$, Output on		150	300	μA
Negative Supply Current	$T_A = 25°C$		80	180	μA
Minimum Operating Voltage	$T_A = 25°C$		3.0	3.5	V

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

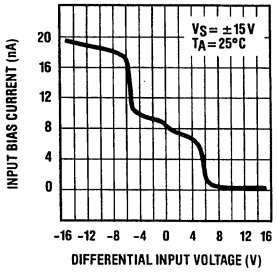
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: Saturation voltage specification applied to collector-emitter voltage (V7-1) for $V_{COLLECTOR} \leq (V^+ - 3V)$.

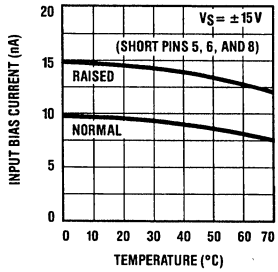
Note 7: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA.

Typical Performance Characteristics

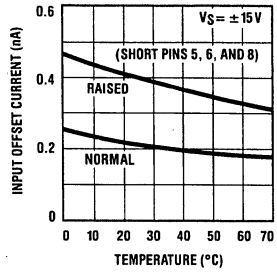
Input Characteristics



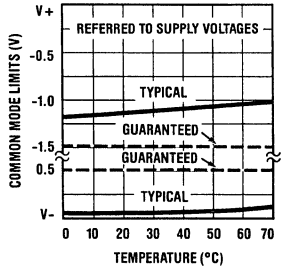
Input Bias Current



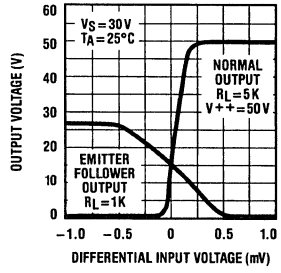
Input Offset Current



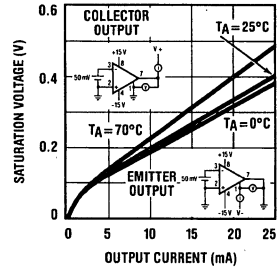
Common Mode Limits



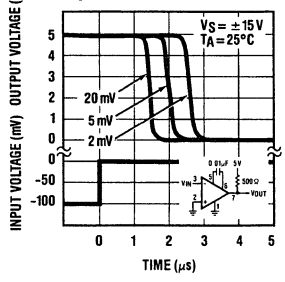
Transfer Function



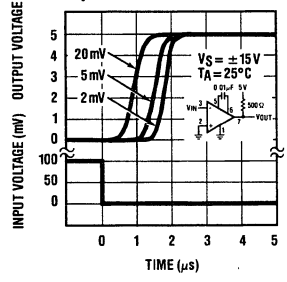
Output Saturation Voltage



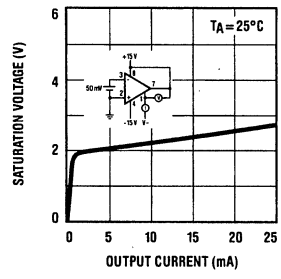
Response Time for Various Input Overdrives



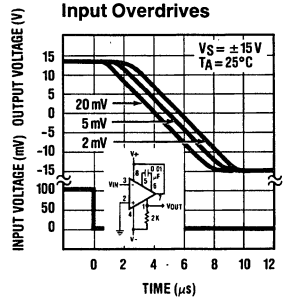
Response Time for Various Input Overdrives



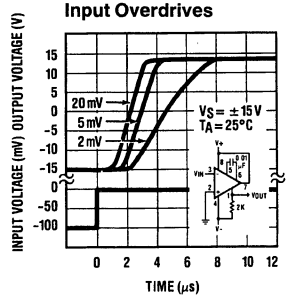
Output Saturation Voltage (Emitter Output)



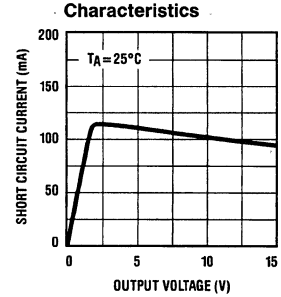
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



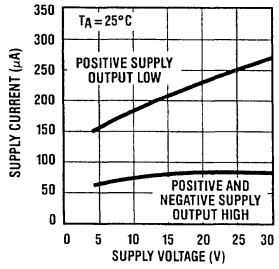
Output Limiting Characteristics



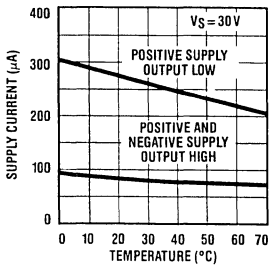
TL/H/5711–5

Typical Performance Characteristics (Continued)

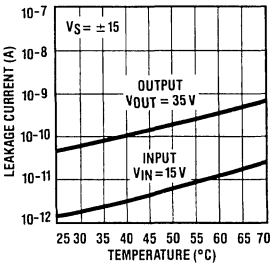
Supply Current



Supply Current



Leakage Currents



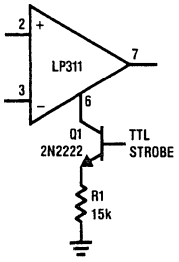
TL/H/5711–6

Applications Information

For applications information and typical applications, refer to the LM311 datasheet.

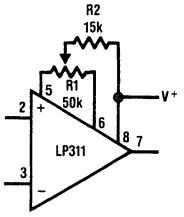
Auxiliary Circuits

Strobing



TL/H/5711–1

Offset Balancing



TL/H/5711–2

Note: Do not ground strobe pin.

National Semiconductor

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

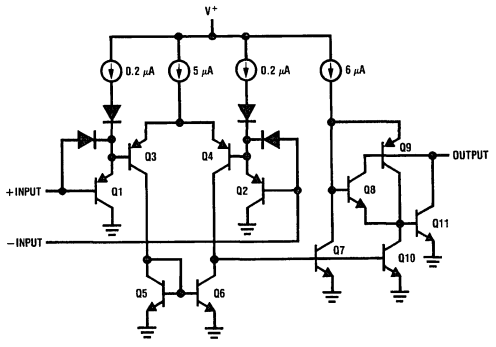
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

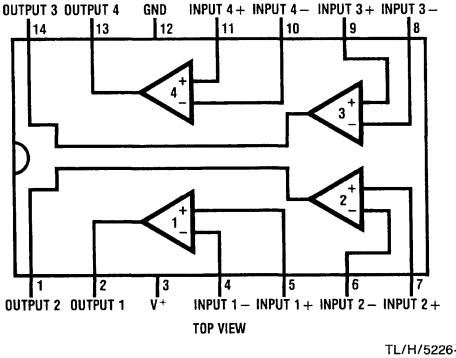
Features

- Ultra-low power supply current drain (60 μA)—independent of the supply voltage (75 μW/comparator at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ±0.5 nA
- Low input offset voltage ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O = 2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



TL/H/5226-1



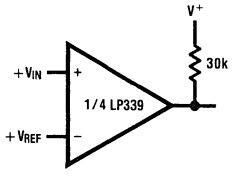
TL/H/5226-2

Order Number LP339M for S.O. Package
See NS Package Number M14A

Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

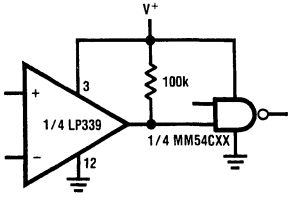
Typical Applications (V^+ = 5.0 V_{DC})

Basic Comparator



TL/H/5226-3

Driving CMOS



TL/H/5226-4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 1) Molded DIP	570 mW
Output Short Circuit to GND (Note 2)	Continuous
Input Current $V_{IN} < -0.3$ V_{DC} (Note 3)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65° to +150°C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260°C
S.O. Package:	
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V+ = 5$ V_{DC}, Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 9)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, $T_A = 25°C$ (Note 5)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	$T_A = 25°C$ (Note 6)	0		$V+ - 1.5$	V_{DC}
Supply Current	R_L = Infinite on all Comparators, $T_A = 25°C$		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, $R_L = 15\ k\Omega$, $V+ = 15$ V_{DC}, $T_A = 25°C$		500		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		1.3		μSec
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1\ k\Omega$, $T_A = 25°C$ (Note 7)		8		μSec
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}, $T_A = 25°C$ (Note 11)	15	30		mA_{DC}
	$V_O = 0.4$ V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 5$ V_{DC}, $T_A = 25°C$		0.1		nA_{DC}
Input Offset Voltage	(Note 9)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		$V+ - 2.0$	V_{DC}
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}	10			mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 30$ V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All V_{IN}'s ≥ 0 V_{DC} (or V− on split supplies) (Note 8)			36	V_{DC}

Note 1: For elevated temperature operation, T_j max is 125°C for the LP339. θ_{ja} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} ($T_A = 25°C$).

Note 4: These specifications apply for $V+ = 5V_{DC}$ and $0°C \leq T_A \leq 70°$ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 6: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ - 1.5V$ ($T_A = 25°C$), but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 μs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics ($V+ = 5\ V_{DC}$, Note 4) (Continued)

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) at $T_A = 25°C$.

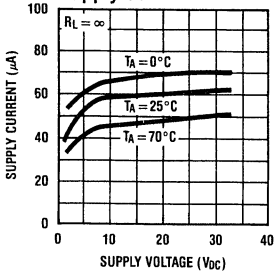
Note 9: At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from $5\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V+ - 1.5\ V_{DC}$).

Note 10: For input signals that exceed $V+$, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

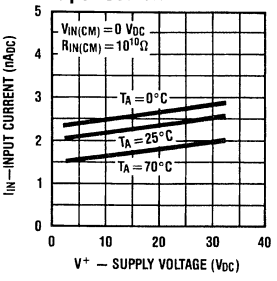
Note 11: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately $1.5\ V_{DC}$ and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics

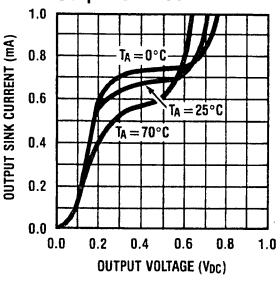
Supply Current



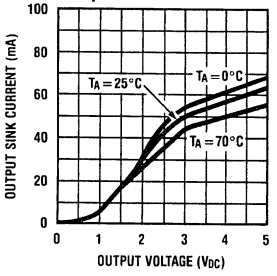
Input Current



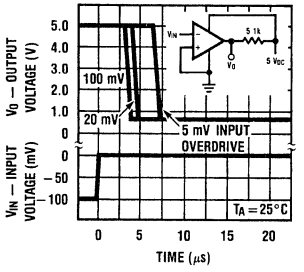
Output Sink Current



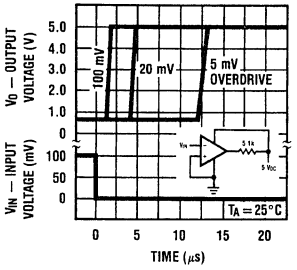
Output Sink Current



Response Times for Various Input Overdrives — Negative Transition



Response Times for Various Input Overdrives — Positive Transition



TL/H/5226–10

Application Hints

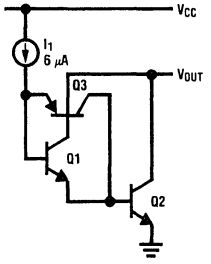
All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2\ V_{DC}$ (Darlington mode) and 700 μA at $V_O = 0.4\ V_{DC}$ (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.



TL/H/5226–11

FIGURE 1

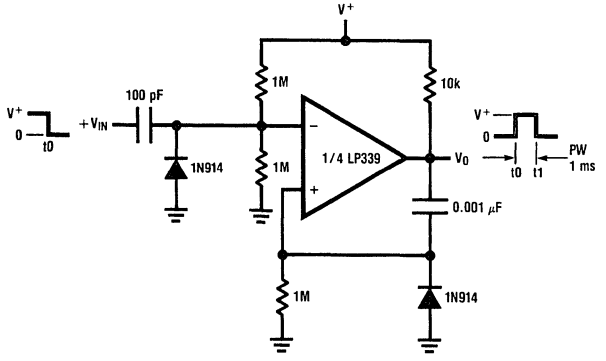
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1\ V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω R_{SAT} of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 μA.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 V_{DC}, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 μA at $V_O = 0.4\ V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

Typical Applications ($V^+ = 15\ V_{DC}$)

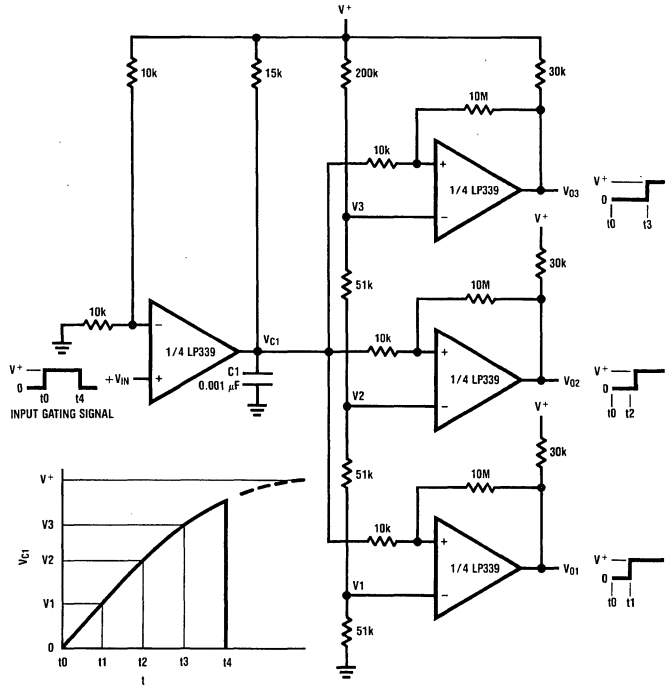
One-Shot Multivibrator



TL/H/5226–13

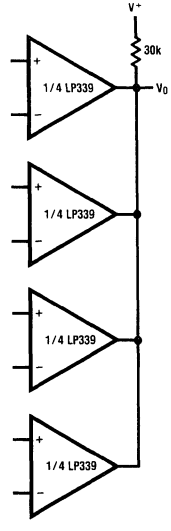
Typical Applications ($V^+ = 15\ V_{DC}$)

Time Delay Generator



TL/H/5226–15

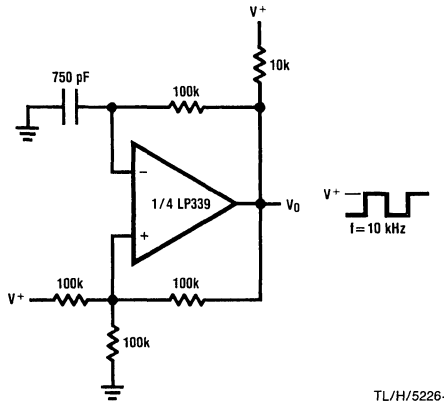
ORing the Outputs



TL/H/5226–16

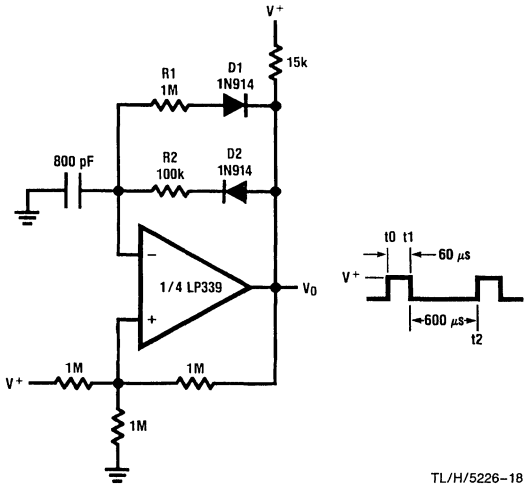
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Squarewave Oscillator



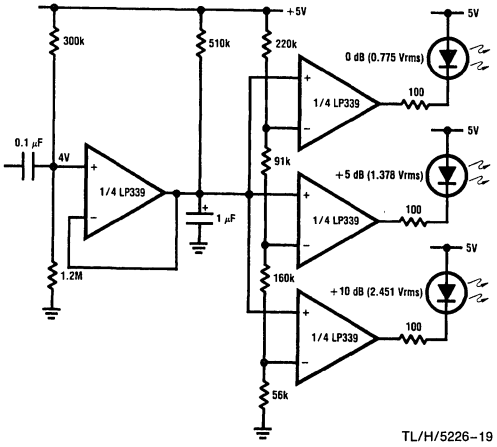
TL/H/5226–17

Pulse Generator



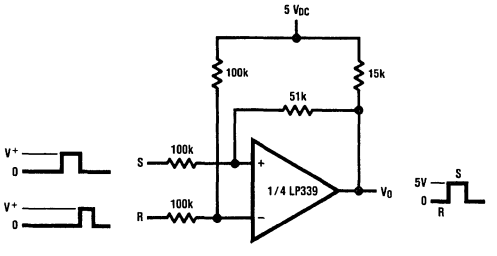
TL/H/5226–18

Three Level Audio Peak Indicator



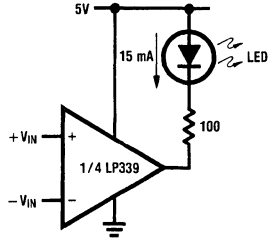
TL/H/5226–19

Bi-Stable Multivibrator



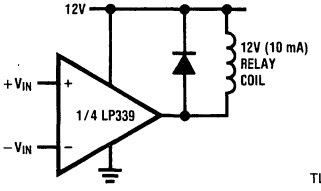
TL/H/5226–21

LED Driver



TL/H/5226–22

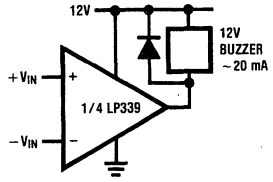
Relay Driver



TL/H/5226–23

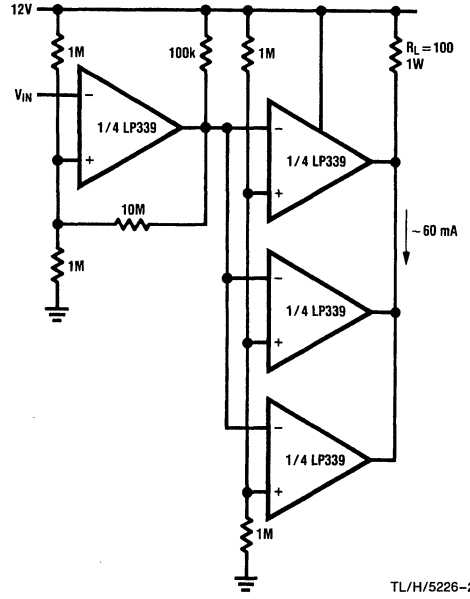
Typical Applications (Continued) (Single Supply)

Buzzer Driver



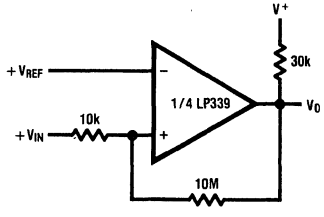
TL/H/5226–24

Comparator With 60 mA Sink Capability



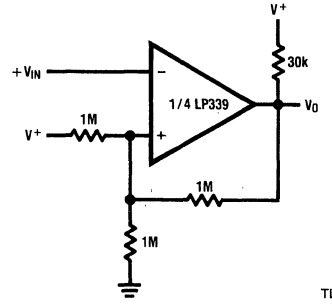
TL/H/5226–25

Non-Inverting Comparator with Hysteresis



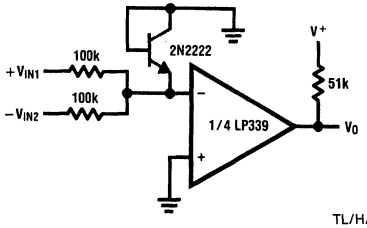
TL/H/5226–26

Inverting Comparator with Hysteresis



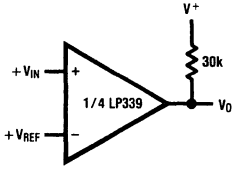
TL/H/5226–27

Comparing Input Voltages of Opposite Polarity



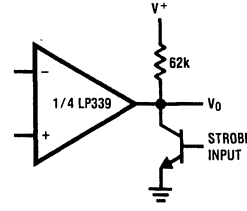
TL/H/5226–28

Basic Comparator



TL/H/5226–29

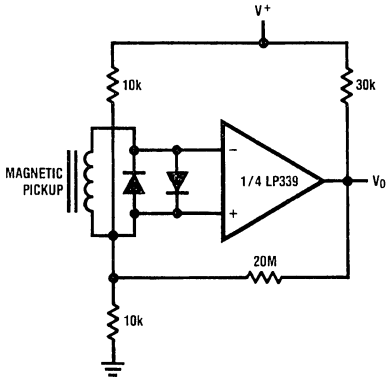
Output Strobing



TL/H/5226–30

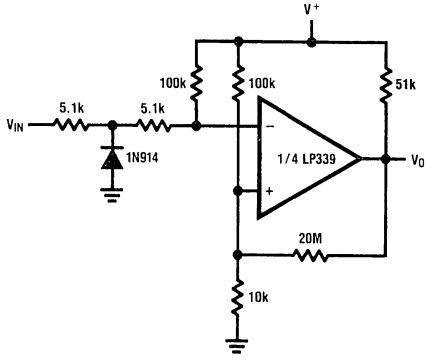
Typical Applications (Continued) (Single Supply)

Transducer Amplifier



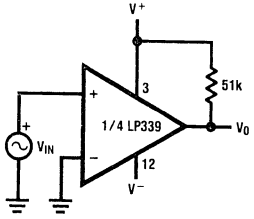
TL/H/5226–31

Zero Crossing Detector (Single Power Supply)



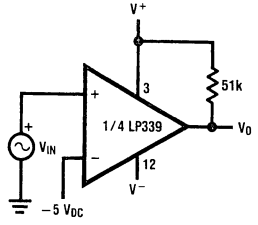
TL/H/5226–32

Split-Supply Applications Zero Crossing Detector



TL/H/5226–33

Comparator With a Negative Reference



TL/H/5226–34

Section 6

Instrumentation Amplifiers

Section 6 Contents

National Semiconductor

Instrumentation Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

Instrumentation Amplifiers Selection Guide

Part Number	Gain Error (Max)	Gain Linearity (Typ)	CMRR dB (Min)	I_B nA (Max)
		$T_A = 25°C$		
LH0036 μ Power	1%	0.03%	72	100
LH0038	0.3%	0.0001%	94	100
LH0084	0.1%	0.002%	76	0.500
LM363	2.5%	0.01%	90	10

Note 1: Datasheet should be referred to for test conditions and more detailed information.

National Semiconductor

LH0036/LH0036C Instrumentation Amplifier

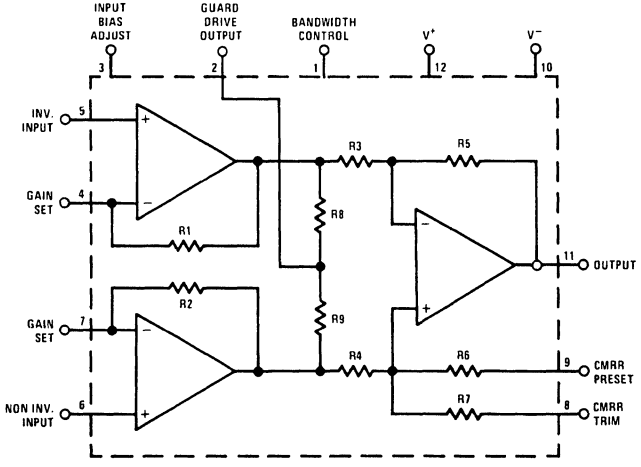
General Description

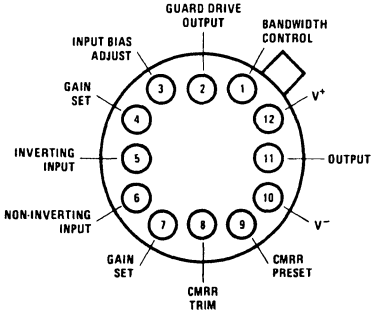
The LH0036/LH0036C is a true micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable from 1 to 1000 with a single external resistor. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036 is specified for operation over the −55°C to +125°C temperature range and the LH0036C is specified for operation over the −25°C to +85°C temperature range.

Features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 90 μW
- Wide supply range — ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

Equivalent Circuit and Connection Diagrams





TOP VIEW

TL/H/5545–1

Order Number LH0036G or LH0036CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range	$\pm V_S$
Shield Drive Voltage	$\pm V_S$
CMRR Preset Voltage	$\pm V_S$
CMMR Trim Voltage	$\pm V_S$
Power Dissipation (Note 3)	1.5W
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0036	−55°C to +125°C
LH0036C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Limits						Units
		LH00336			LH0036C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S = 1.0 kΩ, T_A = 25°C		0.5	1.0		1.0	2.0	mV
(V_{IOS})	R_S = 1.0 kΩ			2.0			3.0	mV
Output Offset Voltage	R_S = 1.0 kΩ, T_A = 25°C		2.0	5.0		5.0	10	mV
(V_{OOS})	R_S = 1.0 kΩ			6.0			12	mV
Input Offset Voltage	$R_S \leq$ 1.0 kΩ		10			10		μV/°C
Tempco ($\Delta V_{IOS}/\Delta T$)								
Output Offset Voltage			15			15		μV/°C
Tempco ($\Delta V_{OOS}/\Delta T$)								
Overall Offset Referred	A_V = 1.0		2.5			6.0		mV
to Input (V_{OS})	A_V = 10 A_V = 100 A_V = 1000		0.7 0.52 0.502			1.5 1.05 1.005		mV mV mV
Input Bias Current	T_A = 25°C		40	100		50	125	nA
(I_B)				150			200	nA
Input Offset Current	T_A = 25°C		10	40		20	50	nA
(I_{OS})				80			100	nA
Input Voltage Range	Differential Common Mode	±10 ±10	±12 ±12		±10 ±10	±12 ±12		V V
Gain Nonlinearity			0.03			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000 (Note 4)		±0.3	±1.0		±1.0	±3.0	%

Electrical Characteristics (Notes 1 and 2) (Continued)

Parameter	Conditions	Limits						Units
		LH00336			LH0036C			
		Min	Typ	Max	Min	Typ	Max	
PSRR	$\pm 5.0V \le V_S \le \pm 15V$, $A_V = 1.0$		1.0	2.5		1.0	5.0	mV/V
	$\pm 5.0V \le V_S \le \pm 15V$, $A_V = 100$		0.05	0.25		0.10	0.50	mV/V
CMRR	$A_V = 1.0$ DC to		1.0	2.5		2.5	5.0	mV/V
	$A_V = 10$ 100 Hz		0.1	0.25		0.25	0.50	mV/V
	$A_V = 100$ $\Delta R_S = 1.0k$		50	100		50	100	μV/V
Output Voltage	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±10	±13.5		±10	±13.5		V
	$V_S = \pm 1.5V$, $R_L = 100\ k\Omega$	±0.6	±0.8		±0.6	±0.8		V
Output Resistance			0.5			0.5		Ω
Supply Current			300	400		400	600	μA
Small Signal Bandwidth	$A_V = 1.0$, $R_L = 10\ k\Omega$		350			350		kHz
	$A_V = 10$, $R_L = 10\ k\Omega$		35			35		kHz
	$A_V = 100$, $R_L = 10\ k\Omega$		3.5			3.5		kHz
	$A_V = 1000$, $R_L = 10\ k\Omega$		350			350		Hz
Full Power Bandwidth	$V_{IN} = \pm 10V$, $R_L = 10k$, $A_V = 1$		5.0			5.0		kHz
Equivalent Input Noise Voltage	0.1 Hz < f < 10 kHz, $R_S < 50\Omega$		20			20		μV/p-p
Slew Rate	$\Delta V_{IN} = \pm 10V$, $R_L = 10\ k\Omega$, $A_V = 1.0$		0.3			0.3		V/μS
Settling Time	To ±10 mV, $R_L = 10\ k\Omega$, $\Delta V_{OUT} = 1.0V$							
	$A_V = 1.0$		3.8			3.8		μS
	$A_V = 100$		180			180		μS

Note 1: Unless otherwise specified, all specifications apply for $V_S = \pm 15V$, Pins 1, 3, and 9 grounded, −25°C to +85°C for the LH0036C and −55°C to +125°C for the LH0036.

Note 2: All typical values are for $T_A = 25°C$.

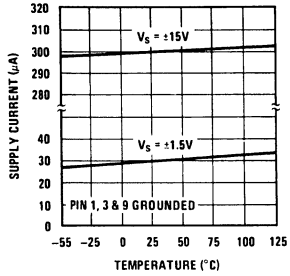
Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W, above 25°C.

Note 4: $A_V = 1000$ guaranteed by design and testing at $A_V = 100$.

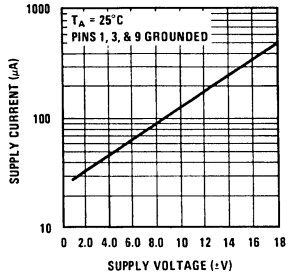
Note 5: Refer to RETS0036G for LH0036G military specifications.

Typical Performance Characteristics

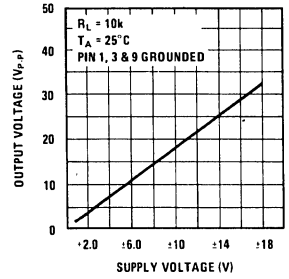
Supply Current vs Temperature



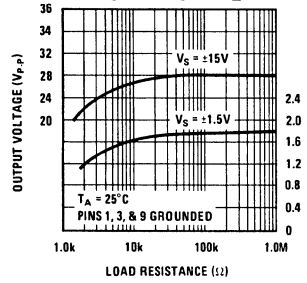
Supply Current vs Supply Voltage



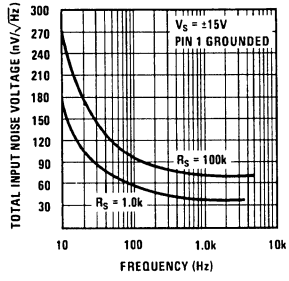
Output Voltage Swing vs Supply Voltage



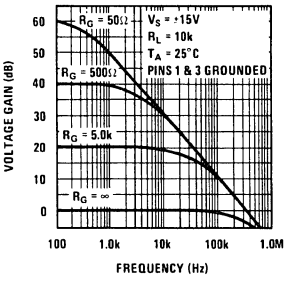
Peak to Peak Output Voltage Swing vs R_L



Total Input Noise Voltage* vs Frequency

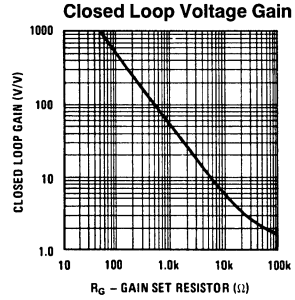


Closed Loop Voltage Gain vs Frequency

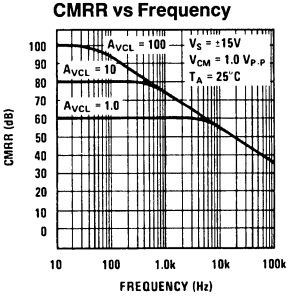


*Noise voltage includes contribution from source resistance

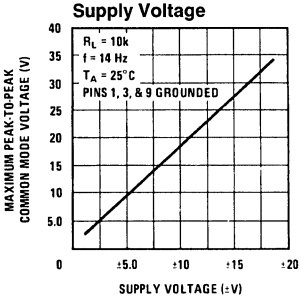
Closed Loop Voltage Gain



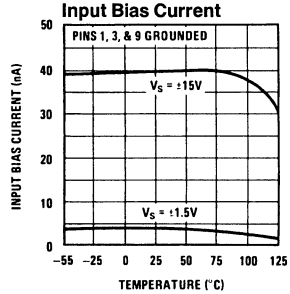
CMRR vs Frequency



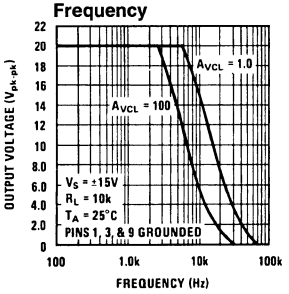
Common Mode Voltage vs Supply Voltage



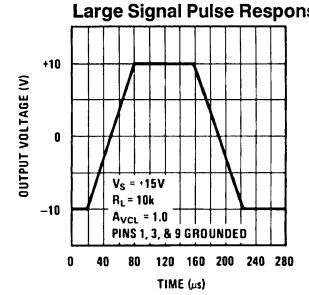
Input Bias Current



Output Voltage Swing vs Frequency



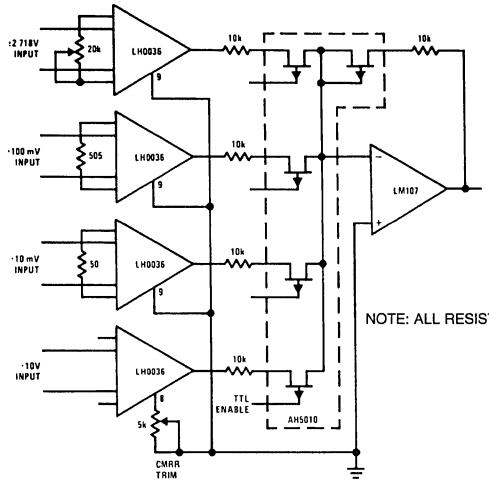
Large Signal Pulse Response



TL/H/5545–2

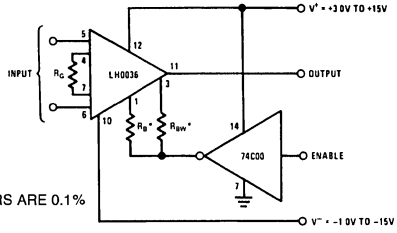
Typical Applications

Pre MUX Signal Conditioning



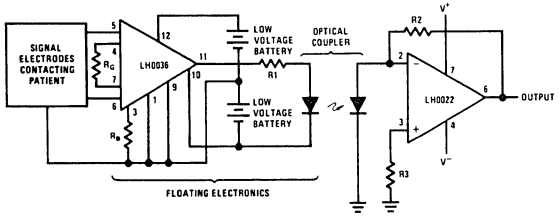
NOTE: ALL RESISTORS ARE 0.1%

Instrumentation Amplifier with Logic Controlled Shut-Down

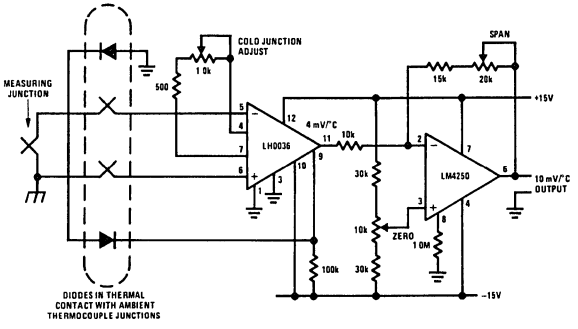


*R_{BW} AND R_B ARE OPTIONAL BANDWIDTH AND INPUT BIAS CURRENT CONTROLLING RESISTORS.

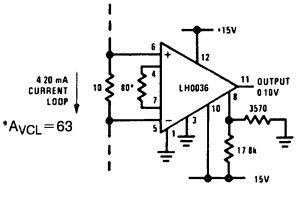
Isolation Amplifier for Medical Telemetry



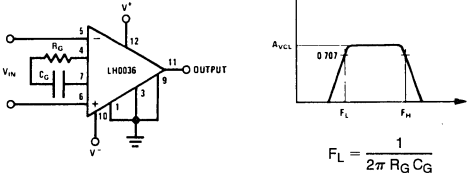
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



High Pass Filter



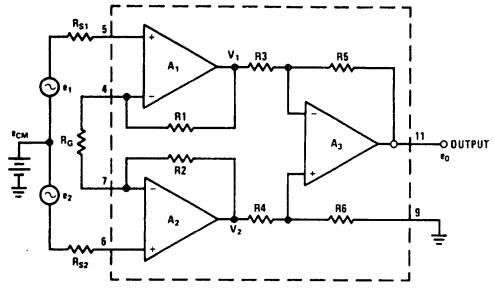
$$F_L = \frac{1}{2\pi R_G C_G}$$

TL/H/5545–3

F_H = A FUNCTION OF SELECTED A_{VCL}, R_S AND R_{SW}

Applications Information

THEORY OF OPERATION



TL/H/5545–4

FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of +1.

Hence:

$$V_1 = \frac{R1+R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For R1 = R2:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for R3 = R5 = R4 = R6, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

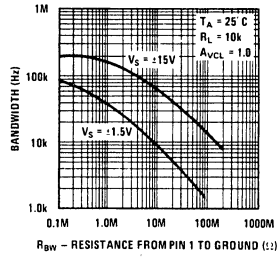
$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

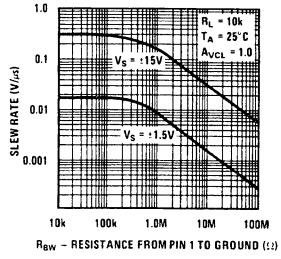
In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically 0.3V/μS and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. *Figure 2* shows typical small signal bandwidth versus R_{BW}.



TL/H/5545–5

FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. *Figure 3* is plot of slew rate versus R_{BW}.



TL/H/5545–6

FIGURE 3. Output Slew Rate vs R_{BW}

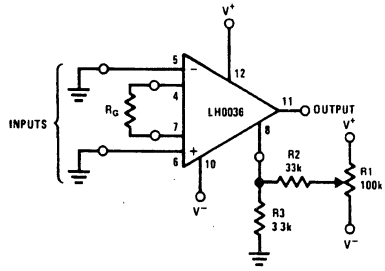
CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in *Figure 4*.

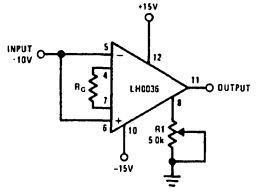


TL/H/5545–7

FIGURE 4. V_{OS} Adjustment Circuit

Applications Information (Continued)

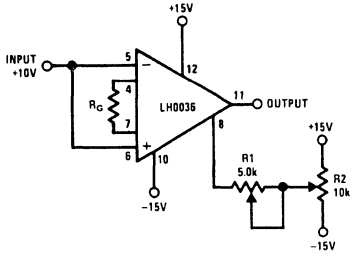
Pin 8 is also used to improve the common mode rejection ratio as shown in *Figure 5*. Null is achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.



TL/H/5545–8

FIGURE 5. CMRR Adjustment Circuit

The circuits of *Figure 4* and *5* may be combined as shown in *Figure 6* to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

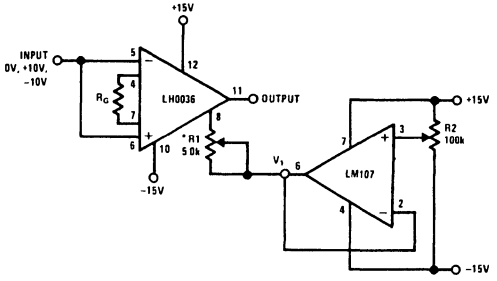


TL/H/5545–10

FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in *Figure 7*. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



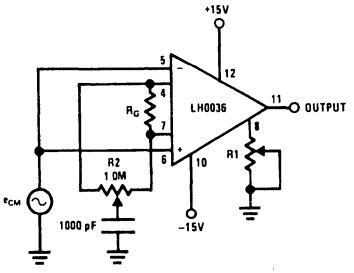
TL/H/5545–11

*Note: Nominal value R1 to Achieve Optimum CMRR is 3.0 kΩ

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of *Figure 8*.



TL/H/5545–9

FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\, R_B} \qquad (6a)$$

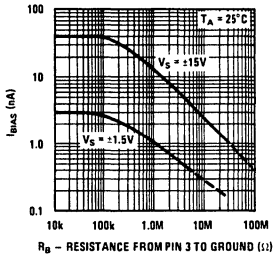
or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\,(I_{BIAS})}{800\, I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)
R_B = External Resistor connected between pin 3 and ground (Ohms)
V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.



TL/H/5545–12

FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\, R_B}$$

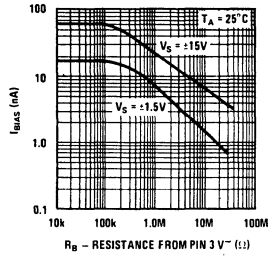
Applications Information (Continued)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

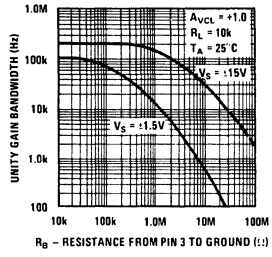
I_{BIAS} = Input Bias Current (nA)
R_B = External resistor connected between pin 3 and V^- (Ohms)
V^+ = Positive Supply Voltage (Volts)
V^- = Negative Supply Voltage (Volts)



TL/H/5545–13

FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. *Figure 11* is a plot of bandwidth versus R_B.

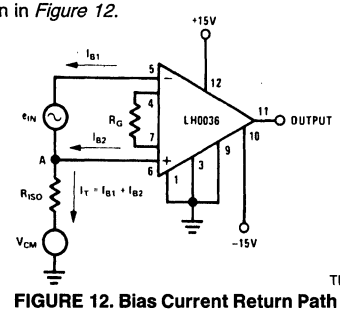


TL/H/5545–14

FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in *Figure 12*.



TL/H/5545–16

FIGURE 12. Bias Current Return Path

In a typical application, $V_S = \pm 15V$, $I_{B1} \cong I_{B2} \cong 40$ nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

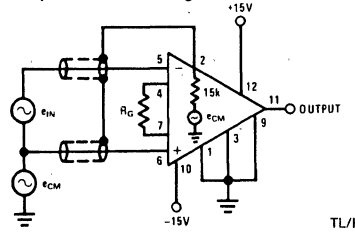
Where:

V_{CMR} = Common Mode Range (10V for the LH0036)
V_{CM} = Common Mode Voltage
$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

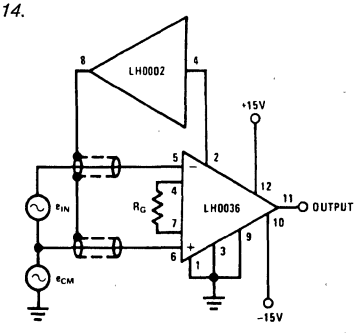
Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in *Figure 13*.



TL/H/5545–15

FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in *Figure 14*.



TL/H/5545–17

FIGURE 14. Guard Pin With Buffer

Definition of Terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

National Semiconductor

LH0038/LH0038C True Instrumentation Amplifier

General Description

The LH0038/LH0038C is a precision true instrumentation amplifier (TIA) capable of amplifying very low level signals, such as thermocouple and low impedance strain gauge outputs. Precision thin film gain setting resistors are included in the package to allow the user to set the closed-loop gain from 100 to 2000. Since the resistors are of a homogeneous single chip construction, they track almost perfectly so that temperature variations of closed loop gain are virtually eliminated.

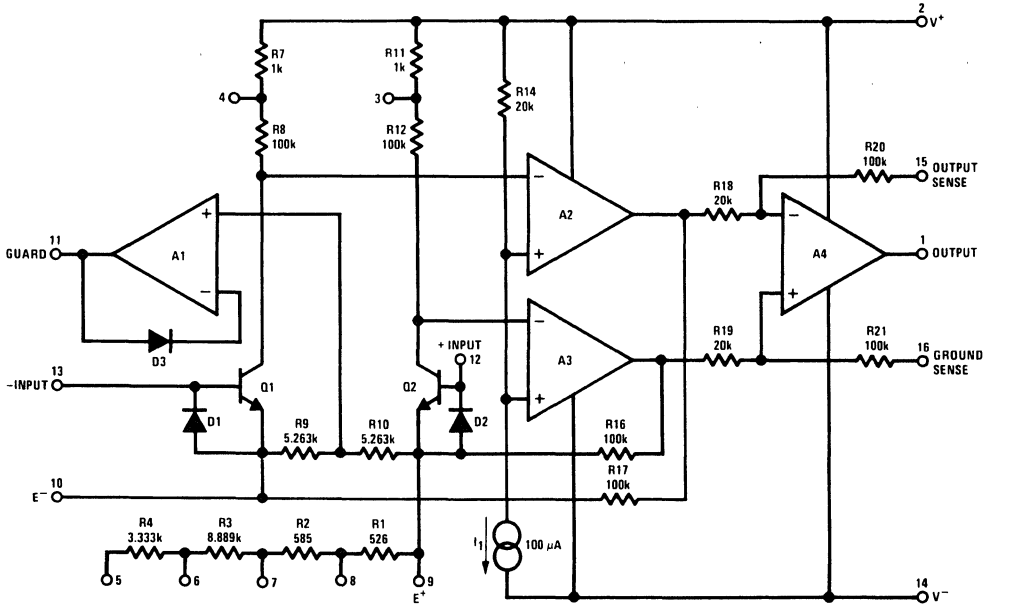
LH0038 exhibits excellent CMRR, PSRR, gain linearity, as well as extremely low input offset voltage, offset voltage drift and input noise voltage.

The devices are provided in a hermetically sealed 16-lead DIP. The LH0038 is guaranteed from −55°C to +125°C; whereas the LH0038C is guaranteed from −25°C to +85°C.

Features

- Ultra-low input offset voltage 25 μV typ., 100 μV max
- Ultra-low input offset drift 0.25 μV/°C max
- Ultra-low input noise 0.2 μVp-p
- Pin strap gain options 100, 200, 400, 500, 1k, 2k
- Excellent PSRR and CMRR 120 dB

Simplified Schematic Diagram



TL/H/5543–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±1V
Input Voltage	$\pm V_S$
Power Dissipation (Note 3)	500 mW
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0038	−55°C to +125°C
LH0038C	−25°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		LH0038			LH0038C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IOS}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$	$T_A = 25°C$		25	100		30	150	µV
						125			220	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Tempco				0.1	0.25		0.2	1.0	µV/°C
V_{OOS}	Output Offset Voltage		$T_A = 25°C$		3	10		5	25	mV
						15			30	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Tempco				25			25		µV/°C
I_B	Input Bias Current		$T_A = 25°C$		50	100		50	100	nA
						200			200	
I_{OS}	Input Offset Current		$T_A = 25°C$		2	5		7	10	
						8			15	
$\Delta I_B/\Delta T$	Input Bias Current Tempco				500			500		pA/°C
A_{VCL}	Closed Loop Gain	Gain Pins Jumpered								V/V
		None			100			100		
		6-10			200			200		
		6-9, 10-5			400			400		
		6-10, 5-9			500			500		
		7-10			1000			1000		
		8-10			2000			2000		
	Closed Loop Gain Error	$A_{VCL} = 100, 200$			0.1	0.3		0.1	0.4	%
		$A_{VCL} = 400, 500$			0.2	0.3		0.2	0.6	
		$A_{VCL} = 1000$			0.3	0.5		0.5	1.0	
		$A_{VCL} = 2000$			1.0	2.0		1.5	3.0	
	Gain Temperature Coefficient	$A_{VCL} = 1k$			7			7		ppm/°C
	Gain Nonlinearity	$100 \le A_{VCL} \le 2k$			1			1		ppm
V_{INCM}	Common-Mode Input Voltage Range			±10	±12		±10	±12		V
V_O	Output Voltage	$R_L \ge 10\ k\Omega$		±10	±12		±10	±12		
V_S	Supply Voltage Range			±5		±18	±5		±18	
	Guard Voltage Error	$-10V < V_{CM} < +10V$			±10	±100		±10	±100	mV
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_{VCL} = 100$	94	110		86	110		dB
			$A_{VCL} = 1000$	114	120		106	110		
PSRR	Power Supply Rejection Ratio	$\pm 5V \le \Delta V_S \le \pm 15V$	$A_{VCL} = 100$	94	110		94	110		
			$A_{VCL} = 1000$	110	120		100	110		

DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions	LH0038			LH0038C			Units
			Min	Typ	Max	Min	Typ	Max	
I_{OSC}	Output Short Circuit Current	T_A = 25°C	±2	±5	±10	±2	±5	±10	mA
I_S	Supply Current	T_A = 25°C		1.6	2.0		1.6	3.0	
R_{IN} DIFF	Input Resistance	A_{VCL} = 1000, T_A = 25°C		5			5		MΩ
R_{IN}^{CM}	Common-Mode Input Resistance			1			1		GΩ
R_{OUT}	Output Resistance			1			1		mΩ

AC Electrical Characteristics V_S = ±15V, T_A = 25°C

Symbol	Parameter	Comment	Conditions		Typ	Units
e_n	Equivalent Input Noise Voltage	*Figure 1*	R_S = 0, f = 0.1 to 10Hz		0.2	μVp-p
$\overline{e_n}$	Equivalent Input Spot Noise Voltage	*Figure 1*	R_S = 100Ω	f = 10 Hz	6.5	nV/√Hz
				f = 100 Hz	6.0	
				f = 1 kHz	6.0	
				f = 10 kHz	6.0	
BW	Large Signal Bandwidth		V_{OUT} = ±10V		1.6	kHz
S_r	Slew Rate		V_{OUT} = ±10V		0.3	V/μs
t_s	Settling Time to 0.01%	*Figure 13*		20V Step	120	μs
				−10V Step	80	
				+10V Step	60	
t_r	Rise Time		ΔV_{OUT}	A_{VCL} = 100	6	μs
				A_{VCL} = 1000	13	
$\overline{i_n}$	Equivalent Input Spot Noise Current		R_S = 100 MΩ	f = 10 Hz	0.1	pA/√Hz

Note 1: The inputs are protected by diodes for overvoltage protection. Excessive currents will flow for differential voltages in excess of ±1V. Input current should be limited to less than 10 mA.

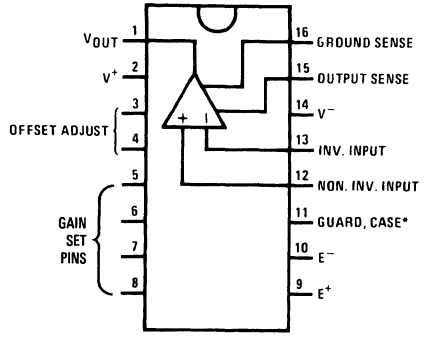
Note 2: Unless otherwise noted these specifications apply for V_S = ±15.0V, pin 15 connected to pin 1, pin 16 connected to ground, over the temperature range −55°C to +125°C for the LH0038 and −25°C to +85°C for LH0038C. $T_A = T_j$ unless otherwise specified.

Note 3: See Typical Performance Characteristics for Thermal Resistance Information.

Note 4: Refer to RETS0038D for LH0038D military specifications.

Connection Diagram

Dual-In-Line Package



TL/H/5543–2

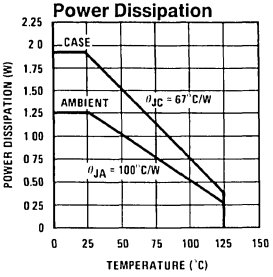
Top View

*Guard output is connected to the case.

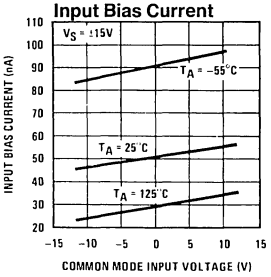
Order Number LH0038 or LH0038CD
See NS Package Number D16D

Typical Performance Characteristics

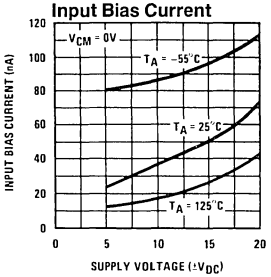
Power Dissipation



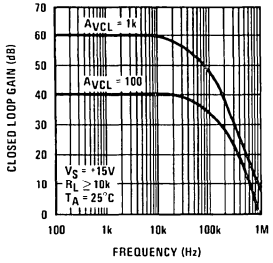
Input Bias Current



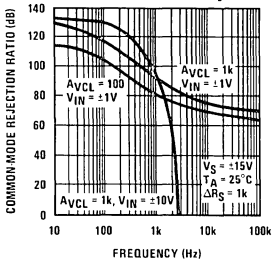
Input Bias Current



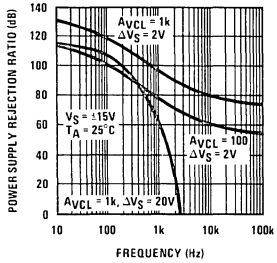
Closed Loop Frequency Response



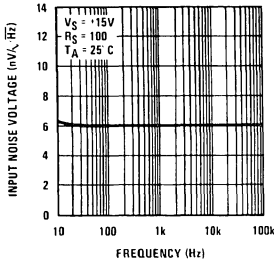
Common-Mode Rejection



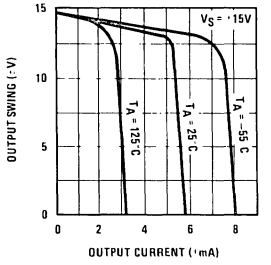
Power Supply Rejection



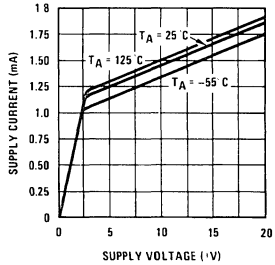
Input Noise Voltage (Includes Source Impedance)



Output Swing

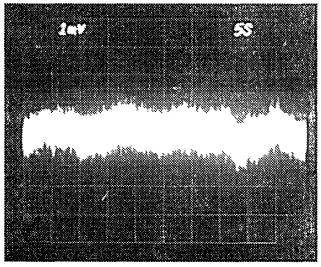


Supply Current



TL/H/5543–3

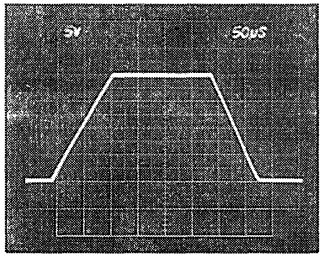
Wide Band Noise



TL/H/5543–4

V_S = ±15V, R_S = 1 kΩ, A_V = 10k, DUT = 1k
Vertical sensitivity: 0.1 μV/CM
Horizontal sensitivity: 5 s/CM
Bandwidth: 0.1 Hz to 10 Hz

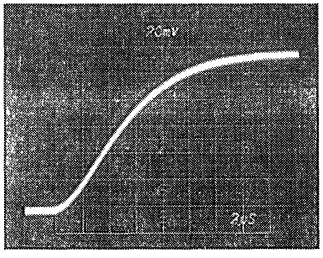
Pulse Response



TL/H/5543–5

V_S = ±15V
R_L ≥ 10 kΩ
A_{VCL} = 1k

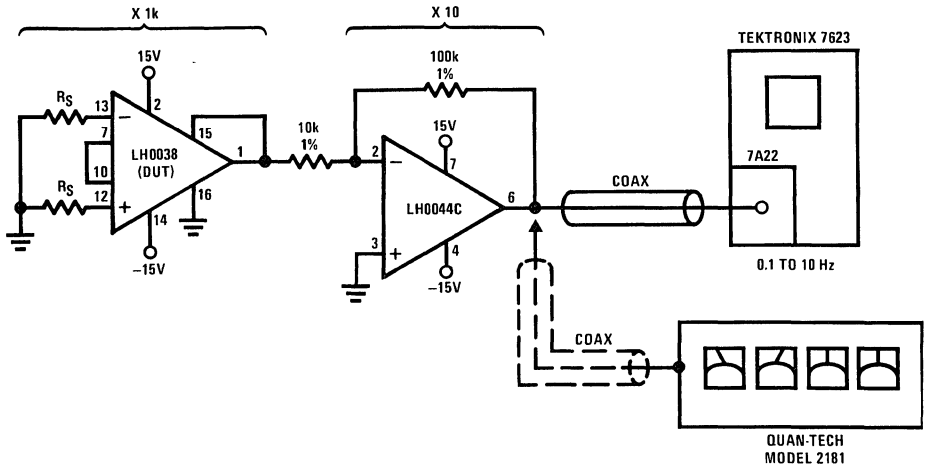
Rise Time



TL/H/5543–6

V_S = ±15V
R_L ≥ 10kΩ
A_{VCL} = 1k

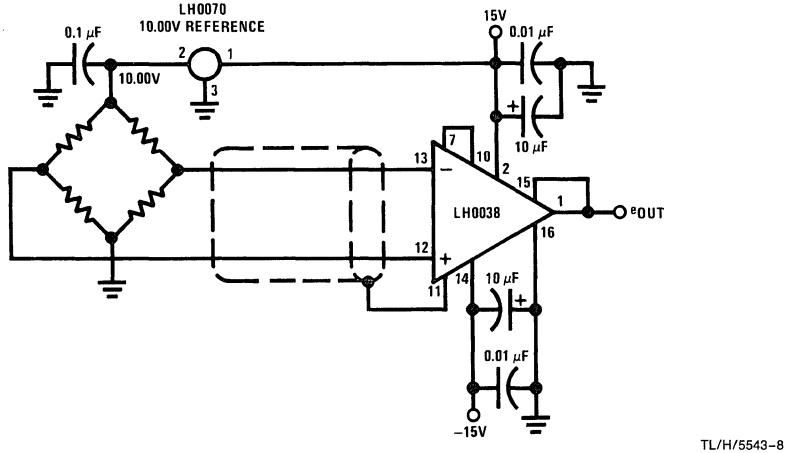
Noise Test Circuit



TL/H/5543–7

FIGURE 1

Typical Application



TL/H/5543–8

FIGURE 2. X1000 Bridge Amplifier

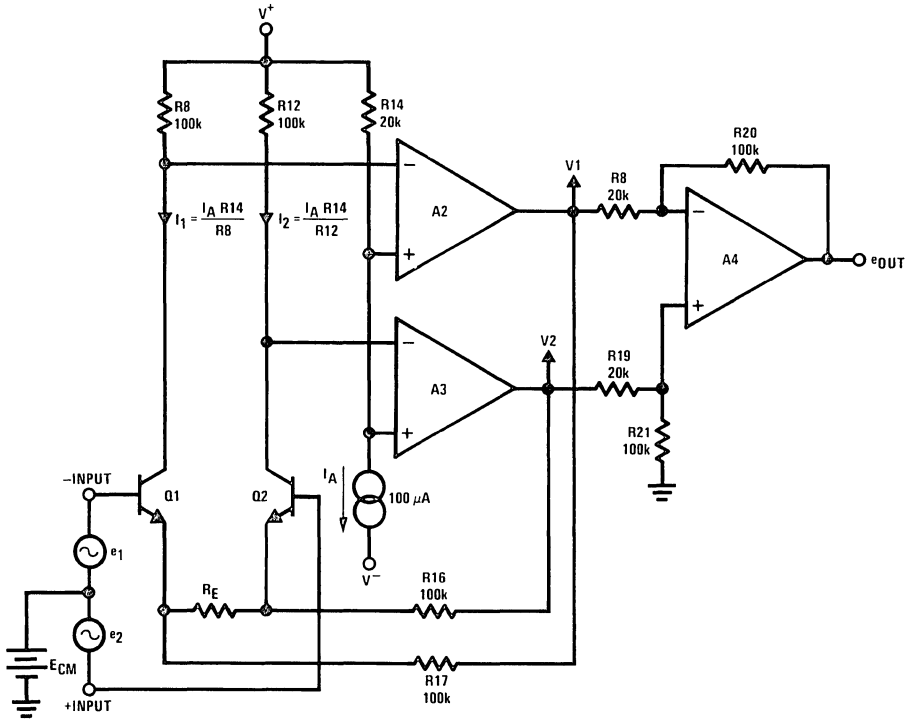
Applications Information

THEORY OF OPERATION

The LH0038 is a 3-stage, true instrumentation amplifier composed of a well matched transistor differential pair, Q1 and Q2, a common-mode loop amplifier, A2 and A3, and a differential to single ended amplifier, A4. A simplified schematic is shown in *Figure 3.*

Current source, I_A, establishes a voltage across R14 of approximately 2V, which results in a 2V drop across R8 and R12. This constant voltage forces the first stage current to be 20 μA per side. The action of A2 and A3 is such that 20 μA is maintained constant despite the presence of common-mode signals. The differential outputs of A2 and A3 are applied to differential amplifier, A4, which converts the signal to a single-ended output and provides gain of 5. The total gain of the amplifier is, therefore, the fixed gain of 5 multiplied by the gain of the composite input stage.

Applications Information (Continued)



TL/H/5543–9

FIGURE 3. LH0038 Simplified Schematic

The closed loop gain of the composite amplifier may be better understood by referring to *Figure 3.* The Q1–A2 loop may be viewed as differential amplifier with the inverting input at the base and non-inverting input at the emitter. Combining small signal AC and large signal DC analysis =

$$v1 = e1\left(\frac{R17 + R_E}{R_E}\right) - e2\left(\frac{R17}{R_E}\right) + E_{CM} - V_{BE1} - I_1R17 \quad (1)$$

By similar analysis:

$$v2 = e2\left(\frac{R16 + R_E}{R_E}\right) - e1\left(\frac{R16}{R_E}\right) + E_{CM} - V_{BE2} - I_2R16 \quad (2)$$

For $I_1 \equiv I_2$, R17 ≡ R16, $V_{BE1} \equiv V_{BE2}$, subtracting equation (1) from (2) results in:

$$v2 - v1 = (e2 - e1)\left(\frac{R16 + R_E}{R_E}\right) + (e2 - e1)\left(\frac{R16}{R_E}\right) \quad (3)$$

$$\frac{v2 - v1}{e2 - e1} = \frac{2\,R16}{R_E} + 1 \quad (4)$$

The differential input voltage (v2 − v1) is amplified by the closed loop gain of A4:

$$e_{OUT} = (A_{VCL4})(e2 - e1) \quad (5)$$

where:

$$A_{VCL4} = \frac{R20}{R8} = 5.00$$

$$\boxed{A_{VCL} = 5\left(\frac{2R16}{R_E} + 1\right)} \quad (6)$$

As an example, with all gain pins open, R_E = 10.525 kΩ, and;

$$A_{VCL} = 5\left(\frac{(2)\,(100k)}{R_E} + 1\right) = 100.0 \quad (7)$$

All other closed loop gain configurations place a precision resistor in parallel with R_E(R9 + R10). For example, for a gain of 200, pin 6 is connected to pin 10 and the gain is predicted by:

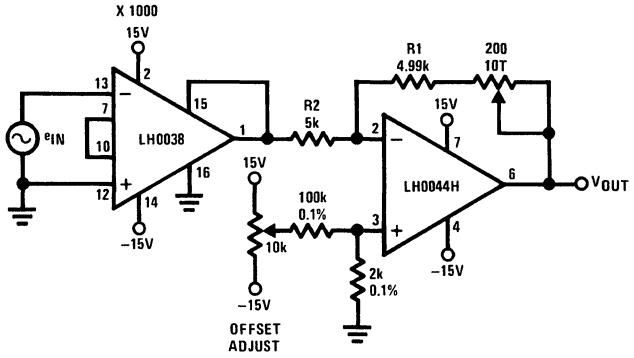
$$A_{VCL} = 5.00\left[\frac{(2)\,(100k)}{(10.526) \parallel (10.000k)} + 1\right] = (5.00)\,(40) = 200 \quad (8)$$

CLOSED LOOP GAIN CONSIDERATIONS USING INTERNAL RESISTORS

Table 1 summarizes the primary gain configurations available with the LH0038. Obviously, other gains are possible. Using the internally supplied resistors has the advantage that R16, R17, and R_E all track thermally, minimizing the device's gain error as a function of temperature.

Gain adjustment by paralleling or series padding internally supplied resistors is generally discouraged since external resistors will generally not thermally track. It is recommended that the gain adjustment be done in a subsequent stage as shown in *Figure 4.*

Applications Information (Continued)



TL/H/5543–10

FIGURE 4. Recommended Gain Adjust Circuit

TABLE I. LH0038 Internal Gain Configurations

Overall Gain	First Stage Gain	Pin Configuration	Effective R_E
100	20	All Gain Pins Open	10.5260 kΩ
200	40	Pin 6 to Pin 10	5.1281 kΩ
400	80	Pin 6 to Pin 9, Pin 10 to Pin 5	2.5316 kΩ
500	100	Pin 6 to Pin 10, Pin 9 to Pin 5	2.0202 kΩ
1000	200	Pin 7 to Pin 10	1.0050 kΩ
2000	400	Pin 8 to Pin 10	0.5013 kΩ

GUARD DRIVE

The LH0038 is provided with a guard drive output, which will always be at the input common-mode voltage. The guard drive amplifier is short-circuit proof and is capable of driving several thousand pF without danger of latch-up or oscillation.

The guard drive tied to a shielded input cable will greatly reduce noise pick-up, and also improve AC CMRR by maintaining the shield at the common-mode voltage. *Figure 5* illustrates the proper use of the guard drive. The guard drive output is also connected to the case to provide electrostatic shielding to the system.

REMOTE OUTPUT SENSE

The feedback network of the LH0038 may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer; e.g. LH0002, may be included within the feedback loop to increase output current capability as shown in *Figure 7.*

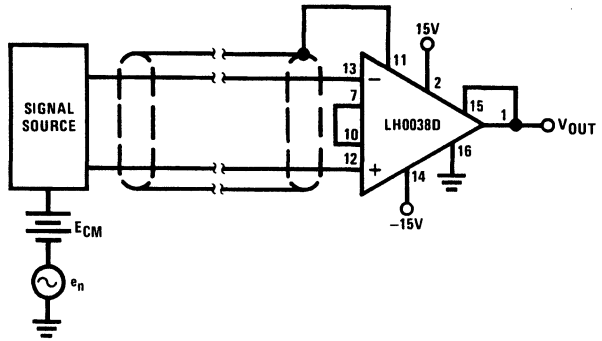


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FIGURE 5. Guard Drive Application

Applications Information (Continued)

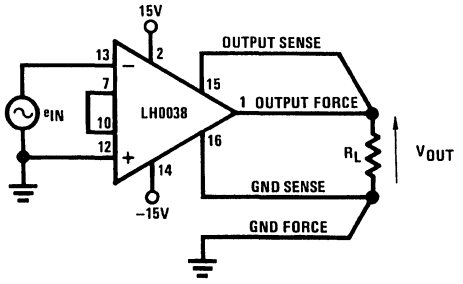

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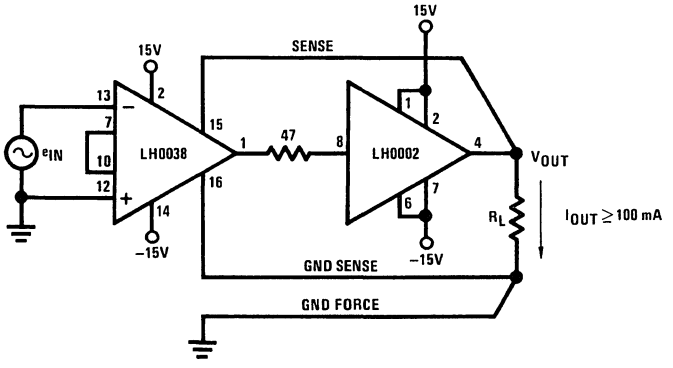
FIGURE 6. Remote Sense Connection



TL/H/5543–13

FIGURE 7. Output Buffer Connection

OFFSET NULL

Offset of the LH0038 is trimmed by the factory to a very low value. The offset may be further trimmed using a 10 kΩ, 10 turn, 100 ppm/°C potentiometer as shown in *Figure 8*. However, a drift increase of 0.3 μV/°C will be caused for each 100 μV of offset adjusted. The recommended offset null is shown in *Figure 4* and is accomplished in the following stage.

BIAS CURRENT CONSIDERATIONS

The LH0038 exhibits bias current of approximately 50 nA per side, and requires a path to ground or supply. The practical limitation to the maximum resistance between the inputs and ground is dictated by negative common-mode range as shown in *Figure 9*. For example, for $V_{CM} = -10V$, $R_{CM} \leq 20\ M\Omega$.

The LH0038 input stage bias was optimized for minimum voltage noise so the input bias currents are higher than might otherwise be expected. Note, however, that the input currents are very well matched, resulting in an offset current value much lower than one might infer from the bias current. In order to take advantage of this low offset current, the source impedances at both inputs should be matched to minimize DC drift. Further, bias current is relatively constant with temperature (as opposed to an FET stage), so one can consider bias current compensation schemes such as shown in *Figure 10*. The danger with such techniques is that the offset current and noise contributed by the bias current compensator will dominate the system noise.

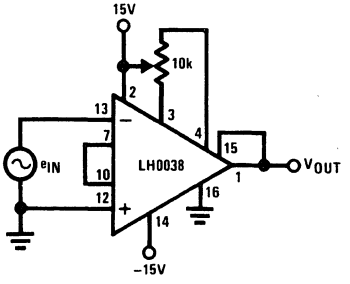


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FIGURE 8. Offset Adjust Circuit (See also *Figure 4*)

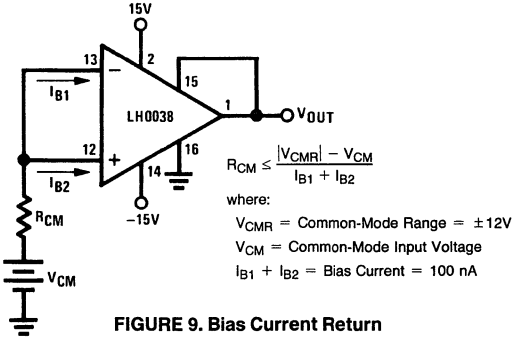


FIGURE 9. Bias Current Return

TL/H/5543–15

Applications Information (Continued)

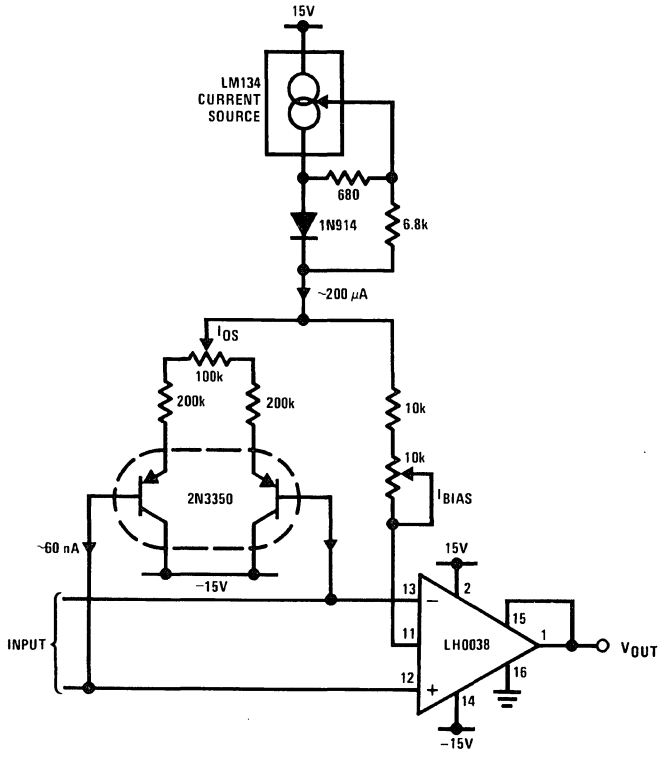


FIGURE 10. Bias Current Compensation

SETTLING TIME

The LH0038 has been purposely over-compensated, and is therefore remarkably free from any undesirable transient response. Small signal settling time is governed by gain-bandwidth product; large signal settling time is dominated by slew rate.

Figure 11 shows an input voltage step of +10V to −10V applied, through a 1000 to 1 voltage divider, to the device configured for an inverting gain of 1000. The output of the device will therefore be equal to the negative of the input after the device is completely settled. By resistively subtracting the input before the divider from the device output, a pseudo summing node is generated. The voltage at this pseudo summing junction goes "off screen" on the photos, since in the first small time increment the input goes instantaneously to −10 mV and the output is still at +10V. About 130 μs after the input has gone negative, the output slews back in range and begins an exponential approach to the final value. *Figure 12* is the same set-up for a −10V to +10V input pulse. Note that there is no overshoot in either case. The test circuit is shown in *Figure 13.*

HIGH FREQUENCY CMRR

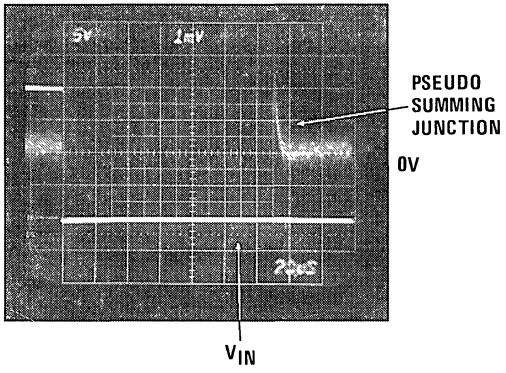
The LH0038 resistor ratios are carefully trimmed for optimum CMRR at DC through 60 Hz. Inevitably, this rejection will degrade at higher frequencies due to 2 separate effects: stray capacitance mismatch and slew rate limiting in the input stage. In most discrete instrumentation amplifier realizations, the stray capacitance mismatch dominates simply because the stray capacitances are relatively large (this can be trimmed out in a discrete amplifier). In a hybrid circuit such as the LH0038, stray capacitance is minimized, so the effects of mismatch are also minimized.

The response to a pulse or noise spike applied as a common-mode signal may be dominated by the slew characteristics of the input stage. Whenever the common-mode input slew rate exceeds 0.2 V/μs, the 2 input amplifiers will apply identical ramp signals to the final stage and cause its output to go to near 0V. Note that the amplifier is not really active under these conditions as normal mode signal variations will *not* be coupled to the output. Some time may be required for the amplifier to settle after a transient of this kind before the output can be considered representative of the input. Slew rate limiting will not normally be the limiting factor for sine wave common-mode signals as 0.2 V/μs corresponds to about 2 kHz (20 Vp-p).

POWER SUPPLY DECOUPLING

Although the LH0038 exhibits in excess of 120 dB PSRR at DC, the figure degrades to 100 dB at 120 Hz. It is recommended that both V^+ and V^- leads be by-passed with 1 μF electrolytic in shunt with 0.01 μF ceramic disc no further than 1 inch from the device.

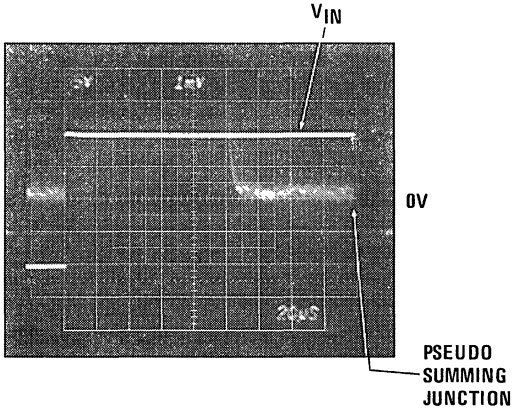
Applications Information (Continued)



TL/H/5543–17

t_S, A_V = 100, V_{IN} = −20V

FIGURE 11. Settling Time



TL/H/5543–18

t_S, A_V = 100, V_{IN} = −20V

FIGURE 12. Settling Time

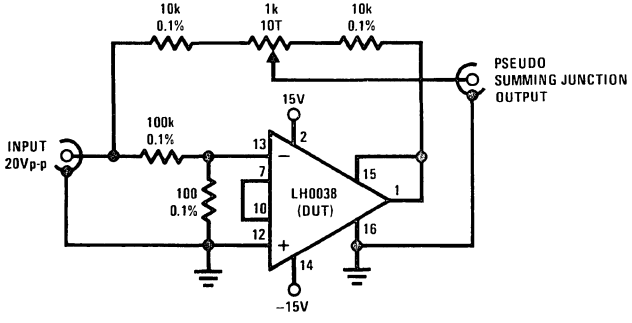


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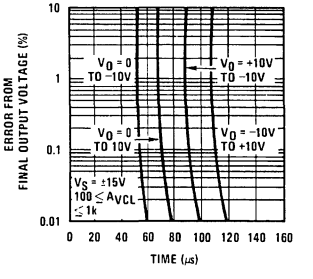
FIGURE 13. Settling Time Test Circuit



TL/H/5543–20

FIGURE 14. Settling Time

6

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to 3 dB below the low frequency.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the outputs of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{IOS} = \frac{(V_{OS})\,2k - (V_{OS})\,100}{1900}$$

Where:

$(V_{OS})2k$ = overall offset voltage for A_{VCL} = 2k.

$(V_{OS})100$ = overall offset voltage for A_{VCL} = 100.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end points expressed as a percent of full-scale (10V for operations on ±15V supply). Note that this is a more stringent specification than deviation from the best straight line and is double the number that would be specified if the percentage were based on a 20V (±10V) range.

Guard Voltage Error: The voltage difference between the guard drive output and the average of the 2 input voltages.

Input Bias Current, I_B: The average of the 2 input currents.

Input Common-Mode Voltage Range, V_{INCM}: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Offset Current, I_{OS}: The difference in the currents into the 2 input terminals when the output is at zero.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Overall Offset Voltage, V_{OS}: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input amplifier offset voltage effects, V_{IOS}, and output amplifier effects, V_{OOS}. It is given by:

$$V_{OS} = (A_{VCL})\,(V_{IOS}) - V_{OOS}$$

Where:

A_{VCL} = closed loop gain = 100 to 2k

V_{IOS} = input stage offset voltage

V_{OOS} = output stage offset voltage

Output Offset Voltage, V_{OOS}: The output voltage when theoutputs of the input stage are forced to 0V. V_{OOS} may be calculated by measuring V_{OS} at closed loop gains of 100 and 2000 and using the following equation:

$$V_{OOS} = \frac{(20)\,(V_{OS})\,100 - (V_{OS})\,2k}{19}$$

Where:

(V_{OS}) 100 = overall offset voltage for A_{VCL} = 100

(V_{OS}) 2k = overall offset voltage for A_{VCL}

Output Voltage, V_O: The peak output voltage swing, referred to zero.

Offset Voltage Temperature Drift, $\Delta V_{IOS}/\Delta T$: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection Ratio, PSRR: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling times, t_S: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate, S_r: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current, $\pm I_S$: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Supply Voltage Range: The range of voltages on the supply terminals for which the device is operational. Note that the specifications are not guaranteed over the full supply voltage range unless specifically stated.

Transient Response, t_r: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from DC to the frequency where the amplifier open loop gain rolls off to 1.

Closed Loop Gain, A_{VCL}: The ratio of output voltage to input voltage under the stated conditions of source resistance (R_S) and load resistance (R_L).

Voltage Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

National Semiconductor

LH0084/LH0084C Digitally-Programmable-Gain Instrumentation Amplifier

General Description

The LH0084/LH0084C is a self-contained, high speed, high accuracy, digitally-programmable-gain instrumentation amplifier. It consists of paired FET-input variable-gain voltage-follower input stages followed by a differential-to-single-ended output stage. The input stage is programmable in accurate gain steps of 1, 2, 5, or 10 controlled by the logic levels of a 2-bit TTL-compatible digital input word. For additional flexibility, the output stage is pin-strappable to fixed gains of 1, 4, or 10 for an overall gain range of 1 to 100.

Applications include increased dynamic range A-to-D converters, test systems, and post multiplexer amplifier for data acquisition systems.

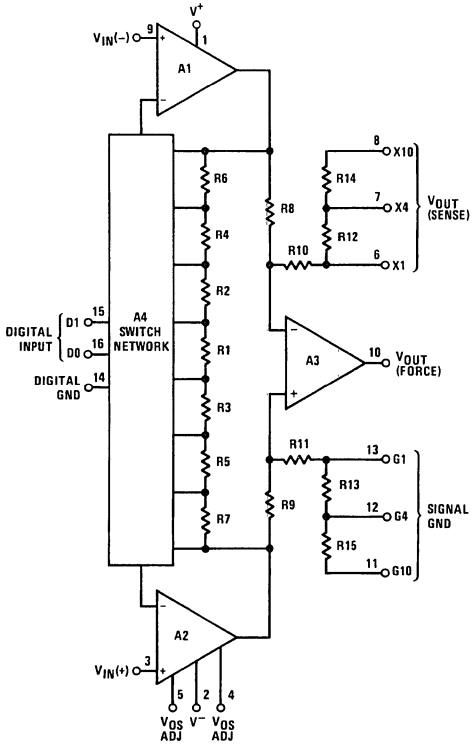
The device exhibits high input impedance, low offset voltage, high PSRR, high speed, and excellent gain accuracy and gain non-linearity.

The LH0084 is guaranteed from −55°C to +125°C. The LH0084C is guaranteed from −25°C to +85°C. Both devices are provided in a hermetically sealed 16-lead dual-in-line metal package.

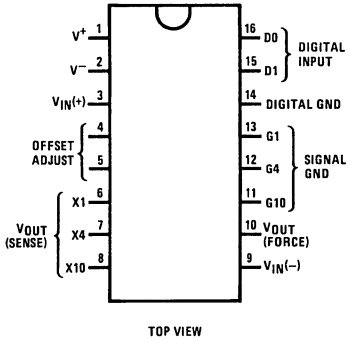
Features

- Excellent gain accuracy — 0.075% max
  and low gain non-linearity — 0.01% typ
- Extremely low gain drift — 1 ppm/°C typ
  10 ppm/°C max
- High input impedance — $10^{11}\Omega$ typ
- High PSRR — 70 dB min
- TTL compatible digital inputs
- High speed, settling to 0.1% — 4 μs max

Simplified Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Case is electrically isolated

Order Number LH0084D or LH0084CD
See NS Package D16D

TL/H/5651–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage (Note 1)	±18V
Analog Input Voltage (Note 2)	±15V
Differential Input Voltage (Note 2)	±30V
Digital Input Voltage	−4V, +18V
Power Dissipation (Note 5)	2.5W
Output Short Circuit Duration	Continuous
Operating Temperature Range	
LH0084	−55°C to +125°C
LH0084C	−25°C to +85°C
Lead Temp. (Soldering, 10 seconds)	+260°C

ESD rating to be determined.

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless noted

Symbol	Parameter	Conditions		LH0084			LH0084C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IOS}	Input Offset Voltage		$T_j = 25°C$		0.3	5		0.3	10	mV
						7			13	
$\Delta V_{IOS}/\Delta T$	Input Offset Voltage Change with Temperature	$R_S = 100\Omega$ $V_{CM} = 0$			10			10		μV/°C
V_{OOS}	Output Offset Voltage	(Note 3)	$T_j = 25°C$		0.6	5		0.6	10	mV
						7			13	
$\Delta V_{OOS}/\Delta T$	Output Offset Voltage Change with Temperature				20			20		μV/°C
I_B	Input Bias Current		$T_j = 25°C$		150	500		150	500	pA
	(Note 4)					500			100	nA
I_{OS}	Input Offset Current		$T_j = 25°C$		50	200		50	200	pA
						200			50	nA
R_{IN}	Input Resistance	Differential			10^{11}			10^{11}		Ω
		Common-Mode			10^{11}			10^{11}		
V_{IN}	Input Voltage Range			±10			±10			V
A_V	Voltage Gain	See Table I			1 2 5 10 20 50 100			1 2 5 10 20 50 100		V/V
	Gain Error	$A_V = 1, 2, 5$	$T_A = 25°C$		0.01	0.075		0.02	0.15	%
		$A_V = 10, 20, 50, 100$			0.02	0.1		0.03	0.2	
		$A_V = 1, 2, 5$			0.02	0.2		0.02	0.2	
		$A_V = 10, 20, 50, 100$			0.03	0.3		0.03	0.3	
	Gain Nonlinearity		$T_A = 25°C$		0.002			0.002		
					0.005			0.005		
$\Delta A_V/\Delta T$	Gain Temperature Coefficient				1	10		1	10	ppm/°C
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	$A_V = 1$	70	80		70	80		dB
			$A_V = 10$	76	94		76	94		
			$A_V = 100$	80	94		80	94		
PSRR	Power Supply Rejection Ratio	$\pm 8V \leq V_S \leq +18V$	$A_V = 1$	70	84		70	84		dB
			$A_V = 10$	76	92		76	92		
			$A_V = 100$	80	104		80	104		
V_O	Output Voltage Swing	$R_L \geq 10\ k\Omega$		±10	±12		±10	±12		V
I_O	Output Short Circuit Current		$T_A = 25°C$	±5	±18	±40	±5	±18	±40	mA
				±2		±40	±2		±40	

DC Electrical Characteristics (Continued) $V_S = \pm 15V$, $R_L = 10\ k\Omega$, $T_{MIN} \le T_A \le T_{MAX}$ unless noted

Symbol	Parameter	Conditions	LH0084			LH0084C			Units
			Min	Typ	Max	Min	Typ	Max	
R_O	Output Resistance			0.05			0.05		Ω
V_{IL}	Digital "0" Input Voltage				0.7			0.7	V
V_{IH}	Digital "1" Input Voltage		2.0			2.0			V
I_{IL}	Digital "0" Input Current	$V_{IN} = 0.4V$		1.5	40		1.5	40	μA
I_{IH}	Digital "1" Input Current	$V_{IN} = 2.4V$		0.01			0.01		μA
V_S	Supply Voltage Range		±8		±18	±8		±18	V
$I_S(+)$	Positive Supply Current	$V_S \le \pm 18V$		12	18		12	26	mA
$I_S(-)$	Negative Supply Current			8	12		8	14	mA
P_D	Power Dissipation	$V_S = \pm 15V$		315	450		315	600	mW

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 10\ k\Omega$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
BW	Bandwidth (*Figure 1*)	Small Signal, −3 dB	$A_V = 1$		3250		kHz
			$A_V = 10$		500		
			$A_V = 100$		350		
		Small Signal, −1%	$A_V = 1$		300		
			$A_V = 10$		75		
			$A_V = 100$		55		
PBW	Power Bandwidth	$V_O = \pm 10V$			200		
SR	Slew Rate			10	13		V/μs
t_s	Settling Time (*Figure 2*) ±0.1%	$\Delta V_o = \pm 20V$	$A_V = 1$		2.3	3.0	μs
			$A_V = 10$		2.7	3.5	
			$A_V = 100$		3.1	4.0	
	Gain Switching Time				3.5		
E_N	Equivalent Input Noise Voltage (*Figure 3*)	BW = 0.1 Hz − 10 Hz	$A_V = 100$		7		μVp-p
		BW = 10 Hz − 10 kHz			1.4		μVrms
I_N	Equivalent Input Noise Current (*Figure 3*)	BW = 10 Hz − 10 kHz			30		pArms

Note 1: Improper supply power-on sequence may damage the device. See Power Supply Connection section under Applications Information.

Note 2: For supply voltages less than ±15V the maximum input voltage is equal to the supply voltage.

Note 3: These parameters are specified at junction temperature, T_J. In normal operation the junction temperature rises above the ambient temperature, T_A, as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient.

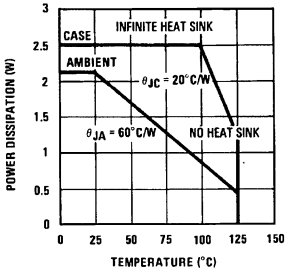
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Note 5: See Typical Performance Characteristics for Thermal Resistance Information.

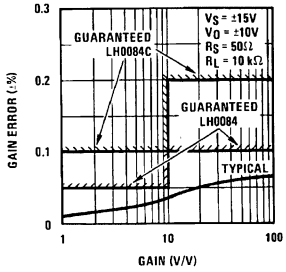
Note 6: Refer to RETS0084D for LH0084D military specifications.

Typical Performance Characteristics

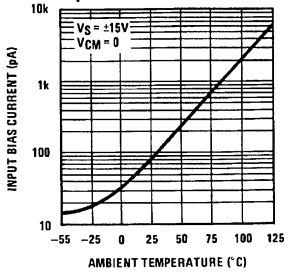
Power Dissipation



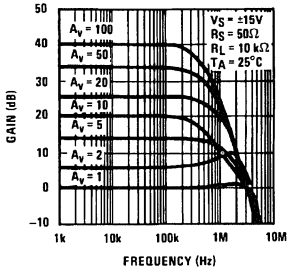
Gain Accuracy



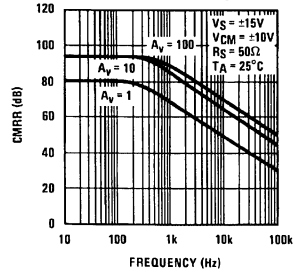
Input Bias Current



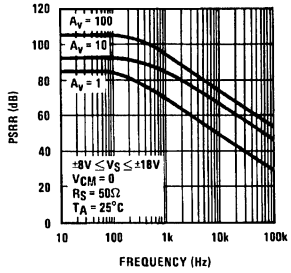
Small Signal Frequency Response



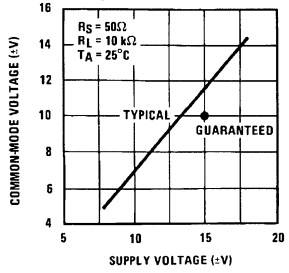
Common-Mode Rejection



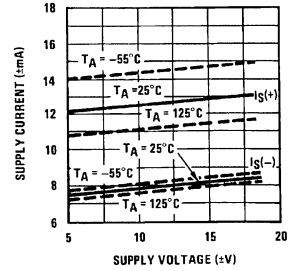
Power Supply Rejection



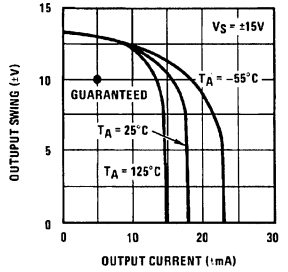
Input Common-Mode Range



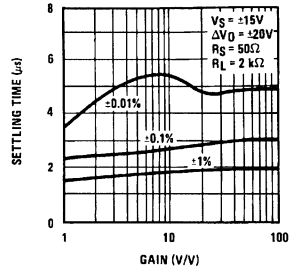
Supply Current



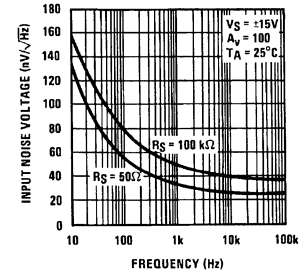
Output Swing



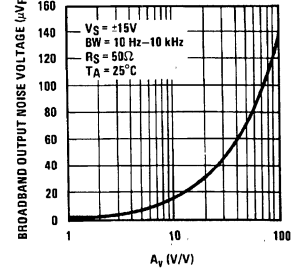
Settling Time



Equivalent Input Noise Voltage (Includes Source-Resistance Noise)



Broadband Output Noise Voltage



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AC Test Circuits

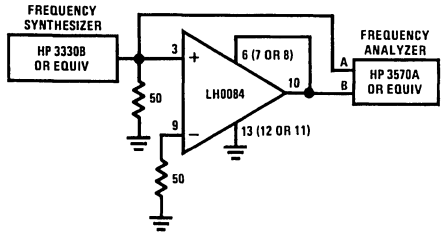


FIGURE 1. Frequency Response Measurement Circuit

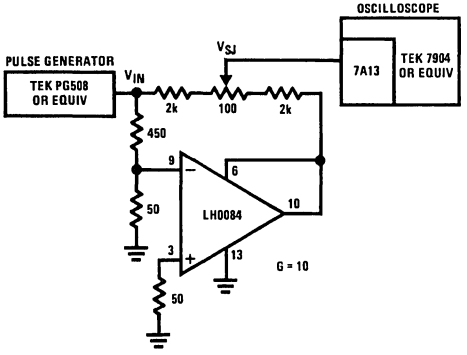
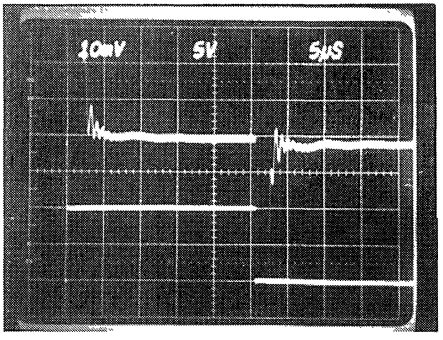


FIGURE 2. Settling Time Measurement Circuit

Settling Time



$A_V = 10$ Input Stage

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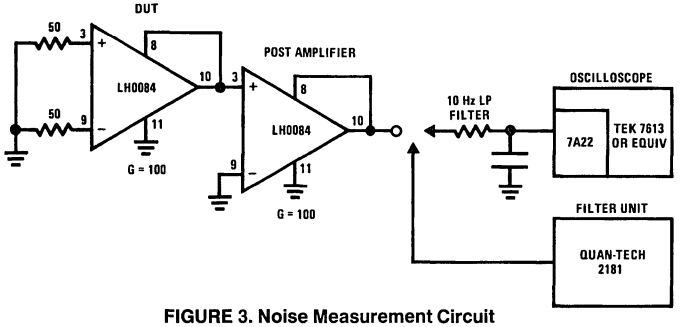

FIGURE 3. Noise Measurement Circuit

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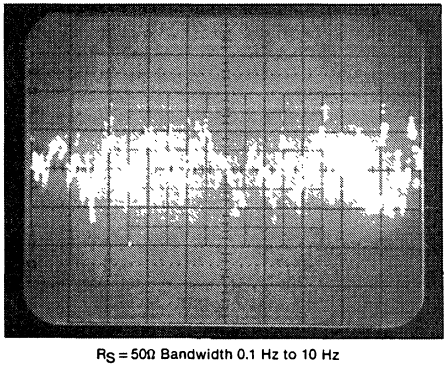
Wideband Noise



$R_S = 50\Omega$ Bandwidth 0.1 Hz to 10 Hz
1μV/Division Vertical 5 Seconds/Division Horizontal

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Applications Information

THEORY OF OPERATION

The LH0084 is a digitally-programmable-gain true-instrumentation amplifier composed of a variable-gain voltage-follower input stage (A1 and A2), followed by a differential output stage (A3). The schematic is shown in *Figure 4.*

The input stage contains matched high-speed FET-input op amps (A1 and A2). A high-stability temperature-compensated resistor network (R1 through R7) controls feedback ratios at the inverting inputs of op amps A1 and A2 via FET switches S1A–S4A and S1B–S4B. Since the FET switches are in series with the op amp input impedance their resistance match and temperature drift do not degrade the gain accuracy of the instrumentation amplifier. The FET switches are controlled through a 1-of-4 decoder and switch driver, by the logic levels applied at the digital input terminals D1 and D0 and set the gain of the input stage as shown in Table I.

If, for example, D1 is High (≥2.0V) and D0 is Low (≤0.7V), FET switch pair S3A and S3B will be closed (and all remaining switches open). The input stage gain, $A_{V(1)}$, can then be shown to be:

$$A_{V(1)} = \frac{V2 - V1}{V_{IN}(+) - V_{IN}(-)}$$

$$= 1 + \frac{R4 + R5 + R6 + R7}{R1 + R2 + R3}$$

$$= 1 + \frac{6k + 6k + 10k + 10k}{4k + 2k + 2k}$$

$$= 5$$

Schematic Diagram

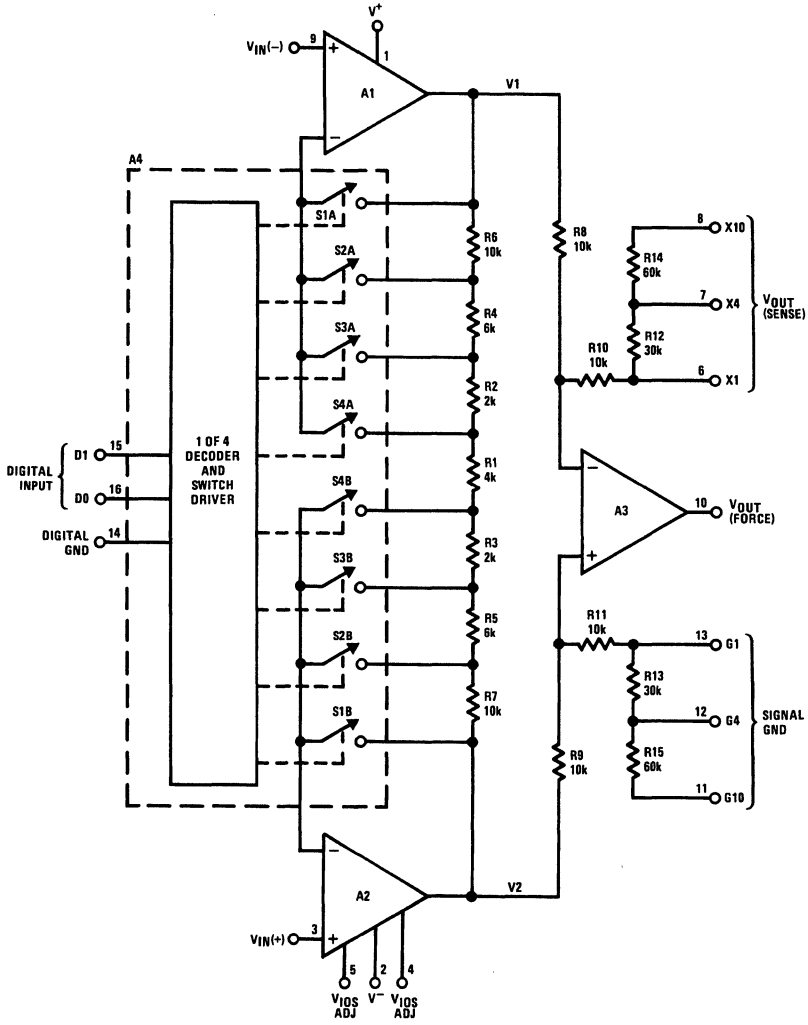

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FIGURE 4

Applications Information (Continued)

TABLE I. Gain Truth Table and Connection Table

Digital Inputs		1st Stage Gain	Pin Connections	2nd Stage Gain	Overall Gain
D1	D0	$A_{V(1)}$		$A_{V(2)}$	A_V
0	0	1	6-10, 13-GND	1	1
0	1	2			2
1	0	5			5
1	1	10			10
0	0	1	7–10, 12-GND	4	4
0	1	2			8
1	0	5			20
1	1	10			40
0	0	1	8–10, 11-GND	10	10
0	1	2			20
1	0	5			50
1	1	10			100

The output stage, consisting of op amp A3 and resistors R8 through R15, converts the voltage difference at the output of the input stage, V2 minus V1, to a single-ended output. For increased flexibility of the LH0084, the output stage gain is pin-strappable by selecting R10, R10+R12, or R10+R12+R14 as feedback resistor for A3. The ratios of these resistors to the differential stage input resistor R3 are kept very accurate to maintain the excellent overall gain accuracy of the device. The output stage gain, $A_{V(2)}$, is equal to the feedback resistance divided by the input resistance. Thus with, for example, Pin 7 wired to Pin 10, that gain would be:

$$A_{V(2)} = \frac{V_{OUT}}{V2-V1} = \frac{R10+R12}{R8} = \frac{10K+30K}{10k} \quad (2)$$

To preserve the high common-mode rejection ratio of the output stage, the ground sense resistor, R11, R11+R13 or R11+R13+R15, must match the feedback resistor used.

The overall gain of the LH0084 is therefore:

$$A_V = \frac{V_{OUT}}{V_{IN}(+)-V_{IN}(-)} = \frac{V2-V1}{V_{IN}(+)-V_{IN}(-)} \bullet \frac{V_{OUT}}{V2-V1} = A_{V(1)} \bullet A_{V(2)} \quad (3)$$

The different gains available are in the range of 1 through 100 and are summarized in Table I.

POWER SUPPLY CONNECTIONS

Proper power supply connections are shown in *Figure 5*. The power supplies should be bypassed to ground as close as possible to device supply pins. For optimum high speed performance V+ and V− should be decoupled with a 0.01 μF ceramic disc in parallel with a 1 μF electrolytic capacitor.

The two ground pins, analog and digital grounds, should be connected together as close to the device as possible, preferably with a ground plane underneath the device. If this is not possible, the grounds should be connected together locally with back-to-back diodes and hard-wired together offboard. If a ground reference offset is used, it must be low impedance compared to the ground sense resistance to avoid CMRR degradation.

Care must be taken in the supply power-on sequence. The LH0084 may suffer irreversible damage if the V+ supply is applied prior to the powering on the V− supply. In most applications using dual tracking supplies and with the device supply pins adequately bypassed, this will not present a problem. If this cannot be guaranteed, a germanium or Schottky protection diode should be connected between the digital ground pin and the V− pin as shown in *Figure 5*.

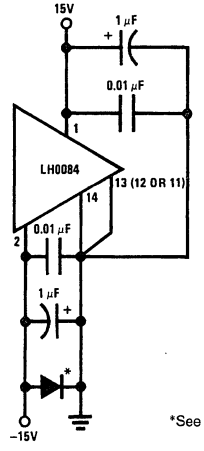

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FIGURE 5. Power Supply Connections

Applications Information (Continued)

SIGNAL CONNECTIONS

The input signals should be connected as shown in *Figure 6*. To minimize errors, $R_S(+)$, $R_S(-)$ and R_{CM} should be kept as small as possible.

The output connections are also shown in *Figure 6*. The feedback leads should be kept short as should the ground sense in order to minimize lead resistance and parasitic capacitance.

OFFSET AND GAIN ADJUSTMENTS

Special care must be taken when using external offset adjustment. Since the LH0084 is a 2-stage amplifier with each stage contributing offset errors, and the amplifier presumably is used at several different gains, it is important to realize that the offsets of both the 1st and the 2nd stages must be nulled to maintain zero offset referred to output (RTO) at all gain settings.

In general, it is recommended that the input stage offset (V_{IOS}) be adjusted with a potentiometer as shown in *Figure 7*. The output stage offset (V_{OOS}) is ideally adjusted at a subsequent gain stage (i.e. sample-and-hold or A-to-D converter), but if this is impractical, it may also be done as shown in *Figure 7*.

Recommended offset adjust procedure is as follows: Initially set both pots to center positions and short both inputs of the LH0084 to ground.

a) Set the input stage gain to 1 (pull D1 and D0 low). Measure the output voltage, V_{OUT1}.

b) Set the input stage gain to 10 (pull D1 and D0 high). Measure the new output voltage, V_{OUT2}.

c) Calculate the portion of V_{OUT2} contributed by the output stage offset per the equation:

$$V_{OOS} = \frac{1}{9}(10 \bullet V_{OUT1} - V_{OUT2}) \quad (4)$$

d) While maintaining an input stage gain of 10, adjust the input offset voltage (V_{IOS}) potentiometer until the output voltage is equal to the voltage calculated in Equation (4).

e) Change the input back to a gain of 1 and adjust the output offset voltage (V_{OOS}) potentiometer until the output voltage is zero.

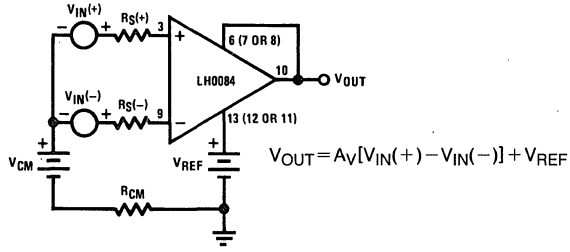

FIGURE 6. Signal Connections

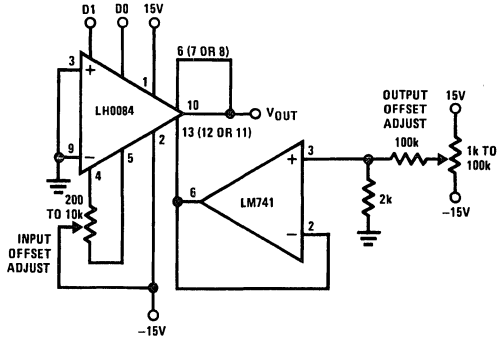

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FIGURE 7. Offset Adjust Circuit

Applications Information (Continued)

An alternate offset adjust scheme is shown in *Figure 8*. The offset should be rezeroed after each time the gain is changed or when the op amp integrator drift warrants a new zero pulse. An additional advantage of this adjustment technique is that it can also be used to cancel out offset voltage drift and common-mode voltage error contributions.

External gain adjustment is generally discouraged since gain accuracy can be optimized for one gain setting only. If gain adjustment is required, however, it should be done at a subsequent gain stage.

LOGIC CONNECTIONS

The digital inputs D1 and D0 are referenced to the digital ground. The device interfaces directly to TTL and, with pull-down resistors, to CMOS.

Interfacing with microprocessors will usually require a latch. A circuit using full 6-bit wide address decode and write strobe is shown in *Figure 9*.

REMOTE OUTPUT SENSE

The feedback resistors of the LH0084 can be connected directly at the load in order to eliminate errors due to lead resistance *(Figure 10)*.

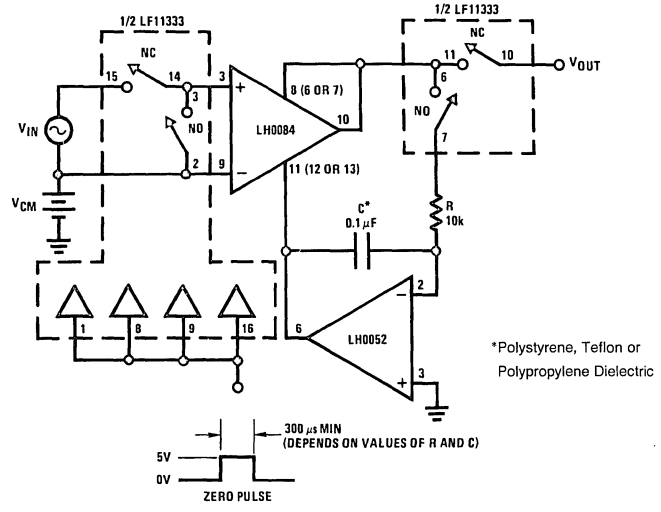

FIGURE 8. Auto Zero Circuit

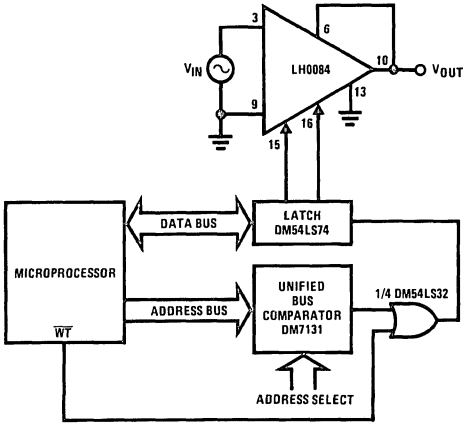

FIGURE 9. Typical Microprocessor Interface

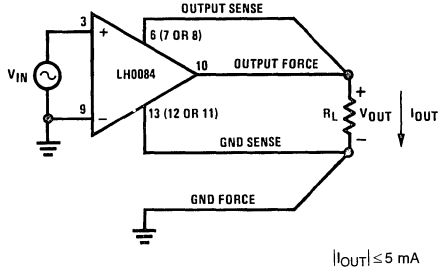

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FIGURE 10. Remote Sense Connection

Applications Information (Continued)

Also, a unity gain buffer, such as the LH0033, may be included in the feedback loop for increased current drive capability as shown in *Figure 11*.

The output sense feature can also be used in other ways such as output offset, *Figure 12*, or current source output, *Figure 13*.

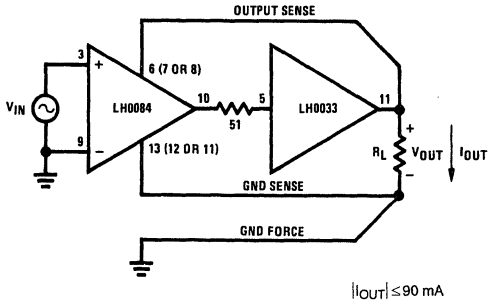

FIGURE 11. Buffered Output Connection

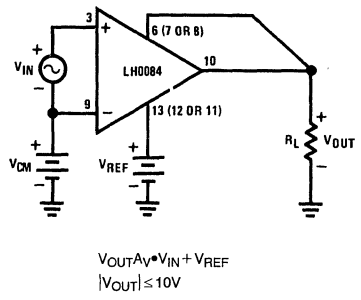

FIGURE 12. Output Offset Connection

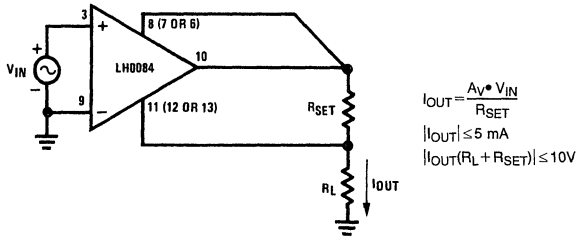

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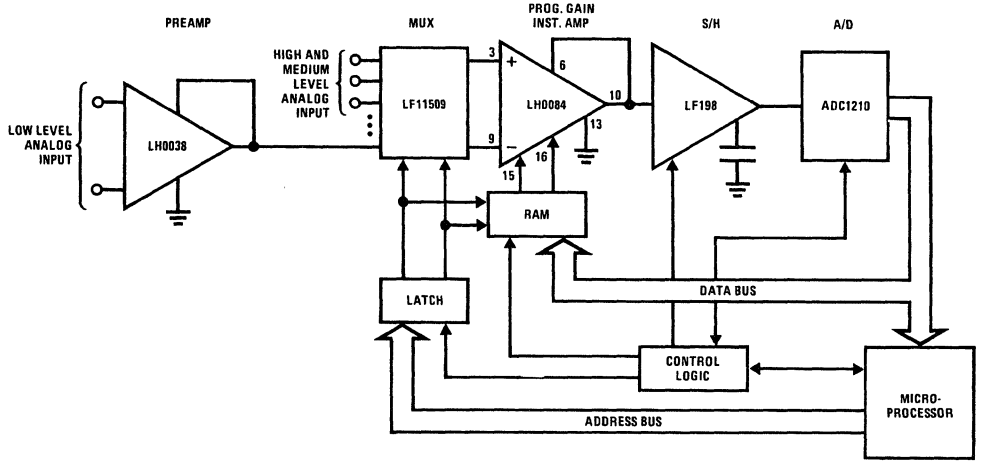
FIGURE 13. Output Current Source Connection

Applications

The LH0084 is ideal for application in increased dynamic range A-to-D converters, test systems, process control, and multi-channel data acquisition system. *Figure 14* shows the device used in a typical data acquisition system.

A software offset and gain error correction scheme is shown in *Figure 15*. By first selecting a multiplexer input connected to analog ground, and then selecting a channel connected to a reference of known value, the overall system gain and offset errors can be calculated. For all subsequent readings, offset and gain corrections can be made mathematically by solving a simple first-order equation in software.



TL/H/5651–11

FIGURE 14. Typical Data Acquisition System

Applications (Continued)

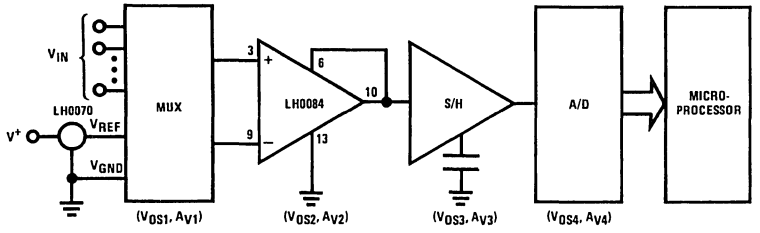


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FIGURE 15. Software System Offset and Gain Calibration Circuit

Definition of Terms

Input Offset Voltage, V_{IOS}: The voltage which must be applied to the inputs to force the output of the input stage to 0V. V_{IOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and using the following equation:

$$V_{IOS}=\frac{1}{9}\left(V_{OS}|_{A_V=10}-V_{OS}|_{A_V=1}\right)$$

where:

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V=10$

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V=1$

Input Offset Current, I_{OS}: The difference in the currents into the 2 analog input terminals at 0V.

Input Bias Current, I_B: The average of the currents into the 2 analog input terminals at 0V.

Input Resistance, R_{IN}: Common-mode input resistance is the change in input voltage range divided by the change in input bias current with both analog inputs at the same voltage. Differential input resistance is the change in input voltage at one input terminal divided by the change in input current at the other input terminal which is kept still at 0V.

Input Voltage Range, V_{IN}: The voltage range for which the device is operational.

Common-Mode Rejection Ratio, CMRR: The ratio of the input common-mode voltage range to the change in input offset voltage over this range.

Power Supply Rejection Ratio, PSRR: The ratio of the specified change in supply voltage to the change in input offset voltage over this range.

Voltage Gain, A_V: The ratio of output voltage change to the input voltage change producing it.

Gain Error: The deviation in percent between the ideal voltage gain and the value obtained when the device is configured for that gain.

Gain Non-Linearity: The deviation of the gain from a straight line drawn through the end-points expressed as a percent of full-scale (10V for operation with ±15V supply). For testing purposes it is the difference between positive swing gain (0V to 10V) and average gain (−10V to 10V) or between negative swing gain (0V to −10V) and average gain.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage for the output to be forced to 0V. V_{OOS} can be calculated by measuring V_{OS} (RTO) at input stage gains of 1 and 10 and applying the following equation:

$$V_{OOS}=\frac{1}{9}\left(10 \bullet V_{OS}|_{A_V=1}-V_{OS}|_{A_V=10}\right)$$

where:

$V_{OS}|_{A_V=1}$ = Overall offset (RTO) for $A_V=1$

$V_{OS}|_{A_V=10}$ = Overall offset (RTO) for $A_V=10$

Offset Voltage (Referred to Output), $V_{OS(RTO)}$: The output voltage when both inputs are connected to 0V. V_{OS} is composed of input offset voltage, V_{IOS}, and output offset voltage, V_{OOS}, and is a function of amplifier gain. The overall offset voltage is given by:

$$V_{OS(RTO)}=A_{V(2)}(A_{V(1)}\ V_{IOS}+V_{OOS})$$

where:

V_{IOS} = Input offset voltage

V_{OOS} = Output stage offset voltage

$A_{V(1)}$ = Input state gain

$A_{V(2)}$ = Output stage gain

Definition of Terms (Continued)

Output Voltage Swing, V_O: The peak output voltage swing referenced to ground into specified load.

Output Short-Circuit Current, I_O: The current supplied by the device with the output connected directly to ground.

Output Resistance, r_o: The ratio of change in output voltage to change in output current around zero output.

Supply Voltage Range, V_S: The supply voltage range for which the device is operational.

Supply Current, I_S: The current required from the supply to operate the device with zero load and with the analog as well as the digital inputs at 0V.

Power Dissipation, P_D: The power dissipated in the device with zero load and with the analog as well as the digital inputs at 0V.

Digital "1" Input Voltage, V_{IH}: Minimum voltage required at the digital input to guarantee a high logic state.

Digital "0" Input Voltage, V_{IL}: Maximum voltage required at the digital input to guarantee a low logic state.

Digital "1" Input Current, I_{IH}: The current into a digital input at specified logic level.

Digital "0" Input Current, I_{IL}: The current into a digital input at specified logic level.

Average Input Offset Voltage Drift, $\Delta V_{IOS}/\Delta T$: The ratio of input offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Output Offset Voltage Drift, $\Delta V_{OOS}/\Delta T$: The ratio of output offset voltage change from 25°C to either temperature extreme divided by the temperature range.

Average Gain Temperature Coefficient, $\Delta A_V/\Delta T$: The ratio of change in gain from 25°C to either temperature extreme divided by the temperature range.

Small Signal Bandwidth, BW: The frequency at which the device gain changes from the low frequency gain by a specified amount.

Power Bandwidth, PBW: Maximum frequency for which the output swing is a large signal sinewave without noticeable distortion.

Slew Rate, SR: The internally limited rate of change in output voltage with a large amplitude step function applied at the input.

Settling Time, t_S: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Gain Switching Time: The time between the initiation of a gain logic change and the time when the final gain switches are closed. It includes overdrive recovery time, but not settling to final value.

Equivalent Input Noise Voltage, E_N: The rms of peak noise voltage referred to the input (RTI) over a specified frequency band.

Equivalent Input Noise Current, I_N: The rms of peak noise current referred to the input (RTI) over a specified frequency band.

National Semiconductor

LM221/LM321/LM321A Precision Preamplifiers

General Description

The LM121 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM121 decreases the closed loop gain error.

The LM121 series operates with supply voltages from ±3V to ±20V and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from 5 μA to 200 μA so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

The extremely low drift of the LM121 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with the LM121. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM121 allows tailoring the input characteristics to match those of specialized op amps.

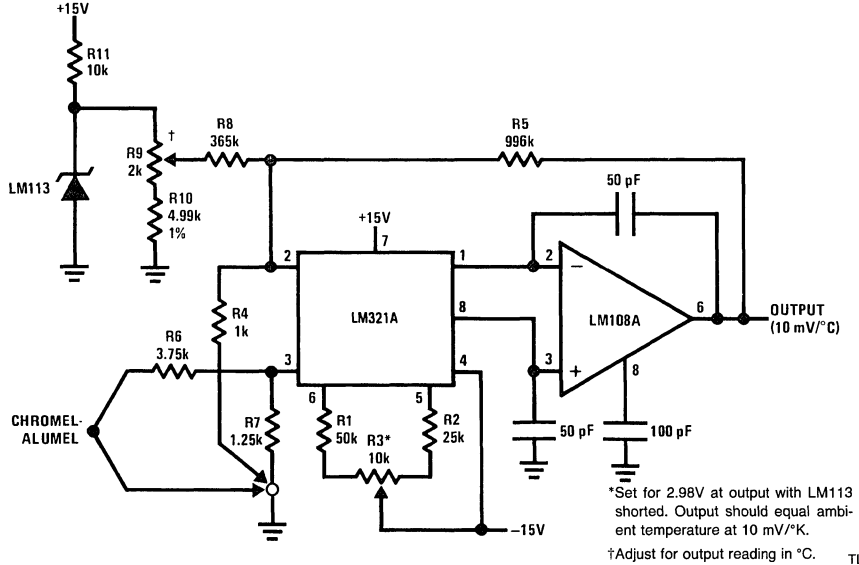
The LM221 is specified over a −25°C to +85°C range and the LM321 over a 0°C to +70°C temperature range.

Features

- Guaranteed drift of LM321A—0.2 μV/°C
- Guaranteed drift of LM221 series—1 μV/°C
- Offset voltage less than 0.4 mV
- Bias current less than 10 nA at 10 μA operating current
- CMRR 126 dB minimum
- 120 dB supply rejection
- Easily nulled offset voltage

Typical Applications

Thermocouple Amplifier with Cold Junction Compensation



*Set for 2.98V at output with LM113 shorted. Output should equal ambient temperature at 10 mV/°K.

†Adjust for output reading in °C.

TL/H/7769–1

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V
Operating Temperature Range LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4) LM321A

Parameter	Conditions	LM321A			Units
		Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $6.4k \le R_{SET} \le 70k$		0.2	0.4	mV
Input Offset Current	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$		 0.3	 0.5 5	 nA nA
Input Bias Current	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$		 5 50	 15 150	 nA nA
Input Resistance	$T_A = 25°C$, $R_{SET} = 70k$ $R_{SET} = 6.4k$	 2 0.2	 8		 MΩ MΩ
Supply Current	$T_A = 25°C$, $R_{SET} = 70k$		0.8	2.2	mA
Input Offset Voltage	$6.4k \le R_{SET} \le 70k$		0.5	0.65	mV
Input Bias Current	$R_{SET} = 70k$ $R_{SET} = 6.4k$		15 150	25 250	nA nA
Input Offset Current	$R_{SET} = 70k$ $R_{SET} = 6.4k$		0.5 5	1 10	nA nA
Input Offset Current Drift	$R_{SET} = 70k$		3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$ Offset Voltage Nulled		 0.07	 0.2	 μV/°C
Long Term Stability			3		μV/yr
Supply Current			1	3.5	mA
Input Voltage Range	$V_S = \pm 15V$, (Note 5) $R_{SET} = 70k$ $R_{SET} = 6.4k$	 ±13 +7, −13			 V V
Common-Mode Rejection Ratio	$R_{SET} = 70k$ $R_{SET} = 6.4k$	126 120	140 130		dB dB
Supply Voltage Rejection Ratio	$R_{SET} = 70k$ $R_{SET} = 6.4k$	118 114	126 120		dB dB
Voltage Gain	$T_A = 25°C$, $R_{SET} = 70k$, $R_L > 3\ M\Omega$	 12	 20		 V/V
Noise	$R_{SET} = 70k$, $R_{SOURCE} = 0$		8		nV/√Hz

Note 1: The maximum junction temperature of the LM321A is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221A, however all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321A the specifications apply over a 0°C to +70°C temperature range.

Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V
Operating Temperature Range	
LM221	−25°C to +85°C
LM321, LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD rating to be determined.	

Electrical Characteristics (Note 4) LM221, LM321

Parameter	Conditions	LM221			LM321			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, 6.4k ≤ R_{SET} ≤ 70k			0.7			1.5	mV
Input Offset Current	T_A = 25°C,							
	R_{SET} = 70k			1			2	nA
	R_{SET} = 6.4k			10			20	nA
Input Bias Current	T_A = 25°C,							
	R_{SET} = 70k			10			18	nA
	R_{SET} = 6.4k			100			180	nA
Input Resistance	T_A = 25°C,							
	R_{SET} = 70k	4			2			MΩ
	R_{SET} = 6.4k	0.4			0.2			MΩ
Supply Current	T_A = 25°C, R_{SET} = 70k			1.5			2.2	mA
Input Offset Voltage	6.4k ≤ R_{SET} ≤ 70k			1.0			2.5	mV
Input Bias Current	R_{SET} = 70k			30			28	nA
	R_{SET} = 6.4k			300			280	nA
Input Offset Current	R_{SET} = 70k			3			4	nA
	R_{SET} = 6.4k			30			40	nA
Input Offset Current Drift	R_{SET} = 70k		3			3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	R_S ≤ 200Ω, 6.4k ≤ R_{SET} ≤ 70k Offset Voltage Nulled			1			1	μV/°C
Long Term Stability			5			5		μV/yr
Supply Current				2.5			3.5	mA
Input Voltage Range	V_S = ±15V, (Note 5)							
	R_{SET} = 70k	±13			±13			V
	R_{SET} = 6.4k	+7, −13			+7, −13			V
Common-Mode Rejection Ratio	R_{SET} = 70k	120			114			dB
	R_{SET} = 6.4k	114			114			dB
Supply Voltage Rejection Ratio	R_{SET} = 70k	120			114			dB
	R_{SET} = 6.4k	114			114			dB
Voltage Gain	T_A = 25°C, R_{SET} = 70k,							
	R_L > 3 MΩ	16			12			V/V
Noise	R_{SET} = 70k, R_{SOURCE} = 0		8			8		nV/√Hz

Note 1: The maximum junction temperature of the LM221 is 100°C. The maximum junction temperature of the LM321 is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

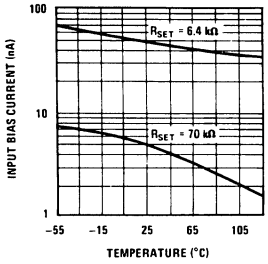
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for ±5 ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C, unless otherwise specified. With the LM221, however all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, and for the LM321 the specifications apply over a 0°C to +70°C temperature range.

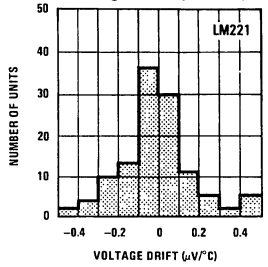
Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Typical Performance Characteristics

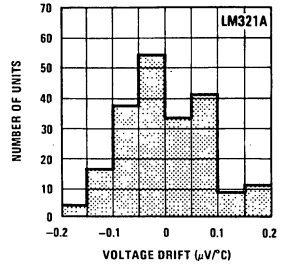
Input Bias Current



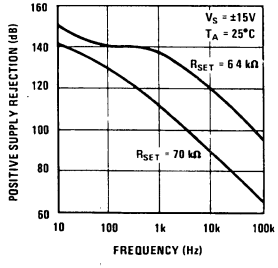
Distribution of Offset Voltage Drift (Nulled)



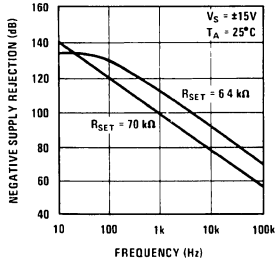
Distribution of Offset Voltage Drift (Nulled)



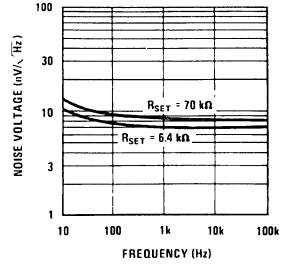
Positive Power Supply Rejection



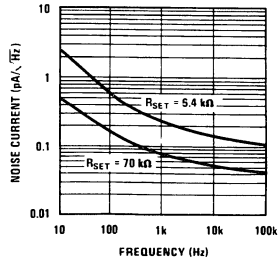
Negative Power Supply Rejection



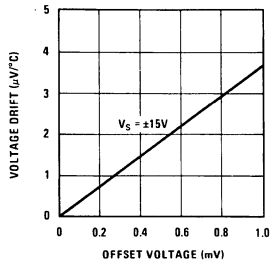
Input Noise Voltage



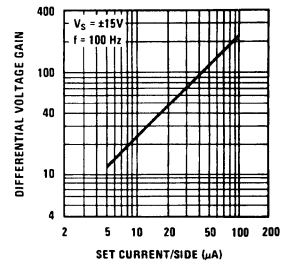
Input Noise Current



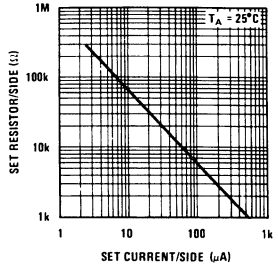
Voltage Drift



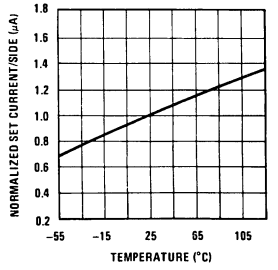
Differential Voltage Gain



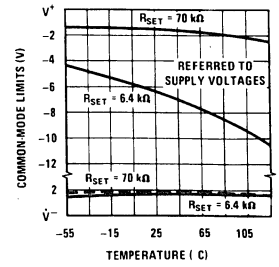
Set Resistor and Set Current



Set Current



Common-Mode Limits



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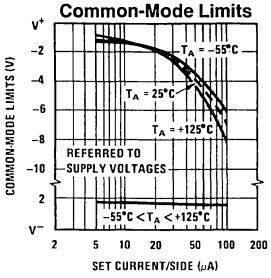
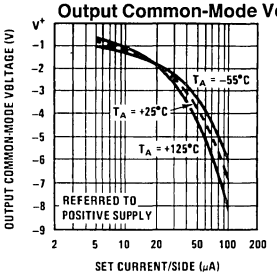
Typical Performance Characteristics (Continued)

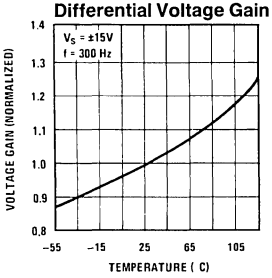
Common-Mode Limits



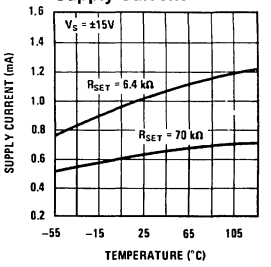
Output Common-Mode Voltage



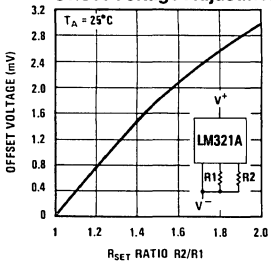
Differential Voltage Gain



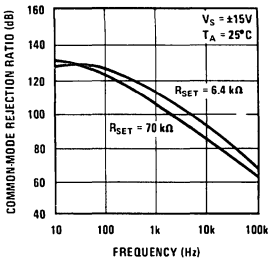
Supply Current



Offset Voltage Adjustment



Common-Mode Rejection Ratio



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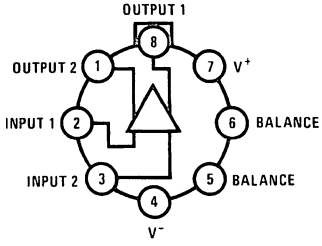
Connection Diagram

Metal Can Package



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Top View

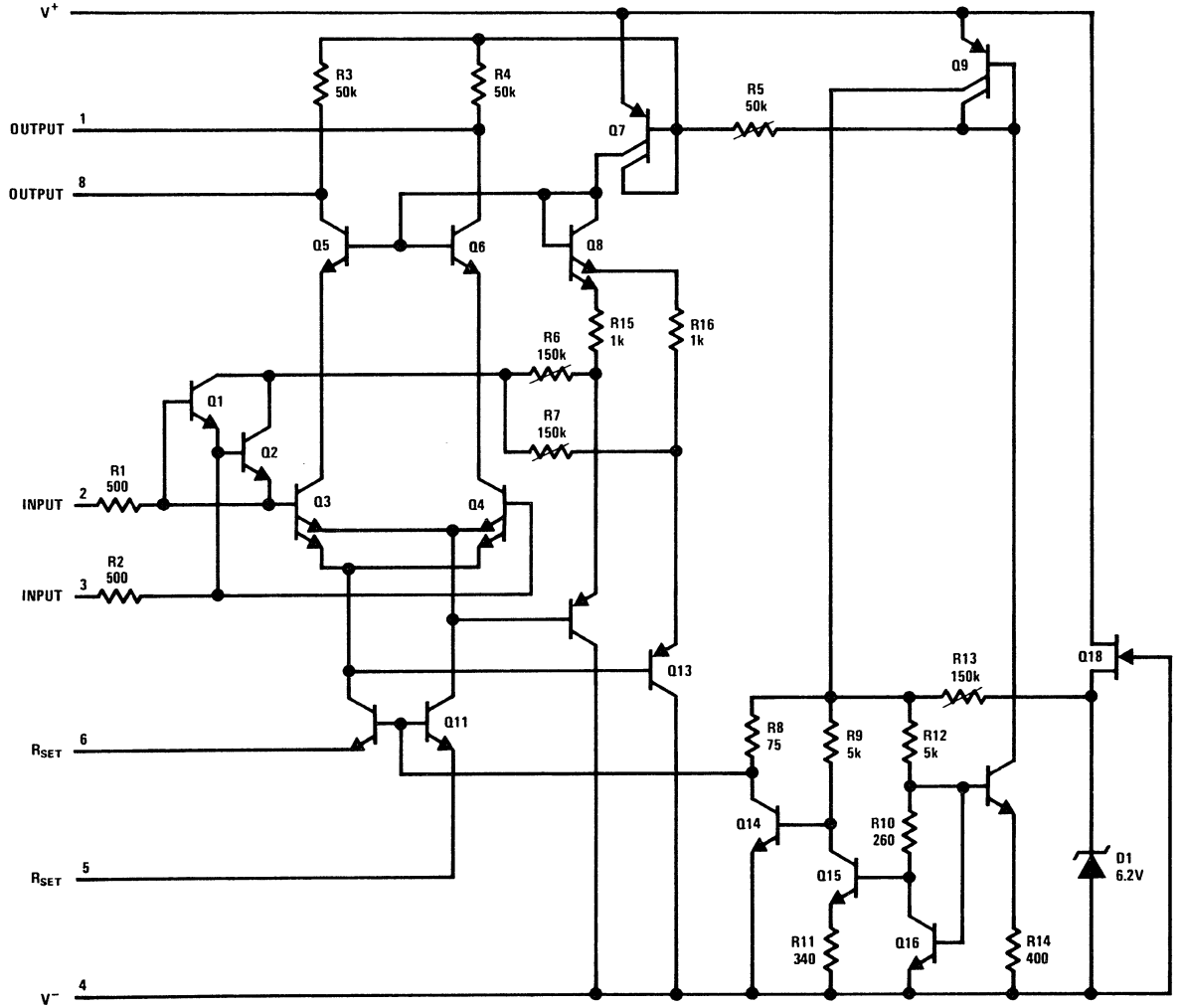
Note: Pin 4 connected to case.

Order Number LM221H, LM321H or LM321AH
See NS Package Number H08C

Note: Outputs are inverting from the input of the same number.

6

Schematic Diagram



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Frequency Compensation

UNIVERSAL COMPENSATION

The additional gain of the LM321 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM321 is less than the gain of the LM321 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM321 is high. When high closed loop gains are used—for example A_V = 1000—and only an addition gain of 200 is inserted by the LM321, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. *Figure 1* shows the basic configuration of frequency stabilizing network. In operation the output of the LM321 is rendered single ended by a 0.01 μF bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

$$C = \frac{4}{10^6 A_{CL} R_{SET}}$$

ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capscitor is:

$$C = \frac{8}{10^6 A_{CL} R_{SET}}$$

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

TABLE I

Closed Loop Gain	Current Set Resistor				
	120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
A_V = 1	68	130	270	680	1300
A_V = 5	15	27	56	130	270
A_V = 10	10	15	27	68	130
A_V = 50	1	3	5	15	27
A_V = 100	–	1	3	5	10
A_V = 500	–	–	1	1	3
A_V = 1000	–	–	–	–	–

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

DESIGN EQUATIONS FOR THE LM321 SERIES

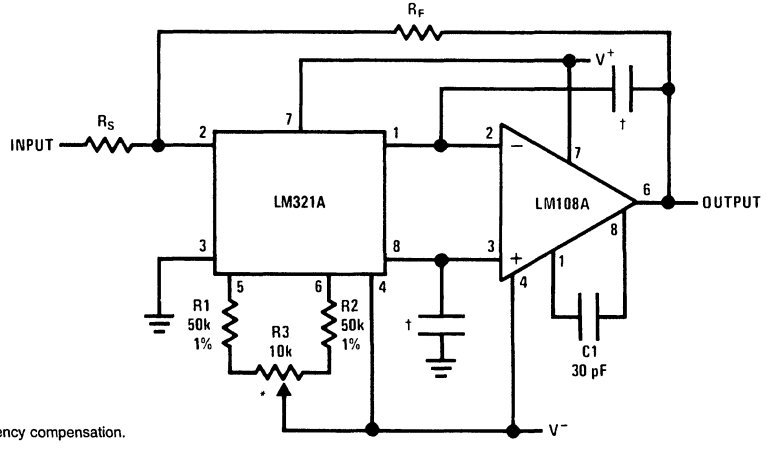
$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{SET}}$$

Null Pot Value should be 10% of R_{SET}

$$\text{Operating Current} \approx \frac{2 \times 0.65V}{R_{SET}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65V \times 50k}{R_{SET}}\right]$$

Typical Applications



*Offset adjust.

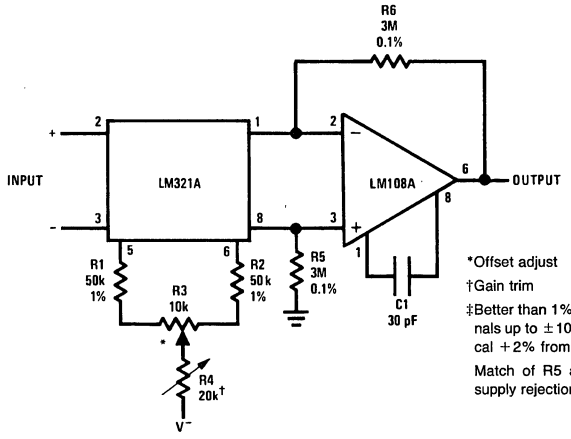
†See table for frequency compensation.

TL/H/7769–2

FIGURE 1. Low Drift Op Amp Using the LM321A as a Preamp

Typical Applications (Continued)

Gain of 1000 Instrumentation Amplifier‡



*Offset adjust

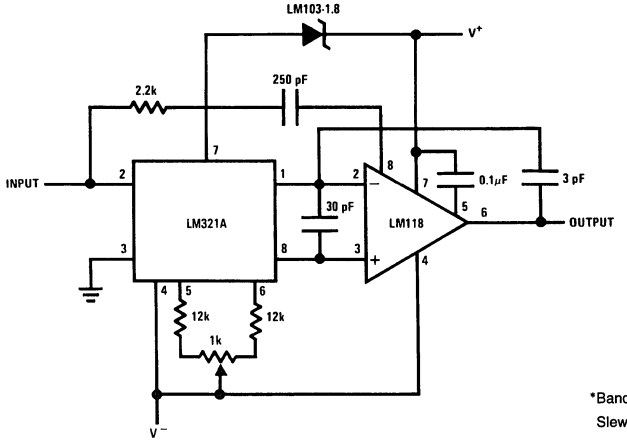
†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical +2% from −55 to +125°C.

Match of R5 and R6 effect power supply rejection

TL/H/7769–3

High Speed* Inverting Amplifier with Low Drift

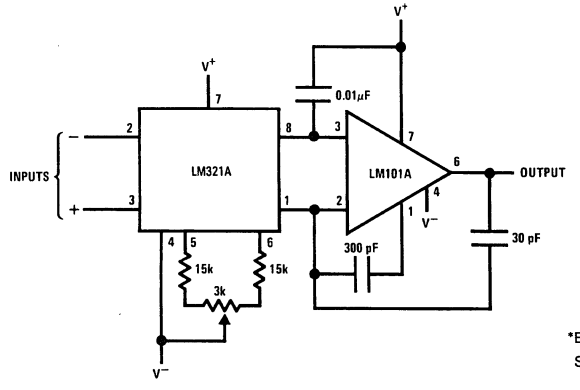


*Bandwidth = 10 MHz

Slew Rate = 40 V/μs

TL/H/7769–4

Medium Speed* General Purpose Amplifier



*Bandwidth = 3.5 MHz

Slew Rate = 1.1 V/μs

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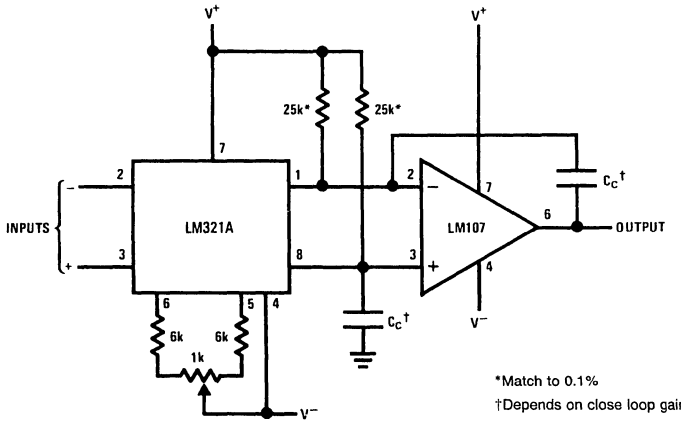
Typical Applications (Continued)

Increased Common-Mode Range at High Operating Currents



*Match to 0.1%

†Depends on close loop gain

TL/H/7769–6

National Semiconductor

LM363 Precision Instrumentation Amplifier

General Description

The LM363 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1000. High precision is attained by on-chip trimming of offset voltage and gain. A super-beta bipolar input stage gives very low input bias current and voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains. The LM363 operates with supply voltages from ±5V to ±18V with only 1.5 mA current drain.

The LM363's low voltage noise, low offset voltage and offset voltage drift make it ideal for amplifying low-level, low-impedance transducers. At the same time, its low bias current and high input impedance (both common-mode and differential) provide excellent performance at high impedance levels. These features, along with its ultra-high common-mode rejection, allow the LM363 to be used in the most demanding instrumentation amplifier applications, replacing expensive hybrid, module or multi-chip designs. Because the LM363 is internally trimmed, precision external resistors and their associated errors are eliminated.

The 16-pin dual-in-line package provides pin-strappable gains of 10, 100 or 1000. Its twin differential shield drivers eliminate bandwidth loss due to cable capacitance. Compensation pins allow overcompensation to reduce bandwidth and output noise, or to provide greater stability with capacitive loads. Separate output force, sense and reference pins permit gains between 10 and 10,000 to be programmed using external resistors.

On the 8-pin HO8 package, gain is internally set at 10, 100 or 500 but may be increased with external resistors. The shield driver and offset adjust pins are omitted on the 8-pin versions.

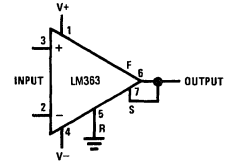
The LM363 is rated for 0°C to 70°C.

Features

- Offset and gain pretrimmed
- 12 nV/√Hz input noise (G = 500/1000)
- 130 dB CMRR typical (G = 500/1000)
- 2 nA bias current typical
- No external parts required
- Dual shield drivers
- Can be used as a high performance op amp
- Low supply current (1.5 mA typ)

Typical Connections

8-Pin Package



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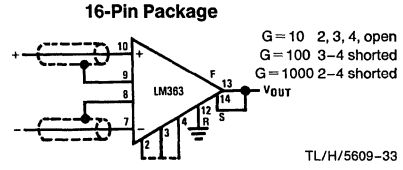
16-Pin Package



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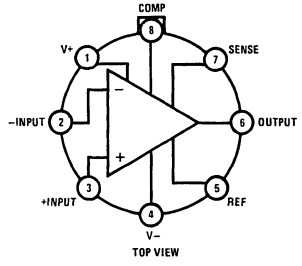
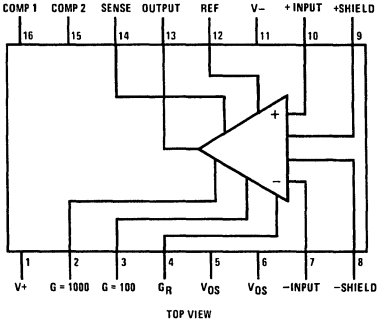
Connection Diagrams

Metal Can Package



Order Number LM363H-10, LM363H-100 or LM363H-500
See NS Package Number H08C

16-Pin Dual-In-Line Package



TL/H/5609–2

Order Number 363D
See NS Package Number D16C

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±10V
Input Current	±20 mA
Input Voltage	Equal to Supply Voltage
Reference and Sense Voltage	±25V
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

LM363 Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	LM363			Units
		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
FIXED GAIN (8-PIN)					
Input Offset Voltage	G=500	30	100	**300**	μV
	G=100	50	200	**600**	μV
	G=10	0.5	2.0	**5**	mV
Input Offset Voltage Drift	G=500	1		**4**	μV/°C
	G=100	2		**8**	μV/°C
	G=10	20		**75**	μV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G=500	0.1	0.5	**0.8**	%
	G=100	0.05	0.5	**0.7**	%
	G=10	0.05	0.5	**0.6**	%
PROGRAMMABLE GAIN (16-PIN)					
Input Offset Voltage	G=1000	50	200	**400**	μV
	G=100	100	400	**800**	μV
	G=10	1	3	**7**	mV
Input Offset Voltage Drift	G=1000	1		**5**	μV/°C
	G=100	2		**10**	μV/°C
	G=10	10		**100**	μV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G=1000	2.0	2.5	**3.0**	%
	G=100	0.1	0.5	**0.7**	%
	G=10	0.6	1.5	**1.7**	%
FIXED GAIN AND PROGRAMMABLE					
Gain Temperature Coefficient	G=1000	40			ppm/°C
	G=500	20			ppm/°C
	G=100, 10	10			ppm/°C
Gain Non-Linearity (±10V Swing, 2 kΩ Load)	G=10, 100	0.01	0.03	**0.04**	%
	G=500, 1000	0.01	0.05	**0.06**	%

LM363 Electrical Characteristics (Continued) (Notes 1 and 2)

Parameter	Conditions	LM363			Units
		Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Common-Mode Rejection Ratio ($-11V \le V_{CM} \le 13V$)	G = 1000, 500	130	114	**104**	dB
	G = 100	120	94	**84**	dB
	G = 10	105	90	**80**	dB
Positive Supply Rejection Ratio (5V to 15V)	G = 1000, 500	130	110	**100**	dB
	G = 100	120	100	**95**	dB
	G = 10	100	85	**78**	dB
Negative Supply Rejection Ratio (−5V to −15V)	G = 1000, 500	120	100	**90**	dB
	G = 100	106	85	**75**	dB
	G = 10	86	70	**60**	dB
Input Bias Current		2	10	**20**	nA
Input Offset Current		1	3	**5**	nA
Common-Mode Input Resistance		100	8		GΩ
Differential Mode Input Resistance	G = 1000, 500	0.2			GΩ
	G = 100	2			GΩ
	G = 10	20			GΩ
Input Offset Current Change	$-11V \le V_{CM} \le 13V$	20	100	**300**	pa/V
Reference and Sense Resistance		50			kΩ
	Min		30	**27**	kΩ
	Max		80	**83**	kΩ
Open Loop Gain	G_{CL} = 1000, 500	10	1		V/μV
Supply Current	Positive	1.2	2.4	**3.0**	mA
				2.8	mA
	Negative	1.6	2.8	**3.4**	mA

Note 1: These conditions apply unless otherwise noted; $V^+ = V^- = 15V$, $V_{CM} = 0V$, $R_L = 2\ k\Omega$, reference pin grounded, sense pin connected to output and $T_j = 25°C$.

Note 2: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range is 0°C to 70°C for the LM363.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% tested. These limits are not used in determining outgoing quality levels.

Note 5: Maximum rated junction temperature is 100°C for the LM363. Thermal resistance, junction to ambient, is 150°C/W for the TO-99(H) package and 100°C/W for the ceramic DIP (D).

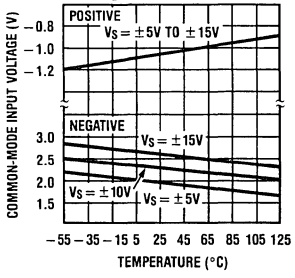
Typical Performance Characteristics $T_A = 25°C$

Parameter	Fixed Gain and Programmable			Units
	1000/500	100	10	
Input Voltage Noise, rms, 1 kHz	12	18	90	nV/√Hz
Input Voltage Noise (Note 6)	0.4	1.5	10	μVp-p
Input Current Noise, rms, 1 kHz	0.2	0.2	0.2	pA/√Hz
Input Current Noise (Note 6)	40	40	40	pAp-p
Bandwidth	30	100	200	kHz
Slew Rate	1	0.36	0.24	V/μS
Settling Time, 0.1% of 10V	70	25	20	μS
Offset Voltage Warm-Up Drift (Note 7)	5	15	50	μV
Offset Voltage Stability (Note 8)	5	10	100	μV
Gain Stability (Note 8)	0.01	0.005	0.05	%

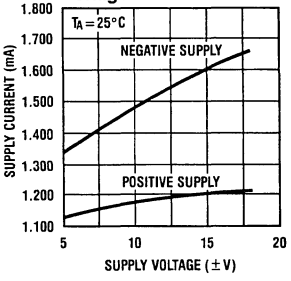
Note 6: Measured for 100 seconds in a 0.01 Hz to 10 Hz bandwidth.

Note 7: Measured for 5 minutes in still air, $V^+ = V^- = -15V$. Warm-up drift is proportionally reduced at lower supply voltages.

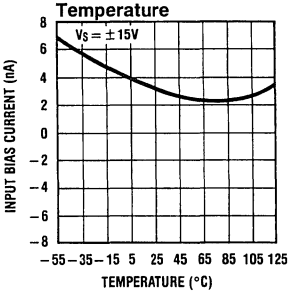
Common-Mode Input Voltage Limit



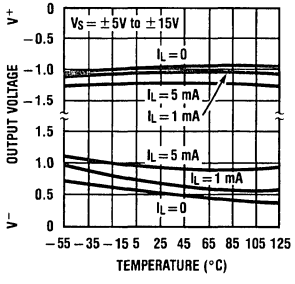
Supply Current vs Supply Voltage



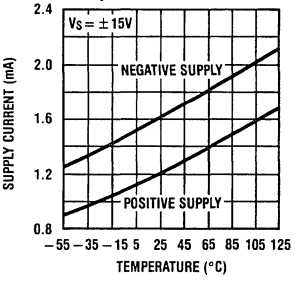
Input Bias Current vs Temperature



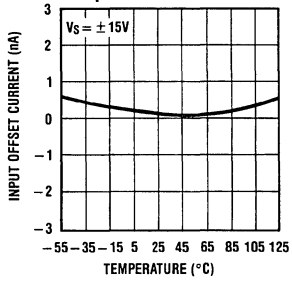
Output Swing Referred to Supplies



Supply Current vs Temperature



Input Offset Current vs Temperature



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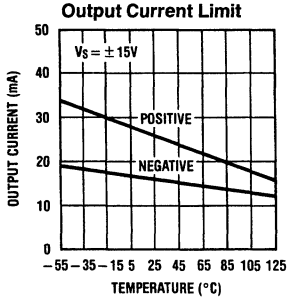
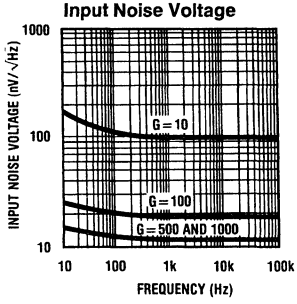
Typical Performance Characteristics (Continued)

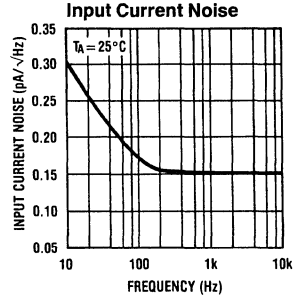
Output Current Limit



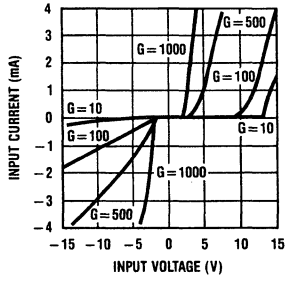
Input Noise Voltage



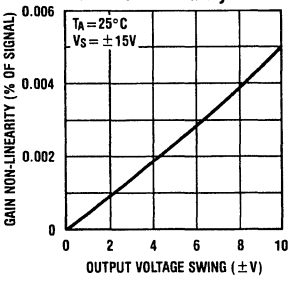
Input Current Noise



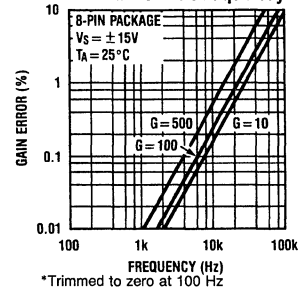
Input Current vs Voltage Overdrive



Gain Non-Linearity

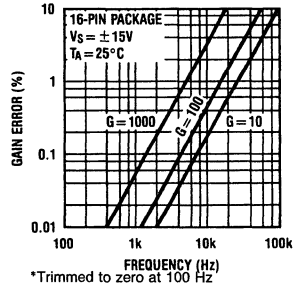


Gain Error vs Frequency*



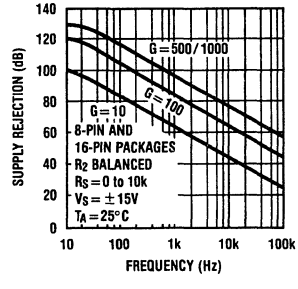
*Trimmed to zero at 100 Hz

Gain Error vs Frequency*

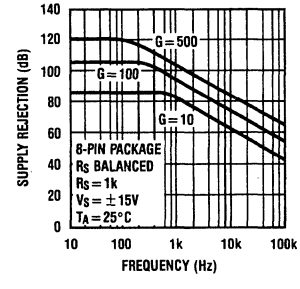


*Trimmed to zero at 100 Hz

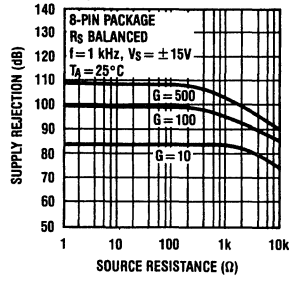
Positive Power Supply Rejection



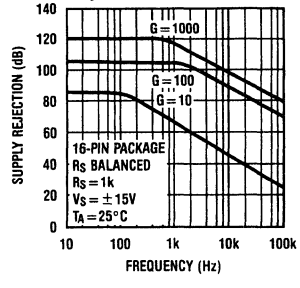
Negative Power Supply Rejection



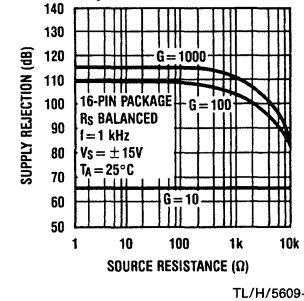
Negative Power Supply Rejection



Negative Power Supply Rejection



Negative Power Supply Rejection



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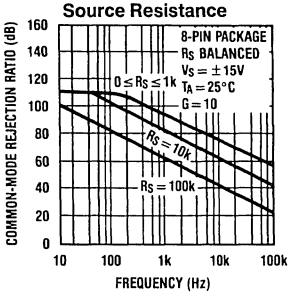
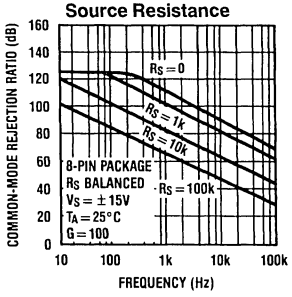
Typical Performance Characteristics (Continued)

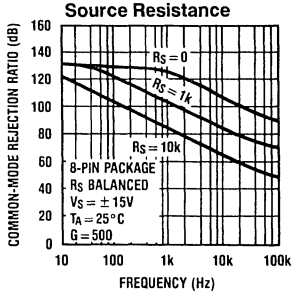
CMRR with Balanced Source Resistance



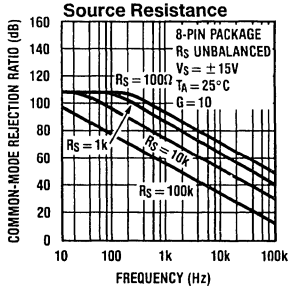
CMRR with Balanced Source Resistance



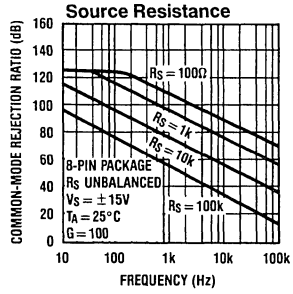
CMRR with Balanced Source Resistance



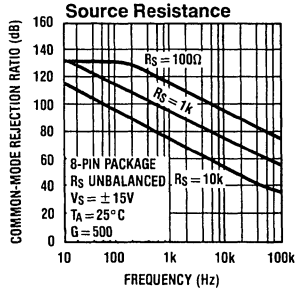
CMRR with Unbalanced Source Resistance



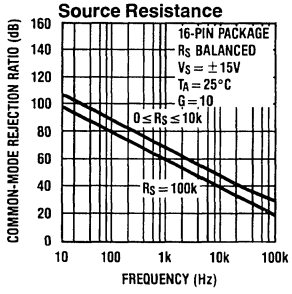
CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



CMRR with Balanced Source Resistance



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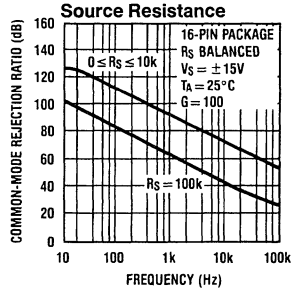
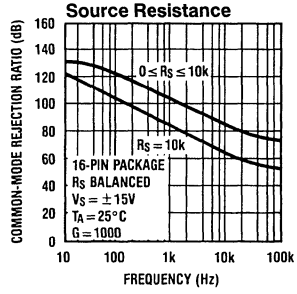
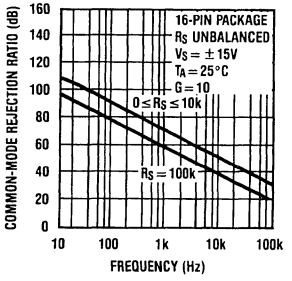


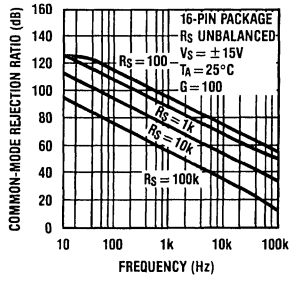
CMRR with Balanced Source Resistance



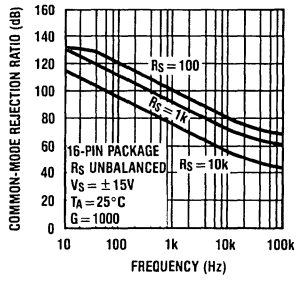
CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



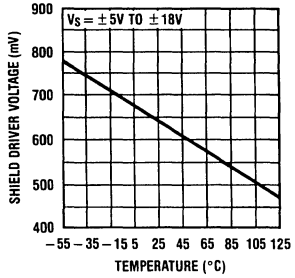
CMRR with Unbalanced Source Resistance



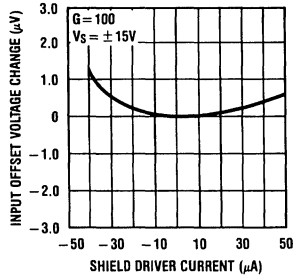
TL/H/5609–5

Typical Performance Characteristics

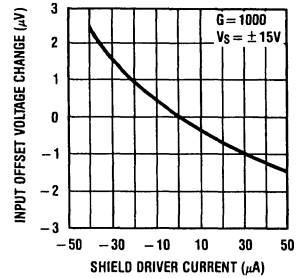
Shield Driver Bias Voltage*



Shield Driver Loading Error



Shield Driver Loading Error



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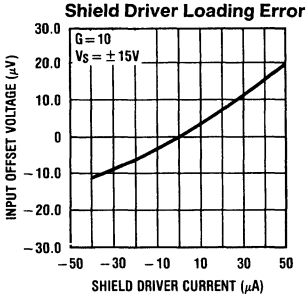
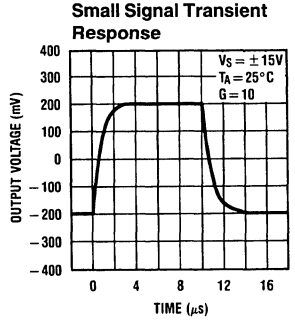


Small Signal Transient Response



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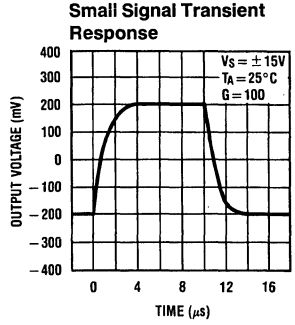

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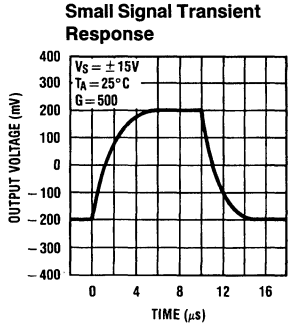

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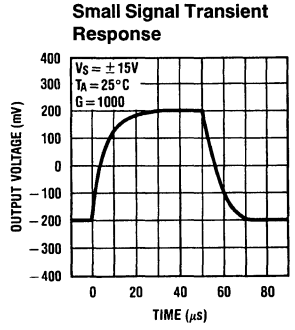

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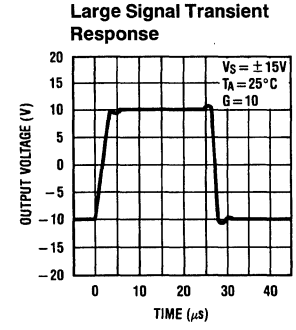
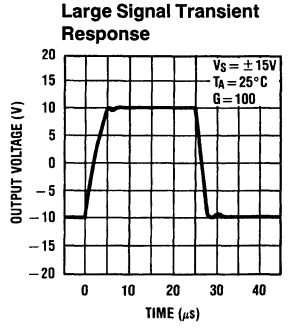
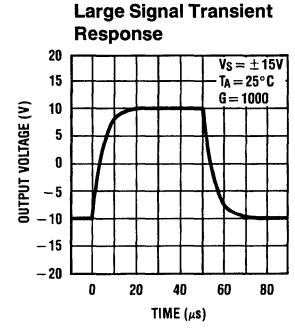


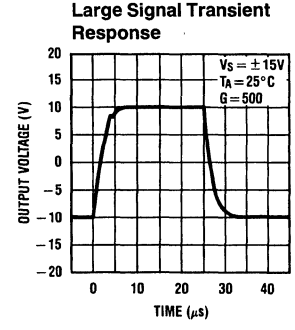
Large Signal Transient Response



Large Signal Transient Response



Large Signal Transient Response



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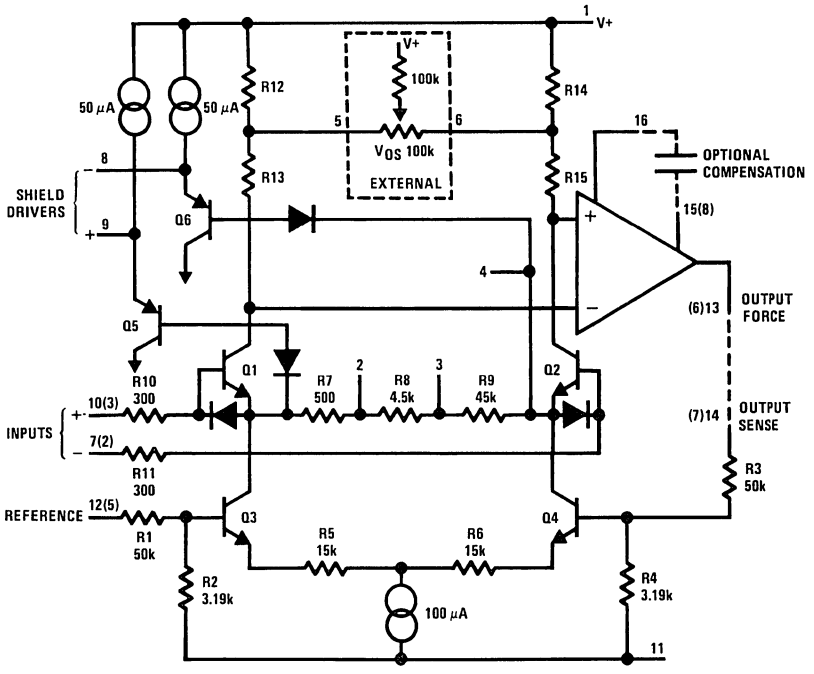
Simplified Schematic (pin numbers in parentheses are for 8-pin package)



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Theory of Operation

Referring to the Simplified Schematic, it can be seen that the input voltage is applied across the bases of Q1 and Q2 and appears between their emitters. If R_{E1-2} is the resistance across these emitters, a differential current equal to V_{IN}/R_{E1-2} flows from Q1's emitter to Q2's. The second stage amplifier shown maintains Q1 and Q2 at equal collector currents by negative feedback to Q4. The emitter currents of Q3 and Q4 must therefore be unbalanced by an amount equal to the current flow across R_{E1-2}. Defining $R_{E3-4} = R5 + R6$, the differential voltage across the emitters of Q4 to Q3 is equal to

$$\frac{V_{IN}}{R_{E\,1-2}} \times R_{E3-4}.$$

This voltage divided by the attenuation factor

$$\frac{R4}{R3+R4} = \frac{R2}{R1+R2}$$

is equal to the output-to-reference voltage. Hence, the overall gain is given by

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{R3+R4}{R4} \times \frac{R_{E3-4}}{R_{E1-2}}.$$

Application Hints

The LM363 was designed to be as simple to use as possible, but several general precautions must be taken. The differential inputs are directly coupled and need a return path to power supply common. Worst-case bias currents are only 10 nA for the LM363, so the return impedance can be as high as 100 MΩ. Ground drops between signal return and IC supply common should not be ignored. While the LM363 has excellent common-mode rejection, signals must remain within the proper common-mode range for this specification to apply. Operating common-mode range is guaranteed from −11V to +13V with ±15V supplies.

The high-gain (500 or 1000) versions have large gain-bandwidth products (15 MHz or 30 MHz) so board layout is fairly critical. The differential input leads should be kept away from output force and sense leads, especially at high impedances. Only 1 pF from output to positive input at 100 kΩ source impedance can cause oscillations. The gain adjust leads on the 16-pin package should be treated as inputs and kept away from the output wiring.

POWER SUPPLY

The LM363 may be powered from split supplies from ±5V to ±18V (or single-ended supplies from 10V to 36V). Positive supply current is typically 1.2 mA independent of supply voltage. The negative supply current is higher than the positive by the current drawn through the voltage dividers for the reference and sense inputs (typ 600 μA total). The LM363's excellent PSRR often makes regulated supplies unnecessary. Actually, supply voltage can be as low as 7V total but PSRR is severely degraded, so that well-regulated supplies are recommended below 10V total. Split supplies need not be balanced; output swing and input common-mode range will simply not be symmetrical with unbalanced supplies. For example, at +12V and −5V supplies, input common-mode range is typically +10.5V to −2V and output swing is +11V to −4V.

When using ultra-low offset versions, best results are obtained at ±15V supplies. For example, the LM363-500's offset voltage is guaranteed within 100 μV at ±15V at 25°C. Running at ±5V results in a worst-case negative PSRR error of 10V (−15V to −5V) multiplied by $3.2X10^{-6}$ (110 dB) or 32 μV, increasing the worst-case offset. Positive PSRR results in another 10 μV worst-case change.

INPUTS

The LM363 input circuitry is depicted in the Simplified Schematic. The input stage is run relatively rich (50 μA) for low voltage noise and wide bandwidth; super-beta transistors and bias-current cancellation (not shown) keep bias currents low. Due to the bias-current cancellation circuitry, bias current may be either polarity at either input. While input current noise is high relative to bias current, it is not significant until source resistance approaches 100 kΩ.

Input common-mode range is typically from 3V above V^- to 1.5V below V^+, so that a large potential drop between the input signal and output reference can be accommodated. However, a return path for the input bias current must be provided; the differential input stage is not isolated from the supplies. Differential input swing in the linear region is equal to output swing divided by gain, and typically ranges from 1.3V at G = 10 to 13 mV at G = 1000.

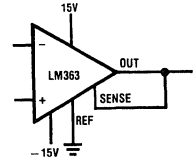
Clamp diodes are provided to prevent zener breakdown and resulting degradation of the input transistors. At large input overdrives these diodes conduct, greatly increasing input currents. This behavior is illustrated in the I_{IN} VS V_{IN} plot in the Typical Performance Characteristics. (The graph is not symmetrical because at large input currents a portion of the current into the device flows out the V^- terminal.)

The input protection resistors allow a full 10V differential input voltage without degradation even at G = 1000. At input voltages more than one diode drop below V^- or two diode drops above V^+ input, current increases rapidly. Diode clamps to the supplies, or external resistors to limit current to 20 mA, will prevent damage to the device.

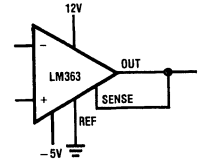
REFERENCE AND SENSE INPUTS

The equivalent circuit is shown in the schematic diagram. Limitations for correct operation are as follows. Maximum *differential* swing between reference and sense pins is typically ±15V (±10V guaranteed). If this limit is exceeded, the sense pin no longer controls the output, which pegs high or low. The *negative* common-mode limit is 1.5V below V^-. (This is permissible because R2 and R4 are returned to a node biased higher than V^-.) If large *positive* voltages are applied to the reference and sense pins, the common-mode range of the signal inputs begins to suffer as the drop across R13 and R16 increases. For example, at ±15V supplies, $V_{REF} = V_{SENSE} = 0V$, signal input range is typically −12V to + 13.5V. at $V_{REF} = V_{SENSE} = 15V$, signal input range drops to −11V to +13.5V. The reference and sense pin can be as much as 10V above V^+ as long as a restricted signal common-mode range (−10V min) can be tolerated.

For maximum bipolar output swing at ± 15V supplies, the reference pin should be returned to a voltage close to ground. At lower supply voltages, the reference pin need not be halfway between the supplies for maximum output swing. For example, at V^+ = + 12V and V^- = −5V, grounding the reference pin still allows a +11V to −4V swing. For single-supply systems, the reference pin can be tied to either supply if a single output polarity is all that is required. For a bipolar input and output, create a low impedance reference with an op amp and voltage divider or a regulator (e.g., LM336, LM385, LM317L). This forms the reference for all succeeding signal-processing stages. (Don't connect the reference terminal directly to a voltage divider; this degrades gain error.) See *Figure 1.*



a. Usual configuration maximizes bipolar output swing.



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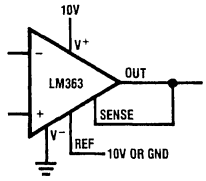
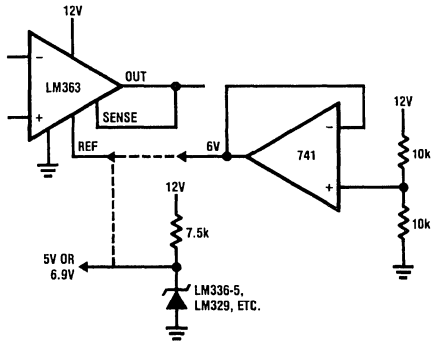
b. Unequal supplies, output ground referred. Full output swing preserved referred to supplies.

FIGURE 1. Reference Connections

Application Hints (Continued)



c. Single Supply, Unipolar Output



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d. Single Supply, Bipolar Output

FIGURE 1. Reference Connections (Continued)

OUTPUTS

The LM363's output can typically swing within 1V of the supplies at light loads. While specified to drive a 2 kΩ load to ±10V, current limit is typically 15 mA at room temperature. The output can stably drive capacitive loads up to 400 pF. For higher load capacitance, the amplifier may be overcompensated. The output may be continuously shorted to ground without damaging the device.

OFFSET VOLTAGE

The LM363's offset voltage is internally trimmed to a very low value. Note that data sheet values are given at $T_j = 25°C$, $V_{CM} = 0V$ and $V^+ = V^- = 15V$. For other conditions, warm-up drift, temperature drift, common-mode rejection and power supply rejection must be taken into account. Warm-up drift, due to chip and package thermal gradients, is an effect separate from temperature drift. Typical warm-up drift is tabulated in the Electrical Characteristics; settling time is approximately 5 minutes in still air. At load currents up to 5 mA, thermal feedback effects are negligible ($\Delta V_{OS} \leq 2\mu V$ at G = 1000).

Care must be taken in measuring the extremely low offset voltages of the high gain amplifiers. Input leads must be held isothermal to eliminate thermocouple effects. Oscillations, due to either heavy capacitive loading or stray capacitance from input to output, can cause erroneous readings. In either case, overcompensation will help. High frequency noise fed into the inputs may be rectified internally, and produce an offset shift. A simple low-pass RC filter will usually cure this problem (*Figure 2*). Use film type resistors for their low thermal EMF. In highly noisy environments, LC filters can be substituted for increased RF attenuation.

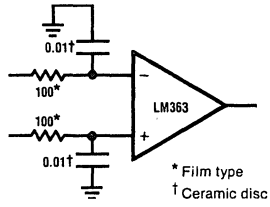

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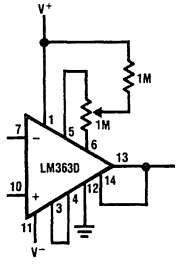
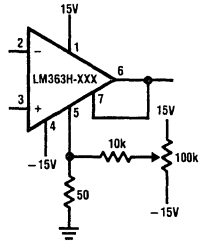
FIGURE 2. Low Pass Filter Prevents RF Rectification

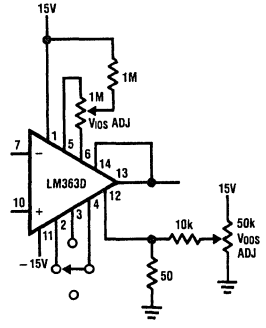
Instrumentation amplifiers have both an input offset voltage (V_{IOS}) and an output offset voltage (V_{OOS}). The total input-referred offset voltage (V_{OSRTI}) is related to the instrumentation amplifier gain (G) as follows: $V_{OSRTI} = V_{IOS} + V_{OOS}/G$. The offset voltage given in the LM363 specifications is the total input-referred offset. As long as only one gain is used, offset voltage can be nulled at either input or output as shown in *Figures 3a* and *3b*. When the 16-pin device is used at multiple gain settings, both V_{IOS} and V_{OOS} should be nulled to get minimum offset at all gains, as shown in *Figure 3c*. The correct procedure is to trim V_{OOS} for zero output at G = 10, then trim V_{IOS} at G = 1000.



a. Input Offset Adj. for 16-Pin Package



b. Output Offset Adj. for 8-Pin Package



c. Input and Output Offset Adjustment for 16-Pin Package

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FIGURE 3. Offset Voltage Trimming

Application Hints (Continued)

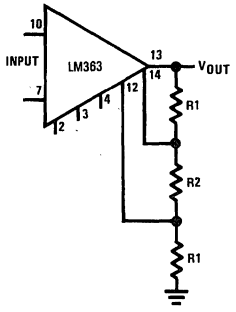
Because the LM363's offset voltage is so low to begin with, offset nulling has a negligible effect on offset temperature drift. For example, zeroing a 100 μV offset, assuming external resistor TC of 200 ppm/°C and worst-case internal resistor TC, results in an additional drift component of 0.08 μV/°C. For this reason, drift specifications are guaranteed, with or without external offset nulling.

GAIN ADJUSTMENT

Gain may be increased by adding an external voltage divider between output force and sense and reference; the preferred connection is shown in *Figure 4*. Since both the sense and reference pins look like 50 kΩ ($\pm$20 kΩ) to V$^-$, impedances presented to both pins must be equal to avoid offset error. For example, a 100Ω imbalance can create a worst-case output offset of 50 mV, creating an input-referred error of 5 mV at G = 10 or 50 μV at G = 1000.

Increasing gain this way increases output offset error. An LM363H-100 may have an output offset of 5 mV, resulting in input referred offset component of 50 μV. Raising the gain to 200 yields a 10 mV error at the output and changes input referred error by an additional 50 μV.

External resistors connected to the reference and sense pins can only *increase* the gain. If ultra-low output impedance is not critical, the technique in *Figure 5* can be used to trim the gain to nominal value. Alternatively, the V_{OS} adjustment terminals on the 16-pin package may be used to trim the gain (*Figure 10b*).



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R1 and R2 should be as low as possible to avoid errors due to 50 kΩ input impedance of reference and sense pins. Total resistance (R2 + 2R1) should be above 4 kΩ, however, to prevent excessive load on the LM363 output. The exact formula for calculating gain (G) is:

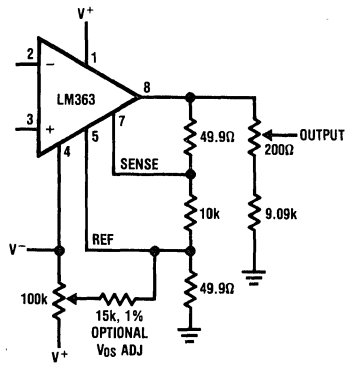
$$G = G_O\left(1 + \frac{2R1}{R2} + \frac{R1}{50k}\right)$$

G_O = preset gain

The last term may be ignored in applications where gain accuracy is not critical. The table below gives suggested values for R1 and R2 along with the calculated error due to "closest value" standard 1% resistors. Total gain error tolerance includes contributions from LM363 G_O error and resistor tolerance ($\pm$1%) and works out to approximately 2.5% in every case.

Gain Increase	1.5	2	2.5	3	4	5	6	7	8	9	10
R1	1.21k	1.21k	2k	2k	1.78k	2k	2.49k	2.94k	3.48k	3.92k	4.42k
R2	5k	2.49k	2.74k	2.05k	1.21k	1k	1k	1k	1k	1k	1k
Error (typ)	+0.6%	−0.2%	0	−0.3%	−0.6%	+0.8%	+0.5%	−0.9%	+0.4%	−0.9%	−0.7%

FIGURE 4. Increasing Gain



TL/H/5609–13

FIGURE 5. Adjusting Gain (8-Pin Package)

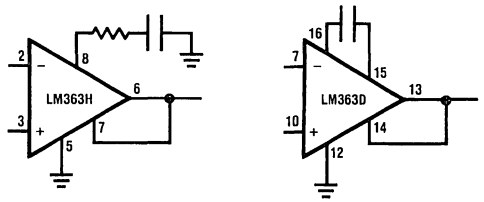
Application Hints (Continued)

COMPENSATION AND OUTPUT CLAMPING

The LM363 is internally compensated for unity feedback from output to sense. Increasing gain with external dividers will decrease the bandwidth and increase stability margin. Without external compensation, the amplifier can stably drive capacitive loads up to 400 pF. When used as an op amp (sense and reference pins grounded, feedback to inverting input), the LM363 is stable for gains of 100 or more. For greater stability, the device may be over-compensated as in *Figure 6.* Tables I and II depict suggested compensation components along with the resulting changes in large and small signal bandwidth for the 8-pin and 16-pin packages, respectively.

Note that the RC network from pin 8 of the 8-pin device to ground has a large effect on power bandwidth, especially at low gains. The Miller capacitance utilized for the 16-pin device permits higher slew rate and larger load capacitance for the same bandwidth, and is preferred when bandwidth must be greatly reduced (e.g., to reduce output noise).

Heavy Miller overcompensation on the 16-pin package can degrade AC PSRR. A large capacitor between pins 15 and 16 couples transients on the positive supply to the output buffer. Since the amplifier bandwidth is severely rolled off it cannot keep the output at the correct state at moderate frequencies. Hence, for good PSRR, either keep the Miller capacitance under 1000 pF or use the pin 15-to-ground compensation.



a. 8-Pin Package b. 16-Pin Package

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FIGURE 6. Overcompensation

TABLE I. Overcompensation on 8-Pin Package

Gain	Compensation Network (Pin 8 to Ground)†	Small Signal 3 dB Bandwidth (kHz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
500	—	125	100k	400
	100 pF, 15k	95	15k	600
	1000 pF, 5k	45	1.8k	800
	0.01 μF,500Ω	10	200	1000*
	0.1 μF	1	20	1000*
100	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	80	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*
10	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	90	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*

*Also stable for $C_L \geq 0.05\ \mu F$ †Pin 15 to ground on 16-pin package

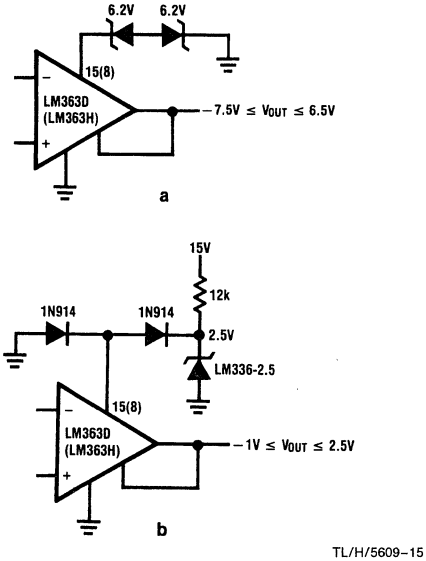
TABLE II. Overcompensation on 16-Pin Package

Gain	Compensation Capacitor (Pin 15 to 16)	Small Signal 3 dB Bandwidth (Hz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
1000	0	45k	45k	1000*
	10 pF	16k	16k	2000*
	100 pF	2.5k	2.5k	2500*
	1000 pF	250	250	3000*
	0.01 μF	25	25	3000*
100	0	140k	100k	900
	10 pF	50k	50k	1600
	100 pF	7.5k	7.5k	2000*
	1000 pF	750	750	2000*
	0.01 μF	75	75	2000*
10	0	180k	90k	600
	10 pF	60k	50k	1100
	100 pF	9k	9k	1600
	1000 pF	900	900	2000*
	0.01 μF	90	90	2000*

*Also stable for $C_L \geq 0.05\ \mu F$

Application Hints (Continued)

Because the LM363's output voltage is approximately one diode drop below the voltage at pin 15 (pin 8 for the 8-pin device), this point may be used to limit output swing as seen in *Figure 7a*. Current available from this pin is only 50 μA, so that zeners must have a sharp breakdown to clamp accurately. Alternatively, a diode tied to a voltage source could be used as in *Figure 7b*.



TL/H/5609–15

FIGURE 7. Output Clamp

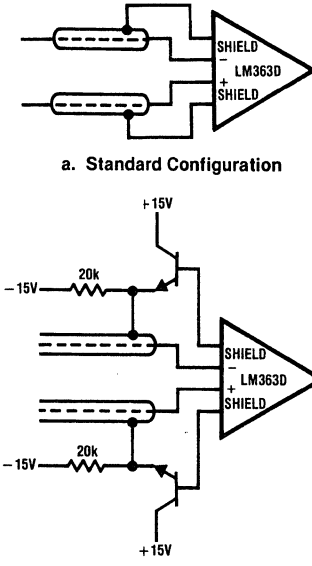
SHIELD DRIVERS

When differential signals are sent through long cables, three problems occur. First, noise, both common-mode and differential, is picked up. Second, signal bandwidth is reduced by the RC low-pass filter formed by the source impedance and the cable capacitance. Finally, when these RC time constants are not identical (unbalanced source impedance and/or unbalanced capacitance), AC common-mode rejection is degraded, amplifying both induced noise and "ground" noise. Either filtering at the amplifier inputs or slowing down the amplifier by overcompensating will indeed reduce the noise, but the price is slower response. The LM363's dual shield drivers can actually increase bandwidth while reducing noise.

The way this is done is by bootstrapping out shield capacitance. The shield drivers follow the input signal. Since both sides of the shield capacitance swing the same amount, it is effectively out of the circuit at frequencies of interest. Hence, the input signal is not rolled off and AC CMRR is not degraded (*Figure 8*). The LM363's shield drivers can handle capacitances (shield to center conductor) as high as 1000 pF with source resistances up to 100 kΩ.

For best results, identical shielded cables should be used for both signal inputs, although small mismatches in shield driver to ground capacitance (≤500 pF) do not cause problems. At certain low values of cable capacitance (50 pF–200 pF), high frequency oscillations can occur at high source resistance (≥ 10 kΩ). This is alleviated by adding 50 pF to ground at both shield driver outputs. Do not use only one shield driver for a single-ended signal as oscillations can result; shield driver to input capacitance must be roughly balanced (±30%). To further reduce noise pickup, the shielded signal lines may be enclosed together in a grounded shield. If a large amount of RF noise is the problem, the only sure cure is a filter capacitor at both inputs; otherwise the RFI may be internally rectified, producing an offset.

DC loading on the shield drivers should be minimized. The drivers can only source approximately 40 μA; above this value the input stage bias voltages change, degrading V_{OS} and CMRR. While the shield drivers can sink several mA, V_{OS} may degrade severely at loads above 100 μA (see Shield Driver Loading Error curve in Typical Performance Characteristics). Because the shield drivers are one diode drop above the input levels, unbalanced leakage paths from shield to input can produce an input offset at high source impedances. Buffering with emitter-followers (*Figure 8b*) reduces this leakage current by reducing the voltage differential and eliminates any loading on the amplifier.



TL/H/5609–16

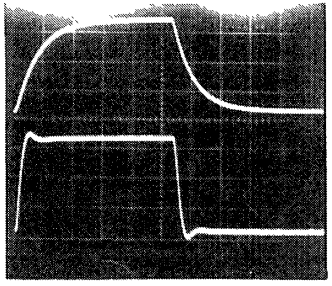
FIGURE 8. Driving Shielded Cables

MISCELLANEOUS TRIMMING

The V_{OS} adjust and shield driver pins available on the 16-pin package may be used to trim the other parameters besides offset voltage, as illustrated in *Figure 10*. The bias-current trim relies on the fact that the voltage on the shield driver and gain setting pins is one diode drop respectively above and below the input voltage. Input bias current can be held to within 100 pA over the entire common-mode range, and input offset current always stays under 30 pA. The CMRR trims use the shield driver pins to drive the V_{OS} adjust pins, thus maintaining the LM363's ultra-high input impedance.

Application Hints (Continued)

If power supply rejection is critical, frequently only the negative PSRR need be adjusted, since the positive PSRR is more tightly specified. Any or all of the trim schemes of *Figure 10* can be combined as desired. As long as the center tap of the 100k trimpot is returned to a voltage 200 mV below V^+, the trim schemes shown will not greatly affect V_{OS}. Both the gain and DC CMRR trims can degrade positive PSRR; the positive PSRR can then be nulled out if desired. The correct order of trimming from first to last is bias current, gain, CMRR, negative PSRR, positive PSRR and V_{OS}.



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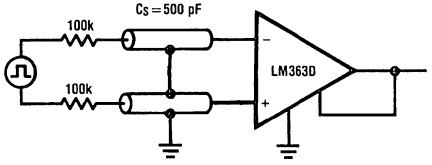
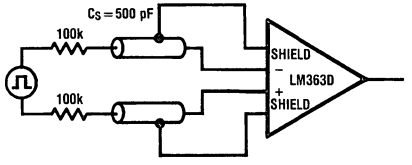
Top Trace: Cable Shield Grounded

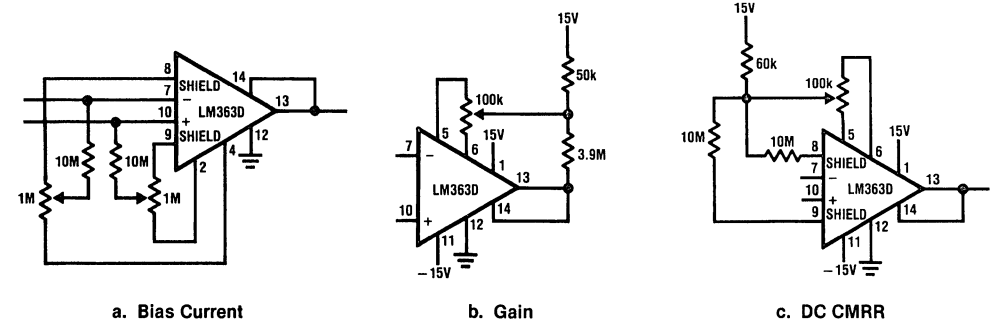


Bottom Trace: Cable Shield Bootstrapped

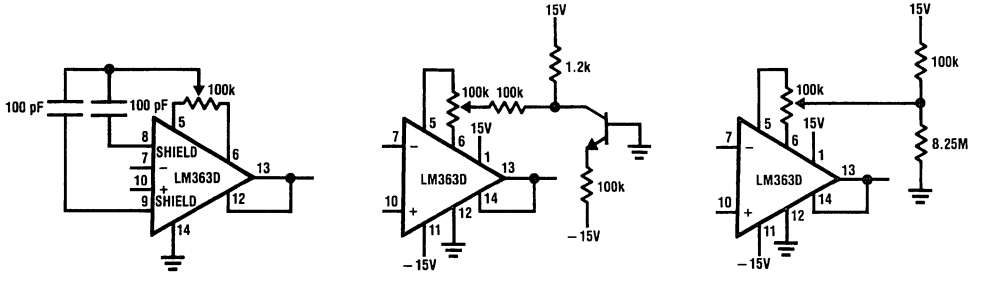


TL/H/5609–18

FIGURE 9. Improved Response using Shield Drivers



a. Bias Current b. Gain c. DC CMRR



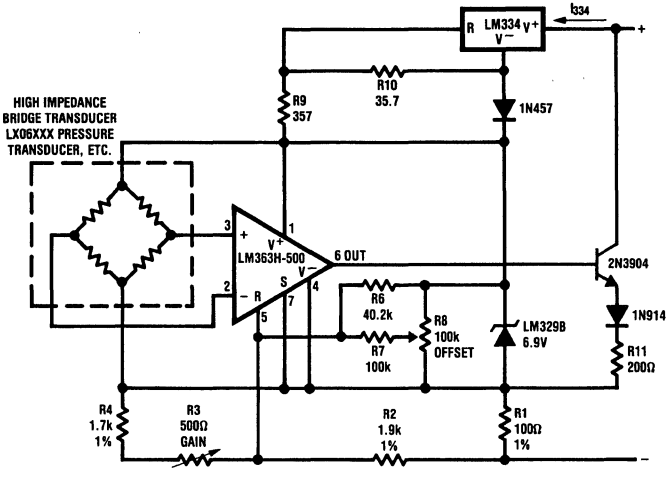
d. AC CMRR e. Negative PSRR f. Positive PSRR

TL/H/5609–19

FIGURE 10. Other Trims for 16-Pin Package

Typical Applications

4 mA-20 mA Two Wire Current Transmitter



TL/H/5609–20

The LM329 reference provides excellent line regulation and gain stability. When bridge is balanced (I_{OUT} = 4 mA), there's no drop across R3 and R4, so that gain and offset adjustments are non-interactive. The LM334 configured as a zero-TC current source supplies quiescent current to circuit. R11 provides current limiting.

Design Equations

$$I_{OS} = (I_{R6} + I_{R7}) \left(1 + \frac{R2}{R1}\right) = 4\ mA$$

$$Gain = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \cong \frac{A_V}{R1} \times \frac{R2 + R3 + R4}{R3 + R4} \cong \frac{10\ mA}{mV}$$

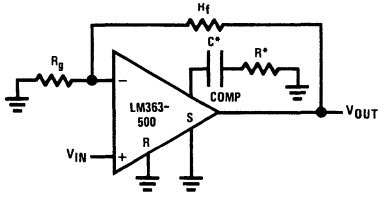
when A_V = LM363 voltage gain

$$Pick\ I_{334} = \frac{0.68V}{R9} + \frac{68\ mV}{R10} \cong 3.8\ mA$$

$$I_{MAX} = I_{334} + \frac{V_Z - 2.4V}{R11} = 26\ mA$$

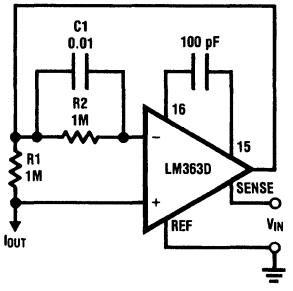
$$I_{BRIDGE(MAX)} \cong I_{334} - I_{363} - I_Z \cong 1.5mA$$

Precision Op Amp



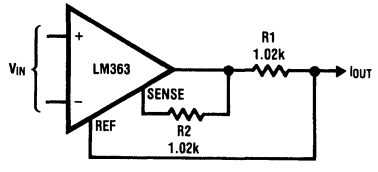
Select for optimum square wave response. Omit for closed loop gains above 100. Not required for instrumentation amplifier configuration.

Precision Current Source (Low Output Current)



TL/H/5609–21

Precision Voltage to Current Converter (Low Input Voltage)



TL/H/5609–22

$R1 = R2$

$Req = R1 \| 50\ k\Omega$

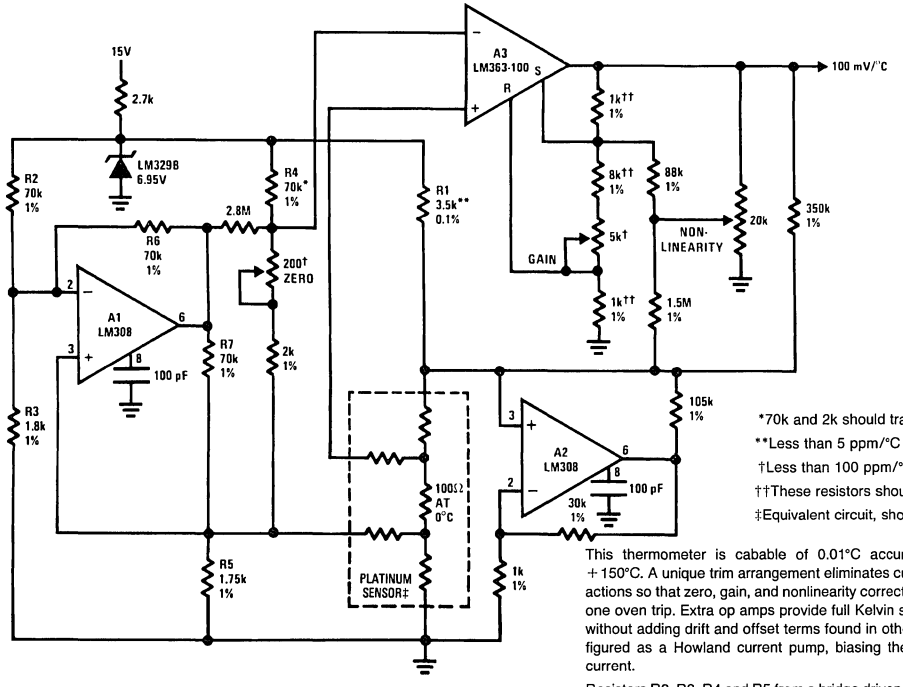
$$I_{OUT} = \frac{G\ V_{IN}}{Req} = \frac{G\ V_{IN}}{1\ k\Omega}$$

$R1 = R2$

$$I_{OUT} = \frac{V_{IN}}{GR1}$$

Typical Applications (Continued)

Curvature Corrected Platinum RTD Thermometer



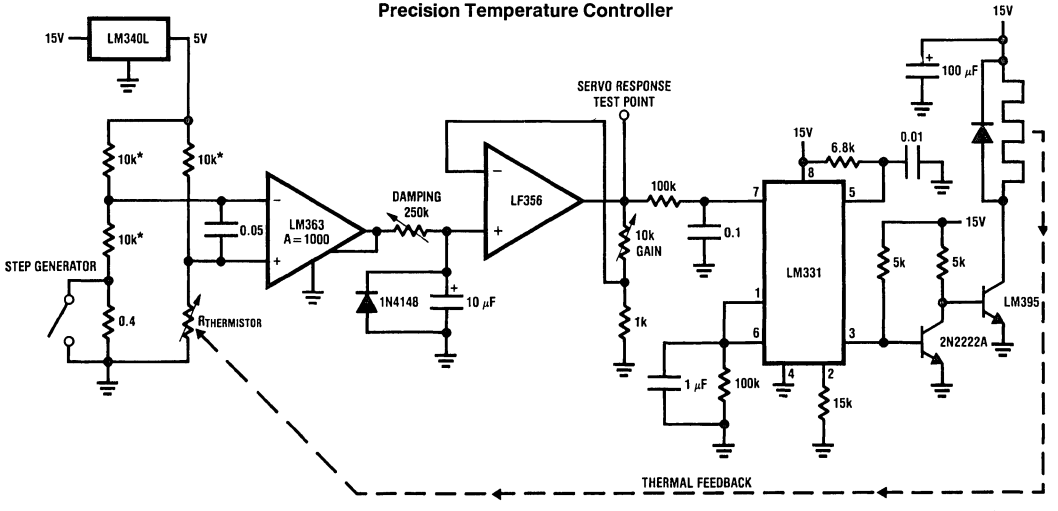
TL/H/5609–23

*70k and 2k should track to 5 ppm/°C
**Less than 5 ppm/°C drift
†Less than 100 ppm/°C drift
††These resistors should track to 20 ppm/°C
‡Equivalent circuit, showing lead resistance

This thermometer is cabable of 0.01°C accuracy over −50°C to +150°C. A unique trim arrangement eliminates cumbersome trim interactions so that zero, gain, and nonlinearity correction can be trimmed in one oven trip. Extra op amps provide full Kelvin sensing on the sensor without adding drift and offset terms found in other designs. A2 is configured as a Howland current pump, biasing the sensor with a fixed current.

Resistors R2, R3, R4 and R5 from a bridge driven into balance by A1. In balance, both inputs of A1 are at the same voltage. Since R6=R7, A1 draws equal currents from both legs of the bridge. Any loading of the R4/R5 leg by the sensor would unbalance the bridge; therefore, both bridge taps are given to the sensor open circuit voltage and no current is drawn.

Precision Temperature Controller



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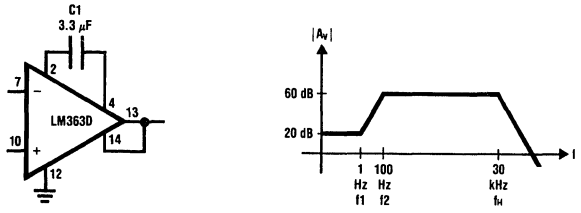
*Ultronix 105A wirewound
Thermistor=Yellow Springs #44032
Setpoint stability=2.5X10−4°C/Hr

Typical Applications (Continued)

Low Frequency Rolloff (AC Coupling)

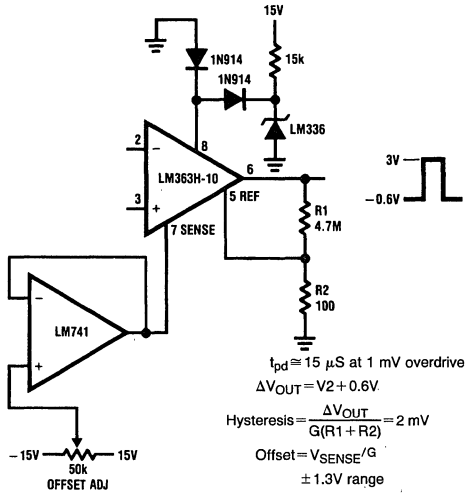


$$f1 = \frac{1}{2\pi C1(50\ k\Omega)} = 1\ Hz$$

f2 = 100 f1 = 100Hz
Reduced DC voltage gain attenuates offset error and 1/f noise by a factor of 100.

TL/H/5609–25

Precision Comparator with Balanced Inputs and Variable Offset



$t_{pd} \cong 15\ \mu S$ at 1 mV overdrive

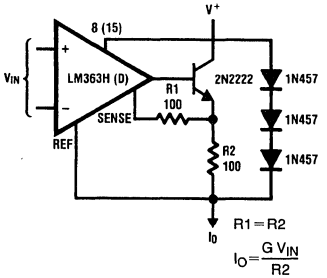
$\Delta V_{OUT} = V2 + 0.6V$

$$\text{Hysteresis} = \frac{\Delta V_{OUT}}{G(R1 + R2)} = 2\ mV$$

$\text{Offset} = V_{SENSE}/G$

±1.3V range

Boosted Current Source with Limiting



R1 = R2

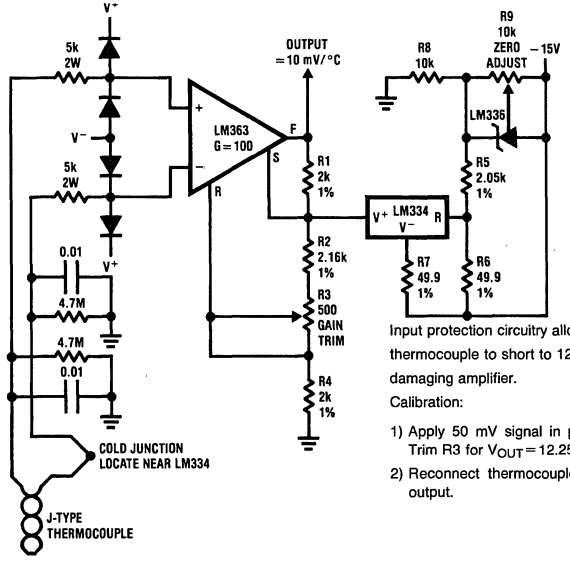
$$I_O = \frac{G\ V_{IN}}{R2}$$

$$I_{MAX} = \frac{V_{BE}}{R2}$$

≅60 mA

TL/H/5609–26

Thermocouple Amplifier with Cold Junction Compensation



Input protection circuitry allows thermocouple to short to 120 V_{AC} without damaging amplifier.

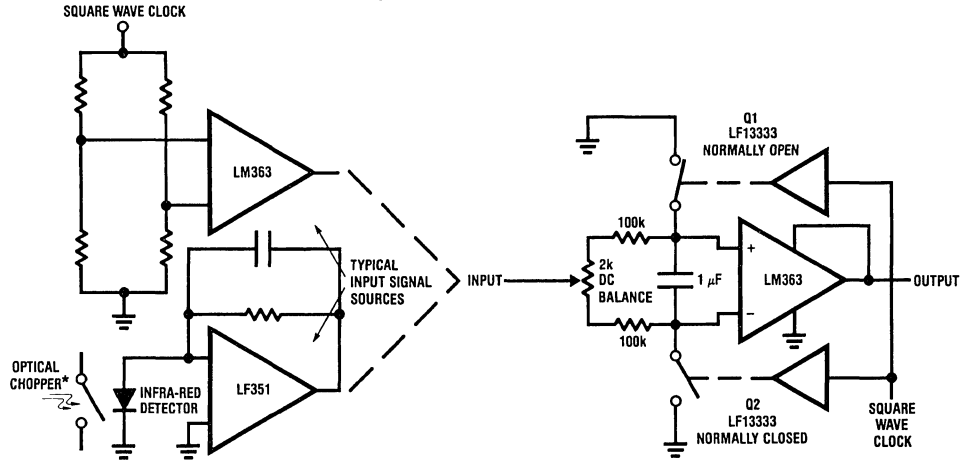
Calibration:

1) Apply 50 mV signal in place of thermocouple. Trim R3 for $V_{OUT} = 12.25V$.
2) Reconnect thermocouple. Trim R9 for correct output.

TL/H/5609–27

Typical Applications (Continued)

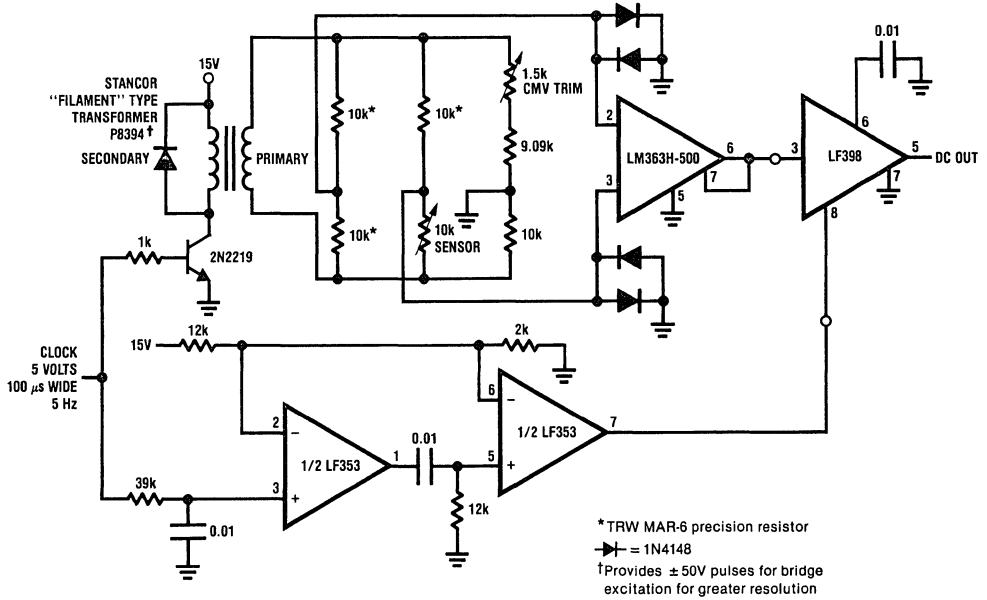
Synchronous Demodulator



TL/H/5609–28

*Use square wave drive produced by optical chopper to run LF13333 switch inputs.

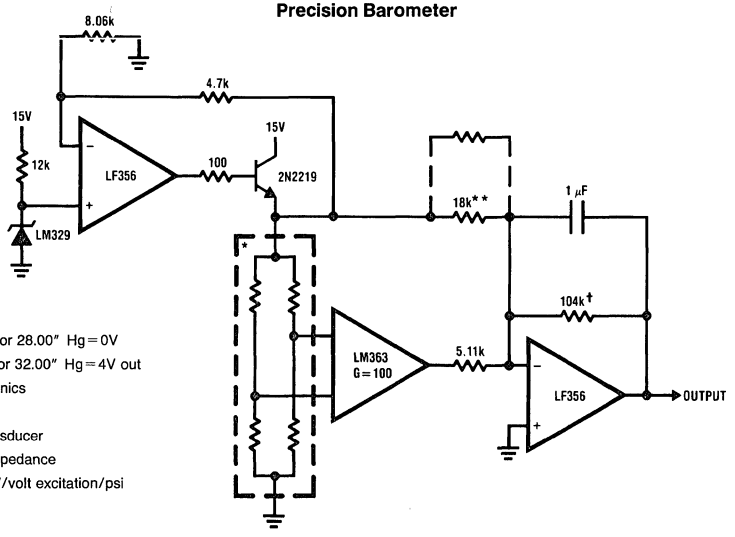
Pulsed Bridge Driver/Amplifier



TL/H/5609–29

Typical Applications (Continued)

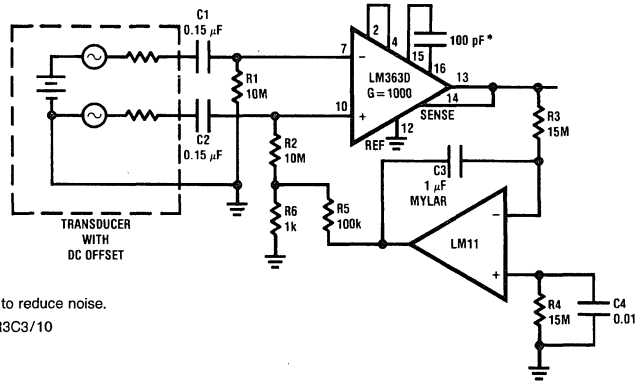
Precision Barometer



**Parallel trim for 28.00" Hg = 0V
†Parallel trim for 32.00" Hg = 4V out
*B.L.H. Electronics
#DHF-444114
Pressure Transducer
350Ω input impedance
Output = 1 mV/volt excitation/psi

TL/H/5609–30

Removing Large DC Offsets



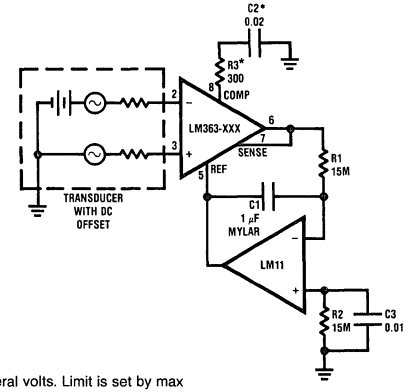
*Optional bandlimiting to reduce noise.
Pick R1C1 = R2C2 = R3C3/10

$$= \frac{1}{2\pi f_l}$$

f_l = 0.1 Hz for values shown. Integrator nulls out offset error to LM363 bias currents flowing into R1 and R2.

TL/H/5609–31

Removing Small DC Offsets



*Optional bandlimiting to reduce noise.
Low frequency break

$$\text{frequency } f_l = \frac{1}{2\pi R1C1} = 0.01 \text{ Hz}$$

Accommodates out referred offset of several volts. Limit is set by max differential between reference and sense terminals.

TL/H/5609–32

Section 7

Surface Mount

Section 7 Contents

National Semiconductor

Surface Mount

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

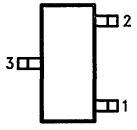
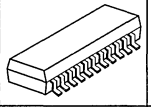
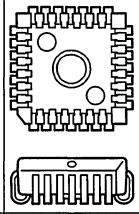
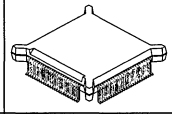
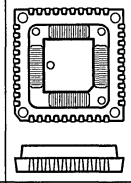
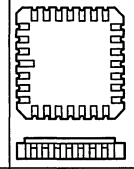
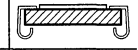
Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

SURFACE MOUNT PACKAGING AT NATIONAL

To help our customers take advantage of this new technology, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK®) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK® (TP)	Leadless Chip Carrier (LCC) (LDCC)	Leaded Chip Carrier
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*)	PCC-20(*) PCC-28(*) PCC-44(*) PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196(*) PQFP-244	TP-40 (*) TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20(*) LCC-28 LCC-32 LCC-44 (*) LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for linear products.

LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A complete list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85
PCC-20	70–100
PCC-28	60–90
PCC-44	40–60

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

TABLE III. Linear Surface Mount Current Device Listing

Amplifiers and Comparators

Part Number	Part Number
LF347WM LF351M LF451CM LF353M	LM392M LM393M LM741CM LM1458M LM2901M
LF355M LF356M LF357M LF444CWM	LM2902M LM2903M LM2904M LM2924M LM3403M
LM10CWM LM10CLWM LM308M LM308AM LM310M	LM4250M LM324M LM339M LM365WM LM607CM
LM311M LM318M LM319M LM324M	LMC669BCWM LMC669CCWM
LM339M LM346M LM348M LM358M LM359M	LF441CM

Regulators and References

Part Number	Part Number
LM317LM LF3334M	LM2931M-5.0 LM3524M LM78L05ACM LM78L12ACM LM78L15ACM
LM336M-2.5 LF336BM-2.5 LM336M-5.0 LM336BM-5.0 LM337LM	LM79L05ACM LM79L12ACM LM79L15ACM LP2951ACM LP2951CM
LM385M LM385M-1.2	
LM385BM-1.2 LM385M-2.5 LM385BM-2.5 LM723CM LM2931CM	

Data Acquisition Circuits

Part Number	Part Number
ADC0802LCV ADC0802LCWM ADC0804LCV ADC0804LCWM ADC0808CCV ADC0809CCV	ADC1025BCV ADC1025CCV DAC0800LCM DAC0801LCM DAC0802LCM DAC0806LCM DAC0807LCM
ADC0811BCV ADC0811CCV ADC0819BCV ADC0819CCV ADC0820BCV ADC0820CCV	DAC0808LCM DAC0830LCWM DAC0830LCV DAC0832LCWM DAC0832LCV
ADC0838BCV ADC0838CCV ADC0841BCV ADC0841CCV ADC0848BCV ADC0848CCV ADC1005BCV ADC1005CCV	

Industrial Functions

Part Number	Part Number
AH5012CM LF13331M LF13509M LF13333M LM555CM	LM13600M LM13700M LMC555CM LM567CM MF4CWM-50
LM556CM LM567CM LM1496M LM2917M	MF4CWM-100 MF6CWM-50 MF10CCWM MF6CWM-100 MF5CWM
LM3046M LM3086M LM3146M	

Commercial and Automotive

Part Number	Part Number
LM386M-1 LM592M LM831M LM832M LM833M	LM1837M LM1851M LM1863M LM1865M LM1870M
LM837M LM838M LM1131CM	LM1894M LM1964V
	LM2893M LM3361AM LM1881M

Hybrids

Part Number	Part Number
LH0002E	LH0032E
LH4002E	LH0033E

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20	M	40	1000
SO-24	M	30	1000
PCL-20	V	50	1000
PCL-28	V	40	1000
PCL-44	V	25	500
PQFP-196	VF	TBD	—
TP-40	TP	100	TBD
LCC-20	E	50	—
LCC-44	E	25	—

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324M ICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324M ICs with date code A

    Pack #2 has 500 LM324M ICs with date code A

    Pack #3 has 2,000 LM324M ICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

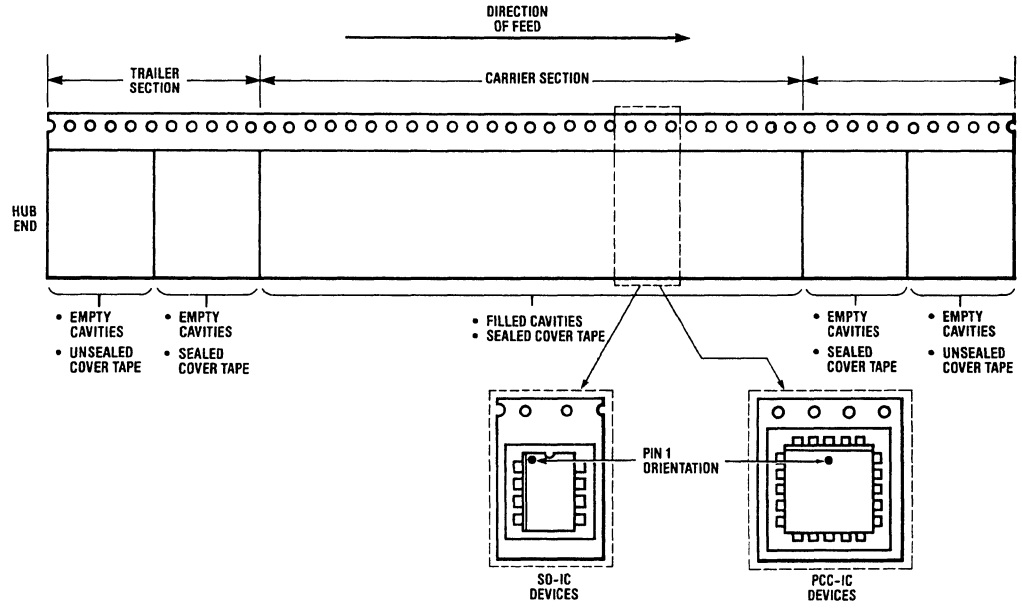
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5
Plastic Chip Carrier IC					
PCC-20	2	2	1000	5	5
PCC-28	2	2	750	5	5
PCC-44	2	2	500	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION



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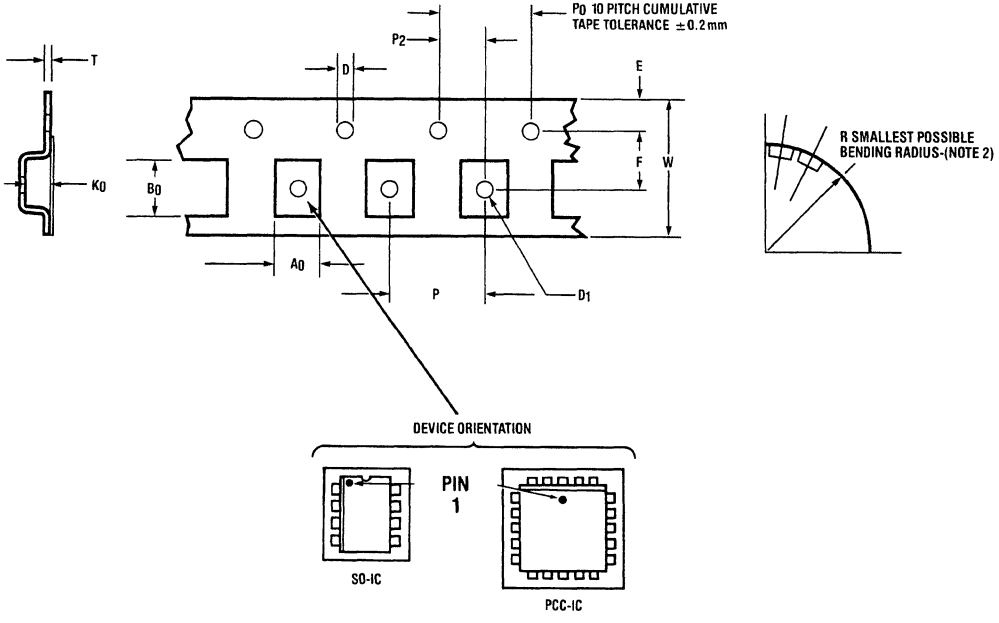
MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  - (1) Conductive cover available
- Reel:
  - (1) Solid 80 pt fibreboard (standard)
  - (2) Conductive fibreboard available
  - (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)



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Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

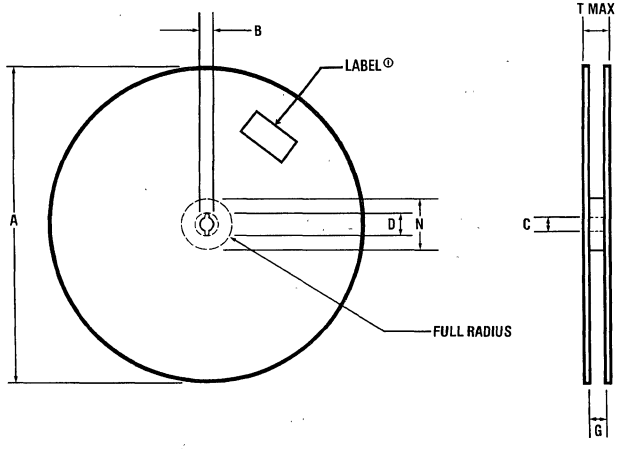
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



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STAR™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number

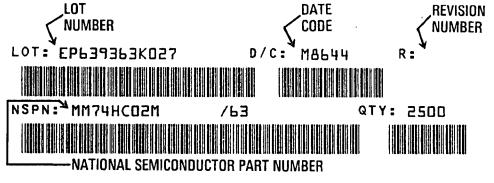
Date Code

Revision Level

National Part No. I.D.

Qty.

EXAMPLE



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Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.
b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.

1. Components on the same side of PW Board.

   Lead insert standard DIPS onto PW Board Wave solder (conventional)

   Wash and lead trim

   Dispense solder paste on SMD pads

   Pick and place SMDs onto PW Board

   Bake

   Vapor phase/IR reflow

   Clean

2. Components on opposite side of PW Board.

   Lead insert standard DIPs onto PW Board

   Wave Solder (conventional)

   Clean and lead trim

   Invert PW Board

   Dispense solder paste on SMD pads

   Dispense drop of adhesive on SMD sites (optional for smaller components)

   Pick and place SMDs onto board

   Bake/Cure

   Invert board to rest on raised fixture

   Vapor/IR reflow soldering

   Clean

B) Vapor/IR reflow solder then Wave Solder.

1. Components on the same side of PW Board.

   Solder paste screened on SMD side of Printed Wire Board

   Pick and place SMDs

   Bake

   Vapor/IR reflow

   Lead insert on same side as SMDs

   Wave solder

   Clean and trim underside of PCB

C) Vapor/IR reflow only.

1. Components on the same side of PW Board.

   Trim and form standard DIPs in "gull wing" configuration

   Solder paste screened on PW Board

   Pick and place SMDs and DIPs

   Bake

   Vapor/IR reflow

   Clean

2. Components on opposite sides of PW Board.

   Solder paste screened on SMD-side of Printed Wire Board

   Adhesive dispensed at central location of each component

   Pick and place SMDs

   Bake

   Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads

   Lead insert DIPs

   Vapor/IR reflow

   Clean and lead trim

D) Wave Soldering Only

1. Components on opposite sides of PW Board.

   Adhesive dispense on SMD side of PW Board

   Pick and place SMDs

   Cure adhesive

   Lead insert top side with DIPs

   Wave solder with SMDs down and into solder bath

   Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. Howerver, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

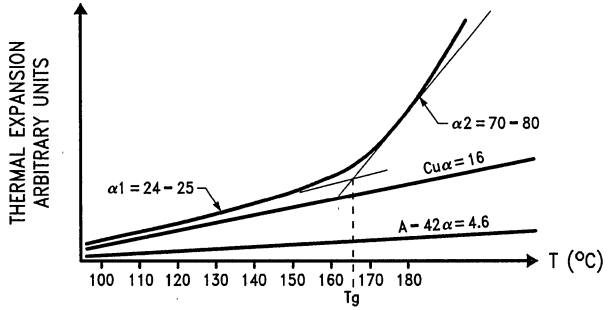

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FIGURE 1. Thermal Expansion and Glass Transition Temperature

Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

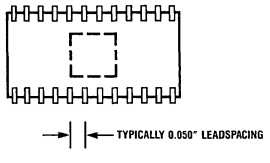
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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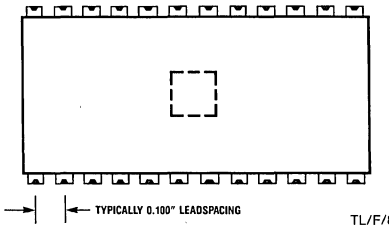
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

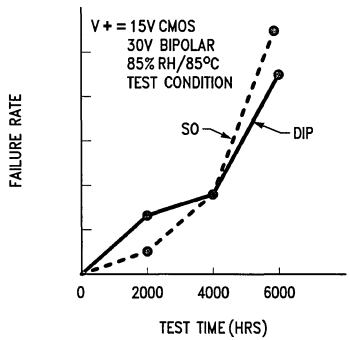

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

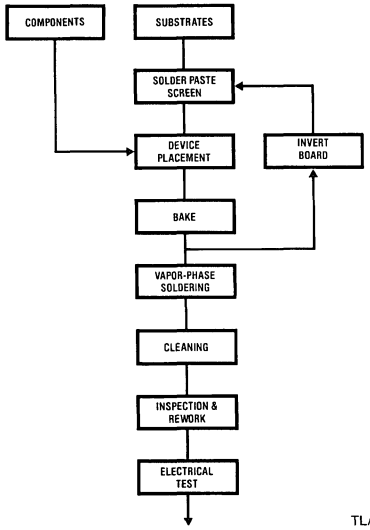
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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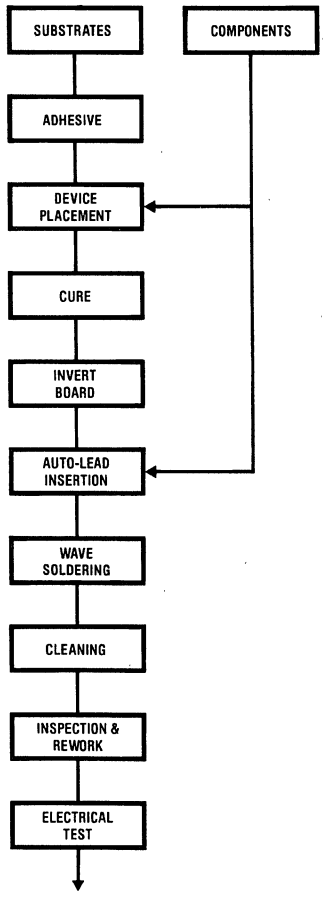
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

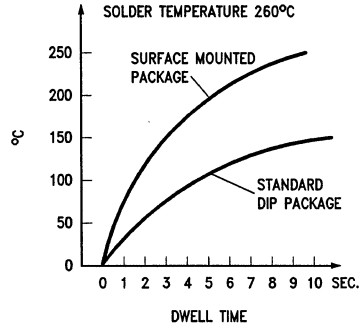

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

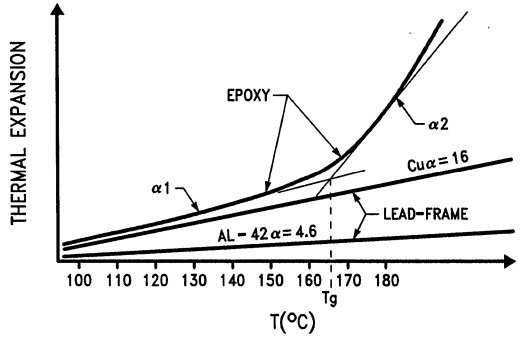

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

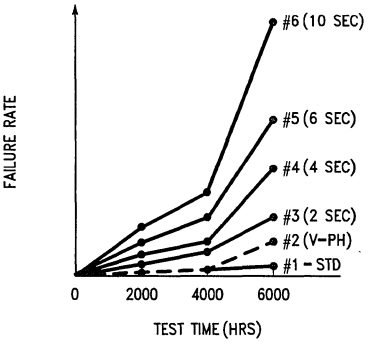

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

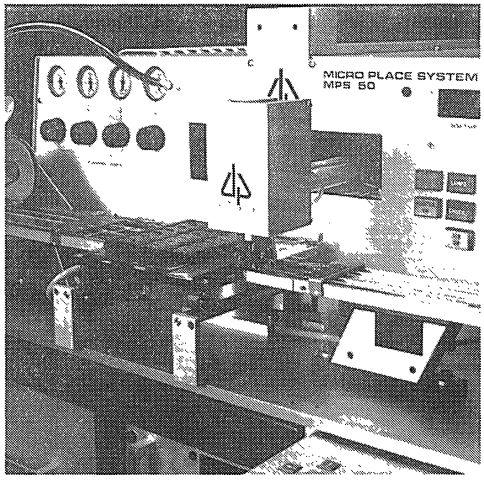
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

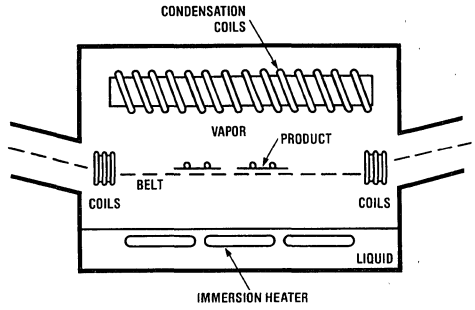
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

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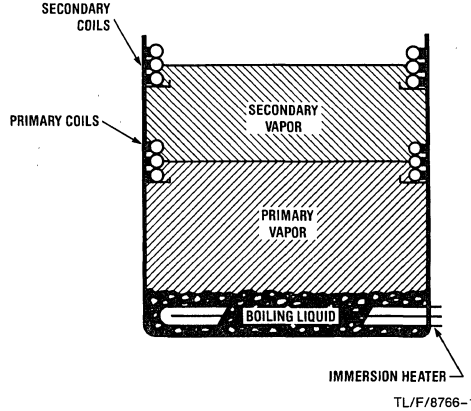
Batch-Fed Production Vapor-Phase Soldering Unit



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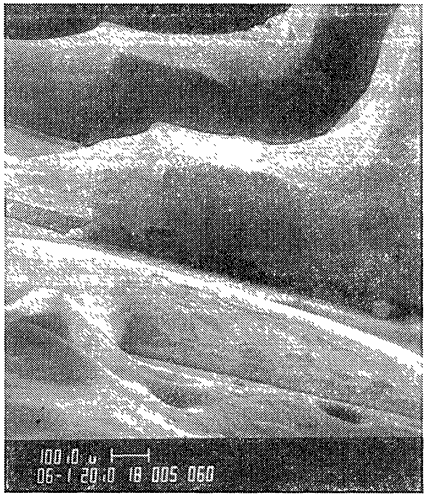
Solder Joints on a SO-14 Package on PCB



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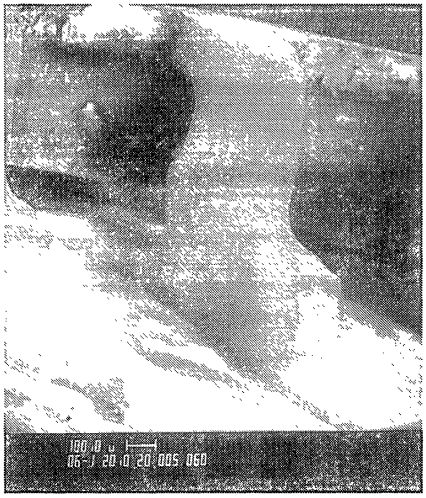
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8", to avoid damage to screens and minimize distortion.

SOLDER PASTE

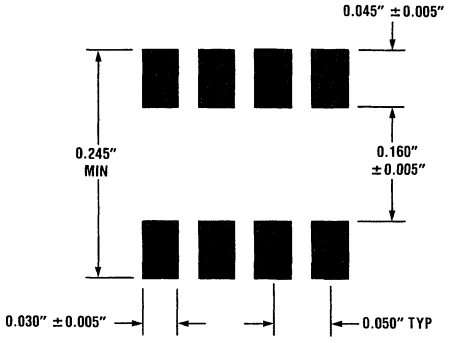
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

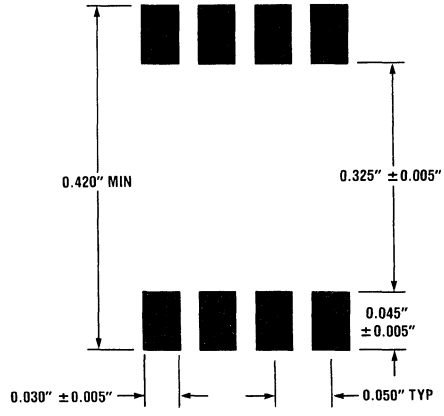
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



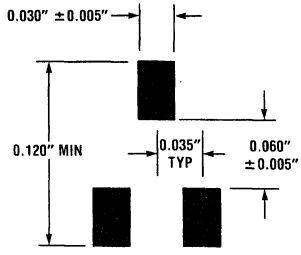
TL/F/8766–14

SO-16L, SO-20



TL/F/8766–15

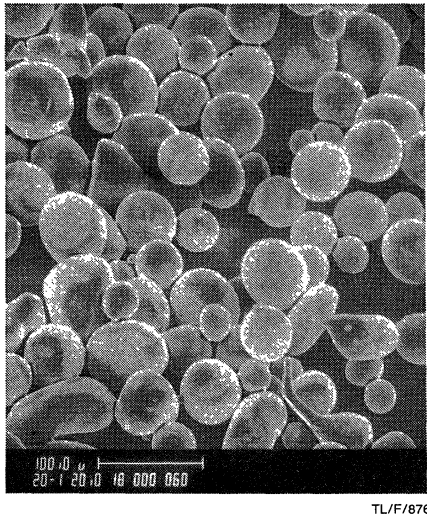
SOT-23



TL/F/8766–16

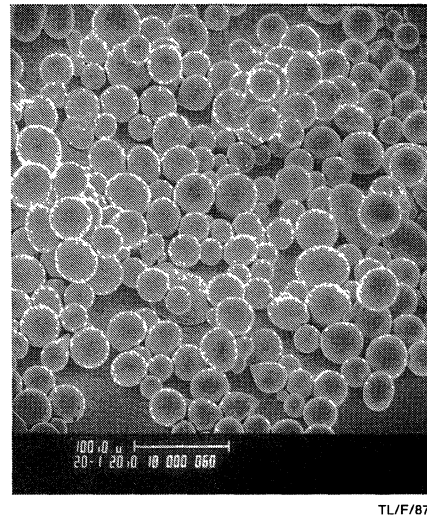
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



TL/F/8766–17

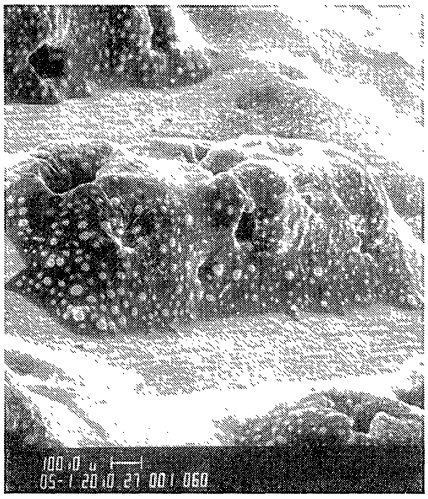
200 × Kester (63/37)



TL/F/8766–18

Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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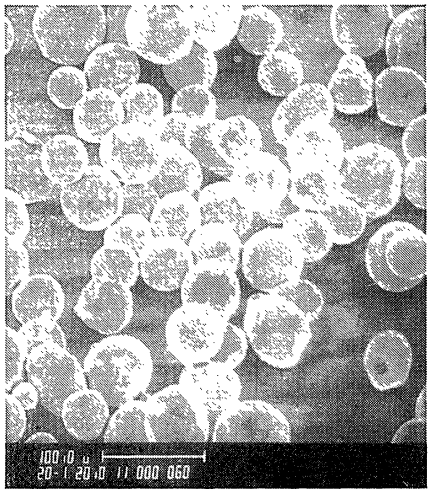
200 × Fry Metal (63/37)



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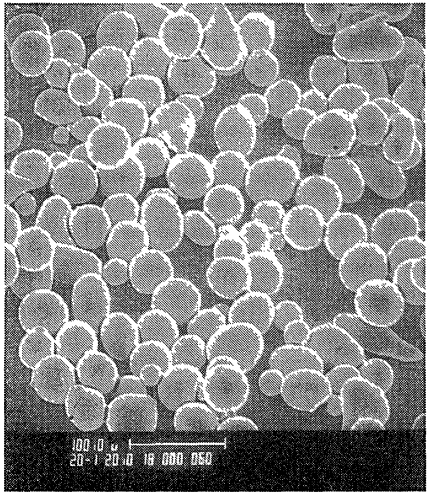
200 ESL (63/37)



TL/F/8766–21

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

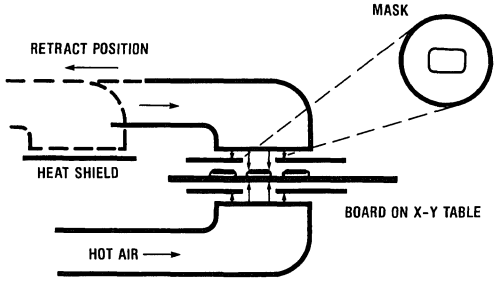
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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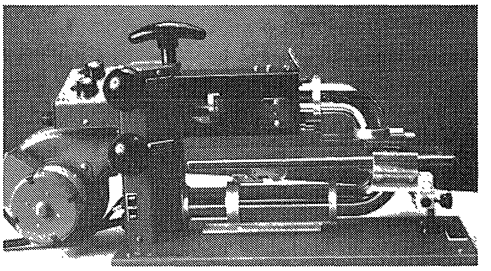
Hot-Air Rework Machine



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WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

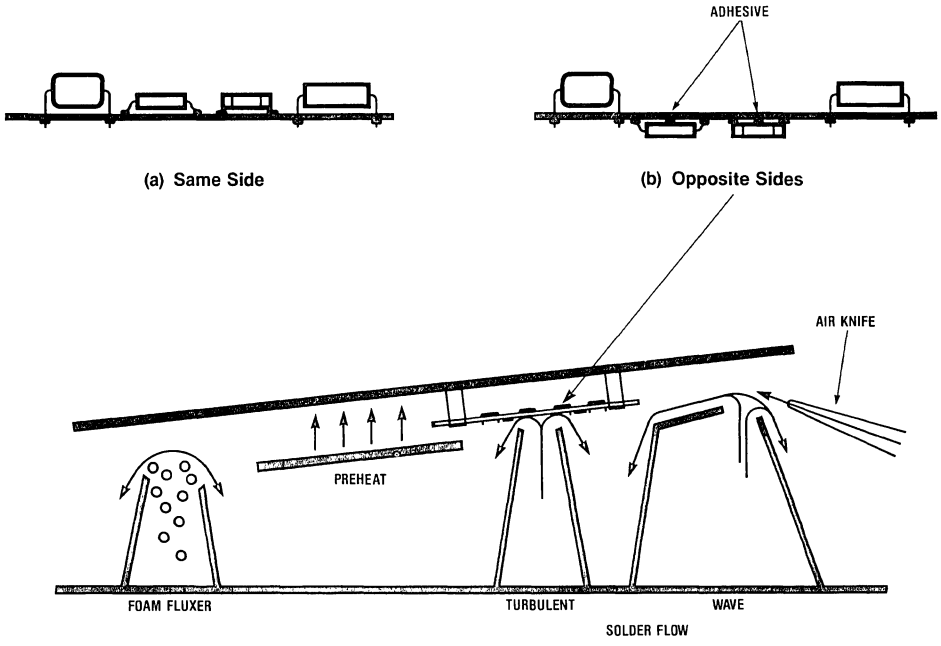
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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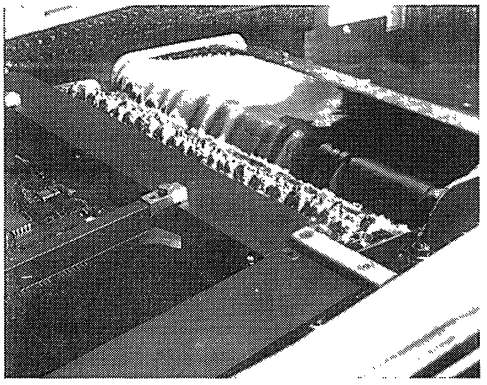
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



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CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Section 8

Appendices/ Physical Dimensions

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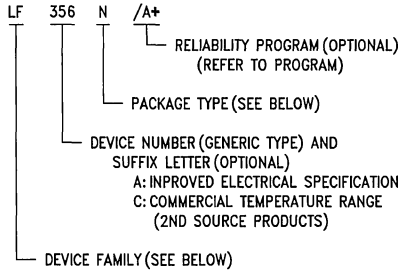
National Semiconductor

Appendix A
General Product Marking & Code Explanation



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Device Family

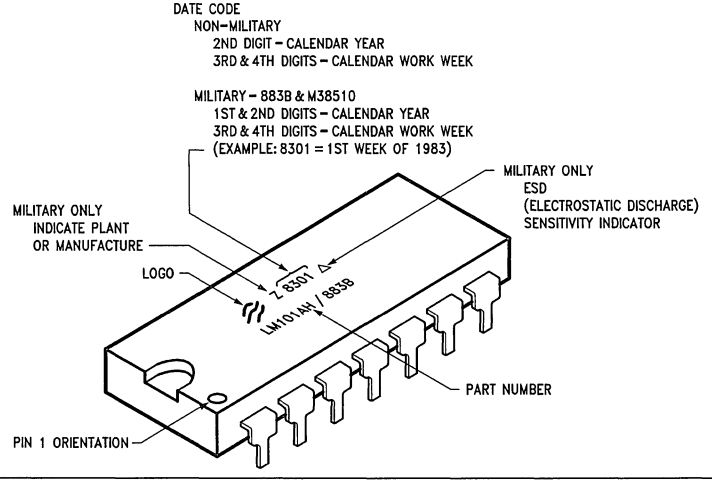
Integrated Circuits (IC's)

ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
AM	Analog Switch (Monolithic)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (Bifet)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LP	Linear (Low Power)
MF	Linear (Monolithic Filter)
SL	Special Linear
LMF	Linear Monolithic Filter

Package Type*

IC's Only

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼" x ¼")
G	12 Lead TO-8 M/C
H	Multi-Lead M/C
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP (Sometimes referred to as the "Fit-Seal" Package).
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 PWR Pkg
Q	Cerdip with UV Window
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package



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National Semiconductor **Appendix B**

APPLICATION NOTE REFERENCED BY PART NUMBER

National Semiconductor Linear Application notes are normally written to explain the operation and use of a particular device or family of IC's, or to present alternative technical solutions. The following PART NUMBER index references the published application notes that would offer application assistance for those specific IC's.

The 1986 Linear Applications Handbook is a complete text for all current Application Notes for both Monolithic and Hybrid products. Specific Application Notes are available upon request through National Semiconductor Sales Offices.

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LM1812	AB-20
LM1818	AN-407
LM1820	LB-29
LM1823	AN-391
LM1828	Appendix B
LM1830	AB-10
LM1837	AN-407
LM1845	Appendix B
LM1863	AN-381, AN-382
LM1865	AN-382, AN-390
LM1870	AN-382
LM1886	AN-402
LM1889	AN-402
LM1894	AN-384, AN-386, AN-390
LM1897	AN-407
LM2878	AN-147
LM2889	AN-391, AN-402
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11

DEVICE NUMBER	APPLICATION NOTE
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3820	AN-147, LB-29
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27
LM3914	LB-48, AB-25
LM3915	AN-386
LM3999	AN161
LM4250	AN-88, LB-34
LM7800	AN-178
LM78L12	AN-146
LMC835	AN-435
LP324	AN-284
MF10	AN-307
MM1458	AN-116
MM1558	AN-116
MM1558C	AN-116
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74LS138	LB-54
2N4339	AN-32
LH4101	AN-480
LM34/35	AN-460
LM32900	AN-478
LM3578	AB-30
LPXXXX	AN-462
LM34	AN-462
LM35	AN-462
LM385	AN-462
LMC13334	AN-462
LP2950	AN-462
LP2951	AN-462
LP311	AN-462
LP324	AN-462
LP339	AN-462
LP365	AN-462

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Appendix C
Summary of Commercial Reliability Programs

General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

Note: Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

P+ Product Enhancement

The P+ product enhancement program applies to regulator devices and offers an added advantage. P+ involves a dynamic self-heating burn-in that tests the thermal shutdown of the regulator. P+ is proven more effective than the standard 125°C burn-in as an early screen for infant mortality defects. It sharply reduces the cost of testing incoming components. Reliability Report L-140 further explains the P+ process. The following chart lists regulators which receive P+ prior to shipment and at no additional cost.

Device	Package Types				
	TO-3 K STEEL	TO-39 H	TO-220 T	TO-202 P	TO-92 Z
LM109/309	X	X			
LM117/317	X	X	X	X	
LM117HV/317HV	X	X			
LM120/320	X	X	X	X	
LM123/323	X				
LM137/337	X	X	X	X	
LM137HV/337HV	X	X			
LM138/338	X				
LM140/340	X	X	X	X	
LM145/345	X				
LM150/250/350	X				
LM196/396	X				
LM2930/2935/2940/2984			X		
LM2931			X		X
LM78XX			X		

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Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government-certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales offices, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

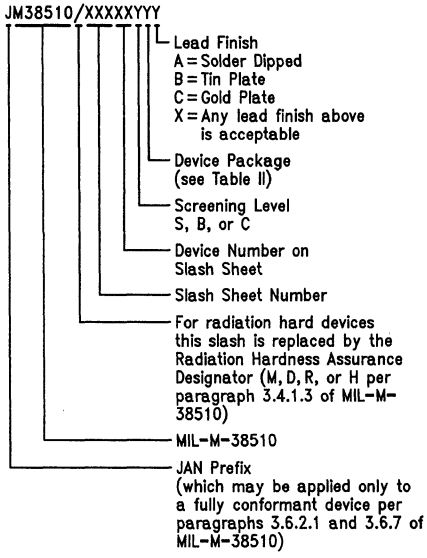
As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking



CI24-1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4" X 1/4" (metal) flat pack
B	14-Pin 3/16" X 1/4" flat pack
C	14-Pin 1/4" X 3/4" dual-in-line
D	14-Pin 1/4" X 3/8" (ceramic) flat pack
E	16-Pin 1/4" X 3/8" dual-in-line
F	16-Pin 1/4" X 3/8" (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4" x 1/4" (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2" x 1-1/4" dual-in-line
K	24-pin 3/8" x 5/8" flat pack
L	24-pin 1/4" x 1-1/4" dual-in-line
M	12-pin TO-101 can or header
N	(Note 1)
P	8-pin 1/4" x 3/8" dual-in-line
Q	40-pin 3/16" x 2-1/16" dual-in-line
R	20-pin 1/4" x 1-1/16" dual-in-line
S	20-pin 1/4" x 1/2" flat pack
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" dual-in-line
W	22-pin 3/8" x 1-1/8" dual-in-line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" chip carrier
3	28-terminal 0.450" x 0.450" chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		—
2. Nondestructive Bond Pull	2023	100%		—
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, 24 hrs. Min.	100%	1008, Condition C, 24 hrs. Min.	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min.) Y_1 Orientation Only	100%	2001, Condition E, (Min.), Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		—
9. Serialization	(Note 5)	100%		—
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	—
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		—
15. PDA Calculation	5% Parametric (Note 14), 3% Functional −25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test	Per Applicable Device Specification		Per Applicable Device Specification	
a) Static Tests				
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005)		100%		100%
c) Functional Test, 25°C (Subgroup 7, Table I, 5005)		100%		100%

TABLE III. 100% Screening Requirements (Continued)

Screen	Class S		Class B	
	Method	**Reqmt**	**Method**	**Reqmt**
17. Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18. Radiographic (Note 10)	2012 Two Views	100%		—
19. Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20. External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 19.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when past burn-in delta measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
AH0014D	x			
AH0015D	x			
AH0019D	x			
LF111H	x			
LF11201D		x		
LF11202D		x		
LF11331D		x		
LF11332D		x		
LF11333D		x		
LF11508D	x			
LF11509D	x			
LF147D		x		
LF155AH		x		
LF155H		x		x
LF155J-8				x
LF155W				x
LF156AH		x		
LF156H		x		x
LF156J-8				x
LF156W				x
LF157AH		x		
LF157H		x		
LF198H		x		
LF411MH		x		x
LF411W				x
LF412MH		x		x
LF441MH	x			
LF442MH		x		
LF444MD		x		
LH0002H		x	x	
LH0003H	x			
LH0004H	x			
LH0020G	x			
LH0021K	x			
LH0022D	x			
LH0022H	x			
LH0023G	x			
LH0024H	x			

Device Type	Mil * Class B	883 Class B	Desc	JAN
LH0032G	x		x	
LH0033AG	x			
LH0033G	x		x	
LH0036G	x			
LH0038D	x			
LH0041G	x			
LH0042D	x			
LH0042H	x			
LH0043G	x			
LH0044AH	x			
LH0044H	x			
LH0052H	x			
LH0053G	x			
LH0061K	x			
LH0062D	x			
LH0062H	x			
LH0063K	x			
LH0070-0H	x			
LH0070-1H	x			
LH0070-2H	x			
LH0071-0H	x			
LH0071-1H	x			
LH0071-2H	x			
LH0075G	x			
LH0076G	x			
LH0082D	x			
LH0084D	x			
LH0086D	x			
LH0091D	x			
LH0094D	x			
LH00101AK	x			
LH0101K	x			
LH2101AD		x		
LH2108AD		x		
LH2108D		x		
LH2110D		x		
LH2111D		x		
LH2111F	x			

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

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Device Type	Mil * Class B	883 Class B	Desc	JAN
LH24250F	x			
LM10H		x		
LM101AH		x		x
LM101AJ-14		x		x
LM101AJ		x		
LM101AW				x
LM102H		x		
LM103H-3.0		x	x	
LM103H-3.3		x	x	
LM103H-3.6		x	x	
LM103H-3.9		x	x	
LM104H		x		
LM105H		x		
LM106H		x		
LM107H		x		
LM107J-14		x		
LM107J		x		
LM108AH		x		x
LM108AJ-8		x		x
LM108AJ		x		
LM108AW				x
LM108H		x		
LM108J-8		x		
LM108J		x		
LM109H		x		
LM109KSTEEL		x		
LM11H		x		
LM110H		x		
LM110J-8		x		
LM110J		x		
LM111H		x		x
LM111J		x		x
LM111W				x
LM112H		x		
LM113-1H		x	x	
LM113-2H		x	x	
LM113H		x	x	
LM117H		x	x	x

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM117HVH		x	x	
LM117HVKSTL		x	x	
LM117KSTEEL		x	x	x
LM118H		x		x
LM118J-8		x		x
LM118J		x		
LM118W				x
LM119H		x	x	
LM119J		x	x	
LM120H-12		x		
LM120H-15		x		
LM120H-5.0		x		
LM120K-12		x		
LM120K-15		x		
LM120K-5.0		x		
LM121AH		x		
LM121H		x		
LM122H		x		
LM123KSTEEL		x		
LM124AJ		x		
LM124J		x		x
LM125H		x		
LM126H		x		
LM129AH		x		
LM129BH		x		
LM131AH		x		
LM131H		x		
LM135H		x		
LM136AH-2.5		x	x	
LM136H-2.5		x		
LM136H-5.0		x		
LM137H		x	x	
LM137HVH		x	x	
LM137HVKSTEEL		x	x	
LM137KSTEEL		x	x	
LM138KSTEEL		x		
LM139AJ		x		
LM139J		x		x

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM139W				x
LM140AK-12		x		
LM140AK-15		x		
LM140AK-5.0		x		
LM140K-12		x		
LM140K-15		x		
LM140K-5.0		x		
LM140LAH-12		x		
LM140LAH-15		x		
LM140LAH-5.0		x		
LM143H		x	x	
LM144H		x	x	
LM145K-5.0		x		
LM145K-5.2		x		
LM146J		x		
LM148J		x		x
LM149J		x		
LM150KSTEEL	x			
LM1536H		x	x	
LM1558H		x		
LM1558J		x		
LM158AH		x		
LM158AJ		x		
LM158H		x		
LM158J		x		
LM1596H	x			
LM160H		x		
LM160J-14		x		
LM160J		x		
LM161F	x			
LM161H		x		
LM161J		x		
LM185BXH-1.2		x		
LM185BYH-1.2		x		

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM185H-1.2		x		
LM193AH		x		
LM193H		x		x
LM193J-8				x
LM193W				x
LM194H		x		
LM195H		x		
LM195K		x		
LM199AH-20		x		
LM199AH		x		
LM199H		x		
LM4250H	x			
LM4250J	x			
LM555H		x		
LM555J		x		
LM556J	x			
LM567H		x		
LM709AH		x		
LM709H		x		
LM710H		x		
LM723H		x		
LM723J				x
LM725H		x		
LM733H	x			
LM741AJ-14		x		
LM741AJ		x		
LM741H		x		x
LM7415-14		x		
LM741J		x		x
LM741W				x
LM747H		x		x
LM747J		x		
LM748H		x		
LM748J		x		

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

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Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

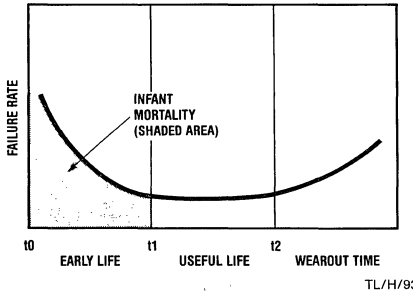

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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

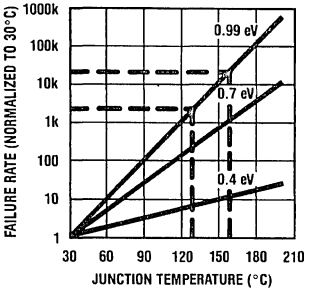

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

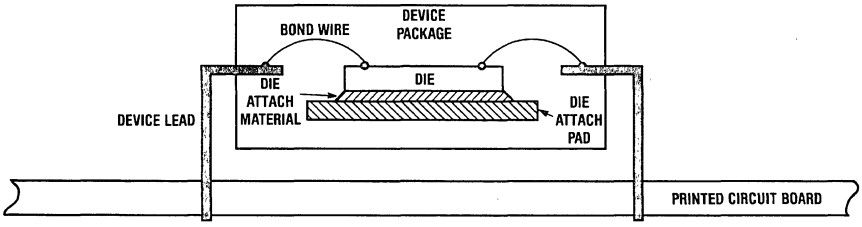

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

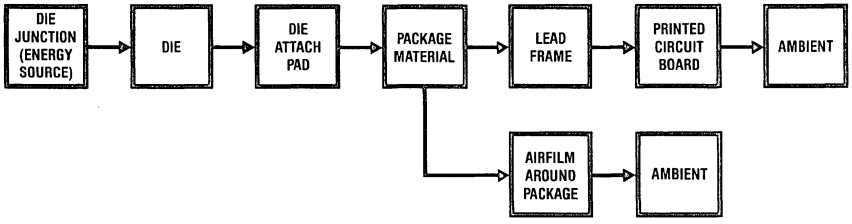

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, $T_A(max)$, the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

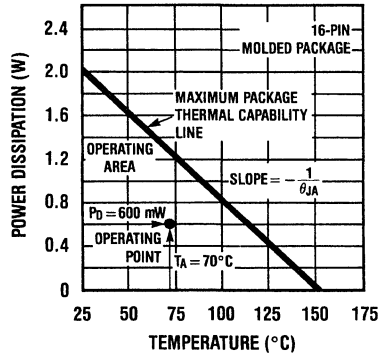

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

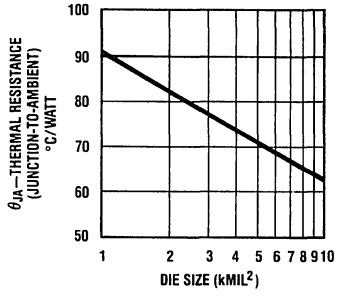

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

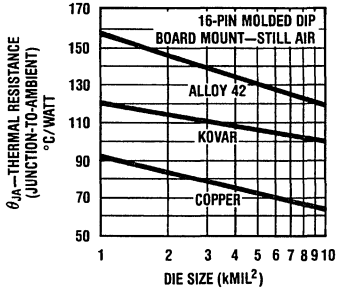

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

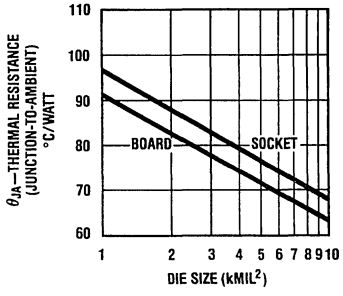

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

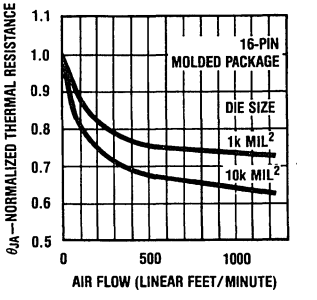

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

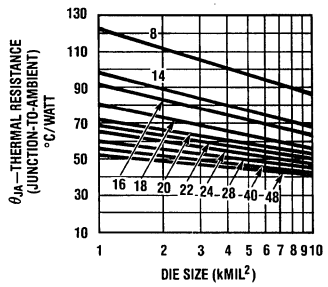
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$= 945\ mW$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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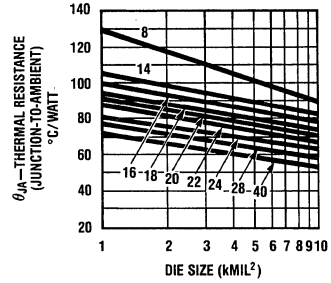
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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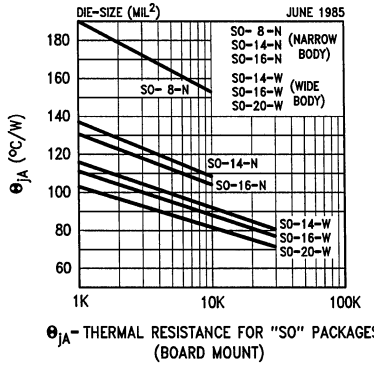
FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)



Θ_{JA} - THERMAL RESISTANCE FOR "SO" PACKAGES (BOARD MOUNT)

TL/H/9312–12

FIGURE 12

National Semiconductor

APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F $T_{MIN} \le T_A \le T_{MAX}$ $0 \le I_L \le 1$ mA	±0.4 **±0.5**	±1.0	**±3.0**	±0.4 **±0.5**	±1.0	**±3.0**	mV/mA mV/mA
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	5V ≤ V_S ≤ 30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	4V ≤ V_S ≤ 30V, +77°F	+0.5	2.0		0.5	2.0		µA
	5V ≤ V_S ≤ 30V	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: −50°F ≤ T_j ≤ + 300°F for the LM34 and LM34A; −40°F ≤ T_j ≤ +230°F for the LM34C and LM34CA; and +32°F ≤ T_j ≤ + 212°F for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for 230°F ≤ T_j ≤ 300°F. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1.*

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

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Appendix G
Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

NSC Part Number	Replacement	Note
ADB1200	ADC3711	2
DAC1200/1201	DAC1265	2
LF352	LM3631	2
LF13300	ADC3711	2
LH0001	LM4250	2
LH0005/LH0005A	LH0003	2
LH0037	LH0036	3
LH0132	LH0032	2
LH2011	LM11	2
LH2201A	LM201A	2
LH2208	LM208	2
LH2208A	LM208A	2
LH24250	LM11	2
LM170/270/370	LM13600N	2
LM171/271/371	no replacement	
LM172/272/372	no replacement	
LM173/273/373	no replacement	
LM174/274/374	no replacement	
LM175/275/375	no replacement	
LM216/316	LM11	2
LM388N-2/N-3	LM388N-1	2
LM377N	LM2877P	3
LM378N	LM2878P	3
LM379	LM2879T	3
LM1014	no replacement	
LM1017	no replacement	
LM1019	no replacement	
LM1821S	LM1823	2
LM1822	LM1823	3
LM1828	no replacement	
LM1848	no replacement	
LM1877N-1/N-2/N-3	LM1877N-9	2
LM2003	no replacement	
LM2808	no replacement	
LM2831	LM1851	2
LM3011	no replacement	
LM3064	no replacement	
LM3075	no replacement	
TBA120V	no replacement	
TBA440C	LM1823	2
TBA510	no replacement	
TBA530	no replacement	
TBA540	no replacement	
TBA560C	no replacement	
TBA920	no replacement	
TBA950-2	no replacement	
TBA970	no replacement	
TBA990	no replacement	
TDA440	no replacement	
TDA2522/23	no replacement	
TDA2530	no replacement	
TDA2530/31	no replacement	
TDA2540/41	no replacement	
TDA2560	no replacement	
TDA2590	no replacement	
TDA3500	no replacement	

Note 1: IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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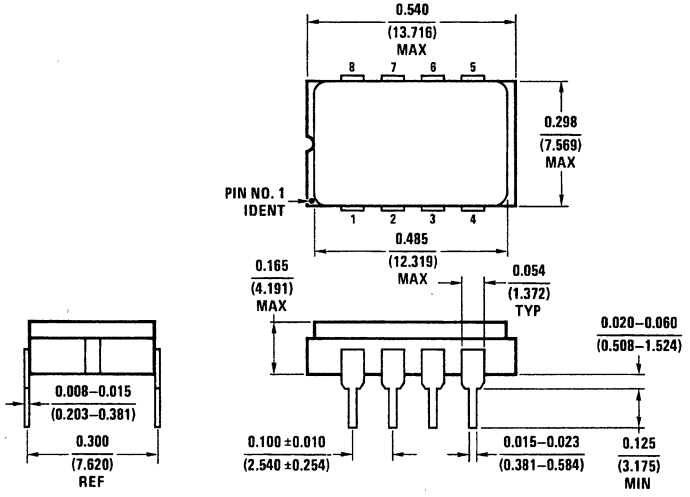
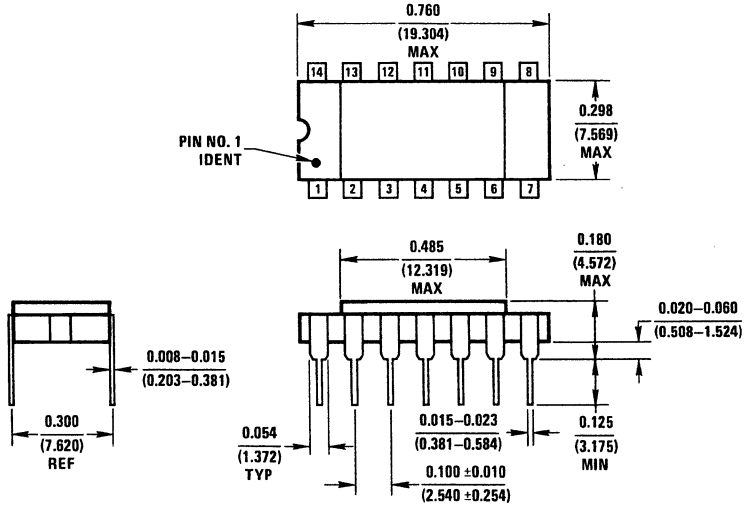
All dimensions are in inches (millimeters)

8 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D08C



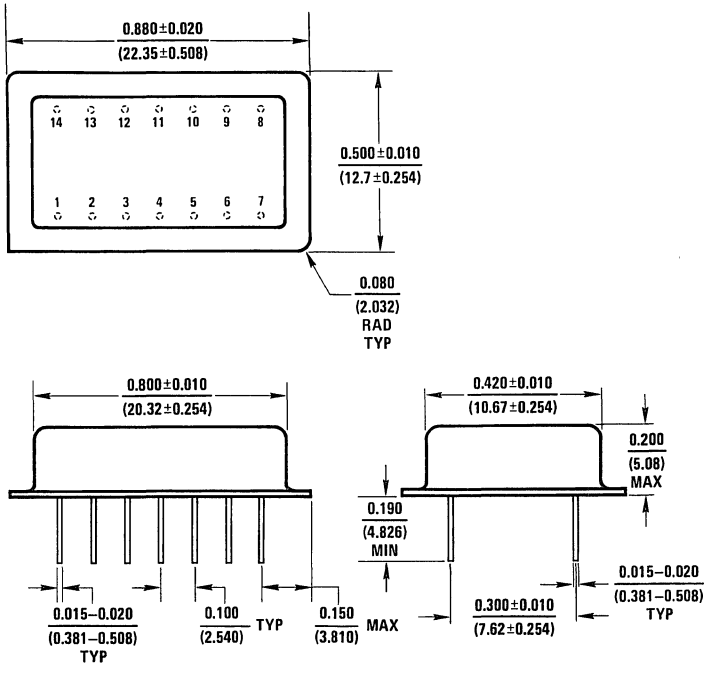
D08C (REV C)

14 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D14E



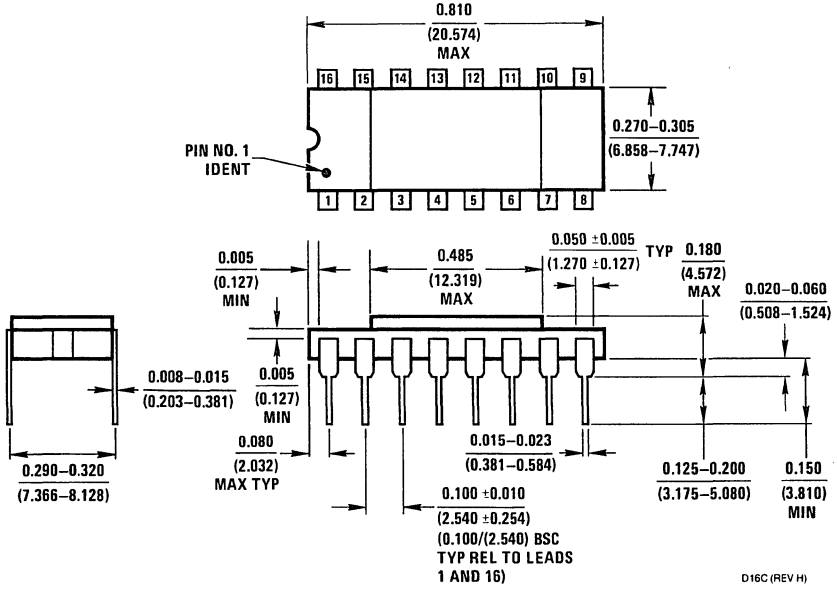
D14E (REV E)

14 Lead Hybrid Metal Can Dual-In-Line Package (D)
NS Package Number D14F



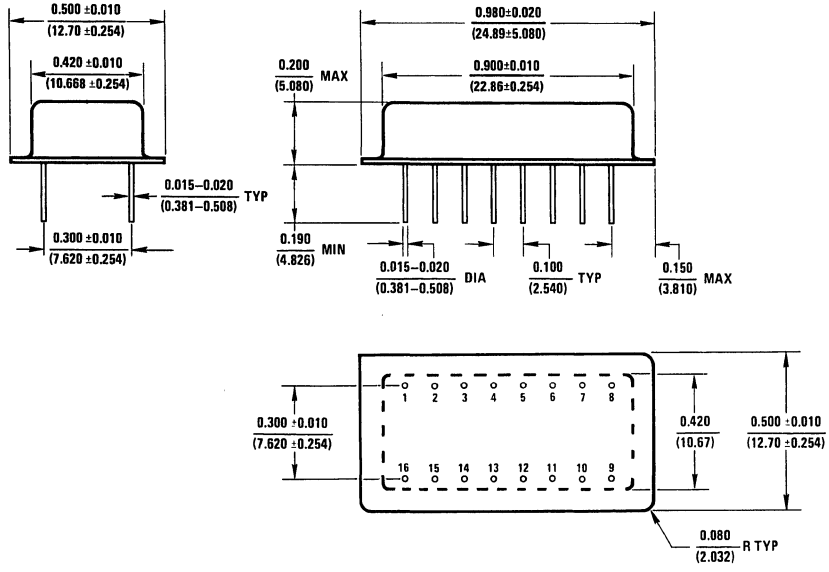
D14F (REV A)

16 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D16C



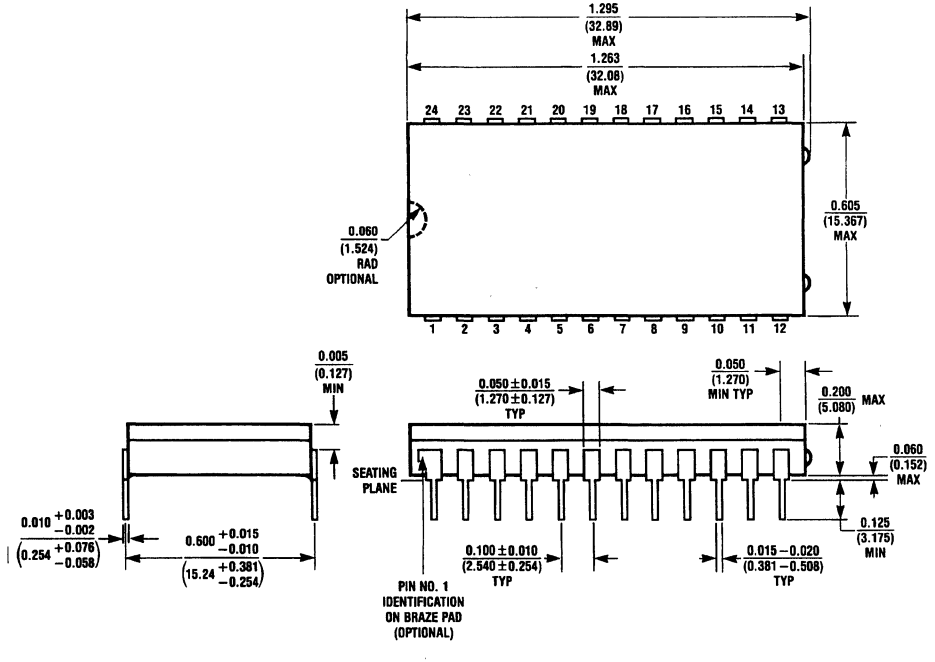
D16C (REV H)

16 Lead Hybrid Metal Can Dual-In-Line Package (D)
NS Package Number D16D



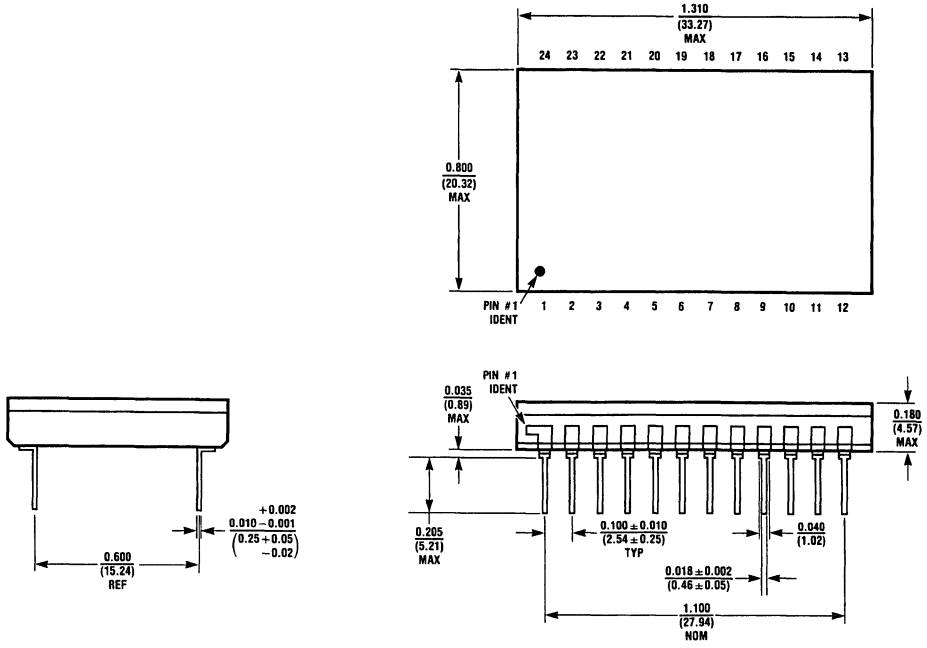
D16D (REV B)

24 Lead Hybrid Sidebrazed Dual-In-Line Package (D)
NS Package Number D24D



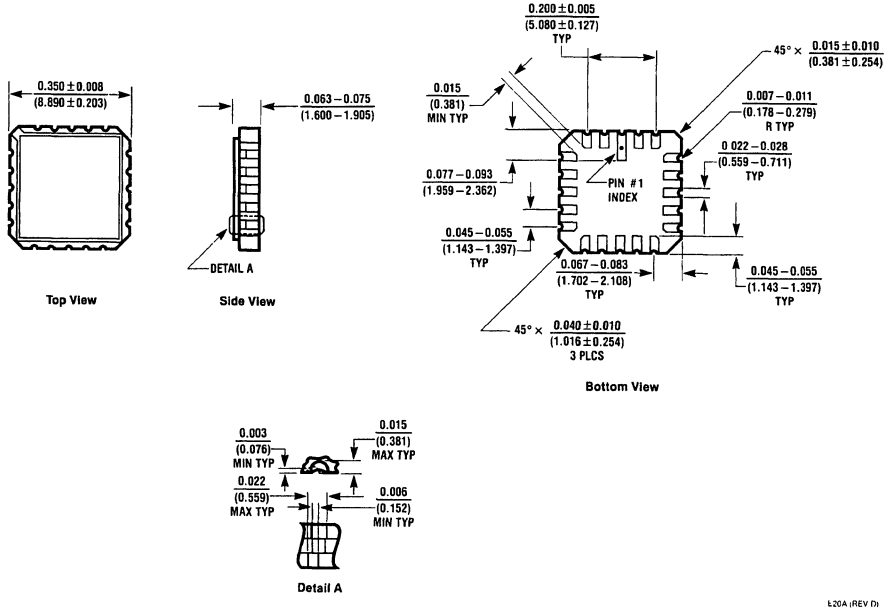
D24D (REV F)

24 Lead (Hybrid Bottom Brazed) Hermetic Dual-In-Line Package (D)
NS Package Number D24J



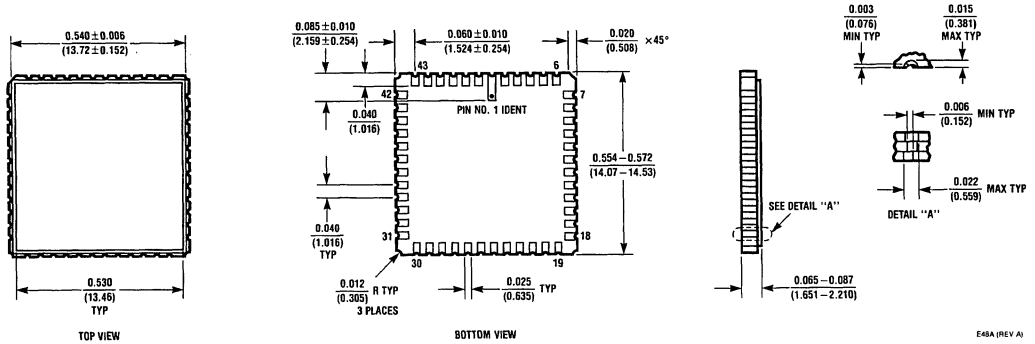
D24J (REV A)

20 Leadless Chip Carrier, Type C (E)
NS Package Number E20A

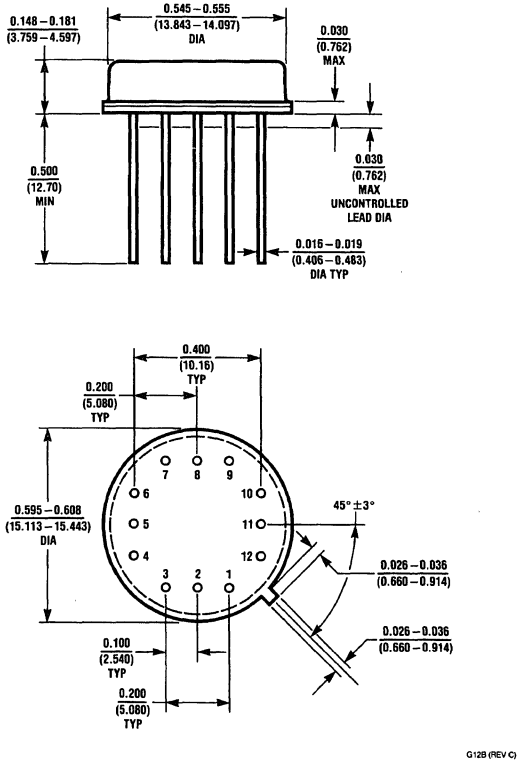


E20A (REV D)

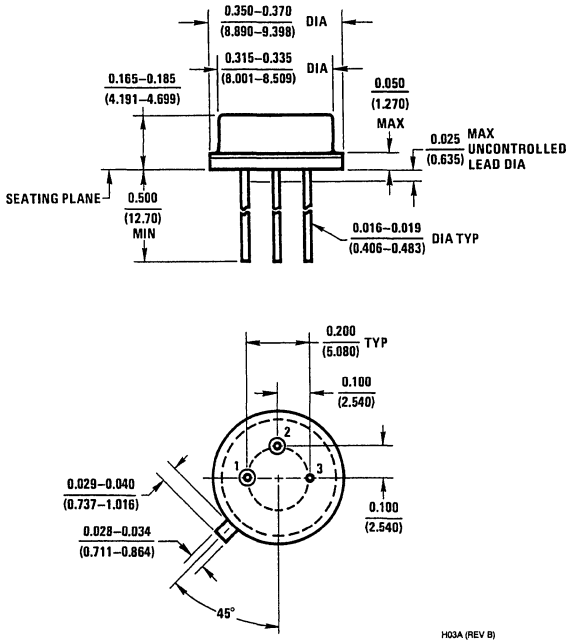
48 Pin Chip Carrier, Type C (E)
NS Package Number E48A



12 Lead (0.400" Square Pattern) Metal Can Package (G)
NS Package Number G12B

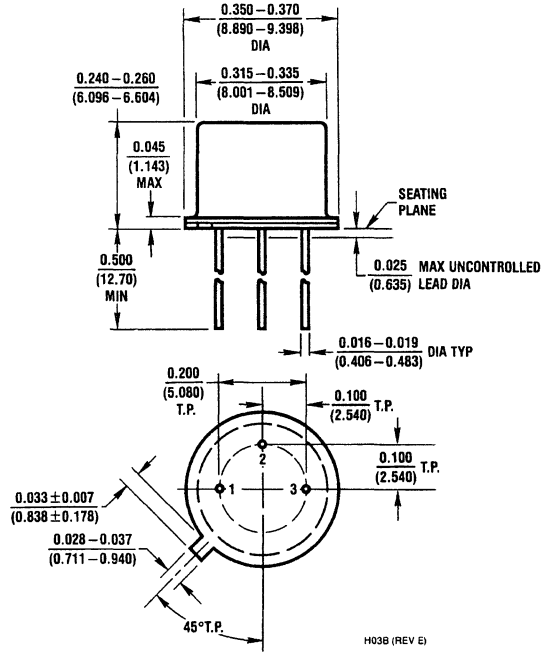


3 Lead (0.200″ Diameter P.C.) Metal Can Package (H)
NS Package Number H03A



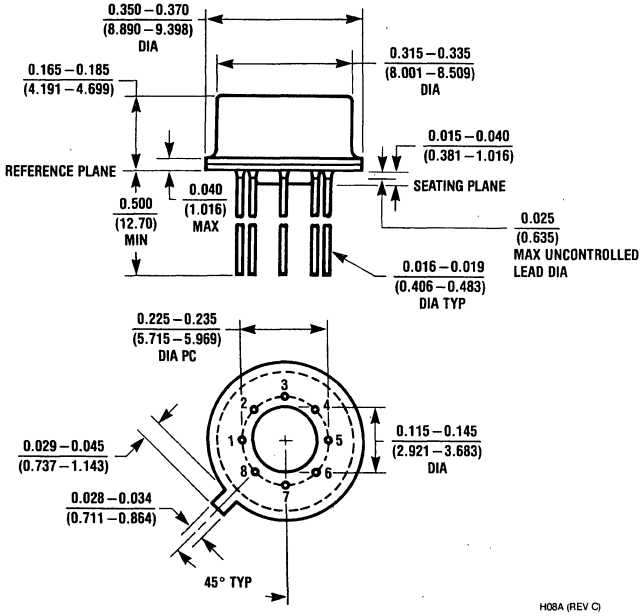
H03A (REV B)

3 Lead (0.200″ Diameter P.C.) TO-39 Metal Can Package (H)
NS Package Number H03B

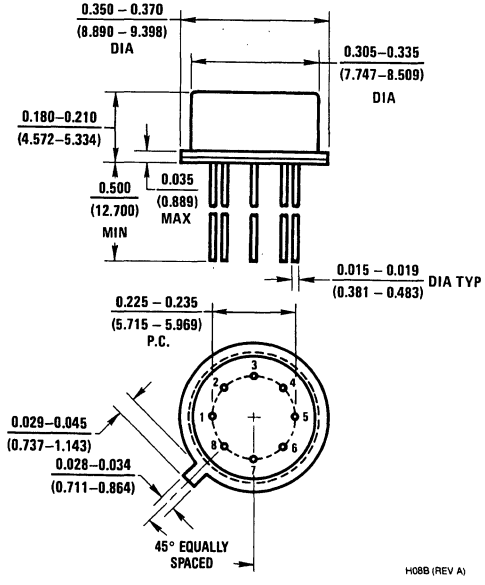


H03B (REV E)

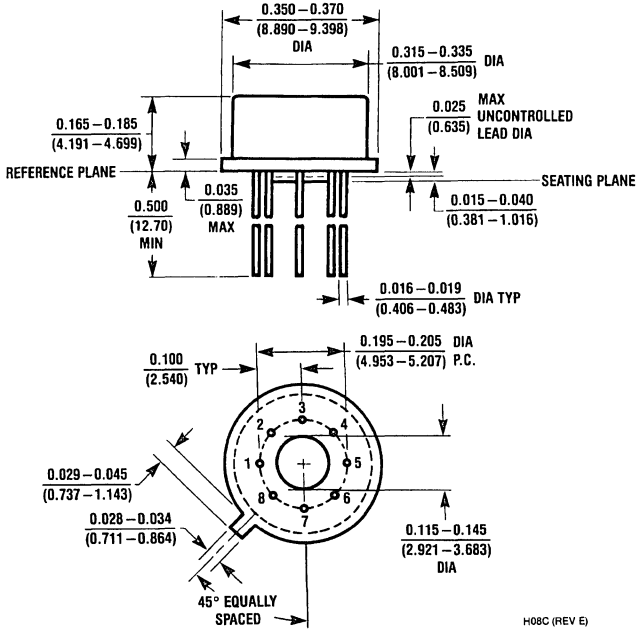
8 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H08A



8 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H08B

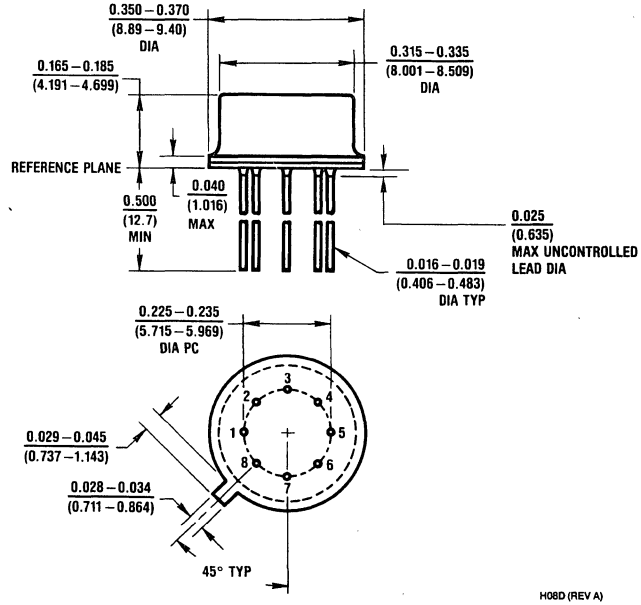


8 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package (H)
NS Package Number H08C



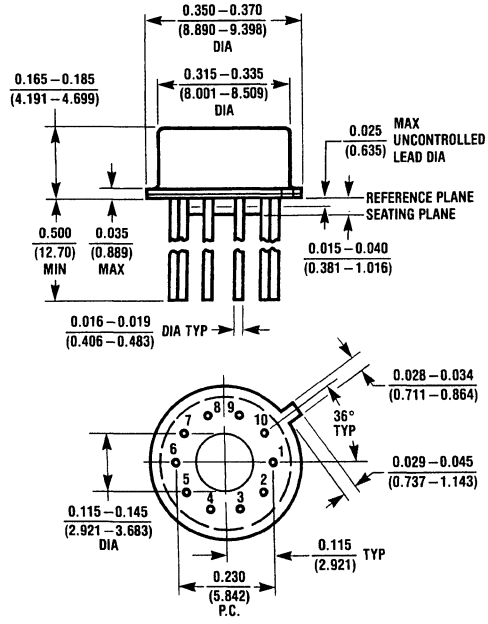
H08C (REV E)

8 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H08D



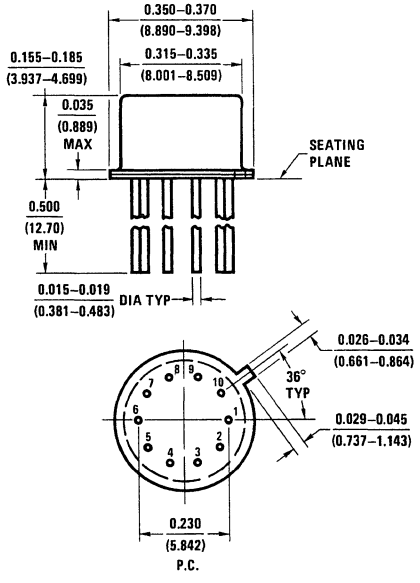
H08D (REV A)

10 Lead (0.230″ Diameter P.C.) TO-100 Metal Can Package (H)
NS Package Number H10C



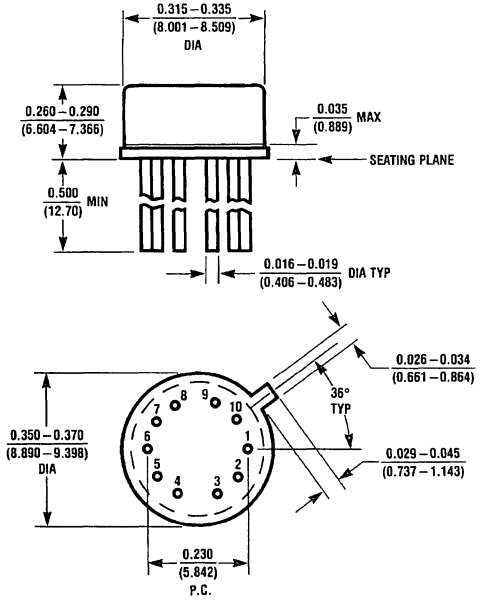
H10C (REV E)

10 Lead (0.230″ Diameter P.C.) Metal Can Package (H)
NS Package Number H10F



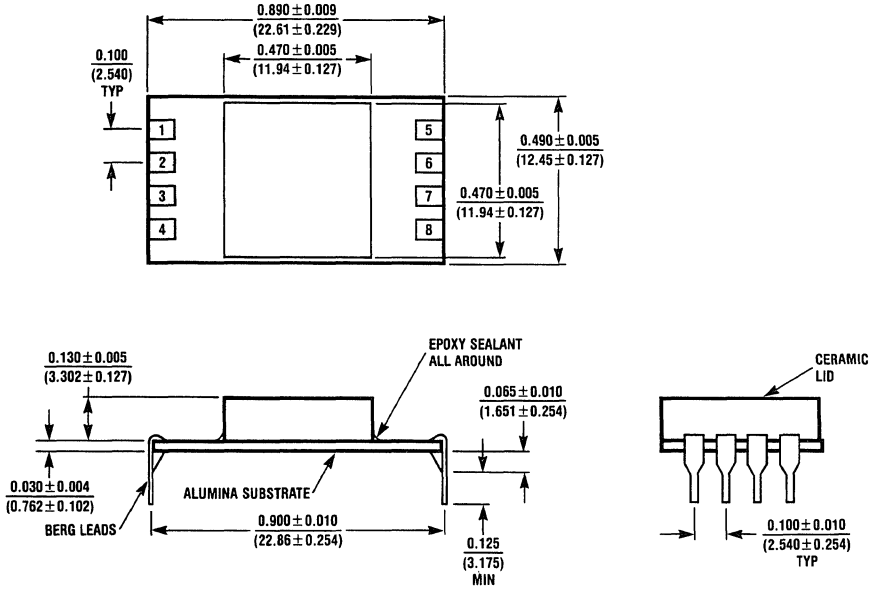
H10F (REV A)

10 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H10G



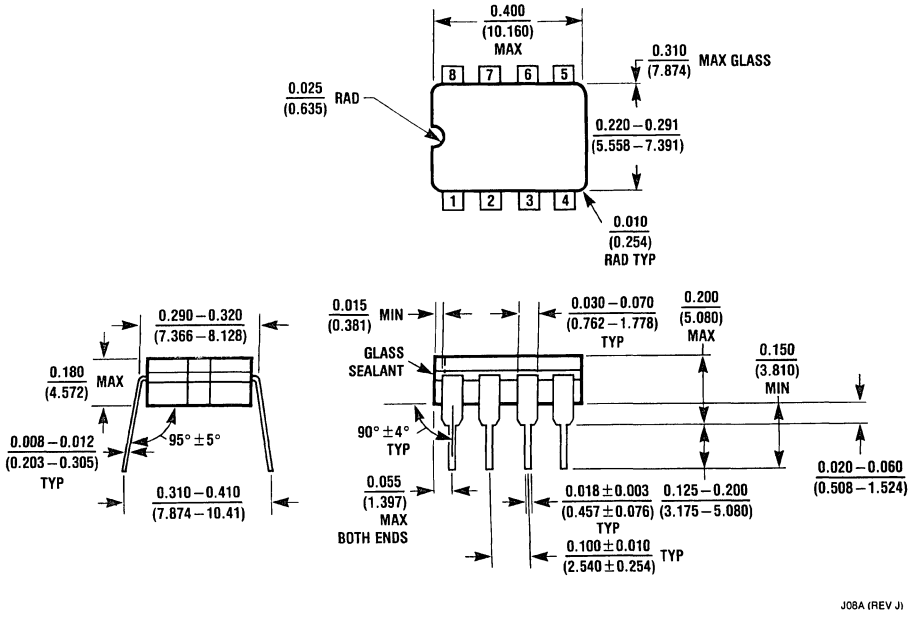
H10G (REV B)

8 Lead Dual-In-Line Hybrid Package (J)
NS Package Number HY08A



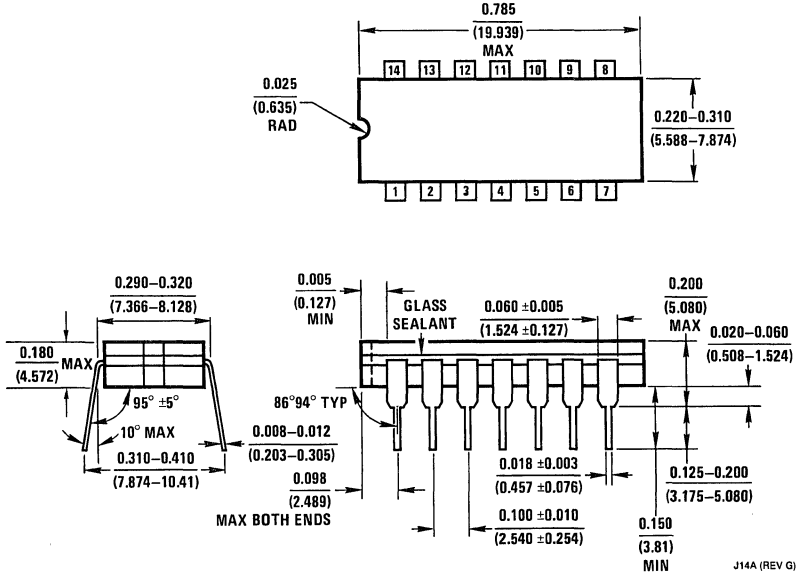
HY08A (REV B)

8 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J08A



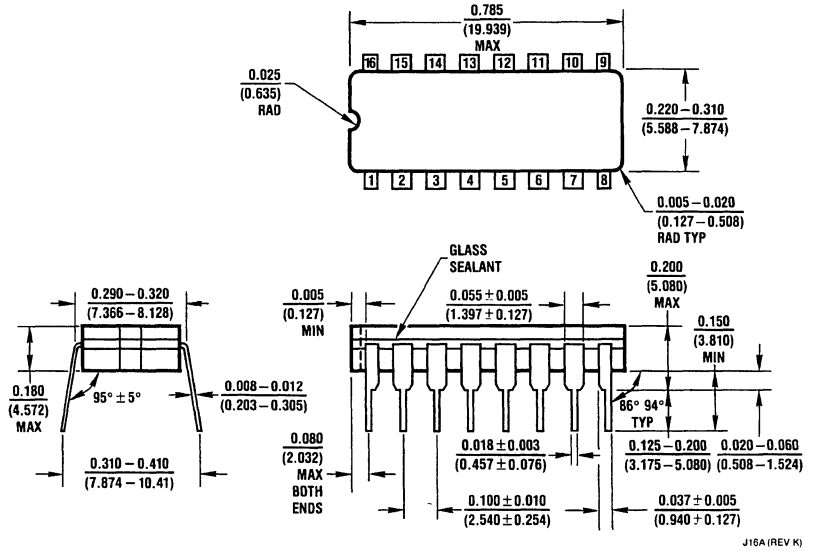
J08A (REV J)

14 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J14A



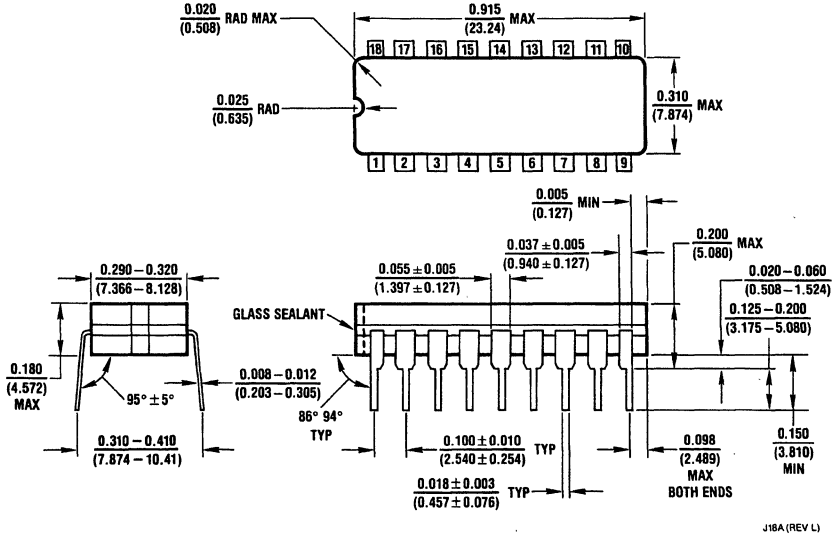
J14A (REV G)

16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



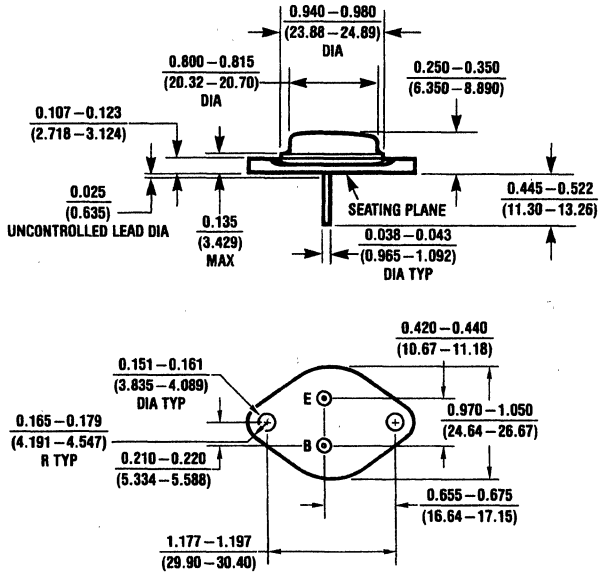
J16A (REV K)

18 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J18A



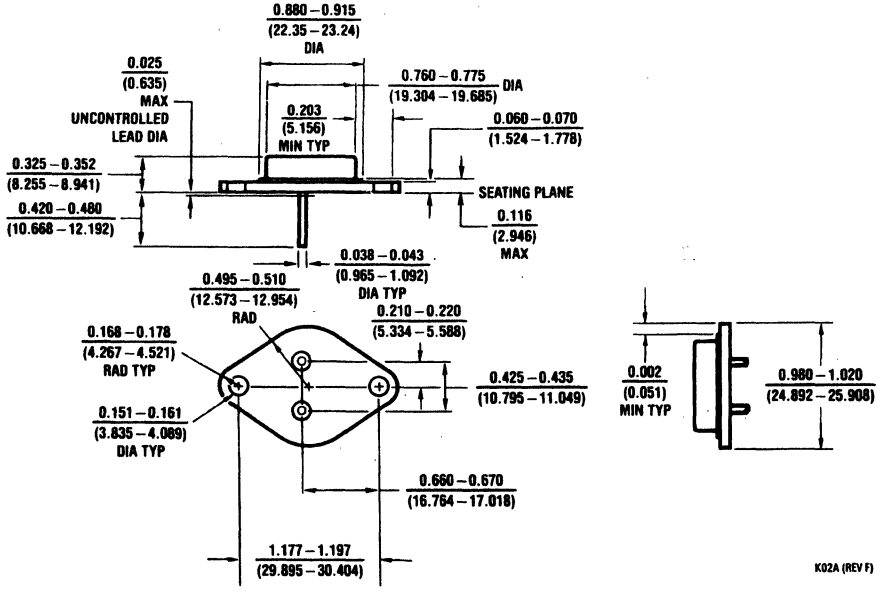
J18A (REV L)

2 Lead TO-3 Aluminum Metal Can Package (K or KC)
NS Package Number KC02A



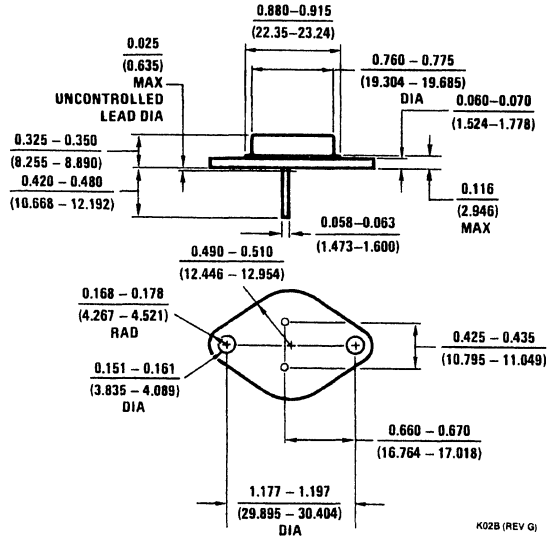
KC02A (REV C)

2 Lead TO-3 Metal Can Package (K)
NS Package Number K02A

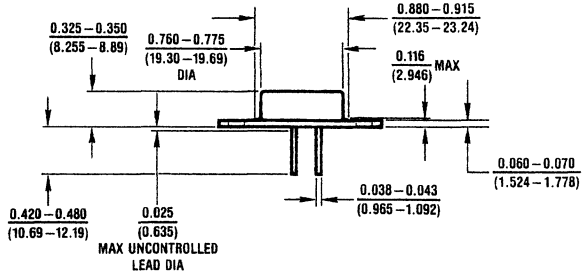


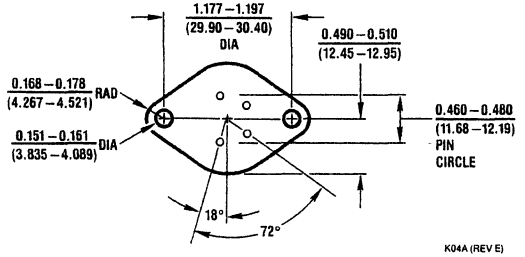
K02A (REV F)

2 Lead TO-3 Metal Can Package (K)
NS Package Number K02B

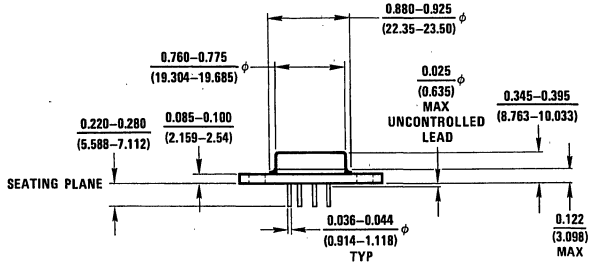


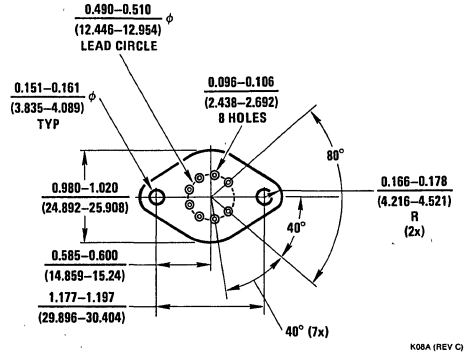
4 Lead TO-3 Metal Can Package (K)
NS Package Number K04A





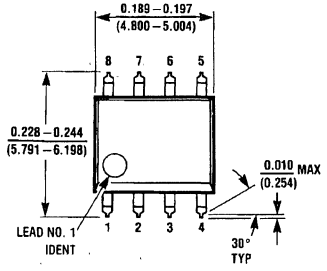
8 Lead TO-3 Metal Can Package (K)
NS Package Number K08A

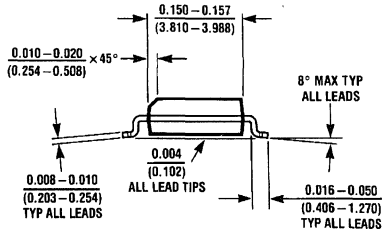


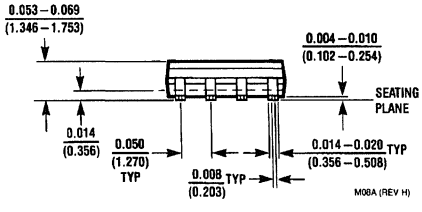


K08A (REV C)

8 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M08A

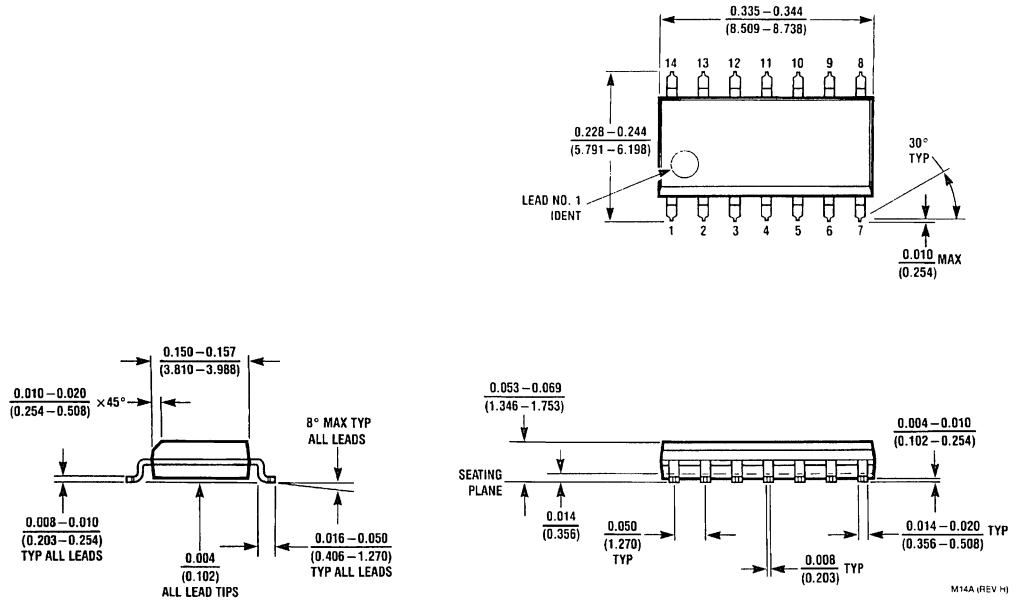




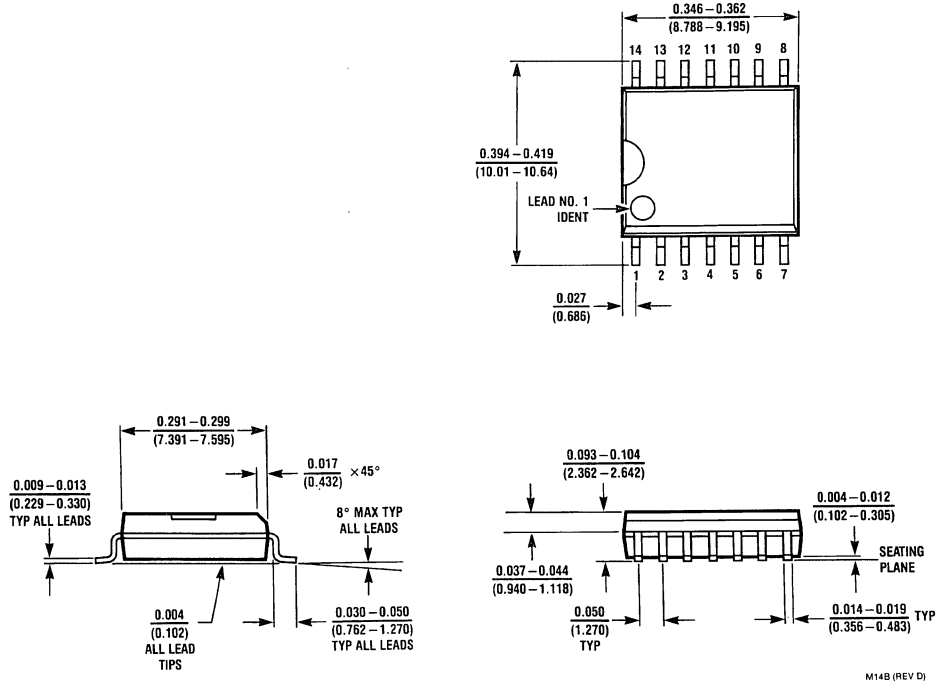


M08A (REV H)

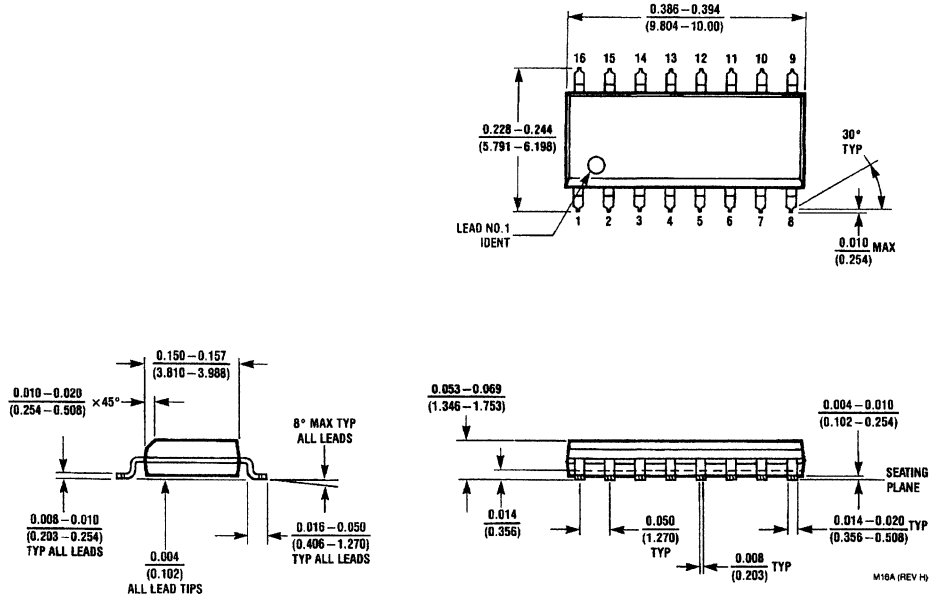
14 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M14A



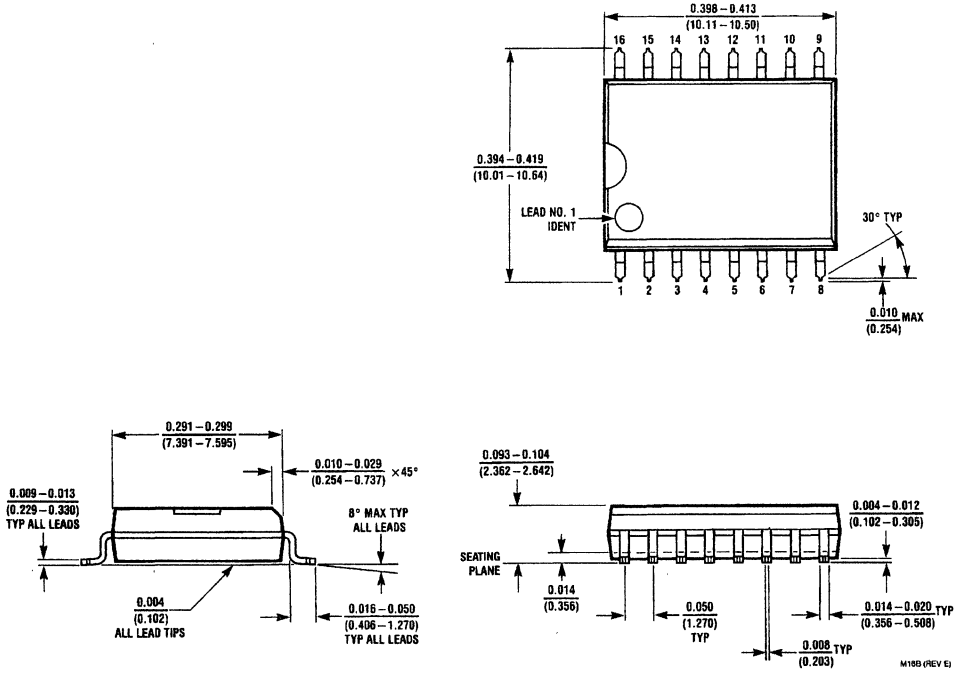
14 Lead (0.300" Wide) Small Outline Molded Package (WM)
NS Package Number M14B



16 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M16A



16 Lead (0.300" Wide) Small Outline Molded Package (WM)
NS Package Number M16B



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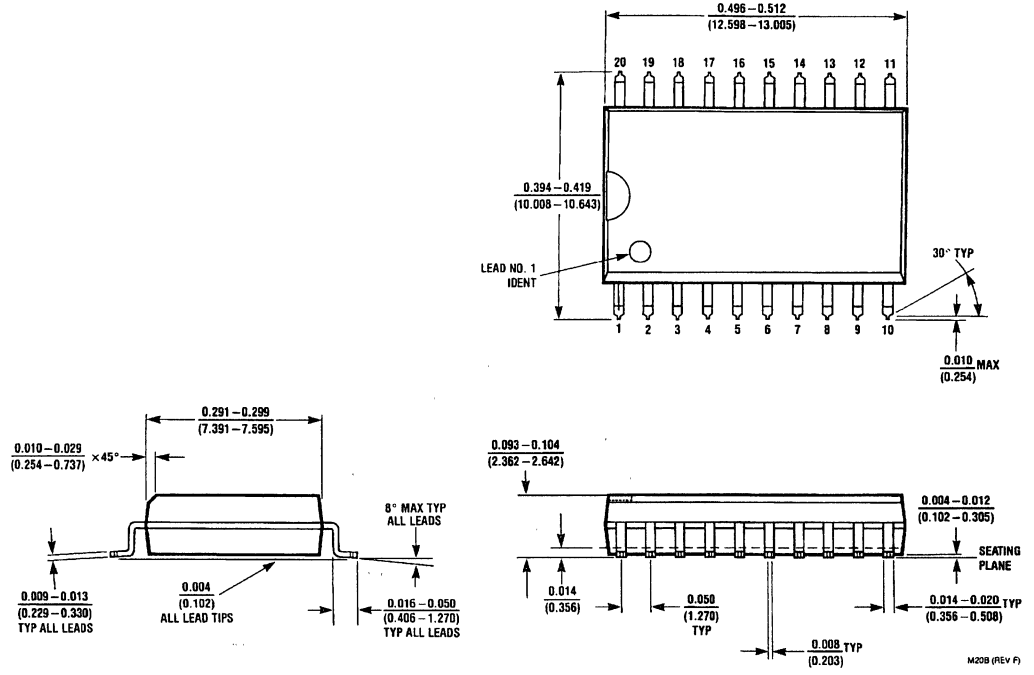
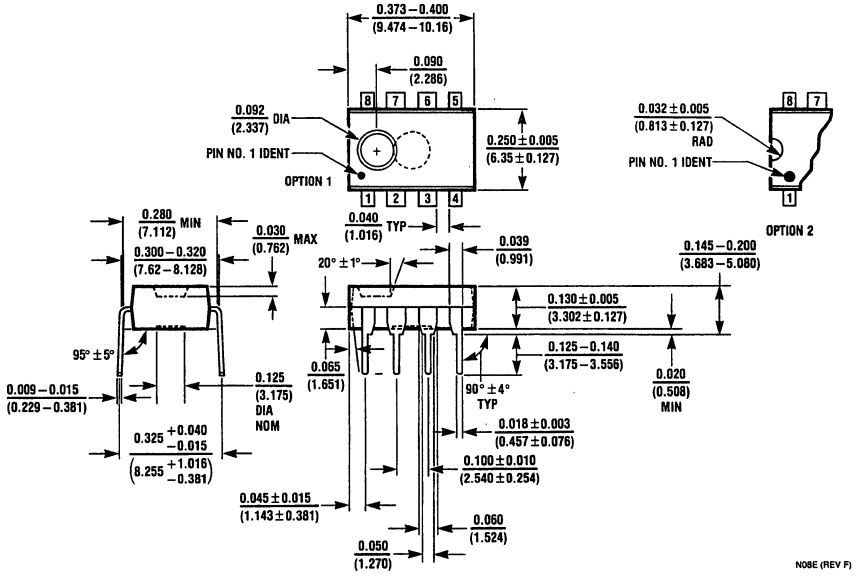
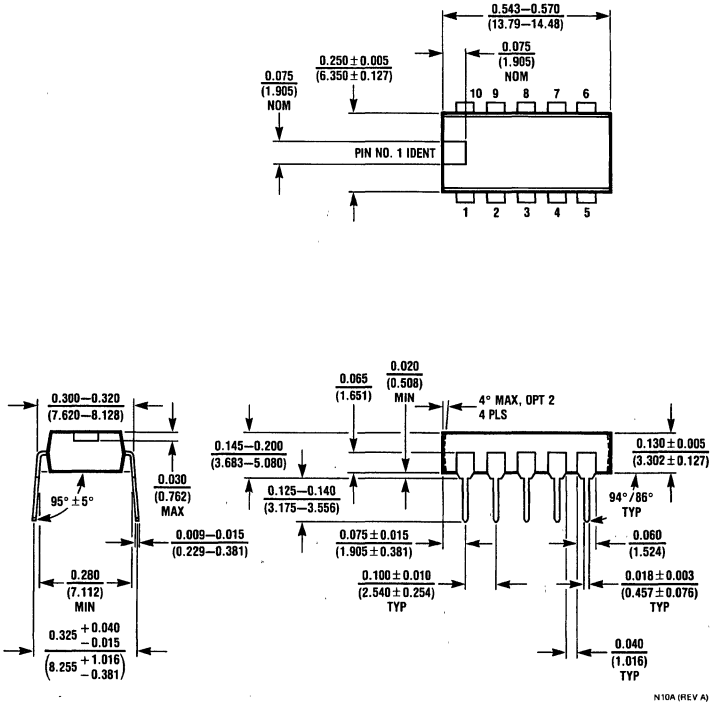
NS Package Number M20B



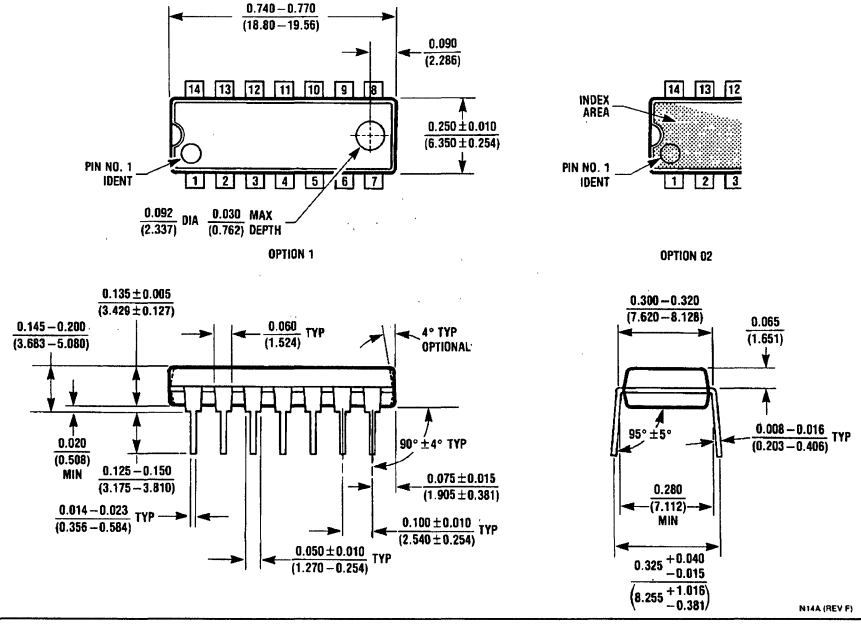
8 Lead Molded Dual-In-Line Package (N)
NS Package Number N08E



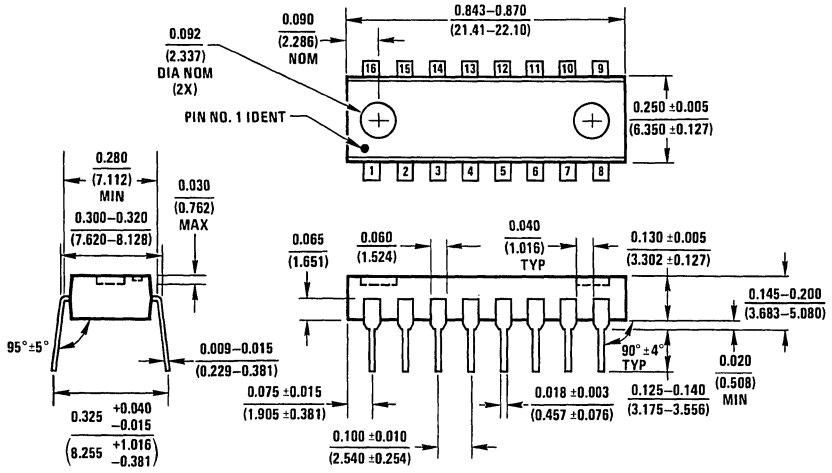
10 Lead Molded Dual-In-Line Package (N)
NS Package Number N10A



14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A

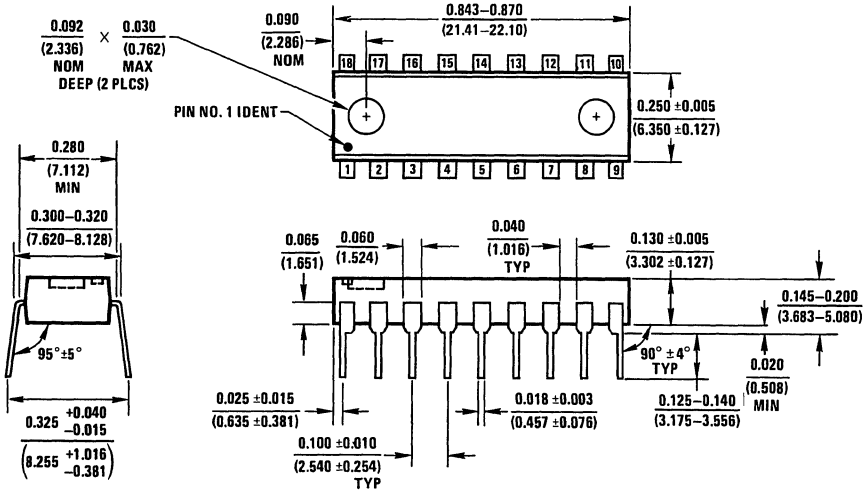


16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A



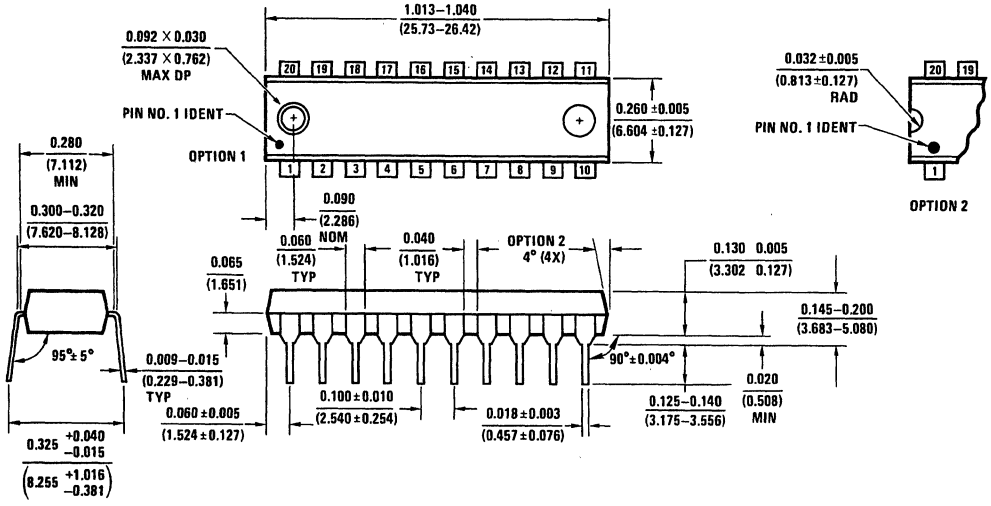
N16A (REV E)

18 Lead Molded Dual-In-Line Package (N)
NS Package Number N18A



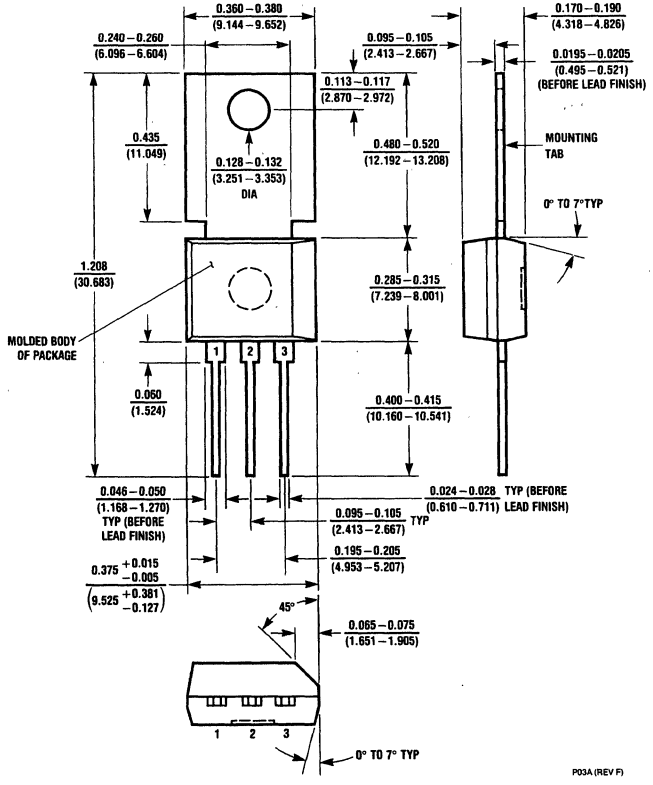
N18A (REV E)

20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A



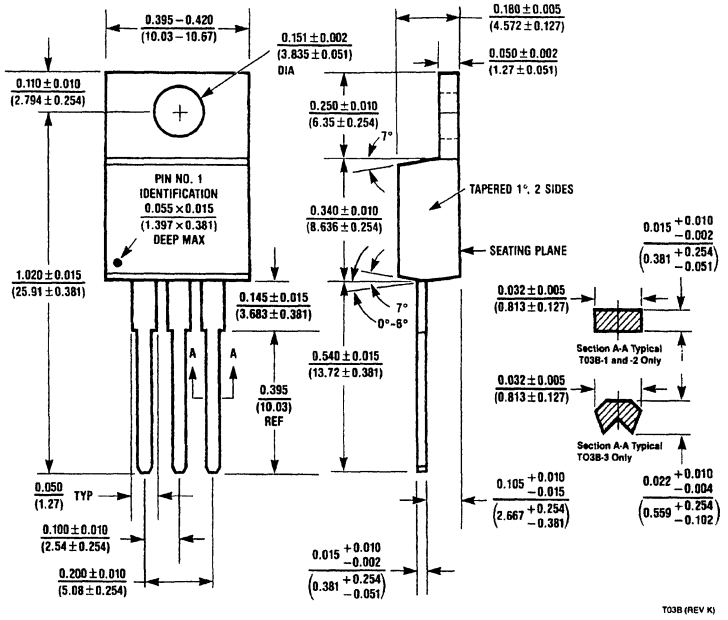
N20A (REV G)

3 Lead TO-202 Molded Package (P)
NS Package Number P03A

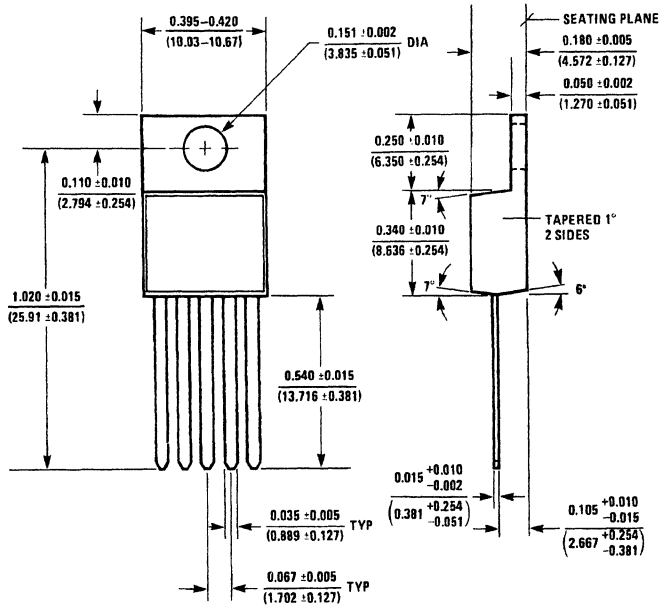


P03A (REV F)

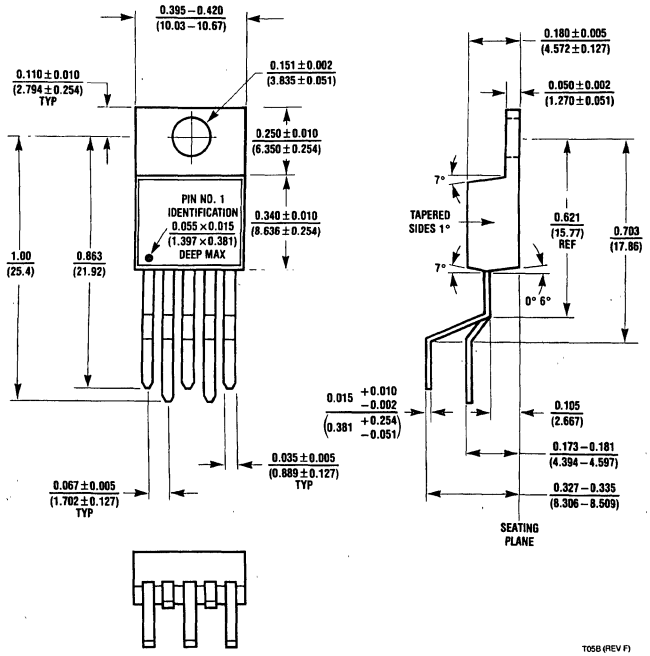
3 Lead TO-220 Molded Package (T)
NS Package Number T03B



5 Lead TO-220 Molded Package (T)
NS Package Number T05A

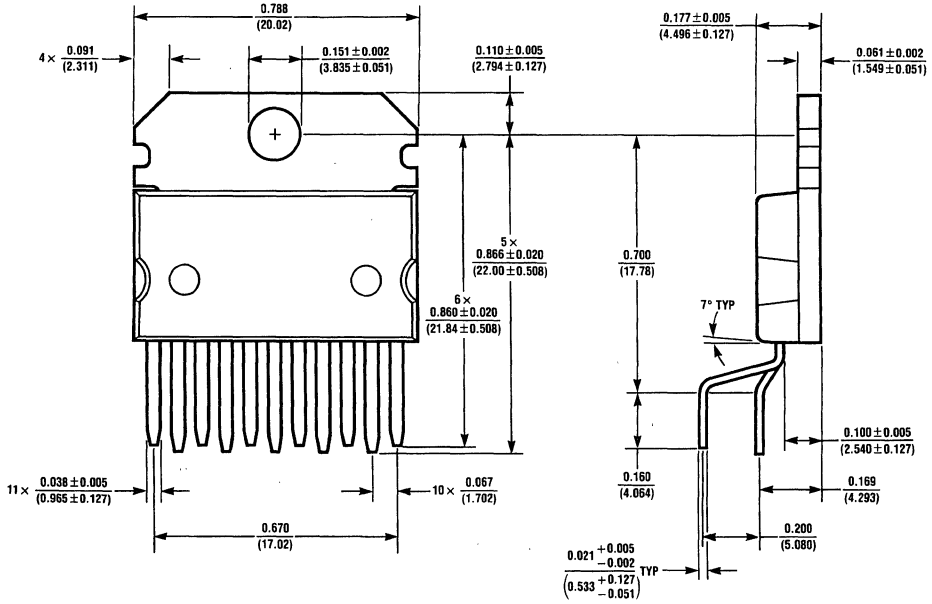


5 Lead TO-220 Molded Package (T)
NS Package Number T05B



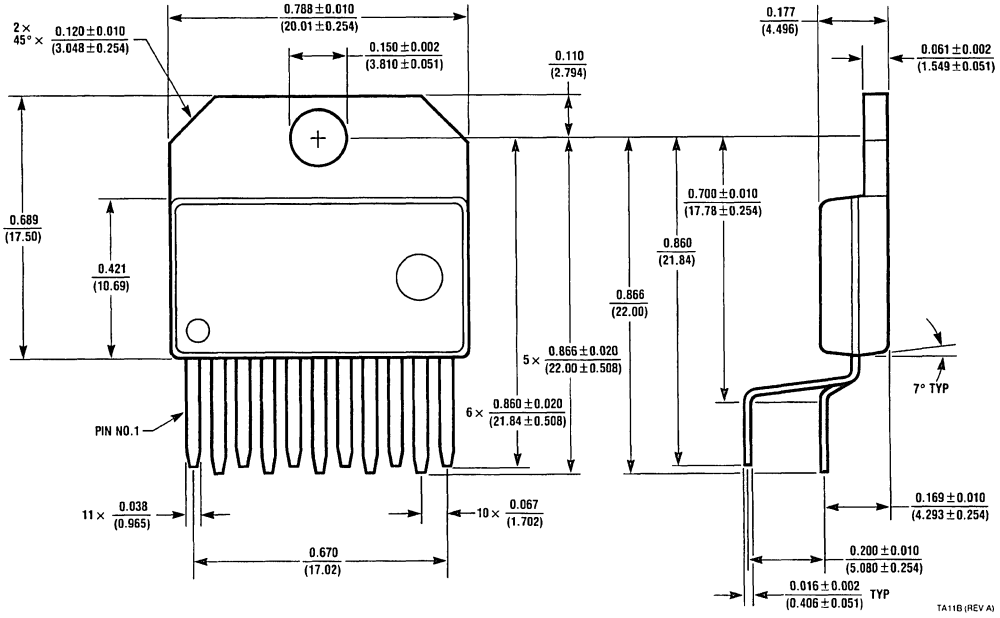
T05B (REV F)

11 Lead TO-220 Molded Package (T)
NS Package Number TA11A

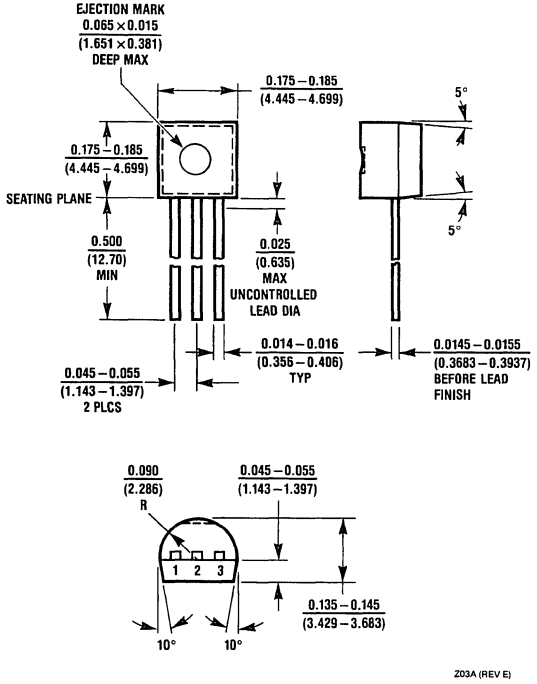


TA11A (REV C)

11 Lead TO-220 Molded Package (T)
NS Package Number TA11B



3 Lead TO-92 Molded Package (Z)
NS Package Number Z03A



NOTES

NOTES

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