National Semiconductor

400088 Rev. 1

Memory Databook

- *PROMs, EPROMs, EEPROMs*
- *Flash EPROMs and EEPROMs*
- *TTL I/O SRAMs*
- *ECL I/O SRAMs*
- *ECL I/O Memory Modules*

A Corporate Dedication to Quality and Reliability

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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisànt des systèmes d'une très grande qualité standard.

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National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

MEMORY
DATABOOK

1988 Edition

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Memory Databook Introduction

National Semiconductor's Memory Databook is a comprehensive collection of information on advanced memory products intended to meet the needs of virtually every electronic system being designed today. National Semiconductor is committed to designing and supplying high performance memory products ranging from state-of-the-art static RAMs to programmable non-volatile EPROMs and EEPROMs.

National Semiconductor has an array of advanced technology processes to apply to memory design and development. These range from our unparalleled BiCMOS process used for the industry's most advanced line of high density ECL I/O SRAMs, to our small geometry, silicon gate, oxide isolated CMOS technology which is now producing unsurpassed, high performance EPROM and EEPROM non-volatile memory devices.

Concurrent with production of these leading edge memory devices is the development of an industry leading FLASH™ EPROM and FLASH EEPROM technology and family of devices designed to be the standard bearers for the next generation of non-volatile memory devices.

National Semiconductor is committed to excellence in design, manufacturing, reliability, and service to our customers through the continuing development of new products and technologies. As new information and devices become available, individual new data sheets will be issued. For the most current information, please contact your local National Semiconductor sales office or Distributor.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Section 1

CMOS EPROMs

Section 1 Contents

National Semiconductor

CMOS EPROMs Non-Volatile Memory Selection Guide

CMOS EPROMs and OTP PROMs

Part No.	Org.	Size	No. of Pins	Access Time	Prog. Volt.	PS Tol.	Temp. Range
NMC27C16Q	2k x 8	16k	24	300, 350, 450, 550	25	5%	0°C to +70°C
NMC27C16QE	2k x 8	16k	24	450	25	5%	−40°C to +85°C
NMC27C32Q	4k x 8	32k	24	300, 350, 450, 550	25	5%	0°C to +70°C
NMC27C32QE	4k x 8	32k	24	450	25	5%	−40°C to +85°C
NMC27C32BQ	4k x 8	32k	24	120, 150, 200, 250	13	10%	0°C to +70°C
NMC27C32BQE	4k x 8	32k	24	200, 250	13	10%	−40°C to +85°C
NMC27C64Q	8k x 8	64k	28	150	13	5%	0°C to +70°C
NMC27C64Q/N	8k x 8	64k	28	150, 200, 250, 300	13	10%	0°C to +70°C
NMC27C64QE	8k x 8	64k	28	150, 200	13	10%	−40°C to +85°C
NMC27C64QM	8k x 8	64k	28	200, 250	13	10%	−55°C to +125°C
NMC27C64BQ/BN	8k x 8	64k	28	120, 150, 200, 250	13	10%	0°C to +70°C
NMC27C64BQE	8k x 8	64k	28	120, 150, 200	13	10%	−40°C to +85°C
NMC27C64BQM	8k x 8	64k	28	150, 200	13	10%	−55°C to +125°C
NMC27CP128Q	16k x 8	128k	28	200, 250, 300	13	10%	0°C to +70°C
NMC27C128BQ/BN	16k x 8	128k	28	120, 150, 200, 250	13	10%	0°C to +70°C
NMC27C128BQE	16k x 8	128k	28	120, 150, 200	13	10%	−40°C to +85°C
NMC27C128QM	16k x 8	128k	28	150, 200	13	10%	−55°C to +125°C
NMC27C128C	16k x 8	128k	28	45, 55, 70	13	10%	0°C to +70°C
NMC27C256Q	32k x 8	256k	28	170, 200, 250	13	5%	0°C to +70°C
NMC27C256Q	32k x 8	256k	28	200, 250, 300	13	10%	0°C to +70°C
NMC27C256QE	32k x 8	256k	28	200, 250	13	10%	−40°C to +85°C
NMC27C256QM	32k x 8	256k	28	250, 350	13	10%	−55°C to +125°C
NMC27C256BQ/BN	32k x 8	256k	28	120, 150, 200, 250	13	10%	0°C to +70°C
NMC27C256BQE	32k x 8	256k	28	120, 150, 200	13	10%	−40°C to +85°C
NMC27C256BQM	32k x 8	256k	28	150, 200	13	10%	−55°C to +125°C
NMC27C256CQ	32k x 8	256k	28	55, 70, 90	13	10%	0°C to +70°C

CMOS EPROMs and OTP PROMs (Continued)

Part No.	Org.	Size	No. of Pins	Access Time	Prog. Volt.	PS Tol.	Temp Range
NMC27C512AQ/AN	64k x 8	512k	28	120, 150, 200, 250	13	10%	0°C to +70°C
NMC27C512AQE	64k x 8	512k	28	120, 150, 200	13	10%	−40°C to +85°C
NMC27C512AQM	64k x 8	512k	28	150, 200	13	10%	−55°C to +125°C
NMC27C010Q	128k x 8	1024k	32	150, 170, 200, 250	13	10%	0°C to +70°C
NMC27C010QE	128k x 8	1024k	32	150, 170, 200	13	10%	−40°C to +85°C
NMC27C010QM	128k x 8	1024k	32	170, 200	13	10%	−55°C to +125°C
NMC27C1024Q	64k x 16	1024k	40	150, 170, 200, 250	13	10%	0°C to +70°C
NMC27C1024QE	64k x 16	1024k	40	150, 170, 200	13	10%	−40°C to +85°C
NMC27C1024QM	64k x 16	1024k	40	170, 200	13	10%	−55°C to +125°C
NMC27C020Q	256k x 8	2048k	32	150, 170, 200, 250	13	10%	0°C to +70°C
NMC27C020QE	256k x 8	2048k	32	150, 170, 200	13	10%	−40°C to +85°C
NMC27C020QM	256k x 8	2048k	32	170, 200	13	10%	−55°C to +125°C
NMC27C2048Q	128k x 16	2048k	40	150, 170, 200, 250	13	10%	0°C to +70°C
NMC27C2048QE	128k x 16	2048k	40	150, 170, 200	13	10%	−40°C to +85°C
NMC27C2048QM	128k x 16	2048k	40	170, 200	13	10%	−55°C to +125°C
CMOS FLASH EEPROMs							
NMC48F512N	64k x 8	512k	32	200, 250, 300	12	10%	0°C to +70°C
NMC48F512NE	64k x 8	512k	32	250, 300	12	10%	−40°C to +85°C
NMC48F512QNM	64k x 8	512k	32	300	12	10%	−55°C to +125°C

National Semiconductor

PRELIMINARY

One-Time-Programmable EPROMs

National Semiconductor plans to introduce the following EPROMs in a plastic One-Time-Programmable package in 1988:

NMC27C32BN
NMC27C64N
NMC27C64BN
NMC27C256BN
NMC27C512AN

The One-Time-Programmable EPROM, or OTP, is an EPROM packaged in a molded plastic package without a quartz window. This part is particularly advantageous for users of the EPROM who are in high volume production, as opposed to those who use it for pattern experimentation and proto-typing. National can produce the OTP very economically because neither a quartz window nor a hermetically sealed package is required.

Since the OTP does not have a quartz window to expose the chip to UV light, the device cannot be erased. It therefore can only be programmed once by the user.

The plastic OTP EPROM has the additional advantage as a production part that it works well in automatic insertion equipment.

National Semiconductor has earned an excellent reputation in the industry for product reliability. The OTP EPROM will be produced with the same stringent reliability standards as other National products.

Surface Mount Packaging

National Semiconductor plans to produce CMOS PROMs in plastic surface mount package. This package will give users the advantages of molded packages and will also be significantly smaller than dual-in-line packages.

The plastic surface mount package does not have a quartz window and it is not hermetically sealed, so it can be produced very economically. It is therefore advantageous for cost sensitive, high volume users who have no need to erase and reprogram.

System designers can use surface mount packages to optimize their PC board density. Surface mount packages differ from dual-in-line packages in that lead spacings are 0.050" instead of 0.100", and the leads bond to the surface of the board as opposed to through-hole mounting. The tighter lead spacings allow a three-to-one improvement in component mounting density. Surface mounting also allows system designers to place components on both sides of the PC board.

National Semiconductor has had many years of experience building surface mount packages. The company has an excellent reputation in the industry for product reliability and the surface mount CMOS PROMs will be built with the same stringent reliability standards as other National products.

National Semiconductor

NMC27C16
16,384-Bit (2048 x 8) UV Erasable CMOS PROM

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

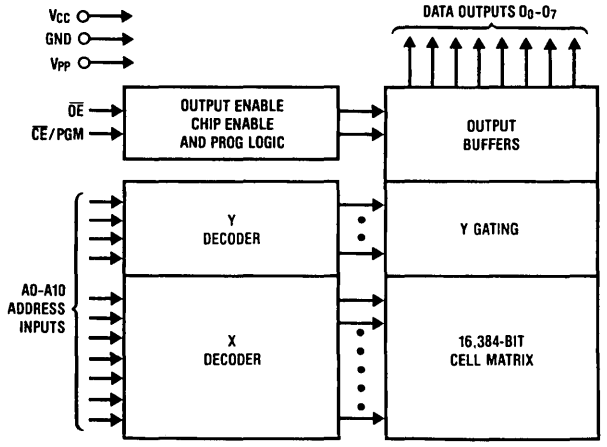
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

Features

- Access time down to 300 ns
- Low CMOS power consumption
  - — Active Power: 26.25 mW max
  - — Standby Power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C16E-45), −40°C to +85°C, 450 ns ±5% power supply
- Pin compatible to MM2716 and higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block Diagram



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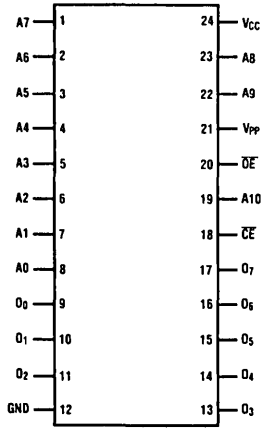
Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package
NMC27C16



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Top View

27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16 pins.

Order Number NMC27C16
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C16-30	300
NMC27C16-35	350
NMC27C16-45	450
NMC27C16-55	550

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground (Note 11)	V_{CC} +0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	
NMC27C16-30, -35, -45, -55	0°C to +70°C
NMC27C16E-45	−40°C to +85°C
V_{CC} Power Supply (Notes 2 and 3)	5V ±5%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		2	10	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16								Units
			-30		-35		E-45, -45		-55		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300		350		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300		350		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120		120		120		160	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

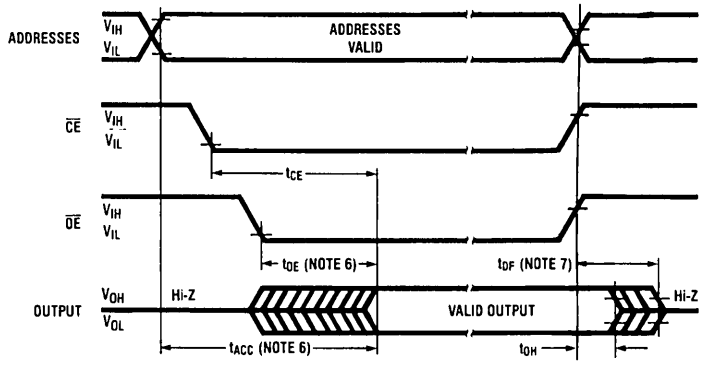
Capacitance $T_A = +25°C, f = 1$ MHz (Note 5)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 2, 8, 9, 10)



TL/D/5275–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Note 11: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 & 3)

(T_A = +25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V

AC Programming Characteristics (Notes 2 & 3)

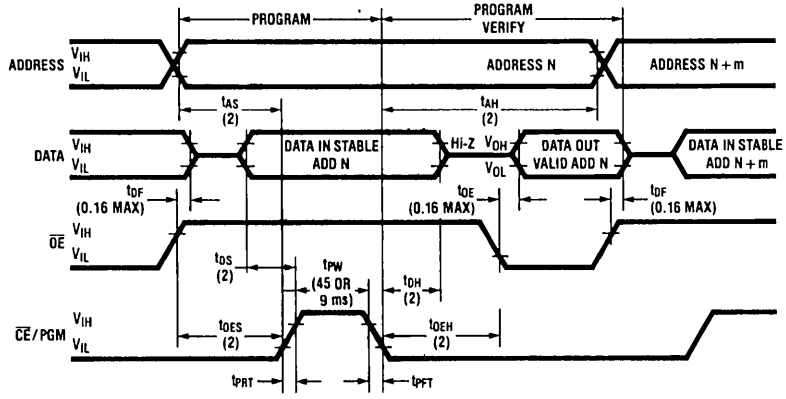
(T_A = +25°C ±5°C, V_{CC} = 5V ±5%, V_{PP} = 25V ±1V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

AC Test Conditions

V_{CC}	5V ±5%
V_{PP}	25V ±1V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3) V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C16 must not be inserted into or removed from a board with V_{PP} at 25V ±1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C16 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The NMC27C16 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Standby Mode

The NMC27C16 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C16 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the NMC27C16.

Initially, and after each erasure, all bits of the NMC27C16 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The NMC27C16 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Functional Description (Continued)

Programming multiple NMC27C16s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled NMC27C16s.

Program Inhibit

Programming multiple NMC27C16s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel NMC27C16s may be common. A TTL level program pulse applied to an NMC27C16's $\overline{CE}$/PGM input with V_{PP} at 25V will program that NMC27C16. A low level $\overline{CE}$/PGM input inhibits the other NMC27C16 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the NMC27C16 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C16 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The NMC27C16-55 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_P (21)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z
Output Disable	X	V_{IH}	V_{CC}	5	Hi-Z

National Semiconductor

NMC27C32
32,768-Bit (4096 x 8) UV Erasable CMOS PROM

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

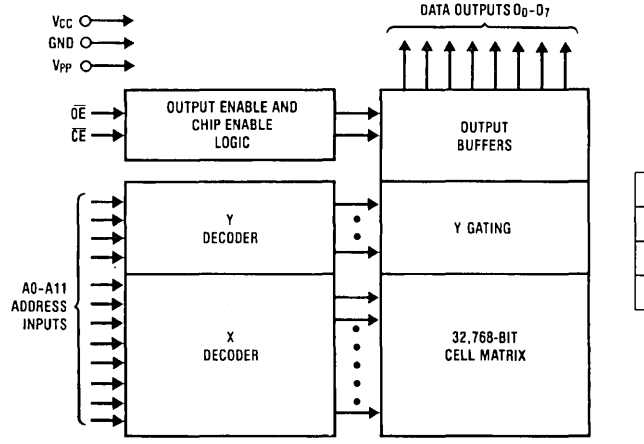
The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, p^2CMOS™ silicon gate technology.

Features

- Access time down to 300 ns
- Low CMOS power consumption
  - Active power: 26.25 mW max
  - Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C32E-45 and NMC27C32HE-45), −40°C to +85°C, 450 ns ±5% power supply
- 10 ms programming available (NMC27C32H), an 80% time savings
- Pin compatible to NMC2732 and higher density EPROMs
- Static-no clocks required
- TTL compatible inputs/ outputs
- Two-line control
- TRI-STATE® output

Block Diagram



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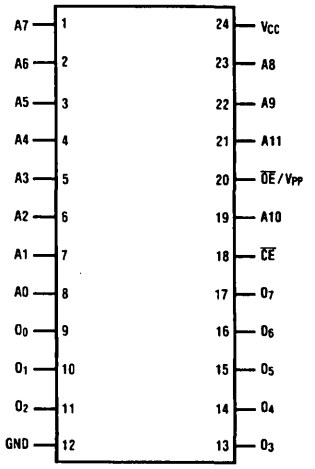
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32
Dual-In-Line Package



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Top View

Order Number NMC27C32
See NS Package Number J24AQ

27C216 27216	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32 pins.

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32-30, NMC27C32H-30	300
NMC27C32-35, NMC27C32H-35	350
NMC27C32-45, NMC27C32H-45	450
NMC27C32-55, NMC27C32H-55	550

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C32E-45, NMC27C32EH-45	450

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground during Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C32-30, NMC27C32-35, NMC27C32-45, NMC27C32-55, NMC27C32H-30, NMC27C32H-35, NMC27C32H-45, NMC27C32H-55	0°C to +70°C
NMC27C32HE-45, NMC27C32E-45	−40°C to +85°C
V_{CC} Power Supply	5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{CC} or GND, f = 1 MHz I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32								Units
			-30, H-30		-35, H-35		-45, H-45 E-45; HE-45		-55, H-55		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300		350		450		550	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300		350		450		550	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		150		150		150		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	130	0	130	0	130	0	130	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

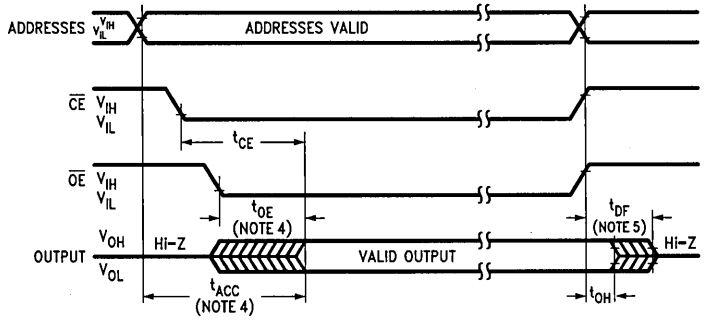
Capacitance $T_A = +25°C, f = 1$ MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF	Timing Measurement Reference Level	
		Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6 & 8)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING (Note 1)

DC Programming Characteristics

T_A = +25°C ±5°C, V_{CC} = 5V ± 5%, V_{PP} = 25V ±1V (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{CC}$ or GND			10	μA
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 μA	2.4			V
I_{CC}	V_{CC} Supply Current			2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level (All Inputs except $\overline{OE}/V_{PP}$)		2.0		V_{CC} + 1	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA

AC Programming Characteristics T_A = +25°C ±5°C, V_{CC} = 5V ± 5%, V_{PP} = 25V ±1V

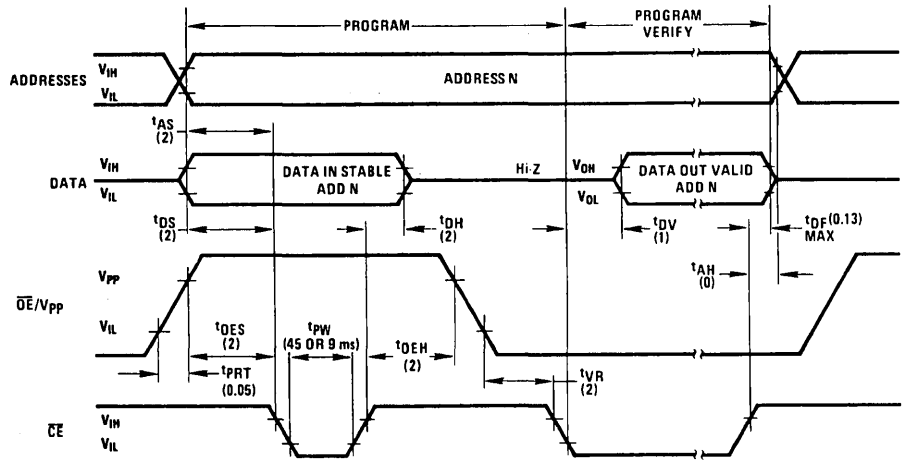
Symbol	Parameter	Conditions	NMC27C32			NMC27C32H			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Setup Time		2			2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			2			μs
t_{DS}	Data Setup Time		2			2			μs
t_{AH}	Address Hold Time		0			0			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	0		130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1			1	μs
t_{PW}	$\overline{CE}$ Pulse Width during Programming		45	50	55	9	10	11	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			50			ns
t_{VR}	V_{PP} Recovery Time		2			2			μs

AC Test Conditions

V_{CC}	5V ± 5%
V_{PP}	25V ± 1V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified..
The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must not be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description (Continued)

DEVICE OPERATION

The 6 modes of operation of the NMC27C32 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The NMC27C32 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC27C32 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C32 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the NMC27C32.

Initially, and after each erasure, all bits of the NMC27C32 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

Functional Description (Continued)

The NMC27C32 is in the programming mode when the $\overline{OE}$/V_{PP} input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}$/V_{PP}, V_{CC}, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C32H devices) active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C32H devices). The NMC27C32 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple NMC27C32s in parallel with the same data can easily be accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32s.

Program Inhibit

Programming multiple NMC27C32s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C32s may be common. A TTL level program pulse applied to an NMC27C32's $\overline{CE}$ input with $\overline{OE}$/V_{PP} at 25V will program that NMC27C32. A high level $\overline{CE}$ input inhibits the other NMC27C32s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}$/V_{PP} and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32 is exprosure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C32 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The NMC27C32-55 and NMC27C32H-55 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}$/V_{PP} (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Output Disable	Don't Care	V_{IH}	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

National Semiconductor

PRELIMINARY

NMC27C32B 32,768-Bit (4k x 8) High Speed Version UV Erasable CMOS PROM

General Description

The NMC27C32B is a high-speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over the Extended Temperature Range.

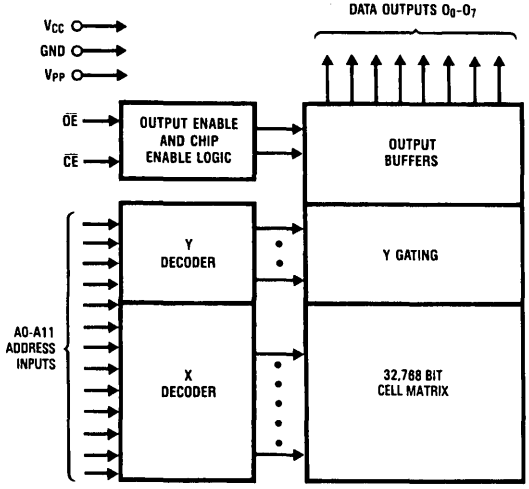
The NMC27C32B is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power 110 mW Max
  - — Standby Power 0.55 mW Max
- Optimal EPROM for total CMOS systems
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C32BQE), −40°C to +85°C, available
- Pin compatible with NMOS 32k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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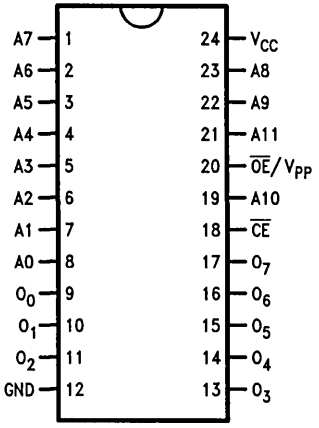
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/ Programming Voltage
O_0–O_7	Outputs

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

NMC27C32B
Dual-In-Line Package



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27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
V_{PP}	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pins.

Order Number NMC27C32BQ
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ120	120
NMC27C32BQ150	150
NMC27C32BQ200	200
NMC27C32BQ250	250

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200
NMC27C32BQE250	250

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Extended Temp Parts	Operating Temp
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}$ V_{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ120, 150, 200, 250	0°C to +70°C
NMC27C32BQE200, 250	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B								Units
			Q120		Q150		Q200, QE200		Q250, QE250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

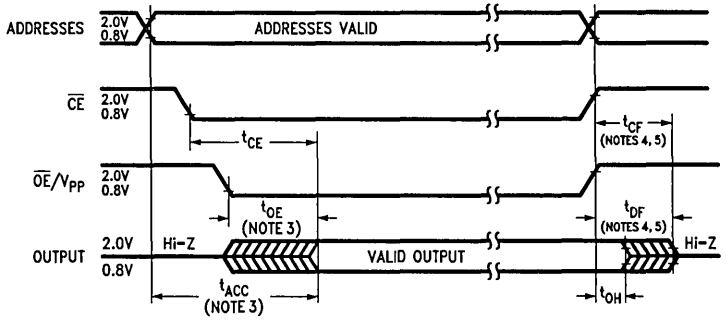
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	V_{IN} = 0V	6	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	20	25	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Note 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

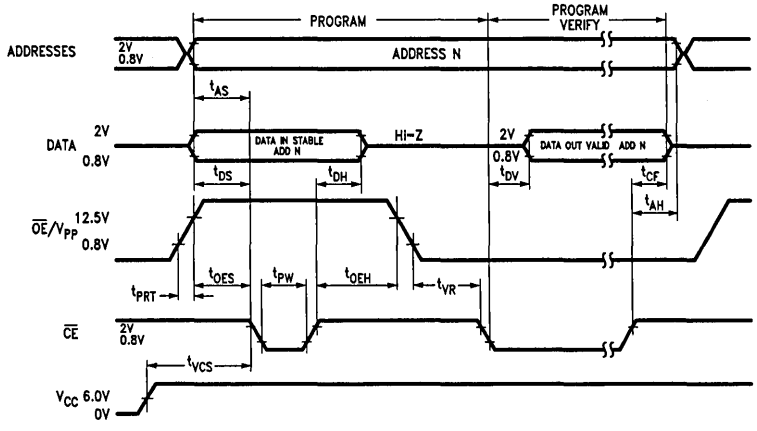
Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



TL/D/8827–4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart (Note 4)

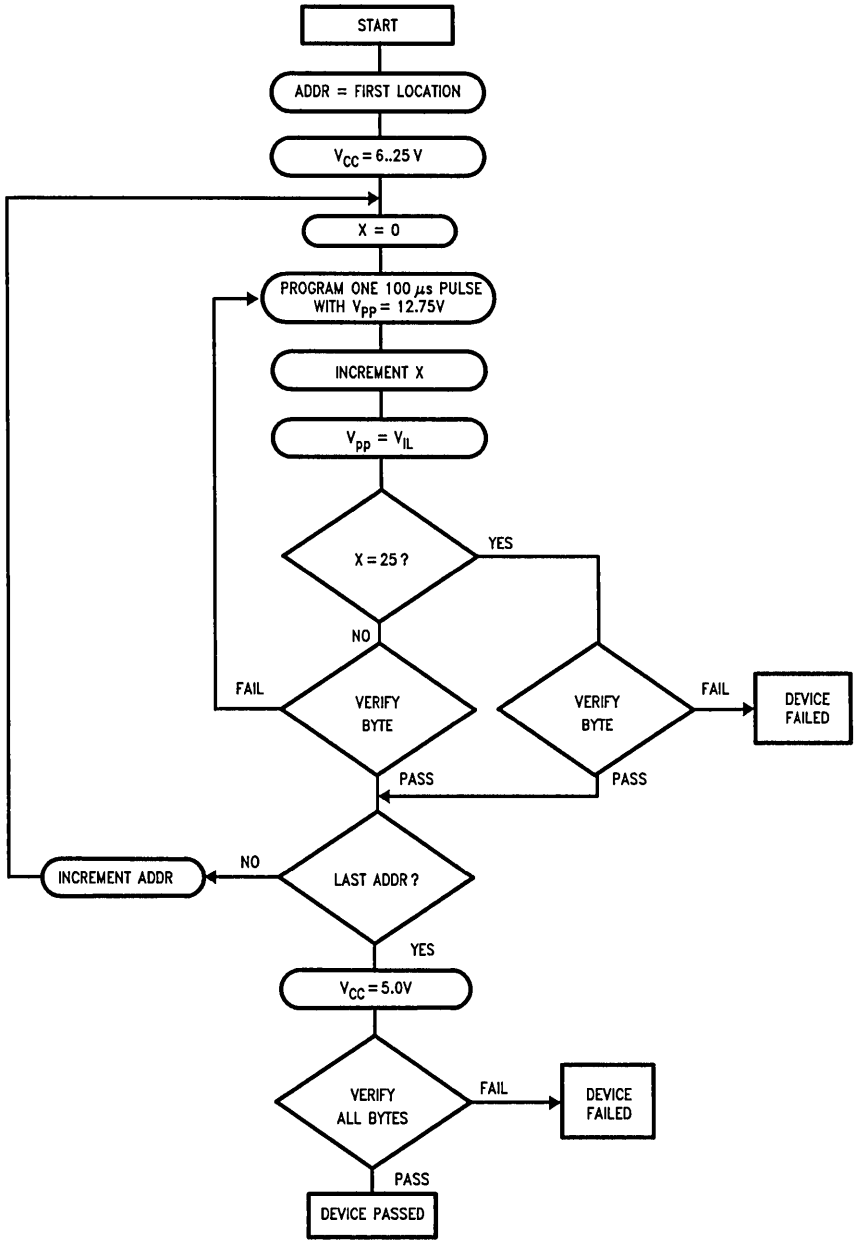


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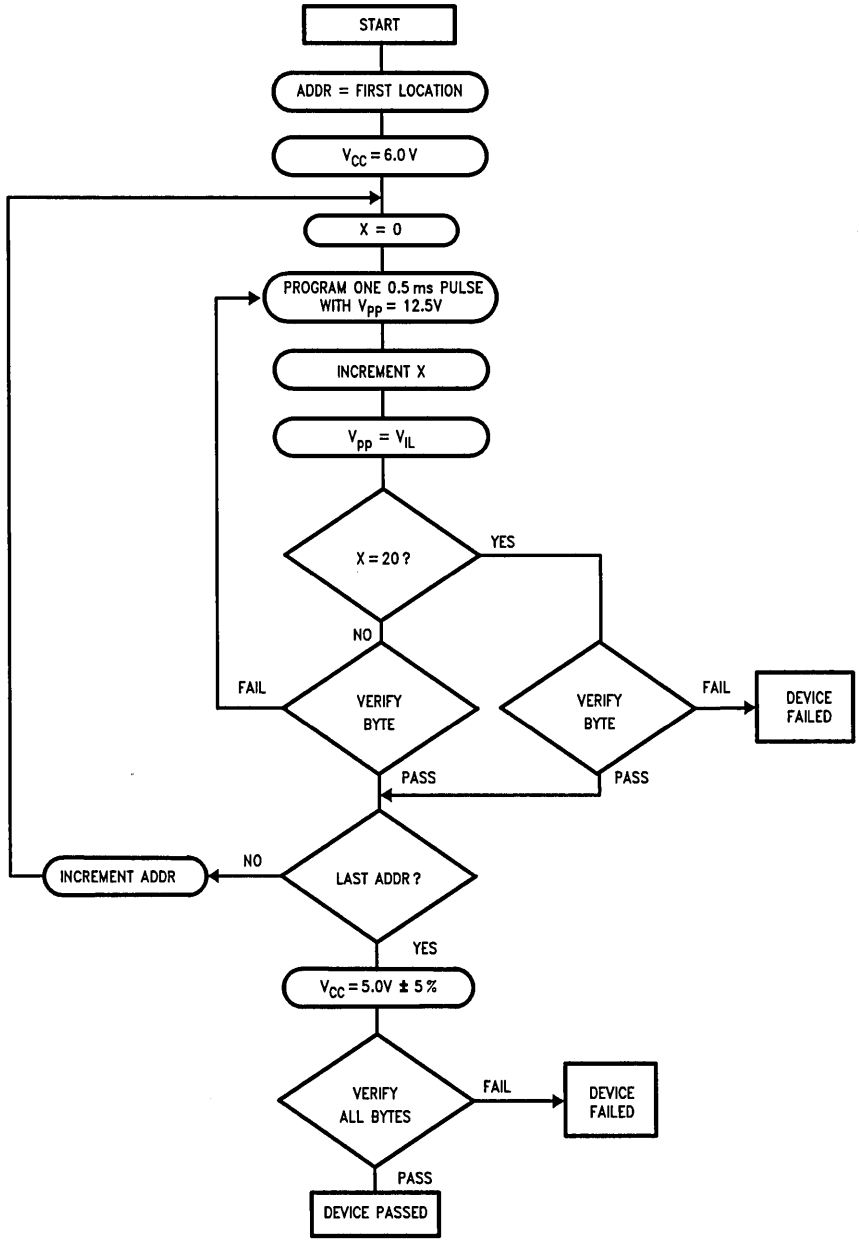
FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)



TL/D/8827–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore the maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 110 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a. The lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 $\overline{OE}/V_{PP}$ will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aide in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F61", where "8F" designates that it is made by National Semiconductor, and "61" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C32B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01

TABLE III. Minimum NMC27C32B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64 65,536-Bit (8k x 8) UV Erasable CMOS PROM

General Description

The NMC27C64 is a high-speed 64k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

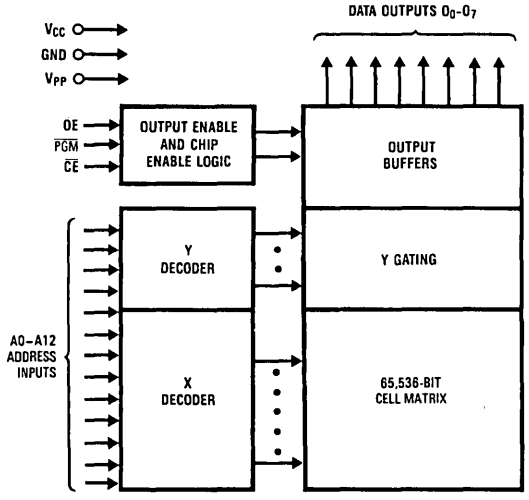
The NMC27C64 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C64QE), −40°C to +85°C, and military temperature range (NMC27C64QM), −55°C to +125°C, available
- Pin compatible with NMOS 64k EPROMs
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control

Block Diagram



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Pin Names

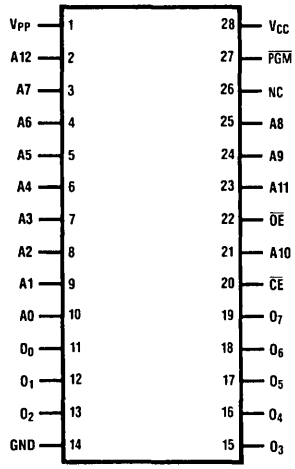
A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64Q
Dual-In-Line Package



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27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Order Number NMC27C64Q
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C64Q15	150

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q150	150
NMC27C64Q200	200
NMC27C64Q250	250
NMC27C64Q300	300

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE150	150
NMC27C64QE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QM200	200
NMC27C64QM250	250

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	
Commercial	−10°C to +80°C
Military and Extended	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q15, Q150, 200, 250, 300	0°C to +70°C
NMC27C64QE200	−40°C to +85°C
NMC27C64QM200, M250	−55°C to +125°C
V_{CC} Power Supply except NMC27C64Q15	+5V ±10%
	+5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64Q								Units
			15, 150, E150		200, E200, M200		250, M250		300		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	0	130	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	0	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

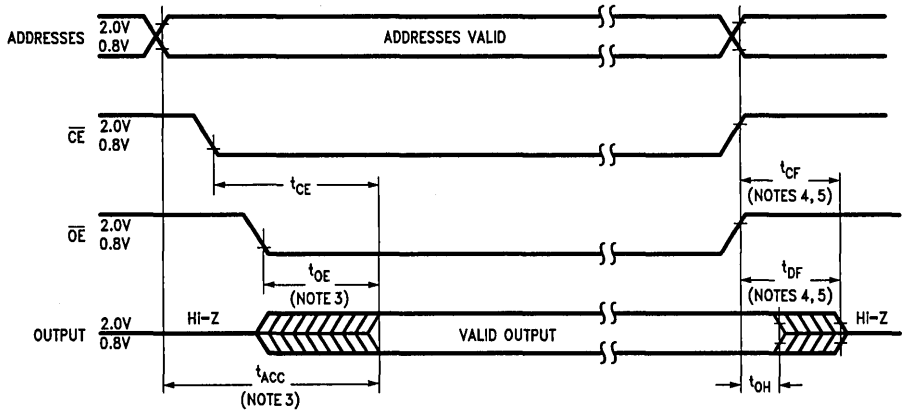
AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

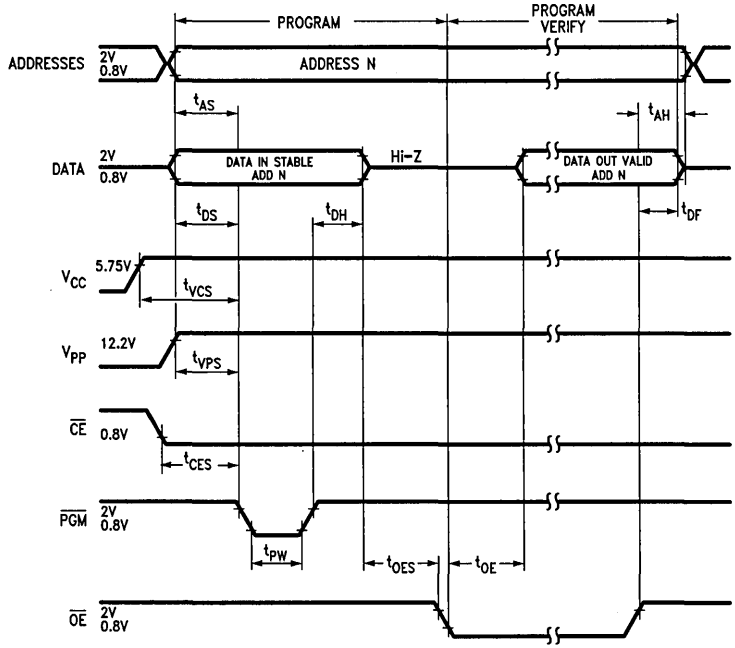
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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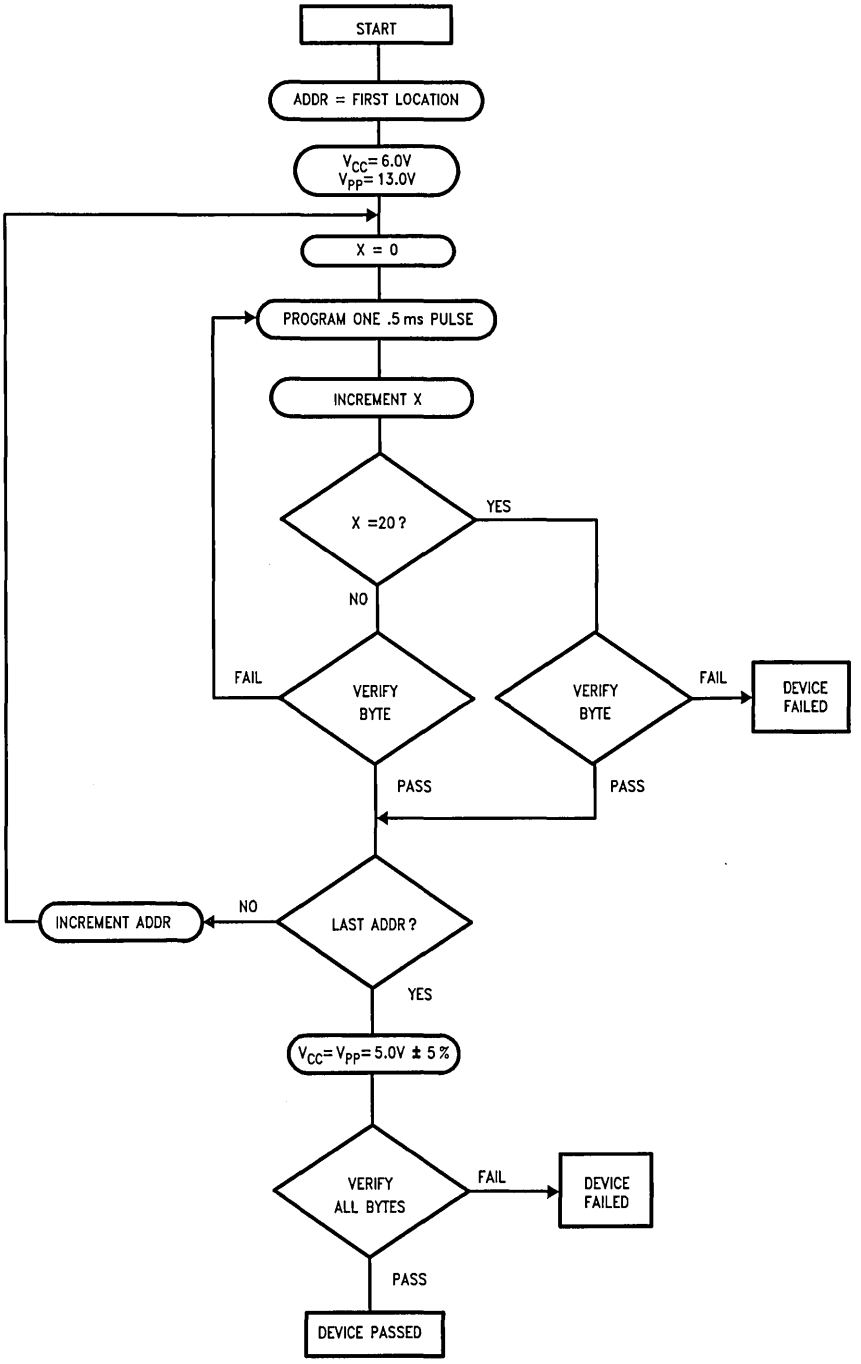
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings. The min and max limit parameters are design parameters, not tested or guaranteed.

Interactive Programming Algorithm Flow Chart



TL/D/8634-5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C64 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64N 65,536-Bit (8k x 8) One-Time Programmable CMOS PROM

General Description

The NMC27C64N is a high-speed 64k one-time programmable CMOS PROM. It is ideally suited for high volume production applications where low cost, fast turnaround, and low power consumption are important factors and reprogramming is not required.

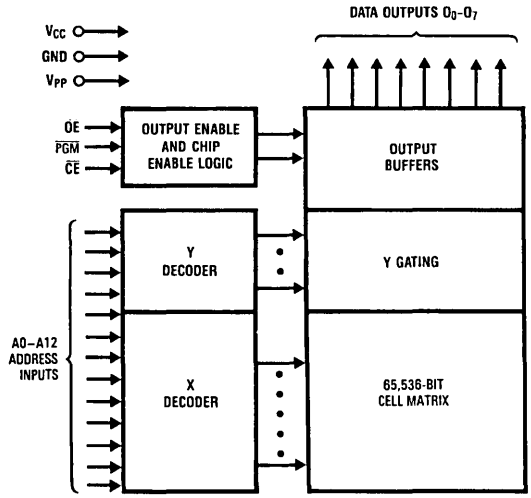
The NMC27C64N is designed to operate with a single +5V power supply with ±10% tolerance. The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This device is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns, CMOS technology
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with all 64k EPROMs
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum PROM for total CMOS systems
- Manufacture's identification code for automatic programming control

Block Diagram



TL/D/9686–1

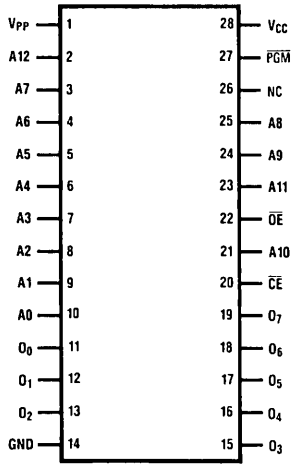
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64N
Dual-In-Line Package



TL/D/9686–2

27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64N pins.

Order Number NMC27C64N
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64N150	150
NMC27C64N200	200
NMC27C64N250	250

(For Non Commercial Temp. Range Parts, Call Factory)

1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 mA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64N						Units
			150		200		250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

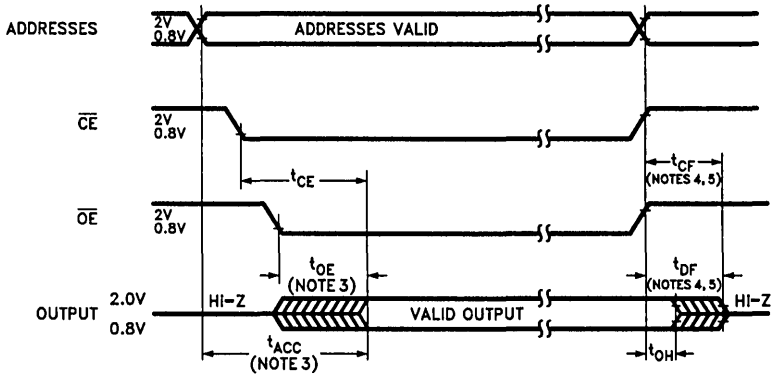
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9686-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −0.2V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

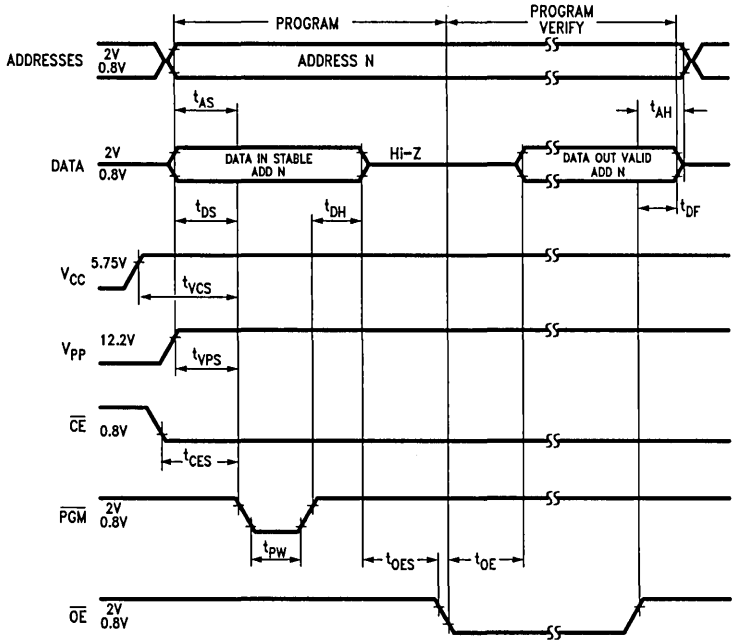
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

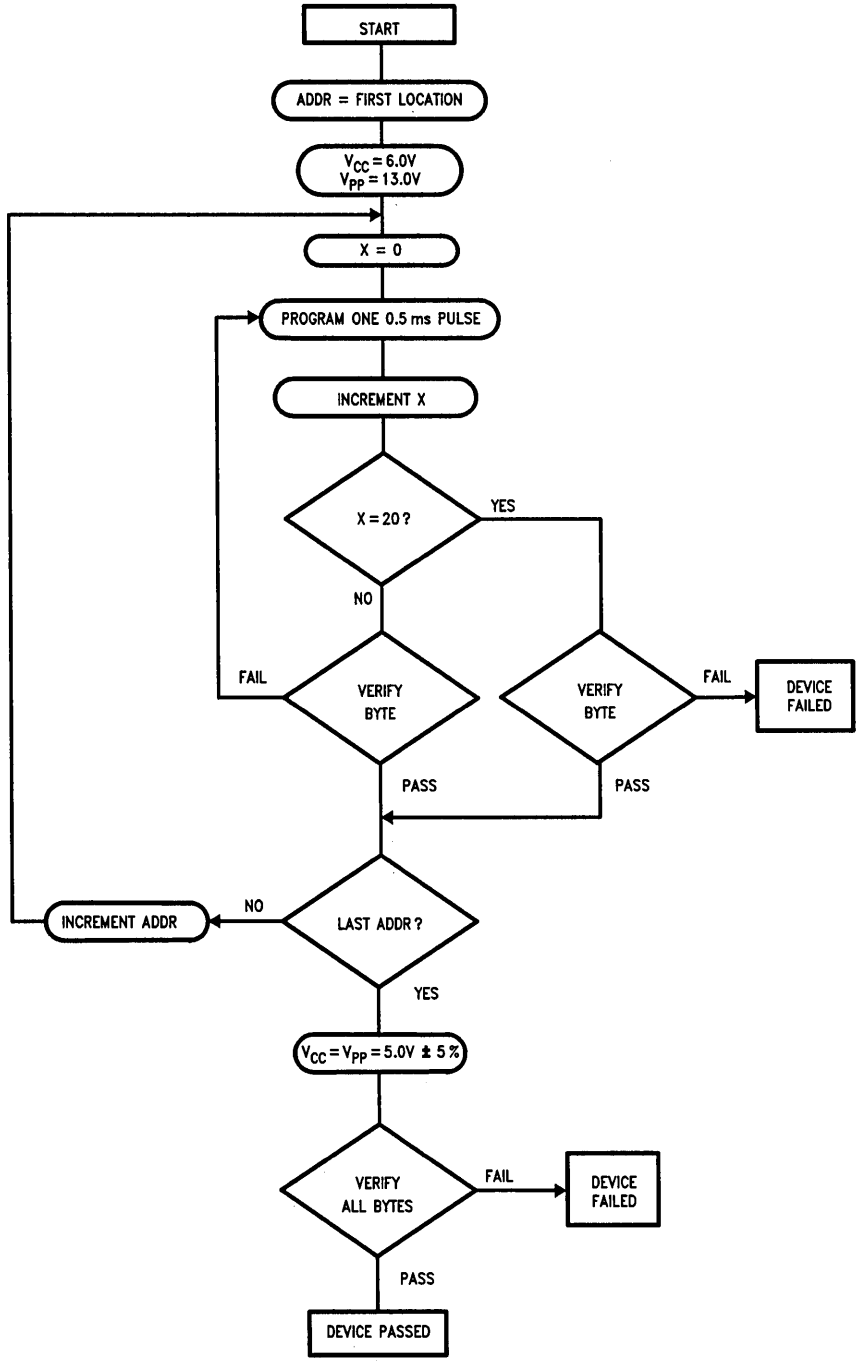
Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings. The min and max limit parameters are design parameters, not tested or guaranteed.

Programming Waveforms (Note 3)



TL/D/9686–4

Interactive Programming Algorithm Flow Chart



TL/D/9686-5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64N are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64N has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64N has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64N is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64Ns are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64N.

Initially, all bits of the NMC27C64N are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed. Due to package constraints programmability of the device is only tested in wafer form.

The NMC27C64N is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data outputs pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64N is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64N must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64Ns in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64Ns may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64Ns.

The NMC27C64N is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Select

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	13.0V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13.0V	6V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64Ns in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64N may be common. A TTL low level program pulse applied to an NMC27C64Ns $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64N. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64Ns from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S INDENTIFICATION CODE

The NMC27C64N has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64N is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

SYSTEM CONSIDERATION

The power switching characteristics of this device require careful decoupling. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

National Semiconductor

PRELIMINARY

NMC27C64B High Speed Version 65,536-Bit (8k x 8) UV Erasable CMOS PROM

General Description

The NMC27C64B is a high-speed 64k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

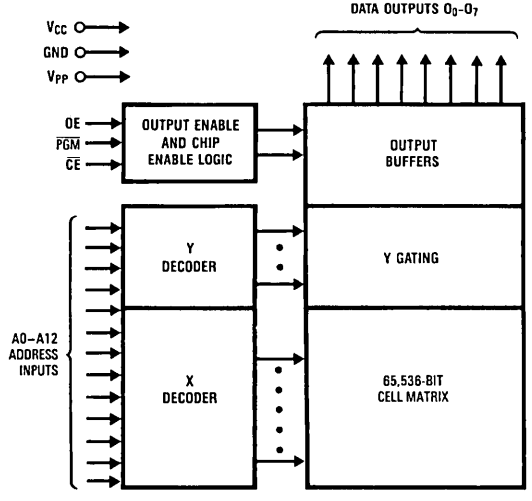
The NMC27C64B is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C64BQE), −40°C to 85°C, and military temperature range (NMC27C64BQM), −55°C to 125°C, available
- Pin compatible with NMOS 64k EPROMs
- Fast and reliable programming (100 μs on most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacture's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9687-1

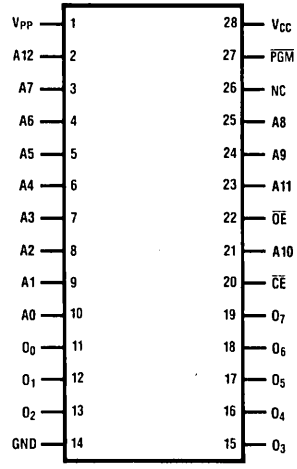
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64BQ
Dual-In-Line Package



TL/D/9687–2

27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64BQ pins.

Order Number NMC27C64BQ
See NS Package Number J28AQ

Commercial Temp Range
(0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64BQ120	120
NMC27C64BQ150	150
NMC27C64BQ200	200
NMC27C64BQ250	250

Extended Temp Range
(−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64BQE120	120
NMC27C64BQE150	150
NMC27C64BQE200	200

Military Temp Range
(−55°C to +125°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64BQM150	150
NMC27C64BQM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (MIL Spec 883C Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64B								Units
			Q120		Q150		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (MIL Spec 883C Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64BQE120, 150, 200	−40°C to +85°C
NMC27C64BQM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64BQ						Units
			E120		E150, M150		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

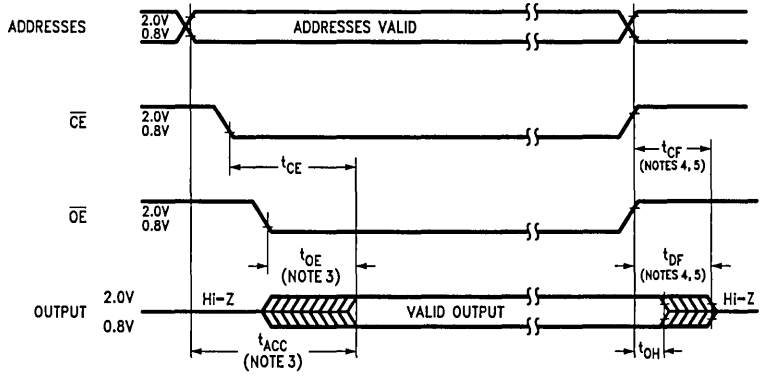
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and T_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} +1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

CL: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temp Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

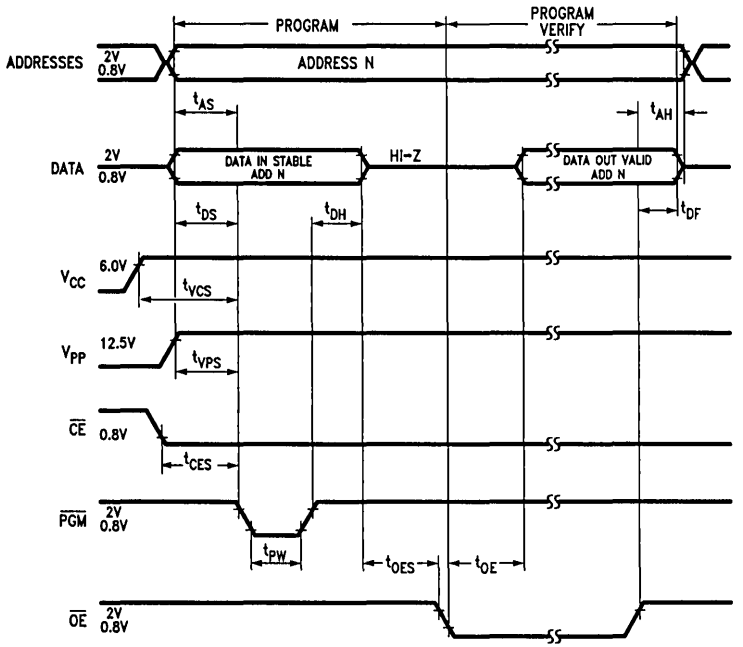
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit parameters are design parameters, not tested or guaranteed.

Programming Waveforms (Note 3)



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Fast Programming Algorithm Flow Chart (Note 4)

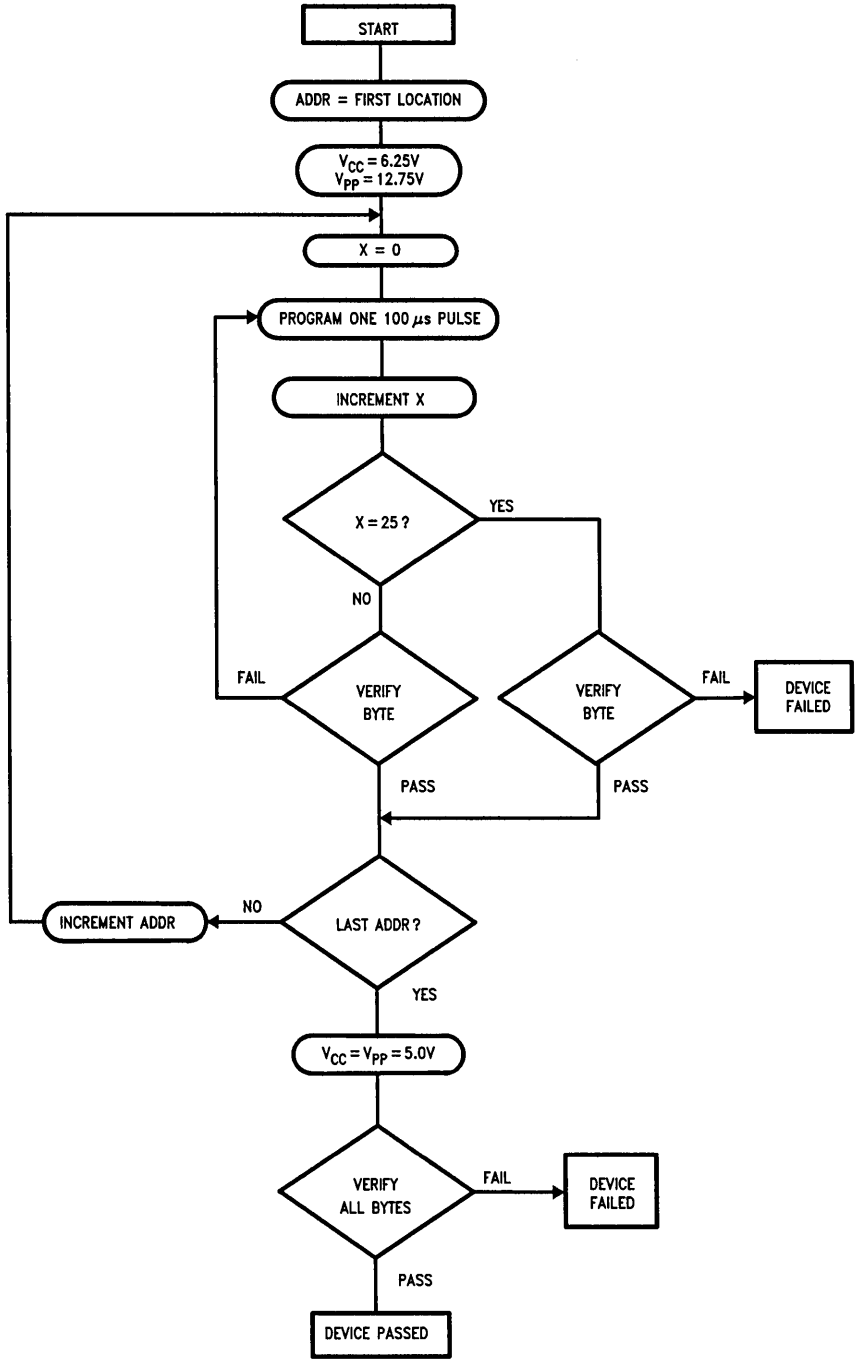

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

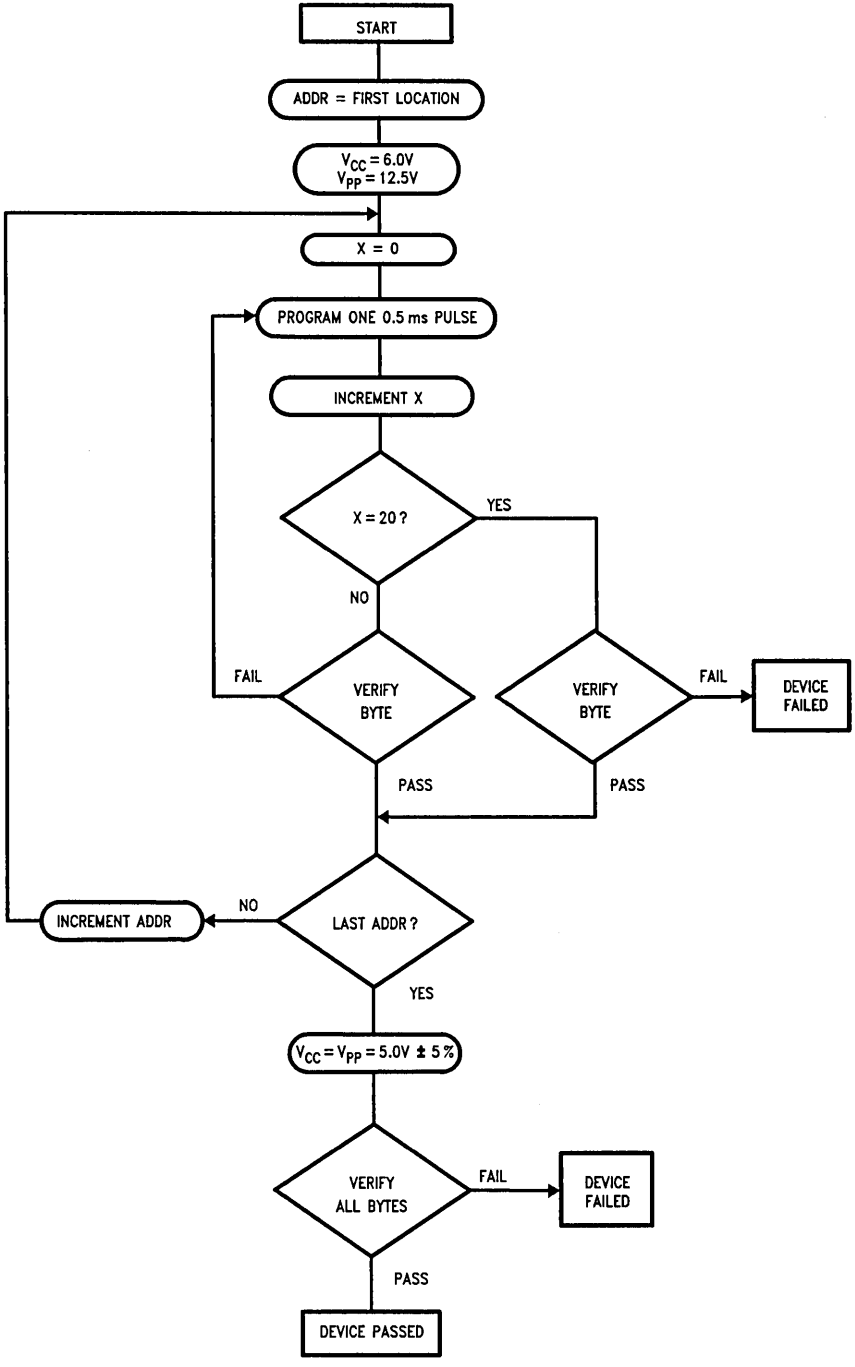

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64B has a standby mode which reduces the active power dissipation by 99%, from 110 mW to 0.55 mW. The NMC27C64B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64B.

Initially, and after each erasure, all bits of the NMC27C64B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C64B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C64B must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64Bs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64Bs.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$* (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

*ALE on 87C64B

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64B's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64B may be common. A TTL low level program pulse applied to an NMC27C64B's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C64B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64B's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64B is "8F02", where "8F" designates that it is made by National Semiconductor, and "02" designates a 64k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64B are such that erasure begins to occur when exposed light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NMC27C64B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	1	0	02

TABLE III. Minimum NMC27C64B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C64BN High-Speed Version 65,536-Bit (8k x 8) One-Time Programmable CMOS PROM

General Description

The NMC27C64BN is a high-speed 64k one-time programmable CMOS PROM. It is ideally suited for high volume production applications where low cost, fast turnaround, and low power consumption are important factors and reprogramming is not required.

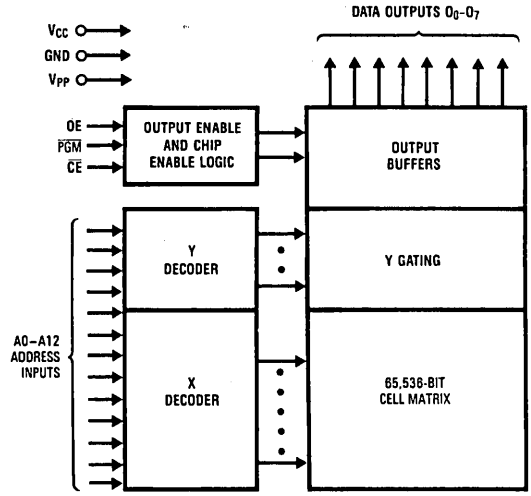
The NMC27C64BN is designed to operate with a single +5V power supply with ±10% tolerance. The NMC27C64BN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming needs to be done once. Also, the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This device is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense for fast-access time down to 120 ns, CMOS technology
- Low CMOS power consumption
  - Active power: 110 mW max
  - Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with all 64k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum PROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9688-1

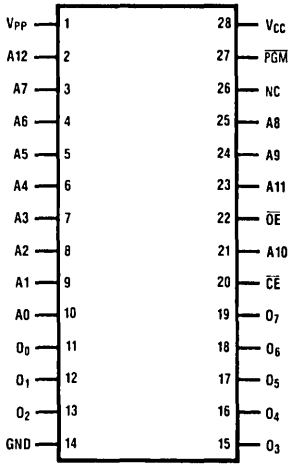
Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 / 27512	27C256 / 27256	27C128 / 27128	27C32 / 2732	27C16 / 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C64BN
Dual-In-Line Package



TL/D/9688-2

27C16 / 2716	27C32 / 2732	27C128 / 27128	27C256 / 27256	27C512 / 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64BN pins.

Order Number NMC27C64BN
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64BN120	120
NMC27C64BN150	150
NMC27C64BN200	200
NMC27C64BN250	250

(For non-commercial temperature range parts, call factory)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64BN								Units
			120		150		200		250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

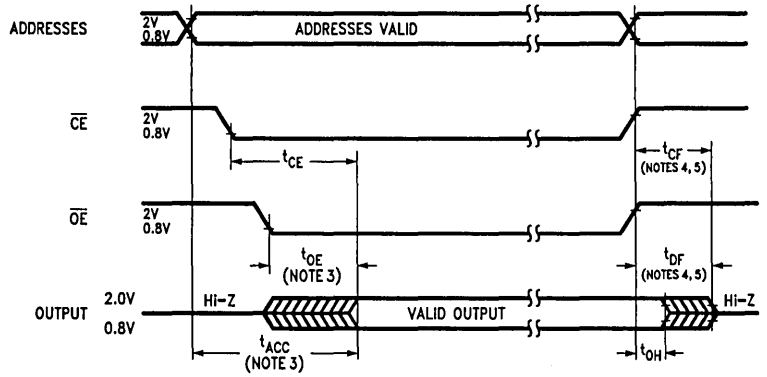
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9688-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

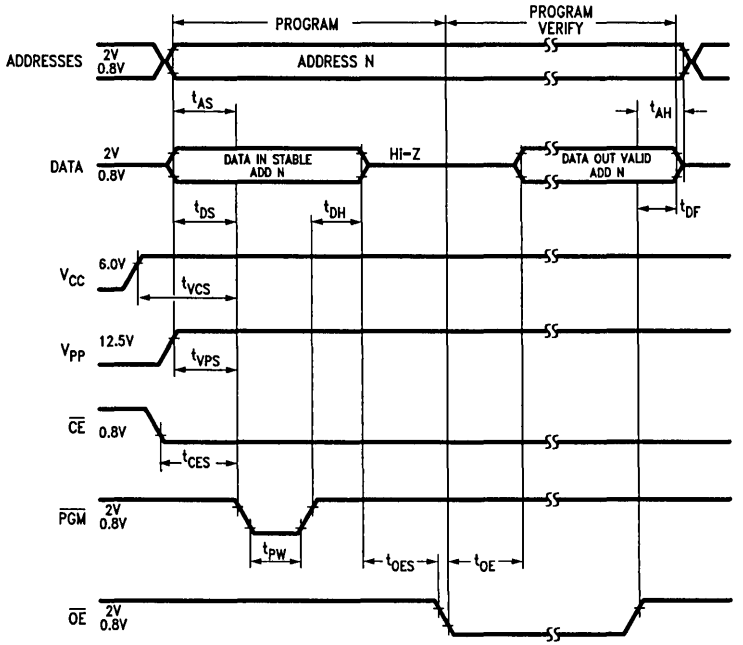
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Level		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Level		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



TL/D/9688–4

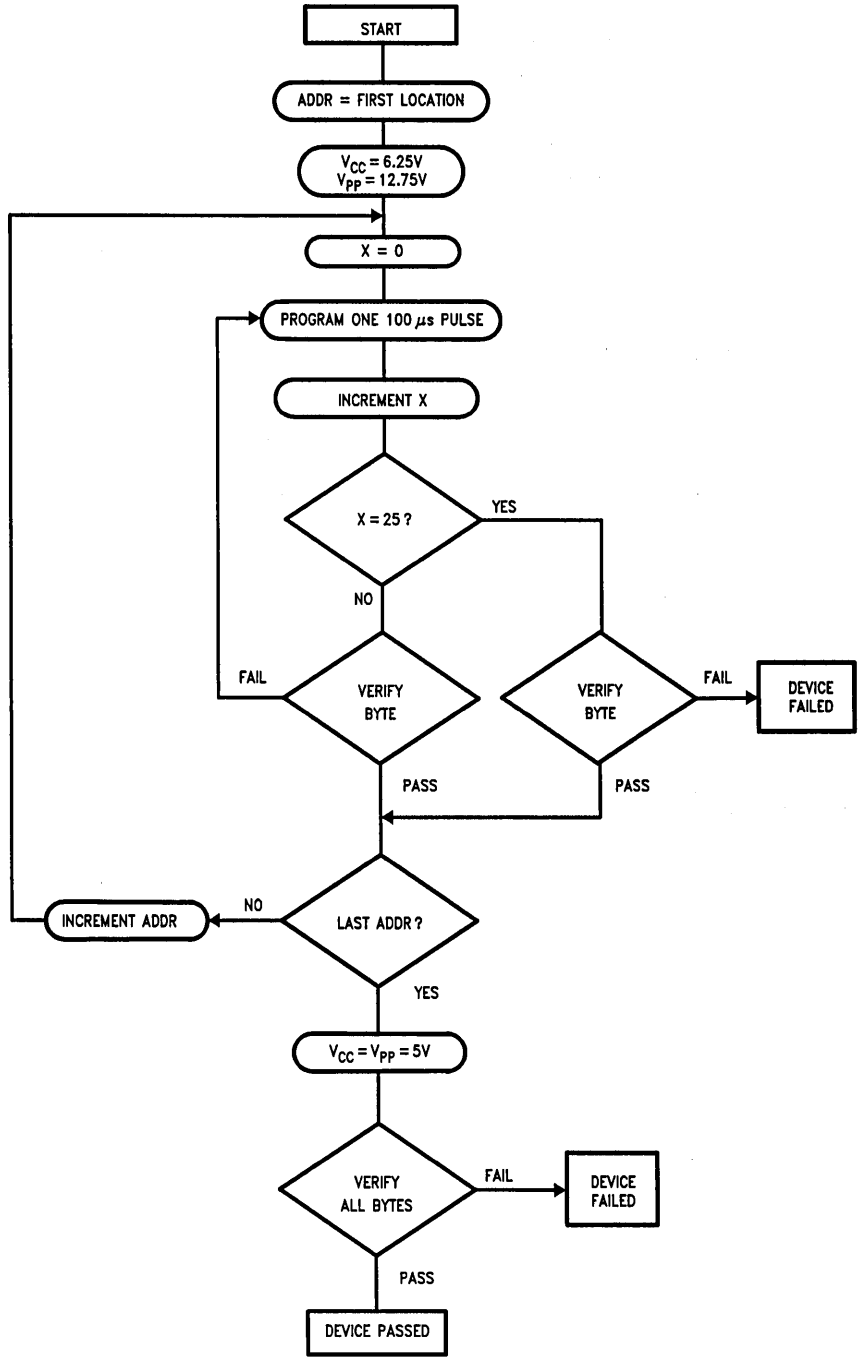
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical Power Supply voltages and timings. The min and max limit parameters are design parameters, not tested or guaranteed.

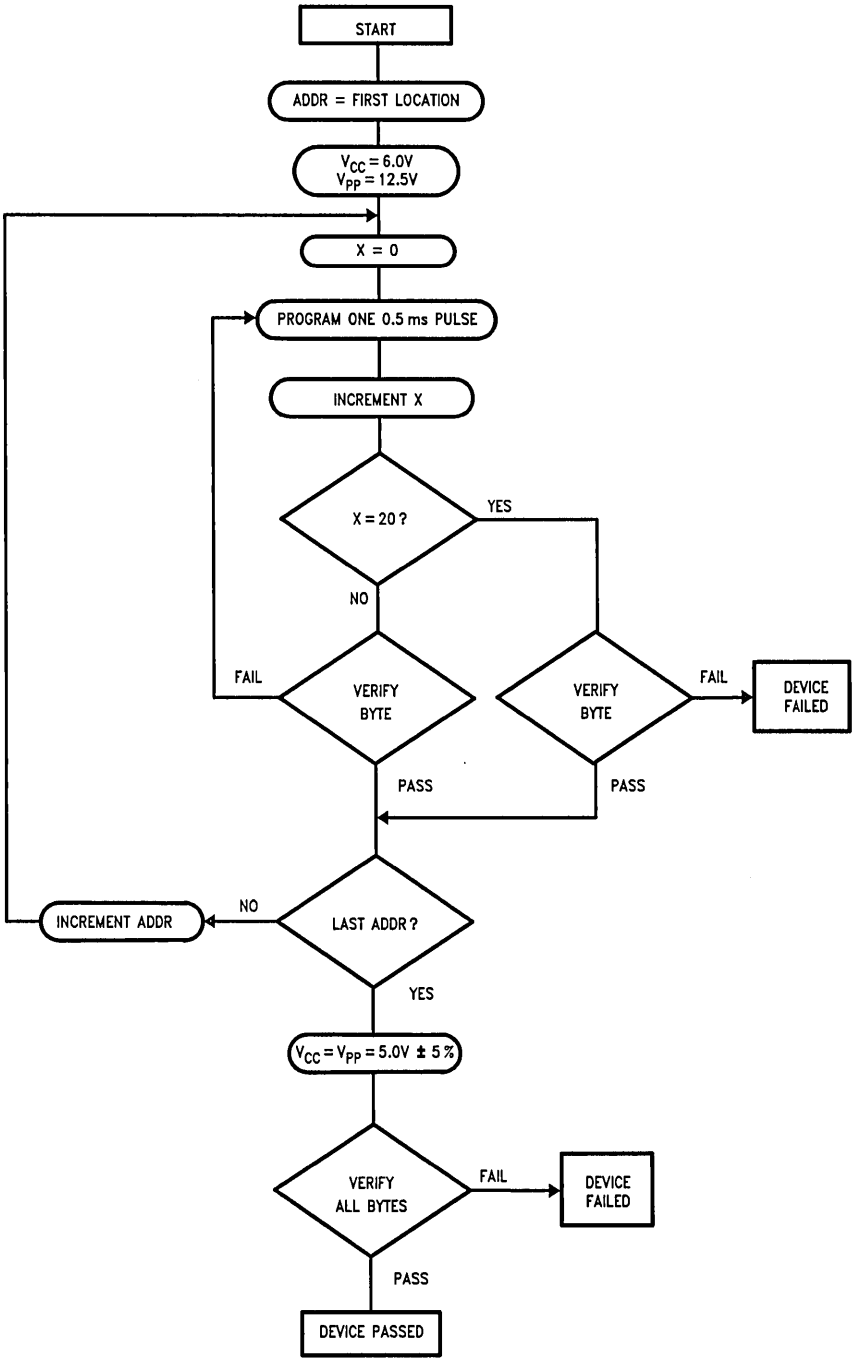
Fast Programming Algorithm Flow Chart (Note 4)



TL/D/9688-5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)



TL/D/9688–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64BN are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64BN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64BN has a standby mode which reduces the active power dissipation by 99%, from 110 mW to 0.55 mW. The NMC27C64BN is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64BNs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64BN.

Initially, and after each erasure, all bits of the NMC27C64BN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C64BN is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64BN is programmed with the Fast Programming Algorithm shown in *Figure 1.* Each address is programmed with a series of 100 μs pulses until it verifies good, up to maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

Note: Some program manufacturers due to equipment limitation may offer interactive program algorithms (shown in *Figure 2*).

The NMC27C64BN must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64BNs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64BNs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64BNs.

The NMC27C64BN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C64BQ UV erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64BNs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64BN may be common. A TTL low level program pulse applied to an NMC27C64BN's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C64BN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64BNs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64BN has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64BN is "8F02", where "8F" designates that it is made by National Semiconductor, and "02" designates a 64k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

SYSTEM CONSIDERATION

The power switching characteristics of this device require careful decoupling. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	1	0	02

National Semiconductor

NMC27CP128
131,072-Bit (16k x 8) UV Erasable CMOS PROM

General Description

The NMC27CP128 is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27CP128 is designed to operate with a single +5V power supply with ±10% tolerance.

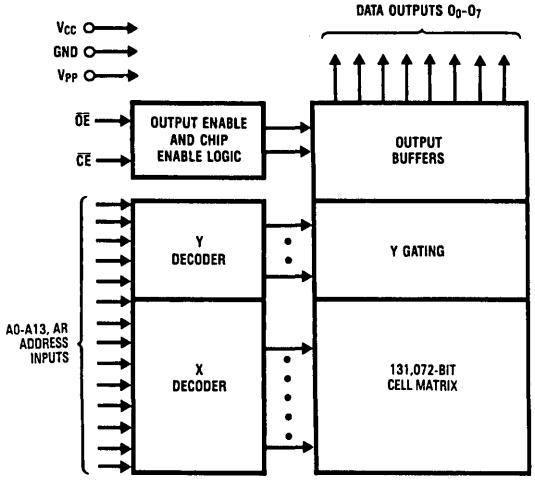
The NMC27CP128 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 200 ns
- Low CMOS power consumption
  - — Active power: 55 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems

Block Diagram



TL/D/8805–1

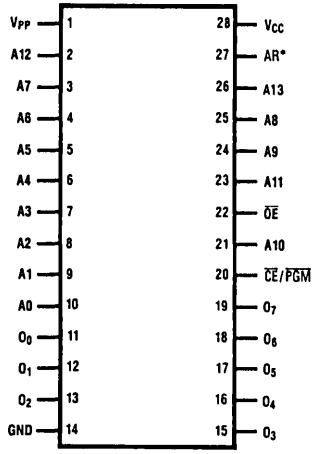
Pin Names

A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
AR	Block Select

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27CP128Q
Dual-In-Line Package



TL/D/8805-2

27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

*AR held at V_{IH}

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27CP128 pins.

Order Number NMC27CP128Q
See NS Package Number J28AQ

Commercial Temp Range
(0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27CP128Q200	200
NMC27CP128Q250	250
NMC27CP128Q300	300

1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{CC} Supply with Respect to Ground	+7.0V to −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range NMC27CP128Q200, 250, 300	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{PP}	V_{PP} Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}/\overline{PGM}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE}/\overline{PGM} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27CP128Q						Units
			200		250		300		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}/\overline{PGM}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}/\overline{PGM} = V_{IL}$		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}/\overline{PGM} = V_{IL}$	0	60	0	60	0	105	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}/\overline{PGM}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$	0		0		0		ns

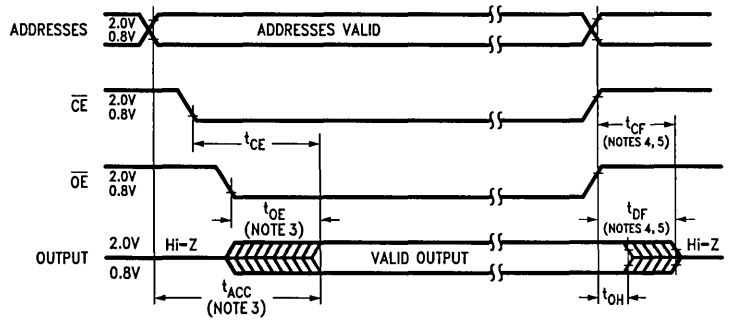
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/8805-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: AR held at V_{IH}.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

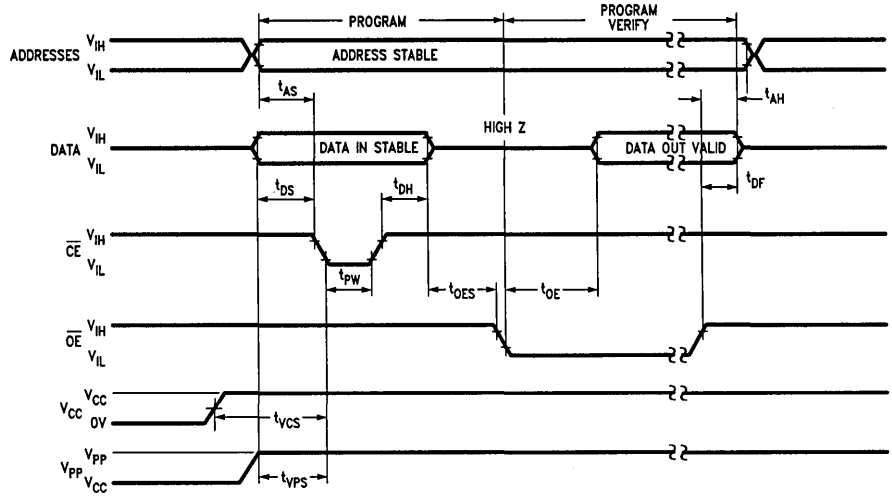
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms (Note 3)



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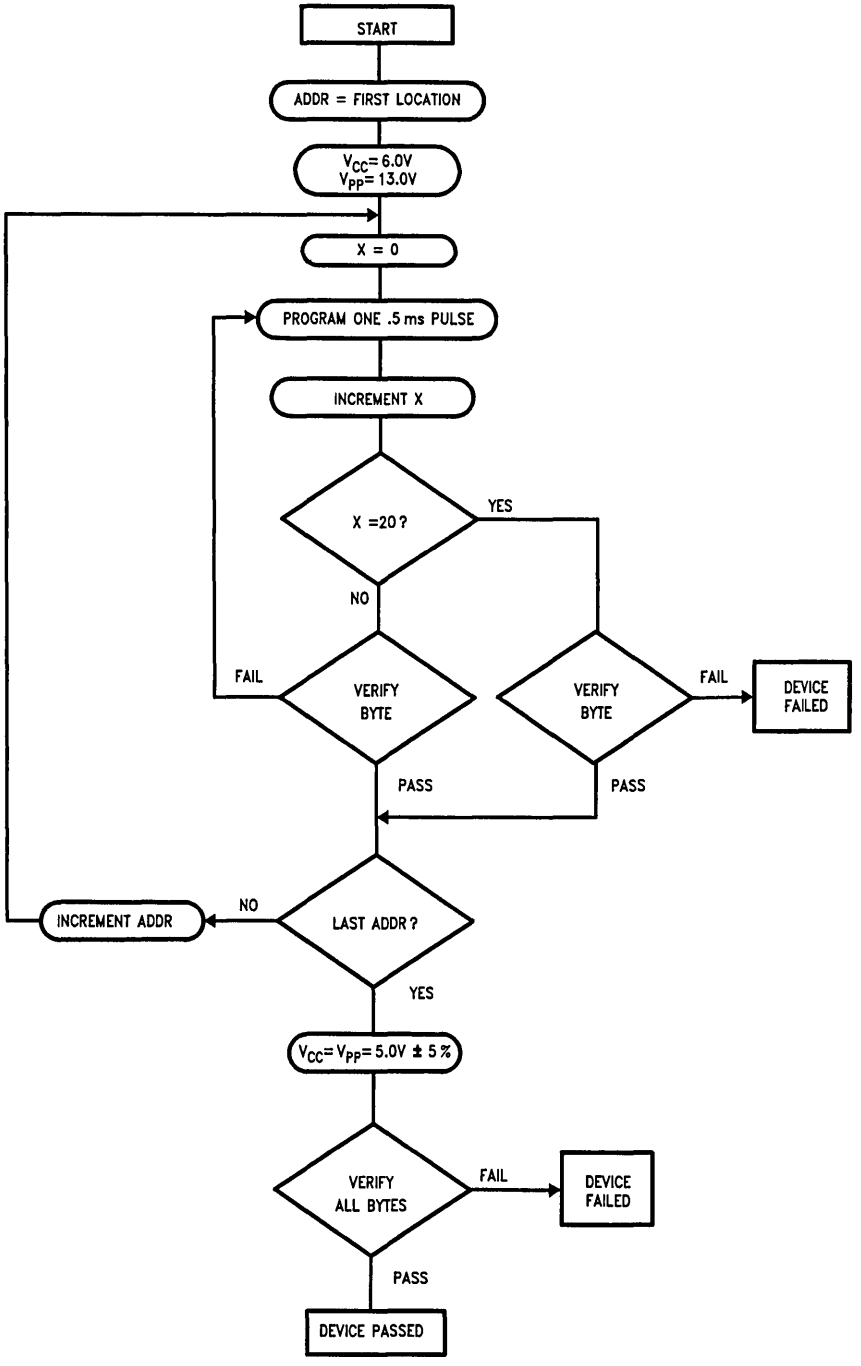
Interactive Programming Algorithm Flow Chart



TL/D/8805–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27CP128 are listed in Table I. It should be noted that all inputs for the six modes may be at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27CP128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27CP128 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27CP128 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27CP128s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27CP128.

Initially, and after each erasure, all bits of the NMC27CP128 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27CP128 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs may be TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27CP128 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Since the NMC27CP128 employs the last 131,072 bits of a 262,144 bit memory array, programming must be started at address 16,384 to provide correct data read. The NMC27CP128 must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27CP128s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27CP128s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27CP128s.

The NMC27CP128 is a partial NMC27C256 and therefore is not program compatible with most 128k EPROMs.

The Manufacturer's Identification Code should not be used for programming control of the NMC27CP128.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	13.0V	6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27CP128s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel NMC27CP128 may be common. A low level $\overline{CE}/\overline{PGM}$ input selects the devices to be programmed. A high level $\overline{CE}/\overline{PGM}$ input inhibits the other devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27CP128 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27CP128's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27CP128 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27CP128 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27CP128 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27CP128 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C128B High Speed Version 131,072-Bit (16k x 8) UV Erasable CMOS PROM

General Description

The NMC27C128B is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C128B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

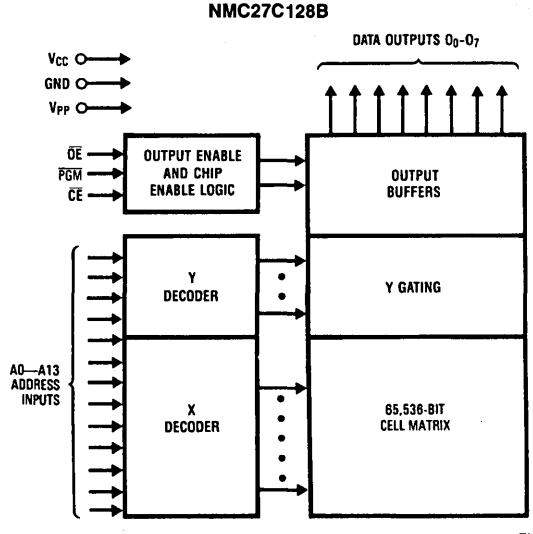
The NMC27C128B is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clock sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C128BQE), −40°C to +85°C, and military temperature range (NMC27C128BQM), −55°C to +125°C available
- Pin compatible with NMOS 128k EPROMs
- Fast and reliable programming (100 μs on most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9689-1

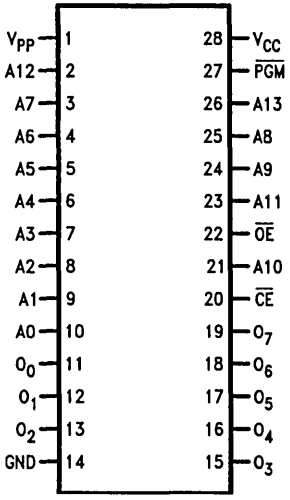
Pin Names

A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagrams

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C128B
Dual-In-Line Package



TL/D/9689–2

27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128B pins.

Order Number NMC27C128BQ
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQ120	120
NMC27C128BQ150	150
NMC27C128BQ200	200
NMC27C128BQ250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQE120	120
NMC27C128BQE150	150
NMC27C128BQE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQM150	150
NMC27C128BQM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128B								Units
			Q120		Q150		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C128BQE120, 150, 200	−40°C to +85°C
NMC27C128BQM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128BQ						Units
			E120		E150, M150		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

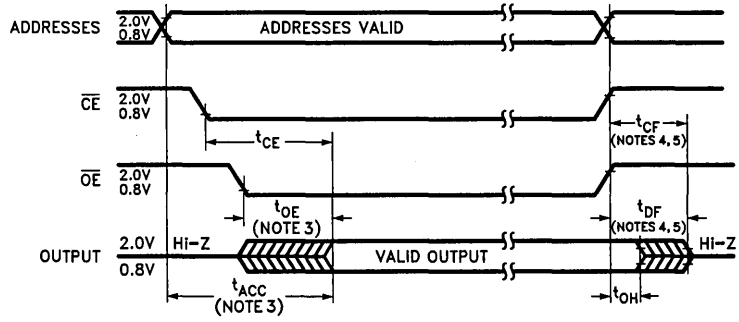
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9689-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V;

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

C_L: 100 pF includes fixture capacitance.

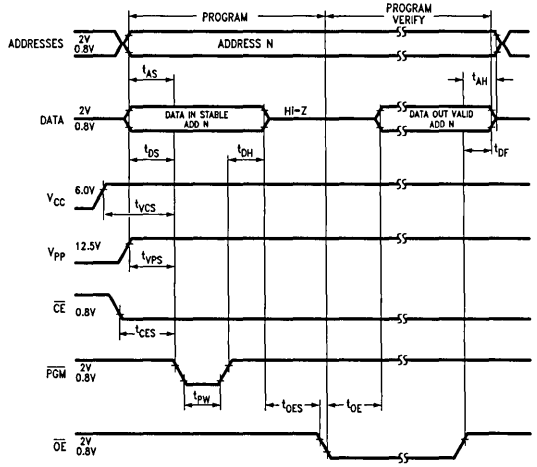
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart (Note 4)

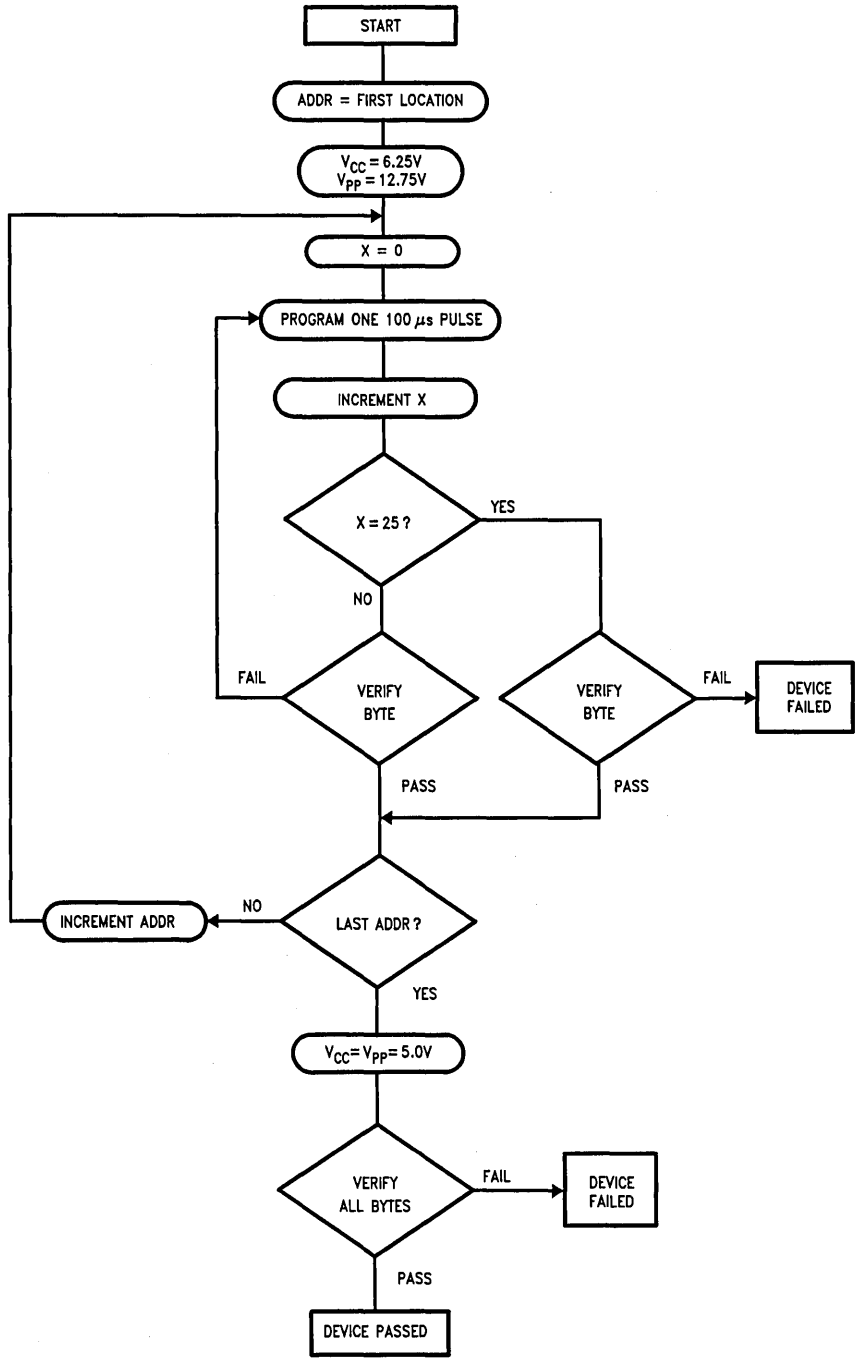

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

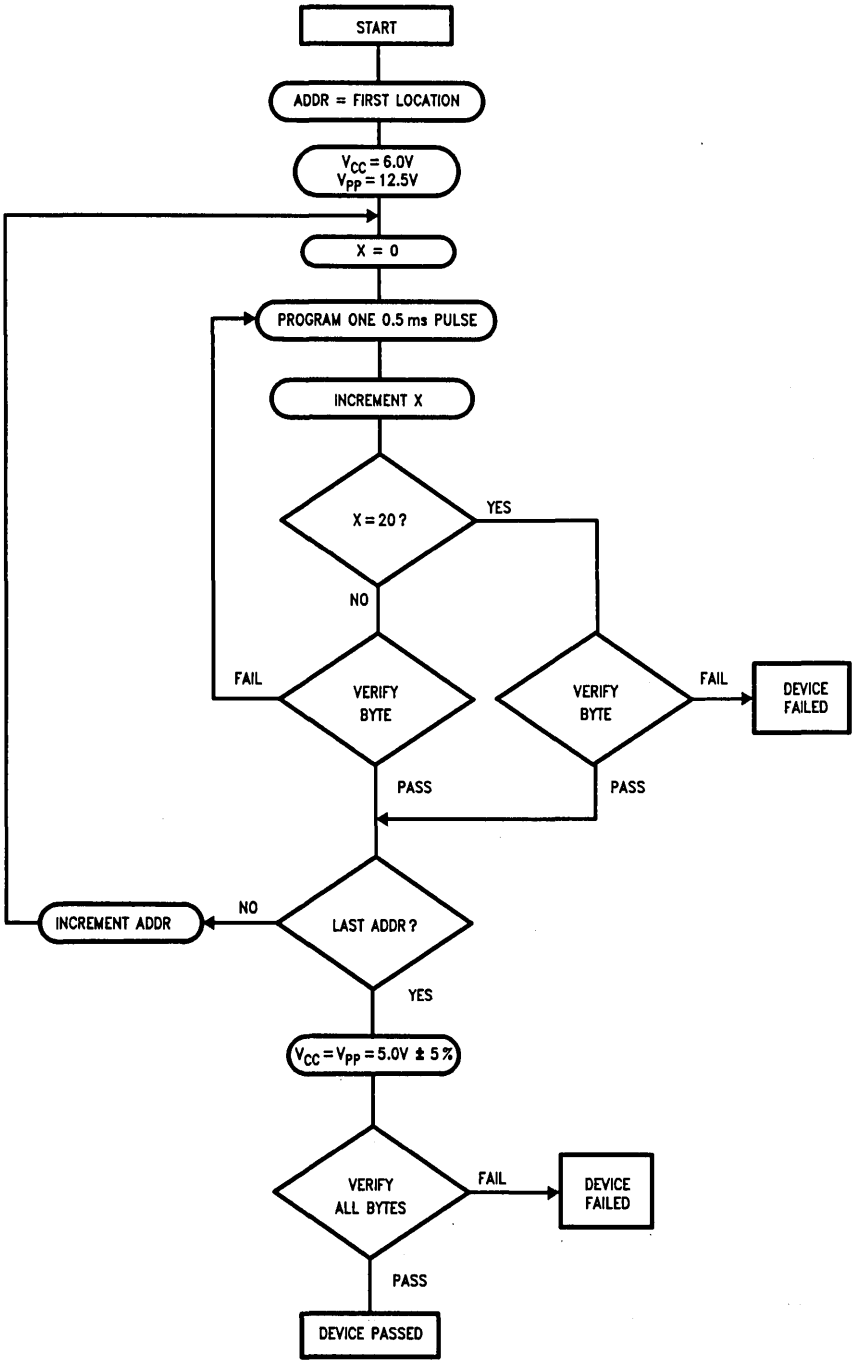

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C128B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C128B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C128B has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C128B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C128Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C128B.

Initially, and after each erasure, all bits of the NMC27C128B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C128B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C128B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C128B must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C128Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C128Bs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C128Bs.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$* (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

*ALE on 87C128B

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C128s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C128Bs may be common. A TTL low level program pulse applied to an NMC27C128B's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C128B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C128Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C128B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C128B is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C128B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NMC27C128B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C128B exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C128B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C128B erasure time for various light intensities.

An erasure system should be cailbrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of this device require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	1	1	83

TABLE III. Minimum NMC27C128B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C128BN
High Speed Version 131,072-Bit (16k x 8) One Time Programmable CMOS PROM

General Description

The NMC27C128BN is a high-speed 128k one time programmable CMOS PROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C128BN is designed to operate with a single +5V power supply with ±10% tolerance.

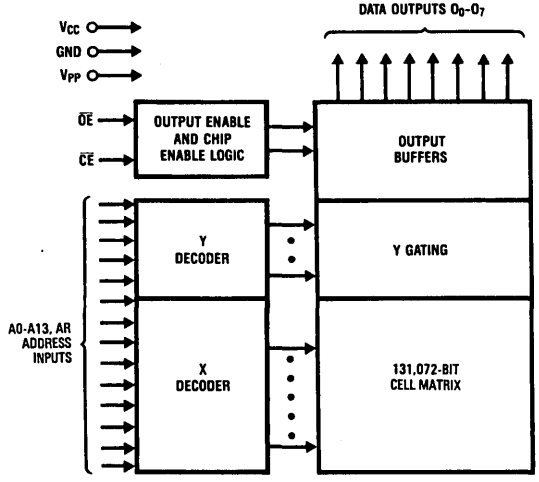
The NMC27C128BN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This PROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 11.0 mW max
  - — Standby Power: 0.55 mW max
- Optimum PROM for total CMOS systems
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with 128k EPROMS
- Fast and reliable programming (100 μs on most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9690-1

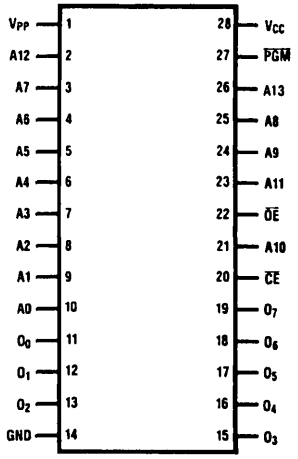
Pin Names

A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128BN pins.

Order Number NMC27C128BN
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BN120	120
NMC27C128BN150	150
NMC27C128BN200	200
NMC27C128BN250	250

For non-commercial temperature range parts, call the factory.

1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −6.0V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C128B								Units
			N120		N150		N200		N250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

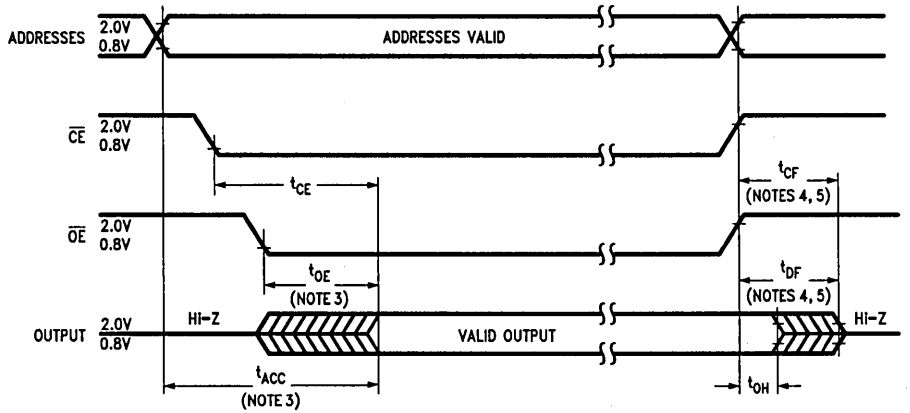
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

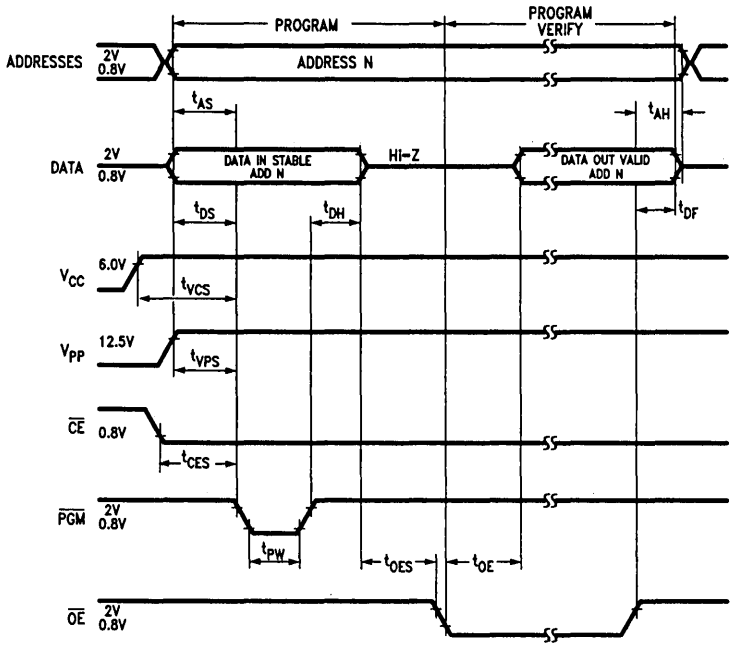
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not tested or guaranteed.

Fast Programming Algorithm Flow Chart (Note 4)

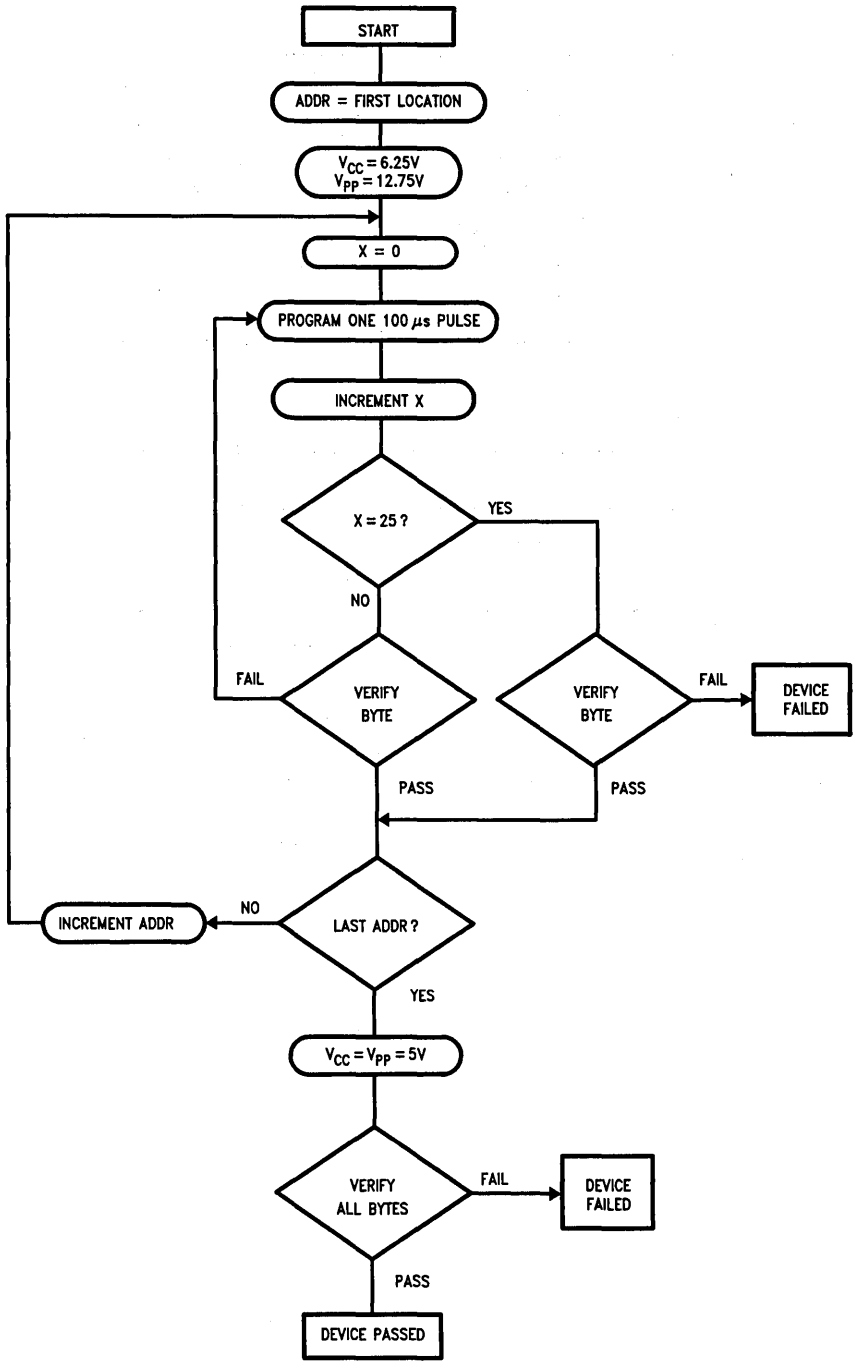

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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

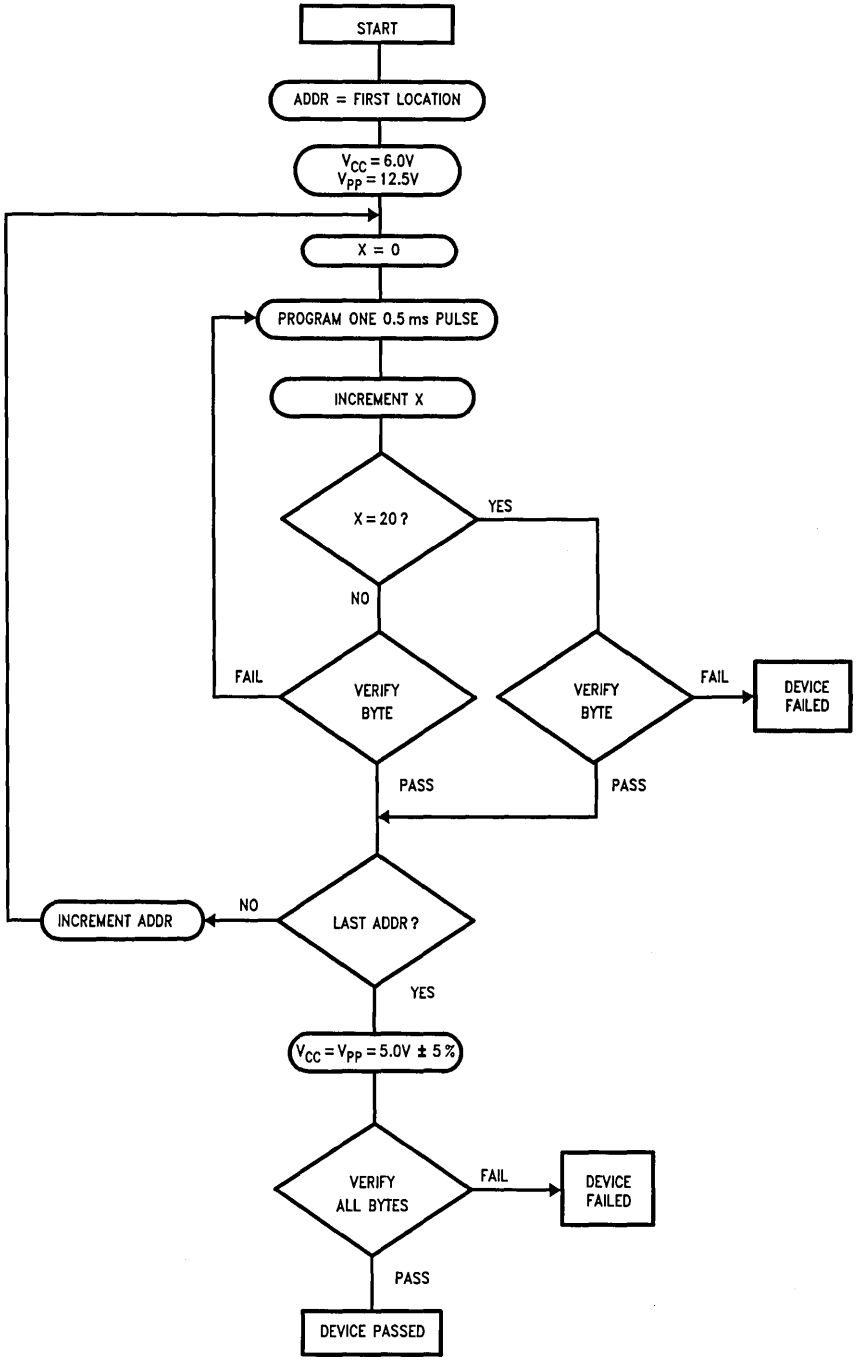

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C128BN are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C128BN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C128BN has a standby mode which reduces the active power dissipation over 99%, from 110 mW to 0.55 mW. The NMC27C128BN is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C128BNs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C128BN.

Initially, and after each erasure, all bits of the NMC27C128BN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word.

The NMC27C128BN is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C128BN is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C128BN must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C128BNs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C128BNs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C128BNs.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

The NMC27C128BN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C128BQ UV Erasable PROM in a windowed package should be used.

Program Inhibit

Programming multiple NMC27C128BNs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C128BNs may be common. A TTL low level program pulse applied to an NMC27C128BNs $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C128BN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C128BNs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V (V_{PP} must be at V_{CC}) except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C128BN has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C128BN is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	1	1	83

National Semiconductor

PRELIMINARY

NMC27C128C 131,072-Bit (16k x 8) UV Erasable CMOS PROM (Very High Speed Version)

General Description

The NMC27C128C is a high-speed 128k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C128C is designed to operate with a single +5V power supply with 10% tolerance.

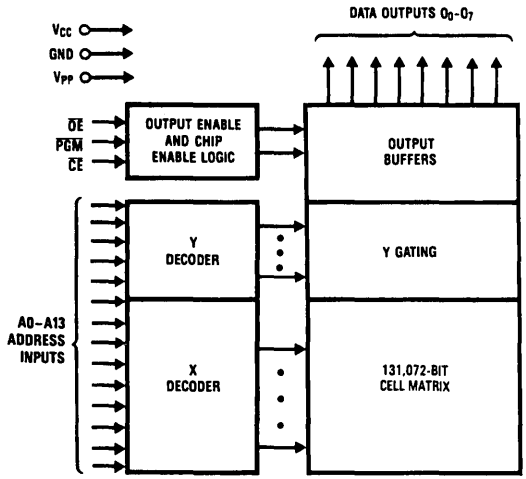
The NMC27C128C is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and two transistor memory cell for fast access time
- Low CMOS power consumption
  - — Active power: 275 mW max
  - — Standby power: 5.1 mW max
- Single 5V power supply
- Pin compatible with standard CMOS and NMOS EPROMs
- Performance compatible with current high-speed microprocessors
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible input/outputs
- TRI-STATE output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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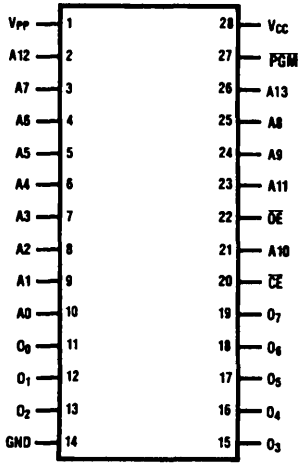
Pin Names

A0–A13	Addresses
$\overline{CE}$-	Chip Enable
$\overline{OE}$-	Output Enable
O_0–O_7	Outputs

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C128C
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128CQ pins.

Order Number NMC27C128CQ
See NS Package Number J28AQ

Commercial Temp. Range (0°C to 70°C)
V_{CC} = 5V ±10%

Parameter/Order	Number	Access Time (ns)
NMC27C128CQ	45	45
NMC27C128CQ	55	55
NMC27C128CQ	70	70

1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −6.0V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating (Mil Std. 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{PP1}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	f = 20 MHz, Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	f = 20 MHz, Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		2	5	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	1	mA
V_{IL}	Input Low Voltage	(Note 10)	−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 7)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 7)	V_{CC} − 0.1			V

AC Electrical Characteristics

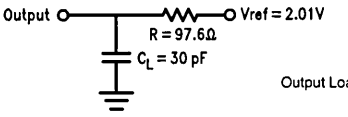
Symbol	Parameter	Conditions	NMC27C128C						Units
			Q45		Q55		Q70		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE}$, = $\overline{CE}$ = V_{IL}		45		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		45		55		70	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		25		25		30	ns
t_{DF} (Note 2)	$\overline{OE}$ Disable to Output Float	$\overline{CE} = V_{IL}$	0	25	0	25	0	30	ns
t_{CF} (Note 2)	$\overline{CE}$ Disable to Output Float	$\overline{OE} = V_{IL}$	0	25	0	25	0	30	ns
t_{OH}	Output Hold from Addresses, $\overline{OE}$ or $\overline{CE}$, Whichever Occurred First	$\overline{OE}$, = $\overline{CE}$ = V_{IL}	0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0V to 3.0V
Output Load is 97.6Ω between all output and 2.01V, CL = 30 pF (Note 8)	
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



Output Loading

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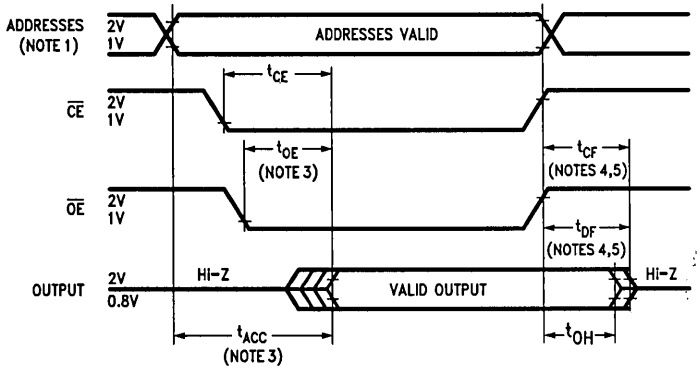
AC Waveforms (Notes 6, 7 and 9)



TL/D/9185-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained by $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: C_L = 30 pF includes fixture capacitance.

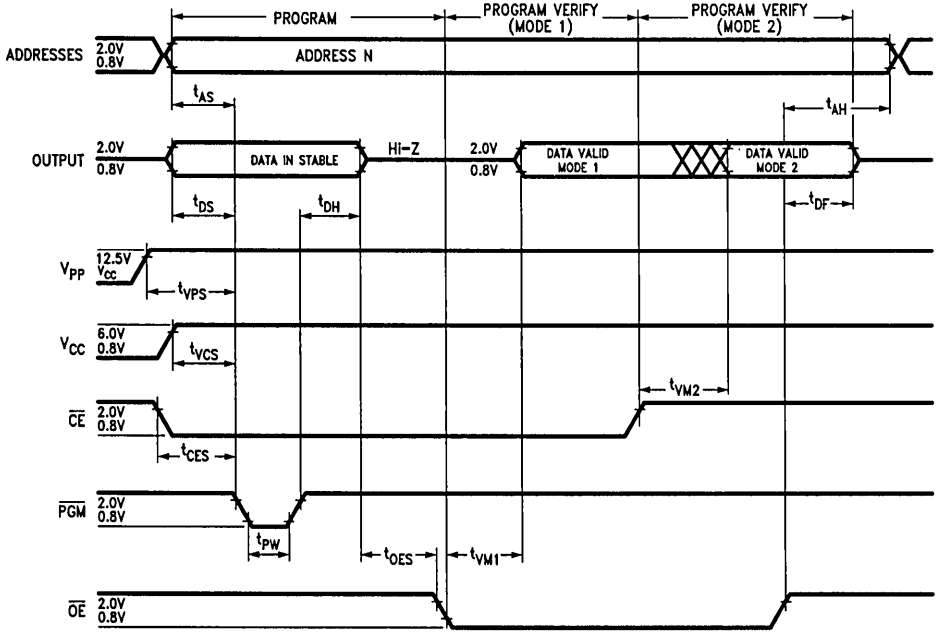
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for a maximum of 20 ns.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay (Notes 5, 6)		0		50	ns
t_{OES}	$\overline{OE}$ Hold Time		1			μs
t_{PW}	Program Pulse Width		95	100	105	μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{OE}$, $\overline{CE}$, $\overline{PGM}$ = V_{IL}		60		mA
I_{CC}	V_{CC} Supply Current			60		mA
t_{VM1}	$\overline{OE}$ to Data Valid During Verify Mode 1	$\overline{PGM}$ = V_{IH}, $\overline{CE}$ = V_{IL}			0.1	μs
t_{VM2}	$\overline{CE}$ to Data Valid During Verify Mode 2	$\overline{PGM}$ = V_{IH}, $\overline{OE}$ = V_{IL}			0.1	μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE}$ = V_{IH}	1			μs
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Level Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Level Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 4)



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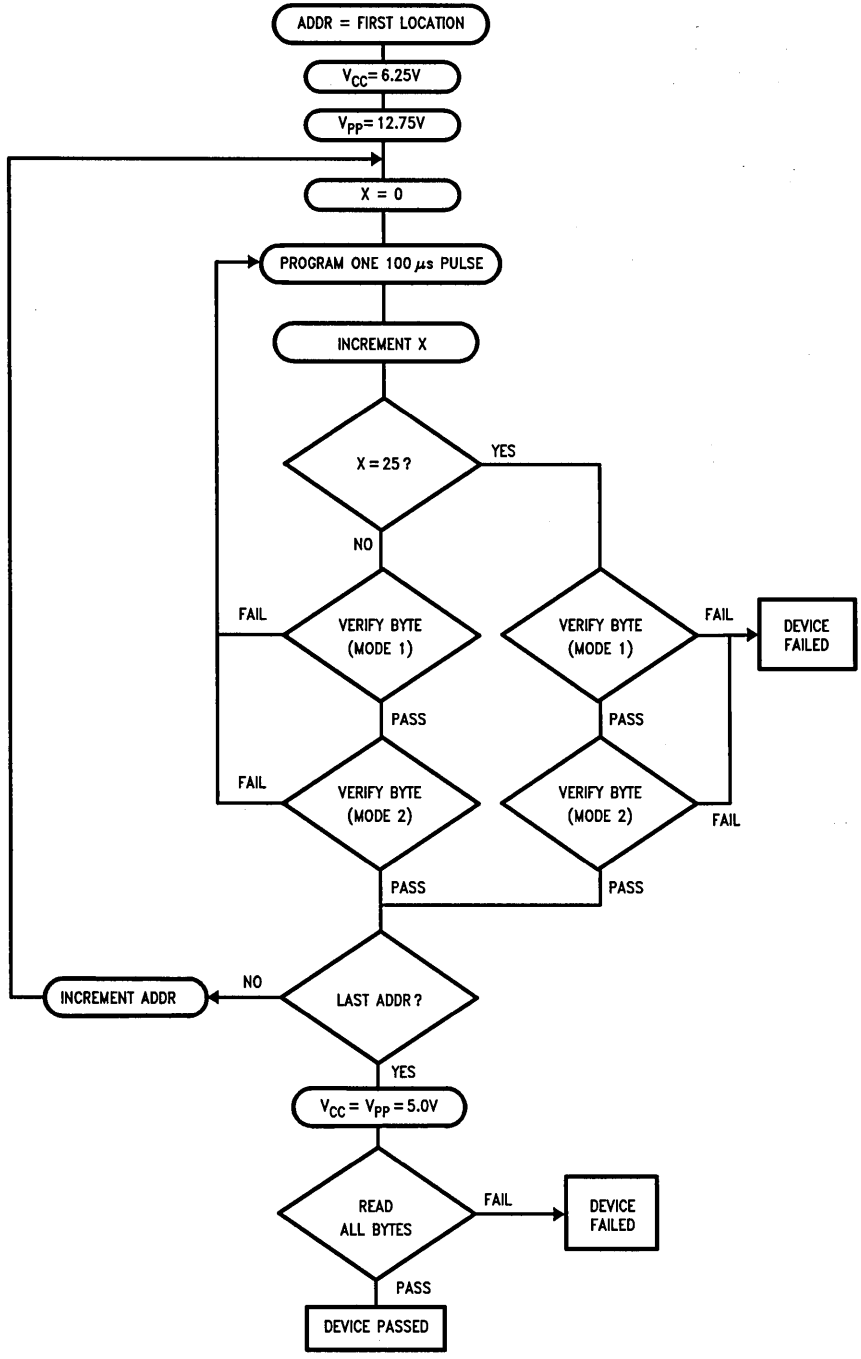
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast programming algorithm at typical power supply voltages and timings. The min and max limit parameters are design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart



TL/D/9185-6

FIGURE 1

Functional Description
Device Operation

The modes of operation of the NMC27C128C are listed in Table I. It should be noted that all inputs may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the programming modes and at 5V in the other modes. The V_{PP} pin must be at 12.75V in the programming and verify mode, and V_{IL} in the read mode.

Read Mode

The NMC27C128C has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$ is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs toe after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least tacc-toe. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C128C has a standby mode which reduces the active power dissipation by 98%, from 275 mW to 5.5 mW. The NMC27C128C is placed in standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Or-Tying

Because NMC27C128Cs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) complete assurance that output bus contention will not occur, and

b) the lowest possible memory power dissipation.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C128C. The NMC27C128C has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed either one or the other of the two transistors is programmed. When accessed, the memory cell will discharge one of the two data lines, providing a differential voltage. This differential signal is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state both transistors source the same current through the data lines and thus no differential is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs. The NMC27C128C is in the program and verify mode when V_{PP} is raised to 12.75V. To verify that a device is totally blank, the verify mode must be entered. In the verify mode each transistor of the memory cell is checked against a reference cell. By toggling $\overline{CE}$ both transistors in the cell are checked. For a totally unprogrammed device in the verify mode all outputs will be at a "1" state for $\overline{CE}$ = V_{IH} and at a "0" state for $\overline{CE}$ = V_{IL}.

During programming it is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address, clock, and data inputs are TTL.

When the addresses, clocks and data are stable, an active low, TTL program pulsed is applied to the $\overline{PGM}$ input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when data from both verify modes matches the input data. The NMC27C128C is programmed with the fast programming algorithm shown in *FIGURE 1*. Each address is programmed with a series of 100 μs pulses until the device verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C128C must not be programmed with a DC signal applied to the $\overline{PGM}$ input. Programming multiple NMC27C128Cs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C128Cs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input (with $\overline{CE}$ low and $\overline{OE}$ high) programs the paralleled NMC27C128Cs.

Program Inhibit

Programming multiple NMC27C128Cs in parallel with different data is also easily accomplished. Except for $\overline{PGM}$ all like inputs (including V_{PP}, $\overline{CE}$ and $\overline{OE}$) of the paralleled NMC27C128Cs may be common. A TTL low level applied to an NMC27C128Cs $\overline{PGM}$ input (with the other control pins at the appropriate levels) will program that NMC27C128C while keeping the same pin high on the others inhibits programming.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. A verify done in the read mode may not ensure that the bits have been programmed with adequate margins for reliable operation. To guarantee adequate margins the device should be verified in the verify mode. In this mode each transistor of the memory cell is checked against a reference cell. Verify

Program Verify (Continued)

mode is entered with V_{CC} at 6.25V V_{PP} at 12.75V, $\overline{OE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. $\overline{CE}$ is at V_{IH} and the data read for verify mode 1, and $\overline{CE}$ is at V_{IL} for verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell.

Manufacturer's Identification Code

The NMC27C128C has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C128C is "8383", where "83" designates that it is made by National Semiconductor, and "83" designates it as a 128k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL} and $\overline{PGM}$ is held at V_{IH}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Erasure Characteristics

The erasure characteristics of the NMC27C128C are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000Å–4000Å range. After programming opaque lables should be placed over the NMC27C128C's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C128C is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C128C should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C128C erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Mode Selection

Mode \ Pins	V_{PP} (1)	$\overline{OE}$ (22)	$\overline{CE}$ (20)	$\overline{PGM}$ (27)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{CC}	V_{IL}	V_{IL}	V_{IH}	5V	D_{OUT}
Standby	V_{CC}	Don't Care	V_{IH}	V_{IH}	5V	Hi-Z
Output Disable	V_{CC}	V_{IH}	Don't Care	V_{IH}	5V	Hi-Z
Program	V_{PP}	V_{IH}	V_{IL}	V_{IL}	6.25V	D_{IN}
Verify (Mode 1)	V_{PP}	V_{IL}	V_{IH}	V_{IH}	6.25V	D_{OUT} V_{OH} if Blank
Verify (Mode 2)	V_{PP}	V_{IL}	V_{IL}	V_{IH}	6.25V	D_{OUT} V_{OL} if Blank
Program Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	6.25V	Hi-Z

National Semiconductor

NMC27C256
262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256 is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

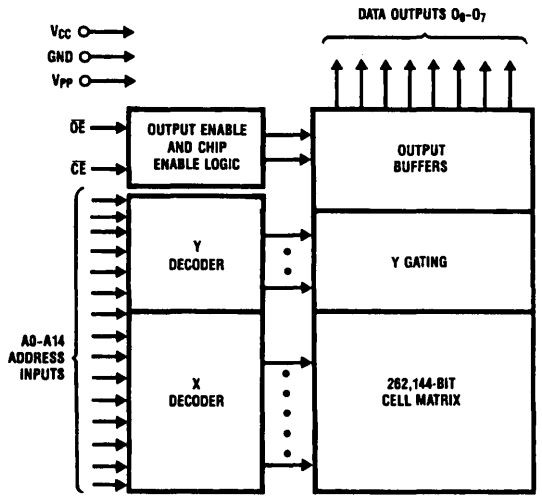
The NMC27C256 is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 170 ns
- Low CMOS power consumption
  - — Active power: 55 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C256QE), −40°C to +85°C, and military temperature range (NMC27C256QM), −55°C to +125°C, available
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems

Block Diagram



TL/D/7512–1

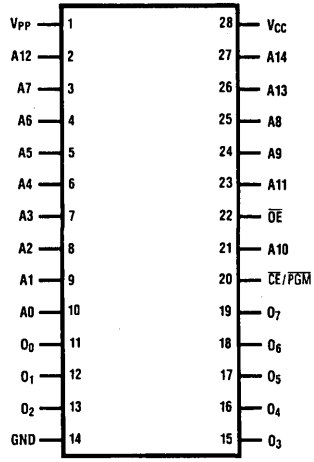
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256Q
Dual-In-Line Package



TL/D/7512–2

27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256 pins.

Order Number NMC27C256Q
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±5%

Parameter/Order Number	Access Time
NMC27C256Q17	170
NMC27C256Q20	200
NMC27C256Q25	250

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C256Q200	200
NMC27C256Q250	250
NMC27C256Q300	300

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C256QE200	200
NMC27C256QE250	250

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C256QM250	250
NMC27C256QM350	350

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C256Q17, 20, 25	5V ±5%
NMC27C256Q200, 250, 300	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256								Units
			Q17		Q20, Q200		Q25, Q250		Q300		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	60	0	105	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp Range
Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V

Operating Conditions (Note 7)

Temperature Range	
NMC27C256QE200, 250	−40°C to +85°C
NMC27C256QM250, M350	−55°C to +125°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OH} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256Q						Units
			E200		E250 M250		M350		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	105	ns

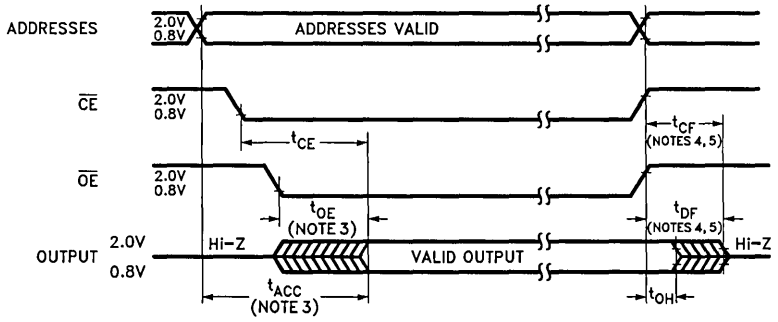
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7 & 9)



TL/D/7512-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

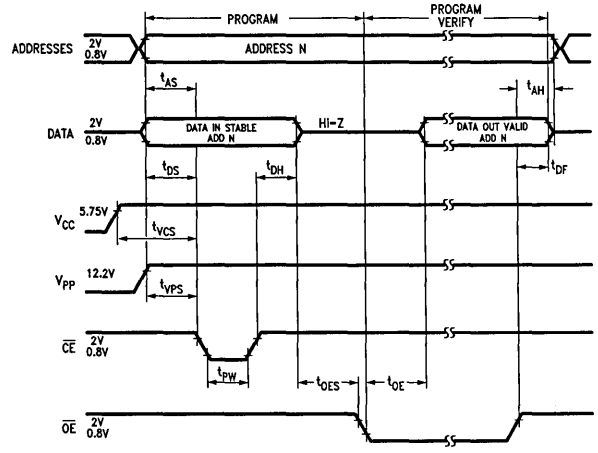
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

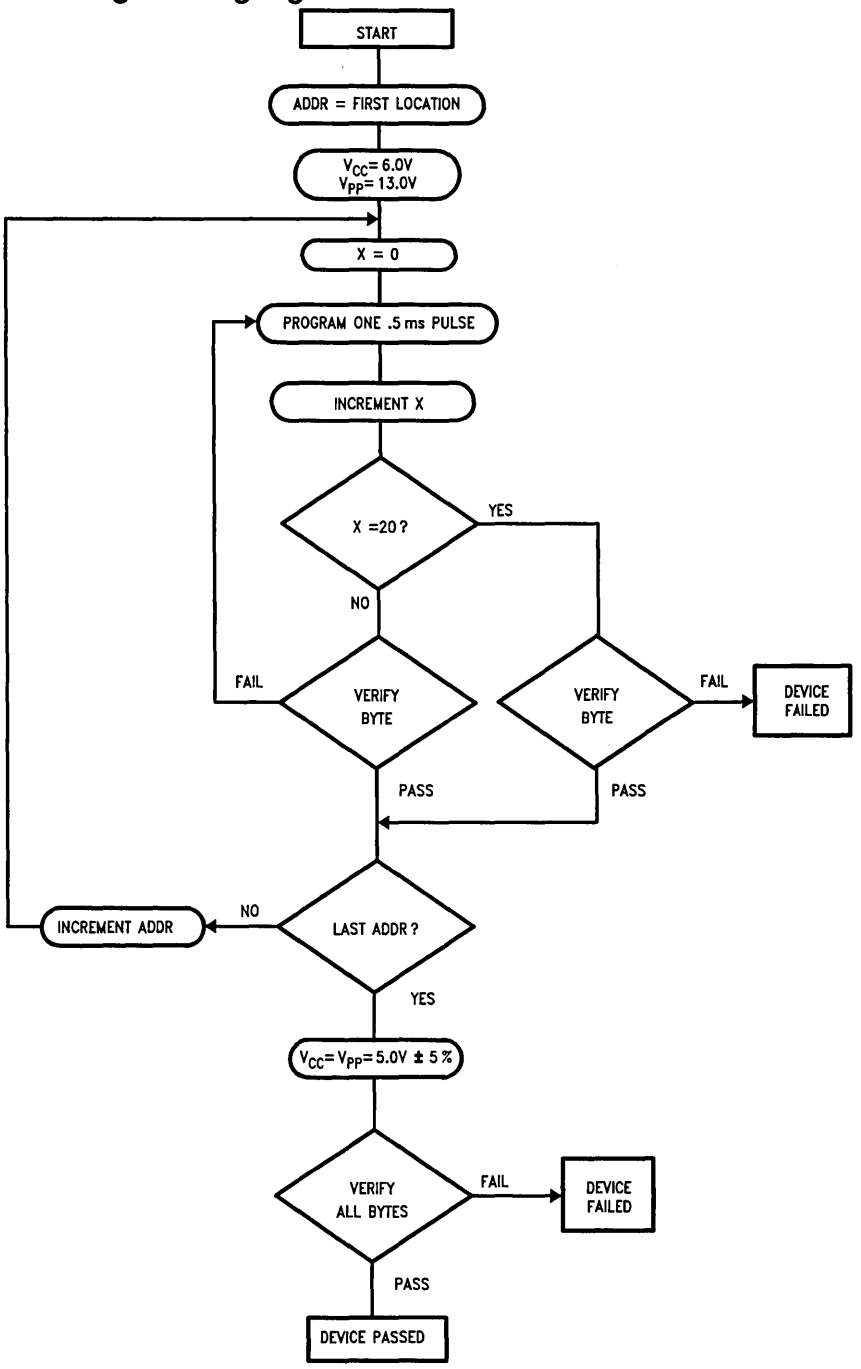
Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms (Note 3)



TL/D/7512–4

Interactive Programming Algorithm Flow Chart



TL/D/7512–5

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C256 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C256 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256.

Initially, and after each erasure, all bits of the NMC27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C256 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C256 must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27C256s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	13.0V	6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0V	6V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C256s may be common. A TTL low level program pulse applied to an NMC27C256's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 13.0V will program that NMC27C256. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C256's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C256 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C256 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C256B High Speed Version 262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256B/87C256B is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256B/87C256B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military temperature ranges.

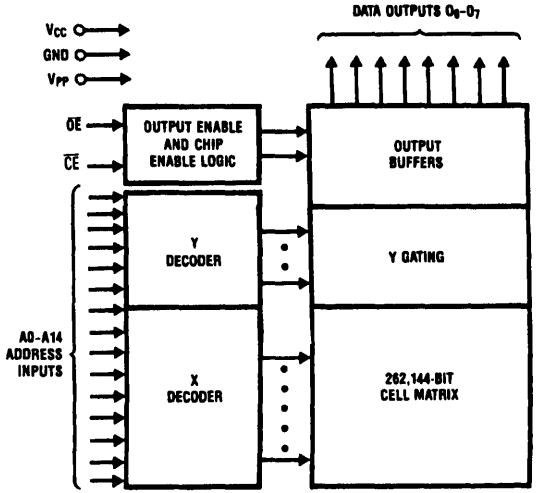
The NMC27C256B/87C256B is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Optimal EPROM for total CMOS systems
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C256BQE), −40°C to +85°C, and military temperature range (NMC27C256BQM), −55°C to +125°C, available
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation for NMC27C256B—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9125–1

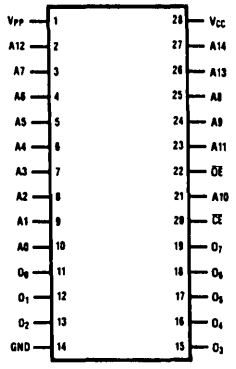
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256BQ
Dual-In-Line Package



TL/D/9125-2

27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256B pins.

Order Number NMC27C256BQ
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQ120	120
NMC27C256BQ150	150
NMC27C256BQ200	200
NMC27C256BQ250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQE120	120
NMC27C256BQE150	150
NMC27C256BQE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQM150	150
NMC27C256BQM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

V_{CC} Power Supply	5V ±10%
Temperature Range	0°C to +70°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1.0	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B								Units
			Q120		Q150		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55		60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

V_{CC} Power Supply	5V ±10%
Temperature Range	
NMC27C256BQE120	−40°C to +85°C
NMC27C256BQM150	−55°C to +125°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B						Units
			QE120		QE150, QM150		QE200, QM200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

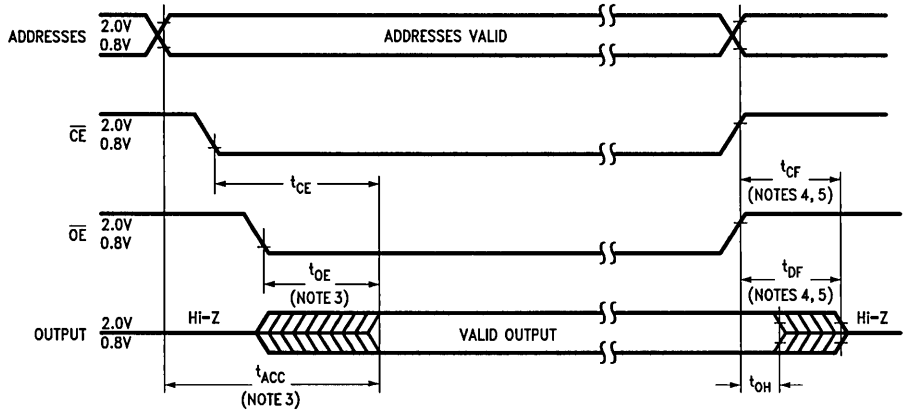
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9125-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

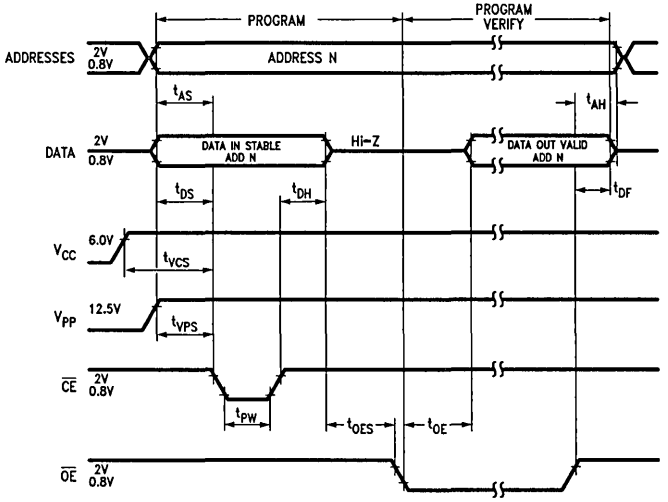
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



TL/D/9125-5

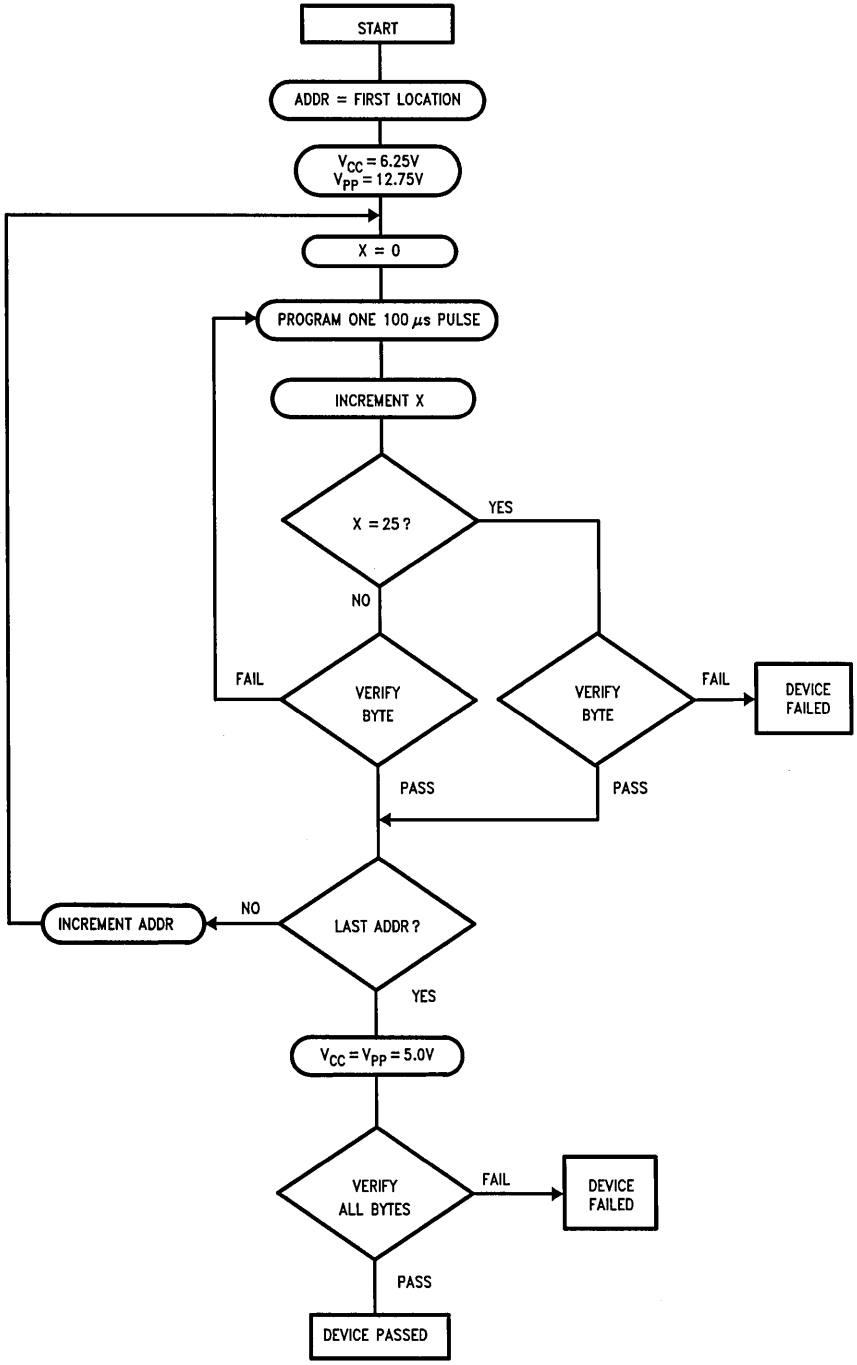
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart (Note 4)



TL/D/9125–7

FIGURE 1

Interactive Programming Flow Chart (Note 4)

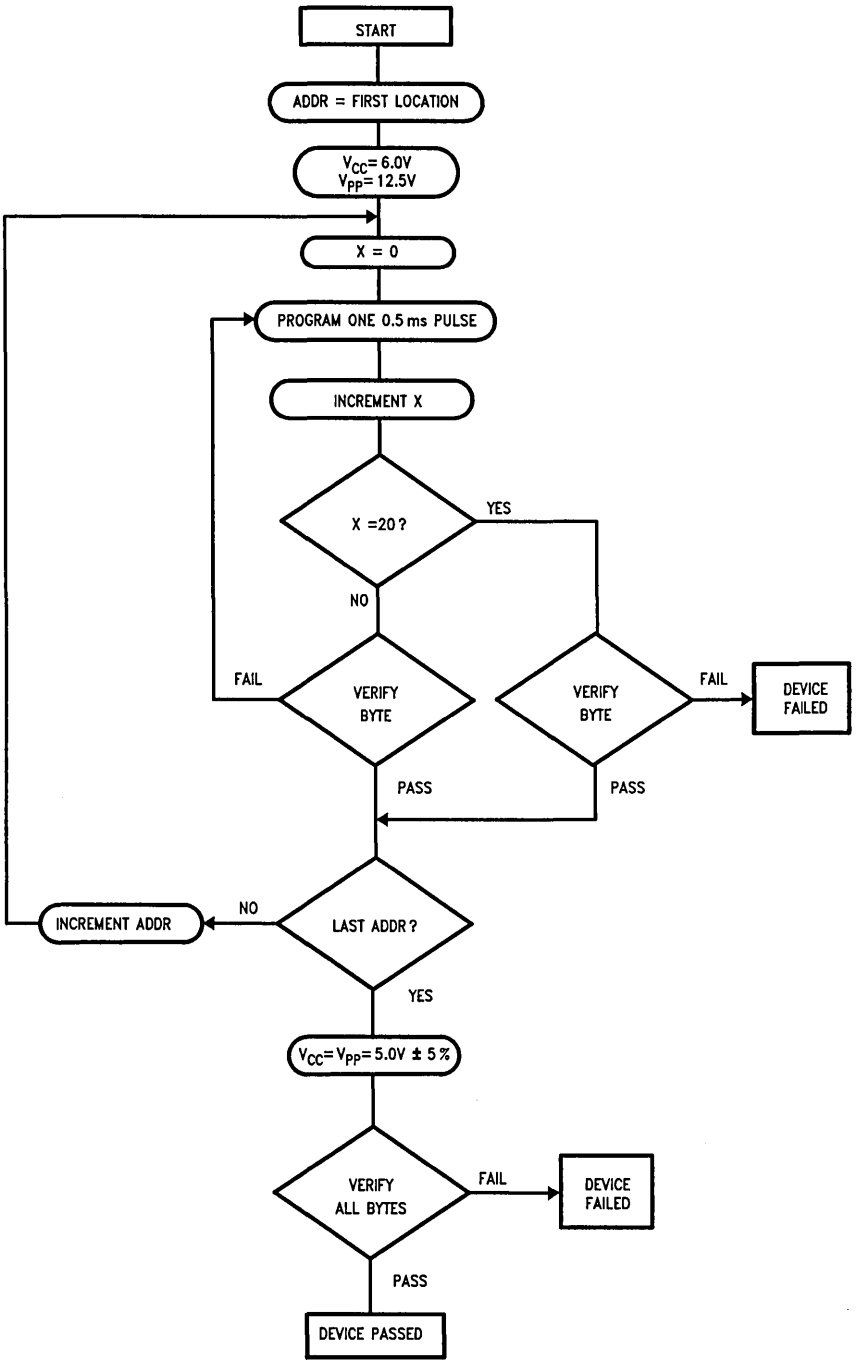


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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256B are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C256B has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256B.

Initially, and after each erasure, all bits of the NMC27C256B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C256B is programmed with the Fast Programming Algorithm shown in *Figure 1.* Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C256B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (ALE)* (20)	$\overline{OE}$ (22)	V_P (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Programming multiple NMC27C256Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C256B.

Program Inhibit

Programming multiple NMC27C256Bs in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C256Bs may be common. A TTL low level program pulse applied to an NMC27C256B $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC27C256B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C256B has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C256B is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C256B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C256B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NMC27C256B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C256BN
High Speed Version 262,144-Bit (32k x 8) One-Time Programmable CMOS PROM

General Description

The NMC27C256BN is a high-speed 256k one-time programmable CMOS PROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C256BN is designed to operate with a single +5V power supply with ±10% tolerance.

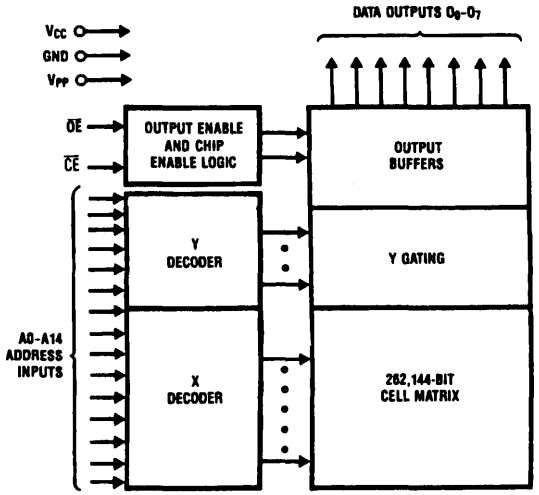
The NMC27C256BN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with NMOS 256k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation for NMC27C256B—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9691-1

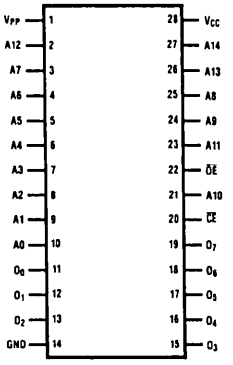
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256BN
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256BN pins.

Order Number NMC27C256BN
See NS Package Number N28B

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BN120	120
NMC27C256BN150	150
NMC27C256BN200	200
NMC27C256BN250	250

Note: For non-commercial temperature range parts, call factory.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256BN								Units
			120		150		200		250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

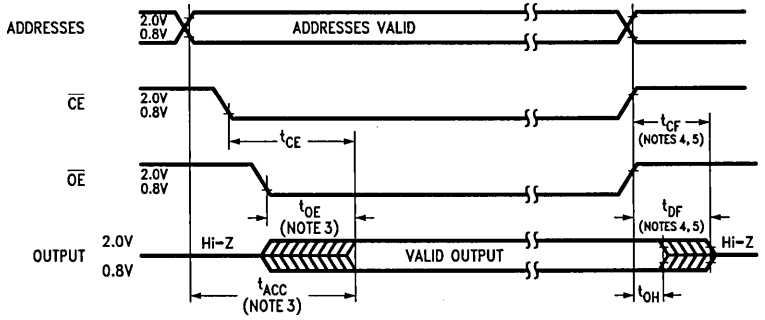
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/9691–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

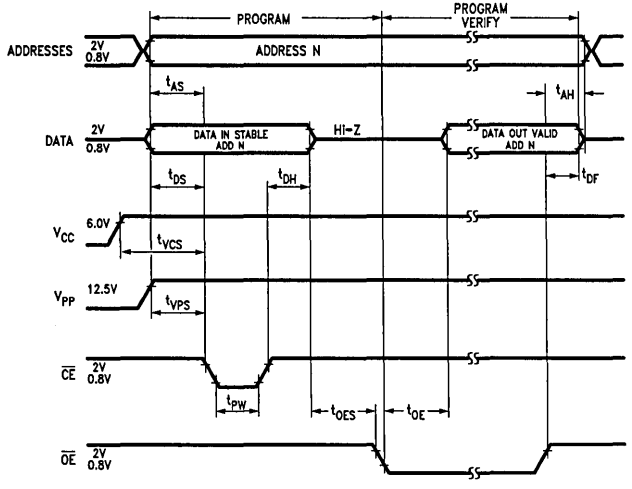
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	ns
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	ns

Programming Waveforms



TL/D/9691–4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart (Note 4)

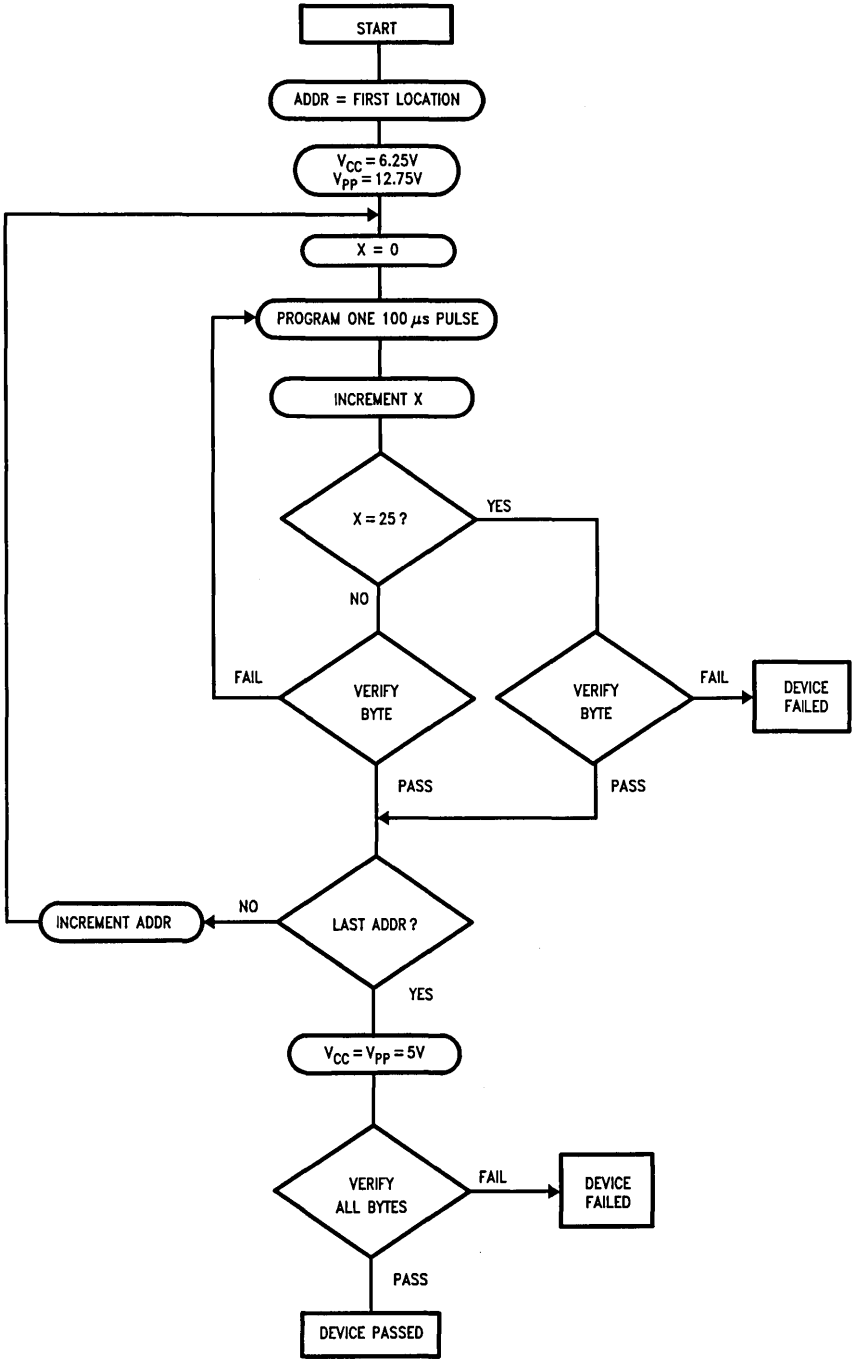


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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

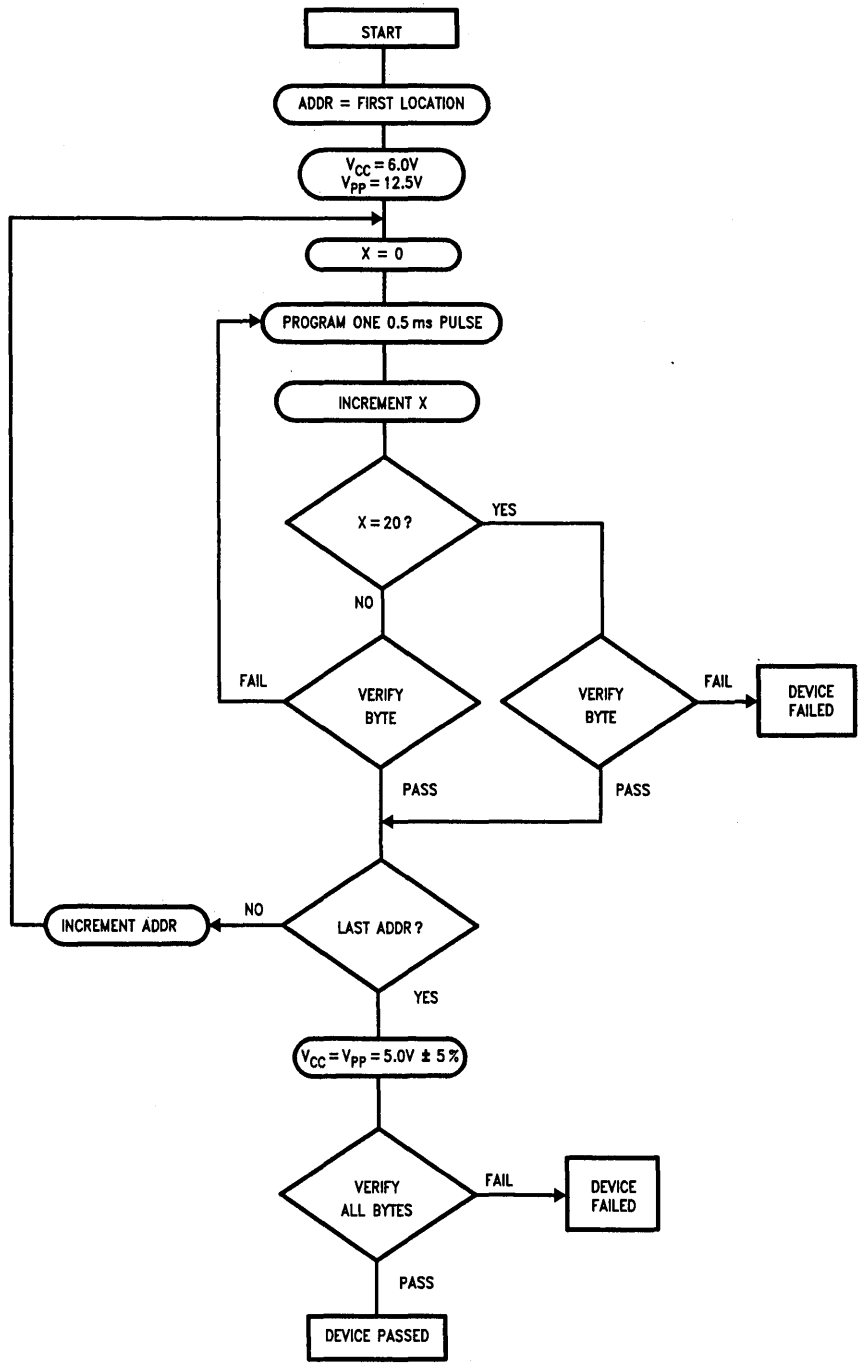

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C256BN are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C256BN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C256BN has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C256BN is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256BN are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256BN.

Initially, and after each erasure, all bits of the NMC27C256BN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256BN is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C256BN is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C256BN must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Note: Some program manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

Programming multiple NMC27C256BNs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256BNs may be connected together when they are programmed with the same data. A low level

1

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_P (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C256BNs.

The NMC27C256BN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C256BQ UV erasable PROM in a windowed package should be used.

Program Inhibit

Programming multiple NMC27C256BNs in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C256BNs may be common. A TTL low level program pulse applied to an NMC27C256BNs $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC27C256BN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256BNs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C256BN has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C256BN is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 12.0V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$5°C.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

National Semiconductor

PRELIMINARY

NMC27C256C 262,144-Bit (32k x 8) UV Erasable CMOS PROM (Very High Speed Version)

General Description

The NMC27C256C is a high-speed 256k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256C is designed to operate with a single +5V power supply with 10% tolerance.

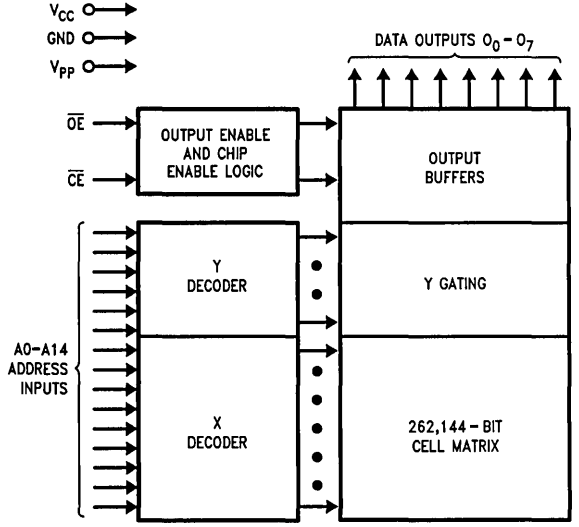
The NMC27C256C is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and two transistor memory cell for fast access time down to 55 ns
- Low CMOS power consumption
  - — Active power: 275 mW max
  - — Standby power: 5.5 mW max
- Performance compatible to current high speed microprocessors
- Pin compatible with standard CMOS and NMOS EPROMS
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/9692-1

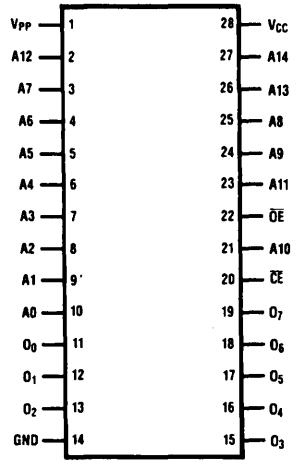
Pin Names

Pin Name	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C256CQ
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256CQ pins.

Order Number NMC27C256CQ
See NS Package Number J28AQ

Commercial Temp Range (0°C to 70°C) V_{CC} = 5V ±10%

Parameter/ Order Number	Access Time (ns)
NMC27C256CQ55	55
NMC27C256CQ70	70
NMC27C256CQ90	90

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{CC} Supply Voltage and A9 with Respect to Ground	+7.0V to −0.6V
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 20 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 20 MHz Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = 2.40V$		2	5	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	1.0	mA
V_{IL}	Input Low Voltage	(Note 10)	−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 7)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 7)	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256C						Units
			Q55		Q70		Q90		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$		55		70		90	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		55		70		90	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		25		30		40	ns
t_{DF} (Note 2)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	25	0	30	0	40	ns
t_{CF} (Note 2)	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	25	0	30	0	40	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Input Rise and Fall Times ≤5 ns

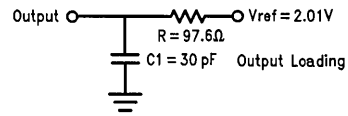
Input Pulse Levels 0V to 3.0V

Output Load is 97.6Ω between All Outputs and 2.01V, C_L = 30 pF (Note 8)

Timing Measurement Reference Level

Inputs 0.8V and 2V

Outputs 0.8V and 2V



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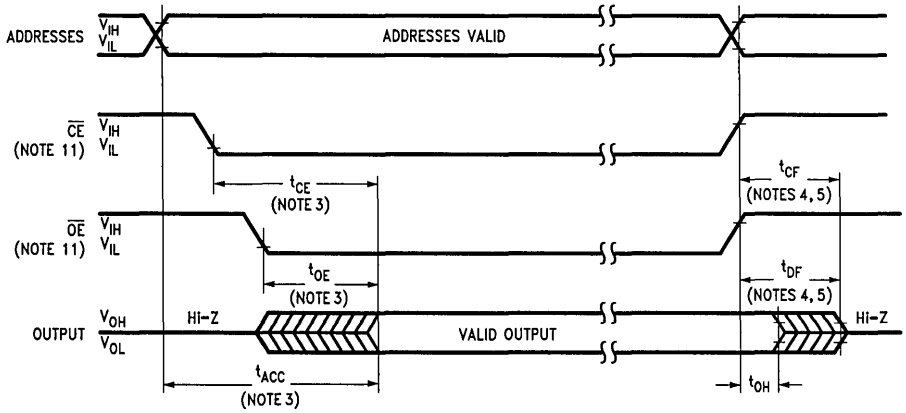
AC Waveforms (Notes 6, 7, 9)



TL/D/9692–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be to $t_{ACC} - t_{OE}$ after address change without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: C_L: 30 pF includes fixture capacitance.

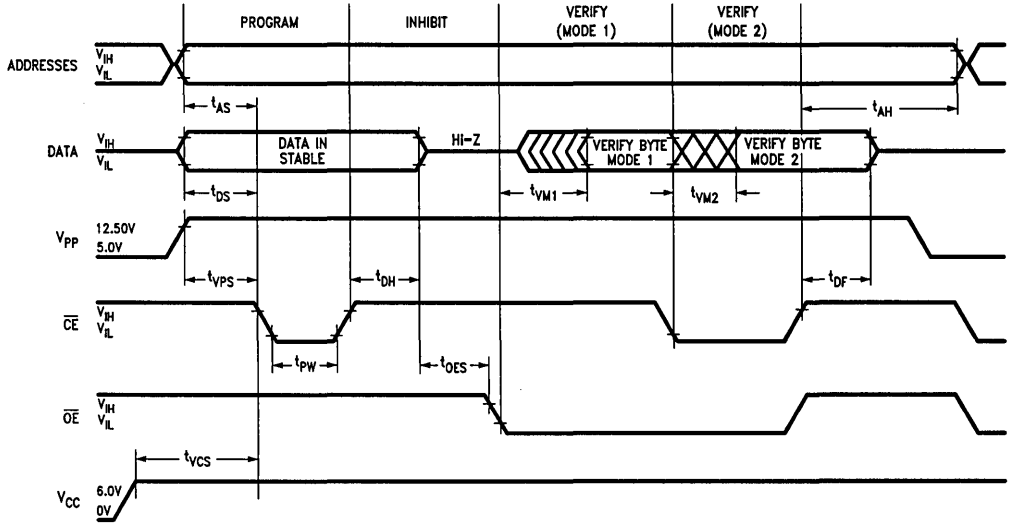
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot −2.0V for a maximum of 20 ns.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	(Notes 5, 6)	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V
t_{VM1}	Data Valid from $\overline{OE}$ (Verify Mode 1)	$V_{PP} = V_{PP}$ $\overline{CE} = V_{IH}$			0.1	μs
t_{VM2}	Data Valid from $\overline{CE}$ (Verify Mode 2)	$V_{PP} = V_{PP}$ $\overline{OE} = V_{IL}$			0.1	μs

Programming Waveforms (Note 4)



TL/D/9692–5

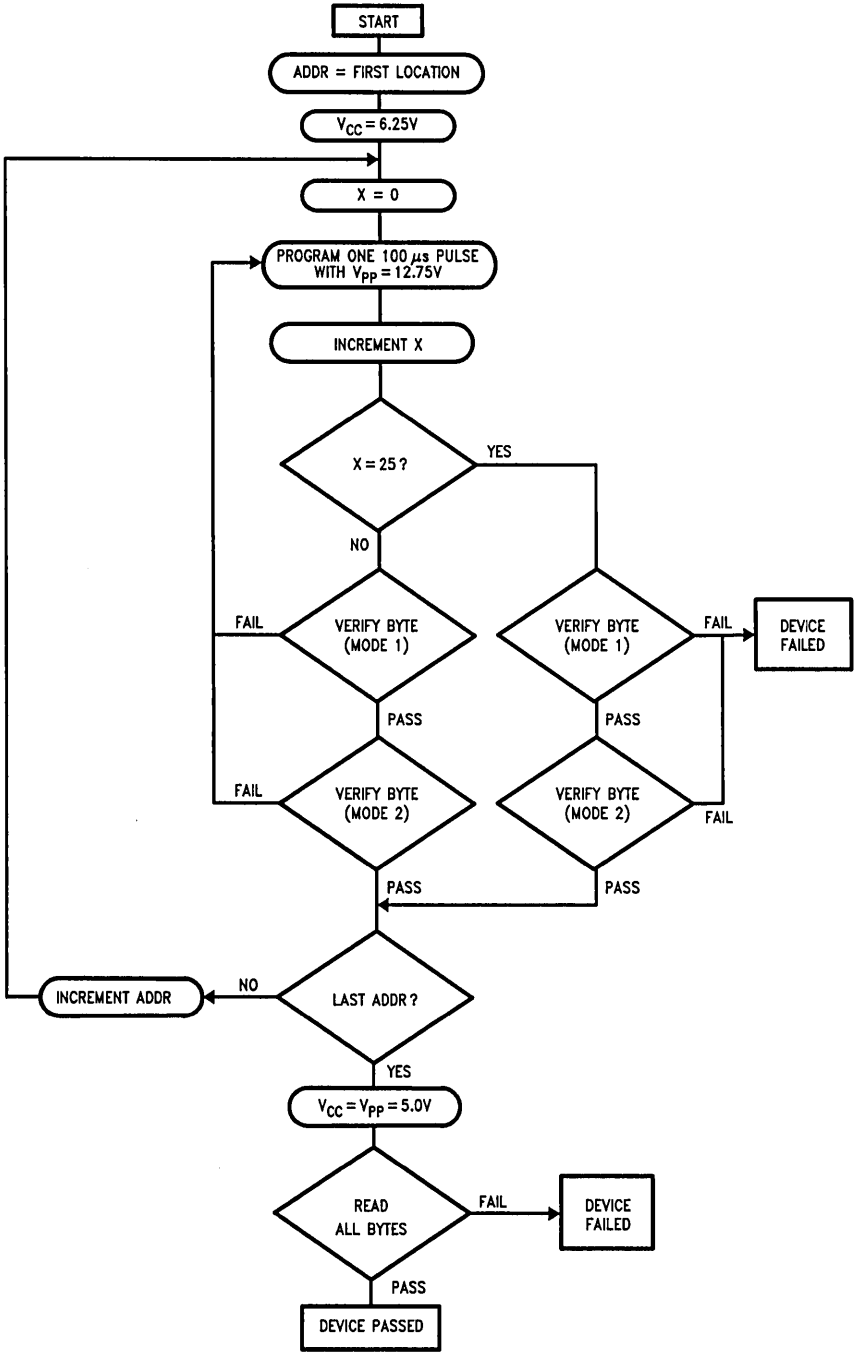
Note 1: National's standard product warranty applies only to devices programmed to the specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NSC27C256CQ must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Programming Algorithm at typical power supply voltages and timings. The Min and Max limit parameters are design parameters, not tested or guaranteed.

Fast Programming Algorithm Flow Chart



TL/D/9692–6

FIGURE 1

Functional Description

DEVICE OPERATION

The modes of operation of the NMC27C256C are listed in Table I. It should be noted that all inputs for the modes may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the programming modes and at 5V in the other modes. The V_{PP} pin must be at 12.75V in the programming and verify mode, and V_{CC} in the read mode.

READ MODE

The NMC27C256C has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

STANDBY MODE

The NMC27C256C has a standby mode which reduces the active power dissipation from 275 mW to 5.5 mW. The NMC27C256C is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because NMC27C256s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a. The lowest possible memory power dissipation, and

b. Complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (Pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (Pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING

CAUTION: Exceeding 14V on Pin 1 (V_{PP}) will damage the NMC27C256C. The NMC27C256C has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed either one or the other of the two transistors is programmed. When accessed the memory cell will discharge one of the two data lines, providing a differential voltage. This differential signal is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state both transistors source the same current through the data lines and thus no differential is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs. To verify that a device is totally blank, the verify mode must be entered. In the verify mode each transistor of the memory cell is checked against a reference cell. By toggling $\overline{CE}$ both transistors in the cell are checked. For a totally unprogrammed device in the verify mode all outputs will be at a "1" state for $\overline{CE} = V_{IH}$ and at a "0" state for $\overline{CE} = V_{IL}$.

The NMC27C256C is in the program mode when V_{PP} is raised to 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address, clock, and data inputs are TTL.

When the addresses, clocks, and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when data from both verify modes matches input

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13) (15–19)
Read	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Standby	V_{IH}	Don't Care	5.0V	5.0V	Hi-Z
Output Disable	V_{IL}	V_{IH}	5.0	5.0	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Verify (Mode 1)	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT} V_{OH} if Blank)
Verify (Mode 2)	V_{IL}	V_{IL}	12.75V	6.25V	D_{OUT} V_{OL} if Blank)
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

data. The NMC27C256C is programmed with the fast programming algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C256C must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C256C in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256C may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input (with $\overline{OE}$ high) programs the paralleled NMC27C256Cs.

PROGRAM INHIBIT

Programming multiple NMC27C256Cs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including V_{PP} and $\overline{OE}$) of the paralleled NMC27C256Cs may be in common. A TTL low level applied to an NMC27C256C's $\overline{CE}$ input (with the other control pins at the appropriate levels) will program that NMC27C256C while keeping the same pin high on the others inhibits programming.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. A verify done in the read mode may not ensure that the bits have been programmed with adequate margins for reliable operation. To guarantee adequate margins the device should be verified in the verify mode. In this mode each transistor of the memory cell is checked against a reference cell. Verify mode is entered with V_{PP} at 12.75V and $\overline{OE}$ at V_{IL}. $\overline{CE}$ is at V_{IH} and the data read for verify Mode 1, and at V_{IL} for verify Mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C256C has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C256C is "8304", where "83" designates that it is made by National Semiconductor, and "04" designates it is a 256k part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A13, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C $\pm$5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256C are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the NMC27C256C's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256C is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15 Wsec/cm^2.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Functional Description (Continued)

The NMC27C256C should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C256C erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled as the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

TABLE III. Minimum NMC27C256C Erasure Time

Light Intensity (μW/cm**2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

National Semiconductor

PRELIMINARY

NMC27C512A
524,288-Bit High Speed Version (64k x 8) UV Erasable CMOS PROM

General Description

The NMC27C512A is a high-speed 512k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C512A is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

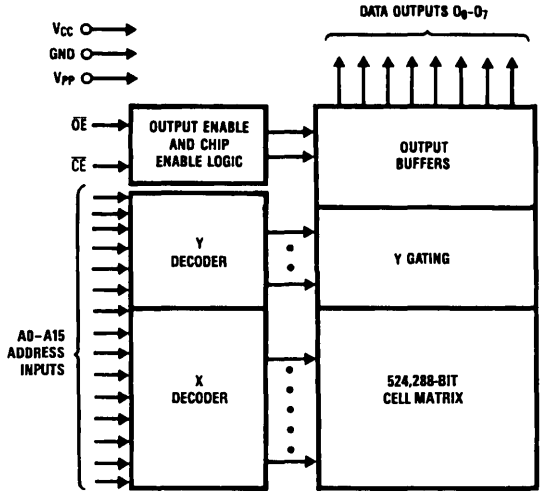
The NMC27C512A is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Optimum EPROM for total CMOS system
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C512AQE), −40°C to 85°C, and military temperature range (NMC27C512AQM), −55°C to 125°C, available
- Pin compatible with NMOS 512k EPROMS
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control.
- High current CMOS level output drivers

Block Diagram



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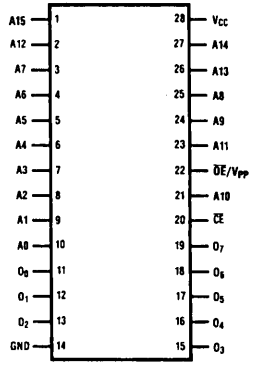
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C512AQ
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/V_{PP}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Order Part Number NMC27C512AQ
See NS Package Number J28AQ

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512A pins.

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQ120	120
NMC27C512AQ150	150
NMC27C512AQ200	200
NMC27C512AQ250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQE120	120
NMC27C512AQE150	150
NMC27C512AQE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQM150	150
NMC27C512AQM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A_9 & $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
ESD Rating (Mil. Std. 883C, Method 3015.2)	2000V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}/V_{PP}$ Supply Voltage & A_9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{PP}	V_{PP} Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A								Units
			Q120		Q150		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 & $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}/V_{PP}$ Supply Voltage & A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
ESD Rating (Mil. Std. 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range	
NMC27C256BQE120, 150, 200	−40°C to +85°C
NMC27C256BQM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A						Units
			QE120		QE150, QM150		QE200, QM200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

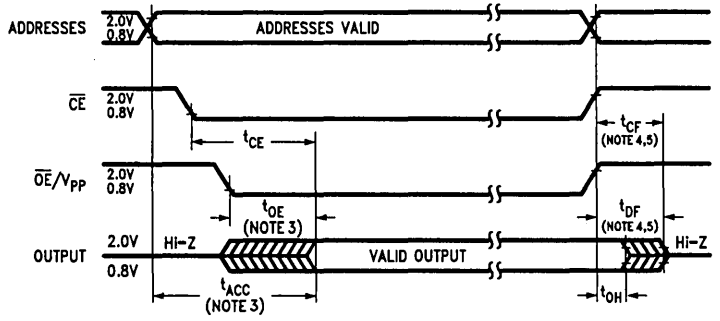
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7)



TL/D/9181-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{cf}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
T_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2	V

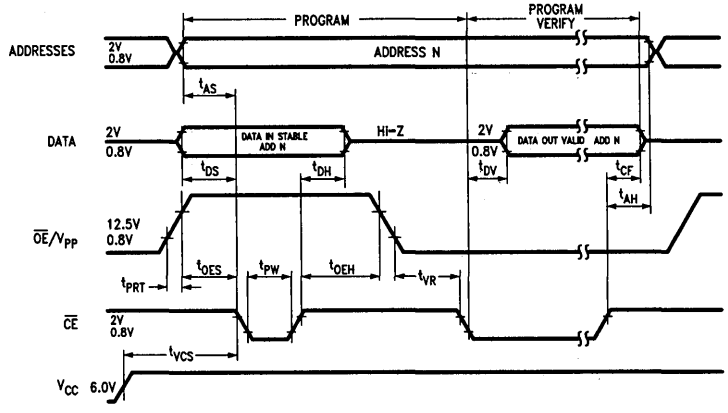
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max limit parameters are design parameters, not tested or guaranteed.

Programming Waveforms



TL/D/9181–5

Fast Programming Algorithm Flow Chart (Note 4)

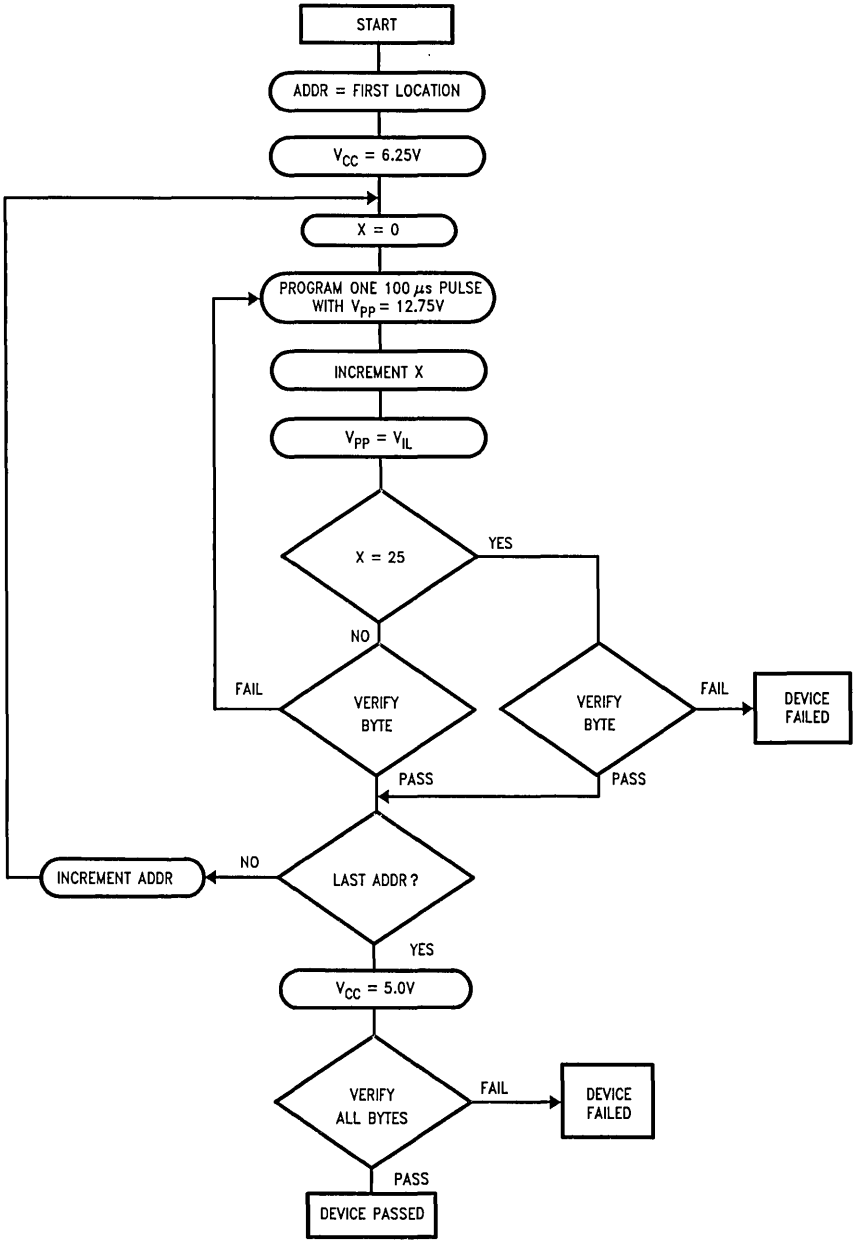


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FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)

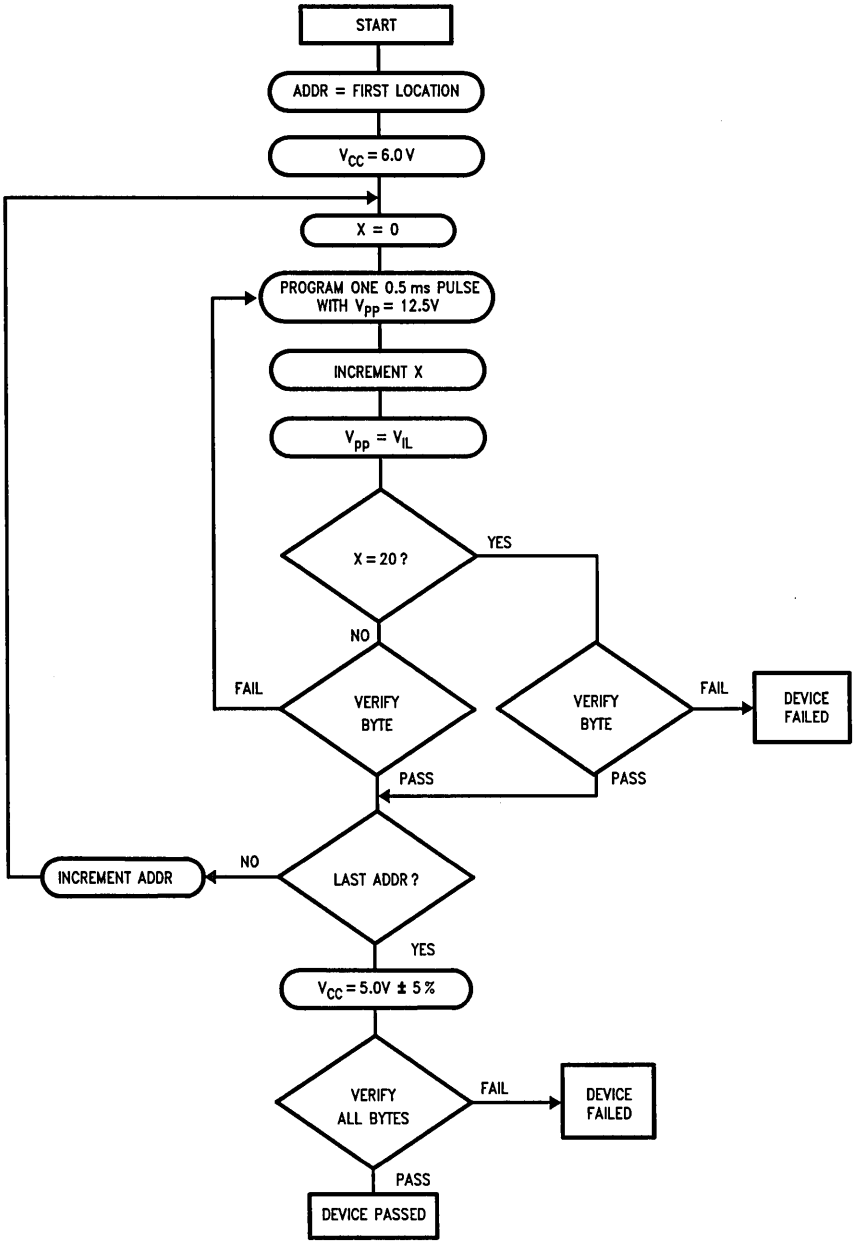

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FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C512A are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C512A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C512A has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C512A is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C512A are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the NMC27C512A.

Initially, and after each erasure, all bits of the NMC27C512A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512A is in the programming mode when the $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed.

The NMC27C512A is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

The NMC27C512A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C512AS in parallel with the same data can be easily acccomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512A may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C512A.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Standby	V_{IH}	Don't Care	5.0V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5.0V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C512A in parallel with different data is also easily accomplished. Except $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C512A may be common. A TTL low level program pulse applied to an NMC27C512A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C512A. A TTL high level $\overline{CE}$ input inhibits the other NMC27C512A from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Manufacturer's Identification Code

The NMC27C512A has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C512A is, "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A9 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C512A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NMC27C512A's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C512A is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C512A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C512A erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IL}	1	0	0	0	0	1	0	1	85

TABLE III. Minimum NMC27C512A Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C512AN 524,288-Bit (64k x 8) One Time Programmable CMOS PROM

General Description

The NMC27C512AN is a high-speed 512k UV one time programmable CMOS EPROM, ideally suited for applications where fast turnaround and low power consumption are important requirements.

The NMC27C512AN is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

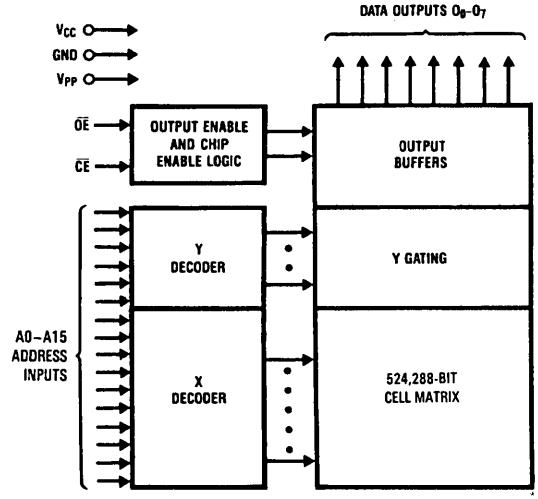
The NMC27C512AN is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once. Also the plastic molded package works well in auto insertion equipment used in automated assembly lines.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 120 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 0.55 mW max
- Optimum EPROM for total CMOS systems
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible with NMOS 512k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



TL/D/8754-1

Pin Names

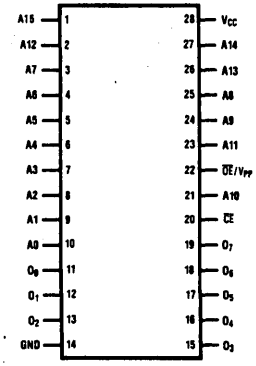
A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C512AN
Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/V_{PP}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Order Number NMC27C512AN
See NS Package Number N28B

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512AN pins.

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AN120	120
NMC27C512AN150	150
NMC27C512AN200	200
NMC27C512AN250	250

Note: For non-commercial temperature range parts, call the factory.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
V_{CC} Supply Voltage with with Respect to Ground	+7.0V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC} +1 to GND −0.6V
$\overline{OE}/V_{PP}$ Supply Voltage and A9 with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Std. 883C, Method 3015.2)	2000V

Operating Conditions (Note 6)

Temperature Range NMC27C512AN120, 150, 200, 250	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A								Units
			Q120		Q150		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		50		60		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

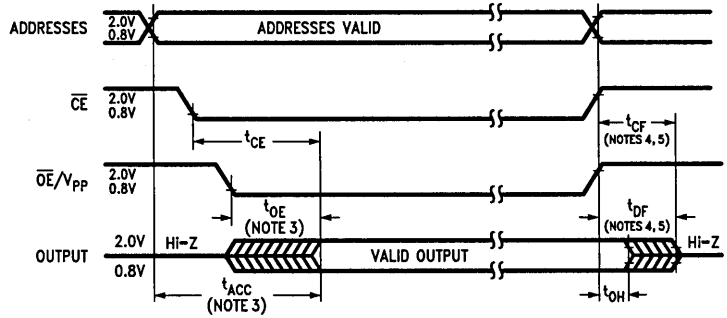
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	16	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V.

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} +1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

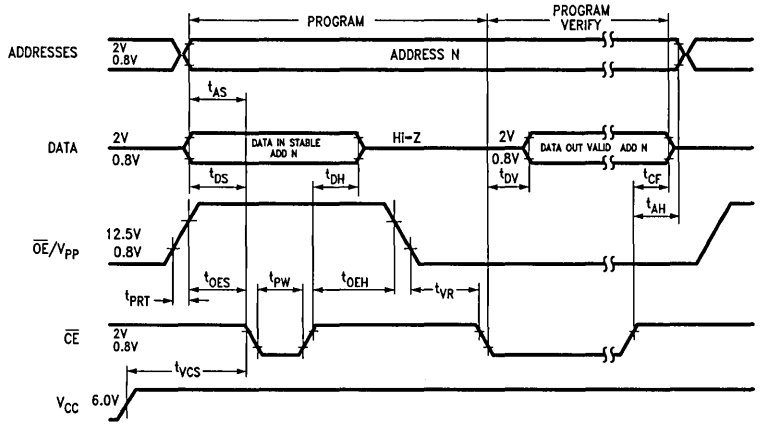
CL: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V
t_{VCS}	V_{CC} Setup Time		1			μs

Programming Waveforms



TL/D/8754-4

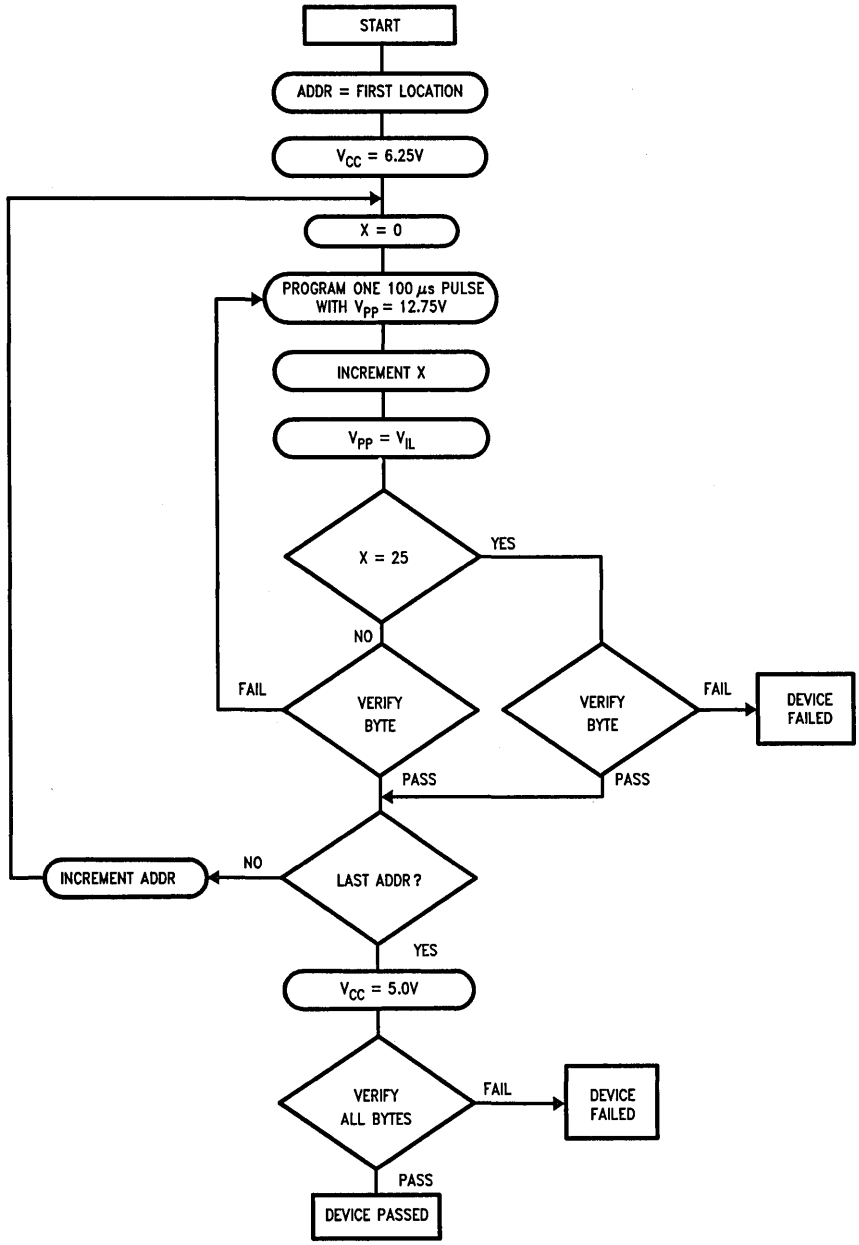
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings. The Min and Max Limit Parameters are design parameters, not tested or guaranteed.

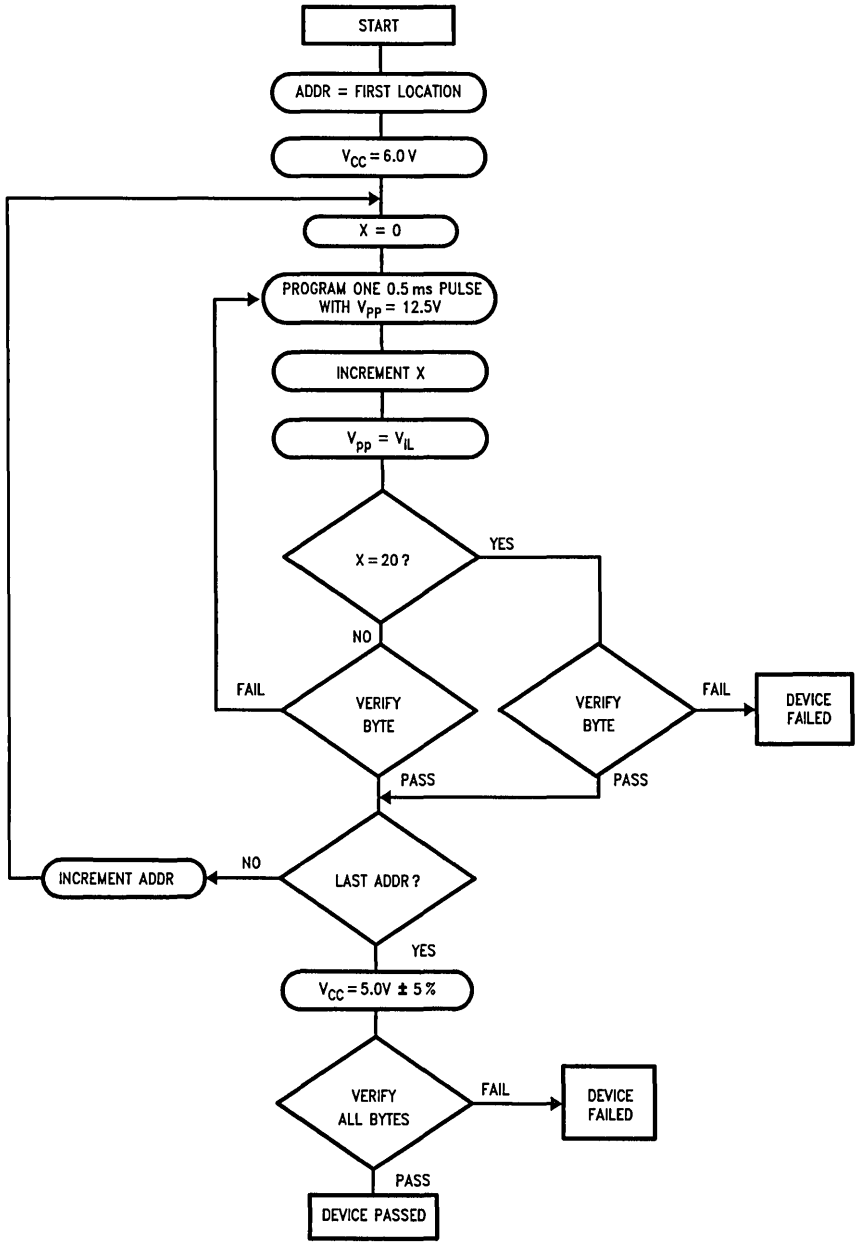
Fast Programming Algorithm Flow Chart (Note 4)



TL/D/8754–5

FIGURE 1

Interactive Programming Algorithm Flow Chart (Note 4)



TL/D/8754–6

FIGURE 2

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C512AN are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C512AN has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C512AN has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C512AN is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the NMC27C512AN.

Initially, and after each erasure, all bits of the NMC27C512AN are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512AN is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μ pulse.

Note: Some programmer manufacturers due to equipment limitation may offer interactive program Algorithm (shown in *Figure 2*).

The NMC27C512AN must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C512As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512AN may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C512AN.

The NMC27C512AN is packaged in a plastic molded package which does not have a transparent lid. Therefore the memory cannot be erased. This means that after a user has programmed a memory cell to a "0" it cannot be changed back to a "1".

If an application requires erasing and reprogramming, the NMC27C512AQ UV Erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Standby	V_{IH}	Don't Care	5.0V	Hi-Z
Output Disable	Don't Care	V_{IH}	5.0V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z

Functional Description (Continued)

PROGRAM INHIBIT

Programming multiple NMC27C512ANs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C512AN may be common. A TTL low level program pulse applied to an NMC27C512A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C512AN. A TTL high level $\overline{CE}$ input inhibits the other NMC27C512A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C512AN has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for NMC27C512AN is "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$ and $\overline{OE}$ are held at V_{IL}. Address A9 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the eight data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

National Semiconductor

PRELIMINARY

NMC27C010 (Former NMC27C1023)* 1,048,576-Bit (128k x 8) UV Erasable CMOS PROM

General Description

The NMC27C010 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C010 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

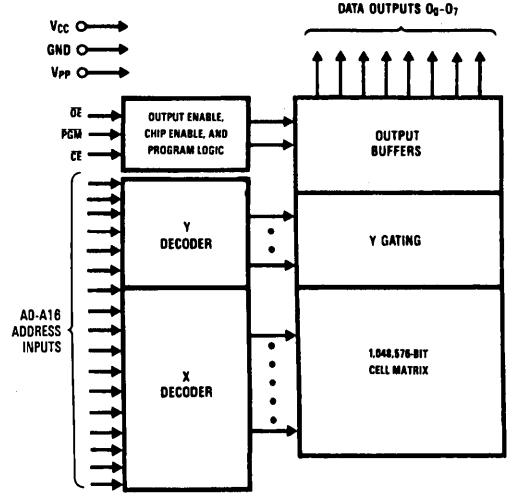
The NMC27C010 is packaged in a 32-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C010QE), −40°C to +85°C and military temperature range (NMC27C010QM), −55°C to +125°C, available
- Pin compatible with NMOS bytewide 1024k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



*Some programmer manufacturers will call this device NMC27C1023.

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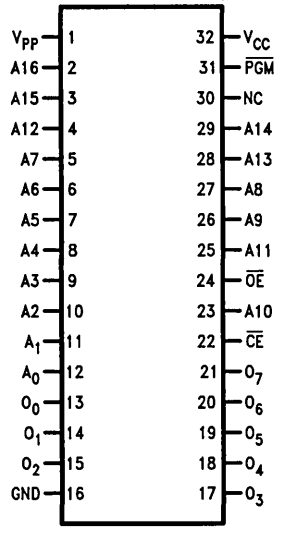
Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

NMC27C010Q
Dual-In-Line Package

27C512 27512	27C256 27256	27C128 27128	27C64 2764
A15	V_{PP}	V_{PP}	V_{PP}
A12	A12	A12	A12
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND



27C64 2764	27C128 27128	27C256 27256	27C512 27512
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$	A14	A14
NC	A13	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C010 pins.

Order Number NMC27C010Q
See NS Package Number J32AQ

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C010Q150	150
NMC27C010Q170	170
NMC27C010Q200	200
NMC27C010Q250	250

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C010QE170	170
NMC27C010QE200	200
NMC27C010QE200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C010QM170	170
NMC27C010QM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C010								Units
			Q150		Q170		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C010QE120, 150, 200	−40°C to +85°C
NMC27C010QM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C010Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

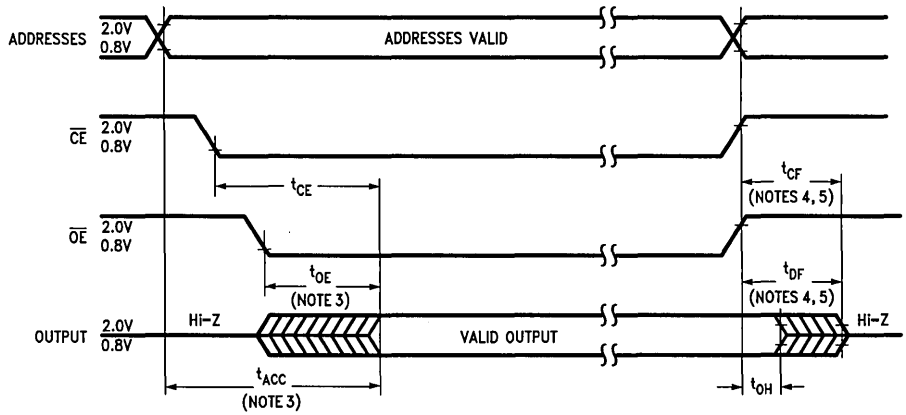
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

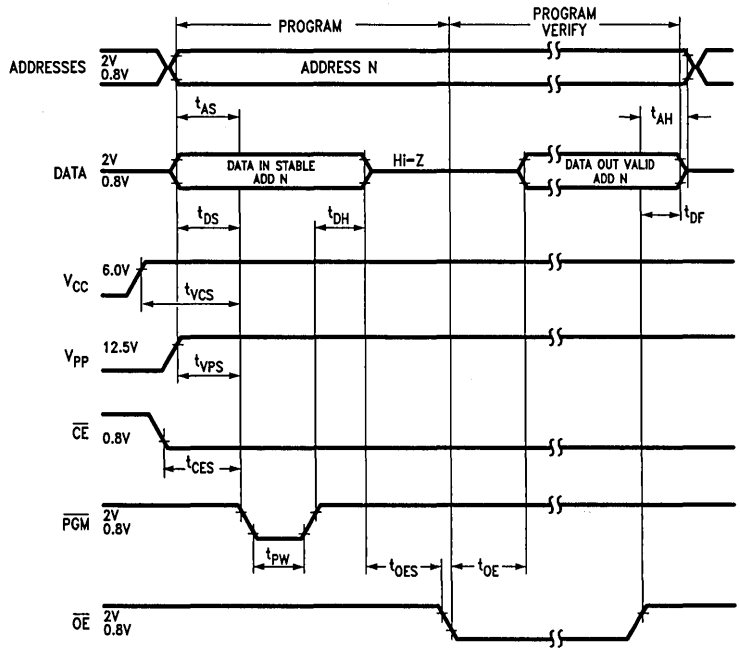
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max limit parameters are design parameters, not tested or guaranteed.

Fast Programming Algorithm Flow Chart

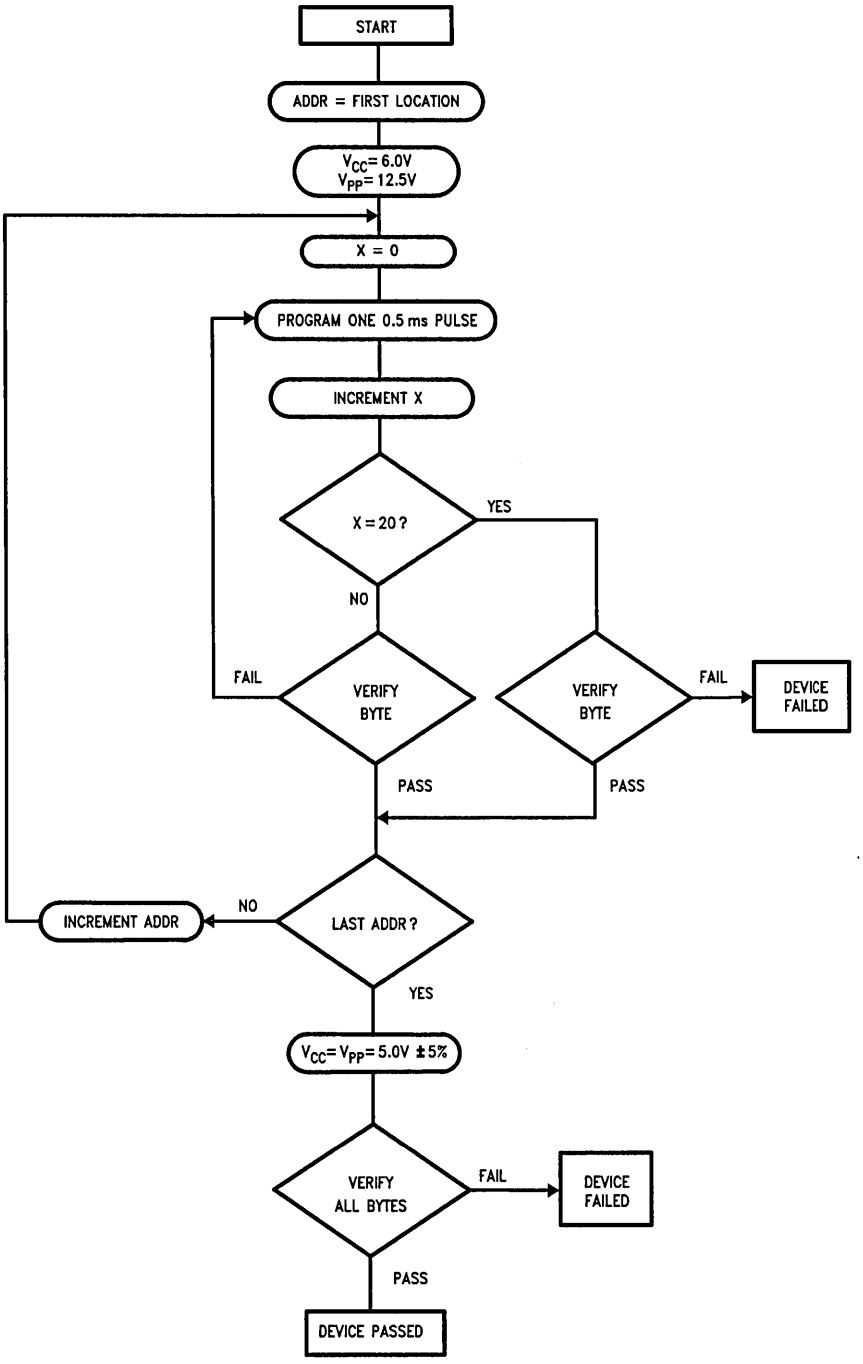

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C010 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C010 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the specified voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C010 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C010 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because the NMC27C010 is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C010.

Initially, and after each erasure, all bits of the NMC27C010 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C010 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C010 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C010 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C010 in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C010 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C010.

Program Inhibit

Programming multiple NMC27C010's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C010 may be common. A TTL low level program pulse applied to an NMC27C010's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C010. A TTL high level $\overline{CE}$ input inhibits the other NMC27C010's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

Manufacturer's Identification Code

The NMC27C010 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1Megabit byte-wide part.

Functional Description (Continued)

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13–15, 17–21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

TABLE II. Manufacturer's Identification Code

Pins	A_0 (12)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	1	0	86

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C010 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

AFTER PROGRAMMING

Opaque labels should be placed over the NMC27C010 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C010 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C010 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C010 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system design—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE III. NMC27C010 Minimum Erasure Time

Light Intensity (μWatts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C1024
1,048,576-Bit (64k x 16) UV Erasable CMOS PROM

General Description

The NMC27C1024 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C1024 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

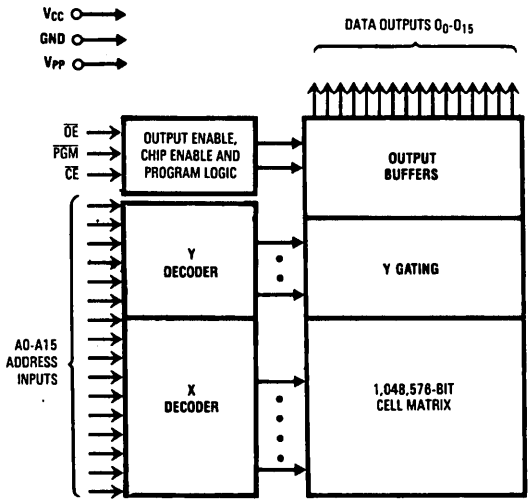
The NMC27C1024 is packaged in a 40-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 550 μW max
- Performance compatible to 16-bit and 32-bit microprocessors
- Single 5V power supply
- Extended temperature range (NMC27C1024QE), −40°C to +85°C, and military temperature range (NMC27C1024QM), −55°C to +125°C, available
- Pin compatible with NMOS wordwide 1024k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's Identification Code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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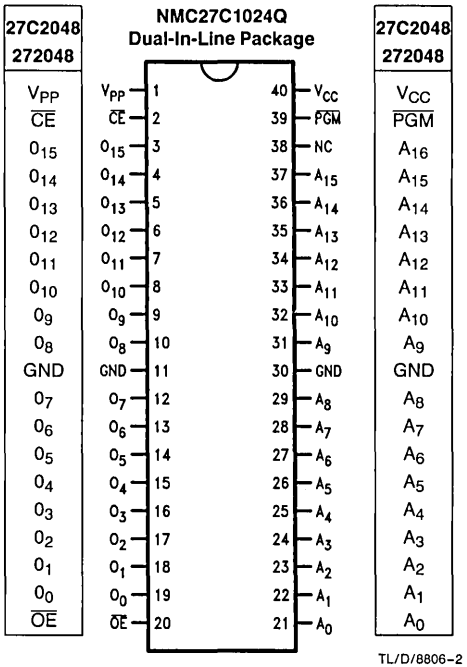
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram



TL/D/8806-2

Order Number NMC27C1024Q
See NS Package Number J40AQ

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C1024 pins.

Commercial Temperature Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024Q150	150
NMC27C1024Q170	170
NMC27C1024Q200	200
NMC27C1024Q250	250

Extended Temperature (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024QE150	150
NMC27C1024QE170	170
NMC27C1024QE200	200

Military Temperature Range (−55°C to +125°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024QM170	170
NMC27C1024QM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0 to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating (MIL Spec 883C Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	Q150		Q170		Q200		Q250		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C1024QE120, 150, 200	−40°C to +85°C
NMC27C1024QM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C1024Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

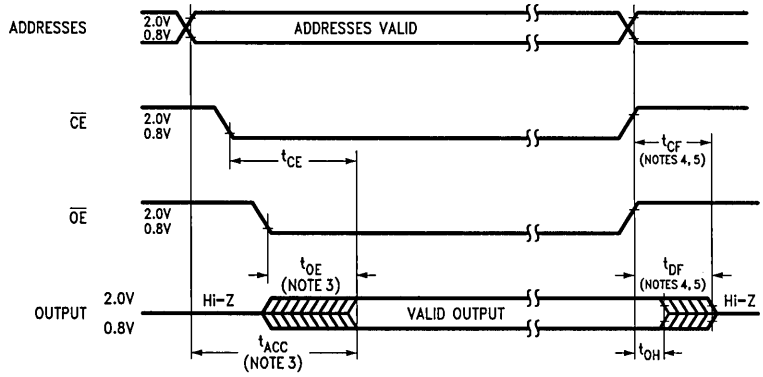
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} +1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
CL: 100 pF includes fixture capacitance.

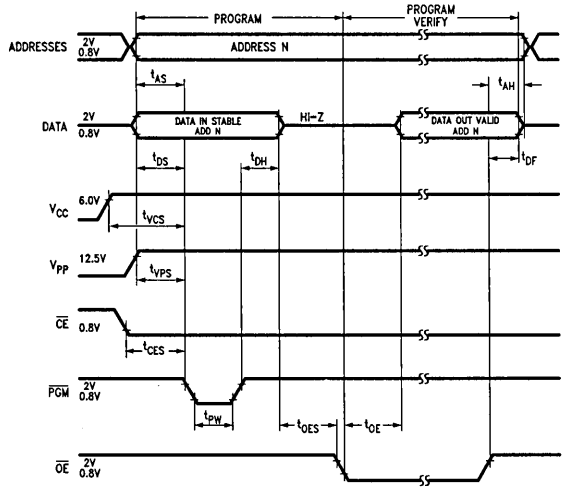
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		1			μs
t_{OES}	$\overline{OE}$ Set-Up Time		1			μs
t_{CES}	$\overline{CE}$ Set-Up Time		1			μs
t_{DS}	Data Set-Up Time		1			μs
t_{VPS}	V_{PP} Set-Up Time		1			μs
t_{VCS}	V_{CC} Set-Up Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid From $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
t_R	Temp Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
T_{CR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings. The min and max limit parameters are design parameters, not tested or guaranteed.

Fast Programming Algorithm Flow Chart

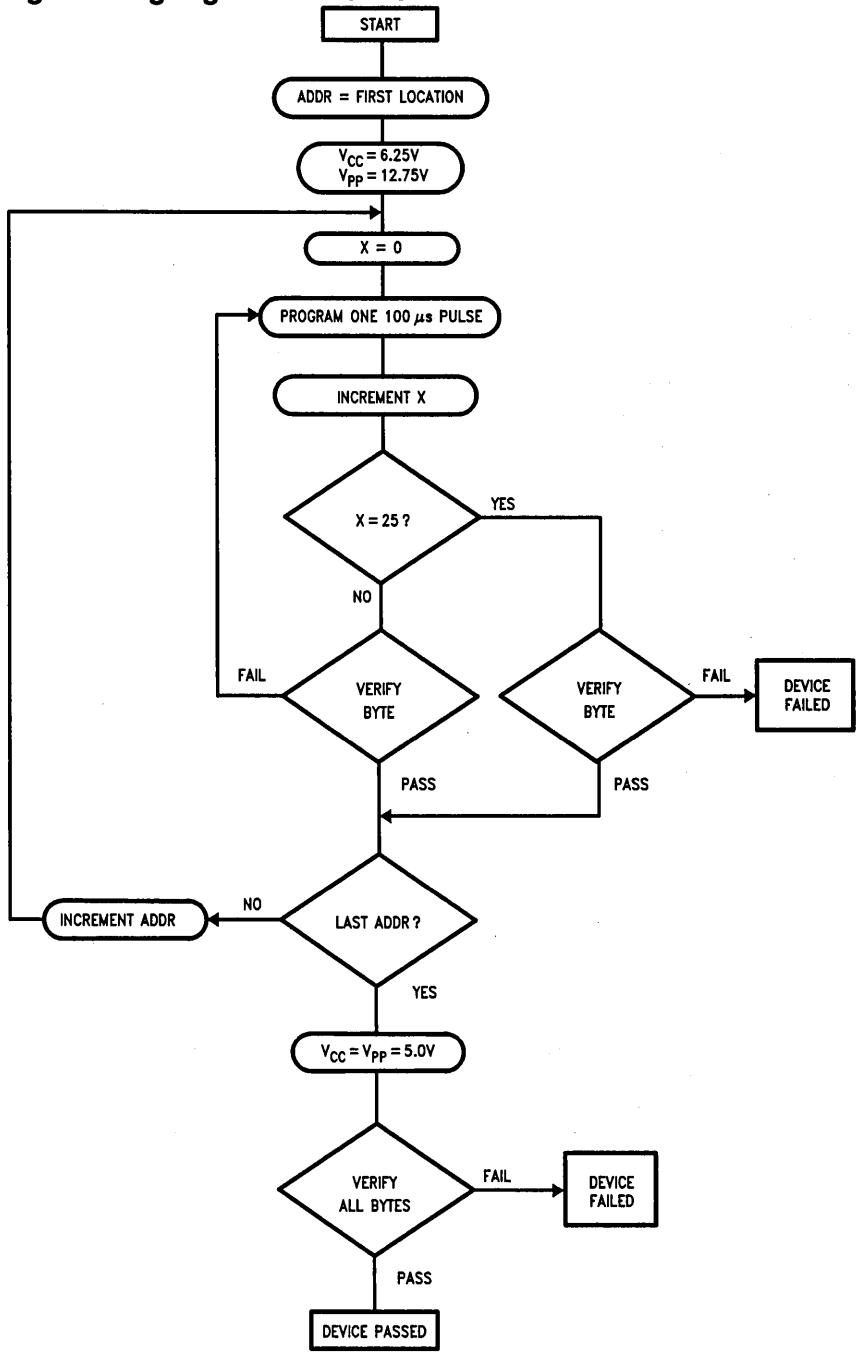

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C1024 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C1024 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C1024 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C1024s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 2) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C1024.

Initially, and after each erasure, all bits of the NMC27C1024 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C1024 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the PGM input. A program pulse must be applied at each address location to be programmed. The NMC27C1024 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C1024 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C1024s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C1024s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C1024s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	V_{PP} (1)	V_{CC} (40)	Outputs (3-10, 12-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C1024 may be common. A TTL low level program pulse applied to an NMC27C1024 $\overline{PGM}$ input with CE at V_{IL} and V_{PP} at 12.5V will program that NMC27C1024. A TTL high level $\overline{CE}$ input inhibits the other NMC27C1024s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C1024 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C1024 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Meg part.

The code is accessed by applying 12 ±0.5V to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C1024 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming opaque labels should be placed over the NMC27C1024 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C1024 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C1024 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C1024 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	1	0	1	1	0	D6

TABLE III. Minimum NMC27C1024 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C020
2,097,152-Bit (256k x 8) UV Erasable CMOS PROM

General Description

The NMC27C020 is a high-speed 2048k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C020 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

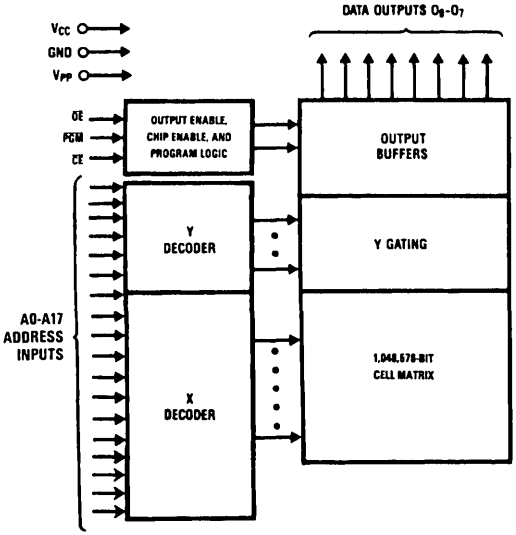
The NMC27C020 is packaged in a 32-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C020QE), −40°C to +85°C and military temperature range (NMC27C020QM), −55°C to +125°C, available
- Pin compatible with NMOS bytewide 2 meg EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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Pin Names

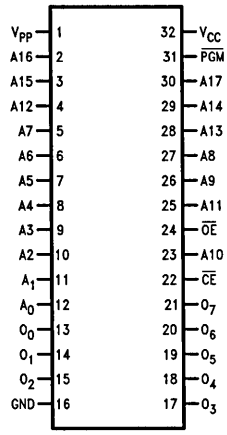
A0–A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program

1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C64 2764	27C010 27010
				V_{PP}
				A16
A15	V_{PP}	V_{PP}	V_{PP}	A15
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27C020Q
Dual-In-Line Package



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27C010 27010	27C64 2764	27C128 27128	27C256 27256	27C512 27512
V_{CC}				
$\overline{PGM}$				
NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
A14	$\overline{PGM}$	$\overline{PGM}$	A14	A14
A13	NC	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C020 pins.

Order Number NMC27C020Q
See NS Package Number J32AQ

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C020Q150	150
NMC27C020Q170	170
NMC27C020Q200	200
NMC27C020Q250	250

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C020QE170	170
NMC27C020QE200	200
NMC27C020QE200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C020QM170	170
NMC27C020QM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C020								Units
			Q150		Q170		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C020QE120, 150, 200	−40°C to +85°C
NMC27C020QM150, 200	−55°C to +125°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C020Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

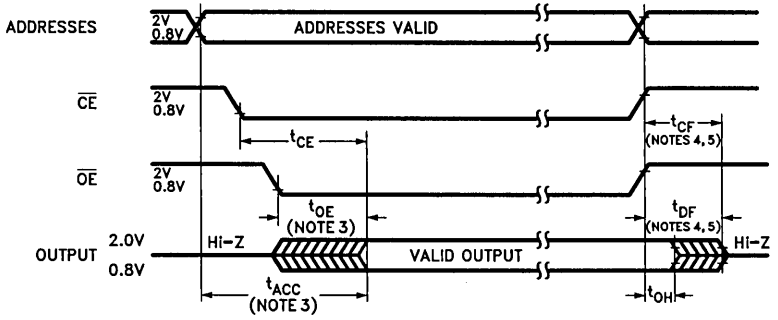
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

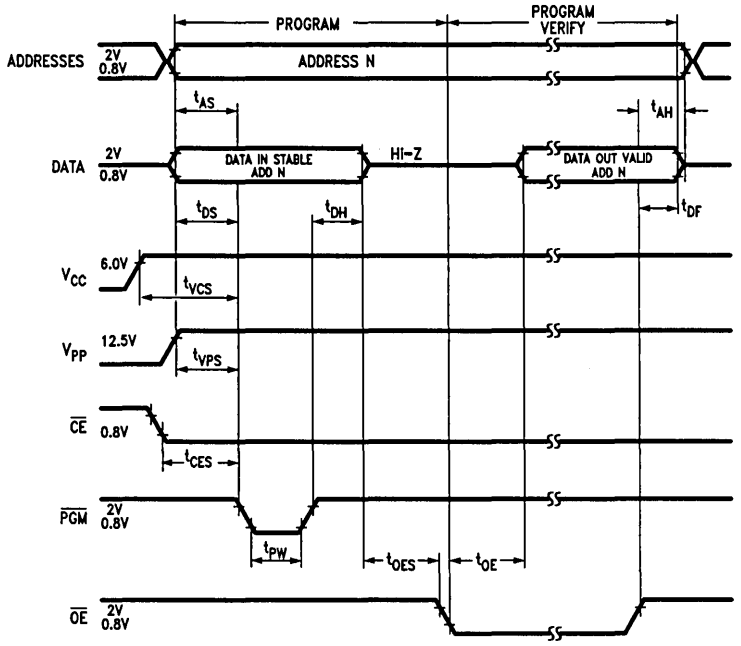
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart

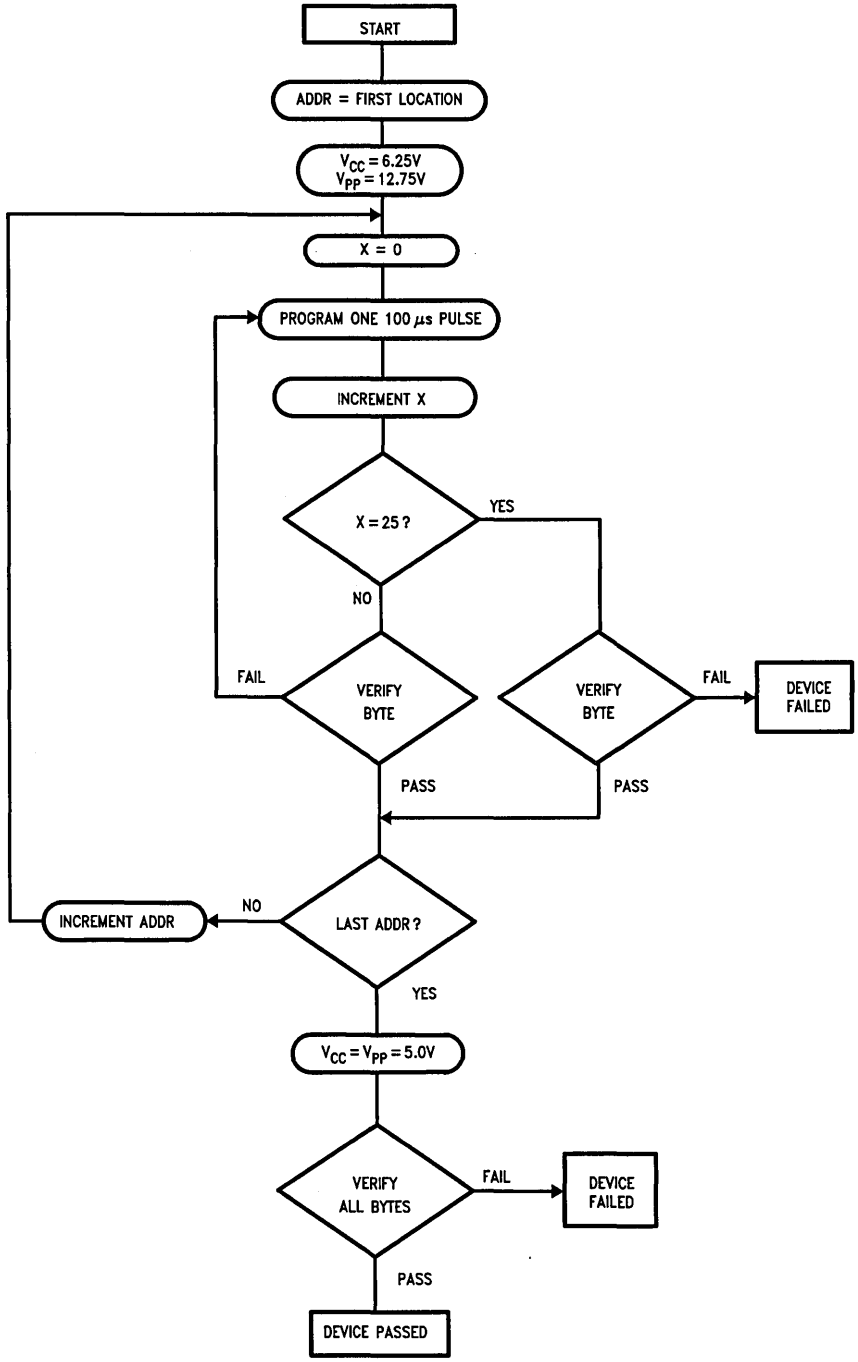

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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C020 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C020 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C020 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C020 are placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C020s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C020.

Initially, and after each erasure, all bits of the NMC27C020 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C020 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C020 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C020 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C020s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C020s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C020s.

Program Inhibit

Programming multiple NMC27C020s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C020s may be common. A TTL low level program pulse applied to an NMC27C020 $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C020. A TTL high level $\overline{CE}$ input inhibits the other NMC27C020s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC27C020 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Functional Description (Continued)

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13–15, 17–21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

TABLE II. Manufacturer's Identificatiion Code

Pins	A0 (12)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	1	1	07

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C020 is "8F07", where "8F" designates that it is made by National Semiconductor, and "07" designates a 2 Megabit byte-wide part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A17, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C020 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27C020 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C020 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C020 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C020 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer)—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE III. NMC27C020
Minimum Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

PRELIMINARY

NMC27C2048
2,097,152-Bit (128k x 16) UV Erasable CMOS PROM

General Description

The NMC27C2048 is a high-speed 2048k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C2048 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

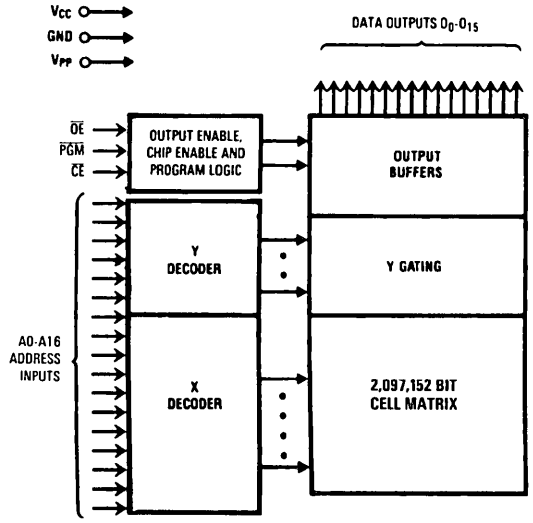
The NMC27C2048 is packaged in a 40-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 110 mW max
  - — Standby Power: 550 μW max
- Performance compatible to 16-bit and 32-bit microprocessors
- Single 5V power supply
- Extended temperature range (NMC27C2048QE), −40°C to +85°C, and military temperature range (NMC27C2048QM), −55°C to +125°C, available
- Pin compatible with NMOS wordwide 2048k EPROMs
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems
- Manufacturer's identification code for automatic programming control
- High current CMOS level output drivers

Block Diagram



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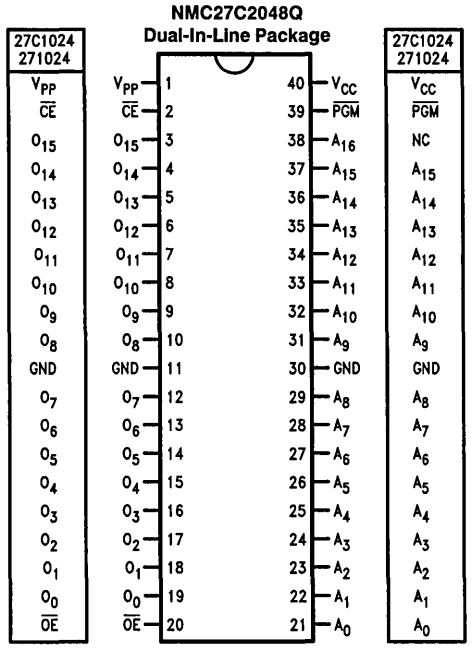
Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram



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Order Number NMC27C2048Q
See NS Package Number J40AQ

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C2048Q pins.

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C2048Q150	150
NMC27C2048Q170	170
NMC27C2048Q200	200
NMC27C2048Q250	250

V_{CC} = 5V ±10% Extended Temperature Range
(−40°C to +85°C)

Parameter/Order Number	Access Time (ns)
NMC27C2048QE170	170
NMC27C2048QE200	200
NMC27C2048QE200	200

V_{CC} = 5V ±10% Military Temperature Range
(−55°C to +125°C)

Parameter/Order Number	Access Time (ns)
NMC27C2048QM170	170
NMC27C2048QM200	200

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C2048								Units
			Q150		Q170		Q200		Q250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	Operating Temp. Range
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C2048QE120, 150, 200	−40°C to +85°C
NMC27C2048QM150, 200	−55°C to +125°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C2048Q						Units
			E150		E170, M170		E200, M200		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		75		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		50	0	55	0	55	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	50	0	55	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

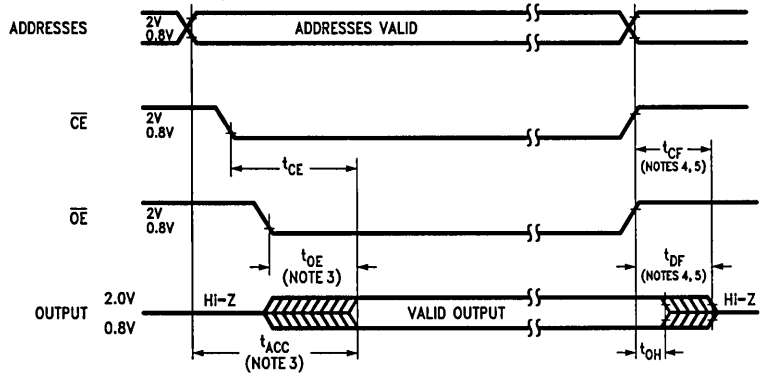
Capacitance $T_A = +25°C, f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

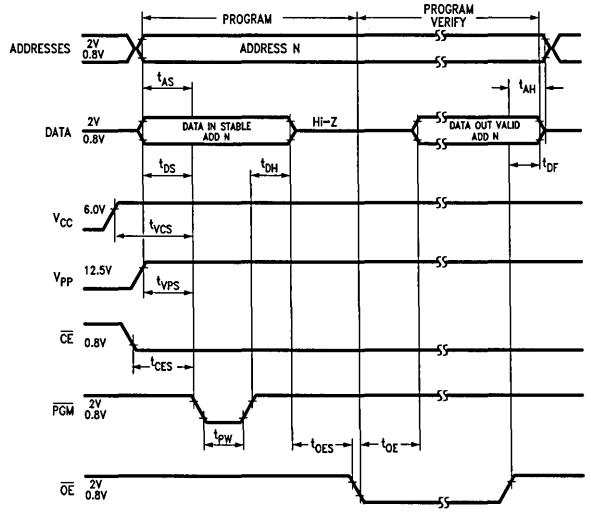
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms (Note 3)



TL/D/9695–4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Fast Programming Algorithm Flow Chart

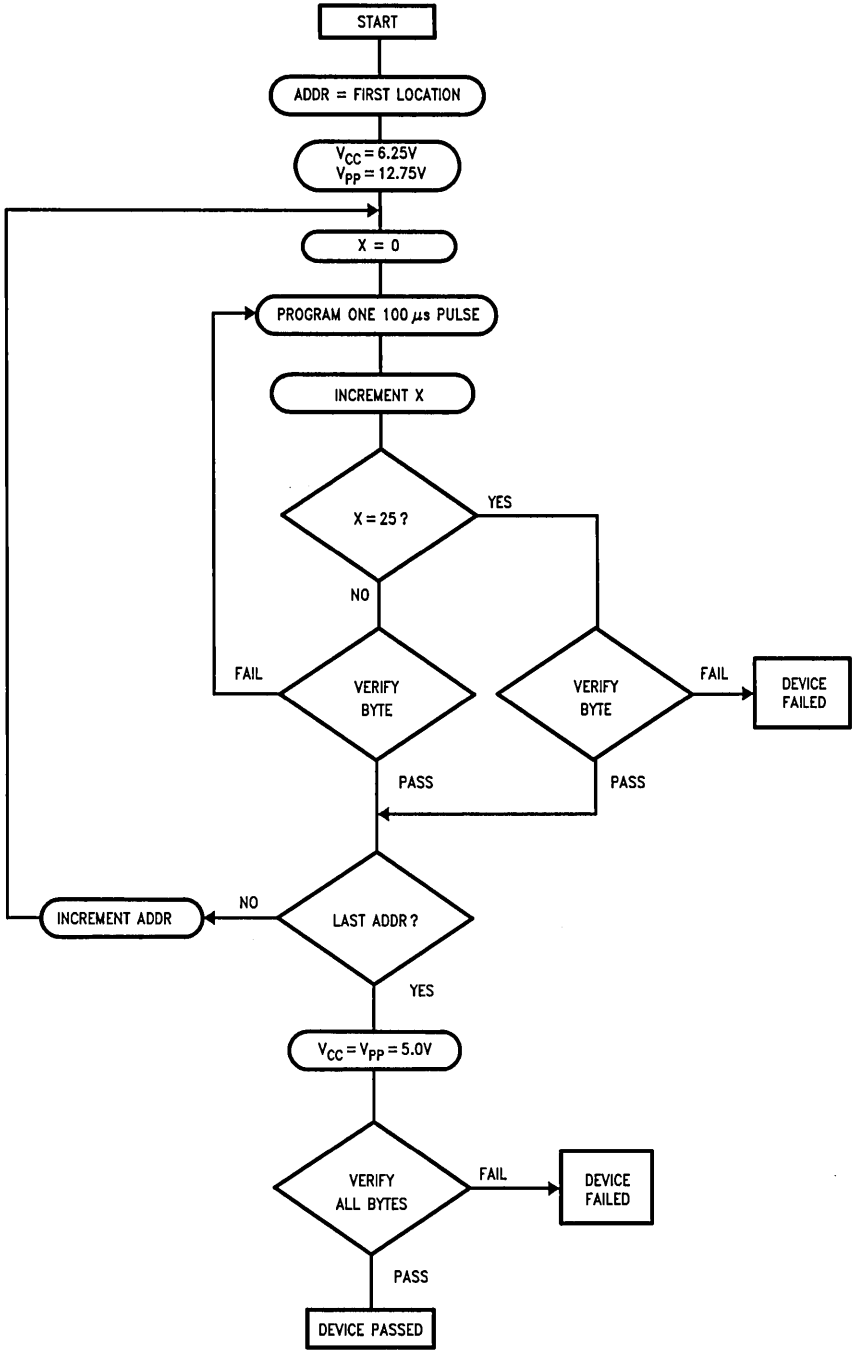


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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C2048 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C2048 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C2048 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC27C2048 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C2048s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 2) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the NMC27C2048.

Initially, and after each erasure, all bits of the NMC27C2048 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C2048 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the PGM input. A program pulse must be applied at each address location to be programmed. The NMC27C2048 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 ns pulses until it verifies good, up to a maximum of 25 pulses. Most memory cell will Program with a single 100 ns pulse. The NMC27C2048 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C2048s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C2048s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C2048s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	V_{PP} (1)	V_{CC} (40)	Outputs (3–10, 12–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	V_{CC}	5V	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.75V	6.25V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C2048s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C2048 may be common. A TTL low level program pulse applied to an NMC27C1024's $\overline{PGM}$ may be common. A TTL low level program pulse applied to an NMC27C1024s $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that NMC27C2048. A TTL high level $\overline{CE}$ input inhibits the other NMC27C2048s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Manufacturer's Identification Code

The NMC27C2048 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C2048 is "8F57", where "8F" designates that it is made by National Semiconductor, and "57" designates a 2 Meg part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C2048 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After Programming

Opaque labels should be placed over the NMC27C2048s window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C2048 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C2048 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C2048 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

1

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	1	0	1	0	1	1	1	57

TABLE III. Minimum NMC27C2048 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Section 2

Flash CMOS EPROMs and EEPROMs

Section 2 Contents

National Semiconductor

FLASH EPROM and EEPROM (Technology Overview)

The FLASH EPROMs and FLASH EEPROMs are built using an EPROM-like process and design approach and are manufactured on National's 1.5μ CMOS process. FLASH technology utilizes a double-poly single metal floating gate with an oxide thickness of 200Å, which permits programming via hot electron injection and erasure thru Fowler-Nordheim tunneling *(Figure 1)*.

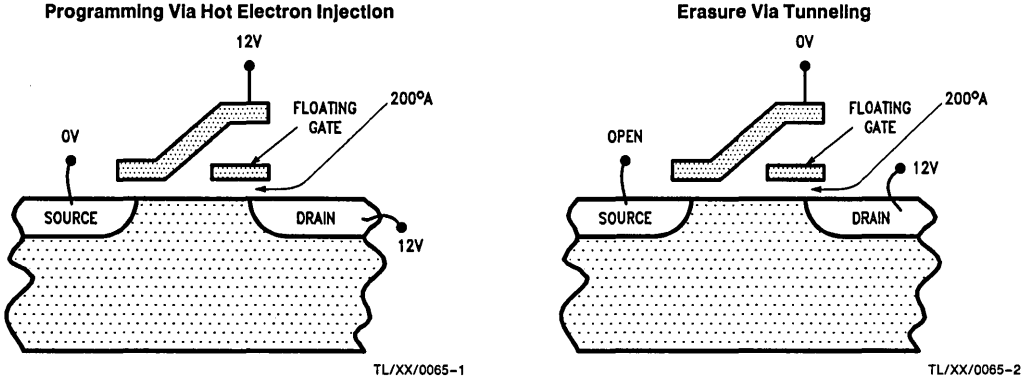


FIGURE 1

The cell structure shown consists of 1.5T per cell and is achieved by the merging of the bit selection and the floating gate transistor, as shown in *Figure 2*. The half transistor which is the bit selection transistor acts as an enhancement device and allows for the selection of the desired column in the array regardless of whether the floating gate is in the depletion or non-depletion mode.

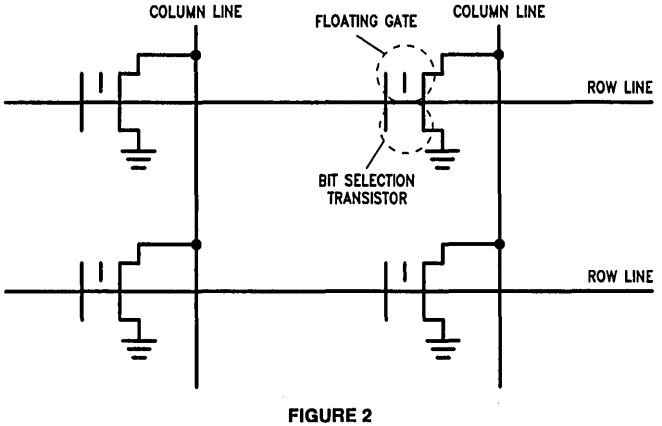
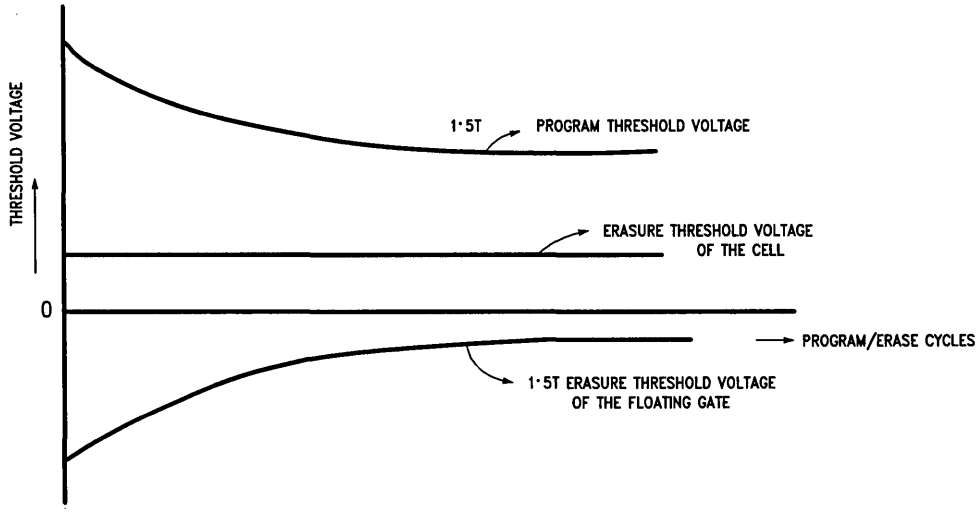


FIGURE 2

2

This unique cell structure permits uniform erasure over the entire array thereby enabling the device to perform to specifications. This cell structure also allows the FLASH memory devices from National Semiconductor to erase over a wide voltage range and erase time as compared to other cell structures.

An additional benefit offered by this cell structure is the ability to achieve higher endurance. As shown in *Figure 3* the programming characteristics on the FLASH 1.5T devices are the same as those seen in UV-EPROMs. In the erase mode however, the floating gate exhibits a depletion characteristic though the cell exhibits a constant threshold voltage regardless of the number of the program/erase cycles. This is achieved by the enhancement characteristics of the bit selection transistor.



TL/XX/0065–4

FIGURE 3

With these benefits and the ability of this technology to achieve die sizes and hence densities comparable to UV-EPROMs, while offering the on-board or in-system program/erase features of EEPROMs, it is not surprising that FLASH is being considered for numerous new designs and applications.

National Semiconductor

ADVANCE INFORMATION

NMC48F512
524,288-Bit (64k x 8) CMOS FLASH EEPROM

General Description

The NMC48F512 is a high speed electrically erasable and programmable read only memory, ideal for on-line, in-system firmware modifications. The NMC 48F512 combines the electrical programmability feature of UV-EPROMs with a fast electrical sector/chip erase feature of EEPROMs. The whole array of the NMC48F512 can be electrically erased in 7.5 seconds (max) compared to the typical 15–20 minutes erase time required by conventional UV-EPROMs.

The NMC48F512 is equipped with on-chip address and data latches and, an on-board timer which allows the host CPU to perform program and erase operations with minimum width instruction cycles, without using wait states. The added benefit of the on-chip integration is to enable the CPU to perform other tasks during the program/erase operations. The NMC48F512 is housed in a 32-pin windowless dual-in-line package allowing for easy upgradeability to 4 Mbit.

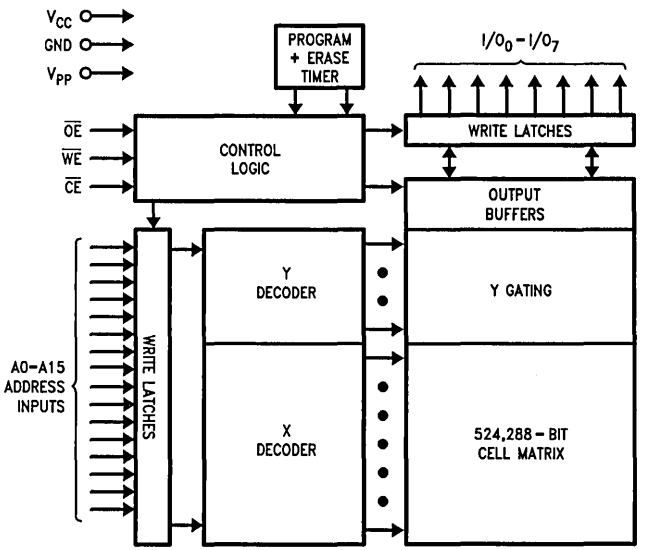
The fast access times of 200 ns and the low active and standby power consumption of the NMC48F512 make it an ideal memory for most high performance systems.

The NMC48F512 is manufactured using National's proprietary time proven CMOS double-polysilicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- In-circuit program/erase
  - 512-byte sector and chip program/erase
  - 7.5 seconds (max) erase time
  - 200 μs (typ) byte program time
- 12V–13V V_{PP} for program/erase
- Designed for total on-line operation
  - Internal address and data latches
  - On-chip program/erase timer
- Low CMOS power consumption
  - Active power: 275 mW max
  - Standby power: 0.55 mW max
- Fast access time: 200 ns
- 32-pin JEDEC approved pinout
  - Upgrade path to 4 Mbit
- Minimum endurance of 100 program/erase cycles
- Program/erase at 0°C to +70°C
- 10 year data retention
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output pins

Block Diagram



TL/D/9705–1

Pin Names

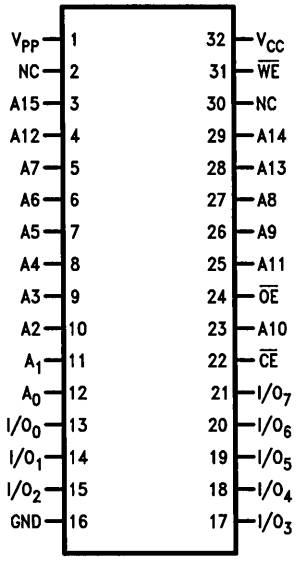
A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O_0–I/O_7	Input/Output
NC	No Connect

Connection Diagram

FLASH EEPROM

4 Mbit	2 Mbit	1 Mbit
A_{18}	V_{PP}	V_{PP}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{12}	A_{12}	A_{12}
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
I/O_0	I/O_0	I/O_0
I/O_1	I/O_1	I/O_1
I/O_2	I/O_2	I/O_2
GND	GND	GND

NMC48F512



1 Mbit	2 Mbit	4 Mbit
V_{CC}	V_{CC}	V_{CC}
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
NC	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
I/O_7	I/O_7	I/O_7
I/O_6	I/O_6	I/O_6
I/O_5	I/O_5	I/O_5
I/O_4	I/O_4	I/O_4
I/O_3	I/O_3	I/O_3

TL/D/9705–2

Note: Socket compatible EEPROM pin configurations are shown in the blocks adjacent to the NMC48F512 pins.

Order Number NMC48F512

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC48F512N200	200
NMC48F512N250	250
NMC48F512N300	300

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC48F512NE250	250
NMC48F512NE300	300

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC48F512NM300	300

Section 3

EEPROMs

Section 3 Contents

EEPROM Selection Guide

Capacity	Organization	Part Number	Access Time (ns)	Cycle Time (ns)	Power Supply (V)	Power Dissipation		Packaging		Operating Temperature
						Active (mA)	Standby (μA)	DIP	SO	
CMOS EEPROM										
256-Bit	16 x 16 Serial	NMC93C06 NMC93CS06*	500	500	+5	2	50	8	14	C, E, M
512-Bit	32 x 16 Serial	NMC93C26 NMC93CS26*	500	500	+5	2	50	8	14	
1024-Bit	64 x 16 Serial	NMC93C46 NMC93CS46*	500	500	+5	2	50	8	14	
	128 x 8 Parallel	NMC98C10	300	400	+5	10	100	18	20	
		NMC98C10-1	180	280						
2048-Bit	128 x 16 Serial	NMC93C56 NMC93CS56*	500	500	+5	2	50	8	14	
	256 x 8 Parallel	NMC98C20	300	400	+5	10	100	18	20	
		NMC98C20-1	180	280						
4096-Bit	256 x 16 Serial	NMC93C66 NMC93CS66*	500	500	+5	2	50	8	14	
	512 x 8 Parallel	NMC98C40	300	400	+5	10	100	18	20	
		NMC98C40-1	180	280						
NMOS EEPROM										
256-Bit	16 x 16	NMC9306	2	4	+5	10	3	8	14, 8	C, E, M
		NMC9307	2	4		10	3	8		
		NMC9313B	2	5		15	5	8		C
1024-Bit	64 x 16	NMC9346	2	4	+5	12	3	8	14, 8	C, E, M
		NMC9314B	2	5		17	5	8		C

*On chip write protection circuitry

Temperature Ranges

C = 0°C to +70°C
E = −40°C to +85°C
M = −55°C to +125°C

National Semiconductor

NMC9306 256-Bit Serial Electrically Erasable Programmable Memory

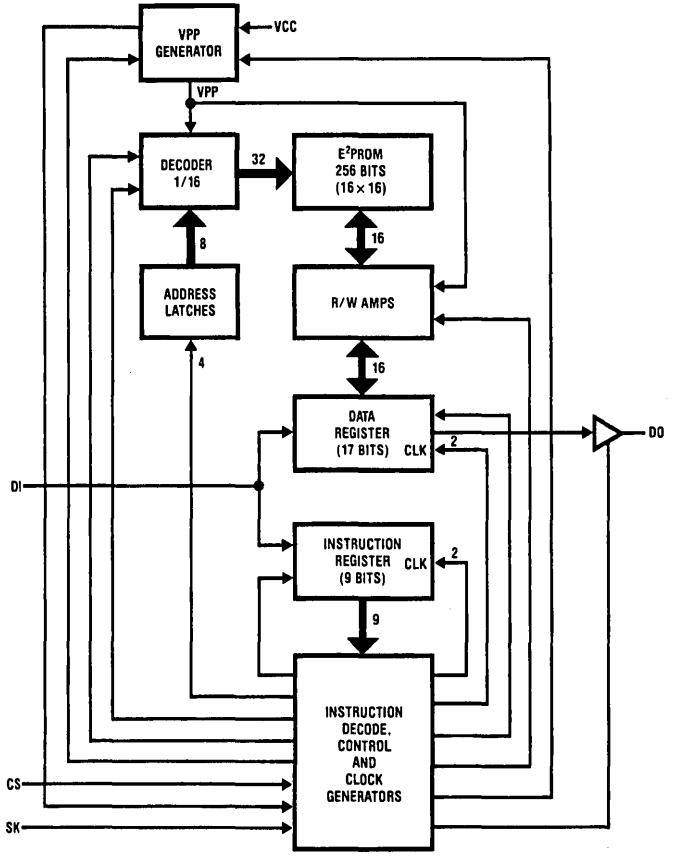
General Description

The NMC9306 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is accessed via the simple MICROWIRE™ serial interface and is designed for data storage and/or timing applications. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306 has been designed to meet applications requiring up to 4×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- 40,000 erase/write cycles typical

Block Diagram

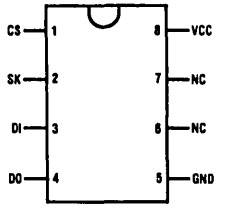


TL/D/5029–1

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Connection Diagram

Dual-In-Line Package (N)

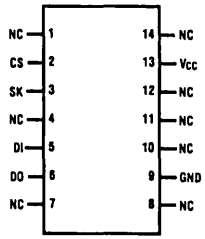


TL/D/5029-10

Top View

See NS Package Number N08E

14-Pin SO Package (M)

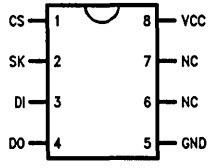


TL/D/5029-12

Top View

See NS Package Number M14B

8-Pin SO Package (M8)



TL/D/5029-11

Top View

See NS Package Number M08A

Ordering Information

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Order Number	Device Marking
NMC9306N	NMC9306N
NMC9306M	9306M14
NMC9306M8	9306

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Order Number	Device Marking
NMC9306EN	NMC9306EN
NMC9306EM	9306EM14
NMC9306EM8	9306E

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ± 10%

Order Number	Device Marking
NMC9306MN	NMC9306MN
NMC9306MM	9306MM14
NMC9306MM8	9306M

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC9306/COP494	0°C to +70°C
NMC9306E	−40°C to +85°C
NMC9306M*	−55°C to +125°C
Positive Supply Voltage	4.5V to 5.5V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Parameter	Part Number	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})	NMC9306, NMC9306E, NMC9306M*		4.5		5.5	V
Operating Current (I_{CC1})	NMC9306	V_{CC} = 5.5V, CS = 1			10	mA
	NMC9306E	V_{CC} = 5.5V, CS = 1			12	mA
	NMC9306M	V_{CC} = 5.5V, CS = 1			14	mA
Standby Current (I_{CC2})	NMC9306	V_{CC} = 5.5V, CS = 0			3	mA
	NMC9306E	V_{CC} = 5.5V, CS = 0			4	mA
	NMC9306M	V_{CC} = 5.5V, CS = 0			5	mA
Input Voltage Levels V_{IL} V_{IH}	NMC9306		 −0.1 2.0		 0.8 V_{CC} + 1	 V V
V_{IL} V_{IH}	NMC9306E		−0.1 2.0		0.8 V_{CC} + 1	V V
V_{IL} V_{IH}	NMC9306M		−0.1 2.0		0.8 V_{CC} + 0.5	V V
Output Voltage Levels V_{OL} V_{OH}	NMC9306, NMC9306E, NMC9306M	 I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4		0.4	 V V
Input Leakage Current	NMC9306, NMC9306E, NMC9306M	V_{IN} = 5.5V			10	μA
Output Leakage Current	NMC9306, NMC9306E, NMC9306M	V_{OUT} = 5.5V, CS = 0			10	μA
SK Frequency SK HIGH TIME t_{SKH} (Note 2) SK LOW TIME t_{SKL} (Note 2)	NMC9306		0 1 1		250	kHz μs μs
SK Frequency SK HIGH TIME t_{SKH} (Note 2) SK LOW TIME t_{SKL} (Note 2)	NMC9306E		0 1 1		 250 	kHz μs μs
SK Frequency SK HIGH TIME t_{SKH} (Note 2) SK LOW TIME t_{SKL} (Note 2)	NMC9306M		0 2 1		200	kHz μs μs
Input Set-up and Hold Times CS t_{CSS} t_{CSH} DI t_{DIS} t_{DIH}	NMC9306, NMC9306E, NMC9306M		 0.2 0 0.4 0.4			 μs μs μs μs
Output Delay DO t_{PD1} t_{PD0}	NMC9306, NMC9306E, NMC9306M	C_L = 100 pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V			 2 2	 μs μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)	NMC9306, NMC9306E, NMC9306M		10		30	ms

*Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Parameter	Part Number	Conditions	Min	Typ	Max	Units
CS Low Time (t_{CS}) (Note 3)	NMC9306, NMC9306E, NMC9306M		1			μs
Endurance	NMC9306, NMC9306E, NMC9306M	Data Changes Per Bit		40,000		Cycles

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Functional Description

The NMC9306 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 10-bit instructions can be executed. The instruction format has a logical 0 as a start bit, followed by a logical 1, four bits as an op code, and four bits of address. An SK clock cycle is necessary after CS equals logical 0 followed by a logical 1 before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming enable instruction (EWEN) is needed to keep the part in the enable state if the power supply (V_{CC}) noise falls below operating range. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1's) before the register can be written (certain bits set to 0's). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1's. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

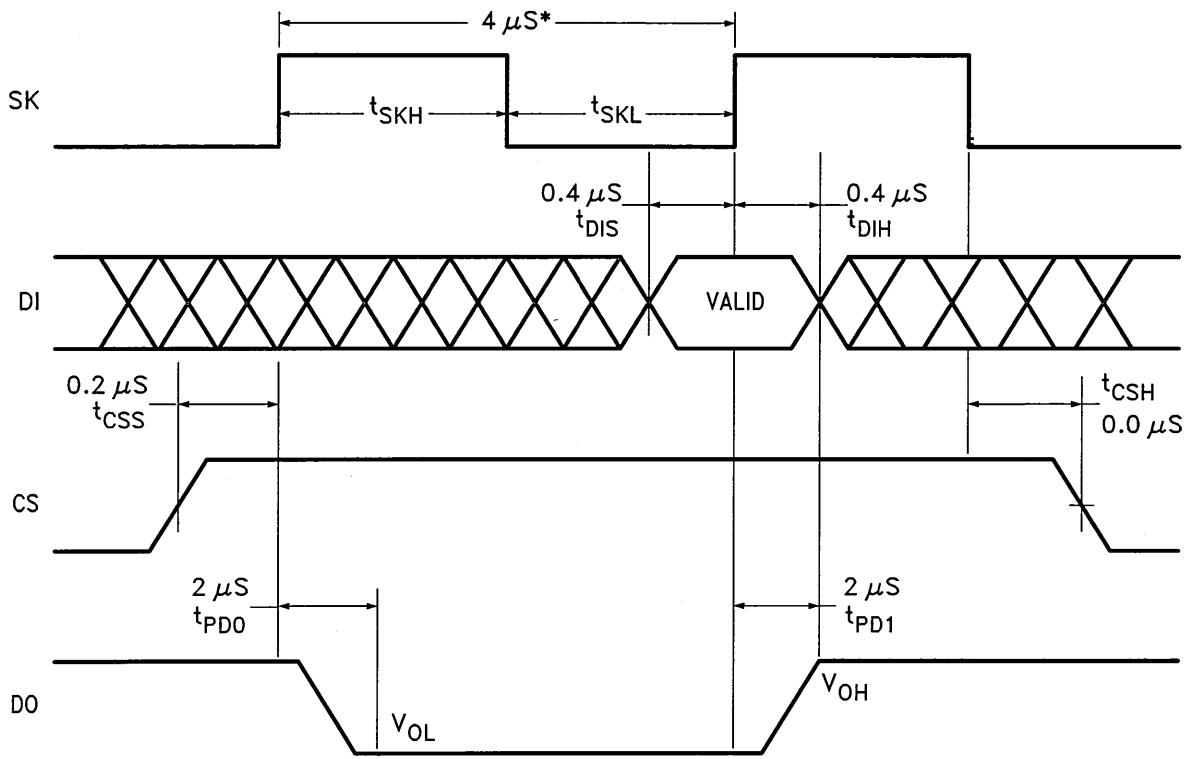
Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NMC9306 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

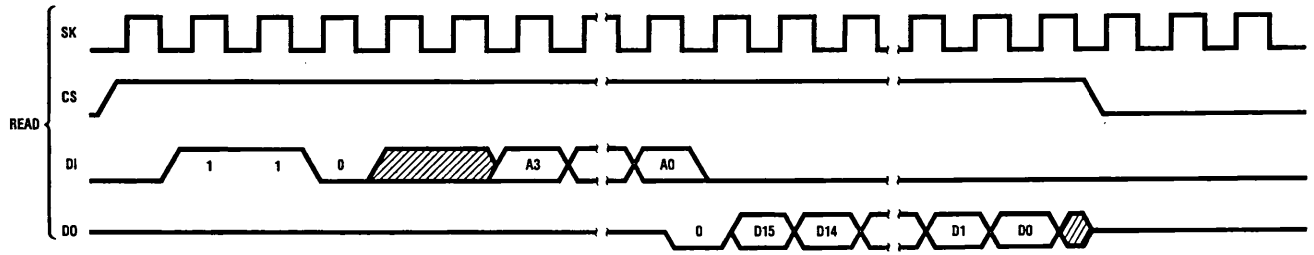
Synchronous Data Timing



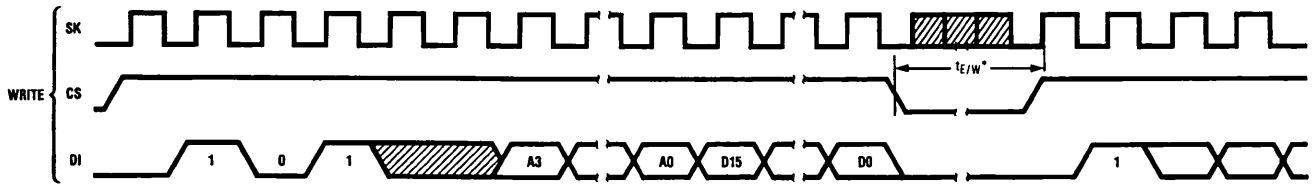
TL/D/5029–13

*This is the minimum SK period and is 5μ for NMC9306M

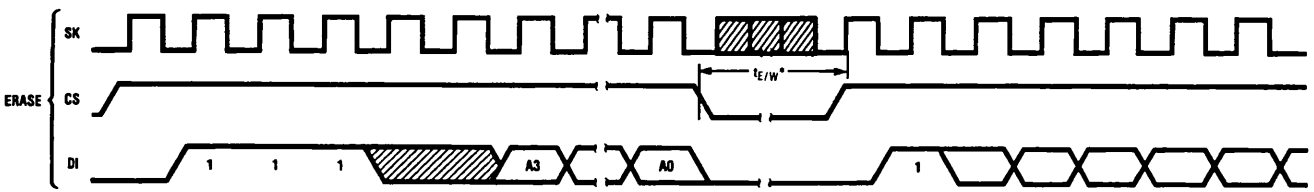
Instruction Timing



TL/D/5029–14



TL/D/5029–15

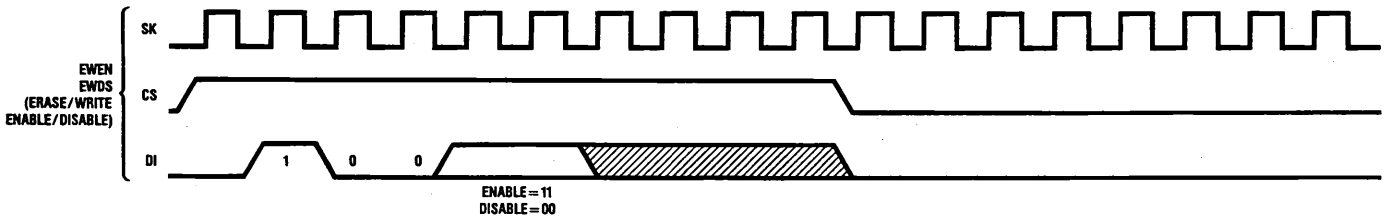


TL/D/5029–16

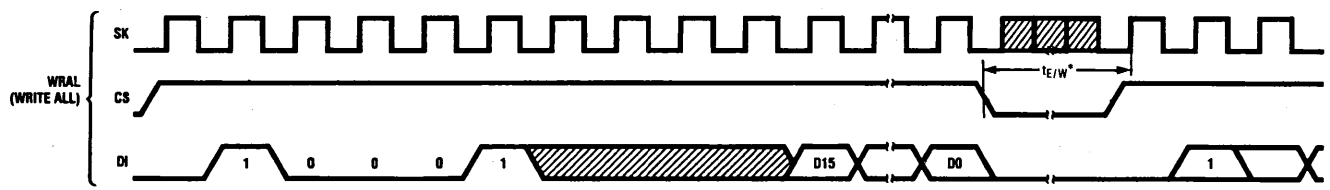
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Timing Diagrams (Continued)

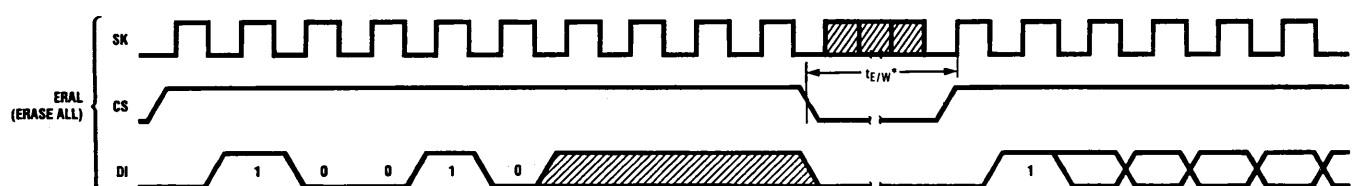
Instruction Timing (Continued)



TL/D/5029–17



TL/D/5029–18



TL/D/5029–19

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

National Semiconductor

PRELIMINARY

NMC93C06/C26/C46 256-Bit/512-Bit/1024-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC93C06/NMC93C26/NMC93C46 are 256/512/1024 bits of CMOS electrically erasable memory divided into 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 5V supply since V_{PP} is generated on-board. The serial organization allows the NMC93C06/NMC93C26/NMC93C46 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status is output on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, Erase/Write Disable. The NMC93C06/NMC93C26/NMC93C46 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming compatibility with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

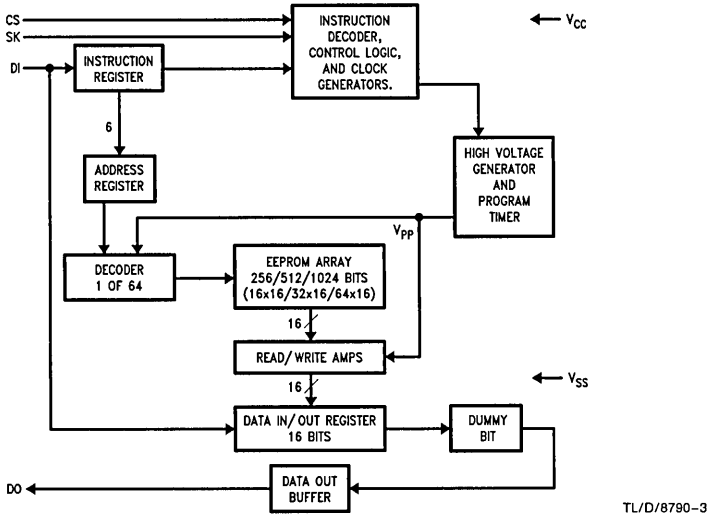
Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346. The NMC93C06/NMC93C26/NMC93C46 are both pin and function compatible with the NMC93C56 2048-bit EEPROM and the NMC93C66 4096-bit EEPROM with the one exception that both of these larger devices require two additional address bits.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5V only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Over 10 years data retention
- Typically 40,000 writes

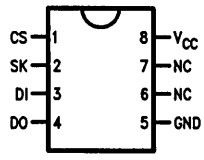
Block Diagram



TL/D/8790–3

Connection Diagrams

Dual-In-Line Package (N)



TL/D/8790-1

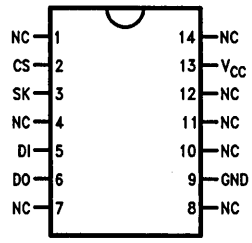
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

SO Package (M)



TL/D/8790-2

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Order Number
NMC93C06N/NMC93C26N/ NMC93C46N NMC93C06M/NMC93C26M/ NMC93C46M

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Order Number
NMC93C06EN/NMC93C26EN/ NMC93C46EN NMC93C06EM/NMC93C26EM/ NMC93C46EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93C06MN/NMC93C26MN/ NMC93C46MN NMC93C06MM/NMC93C26MM/ NMC93C46MM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C06/26/46	0°C to +70°C
NMC93C06/26/46E	−40°C to +85°C
NMC93C06/26/46M	−55°C to +125°C
Positive Supply Voltage	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M*	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	Relative to SK	50 100 100		ns

***Note:** Thruout this table "M" refers to temperature range (−55°C to +125°C), not package.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93C06/26/46 NMC93C06/26/46E NMC93C06/26/46M	$CS = V_{IL}$ AC Test		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit	Typical 40,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For expample, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93C06/NMC93C26/NMC93C46 has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for selection of 1 of 16, 32, or 64 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the 16-bit data output string. Output data changes are initiated by a low-to-high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE)

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is clocked in on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code.

As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 50 ns (t_{CS}).

Erase/Write Disable (EWDS):

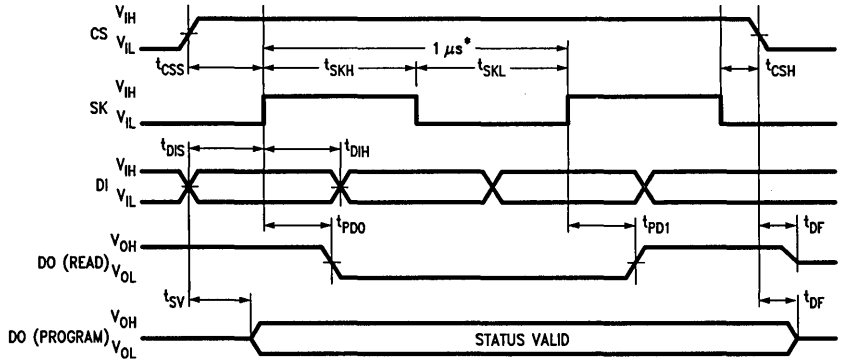
To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C06/26/46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing

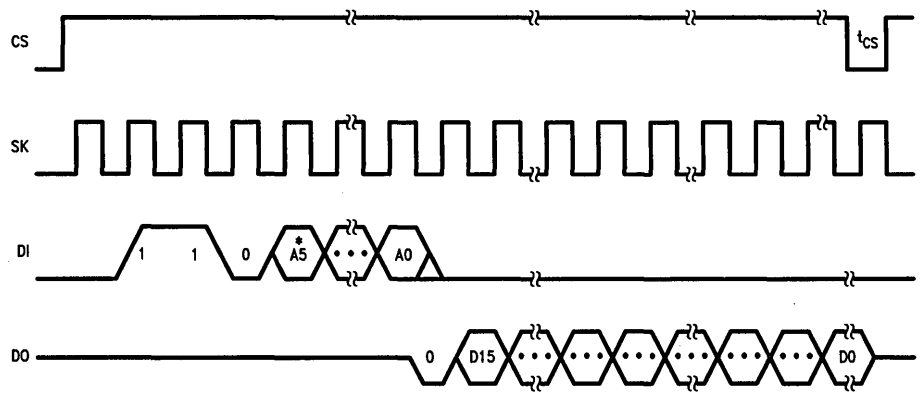


TL/D/8790-4

*This is the minimum SK period (Note 2).

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

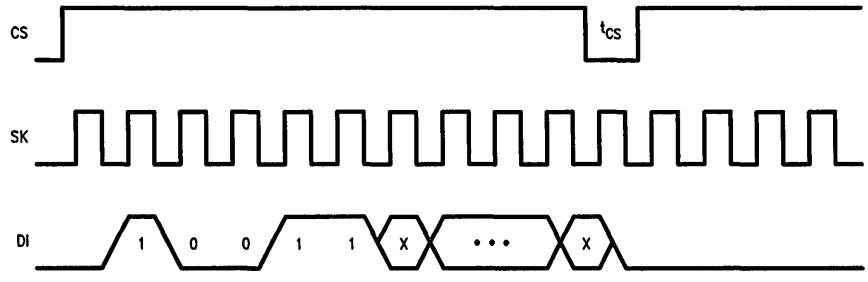
READ:



TL/D/8790-5

*Address bit A5 becomes "don't care" for NMC93C26.
*Address bits A5 and A4 become "don't care" for NMC93C06.

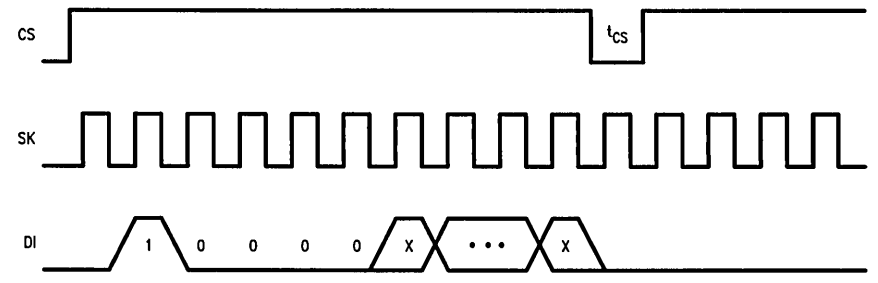
WEN:
DO = TRI-STATE



TL/D/8790-6

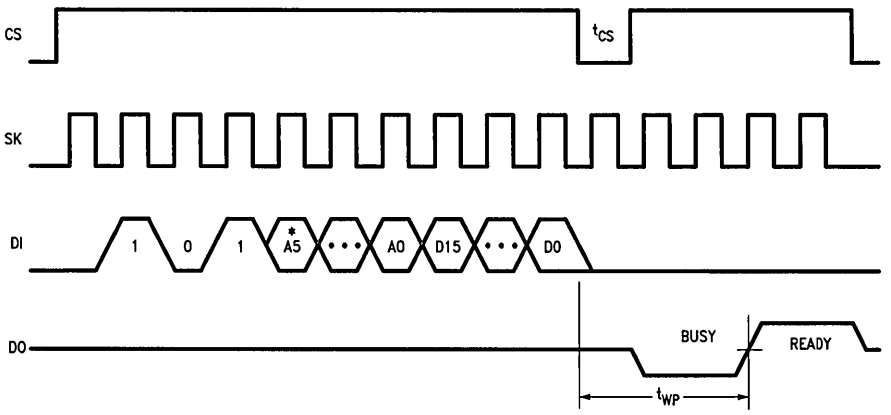
Timing Diagrams (Continued)

EWDS:
DO = TRI-STATE



TL/D/8790-7

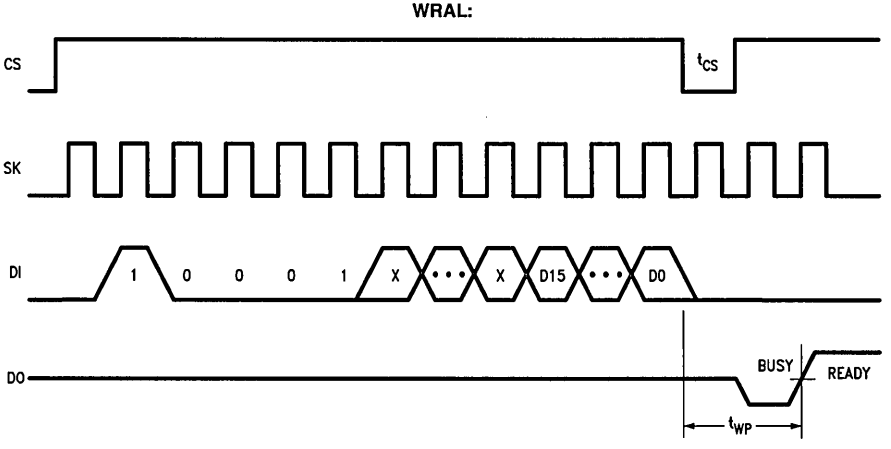
WRITE:



TL/D/8790-8

*Address bit A5 becomes "don't care" for NMC93C26.
*Address bits A5 and A4 become "don't care" for NMC93C06.

WRAL:



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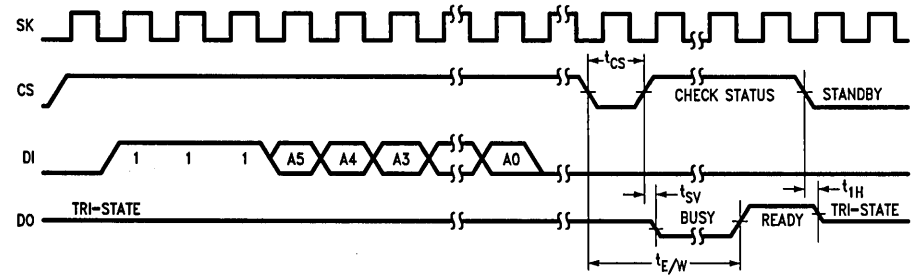
Timing Diagrams (Continued)

ERASE:



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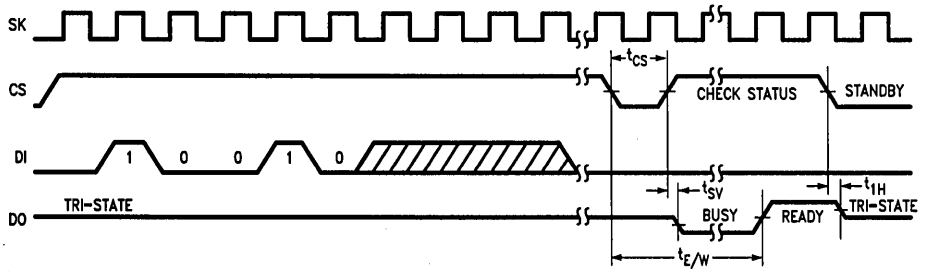
ERAL:



TL/D/8790–11

National Semiconductor

PRELIMINARY

NMC93CS06/CS26/CS46 256-Bit/512-Bit/1024-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93CS06/NMC93CS26/NMC93CS46 are 256/512/1024 bits of read/write memory divided into 16/32/64 registers of 16 bits each. N registers ($N \leq 16$, $N \leq 32$ or $N \leq 64$) can be protected against data modification by programming into a special on-chip register called the memory protect register the address of the first register to be protected. This address can be locked into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the protect register will be aborted.

The read instruction loads the address of the first register to be read into a 6-bit address pointer. Then the data is clocked out serially on the DO pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 256/512/1024 bits. Thus, the NMC93CS06/NMC93CS26/NMC93CS46 can be viewed as a non-volatile shift register.

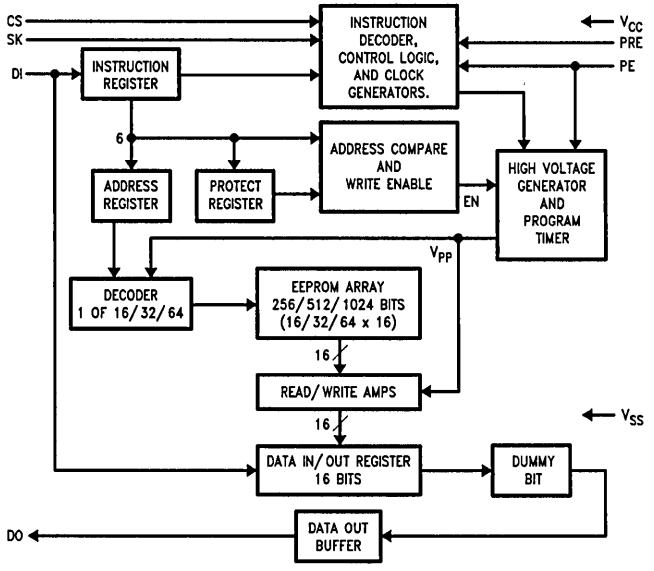
The write cycle is completely self-timed. No separate erase cycle is required before write. The write cycle is only enabled when pin 6 (program enable) is held high. If the address of the register to be written is less than the address in the protect register then the data is written 16 bits at a time into one of the 16/32/64 data registers. If CS is brought high following the initiation of a write cycle the DO pin indicates the ready/busy status of the chip.

National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 10 years.

Features

- Write protection in user defined section of memory
- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- Microwire compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 10 years data retention
- 40,000 write cycles typical

Block Diagram



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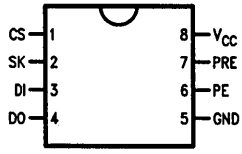
Connection Diagrams

PIN OUT:

Dual-In-Line Package (N)



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Top View

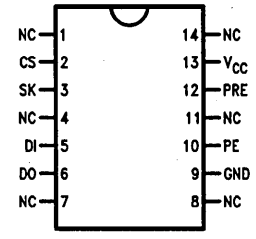
See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



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Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Order Number
NMC93CS06N/NMC93CS26N/ NMC93CS46N
NMC93CS06M/NMC93CS26M/ NMC93CS46M

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Order Number
NMC93CS06EN/NMC93CS26EN/ NMC93CS46EN
NMC93CS06EM/NMC93CS26EM/ NMC93CS46EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93CS06MN/NMC93CS26MN/ NMC93CS46MN
NMC93CS06MM/NMC93CS26MM/ NMC93CS46MM

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93CS06/NMC93CS26/ NMC93CS46	0°C to +70°C
NMC93CS06E/NMC93CS26E/ NMC93CS46E	−40°C to +85°C
NMC93CS06M/NMC93CS26M/ NMC93CS46M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M*	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	50 100 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	50 100 100		ns

*Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	50 100 100		ns
t_{DIS}	DI Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to CS Relative to CS Relative to CS	250 500 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = V_{IL} AC Test		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit	Typical 40,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93CS06, NMC93CS26, and NMC93CS46 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8-bits carry the op code and the 6-bit address for selection of 1 of 16, 32, or 64 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Instruction Set for the NMC93CS06, NMC93CS26 and NMC93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Functional Description (Continued)

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

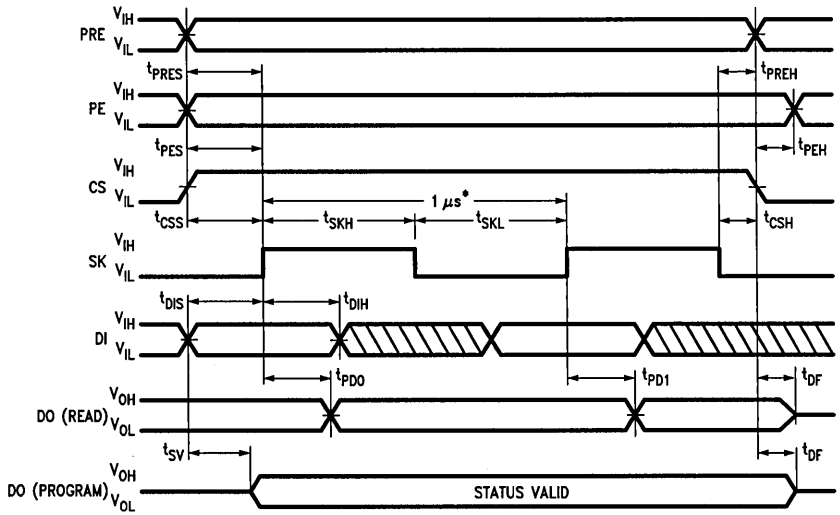
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing



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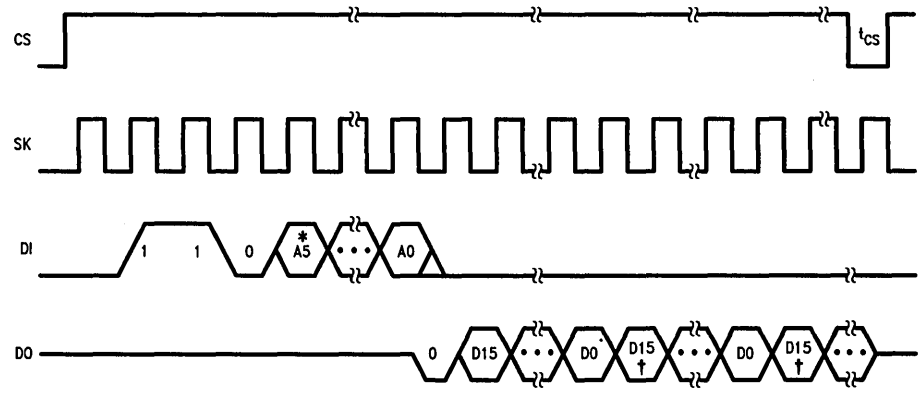
*This is the minimum SK period (See Note 2).

Timing Diagrams (Continued)

READ:
PRE = 0, PE = X



*Address bit A5 becomes a "don't care" for NMC93CS26
*Address bits A5 and A4 become "don't cares" for NMC93CS06
†The memory automatically cycles to the next register.

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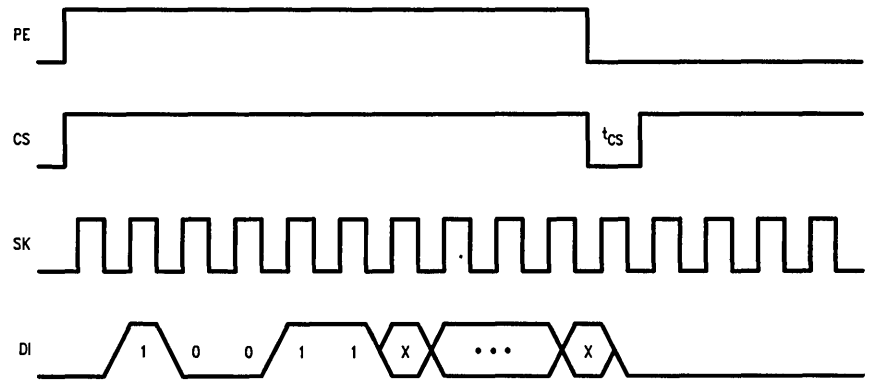
WEN:
PRE = 0, D0 = TRI-STATE



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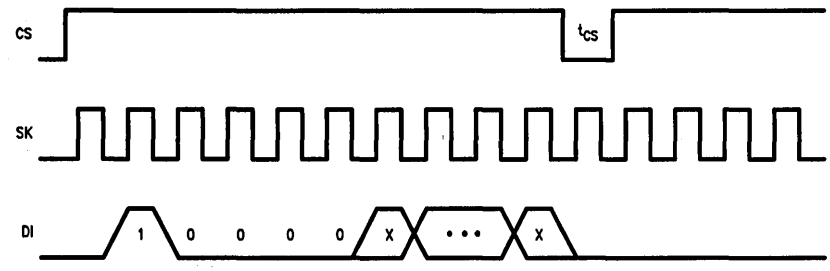
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE



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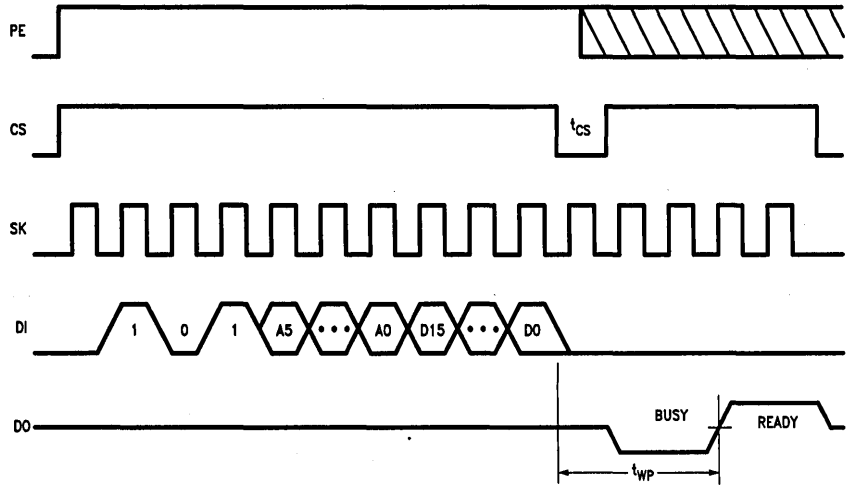
WRITE:
PRE = 0



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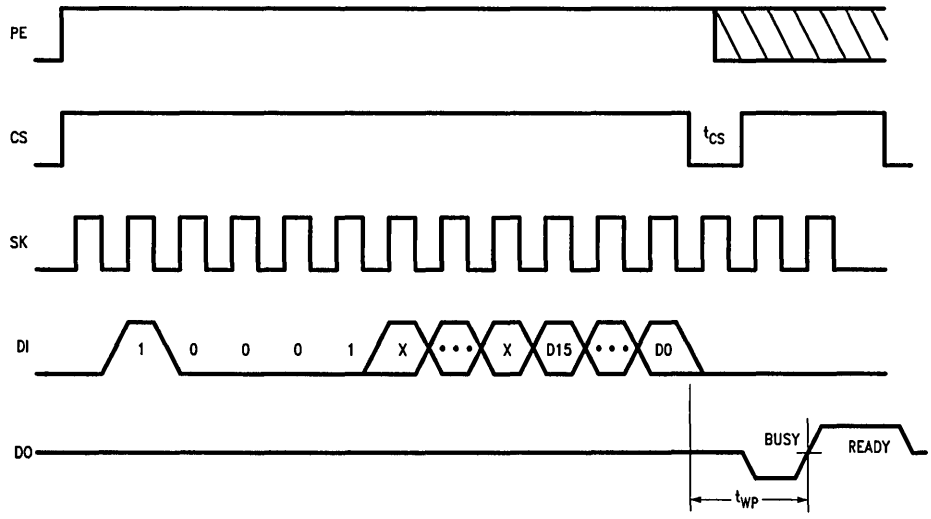
- Address bit A5 becomes a "don't care" for NMC93CS26
- Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

WRALL*:
PRE = 0



*Protect Register **MUST** be cleared.

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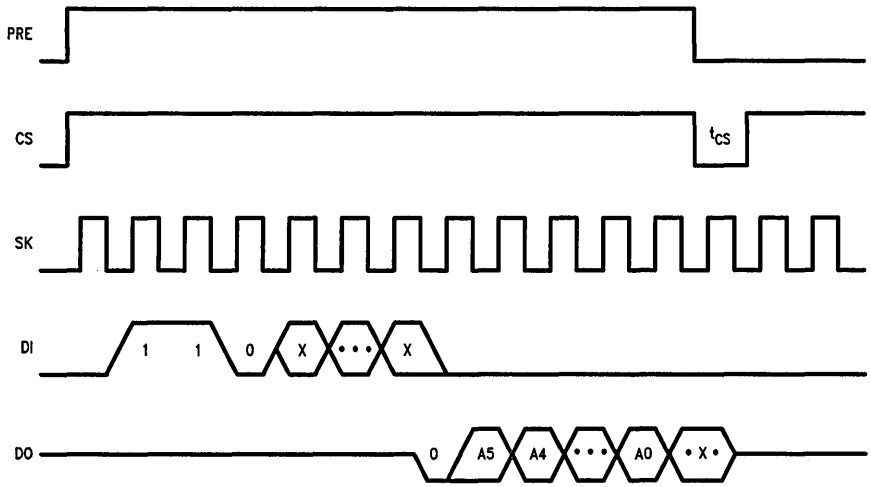
PRREAD:
PE = X



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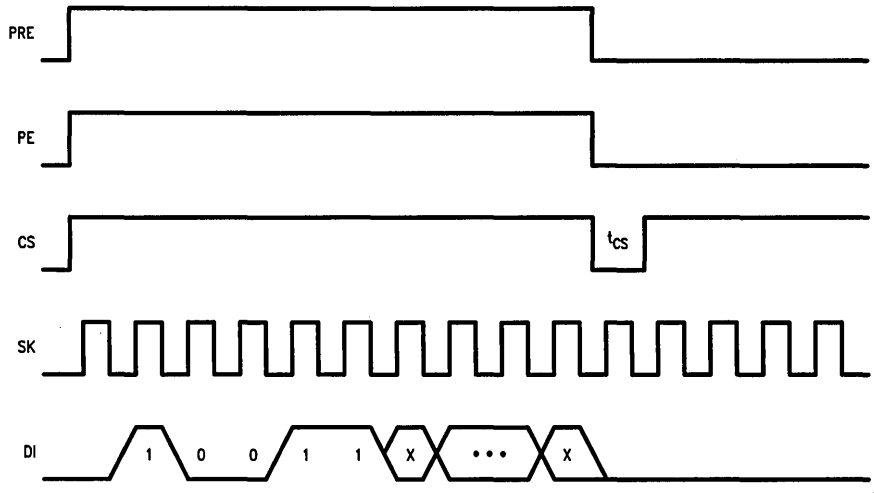
•Address bit A5 becomes a "don't care" for NMC93CS26
•Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

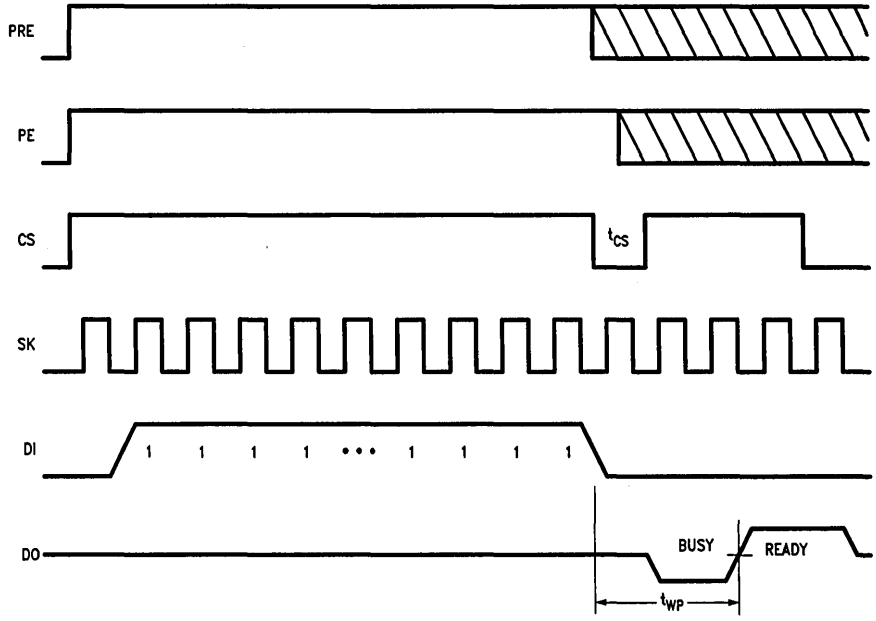
PREN*:
DO = TRI-STATE



TL/D/9208–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:



*A PREN cycle must **immediately** precede a PRCLEAR cycle.

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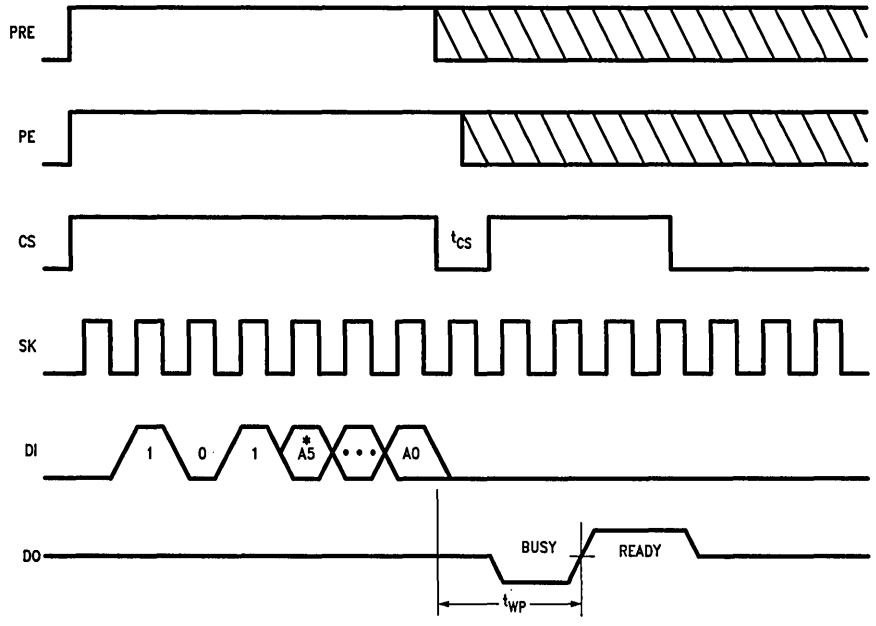
Timing Diagrams (Continued)

PRWRITE†:

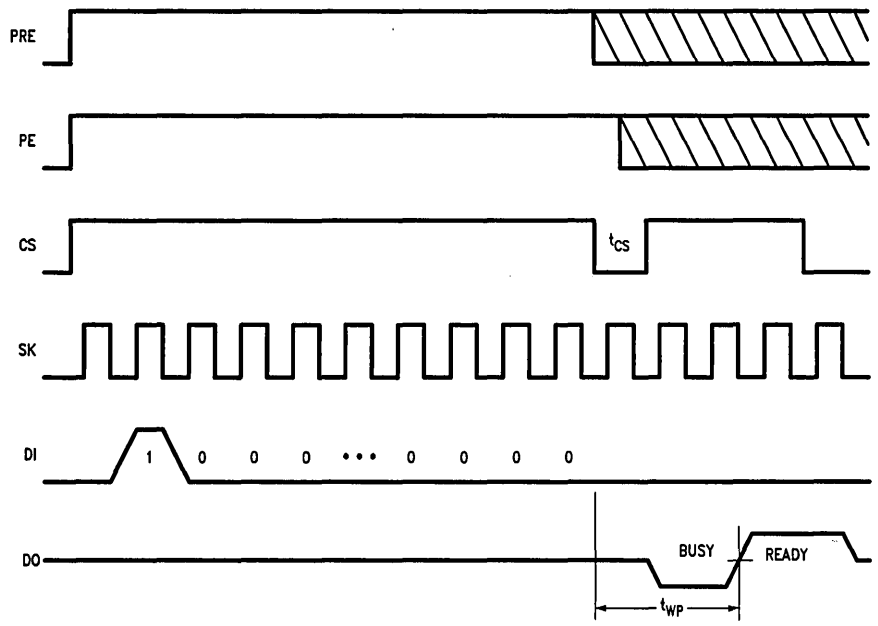


TL/D/9208–13

*Address bit A5 becomes a "don't care" for NMC93CS26
*Address bits A5 and A4 become "don't cares" for NMC93CS06

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **Immediately** precede a PRWRITE cycle.

PRDS*:



TL/D/9208–14

***ONE TIME ONLY** instruction. A PREN cycle must **Immediately** precede a PRDS cycle.

National Semiconductor

NMC9307 256-Bit Serial Electrically Erasable Programmable Memory

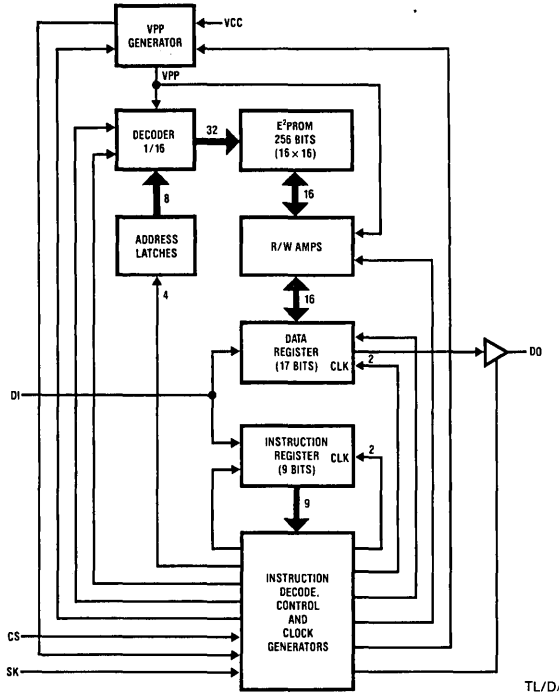
General Description

The NMC9307 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Bulk programming instructions (chip erase, chip write) can be enabled or disabled by the user for enhanced data protection. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9307 has been designed to meet applications requiring up to 40,000 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

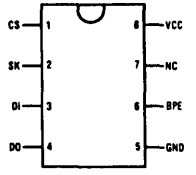
- 40,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/9204-1

Dual-In-Line Package (N)

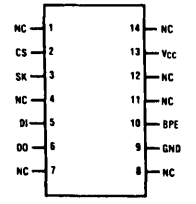


TL/D/9204-2

Top View

See NS Package Number N08E

SO Package (M)



TL/D/9204-3

Top View

See NS Package Number M14B

Note: Contact factory for SO8 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9307	0°C to +70°C
NMC9307E	−40°C to +85°C
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating	2000V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics

Parameter	Conditions	Part No	Min	Max	Units
Operating Voltage (V_{CC})			4.5	5.5	V
Operating Current (I_{CC1})	V_{CC}=5.5V, CS=1	9307		10	mA
		9307E		12	
Standby Current (I_{CC2})	V_{CC}=5.5V, CS=0	9307		3	mA
		9307E		4	
Input Voltage Levels					
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	V_{CC}+1	V
Output Voltage Levels					
V_{OL}	I_{OL}=2.1 mA			0.4	V
V_{OH}	I_{OH}=−400 μA		2.4		V
Input Leakage Current	V_{IN}=5.5V			10	μA
Input Leakage Current	V_{IN}=0 to 5.5V				
PINS 1, 2, 3				±10	μA
PIN 6				±50	μA
Output Leakage Current	V_{OUT}=5.5V, CS=0			10	μA
SK Frequency			0	250	kHz
SK HIGH TIME t_{SKH} (Note 2)			1		μs
SK LOW TIME t_{SKL} (Note 2)			1		μs
Input Set-Up and Hold Times					
CS t_{CSS}			0.2		μs
t_{CSH}			0		μs
DI t_{DIS}			0.4		μs
t_{DIH}			0.4		μs
Output Delay	CL=100 pF				
DO t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V			2	μs
t_{PD0}	V_{IL}=0.45V, V_{IH}=2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)			10	30	ms
CS Low Time (t_{CS}) (Note 3)			1		μs
Endurance	Number of Data Changes per Bit		40, 000 Typical		

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	0, 1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	0, 1	01xx	A3A2A1A0	D15–D0	Write register A3A2A1A0
ERASE	0, 1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	0, 1	0011	xxxx		Erase/write enable
EWDS	0, 1	0000	xxxx		Erase/write disable
ERAL	0, 1	0010	xxxx		Erase all registers
WRAL	0, 1	0001	xxxx	D15–D0	Write all registers

The NMC9307 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9307 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. The NMC9307 is organized as sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E^2PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction. The chip erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., data is not changed.

CHIP WRITE (Note 4)

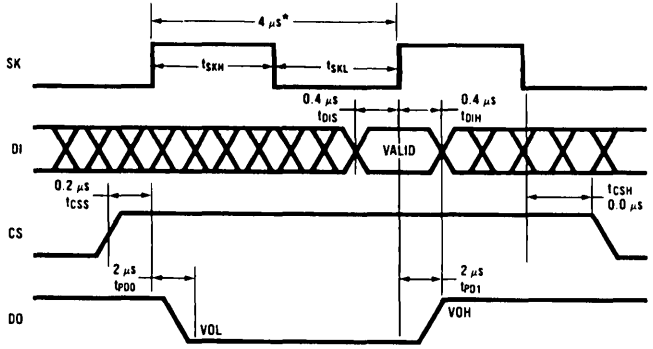
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

The chip write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., the array data is not changed.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

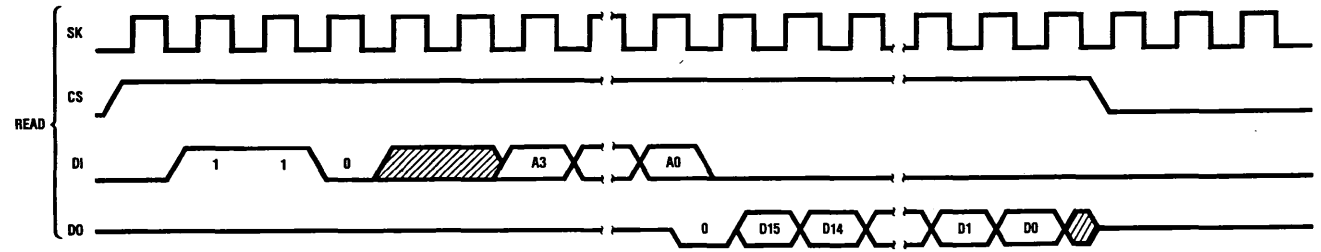
Synchronous Data Timing



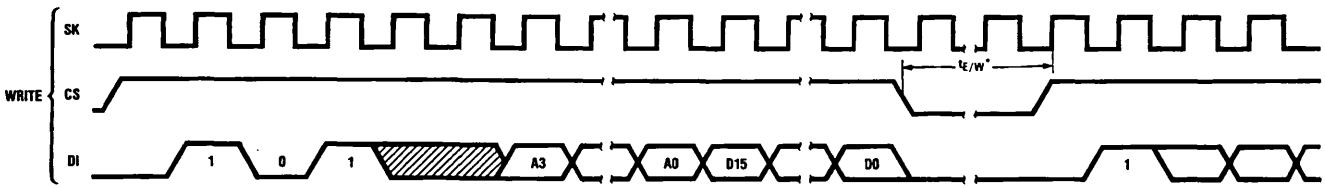
TL/D/9204–4

*This is the minimum SK period

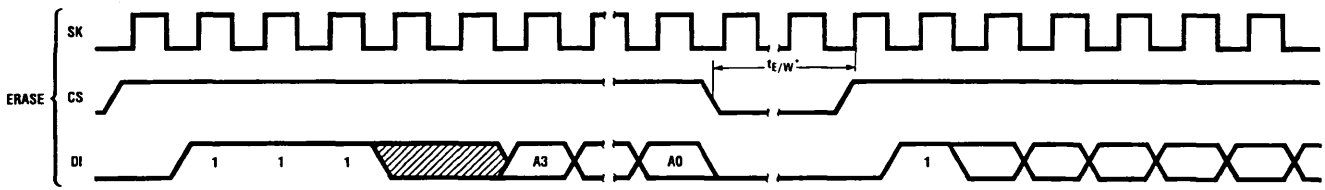
Instruction Timing



TL/D/9204–5



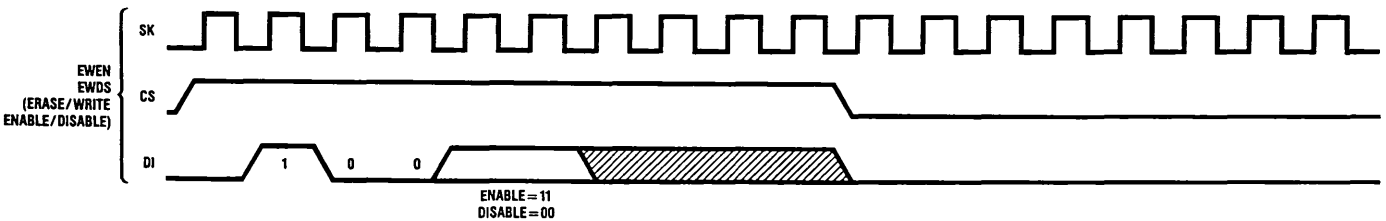
TL/D/9204–6



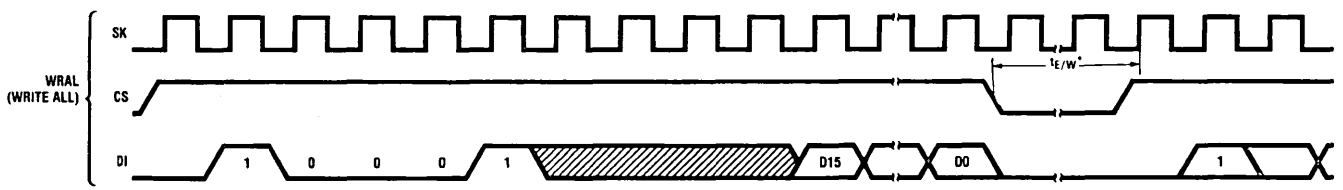
TL/D/9204–7

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

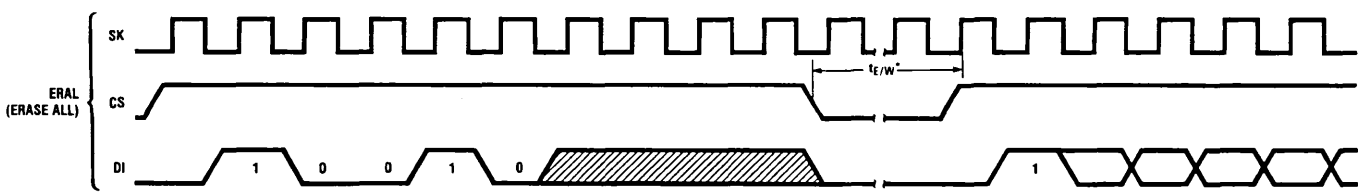
Instruction Timing (Continued)



TL/D/9204–8



TL/D/9204–9



TL/D/9204–10

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

National Semiconductor

NMC9313B 256-Bit Serial Electrically Erasable Programmable Memory

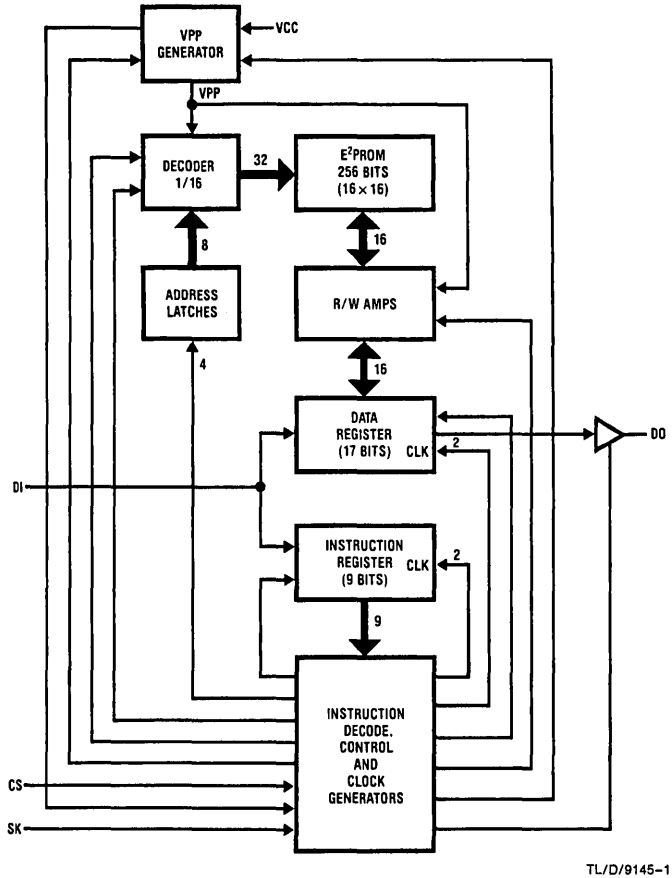
General Description

The NMC9313B is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9313B has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 67 percent.

Features

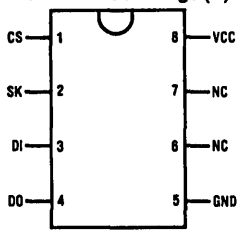
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/9145–1

Dual-In-Line Package (N)



TL/D/9145–2

Top View

Order Number NMC9313B

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature NMC9313B/COP494	0°C to +70°C
Ambient Storage Temperature with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics 0°C ≤TA≤ 70°C, V_{CC} = 5V ± 10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC} = 5.5V, CS = 1			15	mA
Standby Current (I_{CC2})	V_{CC} = 5.5V, CS = 0			5	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC} + 0.5	V
Output Voltage Levels					
V_{OL}	I_{OL} = 2.1 mA			0.4	V
V_{OH}	I_{OH} = −400 μA	2.4			V
Input Leakage Current	V_{IN} = 5.5V			10	μA
Output Leakage Current	V_{OUT} = 5.5V, CS = 0			10	μA
SK Frequency		0		200	kHz
SK HIGH TIME t_{SKH} (Note 2)		3			μs
SK LOW TIME t_{SKL} (Note 2)		2			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	V_{OL} = 0.8V, V_{OH} = 2.0V			2	μs
t_{PD0}	V_{IL} = 0.45V, V_{IH} = 2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 5 μs. e.g. if t_{SKL} = 2 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	01	0011	xxxx		Erase/write enable
EWDS	01	0000	xxxx		Erase/write disable
ERAL	01	0010	xxxx		Erase all registers
WRAL	01	0001	xxxx	D15−D0	Write all registers

NMC9313B has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9313B is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 10-bit instructions can be executed. The instruction format has a logical 0, 1 as start bits, four bits as an op code, and four bits of address. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

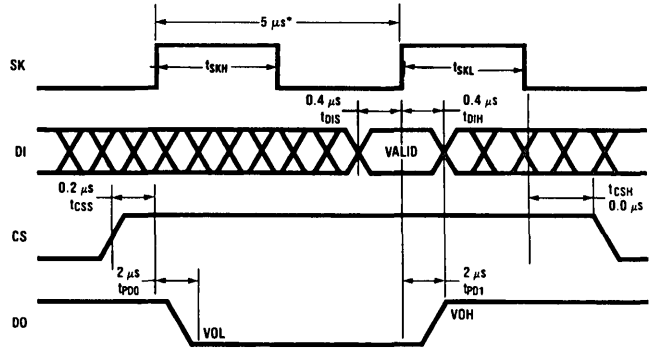
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

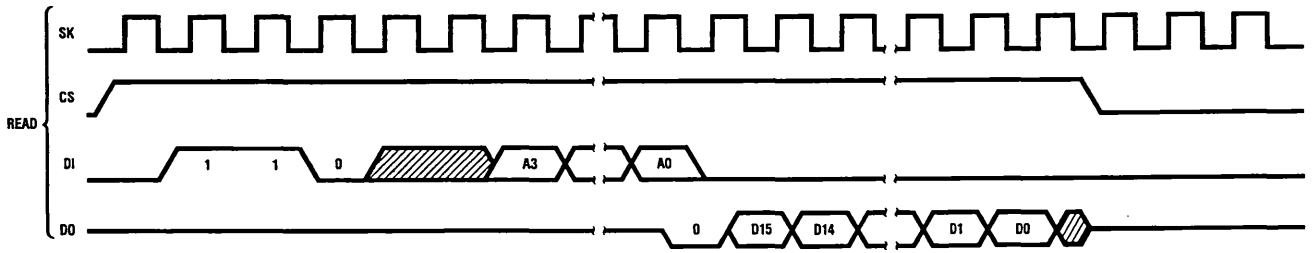
Timing Diagrams



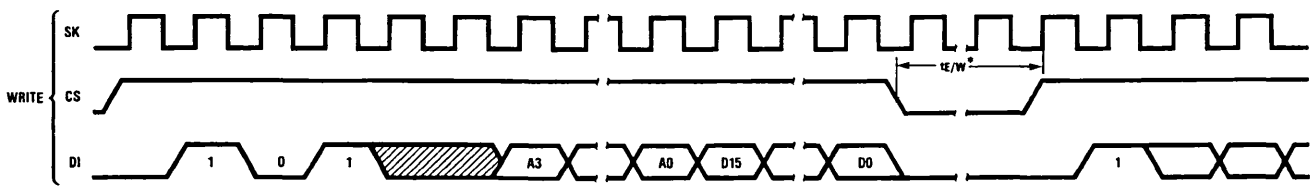
TL/D/9145–3

*This is the minimum SK period

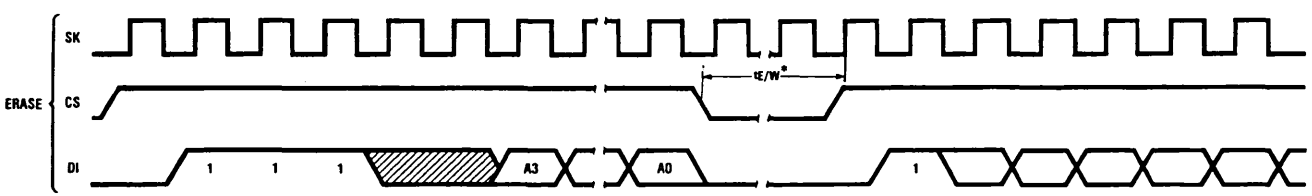
Synchronous Data Timing



TL/D/9145–4



TL/D/9145–5

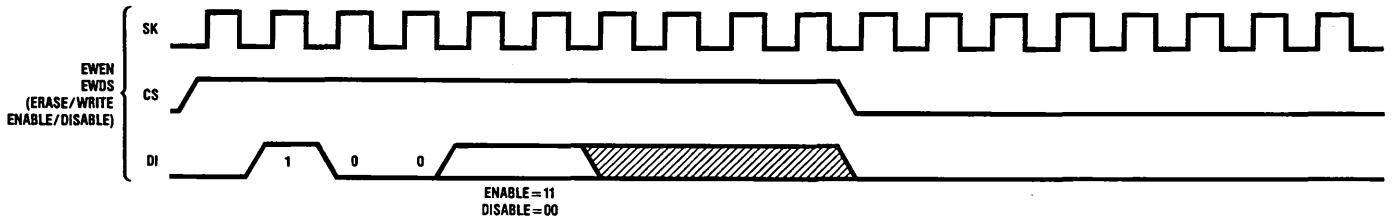


TL/D/9145–6

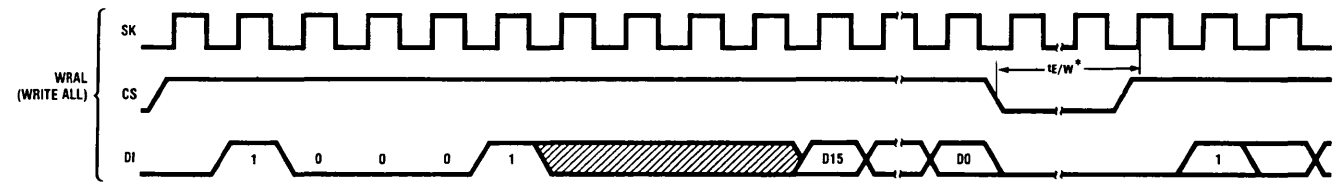
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing

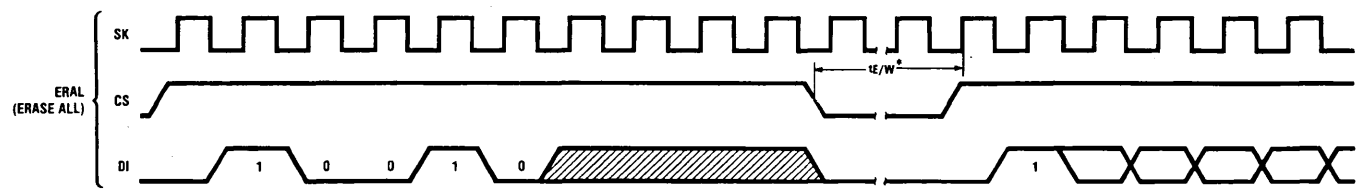
Timing Diagrams (Continued)



TL/D/9145–7



TL/D/9145–8



TL/D/9145–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor

NMC9346 1024-Bit Serial Electrically Erasable Programmable Memory

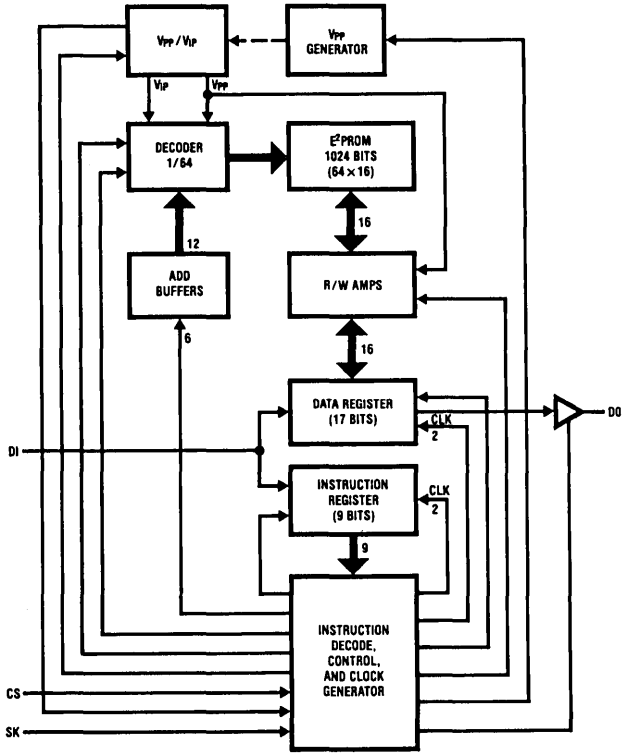
General Description

The NMC9346 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346 has been designed for applications requiring up to 4 x 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

- 40,000 erase/write cycles typical
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block Diagram



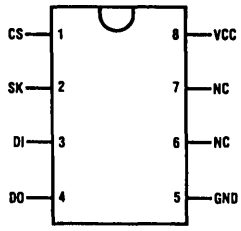
TL/D/9205–1

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	No Connection

3

Connection Diagrams

Dual-In-Line Package (N)

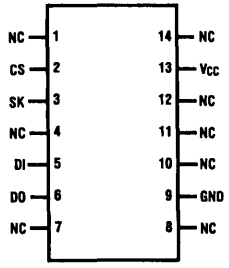


TL/D/9205-2

Top View

See NS Package Number N08E

14-Pin SO Package (M)

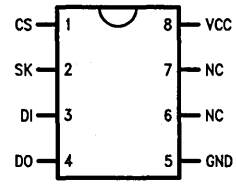


TL/D/9205-3

Top View

See NS Package Number M14B
Device Marking: 9346M14
9346EM14, 9346MM14

8-Pin SO Package (M8)



TL/D/9205-7

Top View

See NS Package Number M08A
Device Marking: 9346,
9346E, 9346M

Ordering Information

Commercial Temp. Range (0°C to +70°C)	Extended Temp. Range (−40°C to +85°C)	Military Temp. Range (−55°C to +125°C)
Order Number	Order Number	Order Number
NMC9346N	NMC9346EN	NMC9346MN
NMC9346M	NMC9346EM	NMC9346MM
NMC9346M8	NMC9346EM8	NMC9346MM8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD rating.	2000V

Operating Conditions

Ambient Storage Temperatures	
NMC9346	0°C to +70°C
NMC9346E	−40°C to +85°C
NMC9346M	−55°C to +125°C
Positive Supply Voltage	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{CC}	Operating Voltage	NMC9346, NMC9346E NMC9346M		4.5	5.5	V
I_{CC1}	Operating Current	NMC9346	V_{CC}=5.5V, CS=1, SK=1		12	mA
	Erase/Write Operating Current		V_{CC}=5.5V		12	mA
	Operating Current	NMC9346E	V_{CC}=5.5V, CS=1, SK=1		14	mA
	Erase/Write Operating Current		V_{CC}=5.5V		14	mA
	Operating Current	NMC9346M	V_{CC}=5.5V, CS=1, SK=1		15	mA
	Erase/Write Operating Current		V_{CC}=5.5V		15	mA

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC2}	Standby Current	NMC9346	V_{CC}=5.5V, CS=0		3	mA
	Standby Current	NMC9346E	V_{CC}=5.5V, CS=0		4	mA
	Standby Current	NMC9346M*	V_{CC}=5.5V, CS=0		5	mA
	Input Voltage Levels	NMC9346, NMC9346E, NMC9346M				
V_{IL}				−0.1	0.8	V
V_{IH}				2.0	V_{CC}+1	V
	Output Voltage Levels	NMC9346, NMC9346E, NMC9346M				
V_{OL}			I_{OL}=2.1 mA		0.4	V
V_{OH}			I_{OH}=−400 μA	2.4		V
I_{LI}	Input Leakage Current	NMC9346, NMC9346E, NMC9346M	V_{IN}=5.5V		10	μA
I_{LO}	Output Leakage Current	NMC9346, NMC9346E, NMC9346M	V_{OUT}=5.5V, CS=0		10	μA
	SK Frequency	MMC9346		0	250	kHz
t_{SKH}	SK High Time (Note 2)			1		μs
t_{SKL}	SK Low Time (Note 2)			1		μs
	SK Frequency	MMC9346E		0		kHz
	SK High Time (Note 2)			1	250	μs
	SK Low Time (Note 2)			1		μs
	SK Frequency	MMC9346M		0		kHz
	SK High Time (Note 2)			2	200	μs
	SK Low Time (Note 2)			1		μs
	Inputs	NMC9346, NMC9346E, NMC9346M				
t_{CSS}	CS			0.2		μs
t_{CSH}				0		μs
t_{DIS}	DI			0.4		μs
t_{DIH}				0.4		μs
	Output	NMC9346,	C_L=100 pF			
t_{pd1}	DO	NMC9346E,	V_{OL}=0.8V, V_{OH}=2.0V		2	μs
t_{pd0}		NMC9346M	V_{IL}=0.45V, V_{IH}=2.40V		2	μs
$t_{E/W}$	Self-Timed Program Cycle	NMC9346			10	ms
	Self-Timed Program Cycle	NMC9346E			10	ms
	Self-Timed Program Cycle	NMC9346M			12	ms
t_{CS}	Min CS Low Time (Note 3)	NMC9346, NMC9346E, NMC9346M		1		μs
t_{SV}	Rising Edge of CS to Status Valid	NMC9346, NMC9346E, NMC9346M	C_L=100 pF		1	μs
t_{OH}, t_{IH}	Falling Edge of CS to DO TRI-STATE®	NMC9346, NMC9346E, NMC9346M			0.4	μs
	Endurance	NMC9346, NMC9346E, NMC9346M	Data Changes per Bit	Typical 40,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g., if t_{SKL} = 1 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

*Thruout this table "M" refers to temperature range (−55°C to +125°C), not package.

Functional Description

The NMC9346 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. The NMC9346 is organized as sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming enable instruction (EWEN) is needed to keep the part in the enable state if the power supply (V_{CC}) noise falls below operating range. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

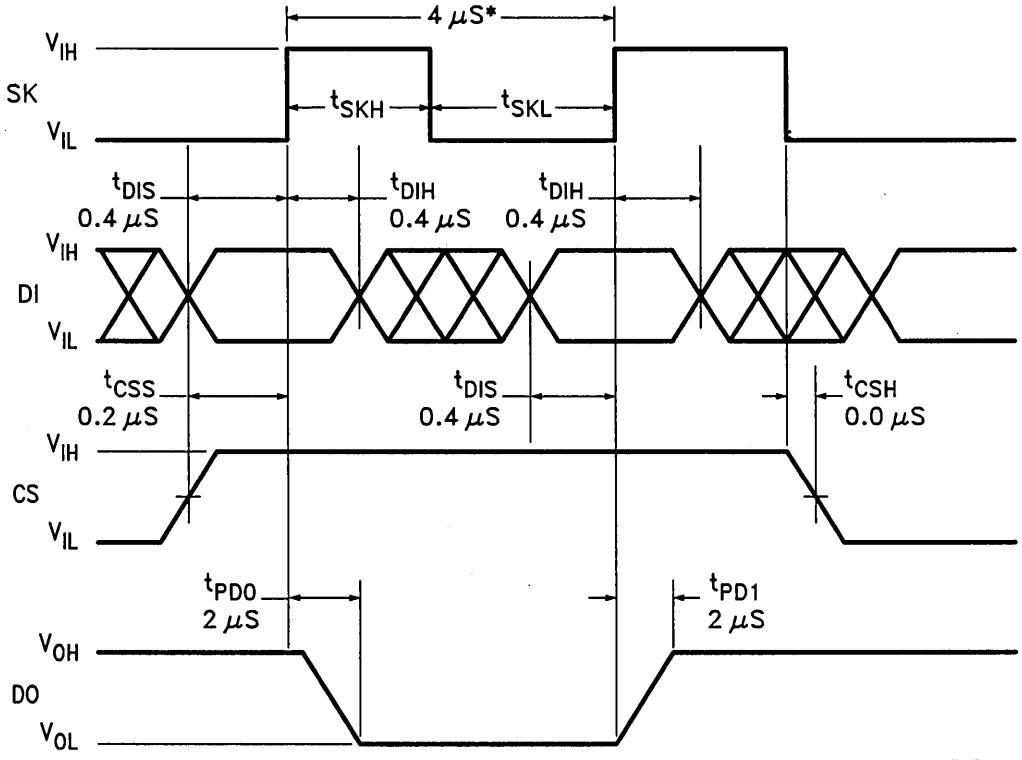
Instruction Set for NMC9346

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read Register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write Register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase Register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/Write Enable
EWDS	1	00	00xxxx		Erase/Write Disable
ERAL	1	00	10xxxx		Erase All Registers
WRAL	1	00	01xxxx	D15–D0	Write All Registers

NMC9346 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Timing Diagrams

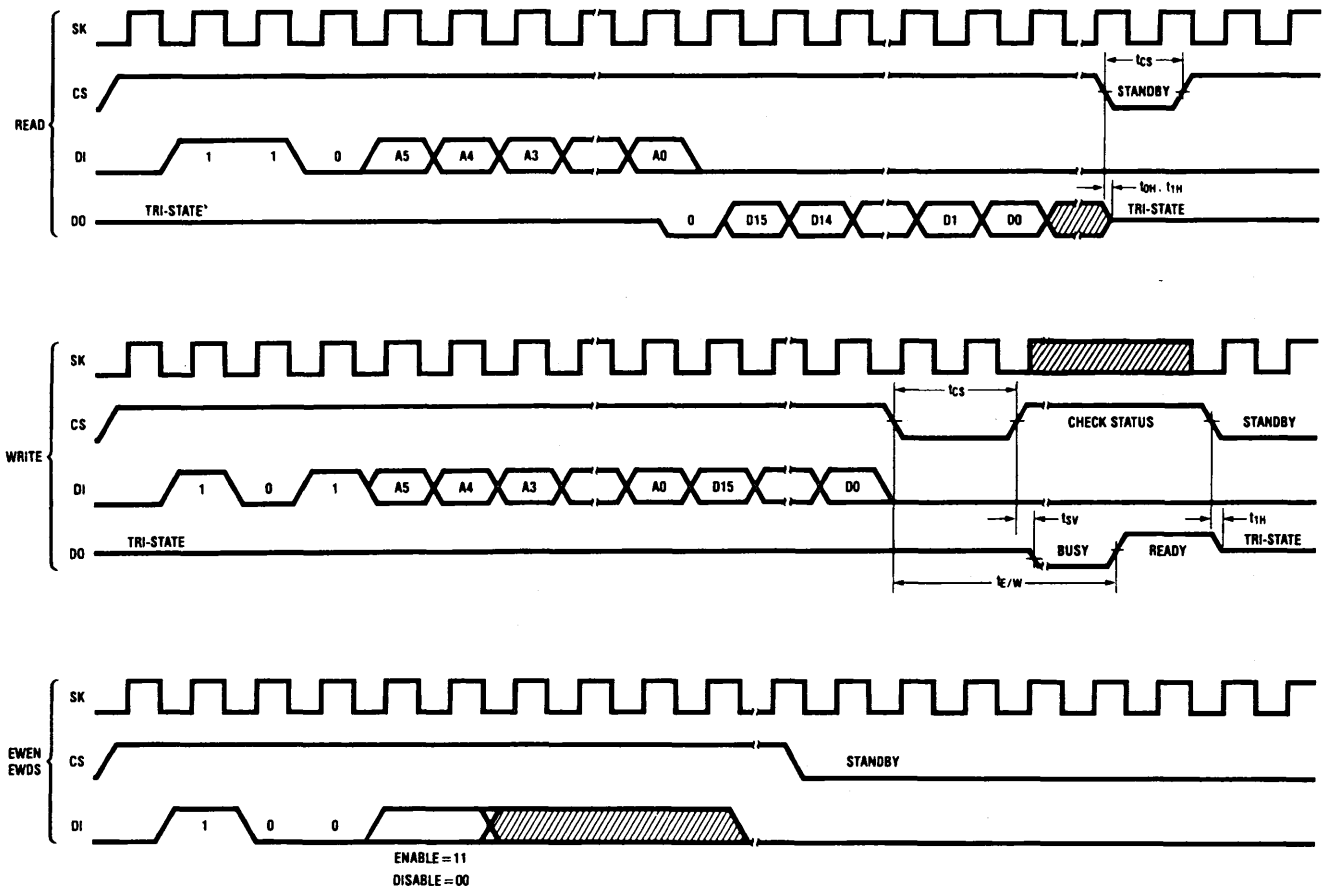
Synchronous Data Timing



TL/D/9205–4

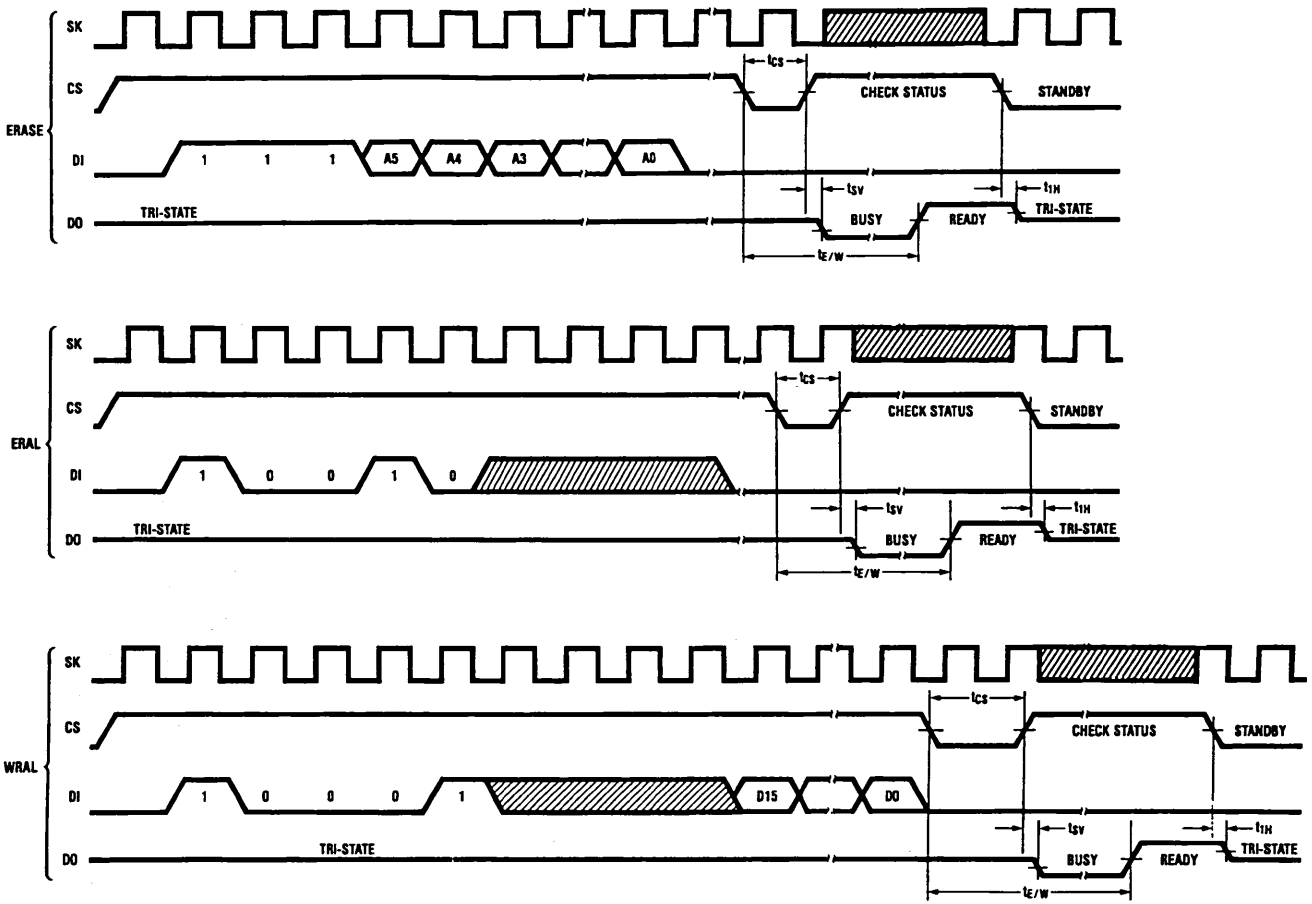
*This is the minimum SK period (5 μs for NMC9306M)

Instruction Timing



TL/D/9205–5

Instruction Timing



TL/D/9205–6

National Semiconductor

NMC9314B 1024-Bit Serial Electrically Erasable Programmable Memory

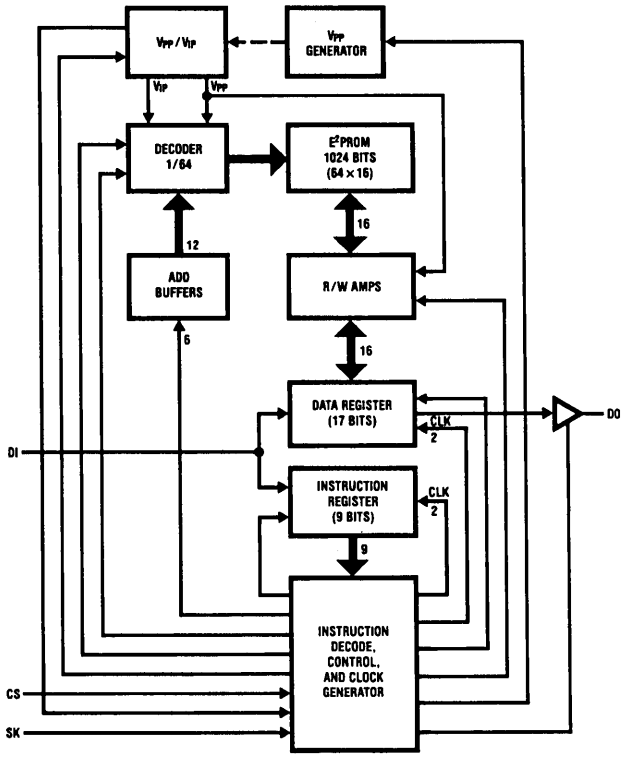
General Description

The NMC9314B is a 1024-bit non-volatile, sequential E^2PROM, fabricated using advanced N-channel E^2PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9314B has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

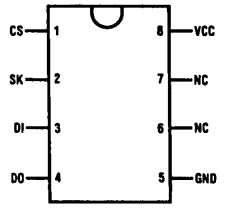
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



TL/D/9144–1

Dual-In-Line Package (N)



TL/D/9144–2

Top View

Order Number NMC9314N
See NS Package N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temp.	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	>2000V

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC}=5.5V$, CS=1, SK=1 $V_{CC}=5.5V$		17 17	mA mA
I_{CC2}	Standby Current	$V_{CC}=5.5V$, CS=0		5	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+0.5$	V
	Output Voltage Levels				
V_{OL}		$I_{OL}=2.1$ mA		0.4	V
V_{OH}		$I_{OH}=-400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN}=5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=5.5V$, CS=0		10	μA
	SK Frequency		0	200	kHz
t_{SKH}	SK High Time (Note 2)		3		μs
t_{SKL}	SK Low Time (Note 2)		2		μs
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L=100$ pF			
t_{pd1}	DO	$V_{OL}=0.8V$, $V_{OH}=2.0V$		2	μs
t_{pd0}		$V_{IL}=0.45V$, $V_{IH}=2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			15	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L=100$ pF		1	μs
t_{0H}, t_{IH}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 5 μs. e.g., if $t_{SKL} = 2\ \mu s$ then the minimum $t_{SKH} = 3\ \mu s$ in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9314B

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9314B has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9314B is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write). The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E^2PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

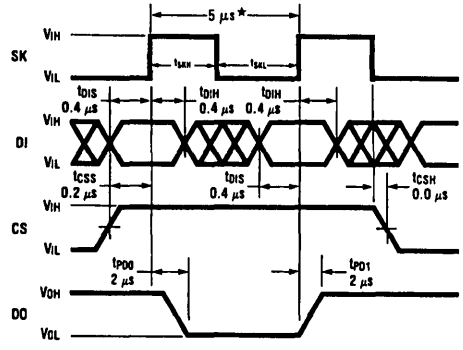
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

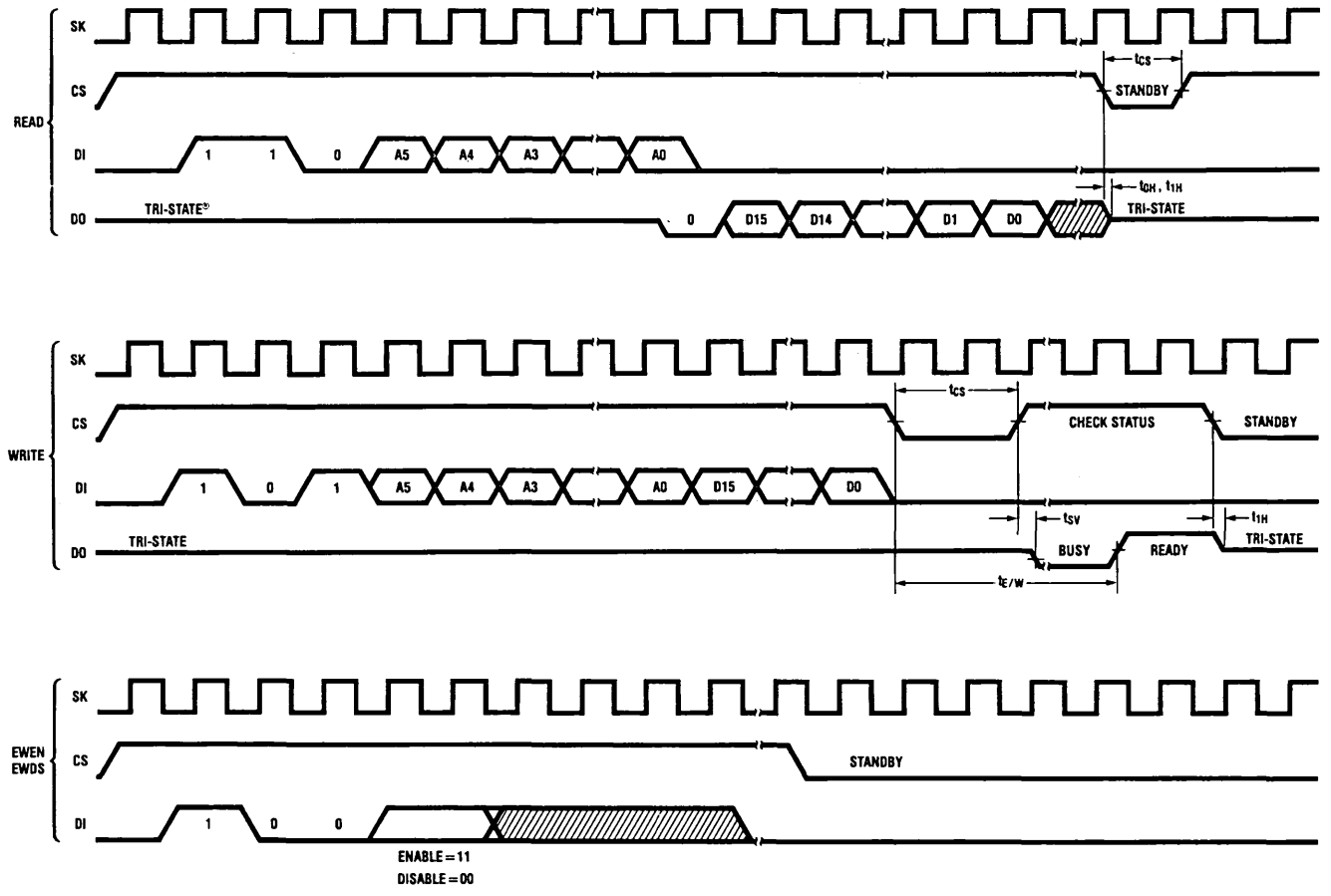
Synchronous Data Timing



TL/D/9144–3

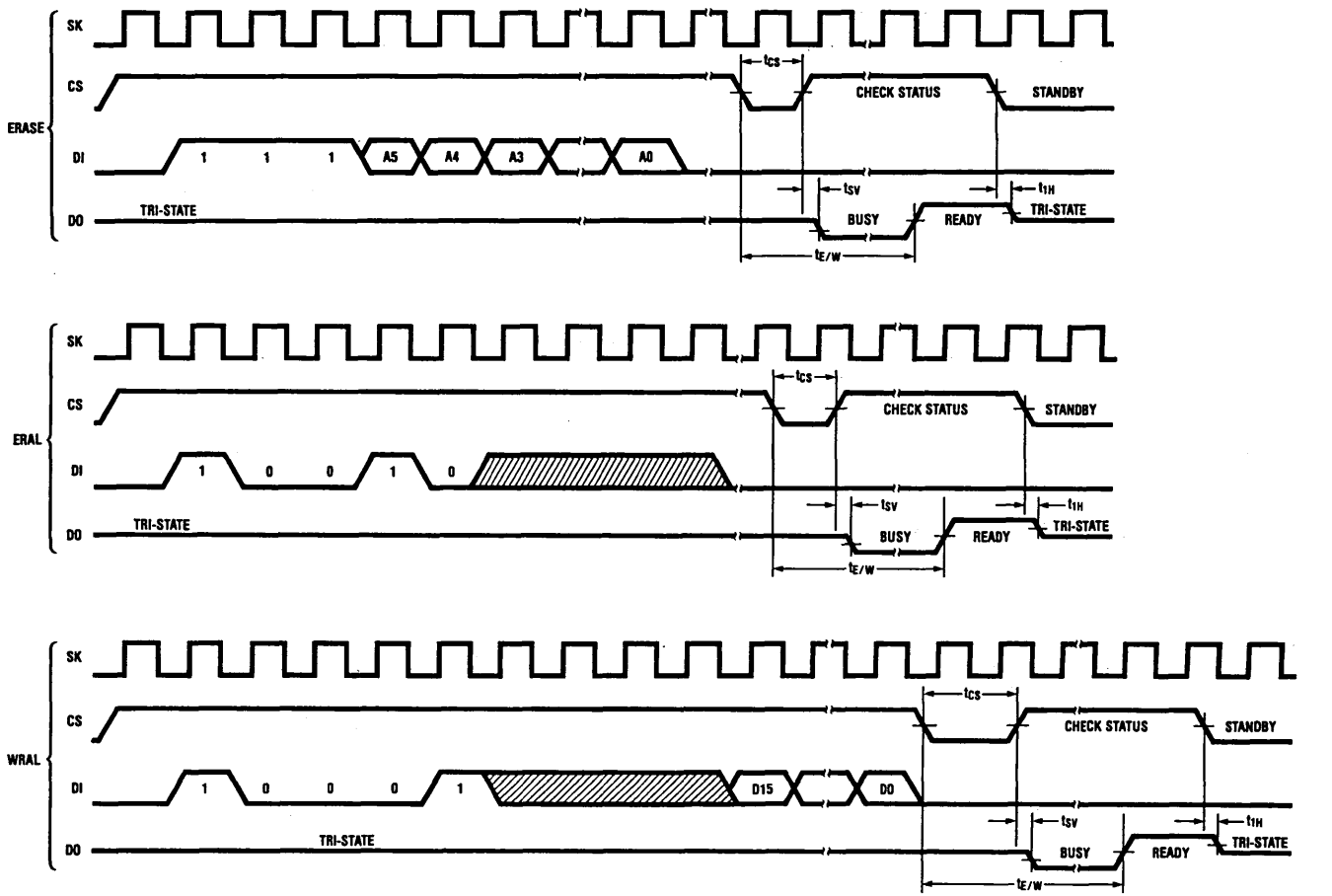
*This is the minimum SK period.

Instruction Timing



TL/D/9144–4

Instruction Timing



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National Semiconductor

NMC93C56/C66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93C56/NMC93C66 are 2048/4096 bits of CMOS electrically erasable memory divided into 128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 5V supply since V_{PP} is generated on-board. The serial organization allow the NMC93C56/66 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status come out on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The NMC93C56/66 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming capability with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

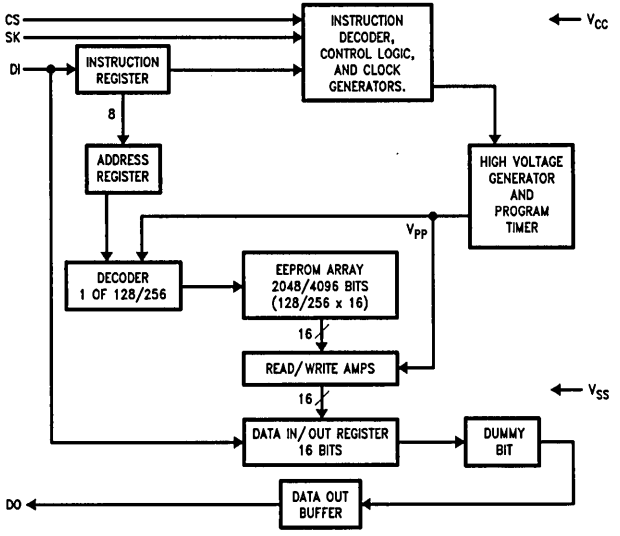
Compatibility with Other Devices

These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346 and CMOS EEPROMs NMC93C06/26/46. The NMC93C56/66 are both pin and function compatible with the NMC93C06/26/46, 256/512/1024-bit EEPROM with the one exception that the NMC93C56/66 require 2 additional address bits.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5V only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 10 years data retention
- Typical 40,000 writes

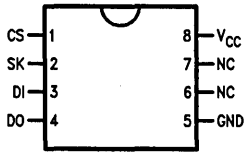
Block Diagram



TL/D/9617-1

Connection Diagrams

Dual-In-Line Package (N)



TL/D/9617-2

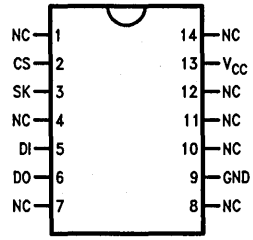
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

SO Package (M)



TL/D/9617-3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93C56N/NMC93C66N
NMC93C56M/NMC93C66M

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93C56EN/NMC93C66EN
NMC93C56EM/NMC93C66EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93C56MN/NMC93C66MN
NMC93C56MM/NMC93C66MM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Ambient Operating Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C56/NMC93C66	0°C to +10°C
NMC93C56E/NMC93C66E	−40°C to +85°C
NMC93C56M/NMC93C66M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M*	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	CS = 0V		50 100 100	µA
I_{IL}	Input Leakage	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA µA
I_{OL}	Output Leakage	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = −10 µA	 V_{CC} − 0.2	0.2	V V
f_{SK}	SK Clock Frequency	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	Relative to SK	50 100 100		ns

*Note: Throughout this table "M" refers to temperature range (−55°C to +125°C), not package type.

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93C56/NMC93C66 NMC93C56E/NMC93C66E NMC93C56M/NMC93C66M	AC Test CS = V_{IL}		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit	Typical 40,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93C56 and NMC93C66 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS):

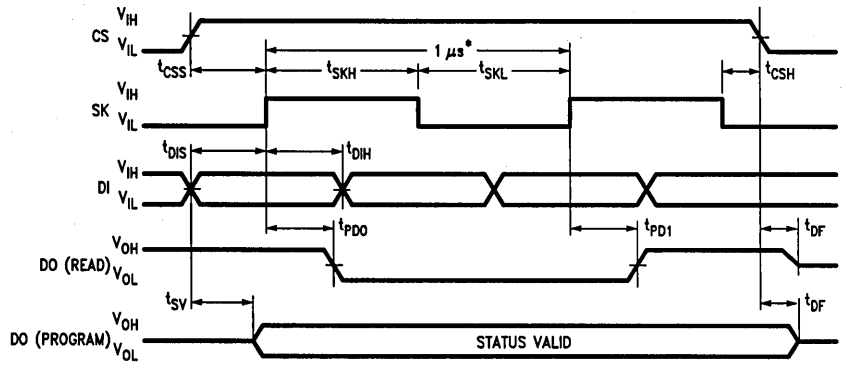
To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C56 and NMC93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers. Valid only when Protect Register is cleared.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



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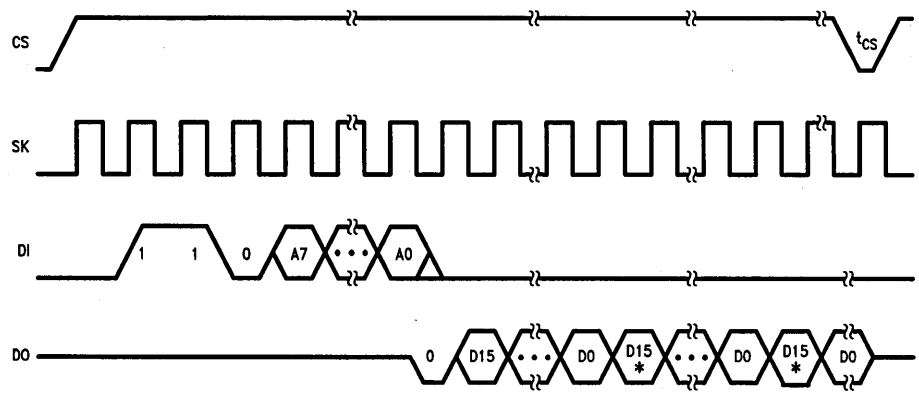
*This is the minimum SK period (Note 2).

READ:

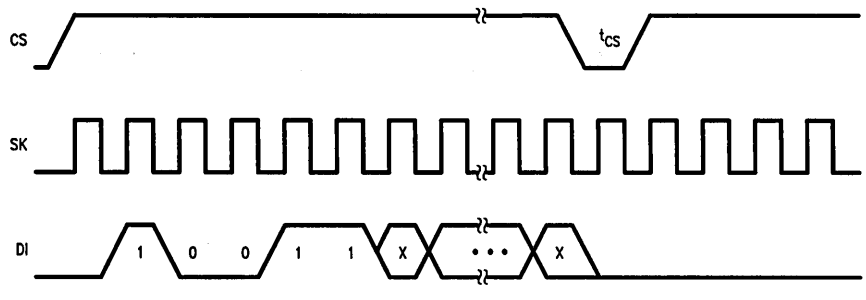


TL/D/9617–5

*Address bit A_7 becomes a "don't care" for NMC93C56.

*The memory automatically cycles to the next register.

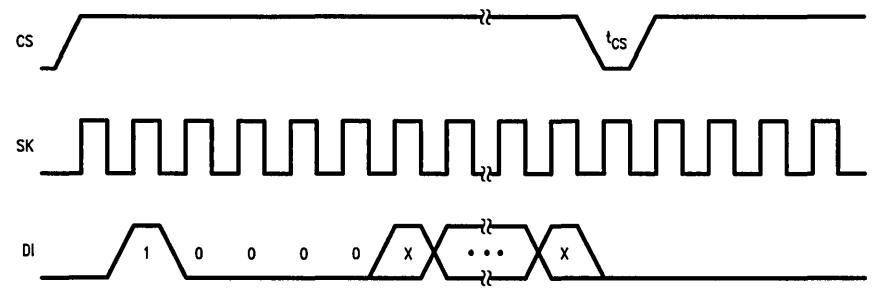
EWEN:



TL/D/9617–6

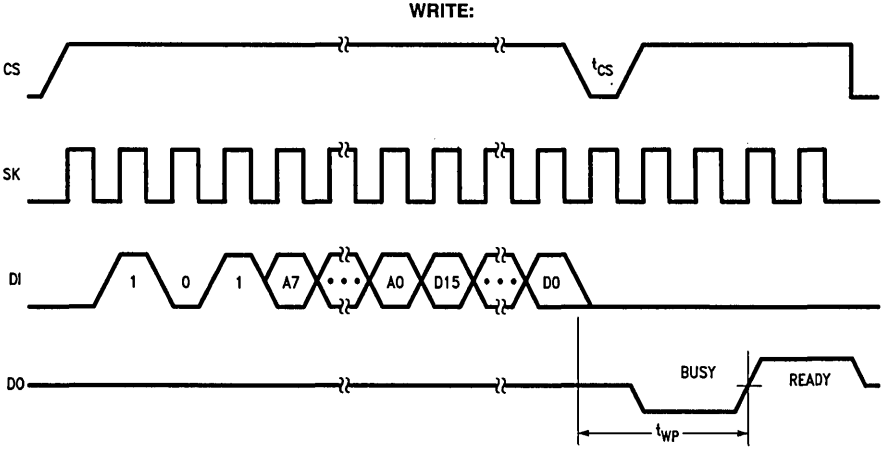
Timing Diagrams (Continued)

EWDS:



TL/D/9617-7

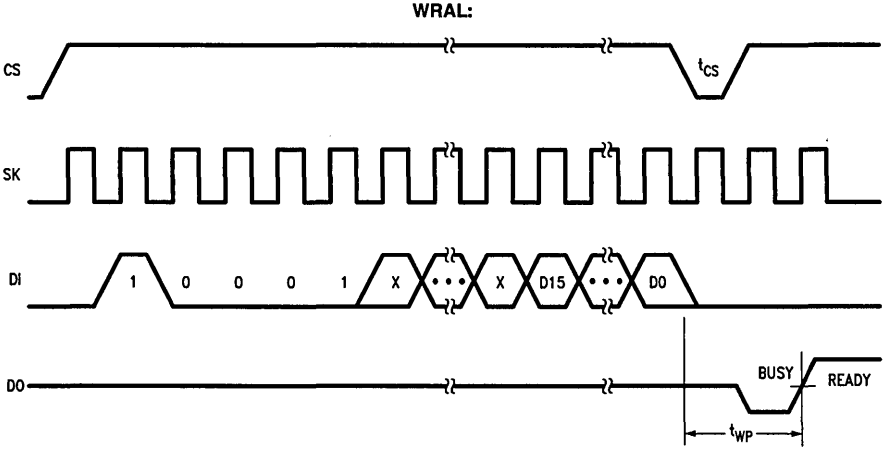
WRITE:



TL/D/9617-8

*Address bit A_7 becomes a "don't care" for NMC93C56.

WRAL:



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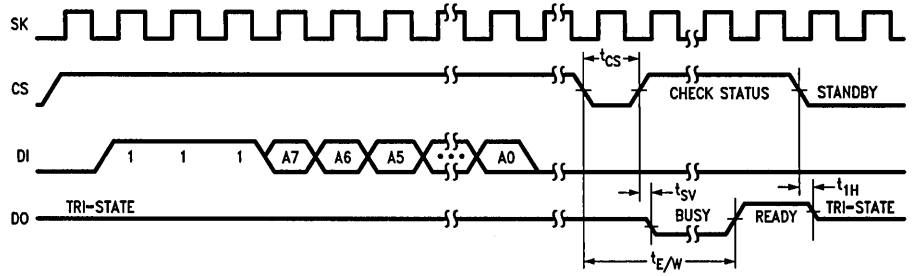
Timing Diagrams (Continued)

ERASE:



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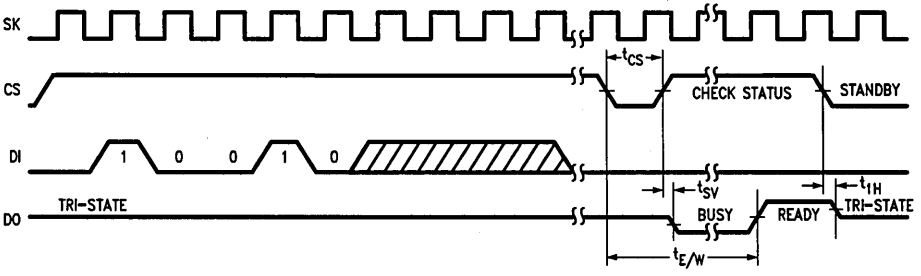
ERAL:



TL/D/9617–11

National Semiconductor

PRELIMINARY

NMC93CS56/CS66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Memories

General Description

The NMC93CS56/NMC93CS66 are 2048/4096 bits of read/write memory divided into 128/256 registers of 16 bits each. N registers (N ≤ 128 or N ≤ 256) can be protected against data modification by programming into a special on-chip register, called the memory "protect register", the address of the first register to be protected. This address can be "locked" into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the "protect register" will be aborted.

The "read" instruction loads the address of the first register to be read into an 8-bit address pointer. Then the data is clocked out serially on the "DO" pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 2048/4096 bits. Thus, the NMC93CS56/NMC93CS66 can be viewed as a non-volatile shift register.

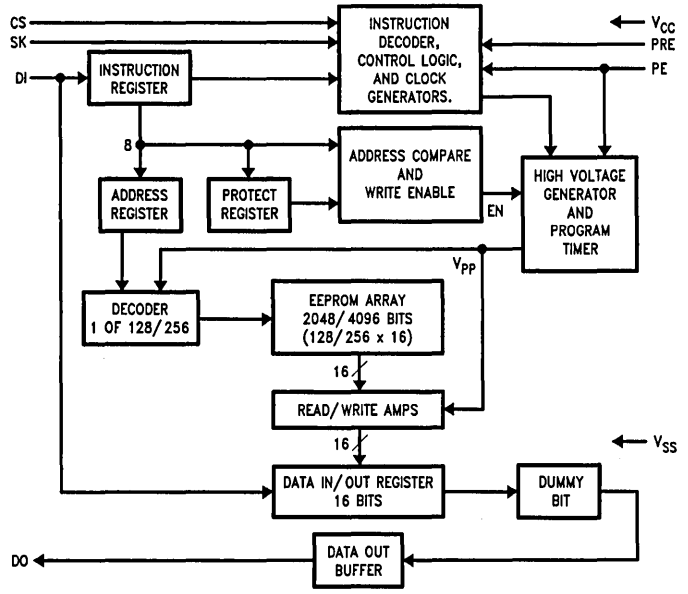
The "write" cycle is completely self-timed. No separate erase cycle is required before write. The "write" cycle is only enabled when pin 6 (program enable) is held "high". If the address of the register to be written is less than the address in the "protect register" then the data is written 16 bits at a time into one of the 128/256 data registers. If "CS" is brought "high" following the initiation of a "write" cycle, the "DO" pin indicates the ready/busy status of the chip.

National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 10 years.

Features

- Write protection in user defined section of memory
- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- Over 10 years data retention
- 40,000 write cycles typical

Block Diagram

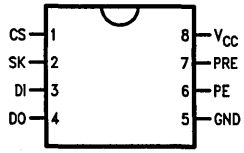


TL/D/9209-3

Connection Diagrams

PIN OUT:

Dual-In-Line Package (N)



TL/D/9209-1

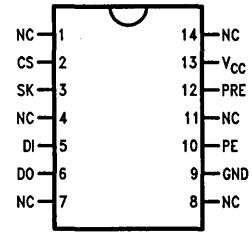
Top View

See NS Package Number N08E

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



TL/D/9209-2

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93CS56N/NMC93CS66N
NMC93CS56M/NMC93CS66M

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93CS56EN/NMC93CS66EN
NMC93CS56EM/NMC93CS66EM

Military Temp. Range (−55°C to +125°C)

Order Number
NMC93CS56MN/NMC93CS66MN
NMC93CS56MM/NMC93CS66MM

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Ambient Operating Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93CS56/MNC93CS66	0°C to +70°C
NMC93CS56E/NMC93CS66E	−40°C to +85°C
NMC93CS56M/NMC93CS66M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M*	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA μA
I_{OL}	Output Leakage	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V V
f_{SK}	SK Clock Frequency	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M		0 0 0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 2) (Note 3) (Note 3)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 4) (Note 5) (Note 5)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns
t_{PRES}	PRE Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns

*Thruout this table "M" refers to temperature range (−55°C to +125°C) not package.

DC and AC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns
t_{DIS}	DI Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to CS Relative to CS Relative to CS	250 500 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test CS = V_{IL}		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit.	Typical 40,000		cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

The NMC93CS56 and NMC93CS66 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The PE pin **MUST** be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin **MUST** be held "high" while loading the instruction. Following the PRREAD instruction the 8-bit address stored in the memory Protect Register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before

Instruction Set for the NMC93CS56 and NMC93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

3

Functional Description (Continued)

the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held "high" while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must *immediately* precede a PRWRITE instruction.

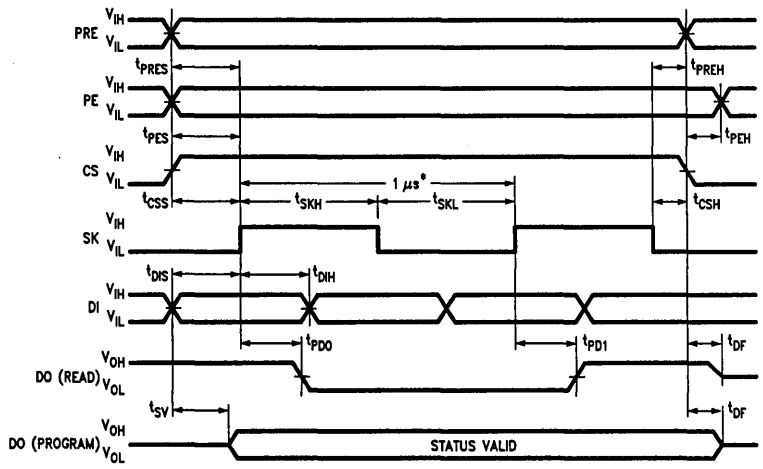
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one time only** instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **Immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing

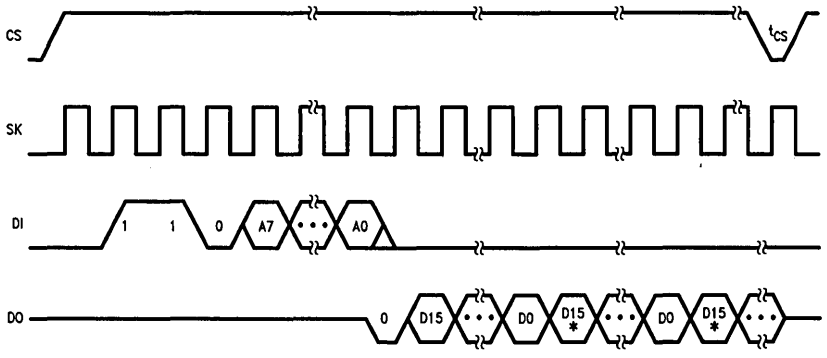


TL/D/9209-4

*This is the minimum SK period (See Note 2).

Timing Diagrams (Continued)

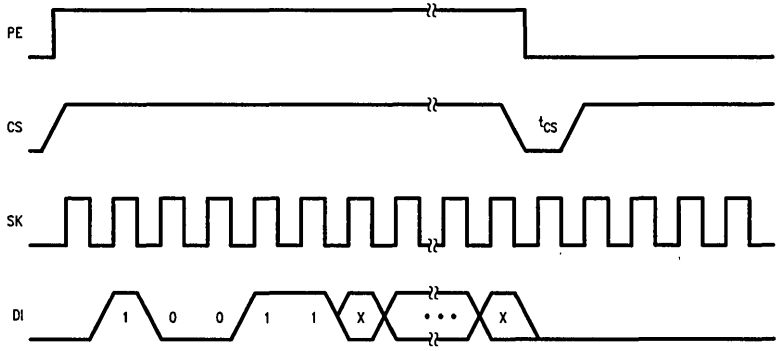
READ:*
PRE = 0, PE = X



TL/D/9209–5

*Address bit A_7 becomes a "don't care" for NMC93CS56.
*The memory automatically cycles to the next register.

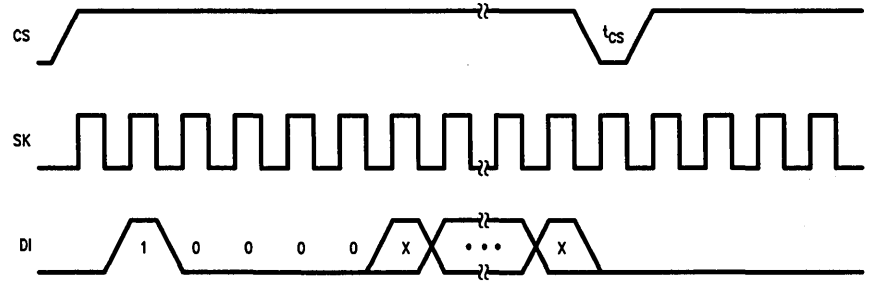
WEN:
PRE = 0, D0 = TRI-STATE



TL/D/9209–6

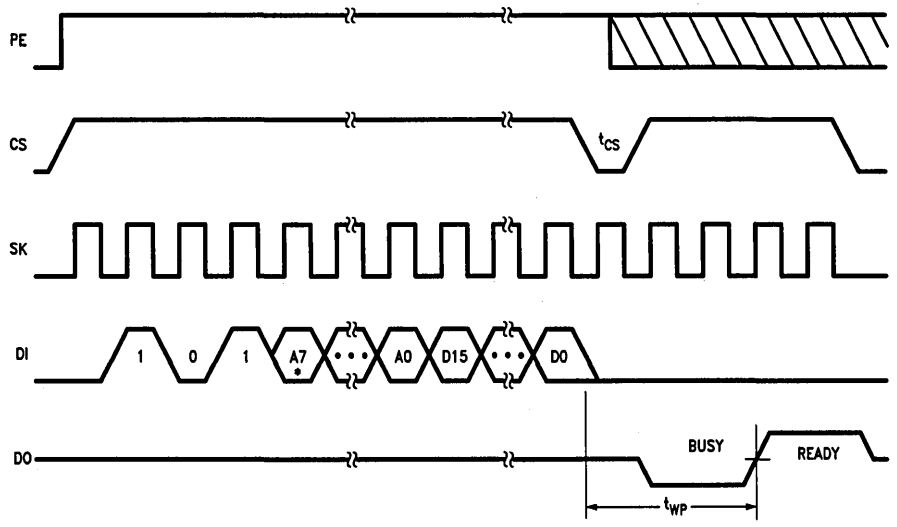
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/9209-7

WRITE:*
PRE = 0

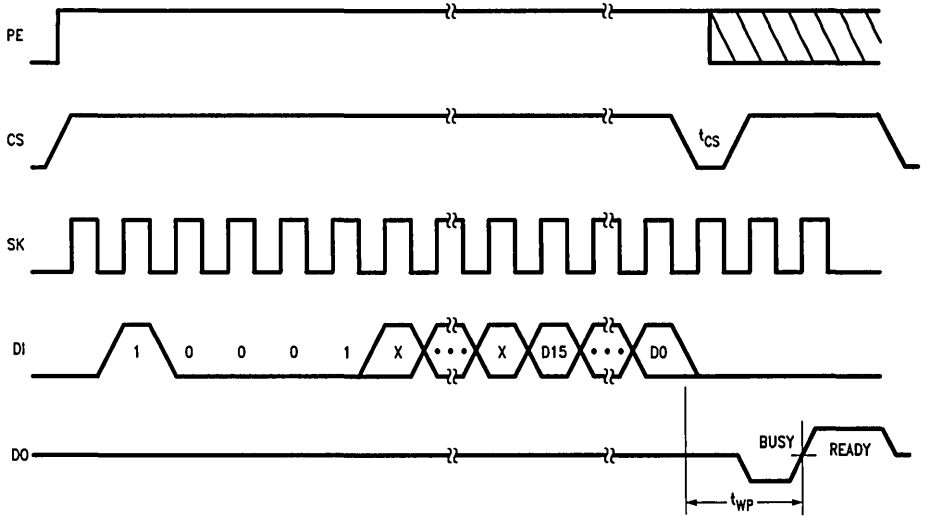


TL/D/9209-8

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

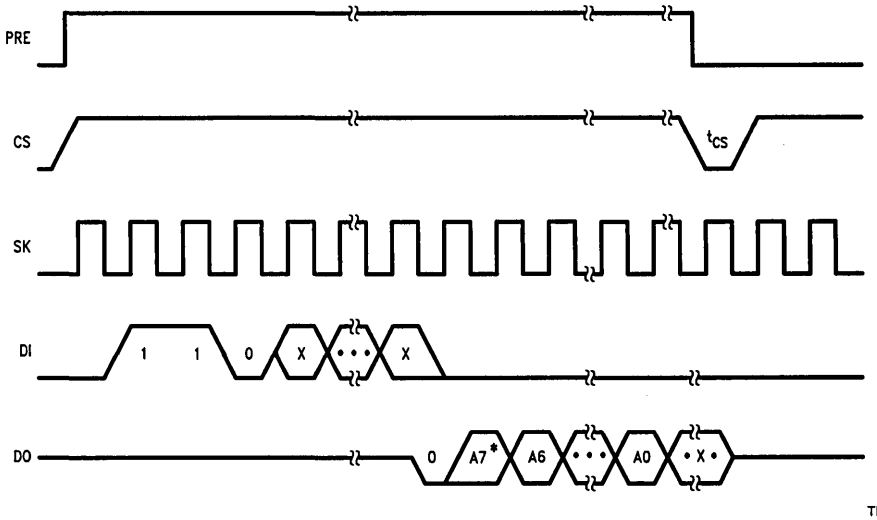
WRALL:*
PRE = 0



TL/D/9209–9

*Protect Register **MUST** be cleared.

PRREAD:*
PE = X

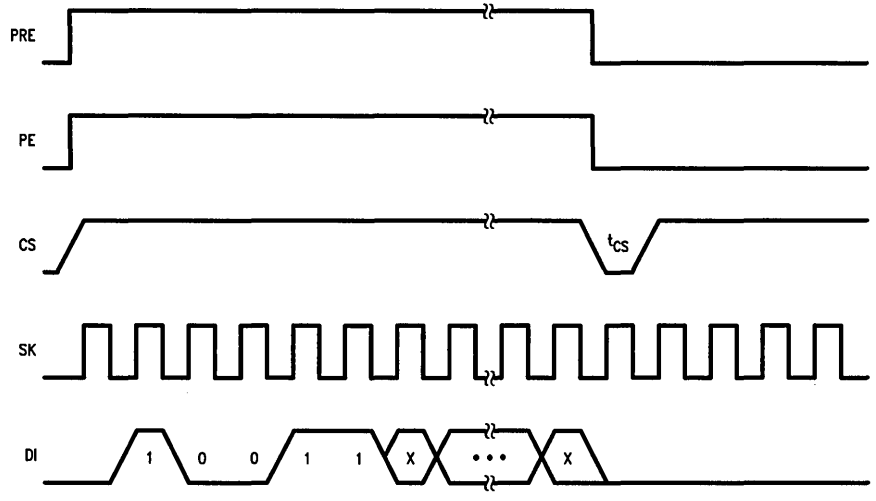


TL/D/9209–10

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

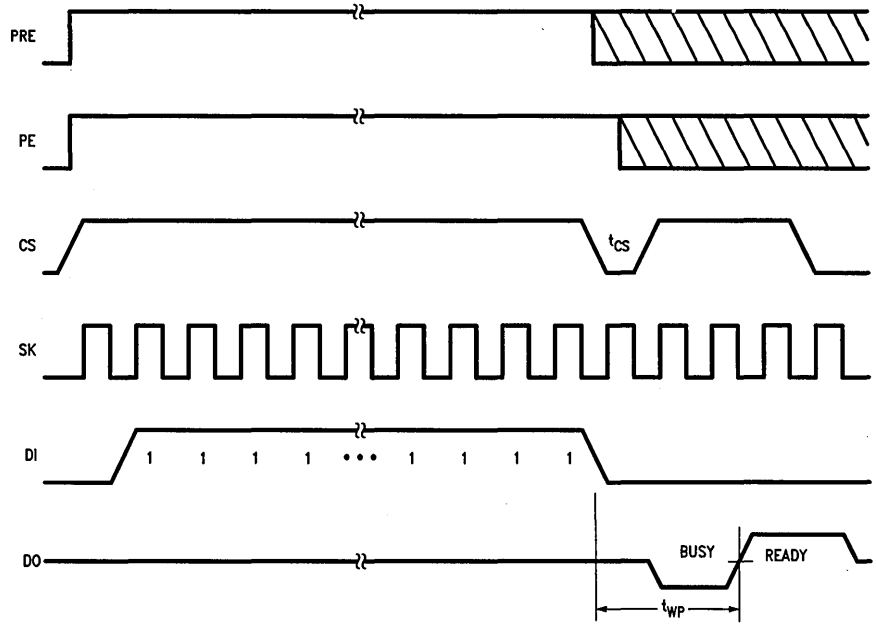
PREN:*
DO = TRI-STATE



TL/D/9209–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR:*

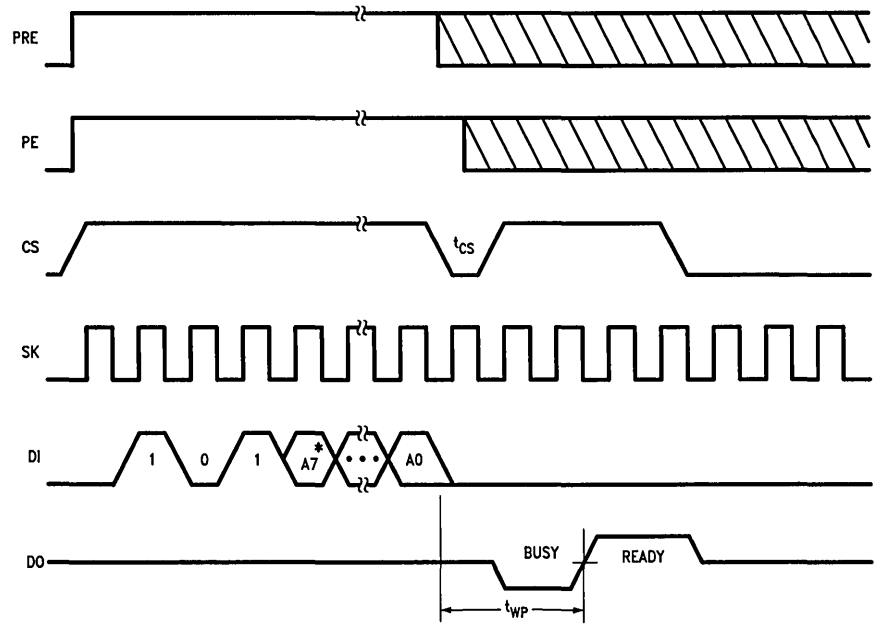


TL/D/9209–12

*A PREN cycle must **immediately** precede a PRCLEAR cycle.

Timing Diagrams (Continued)

PRWRITE:†

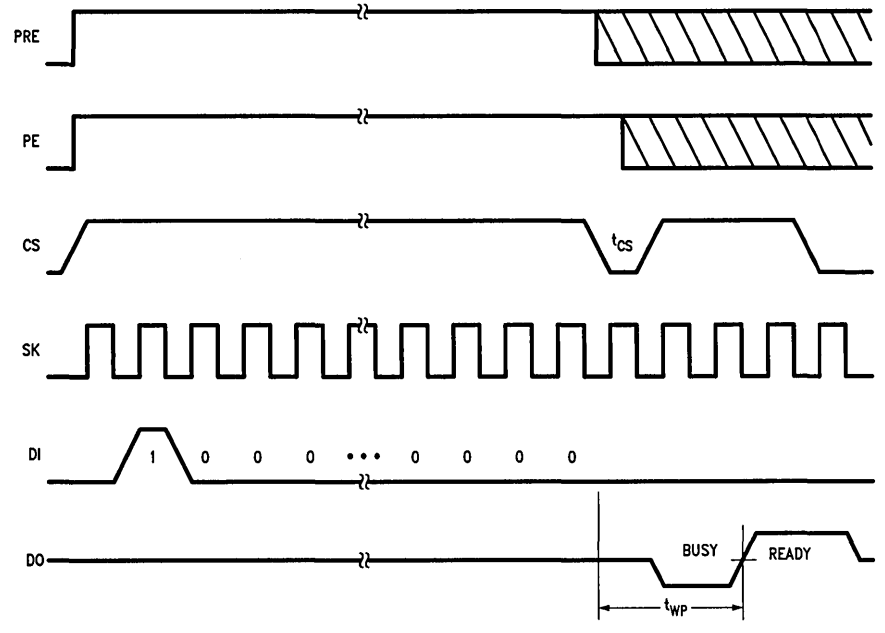


TL/D/9209–13

*Address bit A_7 becomes a "don't care" for NMC93CS56.

†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS:*



TL/D/9209–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor

NMC98C10/C20/C40
Electrically Erasable, Programmable Memories

General Description

The NMC98C10, NMC98C20 and NMC98C40 are 128 by 8, 256 by 8 and 512 by 8, 5-volt programmable, non-volatile, parallel access memories built with CMOS floating gate process. Data and address lines are multiplexed, enabling these devices to be packaged in an 18-pin DIP or 20-pin SO, saving board space. The pin-out is identical to the Intel 8185 static RAM and the 2001 non-volatile RAM, allowing the memories to directly interface with popular 8-bit and 16-bit microprocessors and microcontrollers.

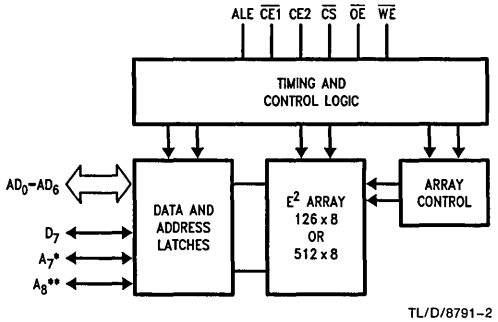
The write cycle is simplified by a self-timed erase before write circuit on-chip. The end of write cycle can be determined by polling the data pins or the controller can simply allow a minimum time between a write command and the subsequent command. To prevent undesirable modification of the memory contents during system power up or power down, a lockout circuit ignores write commands while V_{CC} is below the prescribed level of VLKO.

Applications for these memories include storing position data in robotic systems, storing local area network node address and parameter settings in data communications equipment, storing set-up and last position data in industrial control systems and storing PBX switch data in telecommunications equipment.

Features

- Single 5-volt supply
- Reliable CMOS floating gate process
- Eighteen-pin package
- Multiplexed address and data bus
- Self timed write operation
- 20,000 erase/write cycles typical
- Very low power dissipation
- Ten year data retention
- Minimum board space
- Directly compatible with NSC800, HPC and other standard microprocessors and microcontrollers
- No external sequencing of erase/write cycle

Block Diagram



TL/D/8791–2

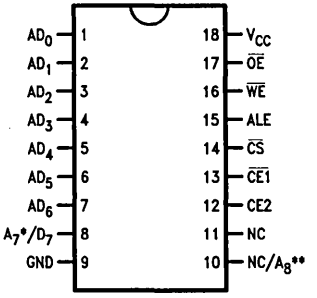
*A7 not used on NMC98C10
**A8 not used on NMC98C10 or NMC98C20

Pin Names

AD_0–AD_7	Multiplexed address and data bits. Pin 8 is DATA only for NMC98C10.
GND	Ground
A8	MSB of address for NMC98C40
NC	No Connection
CE2	Chip Enable 2
$\overline{CE1}$	Chip Enable 1
$\overline{CS}$	Chip Select
ALE	Address Latch Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package (N)



TL/D/8791-1

Top View

See NS Package Number N18A

*A7 not used on NMC98C10
**A8 not used on NMC98C10 or NMC98C20

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Parameter/Order Number	Comments
NMC98C10N/NMC98C20N NMC98C40N	Plastic 18-Pin DIP t_{LD} = 300 ns
NMC98C10N-1/NMC98C20N-1 NMC98C40N-1	Plastic 18-Pin DIP t_{LD} = 180 ns

Extended Temp. Range (−40°C to +85°C)

Parameter/Order Number	Comments
NMC98C10EN/NMC98C20EN NMC98C40EN	Plastic 18-Pin DIP t_{LD} = 300 ns
NMC98C10EN-1/NMC98C20EN-1 NMC98C40EN-1	Plastic 18-Pin DIP t_{LD} = 180 ns

Military Temp. Range (−55°C to +125°C)

Parameter/Order Number	Comments
NMC98C10MN/NMC98C20MN NMC98C40MN	Plastic 18-Pin DIP t_{LD} = 300 ns
NMC98C10MN-1/NMC98C20MN-1 NMC98C40MN-1	Plastic 18-Pin DIP t_{LD} = 180 ns

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin	−0.5V to 6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temp. (Soldering, 10 seconds)	300°C
ESD rating	>2000V

Operating Conditions

(Applies to DC and AC Characteristics)

Positive Supply Voltage	4.5V to 5.5V
Ambient Temperature	
Commercial	0°C to +70°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{LKO}	V_{CC} Level for Write Lockout		4.0		4.4	V
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$			±10.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$			±10.0	μA
I_{CC}	Operating Supply Current	TTL Inputs			15.0	mA
		CMOS Inputs			10.0	mA
I_{CCPD}	Standby Supply Current	TTL Inputs			5.0	mA
		CMOS Inputs			100	μA
I_{SC}	Short-Circuit Current	One Output Pin Shorted		40		mA

AC Electrical Characteristics

Symbol	Parameter	NMC98C10, NMC98C20, NMC98C40		NMC98C10-1, NMC98C20-1, NMC98C40-1		Units
		Min	Max	Min	Max	
t_{AL}	Address to Latch Setup Time	50		50		ns
t_{LA}	Address Hold Time after Latch	45		30		ns
t_{LC}	Latch to OE/WE Control	80		35		ns
t_{OE}	Valid Data Out Delay from Read Control		170		120	ns
t_{LD}	ALE to Data Out Valid		300		180	ns
t_{LL}	Latch Enable Width	100		60		ns
t_{OH}	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (Whichever Changes First)	0		0		ns
t_{OLZ}	$\overline{OE}$ Low to Output Driven	10		10		ns
t_{RDF}	Data Bus Float after Read	0	95	0	60	ns
t_{CL}	OE/WE Control to Latch Enable	0		0		ns
t_{CC}	OE/WE Control Width	250		150		ns
t_{DW}	Data In to Write Setup Time	150		150		ns
t_{WD}	Data In Hold Time after Write	20		15		ns
t_{SC}	Chip Select Set-Up to OE/WE Control	0		0		ns
t_{CS}	Chip Select Hold Time after OE/WE Control	0		0		ns
t_{ALCE}	Chip Enable Set-Up to ALE Falling	30		30		ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	NMC98C10, NMC98C20, NMC98C40		NMC98C10-1, NMC98C20-1, NMC98C40-1		Units
		Min	Max	Min	Max	
t_{LACE}	Chip Enable Hold Time after ALE Falling	45		40		ns
t_{WR}	Byte Write Cycle Time		20		20	ms
t_{WH}	Data Invalid Time after $\overline{WE}$ Falling		1		1	ms
Endurance	Number of Erase/Write Cycles	Typical 20,000		Typical 20,000		Cycles

Capacitance $T_A = 25°C$, f = 1 MHz (Note 3)

Parameter	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
$C_{I/O}$	Input/Output Capacitance	$\overline{OE} = \overline{CE1} = \overline{CS} = V_{IH}$, CE2 = V_{IL}		10	pF

AC Test Conditions

Output Load ..... 1 TTL Gate + C_L = 100 pF

Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.0V to 3.0V

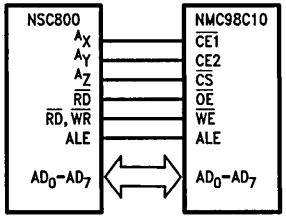
Input/Output Timing Reference Level ..... 0.8V to 2.0V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.

Note 3: This parameter is sampled and not 100% tested.

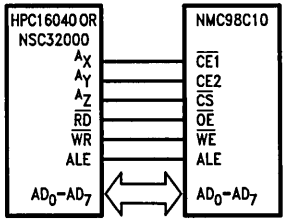
Typical Applications



TL/D/8791–5

Note: A_X, A_Y, A_Z are any three of the NSC800™ address pins A8–A15. By connecting $\overline{CE1}$, CE2, and $\overline{CS}$ to specific address lines, the NMC98C10, NMC98C20 and NMC98C40 can be mapped to a particular range in memory without the need for an external memory address decoder.

FIGURE 1. Using the NMC98C10 with an NSC800 Microcontroller



TL/D/8791–6

FIGURE 2. Using the NMC98C10 with the HPC 16040 Microcontroller or NSC Series 32000®

Functional Description

Table I shows the different modes of operation as a function of the control signals. Standby power down mode: both write and read are inhibited and the device's power consumption is greatly reduced. Standby power up mode: the device consumes the operating power, but read and write are inhibited. Inhibit mode: the device is write protected to avoid inadvertent modifications while the read and write pins are changing.

READ OPERATION

Figure 3 shows the timing diagram for READ operation. The address is latched on the falling edge of ALE. The NMC98C10 pins 1 through 7 are used for address bits, the NMC98C20 uses pin 8 in addition, the NMC98C40 uses pins 8 and 10 in addition to pins 1 through 7 for address bits.

Data appear on pins 1 through 8 after $\overline{OE}$ becomes active (low).

WRITE OPERATION

Figure 4 shows the timing for a write operation. Address is latched on the falling edge of ALE. CE1 and CE2 are latched on the falling edge of ALE with the addresses. The write cycle is initiated by cycling $\overline{WE}$ low for the specified time. The internally timed write cycle begins on the falling edge of $\overline{WE}$. No external ERASE cycle is needed since there is an internally timed ERASE before WRITE. The internal programming cycle requires 20 ms maximum, although once the minimum external cycle is completed the interface signals may change.

Before initiating any subsequent operations, the internally timed programming cycle must be completed. The completion of the programming cycle can be determined by $\overline{DATA}$ POLLING, as described below, or by simply waiting 20 ms after the falling edge of $\overline{WE}$.

$\overline{DATA}$ POLLING

After the write operation is initiated, its conclusion can be monitored by putting the device in the READ mode and polling the D7 data bit. The data bit will be logical inverse of the bit being written to a location in memory until the write operation is completed. At this time the D7 data bit will be the same as the last D7 data bit written into memory.

WRITE LOCKOUT

During system power up or power down, an on-chip write lockout circuit prevents spurious WRITES into the memory locations while V_{CC} is lower than the specified lockout voltage V_{LKO}. This frees the system designer from having to design external write protection circuits.

TABLE I. Mode Table

Mode	$\overline{CE1}$*	CE2*	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit†	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

V_{IL} = Logical Low Input

V_{IH} = Logical High Input

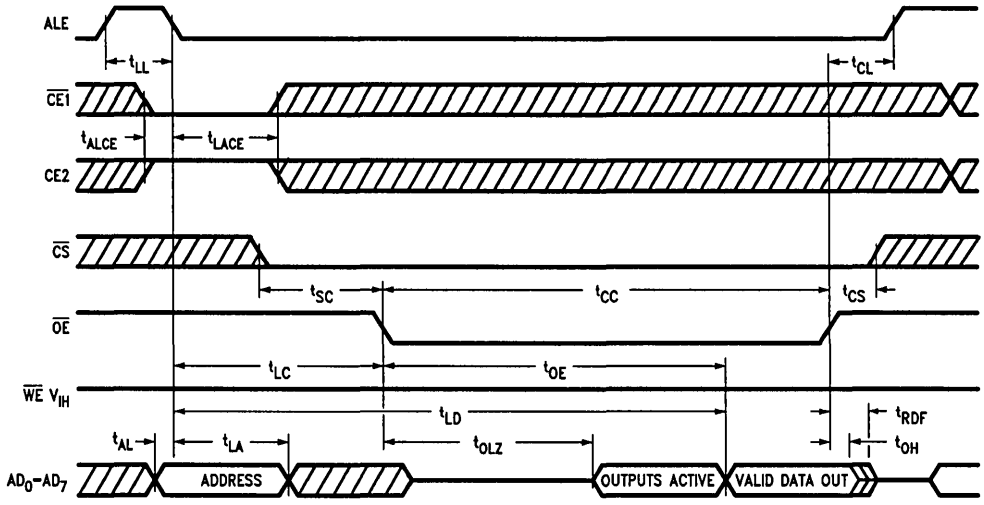
Hi-Z = High Impedance State

X = Don't Care

* = $\overline{CE1}$ and CE2 are latched by ALE

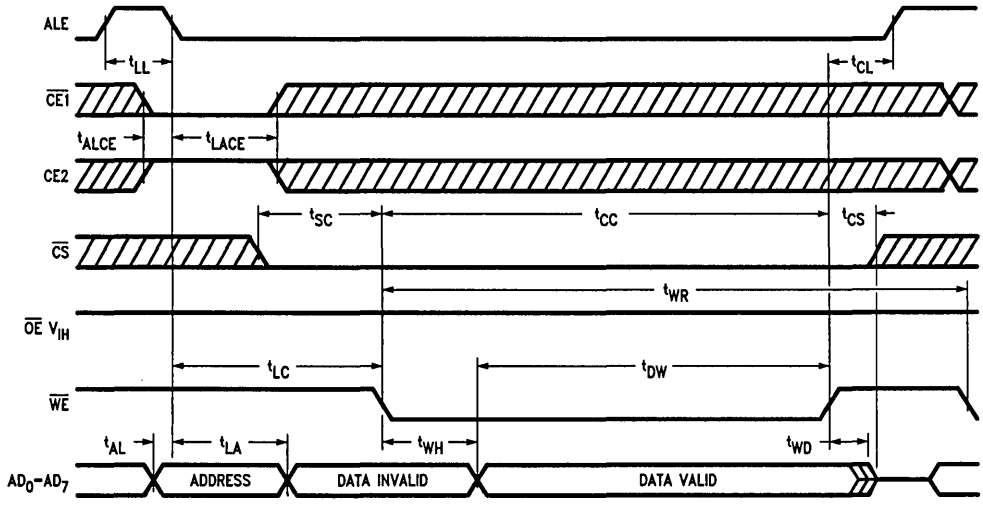
† = This inhibit mode not recommended

Timing Waveforms



TL/D/8791–3

FIGURE 1. Read Timing



TL/D/8791–4

FIGURE 2. Write Timing

Note: When ALE is high, address latch is in "fall through" state. If $\overline{OE}$ goes low, output will go active. With isolation resistors between the driver and AD_0–AD_7, the output will change, thereby changing inputs.

3

Protecting Data in Serial EEPROMs

National Semiconductor
Application Brief 15
Paul Lubeck

National offers a broad line of serial interface EEPROMs which share a common set of features:

- Low cost
- Single supply in all modes (+5V ± 10%)
- TTL compatible interface
- MICROWIRE™ compatible interface
- Read-Only mode or read-write mode

This Application Brief will address protecting data in any of National's Serial Interface EEPROMs by using read-only mode.

Whereas EEPROM is non-volatile and does not require V_{CC} to retain data, the problem exists that stored data can be destroyed during power transitions. This is due to either uncontrolled interface signals during power transitions or noise on the power supply lines. There are various hardware design considerations which can help eliminate the problem although the simplest most effective method may be the following programming method.

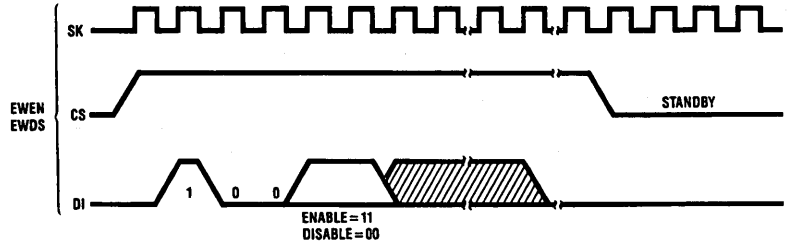
All National Serial EEPROMs, when initially powered up are in the Program Disable Mode*. In this mode it will abort any requested Erase or Write cycles. Prior to Erasing or Writing it is necessary to place the device in the Program Enable Mode†. Following placing the device in the Program Enable Mode, Erase and Write will remain enabled until either executing the Disable instruction or removing V_{CC}. Having V_{CC} unexpectedly removed often results in uncontrolled interface signals which could result in the EEPROM interpreting a programming instruction causing data to be destroyed.

Upon power up the EEPROM will automatically enter the Program Disable Mode. Subsequently the design should incorporate the following to achieve protection of stored data.

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.
2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return

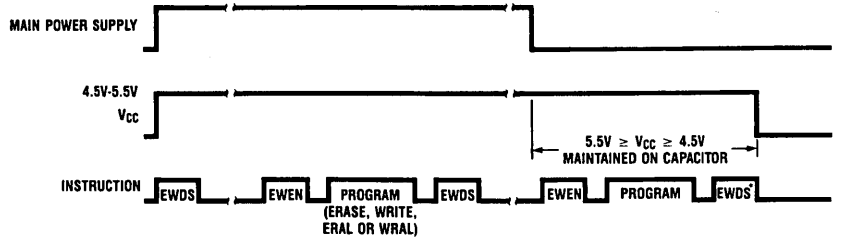
*EWDS or WDS, depending on exact device.

†EWEN or WEN, depending on exact device.



TL/D/7085-1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085-2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Electronic Compass Calibration Made Easy With E^2 Memory, NMC9306

National Semiconductor
Application Brief 18
Doug Zrebski

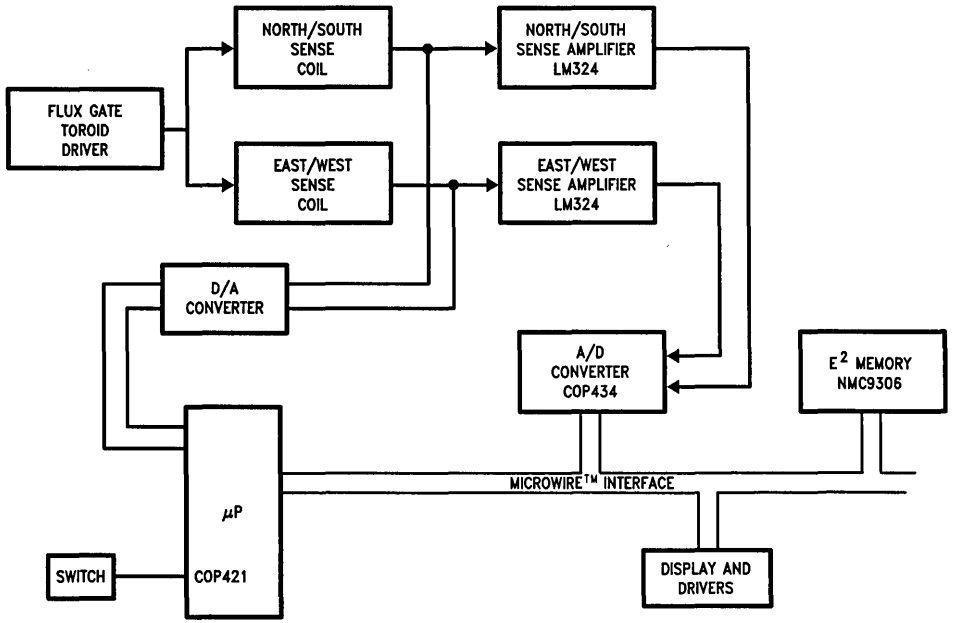
When a compass is first installed in a vehicle, or when new equipment, such as car speakers, are added to a vehicle with a compass, the compass must be compensated for stray magnetic fields. With a magnetic compass, it must be pointed towards magnetic north and then adjusted. This procedure is repeated at all four main points of the compass until the compass is calibrated. This procedure is lengthy and also requires another calibrated compass to point the vehicle in the correct direction.

The block diagram illustrates an electronic compass that, with the aide of an E^2 memory, makes adjusting a compass as easy as pushing a button, and also eliminates the need for another compass. In addition it gives you the ability to adjust for variation between magnetic and true north. This is a major advantage because it is something that even the most expensive magnetic compass cannot do.

The brain of the electronic compass is the COP421 microcontroller. There are two sense coils, one for north/south and one for east/west. The output of each of the sense amplifiers is an analog voltage which is fed into the A to D converter. These voltages are read by the COP421 over the microwire interface. From these voltages, the microcontroller determines the direction and displays the results once again over the microwire interface. To compensate the compass in a new environment the procedure is very simple. Start by pointing the car in any direction and push the switch. The CPU at this time will measure the voltage at the sense amplifiers and store this information in the E^2 memory over the microwire interface. Now the vehicle is turned 180°, and the button is pushed again. The same procedure will be followed internally. The compensation procedures are now complete. During operation the CPU will compensate for stray fields by adding an analog voltage back into the sense amplifiers. This value is stored in E^2 memory and not lost when the power is turned off, but is readjustable if its environment is modified.

Compass variation is the difference between true and magnetic north. This variation differs all over the world and is something that must be taken into consideration when navigating by compass. With the E^2 memory device, a variance can be programmed in for any given location. In California this is approximately 17°, in Michigan approximately 1°. Once again, this cannot be accomplished by a magnetic compass, and would have been impossible to accomplish without an E^2 memory device.

Electronic Compass Block Diagram



TL/D/8613–1

Automatic Low Cost Thermostat

National Semiconductor
Application Brief 22
Kent Brooten

Ths application brief describes the use of the NMC9346 (64 x 16) serial EEPROM. With the advent of the inexpensive COPS™ family from National Semiconductor, heretofore "expensive" applications can now be realized inexpensively. Such an application is a low cost thermostat. Typical features of such a device are:

1) Ability to interface to local and remote temperature sensors,
2) Ability to hold changeable settings,
3) Digital display of present temperature,
4) Inexpensive in high volume.

CIRCUIT DESCRIPTION

The basis of the thermostat is the COP410 microcontroller. This, with the addition of 2 ADC0854 A/D converters, an NMC9346 EEPROM and some logic for LED display, comprise an extremely versatile, yet low cost, system. The ADC0854 allows 4 channels of temperature sensors, 1 local and 3 remote. Temperature sensors used are LM34 (for readings in °F) or LM35 (for readings in °C).

While there are several possible choices for A/D converters that are MICROWIRE™ compatible, the ADC0854 was chosen because of its "settability". By presetting the "cold" temperature (i.e., when the cooling unit should come on—say 80°F) all the microcomputer has to do is to multiplex the inputs and read the data in line. Similarly, the "hot" A/D can be preset to the temperature where the furnace should come on (e.g., 60°F) and scanned in a like manner. Since the microcomputer is also keeping time of day, selecting an A/D with more "smarts" (as in the ADC0854) the software can be kept manageable and an external real time clock chip is not needed.

The EEPROM (NMC9346) holds the presettable temperature ranges (high and low settings) by day of the week. Since data is in EEPROM rather than in mask ROM, it can be changed.

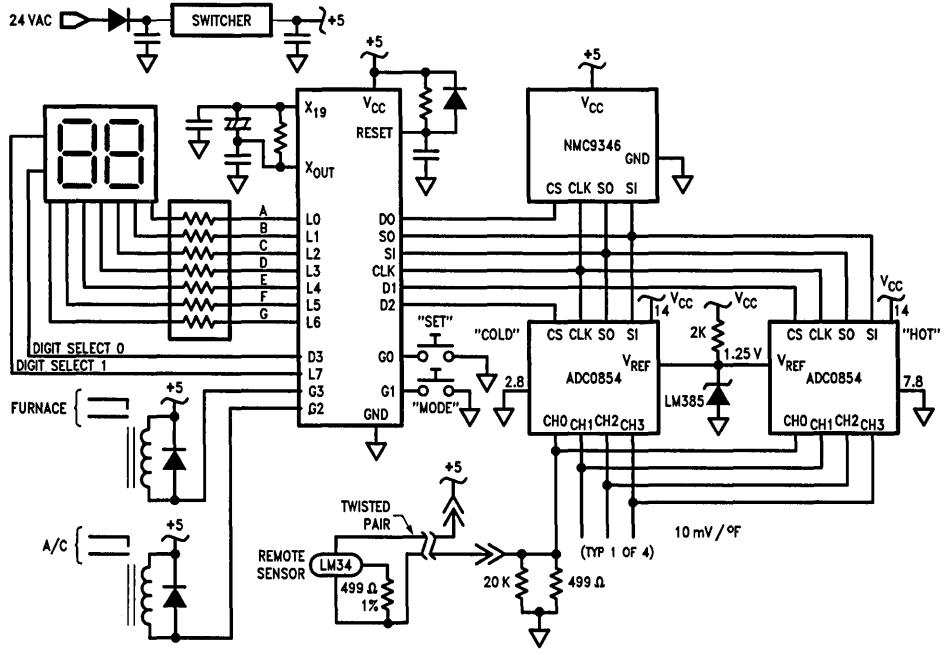
The LED display is multiplexed by the microcomputer. Depending on the type of display selected, external drivers may be necessary.

Input power is typically 24 VAC. Using a linear regulator would cause too much heat to be dissipated, which would upset the local temperature sensors. Thus, a switch mode regulator must be used. Fortunately, National Semiconductor has provided a solution to the problem with the LM3578, a switching regulator in an 8-pin mini-DIP, providing more than enough current for the application, using only a minimum of external components.

SOFTWARE DESCRIPTION

Since a real time clock is implemented in software, all routines must execute the same number of cycles independent of the input. Because of the flexibility of the COPS family instruction set, this is not as difficult a problem as it first appears. Since the EEPROM contains the settings that are periodically sent to the A/D converters, the COPS program merely fetches data from one source and dumps it to another while monitoring the output. Even the SET and MODE keys can be acted upon in a predictable manner IF the software designer carefully plans the program flow BEFORE writing code.

Note: Also see App Brief 15.



TL/D/8647–1

FIGURE 1

Designing with the NMC9306/COP494 a Versatile Simple to Use E² PROM

National Semiconductor
Application Note 338
Masood Alavi

This application note outlines various methods of interfacing an NMC9306/COP494 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NMC9306; as well as how serial data outputted from an NMC9306 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NMC9306/COP494.

The third part of the application note shows a list of various applications that can use a NMC9306/COP494.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

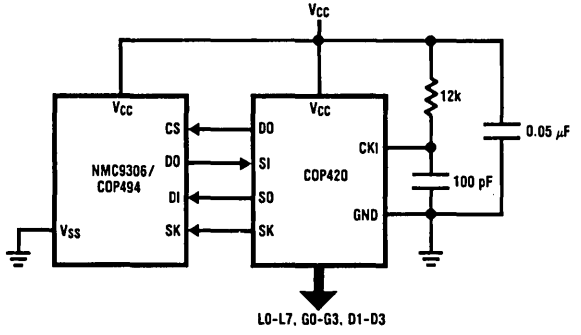
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E²PROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NMC9306/COP494 — COP420 Interface

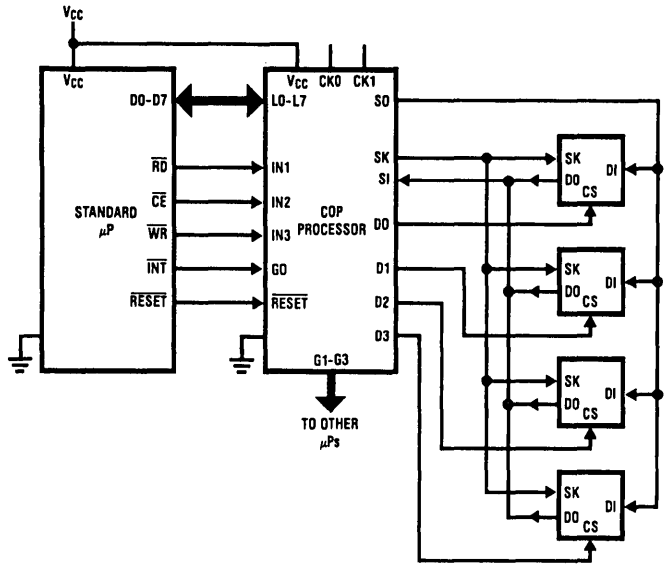
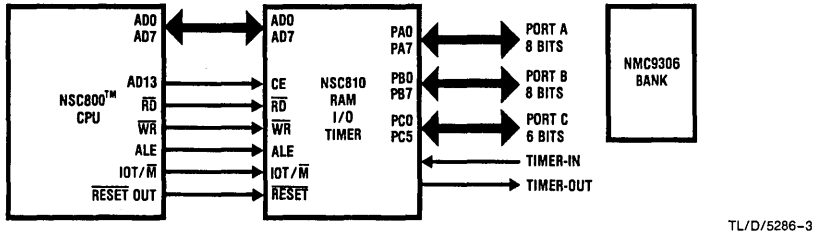


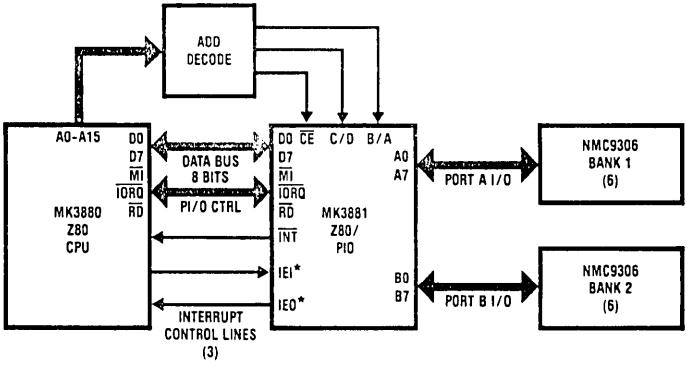
FIGURE 2. NMC93O6 — Standard μP Interface Via COP Processor



PA0 → SK
PA1 → DI/DO
} Common to all 9306's
PA2–7 → 6CS for 6– 9306's

* SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.
* CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.

FIGURE 3. NSC800™ to NMC9306 Interface (also Valid for 8085/8085A and 8156)

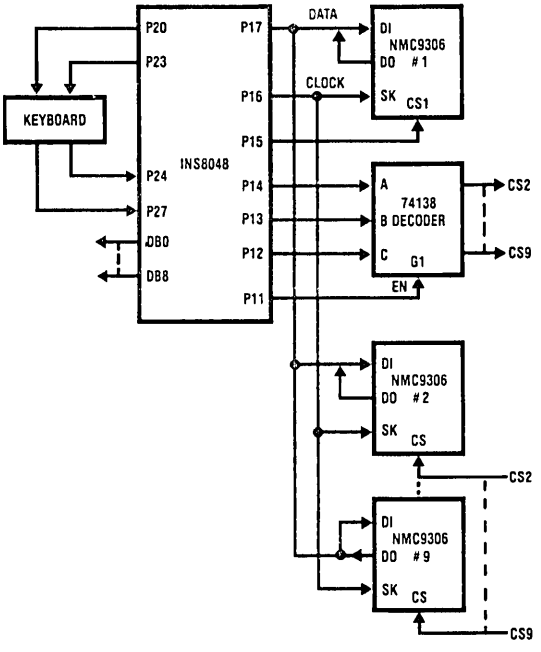


TL/D/5286–4

Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

FIGURE 4. Z80 — NMC9306 Interface Using Z80-PIO Chip

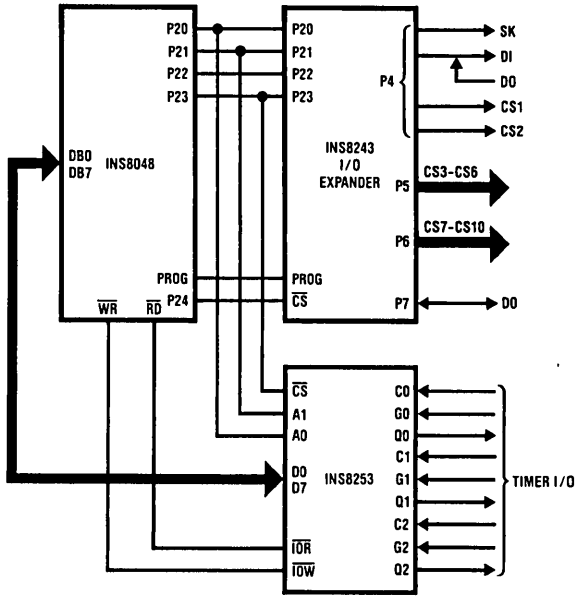


TL/D/5286–5

* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NMC9306 frequency range.

* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP — NMC9306 Interface

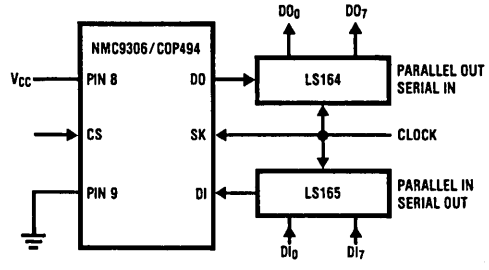


TL/D/5286–6

Expander outputs

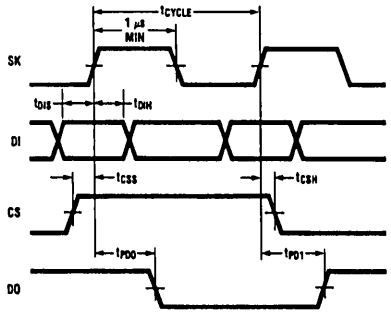
	DI SK	(COMMON)
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion



TL/D/5286–7

FIGURE 7. Converting Parallel Data into Serial Input for NMC9306/COP494



Min	Max
t_{CYCLE} 0	250 kHz
t_{DIS} 400	ns
t_{D1H} 400	ns
t_{CSS} 200	ns
t_{CSH} 0	ns
t_{PD0}	2 μs
t_{PD1}	2 μs

TL/D/5286–8

FIGURE 8. NMC9306/COP494 Timing

THE NMC9306/COP494

Extremely simple to interface with any μP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Serial Clock input
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read, TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

*Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

**DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NMC9306/COP494

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most μPs this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard μP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 μs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for a minimum of ten years independent of V_{CC}, which may be on or off. Read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NMC9306 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

The following is a list of various systems that could use a NMC9306/COP494

A. Airline terminal
   Alarm system
   Analog switch network
   Auto calibration system
   Automobile odometer
   Auto engine control
   Avionics fire control
B. Bathroom scale
   Blood analyzer
   Bus interface
C. Cable T.V. tuner
   CAD graphics
   Calibration device
   Calculator—user programmable
   Camera system
   Code identifier
   Communications controller
   Computer terminal
   Control panel
   Crystal oscillator
D. Data acquisition system
   Data terminal
E. Electronic circuit breaker
   Electronic DIP switch
   Electronic potentiometer
   Emissions analyzer
   Encryption system
   Energy management system
F. Flow computer
   Frequency synthesizer
   Fuel computer
G. Gas analyzer
   Gasoline pump
H. Home energy management
   Hotel lock
I. Industrial control
   Instrumentation
J. Joulemeter
K. Keyboard -softkey
L. Laser machine tool
M. Machine control
   Machine process control
   Medical imaging
   Memory bank selection
   Message center control
   Mobile telephone
   Modem
   Motion picture projector
N. Navigation receiver
   Network system
   Number comparison
O. Oilfield equipment
P. PABX
   Patient monitoring
   Plasma display driver
   Postal scale
   Process control
   Programmable communications
   Protocol converter
Q. Quiescent current meter
R. Radio tuner
   Radar dectector
   Refinery controller
   Repeater
   Repertory dialer
S. Secure communications system
   Self diagnostic test equipment
   Sona-Bouy
   Spectral scanner
   Spectrum analyzer
T. Telecommunications switching system
   Teleconferencing system
   Telephone dialing system
   T.V. tuner
   Terminal
   Test equipment
   Test system
   TouchTone dialers
   Traffic signal controller
U. Ultrasound diagnostics
   Utility telemetering
V. Video games
   Video tape system
   Voice/data phone switch
W. Winchester disk controller
X. X-ray machine
   Xenon lamp system
Y. YAG—laser controller
Z. Zone/perimeter alarm system

The NMC9346—An Amazing Device

National Semiconductor
Application Note 423
Stacy Deming

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NMC9346—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

2^{1024} = number of possible combinations

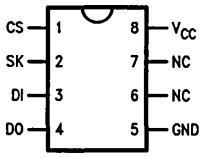
$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NMC9346 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NMC9346. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.

Dual-In-Line Package



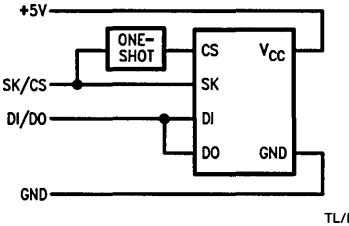
TL/D/8611–1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NMC9346 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

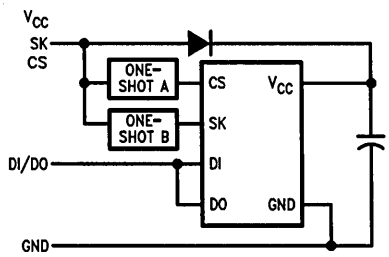


TL/D/8611–2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NMC9346 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611–3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

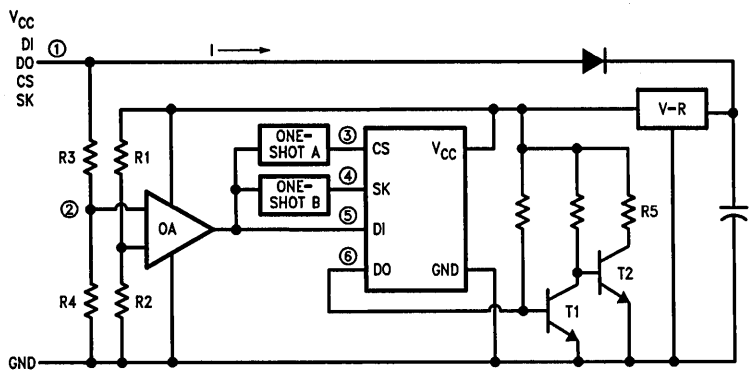
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

Conclusion

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

Note: The circuits in this application note feature the NMC9346. The NMC9306 is a pin-compatible part that stores 256 bits. The NMC9346 was used because it has a self-timing write cycle and the NMC9306 does not. Additional circuitry is not required to use the NMC9306, but an additional chip select signal must occur at the CS pin to terminate a write cycle.



TL/D/8611–4

R1 = 20K

R2 = 30K

R3 = 15K

R4 = 5K

One-Shot A = ½ MM74HC123

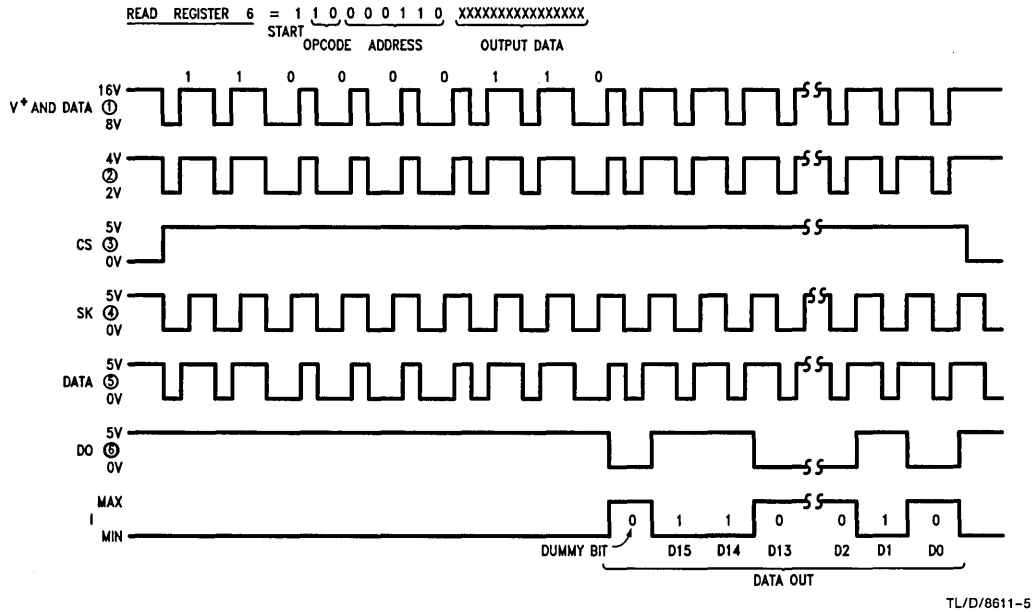
One-Shot B = ½ MM74HC123

V-R = LM2930Z-5.0

OA = LM358

R5 = 1600Ω

FIGURE 4



TL/D/8611-5

FIGURE 5

An Easy/Low Cost Serial EEPROM Interface

National Semiconductor
Application Note 431
Pat Webster

INTRODUCTION

Designers have resisted using a low cost serial EEPROM because of the uncommon interface required. The added components and circuitry have caused many engineers to resort to a larger parallel EEPROM, even when only a few bytes of non-volatile memory were required.

National Semiconductor has a design that is low in support components and takes advantage of a UART with a 1× external clock. This circuit is useful for DIP switch replacement as well as for a permanent record of the UART's communications activity. It can also be used as a security lock. Ease of interface offers the engineer a low cost solution.

THEORY OF OPERATION

Ordinarily small EEPROMs have been used to replace the DIP switch commonly found in microprocessor circuits. Just as common in such designs are UARTs, and the given application takes advantage of this for ease of interface. Because address decoding and microprocessor bus interfacing have already been accomplished, the UART is an ideal support interface for a serial EEPROM. The only true requirements for a serial EEPROM are the serial data path, clock timing, and chip select signal. All of these signals are derived from a UART in this application.

The Data In for the EEPROM is the transmitted data of the UART. Data Out of the EEPROM is directed to the receive data line of the UART. The chip select required by the EEPROM is a modem control line whose level is used to select either the modem device or the EEPROM. Finally, the serial clock required by the EEPROM can be a 1× clock provided by the UART.

THE WRITE CYCLE

When a write cycle is desired, the UART must be set up for an external 1× clock, 8 data bits, 1 stop bit, no parity and RTS must be programmed for a high output prior to data transmissions. It is also necessary to insure that the transmit buffer has been completely emptied of all prior bytes.

Before data can be written, an erase cycle to the desired address must first take place. This can be accomplished by loading the UART transmit register with an A0, A1, A2, A3, XX11 (e.g., an 03_H would result in location 0 being erased). After the transmit shift register has emptied, RTS should be returned to a low state and an erase/write programming time of 30 ms must elapse.

To write data requires that an address-op byte and two data bytes be loaded in the transmit holding register as soon as the holding register becomes empty. Table I shows the relationship of bits as they travel from the micro to the UART and finally to the EEPROM. The MSB 4 bits of the last byte written will not be saved by the EEPROM due to the 16-bit storage ability of the part. As the UART inserts start and stop bits, a total of 4 bits is saved in the EEPROM that are not usable by the microprocessor but are required by the UART.

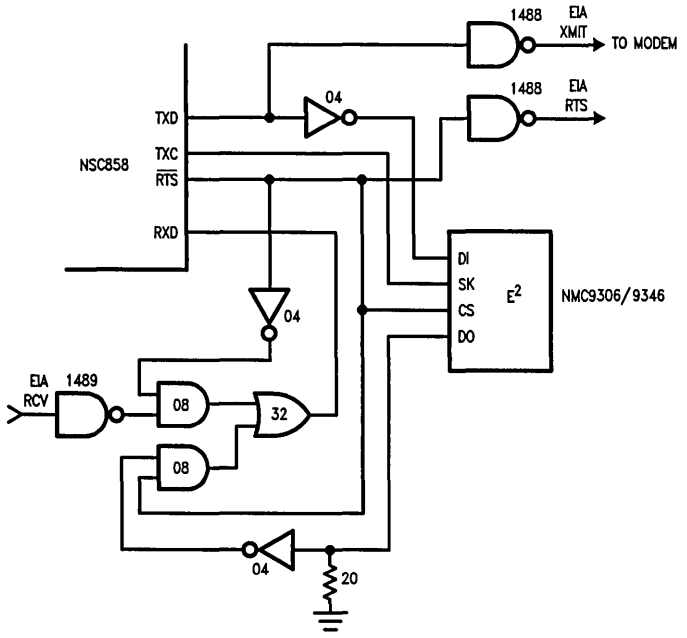
THE READ CYCLE

As was true for the write cycle, the UART must be set up for 8 data bits, 1 stop bit, and an external 1× clock. To start the read cycle, a byte with read op and address must be written to the UART. An example of read location 0 would be 01_H. After the transmit shift register has emptied, the receiver shift register will begin to accumulate the data that was written and two reads will be required before the operation can be considered complete.

CONCLUSION

For a further understanding of this interface, refer to the NMC9306/9346 and the NSC858 data sheets. Parity could be added for data integrity with further sacrifice of usable data bits in the EEPROM and the possibility of the second byte read being in parity error.

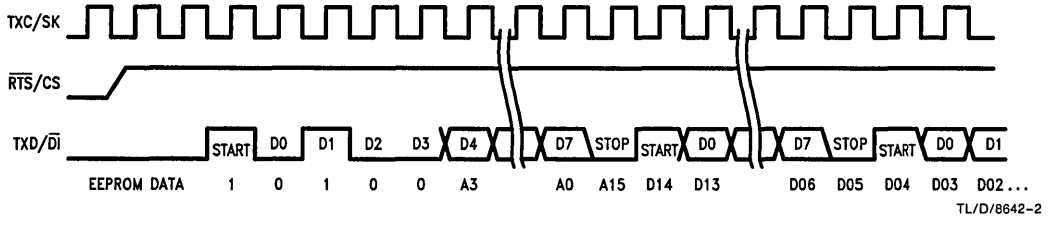
UART/EEPROM Interface



TL/D/8642-1

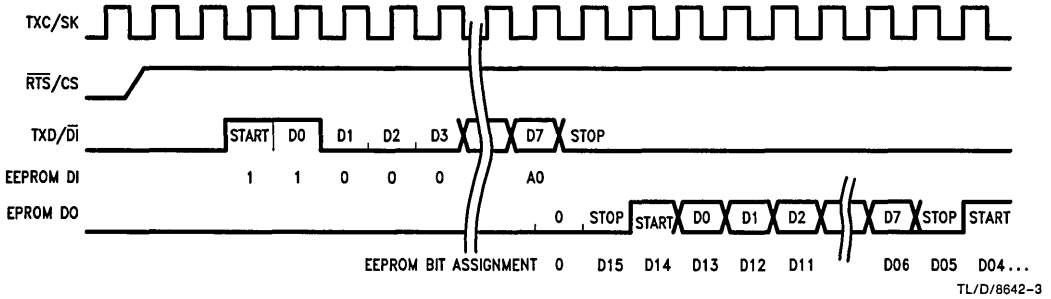
UART/EEPROM Timing

Write Cycle (9306)



TL/D/8642-2

Read Cycle



TL/D/8642-3

Table I

	Micro Data	UART XMIT Data		EEPROM
	—	Start-Bit		1
1st Byte	D0	0		0
	D1	1	Command	1
	D2	0	(Write)	0
	D3	0		0
	D4	A3		A3
	D5	A2		A2
	D6	A1		A1
	D7	A0		A0
	—	Stop-Bit		D15
	—	Start-Bit		D14
2nd Byte	D0	*ED0		D13
	D1	ED1		D12
	D2	ED2		D11
	D3	ED3		D10
	D4	ED4		D09
	D5	ED5		D08
	D6	ED6		D07
	D7	ED7		D06
	—	Stop-Bit		D05
	—	Start-Bit		D04
	D0	ED8		D03
	D1	ED9		D02
	D2	ED10		D01
	D3	ED11		D00
	D4	N/A		N/A
	D5	N/A		N/A
	D6	N/A		N/A
	D7	N/A		N/A
	—	Stop-Bit		N/A

*EDXX = Usable EEPROM Data

Using the NMC9306 for Configuration and Production Information in a TMP Based Terminal System

National Semiconductor
Application Note 433
Richard Zarr

ABSTRACT

This application note gives a detailed description of the use of the NMC9306 E²PROM in a TMP based environment. The function of the E²PROM is to contain all the configuration data for the terminal (i.e., baud rate, auto dial numbers, function selects, etc.) and also production information (i.e., serial number, date of manufacture, etc.)

INTRODUCTION

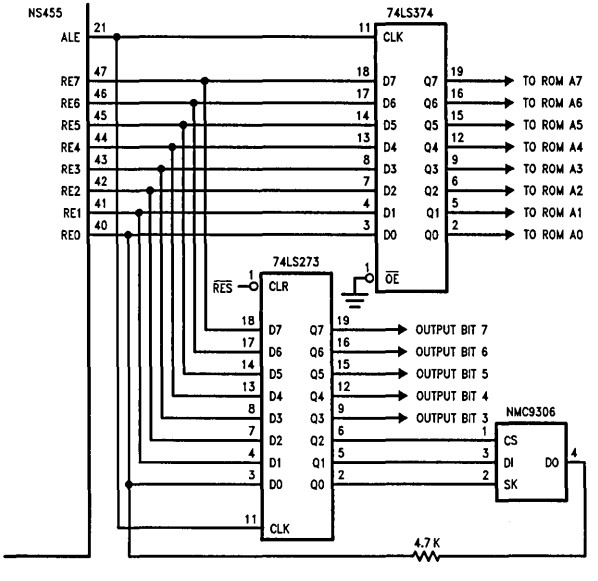
In a computer terminal environment, there are many user selectable options that need to be strapped into the terminal before it can be used. Some terminals have modems built into them that can automatically dial numbers for you. Some terminals can even emulate several different industry standard terminals, all in one. This configuration information is usually programmed into the terminal by using DIP switches accessed through some access cover or by removing a certain panel. A major drawback to this type of configuring is that the terminal must be opened by the user if they are to change the strapping. Another disadvantage is the terminal usually cannot be changed dynamically. Enter NON-VOLATILE RAM or battery-backed-up RAM. This creates another problem in that the system cost is increased, reliability suffers, and board space may not be available. Enter NMC9306 serial E²PROM in an 8-pin Mini-DIP. This device is not only non-volatile, but is small, inexpensive, and simple to use.

HARDWARE MAIN DESCRIPTION

Since the NS455 Terminal Management Processor (TMP) does not have a MICROWIRE™ interface, another method of interfacing must be devised. The TMP has provisions for an external output port attached to the ROM bus which can be used to simulate the MICROWIRE interface. This is done by using three free data bits of a 74LS273 as shown in *Figure 1.* These three bits will be the CHIP SELECT, CLOCK, and the DATA IN inputs to the NMC9306. The TMP also has an input port enable pin that can be used to read a set of buffers such as a 74LS244. A single pin can be used for the DATA OUT signal from the NMC9306 as shown in *Figure 2.* If no input port is required, the DATA OUT signal can be driven directly onto the ROM expansion bus through a 4.7k resistor as shown in *Figure 1.* This is all the hardware that is required to interface the part.

SOFTWARE MAIN DESCRIPTION

This is where things get a bit tricky. Routines must be written to communicate with the NMC9306. These routines must read, write, erase, and enable erase/write in the NMC9306 by simulating the MICROWIRE interface. This is done by turning the output ports pins on and off with the correct timing to simulate the interface without interfering with the other pins. Also, the input data must be converted to usable form as well as converting the outgoing data to serial form. Simple.



TL/D/8644–1

FIGURE 1

To start, there are a few things to be mentioned. The TMP has a modified 8048 processor for its controller. This controller has a 16-bit accumulator, addressed as two 8-bit registers, which are ACC and HACC. The high accumulator (HACC) is accessed through the low accumulator (ACC). This is important since the NMC9306 is arranged in 16 words of 16 bits each. Also, to allow the port to be modified without changing any unwanted bits, a PORT MASK must be defined in the memory of the TMP. Any change to the port should be done by updating the mask, and then sending the mask data to the port. This will also make testing the data on the port possible. The codes for communicating with the NMC9306 can be obtained from the *National Semiconductor 1984 MOS Memory Databook* in Section 7. Also, all critical timing parameters are described therein.

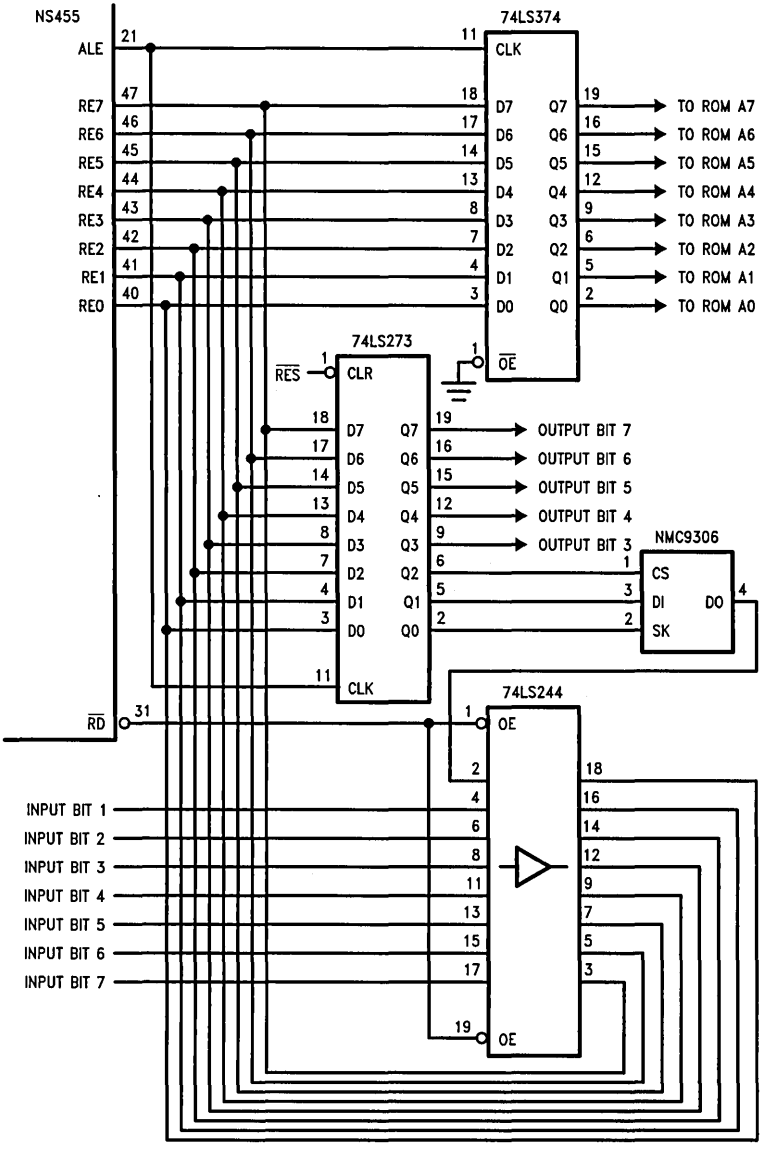
In a typical TMP system, there are large amounts of configuration data that must be set up before the terminal can communicate properly. If the system is really complex, it may need more yet. A typical configuration map is shown below. Along with the configuration data, production information should be included. This may be entered by some code at power-up that is not documented in the end user guide. This set-up screen may ask for the date of assembly, the assembly location code, the serial number, the customer code, the options enabled (tricky sales pitch— "for only $50 more . . . "), the number of times the unit was returned to the factory for service, and any other data that must be tracked for production. If the NMC9306 does not have enough room, the NMC9346 is 4 times larger, and has the same hardware requirements. Only slight software changes are required.

CONCLUSION

It can be seen that the NMC9306 is simple, yet functional in replacing strapping switches and enhancing the product. The NMC9306/NMC9346 components in this application, replace more costly and larger parts, and are easily integrated into a TMP or other terminal design. The end product will be more versatile through enhanced user interface and tracking of important production data.

Typical Configuration Map

Location (Hex)		Description
0	Bit 0	Cursor Blink Enable
	Bit 1	Cursor Underline/Block
	Bit 2	Cursor Inverts Video On
	Bit 3	Screen Norm/Inverse Vid
	Bit 4	Local Mode On/Off
	Bit 5	Status Line Enable
	Bits 6–F	(Spare)
1	Bits 0–3	Baud Rate
	Bit 4	1 or 2 Stop Bits
	Bit 5	7 or 8 Data Bits
	Bit 6	Parity On/Off
	Bit 7	Odd or Even Parity
	Bits 8–F	(Spare)
2	Bits 0–F	(Spare)
3	Bits 0–F	Month and Year of Assem.
4	Bits 0–7	Day of Assembly
	Bits 8–F	Assembly Location
5	Bits 0–7	Inspector Code
	Bits 8–F	No. of Returns
6	Bits 0–F	Serial Number (MSW)
7	Bits 0–F	Serial Number
8	Bits 0–F	Serial Number (LSW)
9	Bits 0–7	Failure Code 1
	Bits 8–F	Failure Code 2
A	Bits 0–F	Check Sum
B–F		(Spare)



TL/D/8644-2

FIGURE 2

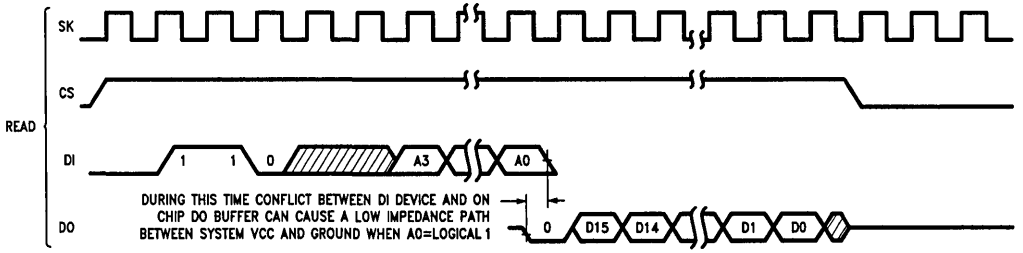
Common I/O Applications of NMC9306/COP494 and NMC9346/COP495 Non-Volatile Serial Access Memories

National Semiconductor
Application Note 481

NMC9306/COP494 and NMC9346/COP495 are serial access non-volatile memories designed for a 4-wire (MICROWIRE™) interface; Chip Select (CS) input, clock (SK) input, serial data input (DI), and serial data output (DO). Since DO is in TRI-STATE® while instructions, address and data are being shifted into the chip on the DI signal line, DI and DO can be tied together as a common I/O to further simplify the interface. However, the following potentially troublesome situations should be kept in mind and dealt with according to these recommendations:

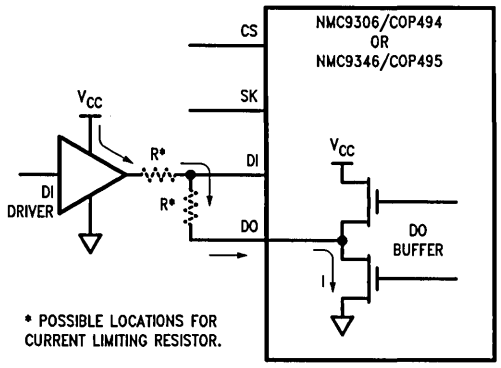
NMC9306/COP494

While clocking in a READ instruction, approximately 500 ns (typical) after the least significant bit (A0) of the register address is clocked into the chip by the rising edge of SK, DO comes out of TRI-STATE and goes low (logical '0') as a dummy bit to signal the start of the data output string *(Figure 1).* In a common I/O application, if A0 is a logical '1' and is still driving DI when the dummy bit becomes valid, a low impedance path between the power supply and ground is created through the DI driver and the on-chip DO buffer *(Figure 2).* If measures are taken to minimize the short circuit current, e.g., by inserting a current limiting resistor between the DI driver and the chip *(Figure 2),* the part will continue to work normally since A0 is clocked onto the chip before this potential disturb condition occurs.



TL/D/9213–1

FIGURE 1. Read Instruction in Common I/O Configuration



TL/D/9213–2

FIGURE 2. Current Path during DI Driver and DO Buffer Conflict during Read Instruction

NMC9346/COP495

The NMC9346/COP495 has a self-timed programming cycle which uses DO to indicate the ready/busy status of the chip. Therefore, in addition to the potential problem in the READ mode similar to NMC9306/COP494 described above, another pitfall may be encountered at the end of a programming cycle in common I/O applications.

The self-timed programming cycle is initiated by the falling edge of CS after a programming instruction (ERASE,

WRITE, ERAL, WRAL) is shifted in. If CS is brought high subsequently, after a minimum of 1 μs (tcs), DO indicates the ready/busy status of the chip. DO = logical '0' indicates that programming is still in progress. DO = logical '1' signals the end of the programming cycle. This 'status check' function of DO is cancelled (i.e., DO returns to TRI-STATE) when a logical '1' on DI is clocked into the chip by SK with CS high. With separate input and output this is automatically accomplished by the start bit of the next instruction *(Figure 3)*.

In a common I/O application, the following clocking sequence is recommended to avoid premature cancellation of the 'ready' status and/or interference of the 'ready' status with the serial input sequence for the next instruction *(Figure 4)*:

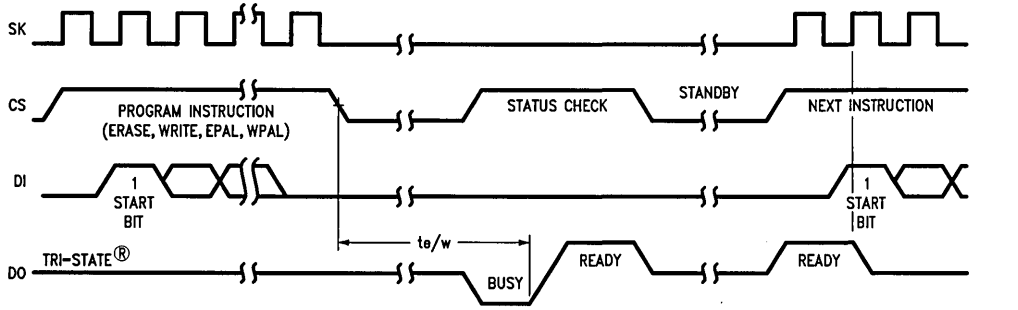
1) Inhibit the SK clock after clocking in the programming instruction.
2) After acknowledging the 'ready' status, clock SK once while the common I/O is still high to cancel the ready/busy status function of DO.
3) Bring CS low for a minimum of 1 μs (tcs) to clear the instruction register before initiating the next instruction.

DO is now reset back to TRI-STATE, and the chip is ready to accept the next instruction.

The chip may enter the 'ready' status mode under certain conditions of V_{CC} power-up. This occurs due to the V_{CC} power-up conditions setting the status mode logic on the chip, and is not an indication of a spurious programming cycle on V_{CC} power-up. The following clocking sequence is recommended to ensure cancellation of this status signal after V_{CC} power-up *(Figure 5)*:

1) Bring CS high.
2) Clock SK once to ensure cancellation of the 'ready' status.
3) Bring CS low for a minimum of 1 μs (tcs) to clear the instruction register before initiating the first instruction.

NMC9346 Timing Diagrams

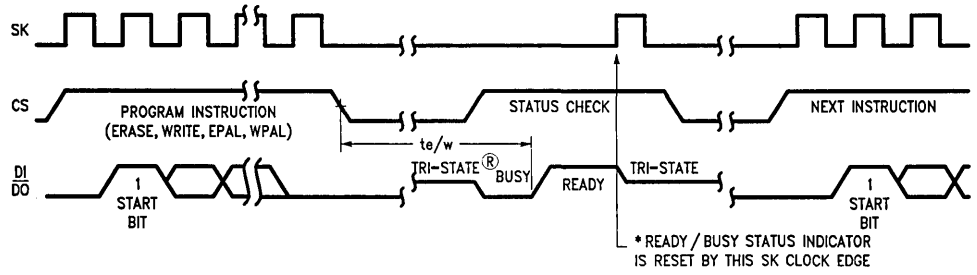


TL/D/9213–3

*The Ready/Busy Status Indicator for a program Instruction (ERASE, WRITE, ERAL, WRAL) is reset when the Start bit for the following Instruction is clocked in.

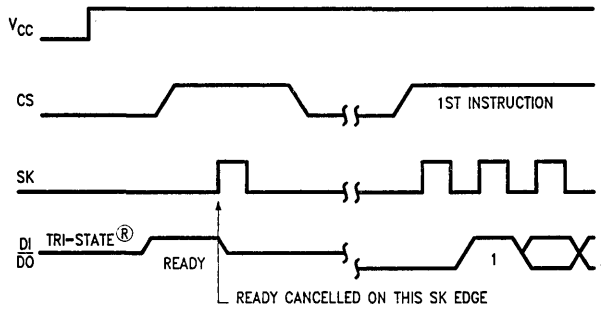
FIGURE 3. Programming Cycle with 4-Wire Interface

NMC9346 Timing Diagrams (Continued)



TL/D/9213-4

FIGURE 4. Recommended Programming Cycle in Common I/O Configuration



TL/D/9213-5

FIGURE 5. Recommended Clocking Sequence on V_{CC} Power-Up in Common I/O Configuration

Error Detection and Correction Techniques for National Semiconductor's EEPROM Products

National Semiconductor
Application Note 482

This application note provides the non-volatile memory system designer who cannot tolerate the very low failure rate associated with National Semiconductor's E²PROMs, with a method to assure data integrity and extend the life span of the product.

With a minimum additional parts cost, the following error detection and correction techniques allow the designer to extend the usable life of an EEPROM device. The technique is applicable for applications requiring 100,000 or more erase/write cycles per register.

All EEPROMs fail with extended erase/write cycling. National Semiconductor EEPROMs fail in a statistically predictable and well behaved fashion as the number of erase/write cycles increase. The failure of one bit cell does not influence the operation of adjacent bit cells. Since bit failure is a gradual wearout phenomenon which only affects discrete cell locations one at a time, it is possible to apply simple encoding techniques which can determine the locations of cell failures so that faltering memory addresses can be avoided in the future.

Single parity checking is the simplest way to check for errors in a binary code. In a parity checking system an extra-parity-bit is chosen so that the number of 1s in the block of data, including the parity bit, is even. In practice this is accomplished using modulo 2 addition (i.e., 0 + 0 = 0; 0 + 1 = 1; 1 + 0 = 1; 1 + 1 = 0; 0 + 0 + 1 = 1; etc.). Modulo 2 addition is quickly accomplished through an exclusive OR gate. When the data is read back, the number of ones are counted and the sum is checked to see if it is odd or even. An odd sum is an indication that an error occurred in the data. This method of single parity checking can detect the occurrence of an error in a block but it cannot be used to determine the exact location of the error to correct the bad data.

A natural extension of single parity checking is the Hamming code. A Hamming code uses several parity checks, instead of just one. This allows errors to be corrected as well as detected. Using bits in blocks of 7, where 4 of the bits are information and 3 are parity allows for error detection and correction of any single bit within the block, including the parity bits themselves.

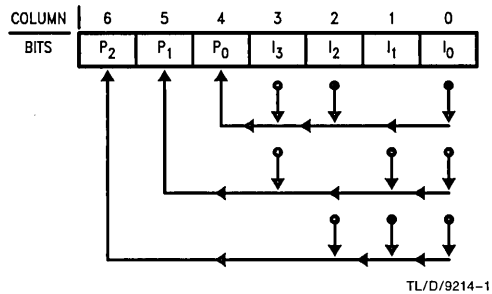


FIGURE 1. Computation Scheme for Parity Bits Using Hamming Code

The initial parity is calculated as shown in *Figure 1*. The parity bits are in columns 4, 5 and 6, while the actual information bits are in columns 0, 1, 2, and 3. The contents of each parity bit comes from summing the contents of a unique combination of three of the four information bits. The parity bit is chosen so that this sum will be an even number when added to the parity bit itself. Notice that each one of the parity bits calculates its contents by using different combinations of the data bits. Every data bit in the block has its information read at least twice. Using this overlapping scheme is what allows the code to correct errors.

Since there are only 4 bits of information there can be only $2^4 = 16$ possible combinations of 1s and 0s. These 16 possible correct combinations are listed on the code word table in Table I. When the encoded block is read back from memory, the same parity coding scheme is used again on the information bits and compared to the original parity bits. This forms what is called a syndrome. If any errors have occurred in the 7-bit block their locations can be determined and the errors corrected. Table II shows the decoding matrix which is used on the syndromes to determine the location of an error. If no errors occurred the syndrome will be 000. Table III shows all the combinations of the 7-bit block. Note that there are only 128 possible variations of 1s and 0s in the block: (7 mistake combinations per block + 1 correct combination per block) × (16 possible block combinations). All these combinations can be stored in a table and called up quickly to check for possible data errors without the need to even create a syndrome upon reading a word. For example, suppose we want to store the data 1000. From Table I we see that the 7-bit block would be 1111000 after the Hamming code had been applied. If information bit 3 for example goes bad, then the new block would read 1110000. This is case number 112 in Table III, and we see that the correct information is 1000. With Table III available in the computer memory, the received codeword can be corrected automatically. An array of 128 bytes can provide both the corrected information and the syndrome information.

The 7-bit codeword works nicely with National Semiconductor's serial EEPROMs because they are organized as arrays of 16-bit registers. Each 16 bit register is modified or accessed with a simple-serial protocol. The 16-bit unit can be partitioned two eight-bit bytes. Each byte can contain a seven-bit codeword and one-bit flag that indicates whether an error has been previously detected in the byte. This scheme provides one byte of error corrected information per 16-bit register. Slightly more elaborate systems can be used which will detect and correct more errors if additional parity bits are added to the data.

TABLE I. Encoding Table for Hamming Code

	Sixteen Code Words						
	Parity Bits			Information Bits			
	P 2	P 1	P 0	I 3	I 2	I 1	I 0
0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	1
2	1	0	1	0	0	1	0
3	0	1	1	0	0	1	1
4	0	1	1	0	1	0	0
5	1	0	1	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	0	1	1	1
8	1	1	1	1	0	0	0
9	0	0	1	1	0	0	1
10	0	1	0	1	0	1	0
11	1	0	0	1	0	1	1
12	1	0	0	1	1	0	0
13	0	1	0	1	1	0	1
14	0	0	1	1	1	1	0
15	1	1	1	1	1	1	1

TABLE II. Syndrome Decoding Table for Hamming Code

Syndrome			Meaning
0	0	0	No error detected
0	0	1	Check bit 0 in error
0	1	0	Check bit 1 in error
0	1	1	Information bit 2 corrected
1	0	0	Check bit 2 in error
1	0	1	Information bit 1 corrected
1	1	0	Information bit 0 corrected
1	1	1	Information bit 3 corrected

With this added data protection the reliability of EEPROMs can be extended because the probability of two or more cells failing on the same codeword is low. To illustrate the Hamming code, an experiment on 16 devices with 1k bits each was conducted. The experiment results are shown in Table IV. While the first bit failure was detected somewhere between 12,589 and 15,849 cycles, the Hamming code just described would have protected against the loss of data until somewhere between 79,433 and 100,000 erase/write cycles. Notice that 55 bit failures were indicated when the first Hamming code failure was detected. This is to be expected because a Hamming failure will not occur until two or more bits within a particular group of seven bits have failed.

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code

	Received Codeword							Syndrome Bits			Corrected Information			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	0	0	0	0	0
2	0	0	0	0	0	1	0	1	0	1	0	0	0	0
3	0	0	0	0	0	1	1	0	1	1	0	1	1	1
4	0	0	0	0	1	0	0	0	1	1	0	0	0	0
5	0	0	0	0	1	0	1	1	0	1	0	1	1	1
6	0	0	0	0	1	1	0	1	1	0	0	1	1	1
7	0	0	0	0	1	1	1	0	0	0	0	1	1	1
8	0	0	0	1	0	0	0	1	1	1	0	0	0	0
9	0	0	0	1	0	0	1	0	0	1	1	0	0	1
10	0	0	0	1	0	1	0	0	1	0	1	0	1	0
11	0	0	0	1	0	1	1	1	0	0	1	0	1	1
12	0	0	0	1	1	0	0	1	0	0	1	1	0	0
13	0	0	0	1	1	0	1	0	1	0	1	1	0	1
14	0	0	0	1	1	1	0	0	0	1	1	1	1	0
15	0	0	0	1	1	1	1	1	1	1	0	1	1	1
16	0	0	1	0	0	0	0	0	0	1	0	0	0	0
17	0	0	1	0	0	0	1	1	1	1	1	0	0	1
18	0	0	1	0	0	1	0	1	0	0	0	0	1	0
19	0	0	1	0	0	1	1	0	1	0	0	0	1	1
20	0	0	1	0	1	0	0	0	1	0	0	1	0	0
21	0	0	1	0	1	0	1	1	0	0	0	1	0	1
22	0	0	1	0	1	1	0	1	1	1	1	1	1	0
23	0	0	1	0	1	1	1	0	0	1	0	1	1	1
24	0	0	1	1	0	0	0	1	1	0	1	0	0	1
25	0	0	1	1	0	0	1	0	0	0	1	0	0	1
26	0	0	1	1	0	1	0	0	1	1	1	1	1	0
27	0	0	1	1	0	1	1	1	0	1	1	0	0	1
28	0	0	1	1	1	0	0	1	0	1	1	1	1	0
29	0	0	1	1	1	0	1	0	1	1	1	0	0	1
30	0	0	1	1	1	1	0	0	0	0	1	1	1	0
31	0	0	1	1	1	1	1	1	1	0	1	1	1	0

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
32	0	1	0	0	0	0	0	0	1	0	0	0	0	0
33	0	1	0	0	0	0	1	1	0	0	0	0	0	1
34	0	1	0	0	0	1	0	1	1	1	1	0	1	0
35	0	1	0	0	0	1	1	0	0	1	0	0	1	1
36	0	1	0	0	1	0	0	0	0	1	0	1	0	0
37	0	1	0	0	1	0	1	1	1	1	1	1	0	1
38	0	1	0	0	1	1	0	1	0	0	0	1	1	0
39	0	1	0	0	1	1	1	0	1	0	0	1	1	1
40	0	1	0	1	0	0	0	1	0	1	1	0	1	0
41	0	1	0	1	0	0	1	0	1	1	1	1	0	1
42	0	1	0	1	0	1	0	0	0	0	1	0	1	0
43	0	1	0	1	0	1	1	1	1	0	1	0	1	0
44	0	1	0	1	1	0	0	1	1	0	1	1	0	1
45	0	1	0	1	1	0	1	0	0	0	1	1	0	1
46	0	1	0	1	1	1	0	0	1	1	1	0	1	0
47	0	1	0	1	1	1	1	1	0	1	1	1	0	1
48	0	1	1	0	0	0	0	0	1	1	0	1	0	0
49	0	1	1	0	0	0	1	1	0	1	0	0	1	1
50	0	1	1	0	0	1	0	1	1	0	0	0	1	1
51	0	1	1	0	0	1	1	0	0	0	0	0	1	1
52	0	1	1	0	1	0	0	0	0	0	0	1	0	0
53	0	1	1	0	1	0	1	1	1	0	0	1	0	0
54	0	1	1	0	1	1	0	1	0	1	0	1	0	0
55	0	1	1	0	1	1	1	0	1	1	0	0	1	1
56	0	1	1	1	0	0	0	1	0	0	1	0	0	0
57	0	1	1	1	0	0	1	0	1	0	1	0	0	1
58	0	1	1	1	0	1	0	0	0	1	1	0	1	0
59	0	1	1	1	0	1	1	1	1	1	0	0	1	1
60	0	1	1	1	1	0	0	1	1	1	0	1	0	0
61	0	1	1	1	1	0	1	0	0	1	1	1	0	1
62	0	1	1	1	1	1	0	0	1	0	1	1	1	0
63	0	1	1	1	1	1	1	1	0	0	1	1	1	1
64	1	0	0	0	0	0	0	1	0	0	0	0	0	0
65	1	0	0	0	0	0	1	0	1	0	0	0	0	1
66	1	0	0	0	0	1	0	0	0	1	0	0	1	0
67	1	0	0	0	0	1	1	1	1	1	1	0	1	1
68	1	0	0	0	1	0	0	1	1	1	1	1	0	0
69	1	0	0	0	1	0	1	0	0	1	0	1	0	1
70	1	0	0	0	1	1	0	0	1	0	0	1	1	0
71	1	0	0	0	1	1	1	1	0	0	0	1	1	1
72	1	0	0	1	0	0	0	0	1	1	1	1	0	0
73	1	0	0	1	0	0	1	1	0	1	1	0	1	1
74	1	0	0	1	0	1	0	1	1	0	1	0	1	1
75	1	0	0	1	0	1	1	0	0	0	1	0	1	1
76	1	0	0	1	1	0	0	0	0	0	1	1	0	0
77	1	0	0	1	1	0	1	1	1	0	1	1	0	0
78	1	0	0	1	1	1	0	1	0	1	1	1	0	0
79	1	0	0	1	1	1	1	0	1	1	1	0	1	1

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
80	1	0	1	0	0	0	0	1	0	1	0	0	1	0
81	1	0	1	0	0	0	1	0	1	1	0	1	0	1
82	1	0	1	0	0	1	0	0	0	0	0	0	1	0
83	1	0	1	0	0	1	1	1	1	0	0	0	1	0
84	1	0	1	0	1	0	0	1	1	0	0	1	0	1
85	1	0	1	0	1	0	1	0	0	0	0	1	0	1
86	1	0	1	0	1	1	0	0	1	1	0	0	1	0
87	1	0	1	0	1	1	1	1	0	1	0	1	0	1
88	1	0	1	1	0	0	0	0	1	0	1	0	0	0
89	1	0	1	1	0	0	1	1	0	0	1	0	0	1
90	1	0	1	1	0	1	0	1	1	1	0	0	1	0
91	1	0	1	1	0	1	1	0	0	1	1	0	1	1
92	1	0	1	1	1	0	0	0	0	1	1	1	0	0
93	1	0	1	1	1	0	1	1	1	1	0	1	0	1
94	1	0	1	1	1	1	0	1	0	0	1	1	1	0
95	1	0	1	1	1	1	1	0	1	0	1	1	1	1
96	1	1	0	0	0	0	0	1	1	0	0	0	0	1
97	1	1	0	0	0	0	1	0	0	0	0	0	0	1
98	1	1	0	0	0	1	0	0	1	1	0	1	1	0
99	1	1	0	0	0	1	1	1	0	1	0	0	0	1
100	1	1	0	0	1	0	0	1	0	1	0	1	1	0
101	1	1	0	0	1	0	1	0	1	1	0	0	0	1
102	1	1	0	0	1	1	0	0	0	0	0	1	1	0
103	1	1	0	0	1	1	1	1	1	0	0	1	1	0
104	1	1	0	1	0	0	0	0	0	1	1	0	0	0
105	1	1	0	1	0	0	1	1	1	1	0	0	0	1
106	1	1	0	1	0	1	0	1	0	0	1	0	1	0
107	1	1	0	1	0	1	1	0	1	0	1	0	1	1
108	1	1	0	1	1	0	0	0	1	0	1	1	0	0
109	1	1	0	1	1	0	1	1	0	0	1	1	0	1
110	1	1	0	1	1	1	0	1	1	1	0	1	1	0
111	1	1	0	1	1	1	1	0	0	1	1	1	1	1
112	1	1	1	0	0	0	0	1	1	1	1	0	0	0
113	1	1	1	0	0	0	1	0	0	1	0	0	0	1
114	1	1	1	0	0	1	0	0	1	0	0	0	1	0
115	1	1	1	0	0	1	1	1	0	0	0	0	1	1
116	1	1	1	0	1	0	0	1	0	0	0	1	0	0
117	1	1	1	0	1	0	1	0	1	0	0	1	0	1
118	1	1	1	0	1	1	0	0	0	1	0	1	1	0
119	1	1	1	0	1	1	1	1	1	1	1	1	1	1
120	1	1	1	1	0	0	0	0	0	0	1	0	0	0
121	1	1	1	1	0	0	1	1	1	0	1	0	0	0
122	1	1	1	1	0	1	0	1	0	1	1	0	0	0
123	1	1	1	1	0	1	1	0	1	1	1	1	1	1
124	1	1	1	1	1	0	0	0	1	1	1	0	0	0
125	1	1	1	1	1	0	1	1	0	1	1	1	1	1
126	1	1	1	1	1	1	0	1	1	0	1	1	1	1
127	1	1	1	1	1	1	1	0	0	0	1	1	1	1

TABLE IV. Hamming Code Experimental Demonstration on 16 Devices of 1k Bits Each

Erase/Write Cycles	Total Bit Failures	Total Codeword Failures	Percent Bit Failures	Percent Codeword Failures
1000	0	0	0.00%	0.00%
1259	0	0	0.00%	0.00%
1585	0	0	0.00%	0.00%
1995	0	0	0.00%	0.00%
2512	0	0	0.00%	0.00%
3162	0	0	0.00%	0.00%
3981	0	0	0.00%	0.00%
5012	0	0	0.00%	0.00%
6310	0	0	0.00%	0.00%
7943	0	0	0.00%	0.00%
10000	0	0	0.00%	0.00%
12589	1	0	0.01%	0.00%
15849	1	0	0.01%	0.00%
19953	1	0	0.01%	0.00%
25119	1	0	0.01%	0.00%
31623	3	0	0.02%	0.00%
39811	4	0	0.02%	0.00%
50119	10	0	0.06%	0.00%
63096	16	0	0.10%	0.00%
79433	55	1	0.34%	0.05%
100000	103	3	0.63%	0.15%

Using the NMC98Cxx Family

National Semiconductor
Application Note 506

INTRODUCTION

This application note is intended for system designers interested in using the NMC98Cxx family of byte-wide, CMOS EEPROM devices. The family is distinguished by its multiplexed address/data bus interface. The multiplexed interface makes the devices ideal for applications with a multiplexed system bus that require physically small, fast access, non-volatile, writeable memory.

EEPROMs are useful in a wide variety of applications because of their non-volatile, writeable characteristic. The devices can be used for applications that store configuration values, such as feature telephones, station presets on radios, and PC boards with configuration DIP switches and jumpers. Adaptive, closed-loop systems, such as environment controllers and motor controllers, can use EEPROMs to store loop control variables. Data logging is another of the many application areas of EEPROMs.

The primary application for NMC98Cxx family devices is in microcontroller-based systems. Most microcontrollers have a multiplexed bus, allowing the devices to be designed in with little or no support logic. Device operation is fast because access is byte-wide using standard read/write instructions. The devices are also applicable in systems with address space limitations and non-multiplexed bus systems by using a technique that maps the device to require only two locations: one for the address to be accessed and one for data.

TABLE I. NMC98Cxx Family

Device	Memory Size
NMC98C10	128 x 8
NMC98C20	256 x 8
NMC98C40	512 x 8

The NMC98Cxx devices have low power consumption due to the low drive requirements of their multiplexed bus interface and the use of CMOS technology. The multiplexed interface allows the device to fit in a smaller package and removes the need for an off-chip address latch, resulting in minimal board space requirements.

NMC98Cxx FAMILY DESCRIPTION

The NMC98Cxx family is a set of three byte-wide, CMOS EEPROM devices with a multiplexed bus interface The members of the family are differentiated by their memory array size, which are 128, 256 and 512 bytes (see Table I).

All three members of the family are packaged in an 18-pin DIP. The only difference in pinout of the devices is the number of address lines present to support the differing memory array sizes.

The devices are identical in all other respects (see *Figure 1*).

Because of the multiplexed bus interface, device read/write operations are a two-step process. The first step is to load the address of the location to be accessed. This is accomplished by raising ALE high to enable the on-chip address latch to be loaded, sending the appropriate address to the device, lowering ALE to save the address, and removing the multiplexed address signals from the bus. The signals stored in the latch are A8–0, $\overline{CE1}$ and CE2. By latching $\overline{CE1}$ low and CE2 high, the device will enter a powered up mode of operation, ready to perform the second step, a read or write of the selected location. There is no limit to the time a device may wait before performing the read or write portion of the operation, though the device will remain powered up.

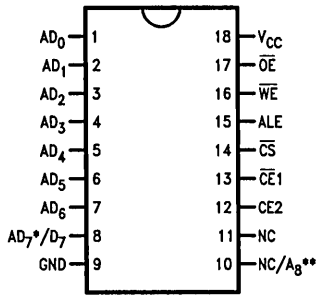
The device should be inhibited from reading or writing, by setting both $\overline{OE}$ and $\overline{WE}$ high, while loading the address latch (see Table II). In general, $\overline{OE}$ and $\overline{WE}$ should be high to inhibit read and write operations and they should never change at the same time. It isn't recommended to inhibit operations by setting $\overline{OE}$ and $\overline{WE}$ both low because of the non-standard, difficult timing required for correct device operation.

TABLE II. NMC98Cxx Modes

Mode	$\overline{CE1}$	CE2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

V_{IL} = Logical Low Input
V_{IH} = Logical High Input
Hi-Z = High Impedance State
X = Don't Care

Pin Name	Function
AD_0–AD_7	Multiplexed address and data bits. AD_7 is DATA only for NMC98C10.
GND	Ground, 0V
A8	MSB of address for NMC98C40, NC for NMC98C10/20
NC	No connection. No internal connection is made to this pin and it may be left floating.
CE2	Chip Enable 2 (See Table II)
$\overline{CE1}$	Chip Enable 1 (See Table II)
$\overline{CS}$	Chip Select (See Table II)
ALE	Address Latch Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Positive Power Supply, 5V



TL/D/9416–1

**NMC98C40
*NMC98C20/40

FIGURE 1. NMC98Cxx Pin Definition and Connection Diagram

A read of a selected location is performed by pulsing $\overline{OE}$ low while $\overline{CS}$ is low and $\overline{WE}$ is high. The device's multiplexed bus data outputs will become active and valid data will appear after $\overline{OE}$ goes low. The outputs will return to an inactive, high-Z condition after $\overline{OE}$ returns high.

A write of a selected location is performed by lowering $\overline{WE}$ while $\overline{CS}$ is low and $\overline{OE}$ is high, driving data onto the multiplexed bus of the device, raising $\overline{WE}$ high to latch the data into the device and initiate the automatic internal write cycle, and then removing the data from the bus. The internal write cycle includes an auto-erase function. AD7 may be read to check from completion of the write cycle. AD7 will be the logical inverse of the data written until completion of the cycle.

The $\overline{CS}$, $\overline{CE1}$ and CE2 signals may be tied active. If $\overline{CE1}$ and CE2 are tied active, the device will be permanently powered up. In addition, write operations are inhibited during system supply power-up, power-down or brown-out.

INTERFACING TO THE NMC98Cxx FAMILY

The NMC98Cxx family was designed to interface easily into microcontroller and microprocessor systems with a multiplexed address/data bus. The interface requires little or no support logic. The external address latch usually required in multiplexed bus systems is on-chip. Address decode is the only function that may require additional logic.

The same approach is used to interface the NMC98Cxx family into different multiplexed bus systems. Most multiplexed bus interfaces are the same. They typically provide ALE, $\overline{RD}$ and $\overline{WR}$ as control signals, multiplexed address/data and upper address. The primary application for these devices is in microcontroller systems. The National HPC and COP family, 8051, and 8096 microcontrollers all provide the same interface. The only difference is the bus size. The NMC98Cxx devices interface to any bus size because the upper address is latched on-chip in addition to the lower multiplexed addresses. The major issue in the interface is how the device is mapped into the address space. Other devices in the system and the size of the address space represent the constraints that must be dealt with . The approach used to interface the devices into an address space limited or non-multiplexed system is also easy and consistent.

HPC 8-BIT INTERFACE

The National HPC family is a set of high performance 16-bit microcontrollers. The HPC family devices, such as the HPC16040, can be used to provide an excellent example of how to interface to the NMC98Cxx family. The HPC family can be configured to provide several different interfaces.

An HPC device can be configured in four operating modes: Single-Chip, Expanded, Single-Chip ROMless, and Expanded ROMless. The Single-Chip mode has 4 kbytes of ad-

dress space and a 4 kbyte internal ROM and performs no external memory operations. The other modes all perform external operations and can be configured to use an 8-bit or 16-bit external bus. Expanded mode uses the 4k internal ROM, but the address space is expanded to 64k. Single-Chip ROMless has a 4k address space and Expanded ROMless has 64k. Neither mode uses the internal ROM. Program memory is stored external to the microcontroller.

The simplest configuration to interface is an HPC device in Expanded mode with an 8-bit external bus connecting to a single NMC98Cxx device. The external memory interface control signals of an HPC device consist of ALE, $\overline{RD}$, $\overline{WR}$, and High Byte Enable ($\overline{HBE}$). $\overline{HBE}$ is used to enable the upper byte of external memory when an HPC is configured with a 16-bit bus. $\overline{HBE}$ isn't used in this interface. In this interface ALE of the HPC is directly connected to ALE of the NMC98Cxx device, $\overline{RD}$ to $\overline{OE}$, and $\overline{WR}$ to $\overline{WE}$. The upper address and multiplexed bus are also directly connected. Since the internal program ROM resides in the upper 4k of the address space, the EEPROM must be placed elsewhere. Connecting A15 to $\overline{CE1}$ places the device in the lower half of the address space. Using $\overline{CE1}$ allows the device to power down when not being accessed. $\overline{CS}$ and CE2 are tied active (see *Figure 2a*).

Should other devices need to be placed in the address space with the NMC98Cxx device, $\overline{CS}$, CE2 and unused upper addresses can be used for device selection. Most device chip selects are active low. Since CE2 is active high, the same address signal can be used to select an NMC98Cxx device and another device. The address is connected to CE2 on the NMC98Cxx device and the chip select on the other device. The EEPROM will be selected when the address is high and the other device will be selected when the address is low (see *Figure 2b*).

Unused upper addresses can also be used for device selection. Each different address signal could be used as a chip select for a different device. Only one device may be selected at a time. Assuming all chip selects are active low, only one of these addresses may be low at a time to prevent contention. The HPC software would have to guarantee this. If these techniques for device selection aren't sufficient, addition of a decoder device or PAL® device should provide more than sufficient decode capability.

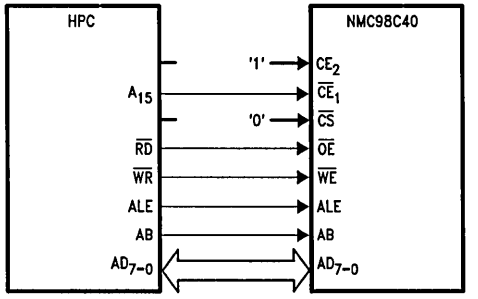


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FIGURE 2a. Simple 8-Bit Interface

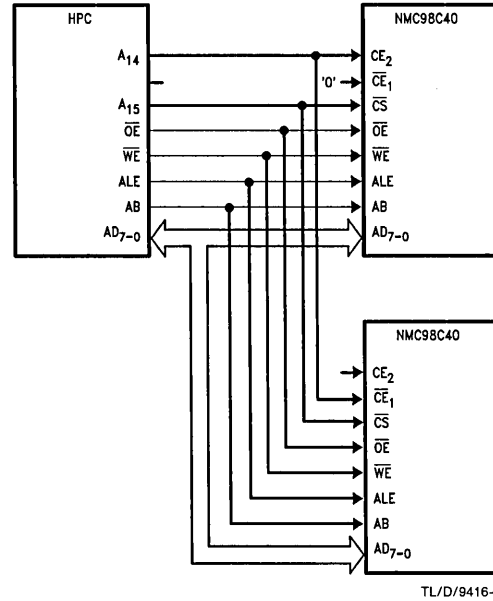

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FIGURE 2b. Multi-Chip Interface

Using only $\overline{CS}$ for device selection allows for a faster memory cycle. $\overline{CS}$ must be low preceeding $\overline{RD}$ or $\overline{WR}$ for proper operation. $\overline{CE1}$ and CE2 must be set before the falling edge of ALE, which happens earlier in a memory cycle. The EEPROM will remain powered up when not being used if $\overline{CE1}$ and CE2 are tied active. By using a port bit to control $\overline{CE1}$ or CE2 the device could be powered up for fast operations then powered down when done.

HPC 16-BIT INTERFACE

If an HPC device is configured with a 16-bit external bus, the interface of a single NMC98Cxx device is nearly the same as for an 8-bit bus. All addresses are now multiplexed. Device access is performed using byte operations. Word operations and program execution can't be performed using the EEPROM because the HPC attempts to access two locations at the same time in parallel. NMC98Cx0 devices don't easily interface in parallel.

In a simple interface, $\overline{CE1}$ or CE2 should be used for device selection because the addresses used for device selection are now multiplexed and remain valid for only part of the memory cycle. $\overline{CS}$ should be tied low. Otherwise, the interface is the same (see *Figure 3*).

NMC98Cxx devices are difficult to connect in parallel because only the addresses are connected in parallel, the data isn't. The low byte of data is connected to the low order EEPROM and the high byte to the high EEPROM. Address and data must be connected together on NMC98Cxx devices because address and data share the same pins. In addition, A0 and $\overline{HBE}$ are used to decode the low and high byte. On NMC98Cxx devices A0 is used to select internal memory array locations.

ADDRESS SPACE LIMITED/ NON-MULTIPLEXED INTERFACE

The multiplexed bus interface of the NMC98Cxx family of devices makes them applicable when system address space is limited and in non-multiplexed bus systems. A device can be selected using as few as two locations. One location is used to store the address of the data to be accessed in the EEPROM device and the other is used for the data accessed.

The primary application for this interface is when the system address space is limited. Most microcontrollers and some microprocessors are limited to an address space of 64 kbytes. An HPC device configured in Single-Chip ROMless mode has only 4 kbytes of address space available for program memory and other devices. An NMC98C40 has 512 bytes of EEPROM. The system may not have the 512 locations to spare that are required for a standard interface. An 8051 using register indirect instructions for external access has an address space of only 256 bytes. Another application for this interface is when the NMC98Cxx device needs to be in the I/O address space of a system. Typically, an I/O address space is intended for ports and is quite limited. For example, in the IBM® PC the I/O address space is 1 kbytes and only 32 of these locations are allocated for prototype or general use.

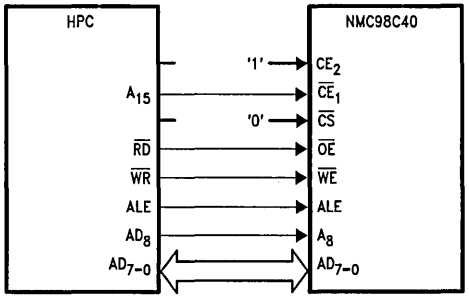

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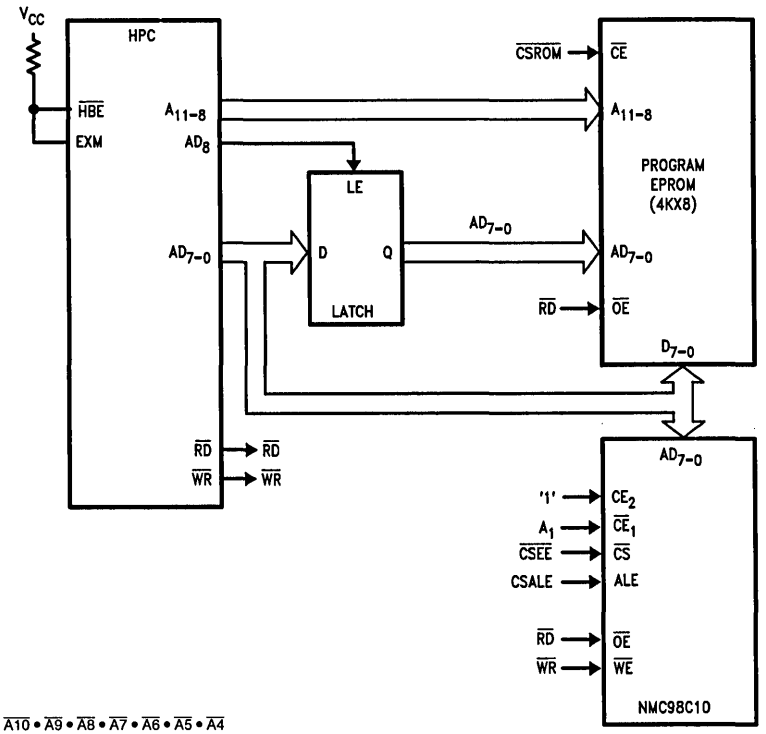
FIGURE 3. 16-Bit Interface



CSPORT = $\overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet \overline{A8} \bullet \overline{A7} \bullet \overline{A6} \bullet \overline{A5} \bullet \overline{A4}$
$\overline{CSROM}$ = CSPORT
CSALE = CSPORT • WR • $\overline{A0}$
$\overline{CSCC}$ = CSPORT • A0

TL/D/9416-5

FIGURE 4. Address Limited/Non-Multiplexed Interface

Device access with this interface takes two memory cycles. In the first cycle, the address to be accessed in the EEPROM is written out to the location allocated. The data is accessed in the second cycle by selecting the data location and performing the read or write function. This interface is possible because the address of the location to be accessed is stored in the on-chip address latch provided to support the multiplexed interface.

To implement the interface, the NMC98Cxx device on-chip address latch must be able to be selected as an output port. ALE of the NMC98Cxx device is used as an active high write enable. The address latch is loaded when it has been selected and data is valid from the processor, such as an HPC device. The simplest interface using an HPC device requires a logical AND of the address latch select signal with $\overline{WR}$ of the HPC device to perform the write enable function. The address latch select must be stable when write is active.

Device selection requires decode logic. If address space is critical, the EEPROM may have to be decoded using as few as two locations. The fewer locations available, the more addresses required for decode functions. A PAL device should be sufficient for most decode functions encountered.

Most HPC systems with multiple external devices will externally latch the addresses presenting a non-multiplexed bus to the devices. The device selection functions would use the latched addresses to guarantee stable addresses throughout a memory cycle. If multiplexed addresses aren't externally latched, the device selection signals must be latched. Individually latched selects are easily created in a PAL device. A non-multiplexed bus system doesn't have this concern.

In the example of *Figure 4*, the HPC is in Single-Chip ROMless mode. All but the the lower sixteen locations of the 4k address space are reserved for the external program EPROM. The address latch is decoded when A0 is low and the data is selected when A0 is high. A1 is used as a chip enable. To enable the device A1 must be low when loading the address latch, otherwise the device will be powered down. A7–4 and A1–0 are assumed to come from the external latch.

SUMMARY

The NMC98Cxx family is ideal for applications based on a multiplexed system bus. The family is primarily intended for microcontroller systems. The devices provide physically small, fast access, non-volatile, writeable memory with a multiplexed address/data bus interface. The previous examples illustrate that the NMC98Cxx family easily interfaces with microcontroller systems, systems with an address space limitation and non-multiplexed bus systems.

Using the NMC93CSxx Family

National Semiconductor
Application Note 507

INTRODUCTION

This application note is intended for system designers interested in using the NMC93CSxx family of CMOS serial EEPROM devices. These devices are well-suited for applications that call for non-volatile, writeable memory. The NMC93CSxx devices offer the additional benefit of selective write-protection by use of an on-chip protect register. This allows the device to perform both read-only memory (ROM) and EEPROM functions on the same chip.

EEPROMs are useful in a wide variety of applications because of their non-volatile, writeable characteristics. The devices can be used for applications that store configuration values, such as feature telephones, station presets on radios, and PC boards with configuration DIP switches and jumpers. Adaptive, closed-loop systems, such as environment controllers and motor controllers, can use EEPROMs to store loop control variables. Data logging is another of the many application areas of EEPROMS.

The NMC93CSxx family can support a new set of applications because of their additional capability to perform selective ROM functions. ROM is a requirement when the integrity of data stored in a device must be guaranteed. Applications can make use of this feature while at the same time allocating other locations in the device to operate as EEPROM.

The NMC93CSxx family devices exhibit extremely low power consumption due to the low drive requirements of their serial interface and the use of CMOS technology. The serial interface also provides the designer with a flexible interface mechanism allowing the devices to be easily designed into microcontroller and microprocessor systems. In microcontroller systems, or those with a serial bus, the devices can be connected with little or no support logic. The serial interface allows the device to fit in a smaller package, resulting in minimal board space requirements.

TABLE I. NMC93CSxx Family

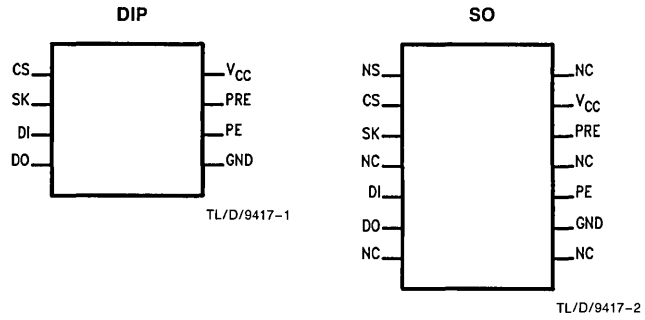
Device	Memory Size
NMC93CS06	16 x 16
NMC93CS26	32 x 16
NMC93CS46	64 x 16
NMC93CS56	128 x 16
NMC93CS66	256 x 16

NMC93CSxx FAMILY DESCRIPTION

The NMC93CSxx family is a set of 5 CMOS serial EEPROM devices with on-chip write-protection logic. The members of the family are differentiated by their memory array size, which ranges from 256 to 4096 bits organized 16 bits wide (see Table I). Because the devices use a serial interface, the pinout for each family member is identical. The devices conform to the MICROWIRE interface and are backwards compatible with previous National serial EEPROM devices (see *Figure 1*).

A set of 10 instructions are provided to control device operation. The general format of the instructions is a start bit (logic 1) followed by opcode, register address and data fields. The register address for the NMC93CS06/26/46 is 6 bits, while the register address for the NMC93CS56/66 is 8 bits. Data is shifted into the device on the D1 pin, and out on the DO pin following a low to high transition of SK. CS must be high to access the device (see Table 2).

A read operation is performed by issuing the start bit, the appropriate opcode (10), and the desired register address. The device responds by shifting out a dummy bit (logic 0) followed by the data in the selected register. The device will continue to shift data from subsequent registers as long as SK is active (non-volatile shift register mode). Write operations are performed by issuing the start bit, opcode (01), register address, and 16 bits of data. CS must be brought low to initiate the self-timed programming cycle, which includes an automatic erase cycle. CS can then be brought high to monitor DO (low to high transition) for completion of the cycle.



Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial In
DO	Serial Out
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

FIGURE 1. NMC93CSxx Device Pinout

TABLE II. NMC93CSxx Instruction Set

Instruction	SB	Op Code	Address	Data	PRE	PR	Comments
READ	1	10	A_X–A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_X–A_0	D15–D0	0	1	Write register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Write all register. Valid only when "protect register" is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in "protect register".
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A_X–A_0		1	1	Programs address into "protect register". Thereafter, memory address < the address in "protect register" are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the "protect register" cannot be altered.

The protect register is used to write protect a segment of registers. The value contained in the protect register designates the first address of the protected segment. All subsequent register locations are write-protected.

USING THE PROTECT REGISTER

The incorporation of the protect register in NMC93CSxx devices sets the family apart from other CMOS serial EEPROMs. Including a protect register allows the devices to function as EEPROM and ROM simultaneously. The distribution of EEPROM and ROM in a device is determined by the value in the protect register. The distribution of EEPROM and ROM can be changed in the system by changing the protect register value.

ROM applications typically require that data storage be non-volatile so that no changes will occur when power is turned off and read-only so that changes won't occur under any other circumstances. EEPROMs are non-volatile, but aren't read-only. An EEPROM will function as a ROM if write operations are never attempted or if any attempted write fails.

The protect register is valuable when an application requires a mix of EEPROM and ROM. A NMC93CSxx device can be made less susceptible to write problems without using the protect register. The entire device may be made read-only by grounding PE. System software can be implemented to avoid writing to read-only locations and limit when write instructions may be performed by making use of the write enable (WEN) and disable (WDS) instructions. The device would only be susceptible to a write problem if a system failure caused an illegal write or some external source with access to the device abused its write privileges. Use of the protect register under system control would be somewhat safer, but the device would still be subject to the above-mentioned problems. Write access to the protect register must be inhibited for the protected locations to be truly read-only.

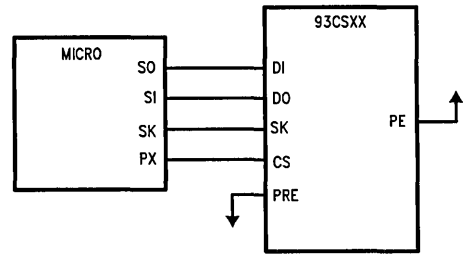


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FIGURE 2a. Protect Register Disabled

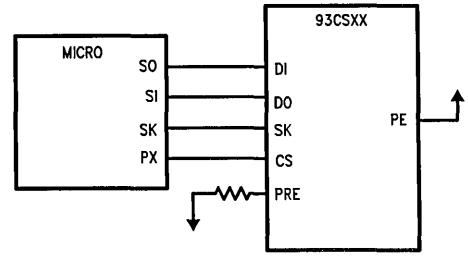

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FIGURE 2b. Protect Register Enabled with Pulldown

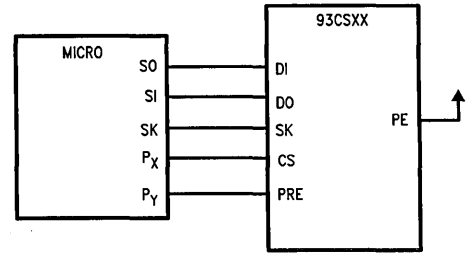

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FIGURE 2c. Protect Register Enabled

ROM devices are most often programmed with data before insertion into a PC board. This approach is applicable to NMC93CSxx devices. In a microcontroller system, program code or data could be off-loaded from the internal ROM of the microcontroller into a ROM section in an NMC93CSxx device. An EEPROM section could be allocated for any writeable data, such as configuration data values. ROM is desirable in this application because any spurious writes that could corrupt the program will be prevented, a smaller internal microcontroller ROM is possible and if ROM code or data needed alteration, it would be much easier and cheaper to reprogram a NMC93CSxx device than the internal ROM of the microcontroller. In manufacturing, the ROM data and the protect register value would be programmed into the device, and the protect register enabled before PC board insertion. The PRE pin would be tied low on the board to prevent write access to the protect register (see *Figure 2a*).

Another application for these devices is in systems that support automated production. Production information, such as date codes and status, would be programmed into the NSC93CSxx on a board as it progressed through each step of the production process. Board identification (serial number) and fixed configuration information could also be programmed into the device as a last step. The PRE pin would be pulled low with a resistor to allow production test equipment to drive it high to write data into the device and set the protect register, but prevent any writes to the protected locations during normal operations. The EEPROM section could be used to allow the application to support automated system configuration. Once all boards are placed in the system, any system configuration dependent variables could be programmed (see *Figure 2b*).

In data logging applications, the protect register is programmed as the data is gathered to reduce the likelihood of modification. When the protect register is accessed regularly by the software, PRE must be accorded an interface line, usually a port pin that is controlled by software. The protect register disable (PRDS) instruction must be used upon completion of logging to fully protect the data. PRDS will prevent any further writing to the protect register, even if the device is removed from the board. Extreme care should be exercised when considering use of PRDS. Data should be written into the device from high locations to low to protect the data as it is read in. In addition, the protect register then serves the dual purpose of being a pointer to the last location written, simplifying software and saving a variable location (see *Figure 2c*).

INTERFACING TO THE NMC93CSxx FAMILY

COP800 Interface

The COP800 family is a set of 8-bit CMOS microcontrollers. The family members differ by program and data memory, on-chip peripherals, and package size. Some members have on-chip EEPROM for program or data memory. The devices with EEPROM for program memory are only intended for development purposes. All members of the family have an on-chip MICROWIRE™ interface.

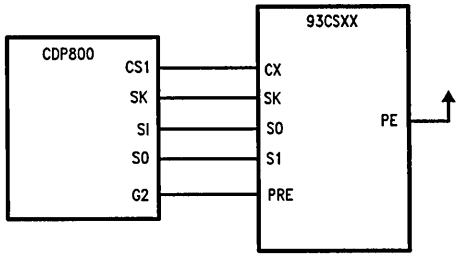

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FIGURE 3. MICROWIRE Interface

The COP800 family provides three options when interfacing to a NMC93CSxx device. The interface could be designed by using the COP800 device parallel port pins under software control, on-chip UART if available, or the MICROWIRE interface port. The most attractive option for the interface is the MICROWIRE because NMC93CSxx devices connect directly to it.

The MICROWIRE port provides a serial clock (SK), serial input (SI), and serial output (SO). These lines are directly connected to SK, DO and DI of the EEPROM. COP800 parallel port pins can be used for providing CS, PE and PRE. If PE or PRE are static in the application, they can be tied low or high. No other hardware is required for the interface (see *Figure 3*). In a system with multiple devices on the MICROWIRE, additional logic may be required to perform chip selection. If available, parallel port pins could be used for additional chip selects. Otherwise, a PAL device could be designed so that chip selects are set serially preceding any serial device operations.

```
;WREEPROM-WRITE DATA TO EEPROM
;
;THIS ROUTINE WILL WRITE A SPECIFIED NUMBER OF BYTES
;TO THE EEPROM USING THE MICROWIRE INTERFACE. THIS CODE
;ASSUMES THE SHIFT CLOCK RATE IS 1/2 THE XTAL FREQUENCY.
;THE ARGUMENT STRING CONSISTS OF A BYTE COUNT, OPCODE,
;REGISTER ADDRESS, FOLLOWED BY A DATA STREAM.
;
WREEPROM:  LD     A,[B+]   ;COPY BYTE COUNT
           X      A,x'F0   ;
           SBIT   1,x'D4   ;CHIP SELECT
           SBIT   7,x'E9   ;SEND START BIT
           SBIT   2,x'EF   ;
           RBIT   2,x'EF   ;
SLOOP:     LD     A,[B+]   ;SEND DATA BYTES
           X      A,x'E9   ;
           SBIT   2,x'EF   ;
BIT_TST:   IFBIT  2,x'EF   ;STILL BUSY?
           JMP    BIT_TST  ;
           DRSZ   x'F0     ;DONE SENDING?
           JMP    SLOOP    ;
           RBIT   1,x'D4   ;DROP CS
           RET
```

FIGURE 4. COP800 MICROWIRE Write Routine

```
;RDEEPROM-READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE MICROWIRE. THE CODE ASSUMES THAT THE
;SHIFT CLOCK IS PROGRAMMED AT 1/2 THE INSTRUCTION CLOCK RATE.
;THE ARGUMENTS PASSED TO THIS ROUTINE ARE A BYTE COUNT, OPCODE,
;AND REGISTER ADDRESS, POINTED TO BY B.
;THE BYTE COUNT AND DATA READ ARE POINTED AT BY B ON RETURN.
;
RDEEPROM:  LD    A,x'FE     ;SAVE POINTER
           X     A,x'F1     ;
           LD    A,[B+]     ;COPY BYTE COUNT
           X     A,x'F0     ;
           SBIT  1,x'D4     ;CHIP SELECT
           SBIT  7,x'E9     ;SEND START BIT
           SBIT  2,x'EF     ;
           RBIT  2,x'EF     ;
           LD    A,[B]      ;SEND INSTRUCTION
           X     A,x'E9     ;
           SBIT  2,x'EF     ;
TST1:      IFBIT 2,x'EF     ;BUSY?
           JMP   TST1       ;
           SBIT  2,x'EF     ;GET DUMMY BIT?
           RBIT  2,x'EF     ;
RLOOP:     CLRA             ;GET DATA BYTES
           SBIT  2,x'EF     ;
TST2:      IFBIT 2,x'EF     ;BUSY?
           JMP   TST2       ;
           X     A,x'E9     ;
           X     A,[B+]     ;
           DRSZ  x'F0       ;DONE GETTING?
           JMP   RLOOP      ;
           LD    A,x'F1     ;RESTORE POINTER
           X     A,x'FE     ;
           RBIT  1,x'D4     ;DROP CHIP SELECT
           RET
```

FIGURE 5. COP800 MICROWIRE Read Routine

Inside a COP800 device the MICROWIRE hardware consists of an 8-bit shift register (SIO), a control bit (BUSY) in the program status word (PSW), and a control register (CNTRL), BUSY is set by the control program to initiate a shift operation and is automatically reset when eight bits have been shifted. BUSY can be reset by the program for shift operations of less than eight bits. CNTRL is used to set the MICROWIRE mode and rate of SK. SK can be set to a divide by 2, 4, or 8 of the instruction clock rate. The MSEL bit of CNTRL sets the MICROWIRE to Master mode or Slave mode. In Master mode, a device will generate SK and in Slave mode it will receive SK. Master mode is used to interface to an NMC93CSxx device.

In addition to initializing the interface, software rountines are required to control data transfers to and from the EEPROM through the MICROWIRE port. The same routines used to read and write to the EEPROM can be used to execute the NMC93CSxx instructions, including accessing the protect register. The only extra step required to access the protect register is that PRE must be set high.

A routine must access SIO to perform an NMC93CSxx instruction. Since the MICROWIRE shift register is only eight bits wide, multiple accesses are required to complete an instruction. In addition, instructions aren't byte-aligned; routines must align the operation. Instructions can be byte-aligned by sending a single start bit followed by a byte of opcode and address. A start bit can be sent by using the set

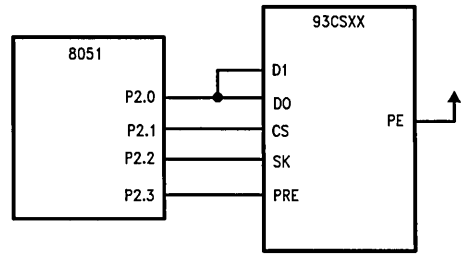
bit (SBIT) instruction to set BUSY, followed by the rest bit (RBIT) instruction when SK is being divided by two, or by sending a byte with seven leading zeros as dummy bits and a single one for the start bit. The NMC83CS56/66 devices require two more bits to be sent for alignment because of their larger address space. In this case it is easier to send the byte with leading zeros.

The write routine, WREEPROM, sets CS to select the device, then writes a single start bit, followed by a byte of opcode and address, and two bytes of data. The bytes sent are stored as a string preceeded by a byte-count. The byte count must, obviously, be three for a write. This routine can be used to perform the other write-only NMC93CSxx instructions by setting the byte-count and data string appropriately. CS is brought low to initiate the automatic erase/write cycle. The routine doesn't bring CS back high to check for completion of the cycle. This allows the routine to be used to perform the other NMC93CSxx instructions and the control program to perform other tasks during the cycle. If the program is unsure of cycle completion, DO should be checked before initiating another instruction (see *Figure 4*).

The read routine, RDEEPROM, sets CS and sends the start bit, opcode and address in the same manner as the write routine. The routine then reads a dummy bit (logic 0) from the EEPROM and the number of bytes of data specified by the byte-count. The dummy bit is read in exactly the same way as a start bit is sent (see *Figure 5*).

HPC Interface

The HPC family is a set of high performance 16-bit microcontrollers. Like the COPS microcontrollers, the HPC devices are MICROWIRE compatible, providing an excellent means of interfacing to NMC93CSxx devices. Though, a software controlled interface using parallel port pins could be used, as well as an on-chip UART.



TL/D/9417–7

FIGURE 7. 8051 Interface

```
#define    SET_CS    *_iporta|=0x40     /* set chip select*/
#define    DROP_CS   *_iporta & = 0xFB /* lower chip select*/
#define    SIO       0xD6             /* SIO register location*/
#define    PORTA     0xC8             /* PORT A location*/
#define    IRPD      0xD2             /* IRPD register location*/
#define    NOT_DONE I(*_Irpd & 0x04)  /* DONE flag set if true*/
#define    BFUN      0xF4             /* BFUN register*/
#define    SK                         \
           *_bfun & = 0xBF            \
           *_bfun | = 0x40;
#define    WR_EE (bytes, data)        \
{          int i;                     \
                                      \
           SK;                        \
           for(I=0; I < bytes; I++)\
           {                          \
            *_sio = *data++;          \
            while(NOT_DONE);          \
            *_irpd & = 0xFB;          \
           }                          \
}
/* Global Definitions*/
char       *_sio = SIO;
char       *_iporta = PORTA;
char       *_irpd = IRPD;
char       *_bufn = BFUN;

wr_eeprom(bytes,data)
int        bytes;   /* byte count*/
char       *data;   /* data buffer*/
{
           SET_CS;
           WR_EE;
           DROP_CS;
}

rd_eeprom(bytes, data)
int        bytes;   /* byte count*/
char       *data;   /* buffer pointer*/
{
           SET_CS;
           WR_EE (1, data);
           SK;                        /* get dummy bit*/
           for (i = 0; i < bytes; I ++){
             *data ++ = *_sio;
             while(NOT_DONE);
             *_irpd & = 0xFB;
           }
           DROP_CS;
}
```

FIGURE 6. HPC C Language Interface Routine

```
;
;SNDBYT - SHIFTS 8 BITS OF DATA TO EEPROM
;
;THIS ROUTINE SHIFTS A BYTE POINTED AT BY R0
;ASSUMES CHIP SELECT ALREADY ACTIVE (HIGH)
;
SNDBYT    MOV   B,#8     ;LOAD SHIFT COUNT
          MOV   A,@R0    ;GET BYTE
S_LOOP:   RLC   A        ;SHIFT
          MOV   P2.0,C   ;SEND BIT
          CLR   P2.2     ;SK
          SETB  P2.2     ;
          DJNZ  B,S_LOOP;DONE?
          RET
;
;WREEPROM - WRITE DATA TO EEPROM
;
;THIS ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO THE
;EEPROM USING SNDBYT UTILITY ROUTINE. THE DATA IS POINTED AT
;BY THE R0 REGISTER AND CONSISTS OF BYTE COUNT, OPCODE/REG ADDR
;AND DATA BYTES. DO IS SET HIGH TO AVOID CONTENTION.
;
WREEPROM: MOV   R2,@R0    ;COPY BYTE COUNT
          INC   R0        ;
          SETB  P2.1      ;CHIP SELECT
          CLR   P2.2      ;START BIT
          SETB  P2.2      ;
WR_LOOP:  LCALL SNDBYT    ;WRITE DATA BYTES
          INC   R0        ;
          DJNZ  R2,WR_LOOP;
          SETB  P2.0      ;DEFAULT DO HIGH
          CLR   P.21      ;DESELECT/PROGRAM
          RET
```

FIGURE 8. 8051 Parallel Port Pin Interface—Write Routines

The MICROWIRE interface provides signals for SK, SI and SO. CS, PE and PRE signals can be provided by using parallel port pins. Port A on the HPC is allocated for general use and is ideal for this function. When used in Master mode, the clock rate for the MICROWIRE is set by programming the appropriate value into the DIVBY register. The 8-bit SIO register is used as a buffer for serial operations.

Unlike the COP800 microcontrollers, the HPC does not use a BUSY bit to control shifting. The DONE flag in the IRPD register is polled to determine completion of a shift operation. A single bit can be transferred by changing the mode of the SK pin back to a general purpose port pin (B.6). This is accomplished by clearing bit six of the port B function register (BFUN). If port B bit six is high, the pin will go high immediately clocking the EEPROM.

```
;RCVBYT - READ A BYTE OF SERIAL DATA
;
;THIS ROUTINE WILL SERIALLY READ 8 BITS OF DATA FROM THE PORT PIN
;AND STORE THE DATA IN THE LOCATION POINTED AT BY R0
;
RCVBYT:    MOV   B,#8       ;LOAD SHIFT COUNT
R_LOOP:    CLR   P2.2       ;SK
           SETB  P2.2       ;
           MOV   C,P2.0     ;GET BIT
           RLC   A          ;SHIFT
           DJNZ  B,R_LOOP   ;DONE?
           MOV   @R0,A      ;STORE DATA
           RET
;RDEEPROM - READ DATA FROM EEPROM
;
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE RCVBYT ROUTINE. INPUT ARGUMENT STRING IS
;A BYTE COUNT, AND OPCODE/REGISTER ADDRESS. ON RETURN, R0 POINTS
;TO A STRING CONTAINING THE BYTE COUNT FOLLOWED BY DATA BYTES
;
RDEEPROM:  MOV   R2,@R0     ;COPY BYTE COUNT
           PUSH  R0         ;SAVE POINTER
           INC   R0         ;
           SETB  P2.1       ;CHIP SELECT
           CLR   P2.2       ;START BIT
           SETB  P2.2       ;
           LCALL SNDBYT     ;SEND INSTRUCTION
           SETB  P2.0       ;DEFAULT DO HIGH
           CLR   P2.2       ;DUMMY BIT
           SETB  P2.2       ;
RD_LOOP    LCALL RCVBYT     ;GET DATA BYTES
           INC   R0         ;
           DJNZ  R2,RD_LOOP;DONE?
           POP   R0         ;RESTORE POINTER
           CLR   P2.1       ;DESELECT
           RET
```

FIGURE 9. 8051 Parallel Port Pin Interface Read Routines

The HPC supports program development in the C language. The software routines to support an HPC interface are similar to those for the COP800, except that they are written in C (see *Figure 6*). The main difference is how the start bit and dummy read bit are handled. Since the HPC supports the C language, core routines are written utilizing macros, eliminating the overhead of an extra level of subroutine calls.

8051 Interface

The 8051 offers two interface alternatives for the NMC93CSxx family; the first uses parallel port pins under software control and the second is based on using the on-chip serial port. Both interfaces require a minimum number of device pins and no support logic. The main differences are that the serial port is faster and requires less software.

The first choice for discussion is the use of the port pins. The 8051 has four 8-bit bidirectional I/O ports. The ports are accessed through a special function register. The port registers are bit addressable which facilitates their use in this application. The minimum interface requires the use of only three port pins. A pin for CS, SK, and one connected to both DI and DO (see *Figure 7*). A two wire interface is possible by tying CS active, but this leaves the device in the active (high power) state and prevents the device programming cycle from being executed.

It is not necessary to have separate lines for DI and DO because DO is placed in a high-Z condition during write operations. During a read operation the DI pin is driven to send the instruction to the EEPROM and DO outputs the dummy bit (0) and data. To prevent contention DI has to stop driving a high before DO can output the dummy bit. The 8051 doesn't drive a high, it uses internal pull-ups to obtain a high, so there is no contention problem. This may be a con-

cern in other designs. The DO pin is driven when CS is brought high following a write operation to time completion of programming Contention will occur on the operation following a write if programming completion isn't checked. A dummy check can be used.

When using the port pins, one must consider that some of the port pins have alternate functions. For example, Port 3 pins 0 and 1 are also allocated for the serial port. Similarly, if the program being executed on the 8051 resides in external memory, then Ports 0 and 2 will serve as the system bus during external memory access.

The software support routines are primarily concerned with controlling the flow of data to/from the EEPROM. Because the 8051 is an 8-bit machine, two utility routines, SNDBYT and RCVBYT, are used to shift a byte of data to and from the NMC93CSxx.

The write routine, WREEPROM, raises CS to access the device, shifts out a start bit, then calls SNDBYT to shift out the opcode/register address byte, and other data bytes, as specified by the byte-count (see *Figure 8*).

The read routine, RDEEPROM, starts out by raising CS, sending a start bit, and using SNDBYT for the opcode/register address byte. The dummy bit is then shifted from the device and RCVBYT is called to shift in the number of bytes of data specified by the byte-count (see *Figure 9*).

```
;RDEEPROM - READS DATA FROM NMC93CSXX DEVICE
;
;THE ROUTINE READS A SPECIFIED NUMBER OF BYTES FROM
;THE EEPROM USING THE SERIAL PORT. R0 POINTS TO AN ARGUMENT STRING
;CONTAINING THE BYTE COUNT AND THE OPCODE/REGISTER BYTE
;A STRING IS RETURNED CONTAINING THE BYTE COUNT FOLLOWED BY DATA.

RDEEPROM:
            PUSH   R0        ;SAVE POINTER
            MOV    R2,@R0    ;COPY BYTE COUNT
            INC    R0        ;
            SETB   P2.1      ;CHIP SELECT
            CLR    P3.1      ;SEND START BIT
            SETB   P3.1      ;
            MOV    SBUF      ;SEND INSTRUCTION
            JBC    TI$       ;DONE?
            CLR    TI        ;
            CLR    P3.1      ;GET DUMMY BIT
            SETB   P3.1      ;
            SETB   REN       ;GET DATA BYTES
RLOOP;      JBC    RI,$      ;DONE?
            CLR    RI        ;
            MOV    @R0,SBUF  ;
            INC    R0        ;
            DJNZ   R2,RLOOP  ;
            CLR    REN       ;
            CLR    P2.1      ;DESELECT
            POP    R0        ;RESTORE POINTER
            RET

;WREEPROM - WRITE DATA TO EEPROM
;
;THE ROUTINE WRITES A SPECIFIED NUMBER OF BYTES TO EEPROM
;POINTED AT BY R0. ARGUMENTS INCLUDE BYTE COUNT AND OPCODE/ADDRESS
;
WREEPROM:   MOV    R2,@R0    ;COPY BYTE COUNT
            INC    R0        ;
            SETB   P2.1      ;CHIP SELECT
            SETB   P3.0      ;START BIT
            CLR    P3.1      ;
            SETB   P3.1      ;
SLOOP:      MOV    SBUF,@R0  ;SEND DATA BYTES
            INC    R0        ;
            JBC    TI,$      ;DONE?
            DJNZ   R2,SLOOP  ;
            CLR    P2.1      ;DESELECT
            RET
```

FIGURE 10. 8051 Serial Port Read and Write Routines

8051 INTERFACE—SERIAL PORT

The 8051 serial port operates in one of four modes: 8-bit shift register, 8-bit UART and two different 9 bit UART modes. The 8-bit shift register mode (Mode 0) is preferred because it operates with no protocol, as opposed to the UART modes which send and receive packeted data. When in Mode 0, the 8051 RxD pin is used as a serial in/out pin and the shift clock is provided on the TxD pin. The TxD pin would be connected to SK and RxD would be connected to DI and DO on the NMC93CSxx device. CS, PE and PRE would be connected the same way as in the port pin interface.

When using the serial port in Mode 0, the serial port control register (SCON) must be programmed by setting the SM0 and SM1 bits (bits 7 and 6) to 0. The serial clock runs at a fixed rate of $1/12$ of the oscillator frequency. The maximum frequency for the serial clock on NMC93CSxx devices is 1 MHz. This means the 8051 can run with an oscillator frequency up to 12 MHz. After every eighth bit is received or transmitted the 8051 hardware will set either the receive interrupt (RI) or transmit interrupt (TI) bit in SCON. These bits may be polled, or used to generate interrupts.

The software routines for the serial port interface are virtually the same as those for the previous example. The only differences are that the 8051 serial port performs the same functions as the SNDBYT and RCVBYT routines. Instead of calling these routines, the REN bit is enabled to initiate reception and the data is read from the serial buffer (SBUF). For writing, the data is written into SBUF to perform the transfer. The routines poll the RI or TI bits. Because data transactions are synchronous, interrupts are not applicable (see *Figure 10*).

8096 INTERFACE

The 8096 is a 16-bit microcontroller. Like other microcontrollers, it interfaces easily to the NMC93CSxx devices. The use of parallel port pins or the on-chip serial port provide two interface options.

When implementing the parallel port pin interface, the choice of the port pins used is more critical because more of these pins have alternate functions. If the 8096 must perform external memory accesses, the use of Ports 3 and 4 becomes a problem because these two 8-bit ports make up the address/data bus. Port 0 pins are used for the analog input channels. Port 2 pins have alternate functions such as the serial port. Port 1 pins do not have alternate functions and may be preferred for use.

The 8096 provides an on-chip serial port which may be used for interfacing the NMC93CSxx devices. The serial port has 4 modes of operation. The mode of interest for this application is the shift register mode (Mode 0). The 8096 shift register mode serial clock rate is not a fixed rate. It is therefore the responsibility of the support software to program the baud rate appropriately.

INTERFACING NMC93CSxx WITH HIGH PERFORMANCE MICROPROCESSORS

High performance microprocessors like the NS32000, iAPX386 and the MC680x0 are usually implemented as central processor in computers and aren't directly involved with peripheral devices. Rather, these machines communicate over a backplane bus. These processors are designed for high speed, parallel data transfers. The NMC93CSxx devices could be used with these processors if a serial bus is implemented as part of the backplane bus. Typically, a serial bus would be used for system configuration or diagnostic purposes. Both the VME bus and Multibus II supply serial communication signals that may be used to interface NMC93CSxx devices to a high performance processor.

SUMMARY

The NMC93CSxx family can be used in a wide variety of applications. The devices provide a non-volatile, writeable memory that requires the least amount of board space, support logic and power. The protect register allows for a flexible mix of RAM and ROM. The previous examples illustrate that the NMC93CSxx family easily interfaces to microcontrollers and systems with a serial bus.

```
;RCYBYT - READ UTILITY ROUTINE
;
;THIS ROUTINE WILL READ 8 BITS OF DATA FROM THE SERIAL PORT
;THE DATA IS STORED IN THE LOCATION POINTED AT BY THE DX REGISTER.
;
RCVBYT:    LDB   AH,#8        ;LOAD SHIFT COUNT
BOP_SK:    ANDB  P2,#FBH      ;STROBE SK
           ORB   P2,#04H      ;
           JBS   P2,3,BIT_1   ;READ BIT
           ANDB  AL,#FEH      ;
           SJMP  R_SHIFT      ;
BIT_1:     ORB   AL,#01H      ;
R_SHIFT:   SHLB  AL,1         ;
           DECB  AH           ;DONE?
           JNE   BOP_SK       ;
           LDB   (DX),AL      ;SAVE DATA
           RET

;RDEEPROM - READ DATA FROM EEPROM
;
;SI, SK, CS, SO = P2[3 . . . 0]
;THIS ROUTINE WILL READ A SPECIFIED NUMBER OF BYTES FROM THE
;EEPROM AND STORE THE DATA. ARGUMENTS SUPPLIED TO THIS ROUTINE
;ARE A BYTE COUNT, OPCODE/REGISTER ADDRESS, AND ADDRESS FOR
;STORING THE DATA.
;
RDEEPROM:  PUSH  DX           ;SAVE POINTER
           LDB   BL,(DX)+     ;COPY BYTE COUNT
           ANDB  P2,#F0H      ;CHIP SELECT,START BIT
           ORB   P2,#03       ;
           ORB   P2,#04       ;
           LCALL SNDBYT       ;SEND INSTRUCTION
           ANDB  P2,#FBH      ;GET DUMMY BIT
           ORB   P2, #04H     ;
RD_LOOP:   LCALL RCVBYT       ;GET DATA BYTES
           INC   DX           ;
           DECB  BL           ;DONE?
           JNE   RD_LOOP      ;
           ANDB  P2,#FDH      ;DESELECT
           POP   DX           ;RESTORE POINTER
           RET
```

FIGURE 11. 8096 Port Pin Interface Read Routines

```
;SNDBYT - WRITE 8 BITS OF DATA TO PORT PIN
;
;THIS ROUTINE WILL WRITE 8 BITS OF DATA TO THE PORT PIN. THE
;DATA BYTE IS POINTED AT BY THE DX REGISTER.
;
SNDBYT:    LDB   AH,#8        ;LOAD SHIFT COUNT
           LDB   AL,(DX)      ;GET DATA BYTE
SLOOP:     JBS   AL,7,BIT_1   ;SEND BIT
           ANDB  P2,#FEH      ;
           SJMP  TOG_SK       ;
BIT1:      ORB   P2,#01H      ;
TOG_SK:    ANDB  P2,#FBH      ;
           ORB   P2,#04H      ;
           SHLB  AL           ;
           DECB  AH           ;DONE?
           JNE   SLOOP
           RET

;WREEPROM - WRITE DATA TO EEPROM
;
;SI, SK, CS, SO = P2[3..0]
;THIS ROUTINE WILL WRITE A SPECIFIED AMOUNT OF BYTES TO THE
;EEPROM. THE DATA TO BE WRITTEN IS POINTED AT BY THE DX REGISTER.
;THE ARGUMENTS INCLUDE THE BYTE COUNT, OPCODE/REGISTER ADDRESS,
;AND 1 OR MORE DATA BYTES.
;
WREEPROM:  LDB   BL,(DX)+     ;COPY BYTE COUNT
           ANDB  P2,#F0H      ;CHIP SELECT, START BIT
           ORB   P2,#03H      ;
           ORB   P2,#04H      ;
WR_LOOP:   LCALL SNDBYT       ;SEND DATA BYTES
           INC   DX           ;
           DECB  BL           ;DONE?
           JNE   WR_LOOP      ;
WR_EXIT:   ANDB  P2#FDH       ;DESELECT/PROGRAM
           RET
```

FIGURE 12. 8096 Parallel Port Pin Interface Write Routines

The Reliability of National Semiconductor's EEPROM Products

This applications note provides the non-volatile memory system designer with the necessary information to design reliable non-volatile memory subsystems. The first section is an introduction to EEPROM technology. Next, is a description of the intrinsic failure mechanisms common to all EEPROM devices. The third section is a description of the reliability aspects of National Semiconductor's manufacturing process.

INTRODUCTION TO EEPROM TECHNOLOGY

EEPROM Background

The Electrically Erasable Programmable Read Only Memory (EEPROM) is a non-volatile, fully static data storage device which is also electrically erasable. It can be erased and written rapidly without removing the chip from the end application system or using a PROM programmer. The technology allows for both byte- and chip-clear operations. These advantages are in contrast to UVPROMs which require removal from the system and total erasure of all the bits on the chip.

Technology Description

National Semiconductor's NMOS EEPROM devices utilize a 2.5 micron process. This technology was developed from the basic NMOS double poly process, which National Semiconductor's Memory Division has been using for about 10 years.

The new family of CMOS devices is based on National's 2 micron M^{2}CMOS process, which is the process National Semiconductor uses most widely for such diverse products as: Gate Arrays, Telecom, Microprocessing and many others. It is presently fabricated in one of the most modern, state-of-the-art, 6 inch wafer fab facilities in the world.

Device Description

National Semiconductor EEPROM devices utilize a double poly silicon gate process. *Figure 1* depicts the basic memory element in cross section. It is comprised of an N-channel transistor with an additional floating polysilicon gate sandwiched between the control gate and the transistor channel region. The gate structures are separated from each other and from the transistor channel and drain regions by silicon dioxide (SiO_2). A tunnel oxide which is less than 120 Angstroms thick is used in the region between the floating polysilicon gate and the N^+ drain region. National's E^2 Cell allows individual bit erasing and writing.

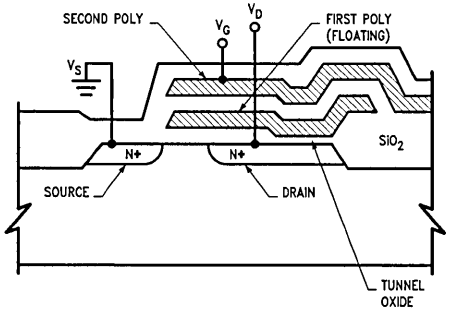


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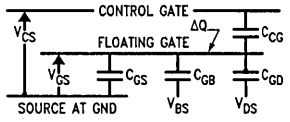
FIGURE 1. Cross Section of MOS Floating Gate EEPROM

EEPROM technology relies upon stored charge on the floating gate to retain information. Floating and control gate voltages are referenced to the source which is grounded. A mode of the equivalent capacitances and voltages for an EEPROM is shown in *Figure 2*. V_{GS} is the voltage on the floating gate, and delta Q is the charge stored on the floating gate. The charge remains on the floating gate even when power is not applied because the surrounding silicon dioxide serves as an excellent insulating material. Electrons are transferred to and from the floating gate and the underlying MOS device through a process known as Fowler-Nordheim tunneling.



TL/X/0006-2

$$V_{GS} = \frac{V_{CS}C_{CG} + V_{DS}C_{GD} + V_{BS}C_{GB} + \Delta Q}{C_{GS} + C_{GB} + C_{GD} + C_{CG}}$$

FIGURE 2. Equivalent Capacitances and Voltages

Tunneling Physics

The non-volatile memory storage in EEPROMs takes advantage of a quantum mechanical phenomenon known as Fowler-Nordheim tunneling. This tunneling process is a function of the energy levels of the materials involved. A schematic of the energy configuration for an EEPROM is illustrated in *Figure 3*. The energy difference between the valence and conduction bands in silicon dioxide (SiO_2) is about 9.05 eV. The energy difference between the same two bands for silicon (Si) is approximately 1.1 eV. When the SiO_2 and the Si are joined together the conduction band of the SiO_2 is 3.25 eV above the conduction band of the Si, while the valence band of the SiO_2 lies about 4.7 eV below the valence band of the Si. Since the thermal energy of an electron at room temperature (23°C) is only 0.025 eV the likelihood of an electron jumping from the valence band of the SiO_2 to the conduction band of the SiO_2 is very slight.

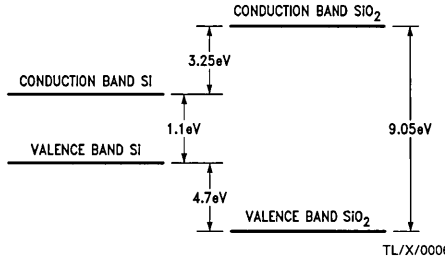


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FIGURE 3. Energy Band Diagram of the Si and SiO_2 System in its Neutral State

Fowler-Nordheim tunneling predicts that these energy bands can be distorted in the presence of an electric field. This process is depicted in *Figure 4*. In EEPROMs, tunneling of electrons occurs between the drain and floating gate through the SiO_2 tunneling region. The direction of Fowler-Nordheim tunneling of electrons through the tunneling region depends on the polarity of the voltages between the control gate and the drain. Tunneling physics predicts that when the electric fields across a thin insulator, such as SiO_2, are high enough, electrons from the negative electrode can acquire enough energy to pass or tunnel through the forbidden gap and enter the conduction band. The resulting current flux (J) is approximately proportional to an exponential function of the applied voltage (V) as illustrated in *Figure 5*. In order to obtain fields strengths large enough to initiate tunneling ($V > 7 \times 10^6$ eV/cm), at reasonable voltages (20V), the SiO_2 layer must be limited to a thickness less than 120 Angstroms.

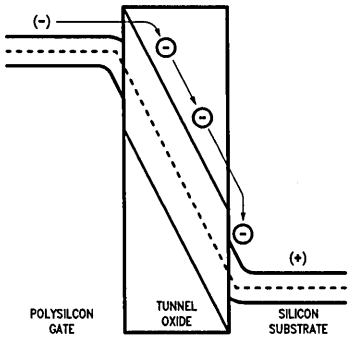

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FIGURE 4. Distortion of Energy Bands in the Presence of a Strong Electric Field

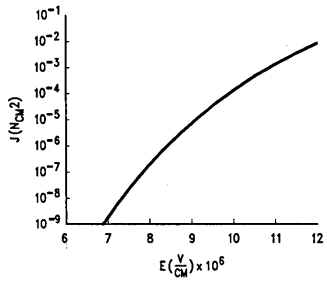

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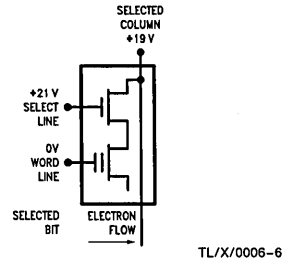
FIGURE 5. Fowler-Nordheim Tunneling I-V Characteristic

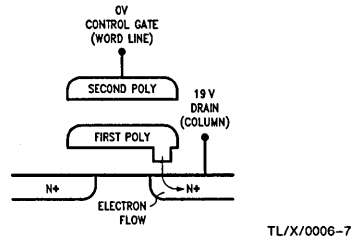
Device Operation

To write the cell to logic "0" the control gate is set to ground potential, and a high voltage (19V) is applied to the drain, while the source is left floating. The write operation is shown in *Figure 6*. This causes electrons on the floating gate to tunnel through the SiO_2 into the drain. In this configuration the transistor will allow current to flow. The electric field strength is highest in the region between the floating gate and the drain. Hence tunneling occurs in this thin SiO_2 region. The electric field intensity across the tunneling SiO_2 region is determined by the capacitive coupling ratio of the cell.



TL/X/0006-6

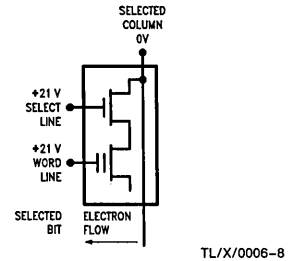
E^2PROM Transistor Write



TL/X/0006-7

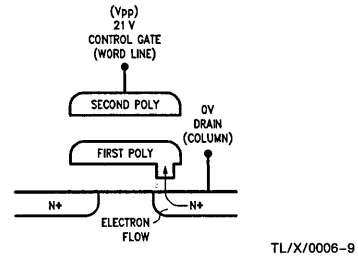
FIGURE 6. Write Operation

During the erase operation the drain is set to ground potential while the control gate is pulled up to 21V, as shown in *Figure 7*. This charging of the control gate causes the floating gate to become capacitively coupled with a positive bias and electrons then tunnel from the drain into the floating gate. The transfer of electrons shifts the cell threshold positive forcing the transistor to pinch-off current flow, which is then interpreted as a logic "1" state at its output.



TL/X/0006-8

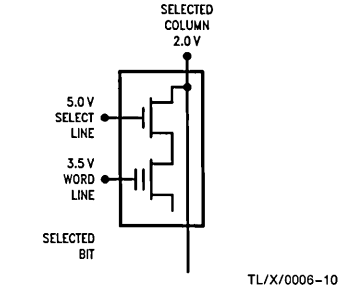
E^2PROM Transistor



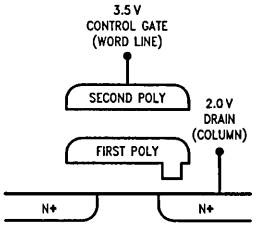
TL/X/0006-9

FIGURE 7. Erase Operation

E²PROM Transistor



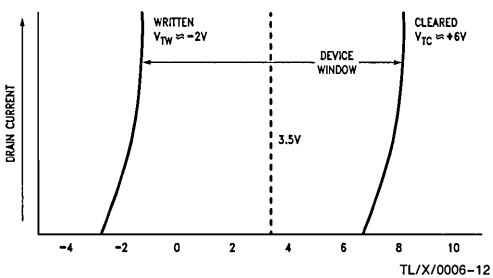
TL/X/0006-10



TL/X/0006-11

FIGURE 8. Read Operation

The read operation is illustrated in *Figure 8*. To read the bit, 3.5V is applied to the gate of the transistor (word line). The charge stored on the floating gate influences the transistor characteristics. When the floating gate has a net negative charge, the transistor will not conduct current, and while positively charged it will pass current. Distinguishing between current flow and non-current flow allows logical states to be represented by the transistor. *Figure 9* illustrates the situation. When written to, the threshold voltage of the transistor (V_{th}) is equal to $-2V$ and the transistor is turned on. This is subsequently read as a logical 0 on the memory pins. While the bit is erased the threshold voltage will be 6V, the transistor remains off, and the logic is interpreted at the output as a logical 1. This difference between high and low voltage states is known as the cell margin, logic margin, or device window.



TL/X/0006-12

FIGURE 9. I-V Characteristics of Floating Gate EEPROM

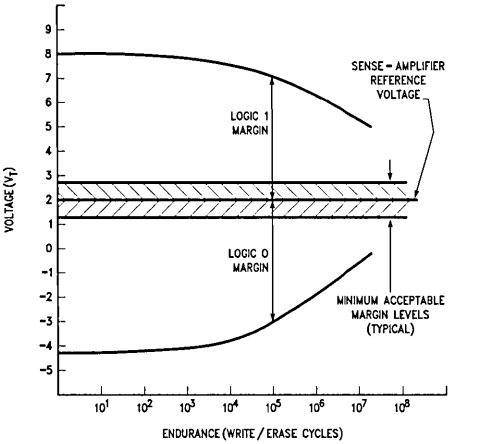
INTRINSIC FAILURE MECHANISMS

EEPROMs and light emitting diodes differ from many other semiconductor devices in that they wear out with use. However, with a basic understanding of the intrinsic wear out and failure mechanisms associated with EEPROMs, the designer can construct systems which successfully account for these limitations. The three primary failure mechanisms which affect all EEPROMs are charge trapping and tunnel oxide breakdown which are endurance related, and charge leakage which is data retention related.

Endurance

An EEPROM's endurance—that is, the number of write and erase operations through which each bit can be cycled reliably—is based largely on the degradation of cell margin. The amount of charge that can be stored and removed from an EEPROM cell decreases as the cumulative number of programming cycles rises.

Charge trapping is an intrinsic failure mechanism associated with EEPROMs which tends to narrow the difference between negatively and positively charged threshold voltages (device window) as a function of erase/write cycles. Eventually, after several million cycles, the window is collapsed completely. *Figure 10* illustrates the situation. This charge trapping is cumulative, and increases proportionally with the magnitude and duration of the programming current.



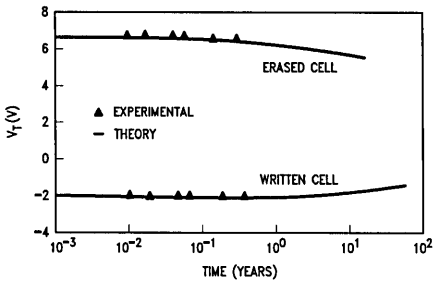
TL/X/0006-13

FIGURE 10. Logic Margin vs Endurance for Floating Gate EEPROM

Tunnel oxide breakdown is the primary intrinsic failure mechanism limiting the endurance of EEPROMs. Tiny defects in the tunneling oxide, caused by imperfections in the manufacturing process, can distort the electric field and cause large localized gradients. Excessive amounts of current flow through the regions where the electric field is tightly concentrated leading to high localized mechanical stresses. As write cycles continue, the probability that some imperfection in the oxide will break down increases. Given enough time, the cell will fail to operate correctly because the silicon dioxide which insulates the floating memory cell from the underlying voltage drain will become shorted. The rate of failures due to tunnel oxide breakdown can be reduced by minimizing particulate contaminants, decreasing the cross sectional area as much as is photo-lithographically possible, and controlling the ramp rate of the programming voltage so as to decrease the peak electric field which is created across the tunneling oxide.

Data Retention

Data retention in an EEPROM specification refers to the device's ability to retain a charge on its floating gate with or without an applied bias to the control gate, over extended periods of time. A floating gate on an EEPROM cell requires between one to five million electrons as stored charge. In order to store this amount of charge a current of approximately 10^{-10}A is required for a period of 10 ms. To insure that a wide enough logic margin exists on the cell, the designed floating gate leakage is limited to 10% of the initial charge (1.0^{-10}A) over a period of 10 years. This means that for continuous reading or storage operations over this period, the leakage must be kept below 10^{-21}A per cycle. *Figure 11* shows a typical plot of logic margin vs. time for EEPROMs.



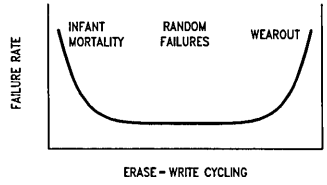
TL/X/0006-14

FIGURE 11. Logic Margin vs Data Retention of MOS Floating Gate EEPROM

Fowler-Nordheim tunneling, the process responsible for charging the floating cell, is also the means by which charge is leaked from the storage cell. This failure mechanism falls into a very broad class of failures which are proportional to $\exp(-E_a/kT)$ where E_a is the activation energy of the process, k is Boltzmann's constant, and T is the absolute temperature. This is very useful because if the activation energy is known for a given process, then tests can be conducted at elevated temperatures, reducing testing time, and the data can be extrapolated to lower operating temperatures using the relationship above.

Combined Effects

The total failure rate of an EEPROM is the sum of the combined rates from all the failure mechanisms involved. *Figure 12* shows the observed failure rate vs. erase/write cycling for EEPROMs. The distribution is a bathtub-shaped curve. The infant mortality region is characterized by an initially high, but rapidly decreasing failure rate. This period is dominated by failures which arise from manufacturing defects. Burn in reliability measures taken during National Semiconductor's manufacturing process are designed to eliminate these devices before they can be shipped to customers. The middle region is dominated by random failures and the rate is approximately level until the wearout region is reached. The wearout region is characterized by an increasing failure rate as the device reaches the end of its useful life.



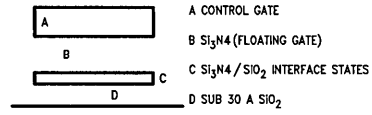
TL/X/0006-15

FIGURE 12. Typical Failure Curve for MOS Floating Gate EEPROM

Comparison to Other Technologies

CMOS static RAM devices with battery backup are often used for non-volatile memory storage. While the CMOS device does not exhibit the wearout mechanisms associated with EEPROM technology, the batteries associated with them do. Nickel Cadmium batteries have a wearout mechanism. Typically, they are good for only a couple of years before they must be replaced. Lithium batteries wear out with use and they display another liability in the fact that when shorted they can become very hot. Cost is another consideration when comparing battery backed up memory vs. EEPROM technology for small sized memory applications. Batteries and their associated mounting hardware can be quite expensive.

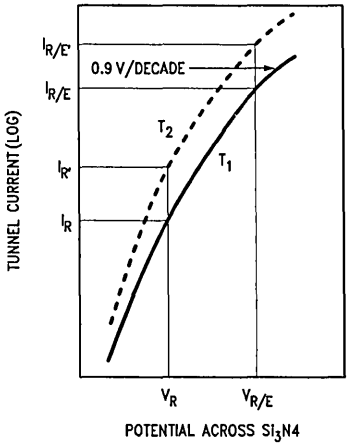
MNOS



TL/X/0006-16

FIGURE 13. Cross Section of Nitride EEPROM

Some semiconductor manufacturers use nitrides in the production of their EEPROMs, resulting in two similar classes of memories known as SNOS and MNOS devices. A cross section of one of these nitride EEPROMs is illustrated in *Figure 13*. Its operation is similar to an MOS EEPROM. The nitride layer is analogous to the floating gate on the MOS devices. One of the problems encountered with the nitride technology is its temperature dependence on the current/voltage curve. This effect is shown in *Figure 14*. As the temperature increases the curve shifts up and to the left. The higher temperature causes a large increase in current for the same read voltage. This leads to poor data retention because Fowler-Nordheim tunneling is enhanced at these higher current levels and thus large amounts of charge can leak with each read cycle. Transistor voltages on nitride structures are also adversely affected by even small voltage stresses. The final problem associated with this technology is that the oxide-nitride interface is degraded by silicon-gate processing.



TL/X/0006-17

FIGURE 14. Current Increase from Increased Temperature Leading to Loss of Data Retention for Nitride EEPROM

On the other hand, MOS EEPROMs which use a polysilicon floating gate structure, tend to have better endurance characteristics and superior data retention under voltage and/or temperature stress. Polysilicon floating gate devices also have a longer history in processing, which accounts for their reproducibility and slow wear out as compared to nitride systems.

RELIABILITY ASPECTS OF EEPROMs IN MANUFACTURING

All of the inherent failure mechanisms associated with EEPROM technology can be reduced by applying quality control techniques during the manufacturing process. Quality control measures the component's conformance to specification. Careful monitoring of both the process and the individual devices assures the customer of the highest possible reliability.

Quality Control

The introduction of any new part into the National Semiconductor product line requires first that the product must pass strict design and manufacturing requirements. A table of the reliability qualification procedure which National Semiconductor follows for the introduction of a new EEPROM product appears in Table I.

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products

	Test	Sample	Allowed Fail.
J Pkg.	Operating Life 125°C 1000 Hrs.	3 x 105	2/Lot 5% LTPD (0.78 AQL)
	Dynamic B-I at 5.5. All inputs exercised. (Read, Disable, Read, Disable . . .)		

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products (Continued)

	Test	Sample	Allowed Fail.
N Pkg.	1) Operating Life 125°C 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	2) 85/85 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1. 3 AQL)
	3) Autoclave 168 Hrs. (No Bias)	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	4) Bias Pressure Cooker 96 Hrs. (Static B-I)	3 x 105	2/Lot 5% LTPD (1.3 AQL)

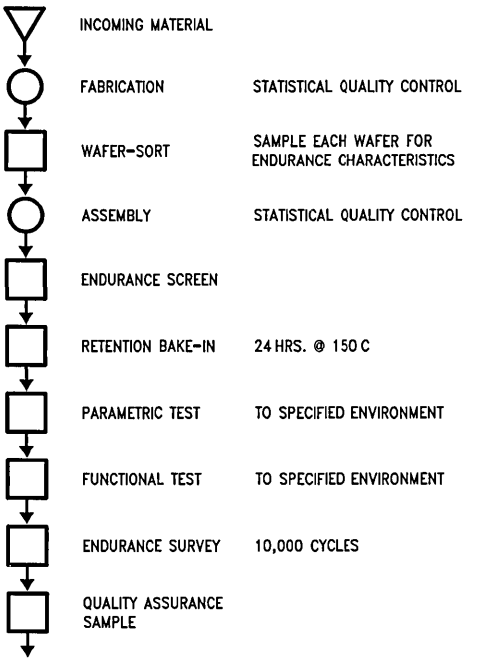


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FIGURE 15. Quality Control Steps for National Semiconductor EEPROMs

For EEPROMs which are in the manufacturing phase, statistical quality control and testing are used to evaluate product compliance to specification. *Figure 15* shows a flow chart of the various quality control steps which National Semiconductor puts their EEPROM chips through.

Burn In

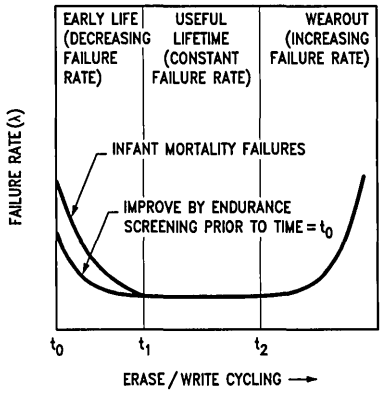
In addition to strict qualifying requirements of products prior to manufacture and tight quality control procedures, National Semiconductor also implements burn-in tests, which weed out the weaker chips, and ensure an even higher level of reliability for the surviving EEPROMs. *Figure 16* is an illustration of typical improvements in product reliability resulting from burning in chips, and removing the ones which would normally fail in the infant mortality region.

RELIABILITY ASPECTS OF EEPROMs IN APPLICATIONS

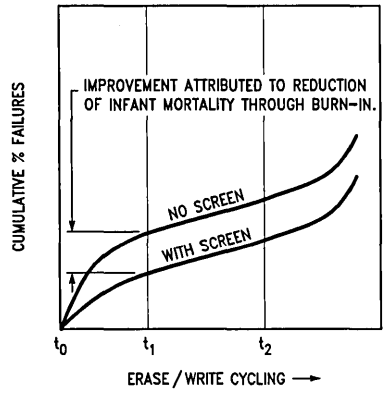
Reliability Testing and Results

Endurance failure in EEPROM testing is often defined in very different ways. One of the more lenient methods of describing failures on an EEPROM is to simply say that every non-operative cell in a memory device constitutes one failure. National Semiconductor, however, chooses to use a fundamentally more rigorous definition, in which a failure is indicated the first time any single memory bit on the entire chip fails. Depending on memory size and specific devices, one can typically expect a failure rate over 10,000 erase/write cycles of about 3% or less. Of this small percentage of chips which fail after ten-thousand cycles, seldom will any have more than a single-bit error.

It is important to note that the two modes of EEPROM failure, endurance and data retention, are fundamentally orthogonal in applications. That is, a cell that is to be written 10,000 times does not require data retention of 10 years between writes, unless of course you require that the product operate for 100,000 years. Further, even adjacent cells in an EEPROM memory device operate independently from each other, so that any given memory location that is updated only upon rare occasions can be expected to retain its information for long periods, even though adjacent cells are being worn out through extended cycling.



TL/X/0006-19



TL/X/0006-20

FIGURE 16. Improvements Attributed to National Semiconductor's Endurance Screen

Section 4

PROMs

Section 4 Contents

Bipolar PROM Selection Guide

Non-Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
256	32 x 8 OC	16	DM54S188	45	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188	35	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288	45	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288	35	20	110	0°C to +70°C
	32 x 8 OC	16	DM54S188A	35	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188A	25	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288A	35	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288A	25	20	110	0°C to +70°C
	32 x 8 TS	16	PL87X288B	15	12	140	0°C to +70°C
1024	256 x 4 OC	16	DM54S387	60	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387	50	25	130	0°C to +70°C
	256 x 4 TS	16	DM54S287	60	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287	50	25	130	0°C to +70°C
	256 x 4 OC	16	DM54S387A	40	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387A	30	20	130	0°C to +70°C
	256 x 4 TS	16	DM54S287A	40	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287A	30	20	130	0°C to +70°C
2048	512 x 4 OC	16	DM54S570	65	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570	55	30	130	0°C to +70°C
	512 x 4 TS	16	DM54S571	65	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571	55	30	130	0°C to +70°C
	512 x 4 OC	16	DM54S570A	60	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571A	60	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571B	50	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571B	35	25	130	0°C to +70°C
	256 x 8 TS	20	DM54LS471	70	35	100	−55°C to +125°C
	256 x 8 TS	20	DM74LS471	60	30	100	0°C to +70°C
4096	512 x 8 OC	20	DM54S473	75	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473	60	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472	75	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472	60	30	155	0°C to +70°C
	512 x 8 OC	20	DM54S473A	60	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472A	60	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472B	50	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472B	35	25	155	0°C to +70°C
	512 x 8 OC	24	DM54S475	75	40	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475	65	35	170	0°C to +70°C
	512 x 8 TS	24	DM54S474	75	40	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474	65	35	170	0°C to +70°C
	512 x 8 OC	24	DM54S475A	60	35	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474A	60	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474B	50	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474B	35	25	170	0°C to +70°C
	1024 x 4 OC	18	DM54S572	75	45	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572	60	35	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573	75	45	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573	60	35	140	0°C to +70°C
	1024 x 4 OC	18	DM54S572A	60	35	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573A	60	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573B	50	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573B	35	25	140	0°C to +70°C

Non-Registered PROMs (Continued)

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
8192	1024 x 8 TS	24	93Z451	40	30	135	0°C to +70°C
	1024 x 8 OC	24	DM77S180	75	35	170	−55°C to +125°C
	1024 x 8 OC	24*	DM77S280	75	35	170	−55°C to +125°C
	1024 x 8 OC	24	DM87S180	55	30	170	0°C to +70°C
	1024 x 8 OC	24*	DM87S280	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181	75	35	170	−55°C to +125°C
	1024 x 8 TS	24*	DM77S281	75	35	170	−55°C to +70°C
	1024 x 8 TS	24	DM87S181	55	30	170	0°C to +70°C
	1024 x 8 TS	24*	DM87S281	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181A	65	35	170	−55°C to +125°C
	1024 x 8 TS	24	DM87S181A	45	30	170	0°C to +70°C
	2048 x 4 OC	18	DM77S184	70	30	140	−55°C to +125°C
	2048 x 4 OC	18	DM87S184	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185	70	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185A	60	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185A	45	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185B	50	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185B	35	25	140	0°C to +70°C
16384	2048 x 8 TS	24	93Z511	45	30	175	0°C to +70°C
	4096 x 4 TS	20	DM77S195A	60	35	170	−55°C to +125°C
	4096 x 4 TS	20	DM87S195A	45	25	170	0°C to +70°C
	4096 x 4 TS	20	DM77S195B	50	30	170	−55°C to +125°C
	4096 x 4 TS	20	DM87S195B	35	25	170	0°C to +70°C
65384	8192 x 8 TS	24	93Z665	30	20	180	0°C to +70°C
	8192 x 8 TS	24	93Z667	30	20	180	0°C to +70°C

*24-Pin Narrow Dual-In-Line Package

Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{SA} (Min) in ns	t_{PLH} (CLK) t_{PHL} (CLK) (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
4096	512 x 8 REG	24*	DM77SR474	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR474B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR474	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR474B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM77SR476	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR476B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR27	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR27B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR476	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR476B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR27	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR27B	35	20	185	0°C to +70°C
8192	1024 x 8 REG	24*	DM77SR181	50	30	175	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR181	40	20	175	0°C to +70°C
	1024 x 8 REG	24*	DM77SR183	45	30	185	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR183	40	25	185	0°C to +70°C
	1024 x 8 REG	24*	DM77SR183B	40	25	185	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR183B	35	20	185	0°C to +70°C
16384	2048 x 8 REG	24*	DM77SR191	25	15	190	−55°C to +125°C
	2048 x 8 REG	24*	DM87SR191	18	10	190	0°C to +70°C
	2048 x 8 REG	24*	DM77SR193	25	15	190	−55°C to +125°C
	2048 x 8 REG	24*	DM87SR193	18	10	190	0°C to +70°C

*24-Pin Narrow Dual-In-Line Package

National Semiconductor

PL87X288B
(32 x 8) 256-Bit TTL Logic PROMs

General Description

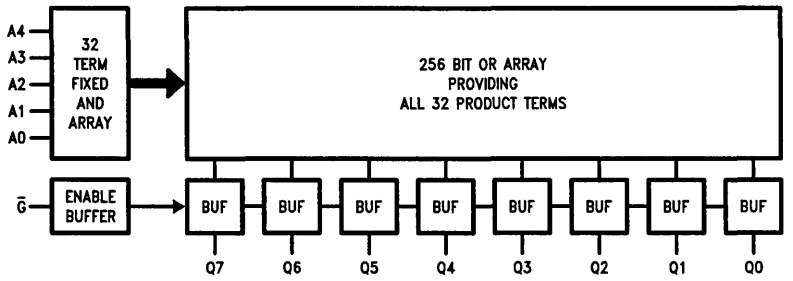
These Schottky programmable logic devices are organized in the popular 32 words by 8-bit configuration. An enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the OFF or high impedance state. The memories are available in the TRI-STATE® version only.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—15 ns max
  - Enable access—12 ns max
  - Enable recovery—12 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge
- TRI-STATE outputs

Block Diagram



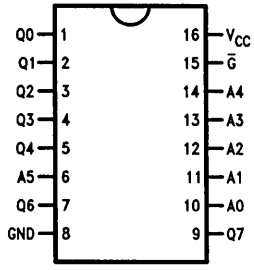
TL/D/6747–1

Pin Names

A0–A4	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

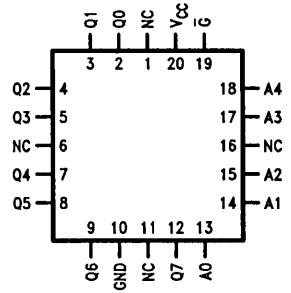


TL/D/6747–2

Top View

Order Number PL87X288BJ or PL87X288BN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/6747–9

Top View

Order Number PL87X288BV
See NS Package Number V20A

Ordering Information

Commercial Temperature Range
0°C to +70°C

Parameter/Order Number	Max Access Time (ns)
PL87X288BN	15
PL87X288BJ	15
PL87X288BV	15

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2 to +5.5V
Output Voltage (Note 2)	−0.5 to +5.5V
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) PL87X288B	4.75	5.25	V
Ambient Temperature (T_A) PL87X288B	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	PL87X288B			Units
			Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.4V		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA		0.35	0.50	V
V_{IL}	Low Level Input Voltage	(Note 7)			0.80	V
V_{IH}	High Level Input Voltage	(Note 7)	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−30		−130	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.4V to 2.4V Chip Disabled			100 −100	μA
V_{OH}	Output Voltage High	I_{OH} = −3.2 mA	2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: C_L = 50 pF.

Note 6: C_L = 5 pF.

Note 7: These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with standard load and operating conditions

Symbol	Parameter	JEDEC Symbol	PL87X288B			Units
			Min	Typ	Max	
t_{AA}	Address Access Time (Note 5)	TAVQV		10	15	ns
t_{EA}	Enable Access Time (Note 5)	TEVQV		8	12	ns
t_{ER}	Enable Recovery Time (Note 6)	TEXQX		8	12	ns
t_{ZX}	Output Enable Time (Note 5)	TEVQX		8	12	ns
t_{XZ}	Output Disable Time (Note 6)	TEXQZ		8	12	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S188
(32 x 8) 256-Bit TTL PROM

General Description

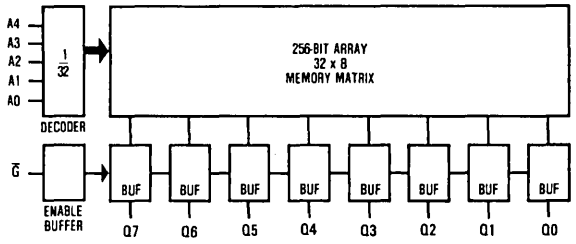
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—25 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9187–1

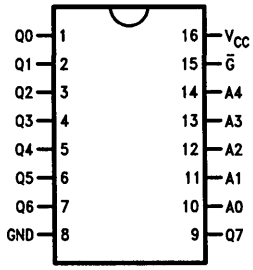
Pin Names

A0–A4	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

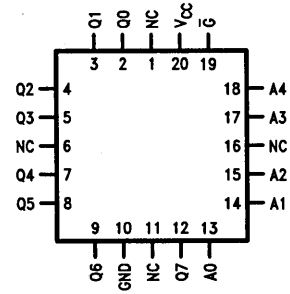


TL/D/9187-2

Top View

Order Number DM54/74S188J, 188AJ, DM74S188N or 188AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9187-3

Top View

Order Number DM74S188V or 188AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S188N	35
DM74S188J	35
DM74S188V	35
DM74S188AN	25
DM74S188AJ	25
DM74S188AV	25

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S188J	45
DM54S188AJ	35

Absolute Maximun Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S188			DM74S188			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110		70	110	mA

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S188			DM74S188A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	35		17	25	ns
TEA	TEVQV	Enable Access Time		15	20		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	20		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

AC Electrical Characteristics with Standard Load and Operating Conditions (Continued)

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S188			DM54S188A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	45		17	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S288 (32 x 8) 256-Bit TTL PROM

General Description

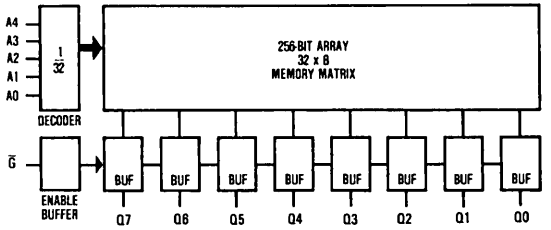
This Schottky memory is organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—25 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram



TL/D/8360–1

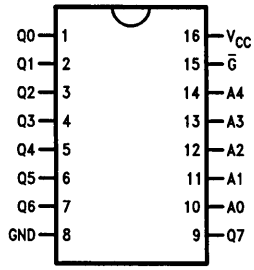
Pin Names

A0–A4	Addresses
$\overline{G}$	Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

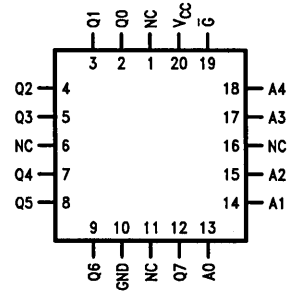


TL/D/8360–2

Top View

Order Number DM54/74S288J, 288AJ or DM74S288N, 288AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8360–7

Top View

Order Number DM74S288V or 288AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S288N	35
DM74S288J	35
DM74S288V	35
DM74S288AN	25
DM74S288AJ	25
DM74S288AV	25

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S288J	45
DM54S288AJ	35

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S288			DM74S288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110		70	110	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMPERATURE RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S288			DM74S288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		22	35		17	25	ns
TEA	Enable Access Time	TEVQV		15	20		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

MILITARY TEMPERATURE RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S288			DM54S288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	45		17	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQZ	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S287
(256 x 4) 1024-Bit TTL PROM

General Description

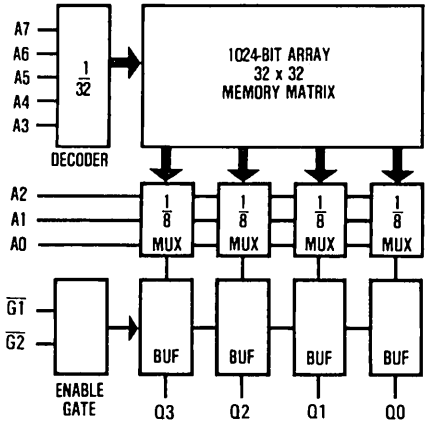
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge
- TRI-STATE® outputs

Block Diagram



TL/D/8359–1

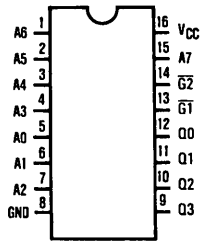
Pin Names

A0–A7	Addresses
$\overline{G1}$, $\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line-Package

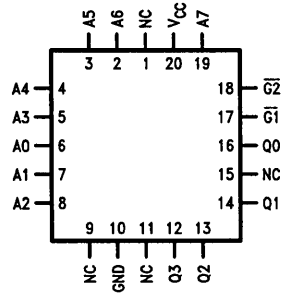


TL/D/8359-2

Top View

Order Number DM54/74S287J, 287AJ, DM74S287N or 287AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8359-7

Top View

Order Number DM74S287V or 287AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S287AJ	30
DM74S287J	50
DM74S287AN	30
DM74S287N	50
DM74S287AV	30
DM74S287V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S287AJ	40
DM54S287J	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S287			DM74S287			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S287			DM74S287A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	50		20	30	ns
TEA	TEVQV	Enable Access Time		15	25		15	20	ns
TER	TEXQX	Enable Recovery Time		15	25		15	20	ns
TZX	TEVQX	Output Enable Time		15	25		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	20	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S287			DM54S287A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	60		20	40	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S387
(256 x 4) 1024-Bit TTL PROM

General Description

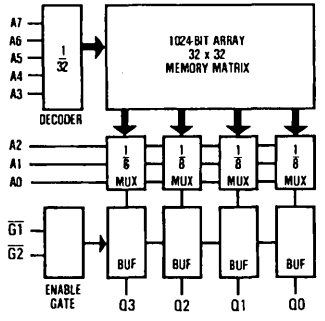
This Schottky memory is organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 30 ns max
  - Enable access—20 ns max
  - Enable recovery—20 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9188-1

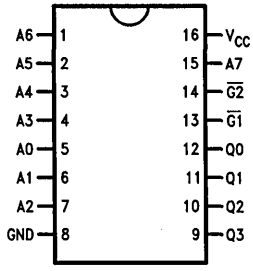
Pin Names

A0–A7	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

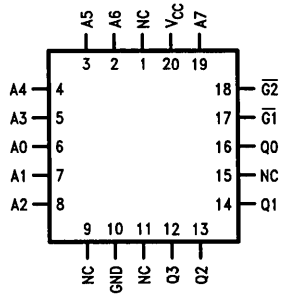


TL/D/9188-2

Top View

Order Number DM54/74S387J, 387AJ, DM74S387N, 387AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9188-3

Top View

Order Number DM74S387V, 387AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S387AJ	30
DM74S387J	50
DM74S387AN	30
DM74S387N	50
DM74S387AV	30
DM74S387V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S387AJ	40
DM54S387J	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to + 7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD	>2000V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S387			DM74S387			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	Parameter	JEDEC Symbol	DM74S387			DM74S387A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	50		20	30	ns
TEA	Enable Access Time	TEVQV		15	25		15	20	ns
TER	Enable Recovery Time	TEXQX		15	25		15	20	ns
TZX	Output Enable Time	TEVQX		15	25		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	25		15	20	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	Parameter	JEDEC Symbol	DM54S387			DM54S387A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	60		20	40	ns
TEA	Enable Access Time	TEVQV		15	30		15	30	ns
TER	Enable Recovery Time	TEXQX		15	30		15	30	ns
TZX	Output Enable Time	TEVQX		15	30		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

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National Semiconductor

DM54/74LS471
(256 x 8) 2048-Bit TTL PROM

General Description

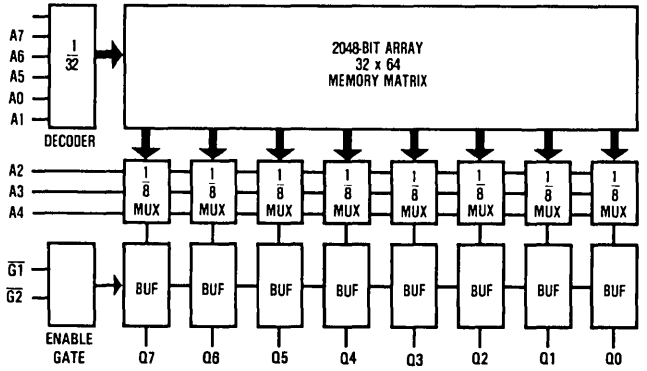
These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—60 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9190–1

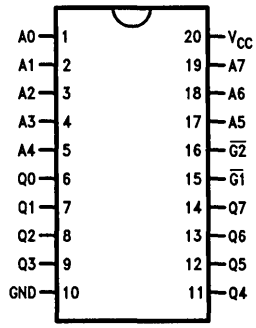
Pin Names

A0–A7	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

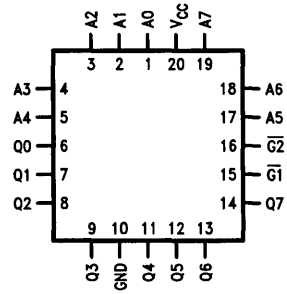


TL/D/9190-2

Top View

Order Number DM54/74LS471J or DM74LS471N
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9190-3

Top View

Order Number DM74LS471V
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74LS471N	60
DM74LS471J	60
DM74LS471V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54LS471J	70

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		75	100		75	100	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0v and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		45	70		40	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S472
(512 x 8) 4096-Bit TTL PROM

General Description

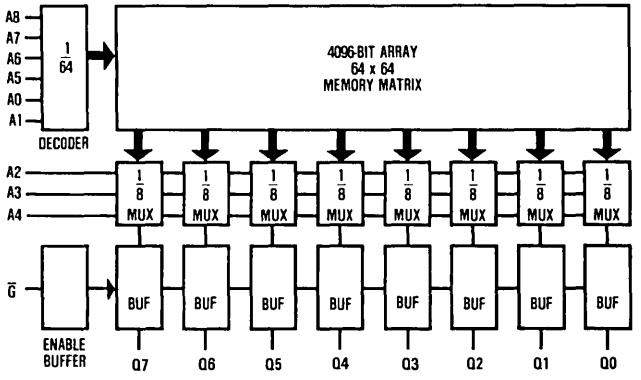
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9191–1

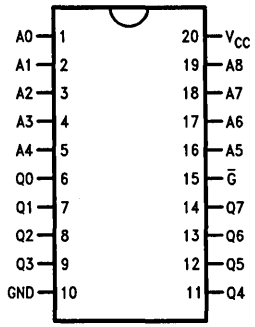
Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

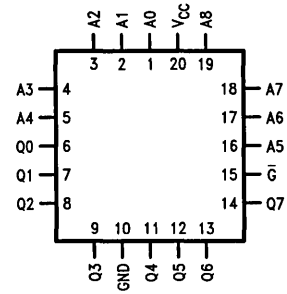


TL/D/9191-2

Top View

Order Number DM54/74S472J, 472AJ, 472BJ
DM74S472N, 472AN, 472BN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9191-3

Top View

Order Number DM74S472V, 472AV, 472BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S472AN	45
DM74S472BN	35
DM74S472N	60
DM74S472AJ	45
DM74S472BJ	35
DM74S472J	60
DM74S472AV	45
DM74S472BV	35
DM74S472V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S472AJ	60
DM54S472BJ	50
DM54S472J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S472			DM74S472			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155		110	155	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S472			DM74S472A			DM74S472B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S472			DM54S472A			DM54S472B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		15	35		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54S473/DM74S473
(512 x 8) 4096-Bit TTL PROM

General Description

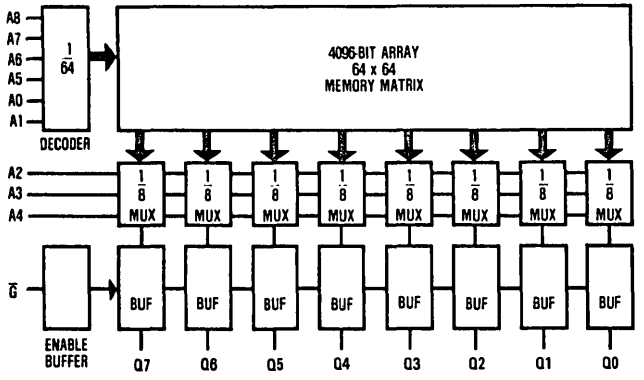
This Schottky memory is organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9715–1

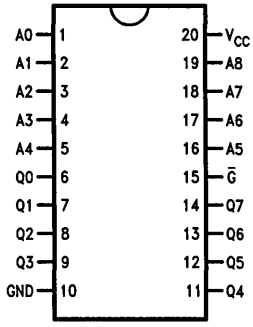
Pin Names

A0–A8	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

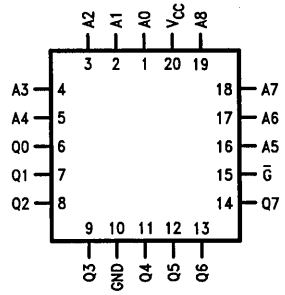


TL/D/9715-2

Top View

Order Number DM54/74S473J, 473AJ, DM74S473N or 473AN
See NS Package Number J20A or N20A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9715-3

Top View

Order Number DM74S473V or 473AV
See NS Package Number V20A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S473AN	45
DM74S473N	60
DM74S473AJ	45
DM74S473J	60
DM74S473AV	45
DM74S473V	60

Military Temp. Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S473AJ	60
DM54S473J	75

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S473			DM74S473			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155		110	155	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP. RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S473			DM74S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

MILITARY TEMP. RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S473			DM54S473A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanuim-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S474
(512 x 8) 4096-Bit TTL PROM

General Description

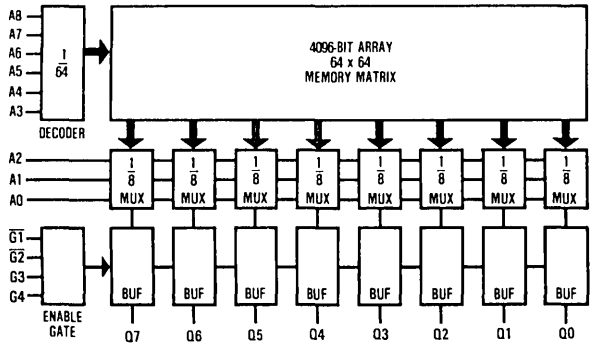
This Schottky memory is organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9714–1

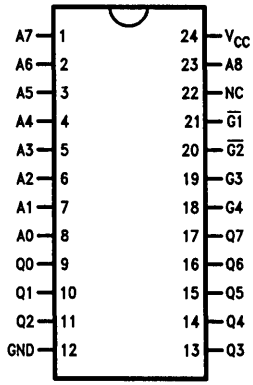
Pin Names

A0–A8	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
NC	No Connection
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

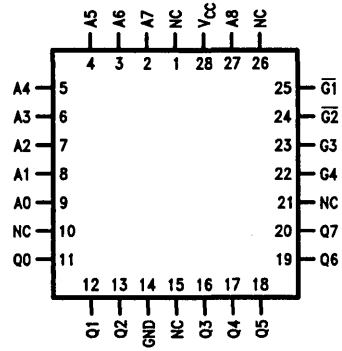


TL/D/9714-2

Top View

Order Number DM54/74S474J, 474AJ, 474BJ, DM74S474N, 474AN, 474BN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9714-3

Top View

Order Number DM74S474V, 474AV, 474BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S474AJ	45
DM74S474BJ	35
DM74S474J	65
DM74S474AN	45
DM74S474BN	35
DM74S474N	65
DM74S474AV	45
DM74S474BV	35
DM74S474V	65

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S474AJ	60
DM54S474BJ	50
DM54S474J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S474			DM74S474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S474			DM74S474A			DM74S474B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		20	35		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	35		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	35		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S474			DM54S474A			DM54S474B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		20	40		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	40		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	40		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	40		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S475 (512 x 8) 4096-Bit TTL PROM

General Description

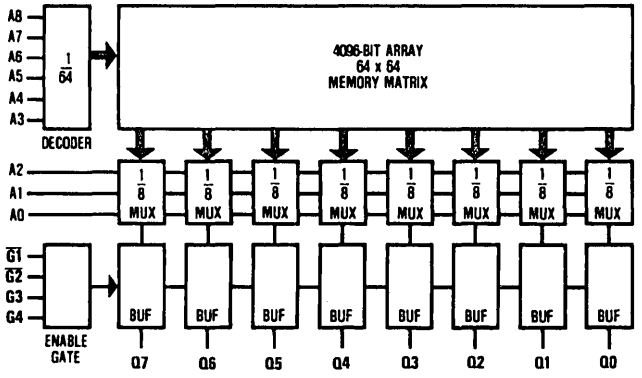
This Schottky memory is organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9192–1

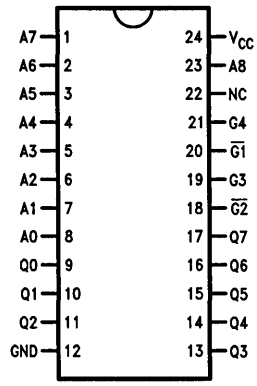
Pin Names

A0–A8	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
NC	No Connection
Q_0–Q_7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line-Package

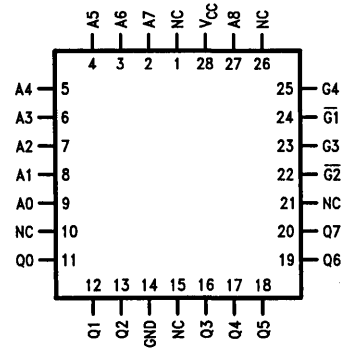


TL/D/9192-2

Top View

Order Number DM54/74S475J, 475AJ, DM74S475N or 475AN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9192-3

Top View

Order Number DM74S475V or 475AV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S475AJ	45
DM74S475J	65
DM74S475AN	45
DM74S475N	65
DM74S475AV	45
DM74S475V	65

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S475AJ	60
DM54S475J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S475			DM74S475			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V, T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded, All Outputs Open		115	170		115	170	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S475			DM74S475A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	65		25	45	ns
T_{EA}	TEVQV	Enable Access Time		20	35		15	25	ns
T_{ER}	TEXQX	Enable Recovery Time		20	35		15	25	ns
T_{ZX}	TEVQX	Output Enable Time		20	35		15	25	ns
T_{XZ}	TEXQZ	Output Disable Time		20	35		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S475			DM54S475A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	75		25	60	ns
T_{EA}	TEVQV	Enable Access Time		20	40		15	35	ns
T_{ER}	TEXQX	Enable Recovery Time		20	40		15	35	ns
T_{ZX}	TEVQX	Output Enable Time		20	40		15	35	ns
T_{XZ}	TEXQZ	Output Disable Time		20	40		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti:W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti:W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti:W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S570
(512 x 4) 2048-Bit TTL PROM

General Description

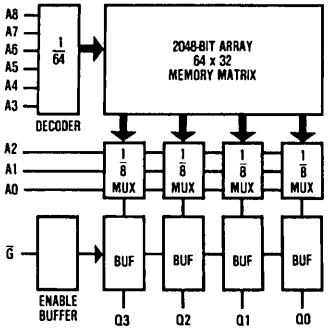
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9189–1

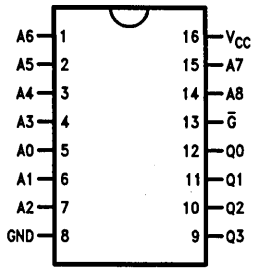
Pin Names

A0–A8	Addresses
$\overline{G}$	Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

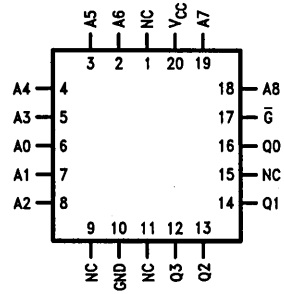


TL/D/9189-2

Top View

Order Number DM54/74S570J, 570AJ
DM74S570N, 570AN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9189-3

Top View

Order Number DM74S570V, 570AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S570AN	45
DM74S570N	55
DM74S570AJ	45
DM74S570J	55
DM74S570AV	45
DM74S570V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S570AJ	60
DM54S570J	65

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S570			DM74S570			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130		90	130	mA

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S570			DM74S570A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45	ns
TEA	TEVQV	Enable Access Time		20	30		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S570			DM54S570A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		30	60	ns
TEA	TEVQV	Enable Access Time		20	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S571
(512 x 4) 2048-Bit TTL PROM

General Description

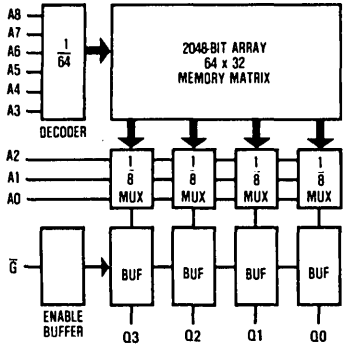
This Schottky memory is organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access down to—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9713–1

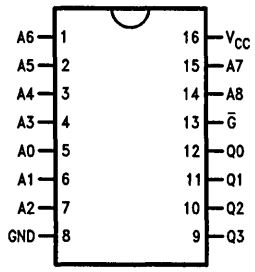
Pin Names

A0–A8	Address
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

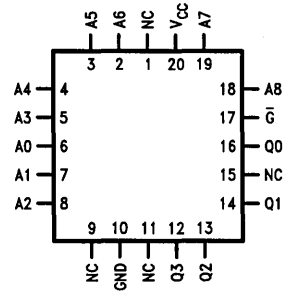


TL/D/9713-2

Top View

Order Number
DM54/74S571J, 571AJ, 571BJ
DM74S571N, 571AN, 571BN
See NS Package Number J16A or N16A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9713-3

Top View

Order Number
DM74S571V, 571AV, 571BV
See NS Package Number V20A

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S571AN	45
DM74S571BN	35
DM74S571N	55
DM74S571AJ	45
DM74S571BJ	35
DM74S571J	55
DM74S571AV	45
DM74S571BV	35
DM74S571V	55

Military Temp. Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S571AJ	60
DM54S571BJ	50
DM54S571J	65

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering 10 sec.)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S571			DM74S571			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130		90	130	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S571			DM74S571A			DM74S571B			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45		30	35	ns
TEA	TEVQV	Enable Access Time		20	30		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	30		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	30		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	30		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S571			DM54S571A			DM54S571B			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		30	60		30	50	ns
TEA	TEVQV	Enable Access Time		20	35		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	35		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	35		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S572
(1024 x 4) 4096-Bit TTL PROM

General Description

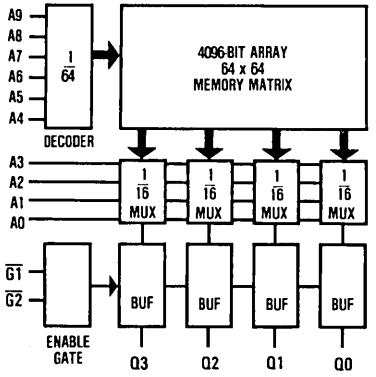
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open collector outputs

Block Diagram



TL/D/9712–1

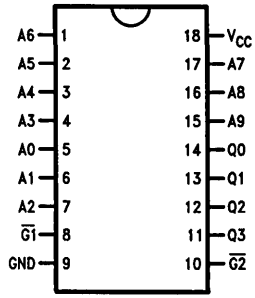
Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line-Package

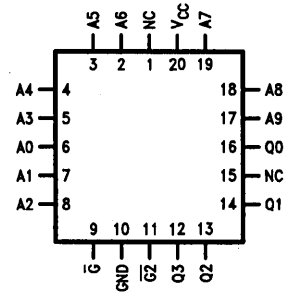


TL/D/9712-2

Top View

Order Number DM54/74S572J, 572AJ, DM74S572N, 572AN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9712-3

Top View

Order Number DM74S572V, 572AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S572AJ	45
DM74S572J	60
DM74S572AN	45
DM74S572N	60
DM74S572AV	45
DM74S572V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S572AJ	60
DM54S572J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S572			DM74S572			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S572			DM74S572A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	60		25	45	ns
T_{EA}	TEVQV	Enable Access Time		20	35		15	25	ns
T_{ER}	TEXQX	Enable Recovery Time		20	35		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S572			DM54S572A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	75		25	60	ns
T_{EA}	TEVQV	Enable Access Time		20	45		15	35	ns
T_{ER}	TEXQX	Enable Recovery Time		20	45		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM54/74S573
(1024 x 4) 4096-Bit TTL PROM

General Description

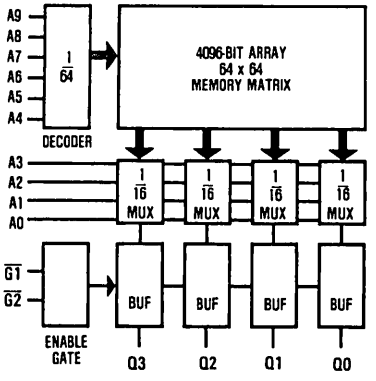
This Schottky memory is organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—down to 35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® Outputs

Block Diagram



TL/D/9193–1

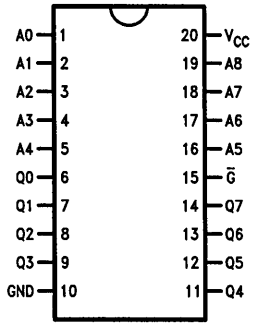
Pin Names

A0–A9	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

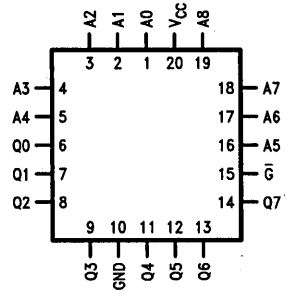


TL/D/9193-2

Top View

Order Number
DM54/74S573J, 573AJ, 573BJ
DM74S573N, 573AN, 573BN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9193-3

Top View

Order Number
DM74S573V, 573AV, 573BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM74S573AJ	45
DM74S573BJ	35
DM74S573J	60
DM74S573AN	45
DM74S573BN	35
DM74S573N	60
DM74S573AV	45
DM74S573BV	35
DM74S573V	60

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM54S573AJ	60
DM54S573BJ	50
DM54S573J	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S573			DM74S573			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM74S573			DM74S573A			DM74S573B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	60		25	45		25	35	ns
TEA	TEVQV	Enable Access Time		20	35		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		20	35		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		20	35		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		20	35		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM54S573			DM54S573A			DM54S573B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		25	60		25	50	ns
TEA	TEVQV	Enable Access Time		20	45		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		20	45		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		20	45		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		20	45		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S180, DM77/87S280 (1024 x 8) 8192-Bit TTL PROMs

General Description

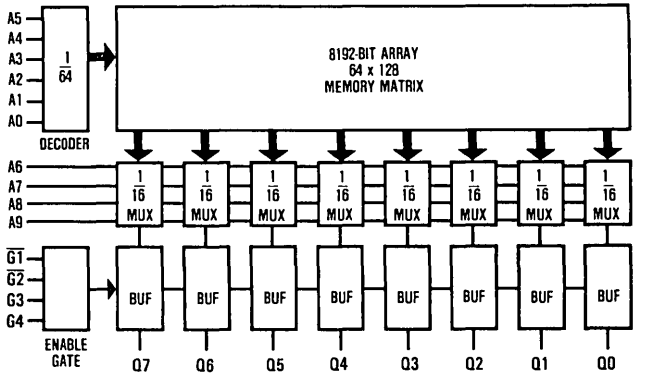
These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—55 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9716–1

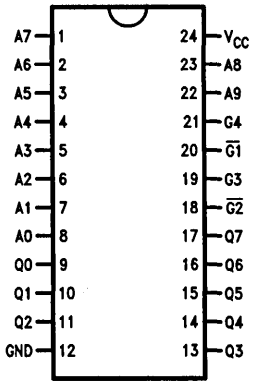
Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line-Package

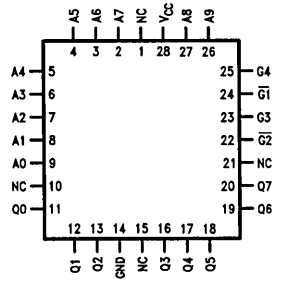


TL/D/9716-2

Top View

Order Number DM77/87S180J, 280J
DM87S180N, 280N
See NS Package Number J24A, J24F, N24A or N24C

Plastic Leaded Chip Carrier (PLCC)



TL/D/9716-3

Top View

Order Number DM87S180V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM87S180J	X		55
DM87S180N	X		55
DM87S180V	X		55
DM87S280J		X	55
DM87S280N		X	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM77S180J	X		75
DM77S280J		X	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S180 DM77S280			DM87S180 DM87S280			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		115	170		115	170	mA

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S180 DM87S280			Units
			Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55	ns
TEA	TEVQV	Enable Access Time		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S180 DM77S280			Units
			Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75	ns
TEA	TEVQV	Enable Access Time		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S181, DM77/87S281 (1024 x 8) 8192-Bit TTL PROMs

General Description

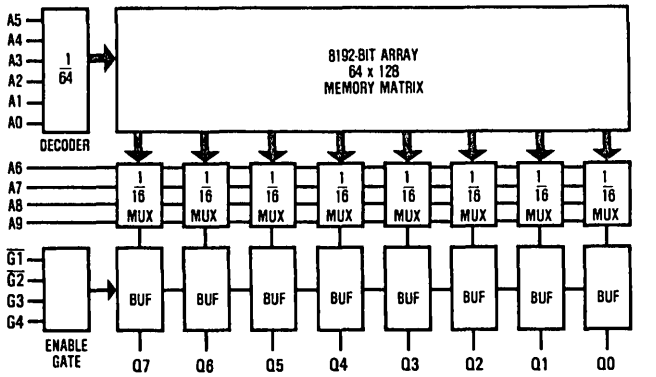
These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45 ns max
  - Enable access—30 ns max
  - Enable recovery—30 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9194–1

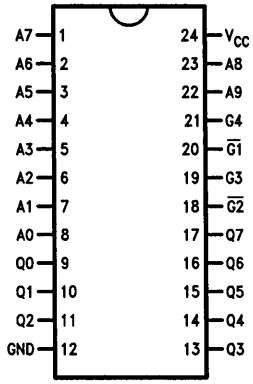
Pin Names

A0–A9	Addresses
$\overline{G1}$, $\overline{G2}$, G3, G4	Output Enables
GND	Ground
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

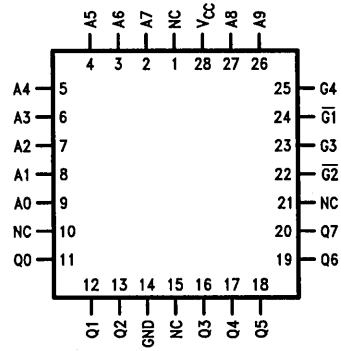


TL/D/9194-2

Top View

Order Number DM77/87S181J, 281J, 181AJ, 281AJ, DM87S181N, 281N, 181AN, 281AN
See NS Package Number J24A, J24F, N24A or N24C

Plastic Leaded Chip Carrier (PLCC)



TL/D/9194-3

Top View

Order Number DM87S181V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM87S181AJ	X		45
DM87S181J	X		55
DM87S181AN	X		45
DM87S181N	X		55
DM87S181V	X		55
DM87S281AJ		X	45
DM87S281J		X	55
DM87S281AN		X	45
DM87S281N		X	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	24-Pin Standard DIP	24-Pin Narrow DIP	Max Access Time (ns)
DM77S181AJ	X		65
DM77S181J	X		75
DM77S281AJ		X	65
DM77S281J		X	75

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S181 DM77S281			DM87S181 DM87S281			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		115	170		115	170	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

4

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S181 DM87S281			DM87S181A DM87S281A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		35	45	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S181 DM77S281			DM77S181A DM77S281A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		35	65	ns
TEA	TEVQV	Enable Access Time		15	35		15	35	ns
TER	TEXQX	Enable Recovery Time		15	35		15	35	ns
TZX	TEVQX	Output Enable Time		15	35		15	35	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	35	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S184
(2048 x 4) 8192-Bit TTL PROM

General Description

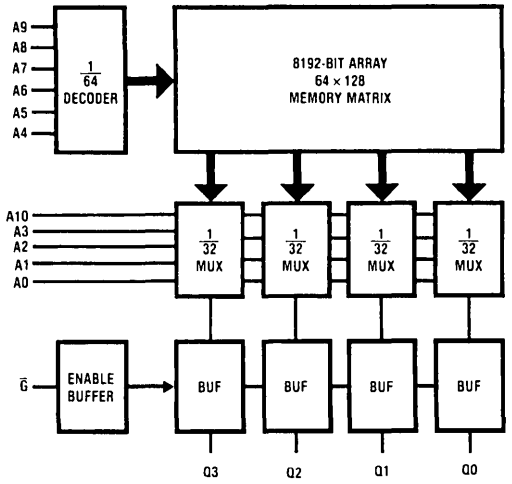
This Schottky memory is organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—55 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Open-collector outputs

Block Diagram



TL/D/9717–1

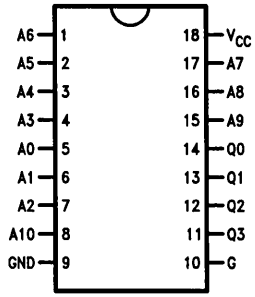
Pin Names

A0–A10	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

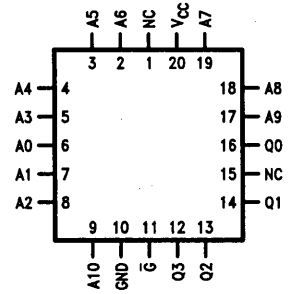


TL/D/9717-2

Top View

Order Number DM77/87S184J, 184AJ or DM87S184N, 184AN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9717-3

Top View

Order Number DM87S184V, 184AV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Acces Time (ns)
DM87S184AN	45
DM87S184N	55
DM87S184AJ	45
DM87S184J	55
DM87S184AV	45
DM87S184V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Acces Time (ns)
DM77S184J	70
DM77S184AJ	60

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S184			DM87S184			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			26			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S184			DM87S184A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45	ns
TEA	TEVQV	Enable Access Time		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S184			DM77S184A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		30	60	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S185
(2048 x 4) 8192-Bit TTL PROM

General Description

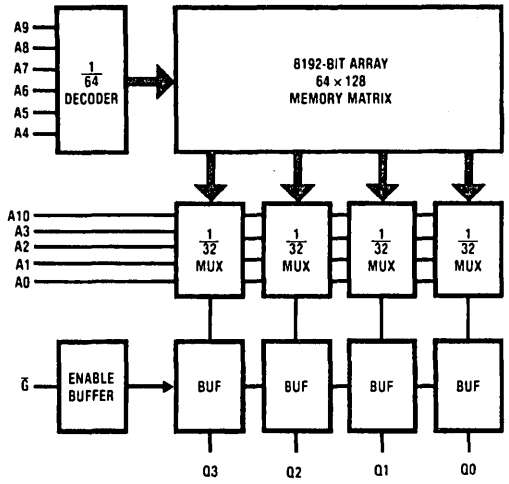
This Schottky memory is organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max
  - Enable access—25 ns max
  - Enable recovery—25 ns max
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE® outputs

Block Diagram



TL/D/9197–1

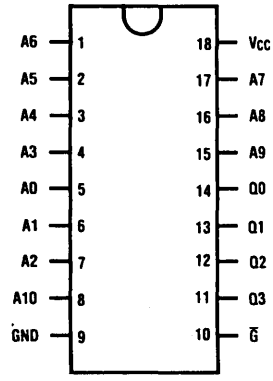
Pin Names

A0–A10	Addresses
$\overline{G}$	Output Enable
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line-Package

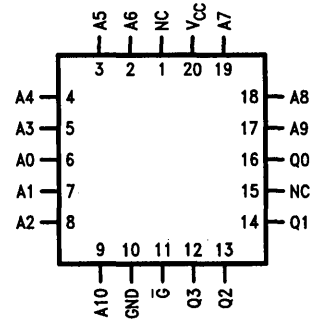


TL/D/9197-2

Top View

Order Number DM77/87S185J, 185AJ, 185BJ
DM87S185N, 185AN, 185BN
See NS Package Number J18A or N18A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9197-3

Top View

Order Number DM87S185V, 185AV, 185BV
See NS Package Number V20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM87S185AJ	45
DM87S185BJ	35
DM87S185J	55
DM87S185AN	45
DM87S185BN	35
DM87S185N	55
DM87S185AV	45
DM87S185BV	35
DM87S185V	55

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM77S185AJ	60
DM77S185BJ	50
DM77S185J	70

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S185			DM87S185			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S185			DM87S185A			DM87S185B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	55		30	45		25	35	ns
TEA	TEVQV	Enable Access Time		15	25		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		15	25		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		15	25		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S185			DM77S185A			DM77S185B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		30	60		25	50	ns
TEA	TEVQV	Enable Access Time		15	30		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87S195
(4096 x 4) 16,384-Bit TTL PROM

General Description

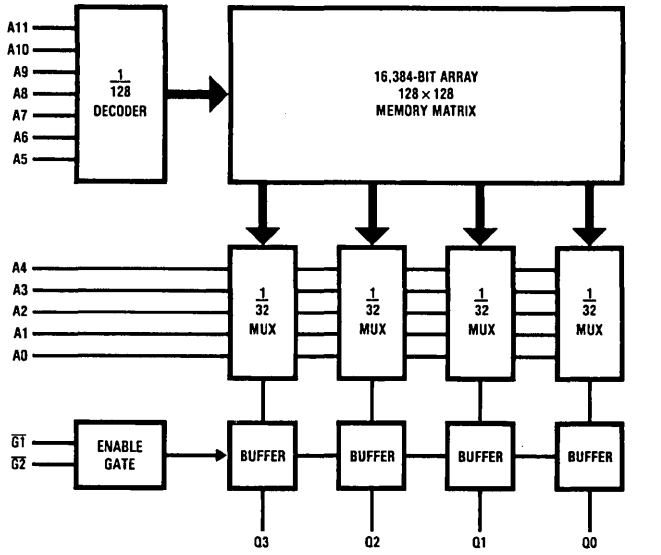
These Schottky memories are organized in the popular 4096 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in TRI-STATE® version only.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced tungsten (W) fuse technology
- Schottky-clamped for high speed
  - Address access—35 ns max
  - Enable access—25 ns typ
  - Enable recovery—25 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- TRI-STATE outputs

Block Diagram



TL/D/9199–1

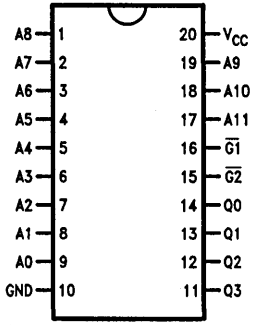
Pin Names

A0–A11	Addresses
$\overline{G1}$–$\overline{G2}$	Output Enables
GND	Ground
Q0–Q3	Outputs
V_{CC}	Power Supply

4

Connection Diagram

Dual-In-Line Package



TL/D/9199–2

Top View

Order Number DM77/87S195AJ, 195BJ
DM87S195AN, 195BN
See NS Package Number J20A or N20A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Max Access Time (ns)
DM87S195AJ	45
DM87S195BJ	35
DM87S195AN	45
DM87S195BN	35

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Max Access Time (ns)
DM77S195AJ	60
DM77S195BJ	50

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
ESD to be determined	

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S195A/B			DM87S195A/B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		120	170		120	170	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V			+50			+50	μA
		Chip Disabled			−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics with Standard Load and Operating Conditions

COMMERCIAL TEMP RANGE (0°C to +70°C)

Symbol	JEDEC Symbol	Parameter	DM87S195A			DM87S195B			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		30	45		30	35	ns
TEA	TEVQV	Enable Access Time		15	25		15	25	ns
TER	TEXQX	Enable Recovery Time		15	25		15	25	ns
TZX	TEVQX	Output Enable Time		15	25		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	25		15	25	ns

MILITARY TEMP RANGE (−55°C to +125°C)

Symbol	JEDEC Symbol	Parameter	DM77S195A			DM77S195B			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		30	60		30	50	ns
TEA	TEVQV	Enable Access Time		15	30		15	30	ns
TER	TEXQX	Enable Recovery Time		15	30		15	30	ns
TZX	TEVQX	Output Enable Time		15	30		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidty life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

93Z451 1024 x 8-Bit Programmable Read Only Memory

General Description

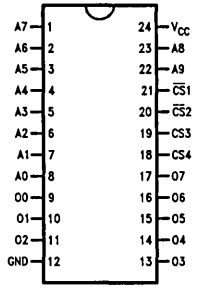
The 93Z451 is a fully decoded 8,192-bit Programmable Read Only Memory (PROM), organized 1024 words by eight bits per word. The 93Z451 is manufactured using highly reliable ISO-Z vertical fuse technology.

Features

- Available in 300 mil and 600 mil CERDIP, plastic DIP, LCC and flatpak
- Commercial address access time—40 ns Max
- Highly reliable vertical fuses ensure high programming yields
- Power up TRI-STATE® (93Z451) outputs
- Low current PNP inputs
- Complete AC/DC testability

Connection Diagrams

Dual-In-Line Package

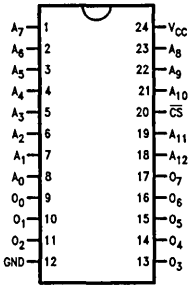


TL/D/9667-2

Top View

Order Number 93Z451AD, D, 93Z451AP, P, 93Z451ASD, SD See NS Package Number J24F*, J24A* or N24A*

Ceramic Flatpak

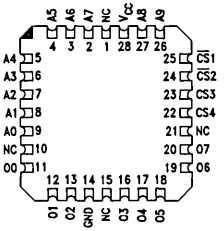


TL/D/9667-3

Top View

Order Number 93Z451AF, F See NS Package Number W24C*

Leadless Chip Carrier



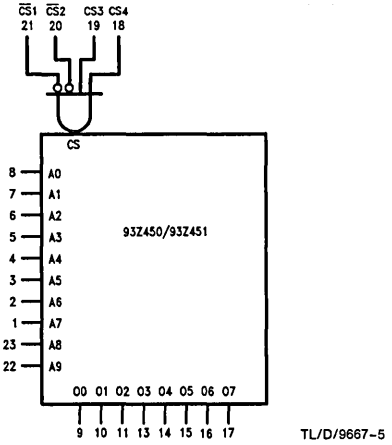
TL/D/9667-4

Top View

Order Number 93Z451AL, L See NS Package Number E28A*

*For most current package information, contact product marketing.

Logic Symbol



TL/D/9667-5

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	−1.5V to V_{CC}
Voltage Applied to Outputs (Output HIGH)	−1.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C
Ambient Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C

Recommended Operating Conditions

Ambient Operating Temperature	0°C to +70°C
Positive Supply Voltage	5.0V ±5%

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.45V		−10	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.4V to V_{CC}	−40		40	μA
I_{OHZ} I_{OLZ}	Output Leakage Current for High Impedance State	V_{OH} = 2.4V V_{OL} = 0.4V			40 −40	μA μA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_O = 0V, (Note 2) Address Any "1"	−20	−45	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded, Outputs Open		110	135	ma
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs	2.0			V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.2	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.30	0.45	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −2.0 mA Address Any "1"	2.4			V

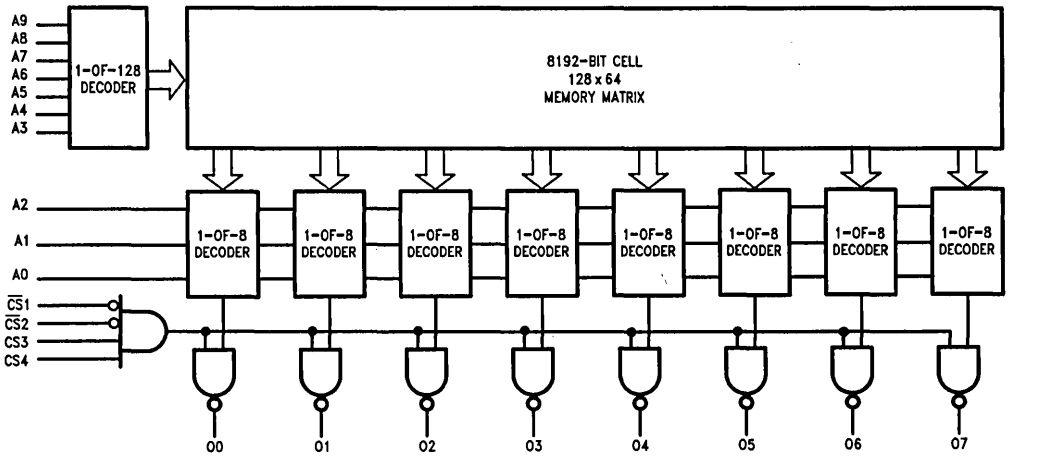
AC Electrical Characteristics V_{CC} = 5.0V ± 5%, GND = 0V, T_C = 0°C to +70°C

Symbol	Parameter	Conditions	'A'	Std	Units
t_{AA}	Address to Output Access Time	See AC Output Load	35	40	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load	25	30	ns

Note 1: Typical values are at V_{CC} = 5.0V, T_C = −25°C.

Note 2: Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Block Diagram



TL/D/9667–1

Pin Names

A0–A9	Address Inputs
$\overline{CS1}$, $\overline{CS2}$	Chip Select Inputs (Active LOW)
CS3, CS4	Chip Select Inputs (Active HIGH)
O0–O7	Data Outputs

Functional Description

The 93Z451 is a TTL bipolar field Programmable Read Only Memory (PROM) organized 1024 words by eight bits per word. The 93Z451 has TRI-STATE outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Four Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}1$ and $\overline{CS}2$ are LOW and CS3 and CS4 are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z451 uses open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic "0" state. Cells can be programmed to a logic "1" state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A0 through A9 and the chip is selected. Data is then available at the outputs after t_{AA}.

Programming

The 93Z451 is manufactured with all bits in the logic "0" state. Any desired bit (output) can be programmed to a logic "1" state by following the procedure shown below. One may build a programmer to satisfy the specifications or buy any of the commercially available programmers which meet these specifications.

Programming Sequence

The 93Z451 is programmed using the following method:

1. Address the word to be programmed by applying the appropriate voltages to address pins A0 through A9. Select the PROM by applying a LOW to $\overline{CS}1$ and $\overline{CS}2$ and a HIGH to CS3 and CS4.
2. Apply the proper power for a High V_{CC} read. V_{CC} = 6.5V, GND = 0V.
3. Read the output to be programmed and verify it is in the unprogrammed logic "0" state.
4. Enable the chip for programming by application of the Chip Select Programming Voltage (V_{CSP} = 20.0V) to $\overline{CS}2$. $\overline{CS}1$ should remain LOW and CS3 and CS4 HIGH.
5. a. To program the bit apply I_{OP}, the programming current ramp to the output.

   Note: Only one output may be programmed at a time. The other outputs must be left open.

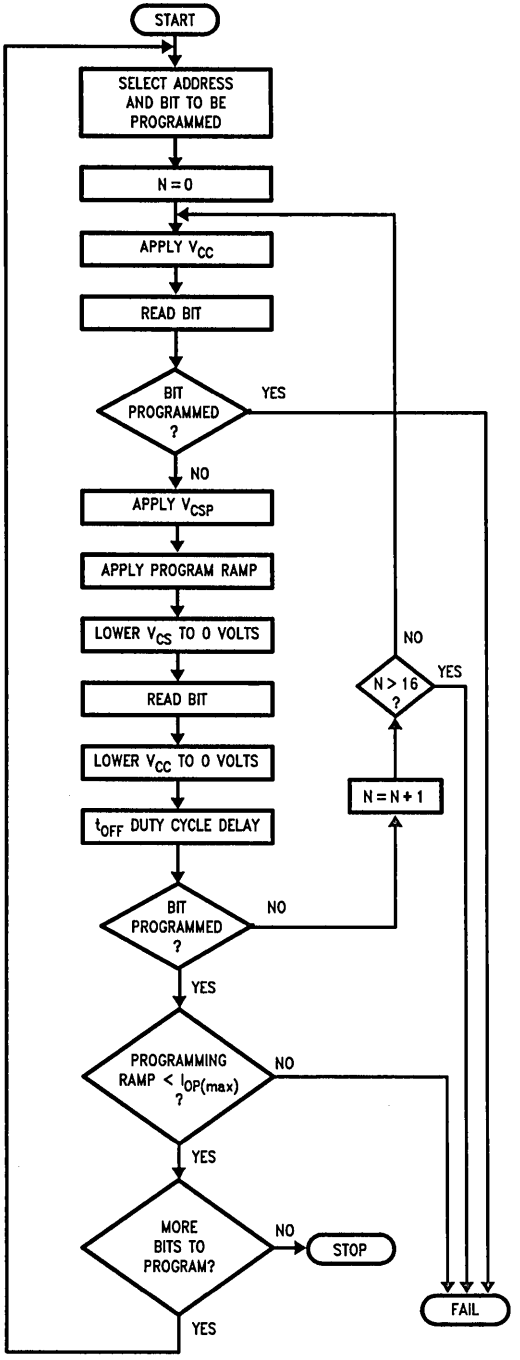
   b. During the rise of the current ramp, a drop in voltage (V_{ps}) at the output may be sensed. This indicates that the current needed to program the junction has been reached and the bit has programmed.

   c. Upon detection of the voltage drop (V_{ps}), the current ramp should be held at a constant current for a time (t_{hAP}) and then shut off.
6. Once the current ramp has been shut off, lower V_{CSP} to 0V and read the output.
7. Lower V_{CC} to 0V. The power supply duty cycle must be less than or equal to 50%.
8. If the read performed in step 6 indicates that the bit has not programmed then go to step 1 and repeat the programming sequence (up to a maximum of 16 attempts total).
9. If the read performed in step 6 indicates that the bit has programmed then one of the two following conditions exist:

   a. If the required programming current was less than $I_{OP(max)}$ then go to step 10.

   b. If the required programming current was equal to $I_{OP(max)}$ then the device is considered a failure and no future attempts at programming should be made.
10. Repeat the above procedure from step 1 until all the desired bits in the memory have been programmed.

Programming Flow Chart



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Programming Specifications (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Power Supply Voltage	Typical I_{CC} at 6.5V = 250 mA	6.4	6.5	6.6	V
t_{rVCC}	Power Supply Rise Time (Note 3)		0.2	2.0		μs
t_{fVCC}	Power Supply Fall Time		0.2	2.0		μs
t_{ON}	V_{CC} On Time	See Programming Timing Diagram	(Note 1)			
t_{OFF}	V_{CC} Off Time	See Programming Timing Diagram	(Note 2)			
	Duty Cycle for V_{CC}	$t_{ON}/(t_{OFF} + t_{ON})$			50	%
READ STROBE						
t_{dRBP}	Read Delay before Programming	Initial Check		3.0		μs
t_w	Fuse Read Time			1.0		μs
t_{dVCC}	Delay to V_{CC} Off			1.0		μs
t_{dRAP}	Delay to Read after Programming	Verify		3.0		μs
CHIP SELECT						
V_{CSP}	Chip Select Programming Voltage		20.0	20.0	22.0	V
I_{CSP}	Chip Select Program Current Limit		175	180	185	mA
V_{IL}	Input Voltage LOW		0	0	0.4	V
V_{IH}	Input Voltage HIGH		2.4	5.0	5.0	V
t_{dCS}	Delay to Chip Deselect			1.0		μs
t_{rCS}	Chip Select Pulse Rise Time		3.0	4.0		μs
t_{dAP}	Delay to Chip Select Time		0.2	1.0		μs
t_{fCS}	Chip Select Pulse Fall Time		0.1	0.1	1.0	μs
CURRENT RAMP						
I_{OPLP}	Programming Current Linear Point	Point after Which the Programming Current Ramp Must Rise at a Linear Slew Rate		10	20	mA
$I_{OP(max)}$	Output Programming Current Limit	Apply Current Ramp to Selected Output	155	160	165	mA
$V_{OP(max)}$	Output Programming Voltage Limit		24	25	26	V
SR_{IOP}	Current Slew Rate	Constant after Linear Point	0.9	1.0	1.1	mA/μs
V_{PS}	Blow Sense Voltage		0.7			V
t_{dBP}	Delay to Programming Ramp	V_{CSP} Must Be at Minimum	2.0	3.0		
t_{LP}	Time to Reach Linear Point		0.2	1.0	10	μs
t_{SS}	Program Sense Inhibit		2.0	3.0	10	μs
t_{tp}	Time to Program Fuse		3.0		150	μs
t_{hAP}	Programming Ramp Hold Time	After Fuse Programs	1.4	1.5	1.6	μs
t_{flOP}	Program Ramp Fall Time			0.1	0.2	μs

Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

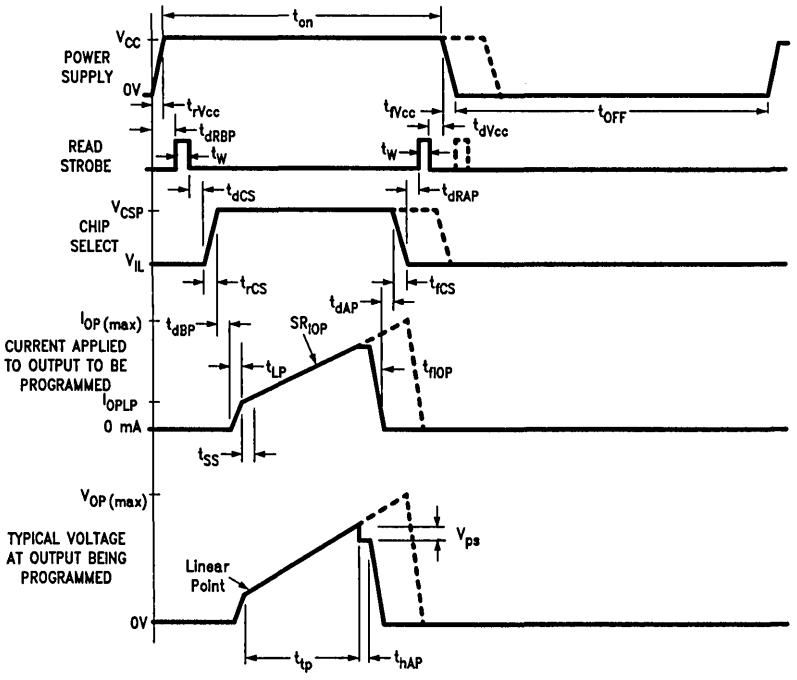
Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temp. T_A = 25°C ± 10°C

Timing Diagrams

Programming Timing Diagram



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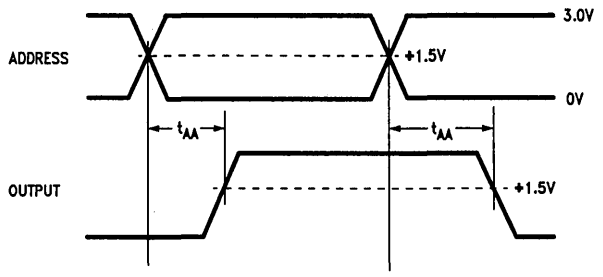
AC Waveforms



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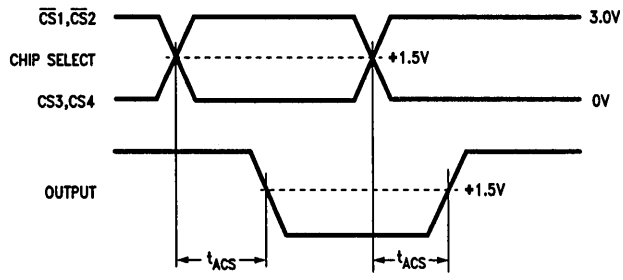
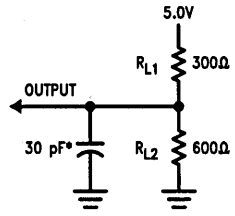
Timing Diagrams (Continued)

AC Waveforms (Continued)



TL/D/9667–9



TL/D/9667–10

*Includes jig and probe capacitance.

FIGURE 1. AC Test Output Load

Test Conditions

Input pulse: 0V to 3.0V.

Input pulse rise and fall times: 5 ns between 1V and 2V.

Measurements made at 1.5V level.

National Semiconductor

93Z511
2048 x 8-Bit Programmable Read Only Memory

General Description

The 93Z511 is a fully decoded 16,384-bit Programmable Read Only Memory (PROM), organized 2048 words by eight bits per word.

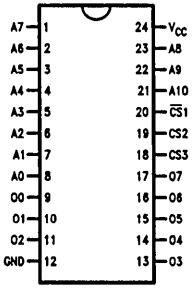
The 93Z511 is manufactured using highly reliable ISO-Z vertical fuse technology.

Features

- Available in 300 mil and 600 mil cerdip, plastic DIP, LCC and flatpak
- Commercial address access time—45 ns max
- Military address access time—55 ns max
- Highly reliable vertical fuses ensure high programming yields
- Power up TRI-STATE® (93Z511) outputs
- Low Current PNP inputs
- Complete AC/DC testability

Connection Diagrams

Dual-In-Line Package

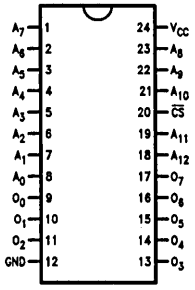


TL/D/9668-2

Top View

Order Number 93Z511D, 93Z511P or 93Z511SD
See NS Package Number J24F* or N24A*

Flatpak

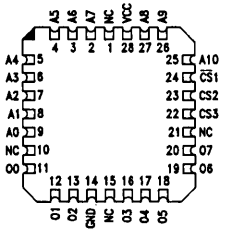


TL/D/9668-3

Top View

Order Number 93Z511F
See NS Package Number W24C*

Leadless Chip Carrier

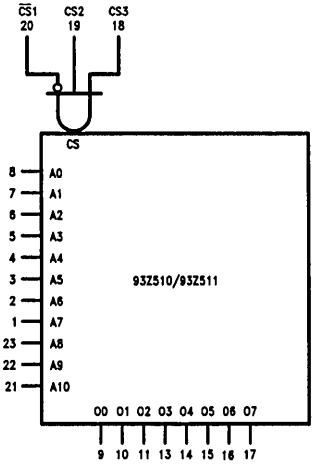


TL/D/9668-4

Order Number 93Z511L
See NS Package Number E28A*

*For most current package information, contact product marketing.

Logic Symbol

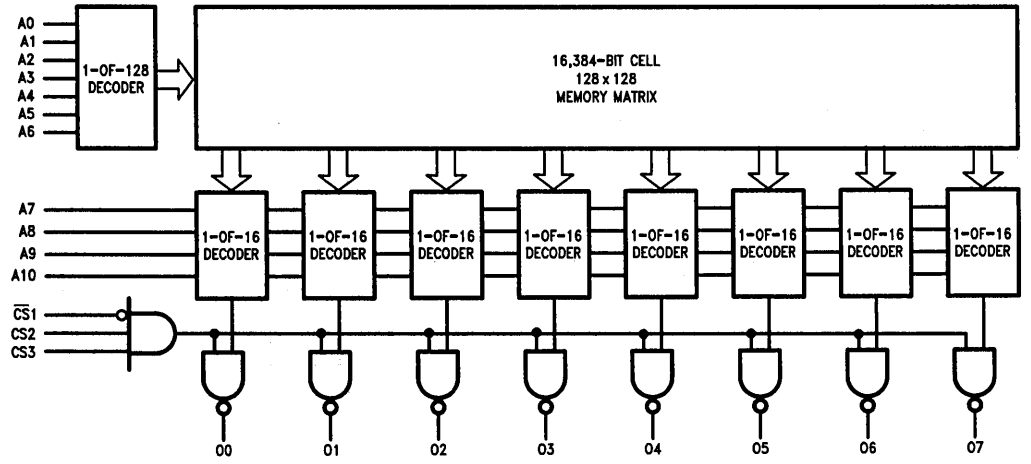


TL/D/9668-5

V_{CC} = Pin 24
GND = Pin 12

4

Block Diagram



TL/D/9668-1

Pin Names

A_0–A_{10}	Address Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2, CS_3	Chip Select Inputs (Active HIGH)
O_0–O_7	Data Outputs

Functional Description

The 93Z511 is a TTL bipolar field Programmable Read Only Memory (PROM) organized 2048 words by eight bits per word. The 93Z511 has TRI-STATE outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Three Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128k without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. The device is enabled only when $\overline{CS}_1$ is LOW and CS_2 and CS_3 are HIGH.

The device contains an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z511 uses open based vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic "0" state. Cells can be programmed to a logic "1" state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read junction is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_{10} and the chip is selected. Data is then available at the outputs after t_{AA}.

PROGRAMMING

The 93Z511 is manufactured with all bits in the logic "0" state. Any desired bit (output) can be programmed to a logic "1" state by following the procedure shown below. One may build a programmer to satisfy the specifications or buy any of the commercially available programmers which meet these specifications.

PROGRAMMING SEQUENCE

The 93Z511 is programmed using the following method.

1. Apply the proper power, V_{CC} = 6.5V, GND = 0V.
2. Select the word to be programmed by applying the appropriate voltages to the Address pins A_0 through A_9. Verify that the bit to be programmed is in the "0" logic state.
3. Enable the chip for programming by application of the Chip Select Voltage, $V_P(\overline{CS})$ = 20V, to $\overline{CS}_1$ (pin 20). CS_2 and CS_3 should be left HIGH.
4. Apply I_{OP} programming current ramp pulse for up to 140 μs to the output to be programmed. The other outputs must be left open. Only one output may be programmed at a time.
5. To verify the logic "1" in the bit just programmed after the programming current ramp pulse from the output has shut off, lower $V_P(\overline{CS})$ to 0V and sense the output.
6. If the bit is verified at V_{CC} = 6.5V as not having been programmed, then repeat the programming pulse sequence up to 15 times until the bit is programmed. If the bit does not program after 16 programming attempts, then the part fails.
7. If the bit is verified at V_{CC} = 6.5V as having been programmed, then one of two conditions exists:
   a. if the current pulse required was less than $t_{OP(MAX)}$, then go to the next bit;
   b. if the current pulse required was equal to $t_{OP(MAX)}$, then the part fails.
8. The above procedure is then repeated to program other bits on the chip.

DC Performance Characteristics: over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Conditions	Min	Typ (Note 1)	Max	Units
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_{IH}	Input HIGH Voltage	Guaranteed Input LOW Voltage for All Inputs	2.0			V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = − 18 mA			−1.2	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.30	0.45	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −2.0 mA Address Any "1"	2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.45V		−10	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.4V to V_{CC}	−40		40	μA
I_{OHZ} I_{OLZ}	Output Leakage Current for High Impedance State	V_{OH} = 2.4V V_{OL} = 0.4V			40 −40	μA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_O = 0V, (Note 2) Address Any "1"	−15	−35	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs GND All Outputs Open		120	175	mA

Commercial

AC Characteristics V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +70°C

Symbol	Characteristic	Conditions	Max	Units
t_{AA}	Address to Output Access Time	See AC Output Load	45	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load	30	ns

Military

AC Characteristics V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

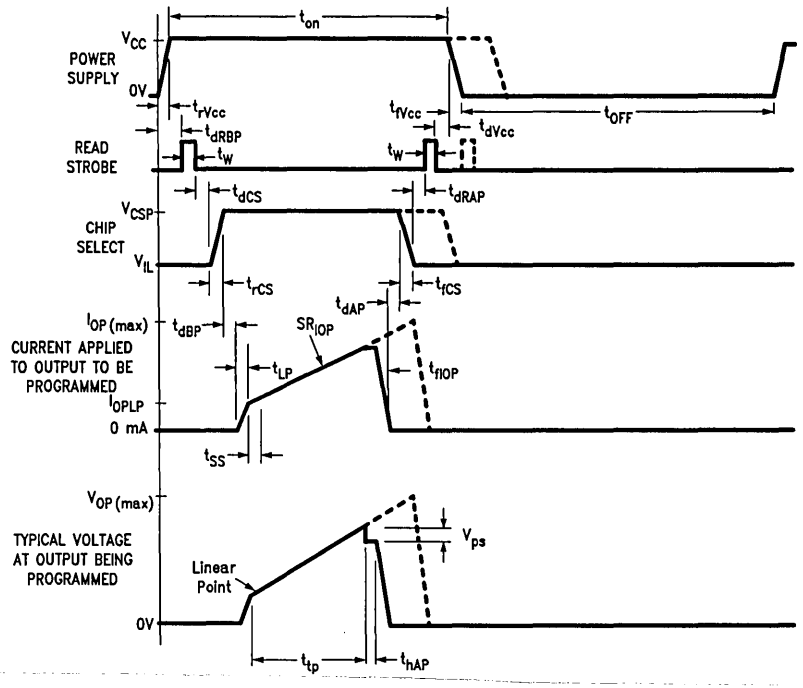
Symbol	Characteristic	Conditions	Max	Units
t_{AA}	Address to Output Access Time	See AC Test Output Load	55	ns
t_{ACS}	Chip Select to Output Access Time	See AC Test Output Load	35	ns

Note 1: Typical values are at V_{CC} = 5.0V, T_C = +25°C.

Note 2: Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Timing Diagrams

Programming Timing Diagram



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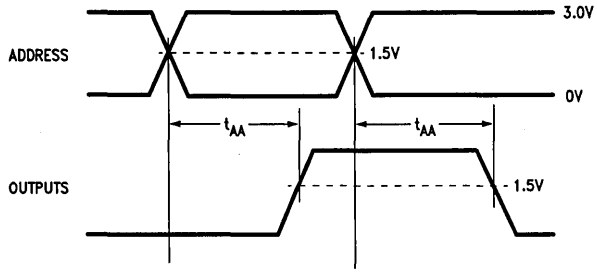
4

Timing Diagrams (Continued)

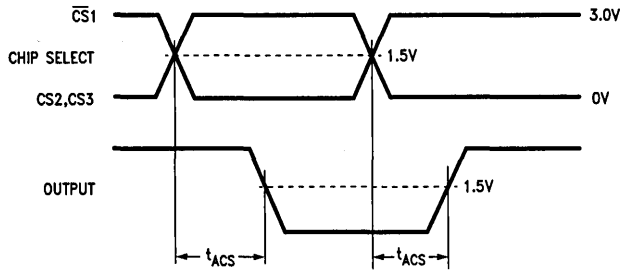
AC Waveforms

2a Propagation Delay from Address Inputs



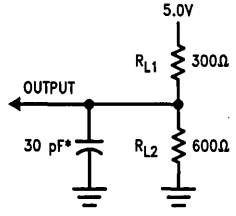
TL/D/9668-7

2b Propagation Delay from Chip Select



TL/D/9668-8

AC Test Output Load



TL/D/9668-9

*Includes jig and probe capacitance.

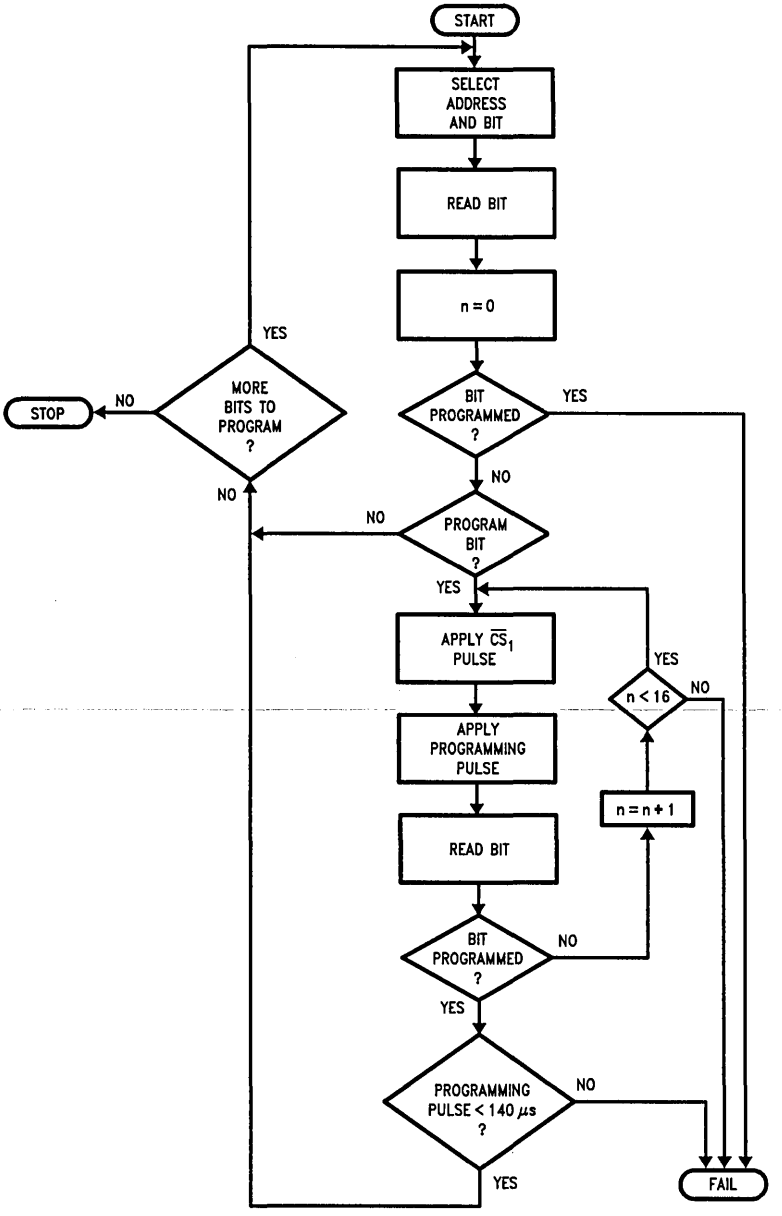
Test Conditions

Input Pulse 0V to 3.0V

Input Pulse Rise and Fall Times 5 ns Between 1V and 2V

Measurements made at 1.5V Level

Programming Flow Chart



TL/D/9668–10

Programming Specifications (Notes 1, 2, 3 and 4)

Symbol	Parameter	Min	Typ	Max	Units	Comments
POWER SUPPLY						
V_{CC}	Power Supply Voltage	6.4	6.5	6.6	V	Typical I_{CC} at 6.5V = 250 mA
t_rV_{CC}	Power Supply Rise Time (Note 3)	0.2	2.0		μs	
t_fV_{CC}	Power Supply Fall Time	0.2	2.0		μs	
t_{ON}	V_{CC} On Time	(Note 1)				See Programming Timing Diagram
t_{OFF}	V_{CC} Off Time	(Note 2)				
	Duty Cycle for V_{CC}			50	%	$t_{ON}/(t_{OFF} + t_{ON})$
READ STROBE						
t_{dRBP}	Read Delay before Programming		3.0		μs	Initial Check
t_W	Fuse Read Time		1.0		μs	
t_dV_{CC}	Delay to V_{CC} Off		1.0		μs	
t_{dRAP}	Delay to Read after Programming		3.0		μs	Verify
CHIP SELECT						
V_{CSP}	Chip Select Programming Voltage	20.0	20.0	20.0	V	
I_{CSP}	Chip Select Program Current Limit	175	180	185	mA	
V_{IL}	Input Voltage LOW	0	0	0.4	V	
V_{IH}	Input Voltage HIGH	2.4	5.0	5.0	V	
t_{dCS}	Delay to Chip Deselect		1.0		μs	
t_{rCS}	Chip Select Pulse Rise Time	3.0	4.0		μs	
t_{dAP}	Delay to Chip Select Time	0.2	1.0		μs	
t_{fCS}	Chip Select Pulse Fall Time	0.1	0.1	1.0	μs	
CURRENT RAMP						
I_{OPLP}	Programming Current Linear Point		10	20	mA	Point after which the programming current ramp must rise at a linear slew rate
$I_{OP(MAX)}$	Output Programming Current Limit	155	160	165	mA	Apply current ramp to selected output
$V_{OP(MAX)}$	Output Programming Voltage Limit	24	25	26	V	
SR_{IOP}	Current Slew Rate	0.9	1.0	1.1	mA/μs	Constant after Linear Point
V_{PS}	Blow Sense Voltage	0.7			V	
t_{dBP}	Delay to Programming Ramp	2.0	3.0		μs	V_{CSP} must be at minimum
t_{LP}	Time to Reach Linear Point	0.2	1.0	10	μs	
t_{SS}	Program Sense Inhibit	2.0	3.0	10	μs	
t_{tp}	Time to Program Fuse	3.0		150	μs	
t_{hAP}	Programming Ramp Hold Time	1.4	1.5	1.6	μs	After fuse programs
t_{fIOP}	Program Ramp Fall Time		0.1	0.2	μs	

Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temp. T_A = 25°C ±10°C.

National Semiconductor

93Z665/93Z667
8192 x 8-Bit Programmable Read Only Memory

General Description

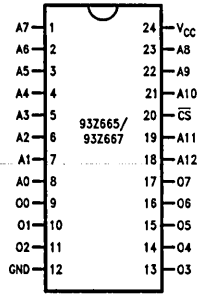
The 93Z665/93Z667 are fully decoded 65,536-bit Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. The 93Z665 and 93Z667 are manufactured using highly reliable ISO-Z vertical fuse technology.

Features

- 93Z667 available in 300-mil side-braze DIP
- 93Z665 available in 600-mil side-braze DIP, leadless chip carrier, and Flatpak
- Commercial address access time — 35 ns, 40 ns and 45 ns max
- Military address access time — 45 ns, 50 ns and 55 ns max
- Highly reliable vertical fuses ensure high programming yields
- Power-up TRI-STATE® outputs
- Low current PNP inputs
- Complete AC/DC testability

Connection Diagrams

Dual-In-Line Package

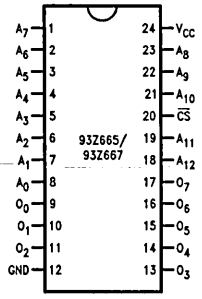


TL/D/9669-2

Top View

Order Number 93Z665D or 93Z667D
See NS Package Number D24H*

Flatpak

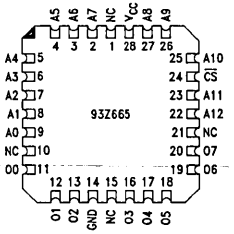


TL/D/9669-10

Top View

Order Number 93Z665F
See NS Package Number W24C*

Leadless Chip Carrier



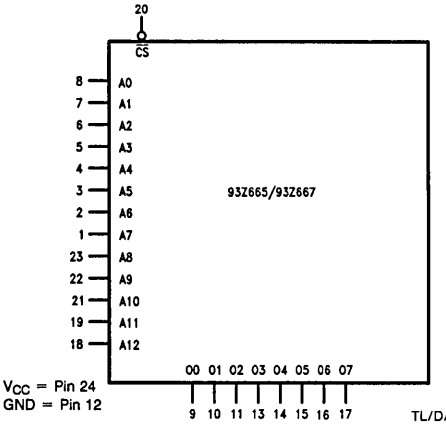
TL/D/9669-3

Top View

Order Number 93Z665L
See NS Package Number V28A*

*For most current package information, contact product marketing

Logic Symbol

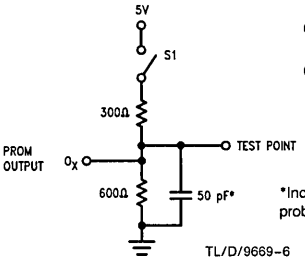


TL/D/9669-5

Pin Names

A0–A12	Address Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
O0–O7	Data Outputs

AC Test Output Load



TL/D/9669-6

Absolute Maximum Ratings Above which the useful life may be impaired

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Notes 1 & 2)	−1.5V to V_{CC}
Voltage Applied to Outputs (Output HIGH) (Notes 2 & 3)	−1.5V to +5.5V
Lead Temp. (Soldering, 10 seconds)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current per Output (10 seconds Max)	−100 mA for V_{OH} and +100 mA for V_{OL}
Output Current High Impedance	+20 mA (Max)
Input Current (DC)	−18 mA to +5.0 mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

Note 2: These values may be exceeded as required during PROM programming.

Note 3: Output Current limit required.

Operating Conditions

Ambient Operating Temperature	
Commercial	0°C to +70°C
Military	−55°C to +125°C
Positive Supply Voltage	
Commercial	5.0V ±5%
Military	5.0V ±10%
Maximum Low-Level Input Voltage (V_{IL})	0.8V
Minimum High-Level Input Voltage (V_{IH})	2.0V

DC Performance Characteristics: over guaranteed operating ranges unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs	2.0			V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.2	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.30	0.45	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −2.0 mA Address Any "1"	2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.45V		−10	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.4V to V_{CC}	−40		40	μA
I_{OHZ} I_{OLZ}	Output Leakage Current for HIGH Impedance State	V_{OH} = 2.4V V_{OL} = 0.4V			40 −40	μA μA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_O = 0V (Note 2) Address Any "1"	−15	−80	−100	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs GND, All Outputs Open			180	mA
C_{IN}	Input Pin Capacitance	V_{CC} = 5.0V, V_{IN} = 4.0V, f = 1.0 MHz		7.0 (Note 3)	15.0	pF
C_O	Output Pin Capacitance	V_{CC} = 5.0V, V_O = 4.0V, f = 1.0 MHz		10.0 (Note 3)	15.0	pF

AC Performance Characteristics

Symbol	Parameter	Conditions	-35	-40	-45	Units
COMMERCIAL V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C						
t_{AA}	Address to Output Access Time	See AC Output Load and Note 5	35	40	45	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load and Note 5	20	20	30	ns
t_{HZ}	Chip Deselect to Output TRI-STATE	See AC Output Load and Note 4	20	20	30	ns

AC Performance Characteristics (Continued)

Symbol	Parameter	Conditions	-40	-45	-50	Units
MILITARY V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C						
t_{AA}	Address to Output Access Time	See AC Output Load and Note 5	45	50	55	ns
t_{ACS}	Chip Select to Output Access Time	See AC Output Load and Note 5	25	25	30	ns
t_{HZ}	Chip Deselect to Output TRI-STATE	See AC Output Load and Note 4	25	25	30	ns

Note 1: Typical values are at V_{CC} = 5.0V, +25°C and maximum loading.

Note 2: Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Note 3: This parameter value is based on initial design qualification and is also verified on every design change. These are not tested in production.

Note 4: t_{HZ} is tested with load shown in *Figure 2*. Transition to High-Z is measured at steady state high V_{OH} level −500 mV or steady state low V_{OL} level +500 mV on the outputs from the point at which chip select crosses the 1.5V level towards its V_{IH} level.

Note 5: AC Address Access and Chip Select Access is done under the following test conditions. Input pulse levels are from 0V to 3V and input/output timing reference levels at 1.5V.

Current-Pulse Programming Specifications (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Power Supply Voltage	Typical I_{CC} at 6.5V = 250 mA	6.4	6.5	6.6	V
$t_{r\,VCC}$	Power Supply Rise Time (Note 3)		0.2	2.0		µs
$t_{f\,VCC}$	Power Supply Fall Time		0.2	2.0		µs
t_{ON}	V_{CC} ON Time	See Programming Timing Diagram	(Note 1)			
t_{OFF}	V_{CC} OFF Time		(Note 2)			
	Duty Cycle for V_{CC}	$t_{ON}/(t_{OFF} + t_{ON})$			50	%
READ STROBE (Note 5)						
t_W	Fuse Read Time	Machine Cycle		1.0		µs
t_{dRAP}	Delay to Read after Programming	Verify		3.0		µs
t_{CS}	Chip Enable		0.1	1.0		µs
OUTPUT DESELECT						
V_{OS}	Output Deselect Voltage		11.8	12	12.5	V
I_{OS}	Output Deselect Current Limit		20	50	100	mA
O_{VS}	Output Voltage Select	TTL H or L		5.0	5.5	V
t_{rod}	Output Deselect Rise Time		1.0	1.0	2.0	µs
t_{fod}	Output Deselect Fall Time		0.1	0.1	1.0	µs
t_{CSDD}	Deselect Chip to Deselect Output		0.1	1.0		µs
PROGRAMMING CURRENT-PULSE TRAIN ON CHIP SELECT						
$I_{CSp(Min)}$	Initial Current Pulse			40	60	mA
$I_{CSp(Max)}$	CS Programming Current Limit	Apply Current Pulse to Chip Select Pin 20	155	160	165	mA
$V_{CSp(Max)}$	CS Programming Voltage Limit		24	25	26	V
t_{rcsp}	Programming Pulse Rise Time		160	100	100	mA/µs
t_{dBP}	Delay to Initial Programming Pulse		2.0	3.0		µs
t_{dAP}	Delay after Programming Pulse		1.0	1.0		µs
t_{PW}	Programming Pulse Widths		6.0	7.0	9.0	µs
t_{fCSp}	Programming Pulse Fall Time (Note 3)		0.1	0.1	0.2	µs
ΔI_{CSp}	Current Pulse Step Increase		5.0	10.0	10.0	mA
	Duty Cycle for Programming Pulses	Each Successive Pulse is Increased by ΔI_{CSp}	10	50	50	%

Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

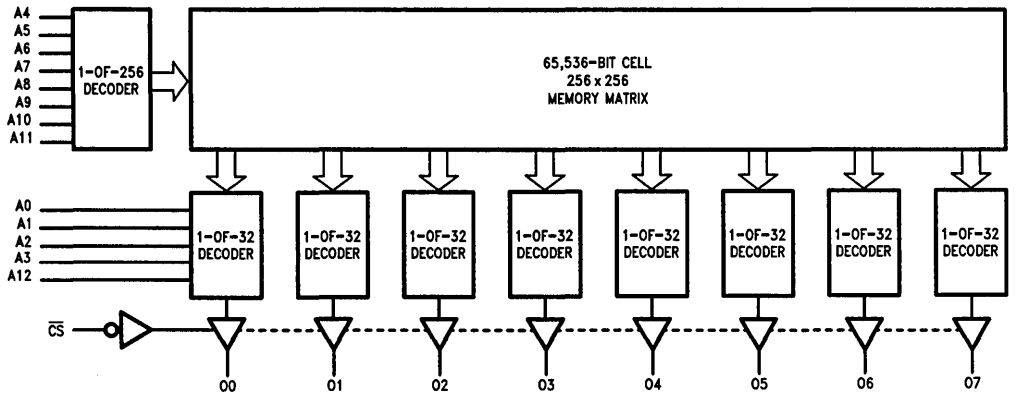
Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temp. T_C = +25°C ±10°C.

Note 5: Proceed to next address after read strobe indicates programmed cell.

Block Diagram



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Note: Programmed = Low
Unprogrammed = High on the Outputs

Functional Description

The 93Z665 and 93Z667 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. The 93Z665 and 93Z667 have TRI-STATE outputs which provide active pull-ups and pull-downs when enabled and high output impedence when disabled. This allows optimization of word expansion in bus organized systems.

Chip Select is provided for memory expansion without the need for additional decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. The device is enabled only when $\overline{CS}$ is LOW. During system power up, outputs remain in the high impedance state until DC power supply conditions are met, thereafter changing state according to the condition of $\overline{CS}$.

The devices contain internal test rows and test columns which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters. PROM programmability is verified through test row and test column. PROM input levels on unprogrammed devices are also verified through testing of test row and test column.

The 93Z665 and 93Z667 use open base vertical (junction) fuse cells. Initially the unprogrammed cell is in the logic "1" state. A cell can be programmed to the logic "0" state by following the specified programming procedure which defuses aluminum through the emitter base junction of the cell transistor, thereby forming a low impedance path.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A0 through A12 and the chip is selected. Data is then available at the outputs after t_{AA}.

Programming

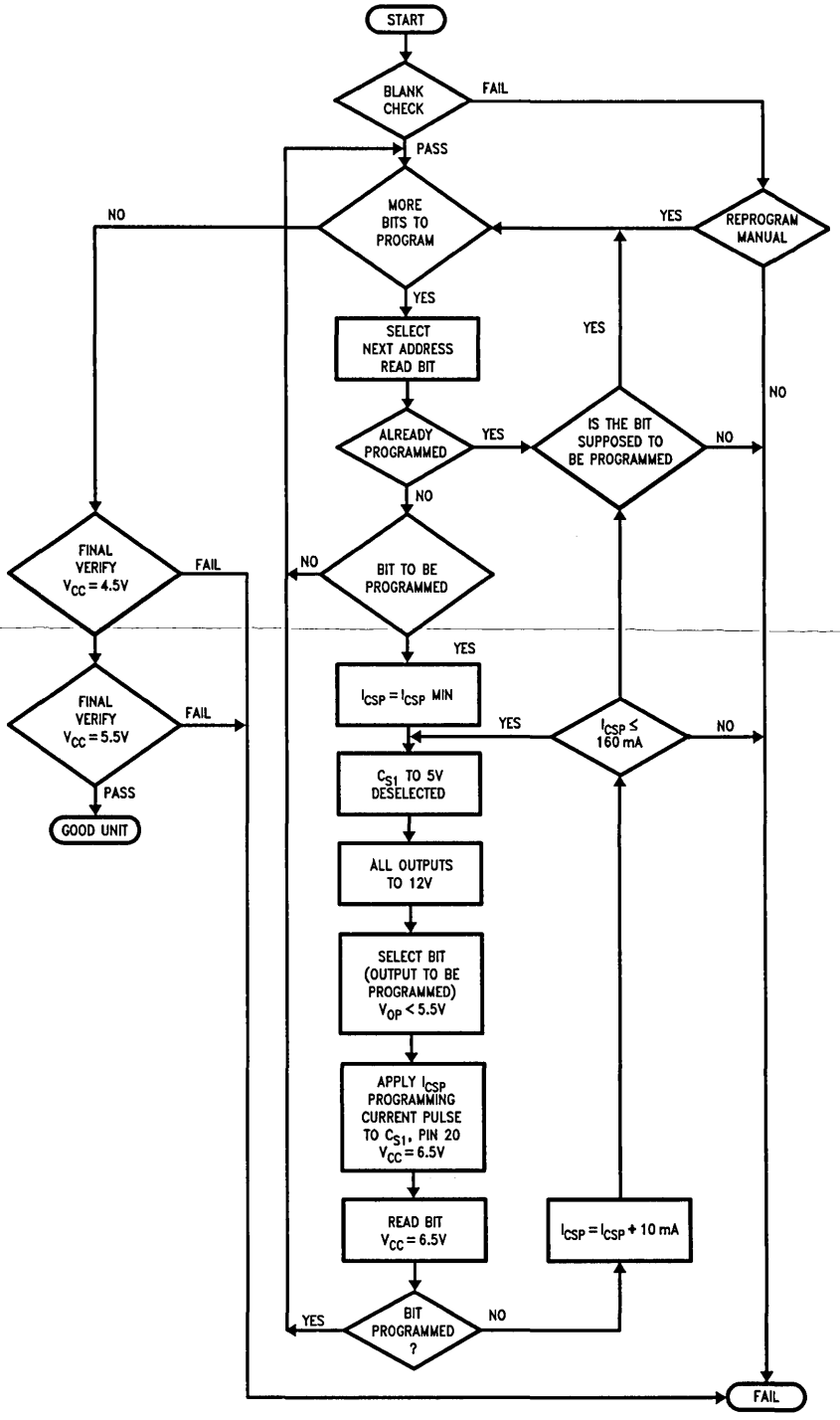
The 93Z665 and 93Z667 are manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure below. One may use any of the commercially available programmers which have been approved by National Semiconductor.

I. Blank Check—Initial Read.
   - A. Chip Select is Enabled
   - B. V_{CC} is Raised to 5.5V
   - C. TTL Levels are Applied to All Address Lines
   - D. Verify All Outputs are TTL High on All Addresses
   - E. Repeat C and D until All Addresses have been Checked

II. Programming Mode
   - A. TTL Levels are Applied to All Address Lines
   - B. V_{CC} is Raised to 6.5V
   - C. Chip Select is Deselected
   - D. All Outputs are Raised to 12V
   - E. Selected Output is Lowered Below 5.5V
   - F. Programming Current Pulse Train is Applied to the Chip Select Pin
   - G. Consecutive Current Pulses are 7 μs–9 μs Wide and Increase at 10 mA per Pulse
   - H. A Read is Performed before and after Each Pulse (V_{CC} = 6.5V)
   - I. The Programming Current is Stepped Up until the Cell Programs

III. Final Verify (2 Pass)
   - A. V_{CC} is Lowered to 4.5V
   - B. Chip Select is Enabled
   - C. TTL Levels are Applied to All Address Lines
   - D. Verify Pattern on All Outputs, All Addresses
   - E. Repeat C and D for All Addresses
   - F. V_{CC} Increases to 5.5V
   - G. Repeat B, C, D and E

Programming Flow Chart



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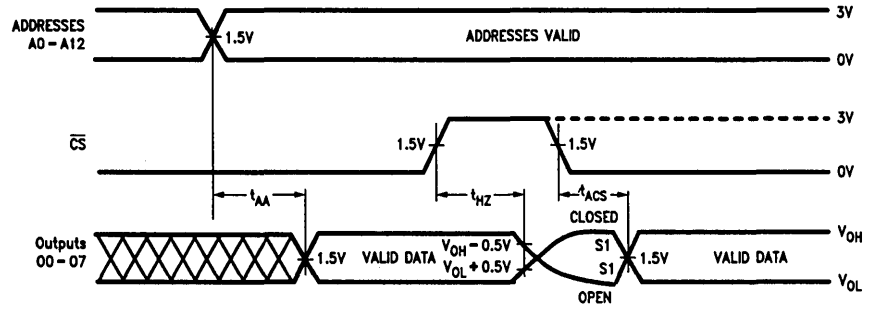
Timing Diagrams

READ MODE TIMING

Propagation Delay from Address Valid to Output and $\overline{CS}$ Valid to Output



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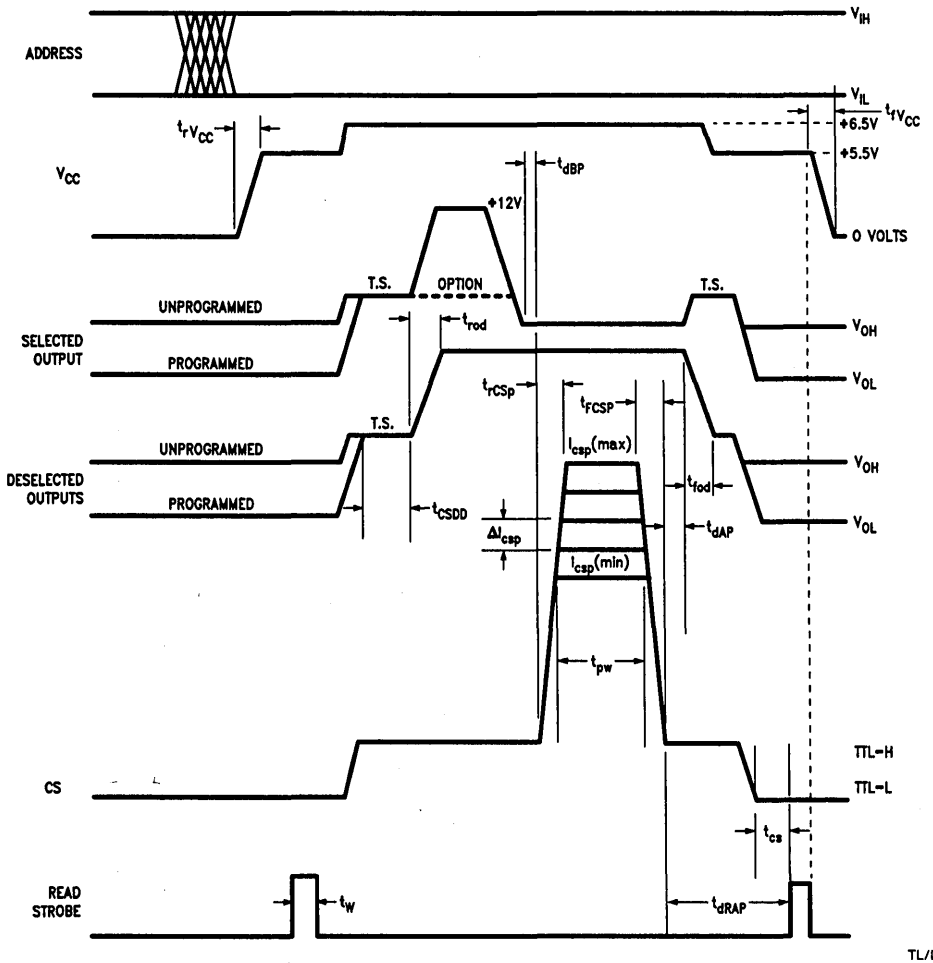
PROGRAMMING TIMING DIAGRAM



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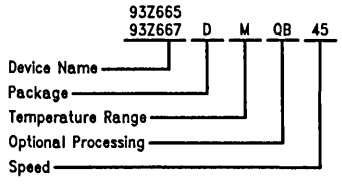
Note:

Typical Output Characteristics using a 1 kΩ Pull-Up Resistor to 5V. 12V, TTL-H, and TTL-L Force Voltages.
T.S. is TRI-STATE.

Ordering Information



TL/D/9669–4

Packages

D = Side-Braze DIP
L = Leadless Chip Carrier
F = Flatpak

Temperature Ranges

Com. = 0°C to +75°C
Mil. = −55°C to +125°C

Speed

Com	= 35 ns	Mil.	= 45 ns
	= 40 ns		= 50 ns
	= 45 ns		= 55 ns

Optional Processing

QB = Mil STD 883
Method 5004 & 5005
Level B

National Semiconductor

PRELIMINARY

NMC27C49 Very High Speed Version 65,536-Bit (8k x 8) UV Erasable CMOS PROM Pin Compatible with 64k Bipolar PROMs

General Description

The NMC27C49 is a very high-speed 64k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C49 is designed to operate with a single +5V power supply with ±10% tolerance.

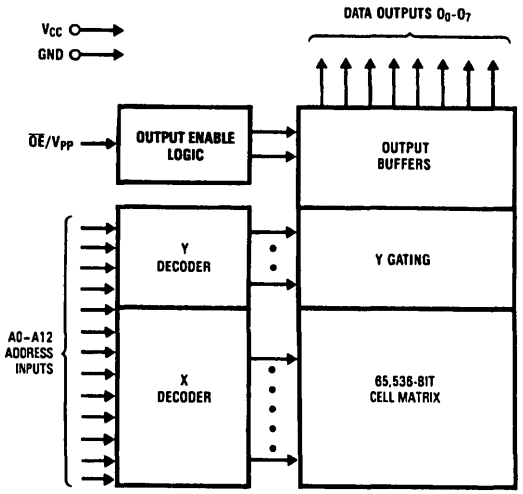
The NMC27C49 is packaged in a 300 mil, 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time-proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and a two transistor memory cell for fast acess time down to 35 ns
- Low CMOS power consumption
  —Active power: 275 mW max
- Performance compatible to current high speed microprocessors
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with 64k Bipolar PROMs
- Manufacturer's identification code for automatic programming control
- High current CMOS level output driver

Block Diagram



TL/D/9186-1

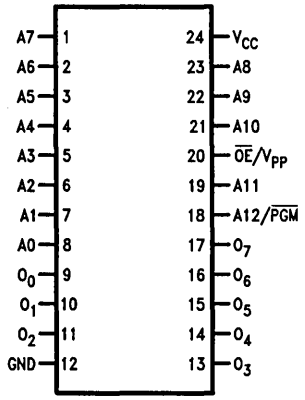
Pin Names

A0–A12	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program

Connection Diagram

27C53	27C51
A9	A9
A8	A8
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O_0	O_0
O_1	O_1
O_2	O_2
GND	GND

Dual-In-Line Package



TL/D/9186-2

27C51	27C53
V_{CC}	V_{CC}
A10	A10
A11	A11
A12	A12
A13	A13
$\overline{OE1}/V_{PP}$	A14
$\overline{OE2}/\overline{VFY}$	$\overline{OE1}/V_{PP}$
OE3	$OE2/\overline{PGM}$
$\overline{OE4}/\overline{PGM}$	$\overline{OE3}/\overline{VFY}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C49 pins.

Order Number NMC27C49Q
See NS Package Number J24CQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C49Q35	35
NMC27C49Q45	45
NMC27C49Q55	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and A10 with Respect to Ground (Note 4)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 4)	V_{CC} + 1.0V to GND − 0.6V
$\overline{OE}/V_{PP}$ Supply Voltage, A9 and A10 with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{OE}/V_{PP} = V_{IH}$			1.0	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 1)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = V_{IL}$, f = 20 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 1)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE}$ = GND, f = 20 MHz Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
V_{IL}	Input Low Voltage	(Note 4)	−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 8)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 8)	V_{CC} − 0.1			V

AC Electrical Characteristics

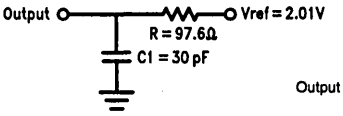
Symbol	Parameter	Conditions	NMC27C49						Units
			Q35		Q45		Q55		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE} = V_{IL}$		35		45		55	ns
t_{OE}	OE to Output Delay	$\overline{OE} = V_{IL}$		20		25		25	ns
t_{DF} (Note 3)	OE High to Output Float	$\overline{OE} = V_{IH}$	0	20	0	25	0	25	ns
t_{OH}	Output Hold from Addresses, or $\overline{OE}$ = Enable, Whichever Occurred First	$\overline{OE} = V_{IL}$	0		0		0		ns

Capacitance $T_A = +25°C, f = 1$ MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

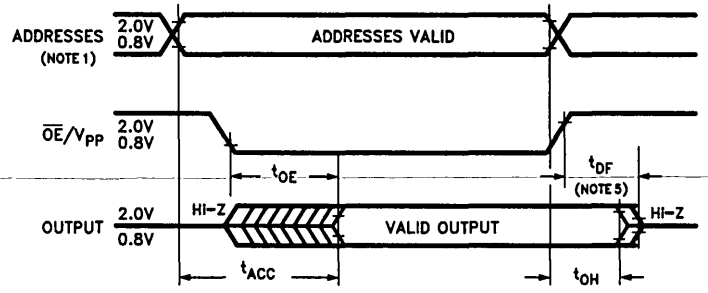
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0V to 3.0V
Output Load (Note 6)	R = 97.6Ω C_L = 30 pF V_{REF} = 2.01V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



Output Loading

TL/D/9186-3

AC Waveforms (Notes 7 & 8)



TL/D/9186-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: Inputs and outputs can undershoot to −2.0V for 20 ns max.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: C_L: 30 pF includes fixture capacitance.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Programming Characteristics

T_A = +25°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V (Notes 1–4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{LS}	A_{11} Setup Time for Latching		50			ns
t_{LH}	A_{11} Hold Time for Latching		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay (Note 5)		0		40	ns
t_{DV}	Data Valid from $\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP} = V_{IH}$ or V_{IL}			100	ns
t_{AV}	Data Valid from Address	$\overline{OE}/V_{PP} = V_{IH}$ or V_{IL}			100	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns
t_{VPW}	V_{PP} Level Pulse Width on A9 or A10		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$A12/\overline{PGM} = V_{IL}$			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal supply voltages.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Functional Description

DEVICE OPERATION

The modes of operation of the NMC27C49 are listed in Table I. It should be noted that all inputs for the modes may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the programming and verify modes, and at 5V in the other modes. The $\overline{OE}/V_{PP}$ pin must be at 12.75V in four of the programming modes, and V_{IL} in the read mode.

READ MODE

The NMC27C49 has one control function, Output Enable ($\overline{OE}/V_{PP}$), which must be logically active in order to obtain data at the outputs. This is only true, however, when the device is not latched into programming mode or verify mode, so care must be taken to be sure the device is not in these modes. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground), an address transition must be performed after the drop to ensure proper output data.

PROGRAMMING

CAUTION: Exceeding 14V on pin 20 ($\overline{OE}/V_{PP}$) will damage the NMC27C49.

The NMC27C49 has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed, one or the other of the two transistors is programmed. When accessed, the memory cell will discharge one of the two data lines, providing a differential voltage. This differential voltage is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state, both transistors source the same current through the data lines and thus no differential voltage is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs.

To verify that a device is totally blank, the verify mode must be entered. This is accomplished by raising A10 to V_{PP} and then back to the proper logic level (less than 5V). In the verify mode, each transistor of the memory cell is checked against a reference cell. By toggling $\overline{OE}/V_{PP}$, both transistors in the cell are checked. For a totally unprogrammed device in the verify mode, all outputs will be at a "1" state for $\overline{OE}/V_{PP} = V_{IH}$ and at a "0" state for $\overline{OE}/V_{PP} = V_{IL}$. The verify mode is exited by either powering down the device, or by raising A9 to V_{PP} and then back to a logic level (less than 5V) with $\overline{OE}/V_{PP}$ at V_{IH}.

The programming mode is entered by raising $\overline{OE}/V_{PP}$ to 12.75V. In this mode, the A12/$\overline{PGM}$ pin functions as the programming control pin. Addressing while in programming mode is accomplished by placing the A12 address on A11 and then latching this into an onboard register when $\overline{OE}/V_{PP}$ is raised to 12.75V. The NMC27C49 is now locked into the programming mode and half of the chip can be programmed. Once half of the device is programmed and verified, the programming mode must be exited and then re-entered with the opposite data for address A12 in order to program the other half of the device. The programming mode is exited by powering down the device, or by dropping $\overline{OE}/V_{PP}$ to V_{IH} and then raising A9 to V_{PP} and then back to a logic level.

It is required that at least a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the device has been latched into programming mode and the addresses and data are stable, an active low TTL program pulse is applied to the A12/$\overline{PGM}$ input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when, in the verify mode, toggling $\overline{OE}/V_{PP}$ reads back the same data in both modes. The NMC27C49

TABLE I. Mode Selection

Mode \ Pins	$\overline{OE}/V_{PP}$ (20)	A12/$\overline{PGM}$ (18)	A9 (22)	A10 (21)	A11 (19)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	X	X	X	X	5V	D_{OUT}
Output Disable	V_{IH}	X	X	X	X	5V	Hi-Z
Enter Programming Mode for Addresses with A12 = V_{IL}	12.75V	V_{IH}	X	X	V_{IL}	6.25V	D_{IN}
Enter Programming Mode for Addresses with A12 = V_{IH}	12.75V	V_{IH}	X	X	V_{IH}	6.25V	D_{IN}
Program	12.75V	V_{IL}	X	X	X	6.25V	D_{IN}
Enter Initial Verify Mode	X	X	X	12	X	6.25V	D_{OUT}
Verify (Mode 1)	V_{IH}	V_{IH}	X	X	X	6.25V	D_{OUT} (V_{OH} if Blank)
Verify (Mode 2)	V_{IL}	V_{IH}	X	X	X	6.25V	D_{OUT} (V_{OL} if Blank)
Program Inhibit	12.75V	V_{IH}	X	X	X	6.25V	Hi-Z
Exit Programming Mode and Verify Mode	V_{IH}	V_{IH}	12	X	X	6.25V	Hi-Z

X = Don't Care

Functional Description (Continued)

is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C49 must not be programmed with a DC signal applied to the A12/$\overline{PGM}$ input.

Programming multiple NMC27C49s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C49s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the A12/$\overline{PGM}$ input programs the paralleled NMC27C49s.

PROGRAM INHIBIT

Programming multiple NMC27C49s in parallel with different data is also easily accomplished. Except for A12/$\overline{PGM}$, all like inputs (including $\overline{OE}/V_{PP}$) of the paralleled NMC27C49s may be common. A TTL low level applied to an NMC27C49's A12/$\overline{PGM}$ input will program that NMC27C49 while keeping the same pin high on the others inhibits programming.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. A verify done in the read mode may not ensure that the bits have been programmed with adequate margins for reliable operation. To guarantee adequate margins the device should be verified in the verify mode, where each transistor of the memory cell is checked against a reference cell. Verify mode can be entered two different ways. The first way is by verifying after programming. When $\overline{OE}/V_{PP}$ is at 12.75V, the device is in programming mode, and when $\overline{OE}/V_{PP}$ is brought back down to V_{IH} or V_{IL}, it is in the verify mode. The second method for entering the verify mode is to apply 12V to address pin A10 with the other pins at V_{IH} or V_{IL}. This method is recommended if possible for an initial verify when the device is totally unprogrammed because power up only needs to be performed once. Independent of how verify mode is entered, $\overline{OE}/V_{PP}$ is biased at V_{IH} and the data is read for verify mode 1 and at V_{IL} for verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell. For a totally unprogrammed device, all outputs will be at a "1" state for verify mode 1 and at a "0" state for verify mode 2. As in programming mode, verify mode is exited by powering down the device, or by raising A9 to V_{PP} and then back to a logic level with $\overline{OE}/V_{PP}$ at V_{IH}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C49 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip.

It identifies the manufacturer and the device type. The code for the NMC27C49 is "83C2", where "83" designates that it is made by National Semiconductor, and "C2" designates that it is a 64k part. The code is acessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A12, and $\overline{OE}/V_{PP}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C49 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Opaque labels should be placed over the NMC27C49s window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C49 Erasure Time

Light Intensity ($\mu W/cm^2$)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Functional Description (Continued)

The recommended erasure procedure for the NMC27C49 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

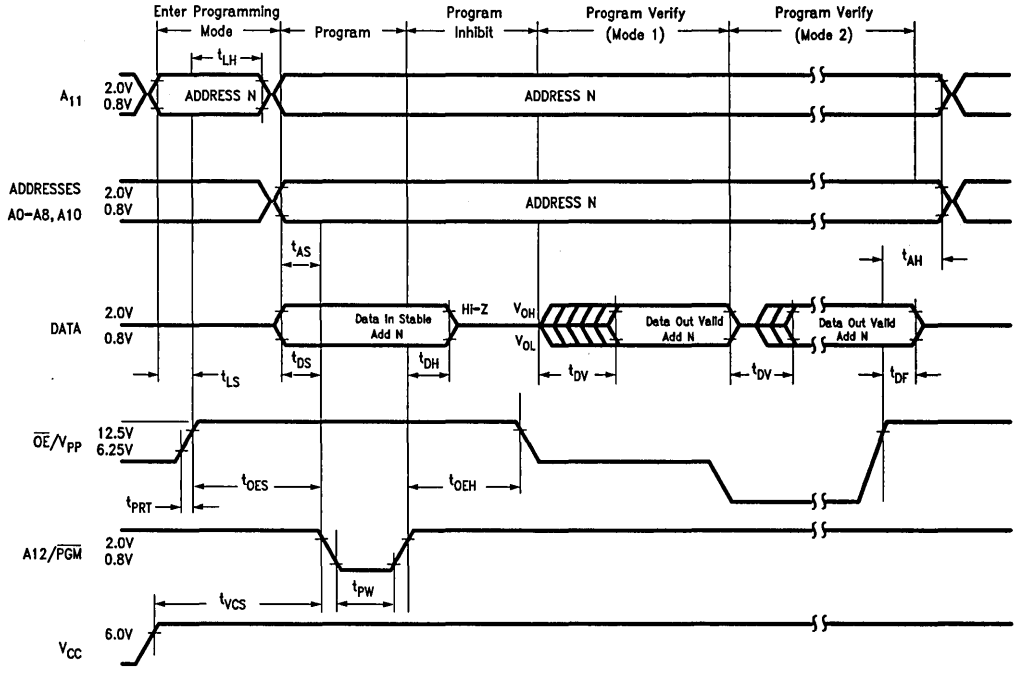
The NMC27C49 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C49 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

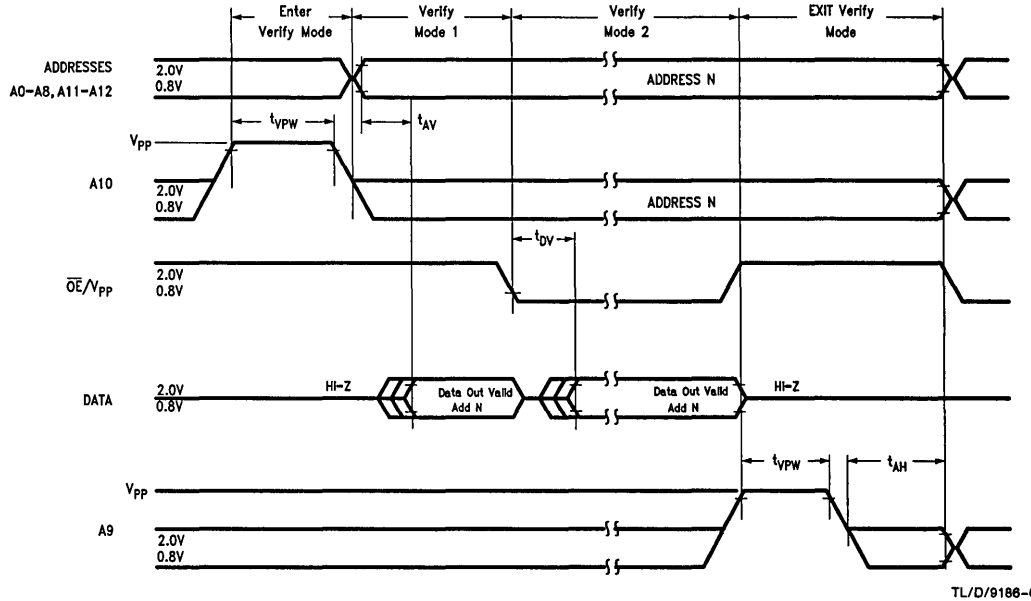
The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Programming Waveforms (Note 3)

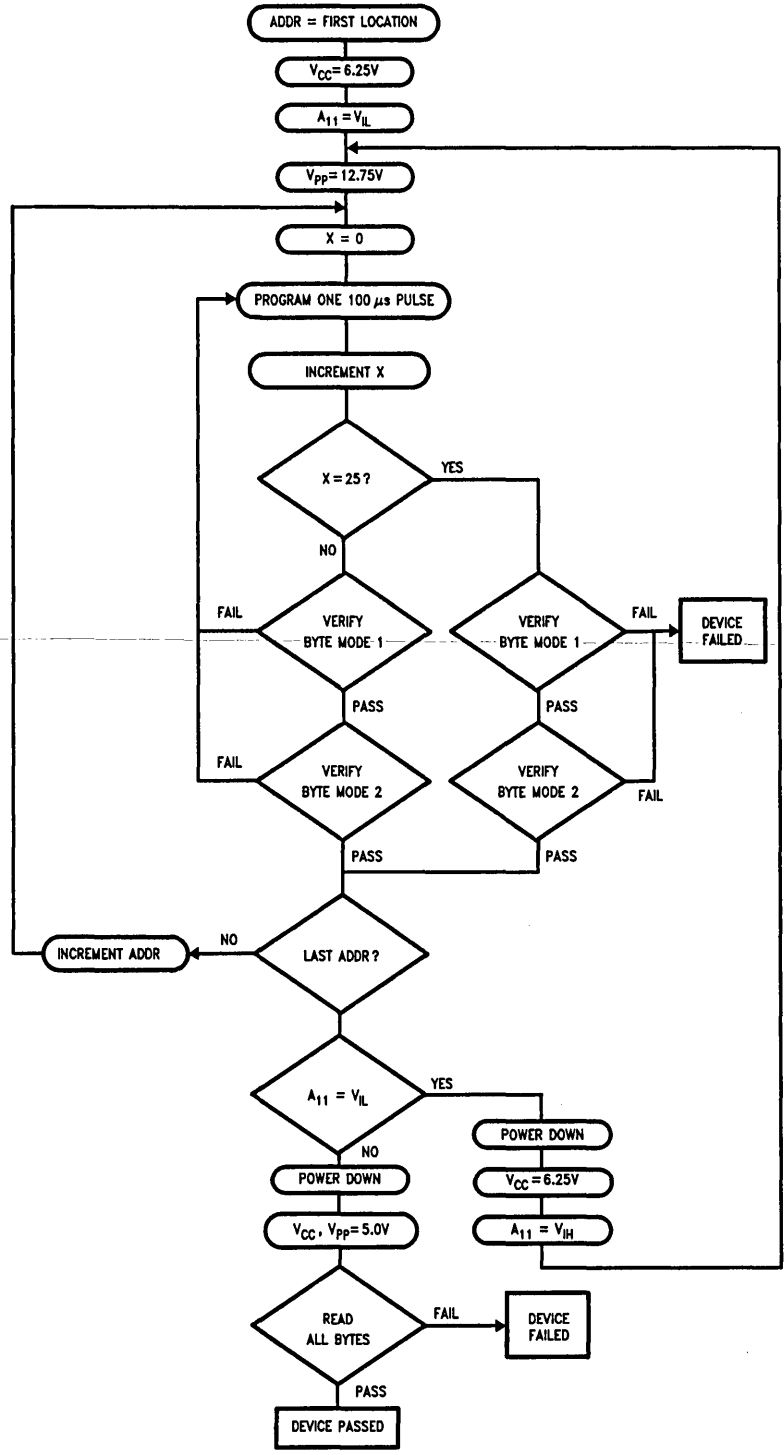


TL/D/9186-5

Initial Program Verify Waveforms



TL/D/9186-6



TL/D/9186–7

FIGURE 1. Fast Programming Algorithm Flow Chart

National Semiconductor

PRELIMINARY

NMC27C51 Very High Speed Version 131,072-Bit (16k x 8) UV Erasable CMOS PROM Pin Compatible with 128k Bipolar PROMs

General Description

The NMC27C51 is a very high-speed 128k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C51 is designed to operate with a single +5V power supply with ±10% tolerance.

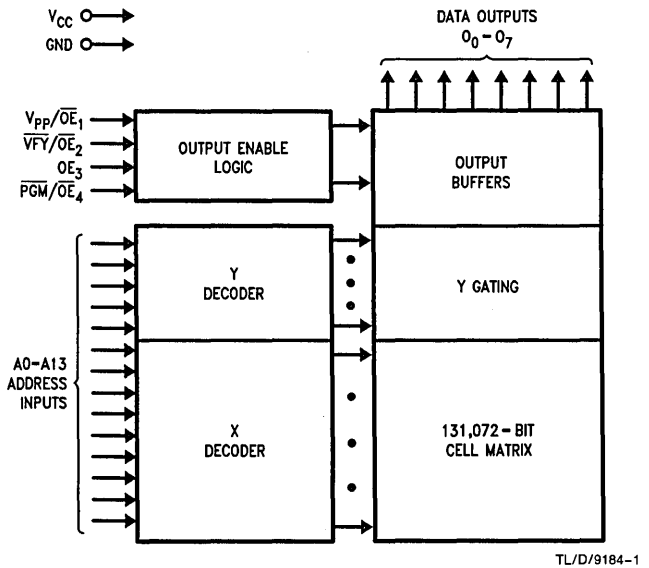
The NMC27C51 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and a two transistor memory cell for fast access time down to 45 ns
- Performance compatible with current high-speed microprocessors
- Low CMOS power consumption
  — Active power: 275 mW max
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with 128k Bipolar PROMs
- Manufacturer's identification code for automatic programming control
- High current CMOS level output driver

Block Diagram



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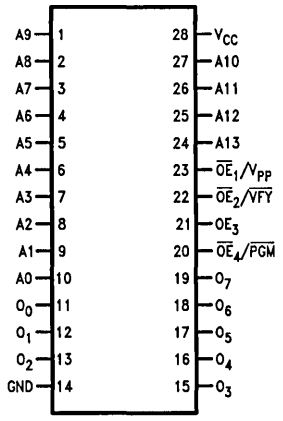
Pin Names

A0–A13	Addresses
$\overline{OE}_1$–$\overline{OE}_4$	Output Enable
$\overline{VFY}$	Verify
$\overline{PGM}$	Program
O0–O7	Outputs

Connection Diagram

27C53	27C49
A9	
A8	
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O0	O0
O1	O1
O2	O2
GND	GND

NMC27C51Q
Dual-In-Line Package



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27C49	27C53
	VCC
	A10
VCC	A11
A8	A12
A9	A13
A10	A14
OE/VPP	OE1/VPP
A11	OE2/PGM
A12/PGM	OE3/VFY
O7	O7
O6	O6
O5	O5
O4	O4
O3	O3

Note: National's socket compatible EPROM with configurations are shown in the blocks adjacent to the NMC27C51Q pins.

Order Number NMC27C51Q
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C51Q45	45
NMC27C51Q55	55
NMC27C51Q70	70

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A13 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
$\overline{OE}_1/V_{PP}$ and A13 Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND; $\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_4 = V_{IH}$ or $OE_3 = V_{IL}$			1.0	μA
I_{PP1}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 7)	V_{CC} Current (Active) TTL Inputs	f = 20 MHz, All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 7)	V_{CC} Current (Active) CMOS Inputs	f = 20 MHz, All Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
V_{IL}	Input Low Voltage	(Note 10)	−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 8)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 8)	V_{CC} − 0.1			V

AC Electrical Characteristics

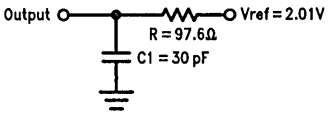
Symbol	Parameter	Conditions	NMC27C51						Units
			Q45		Q55		Q70		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_4 = V_{IL}$, $OE_3 = V_{IH}$		45		55		70	ns
t_{OE}	OE to Output Delay			25		25		30	ns
t_{DF} (Note 3)	OE Disable to Output Float		0	25	0	25	0	30	ns
t_{OH}	Output Hold from Addresses, $\overline{OE}_1$, $\overline{OE}_2$, OE_3 or $\overline{OE}_4$, Whichever Occurred First	$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_4 = V_{IL}$ $OE_3 = V_{IH}$	0		0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

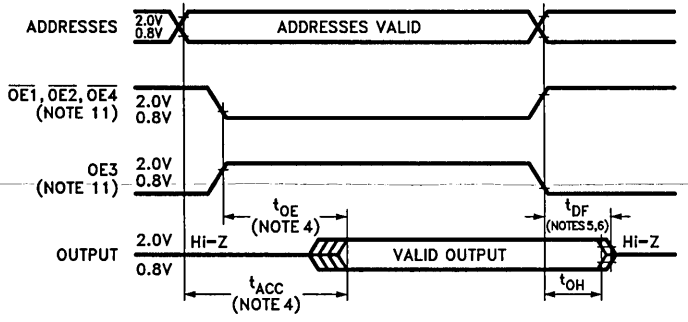
AC Test Conditions

Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0 to 3.0V
Output Load (Note 9)	R = 97.6Ω
	C_L = 30.0 pF
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



TL/D/9184-3

AC Waveforms (Notes 7, 8 & 11)



TL/D/9184-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: OE/$\overline{OE}$ true may be delayed up to $t_{ACC} - t_{OE}$ after address change without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V.
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained by any OE signal.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: C_L: 30 pF includes fixture capacitance.

Note 10: Inputs and outputs can undershoot −2.0V for a maximum of 20 ns.

Note 11: For the output to be in low-Z all OE/$\overline{OE}$ inputs must be in their logical true states, i.e., $\overline{OE1}$, $\overline{OE2}$, $\overline{OE4}$ must be at V_{IL} and OE3 must be at V_{IH}. If any or all of these inputs are not at their logical true level then the outputs will be in Hi-Z.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}_4$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		50	ns
t_{PW}	Program Pulse Width		95	100	105	μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{OE}_4 = V_{IL}$			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
t_{VM1}	$\overline{OE}_2$ to Data Valid During Verify Mode 1 (Verify Mode)	$\overline{OE}_1/V_{PP} = V_{PP}$, $\overline{OE}_4, OE_3 = V_{IH}$			0.1	μs
t_{VM2}	$\overline{OE}_4$ to Data Valid During Verify Mode 2 (Verify Mode)	$\overline{OE}_1/V_{PP} = V_{PP}$, $\overline{OE}_2 = V_{IL}$ $OE_3 = V_{IH}$			0.1	μs
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C51 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 pF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C51 are listed in Table I. It should be noted that all inputs may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the four programming modes, and at 5V in the other two modes. The $\overline{OE}_1/V_{PP}$ pin must be at 12.75V in the programming and verify mode, and V_{IL} in the read mode.

READ MODE

The NMC27C51 has four select functions, all of which must be logically active in order to obtain data at the outputs. Data is available at the falling edges of $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_4$ and the rising edge of OE_3, assuming that the addresses have been stable for at least t_{ACC}-t_{OE}. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

OUTPUT OR-TYING

Because NMC27C51s are usually used in larger memory arrays, National has provided a 4-line control function that accommodates this use of multiple memory connections. The 4-line control function allows for complete assurance that output bus contention will not occur. All Output Enables are functionally equivalent.

PROGRAMMING

CAUTION: Exceeding 14V on pin 23 ($\overline{OE}_1/V_{PP}$) will damage the NMC27C51.

The NMC27C51 has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed, one or the other of the two transistors is programmed. When accessed the memory cell will discharge one of the two data lines, providing a differential voltage. This differential signal is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state both transistors source the same current through the data lines and thus no differential is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs.

The NMC27C51 is in the program mode when $\overline{OE}_1/V_{PP}$ is raised to 12.75V. In this mode, the $\overline{OE}_4$/PGM pin functions as the PGM pin which controls the programming pulse width (t_{PW}) and the $\overline{OE}_2$/VFY pin functions as the VFY pin which is to be held at V_{IL} during program verify.

To verify that a device is totally blank, the verify mode must be entered. In the verify mode each transistor of the memory cell is checked against a reference cell. By toggling $\overline{OE}_4$ both transistors in the cell are checked. For a totally unprogrammed device in the verify mode all outputs will be at a "1" state for $\overline{OE}_4 = V_{IH}$ and at a "0" state for $\overline{OE}_4 = V_{IL}$.

It is required that at least a 0.1 μF capacitor be placed across $\overline{OE}_1/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address, clock, and data inputs are TTL.

When the addresses, clocks, and data are stable, an active low, TTL program pulse is applied to the $\overline{OE}_4$ input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when data from both verify modes matches the input data. The NMC27C51 is programmed with the fast programming algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses up to a maximum of 25 pulses until the device verifies good. Most memory cells will program with a single 100 μs pulse. The NMC27C51 must not be programmed with a DC signal applied to the $\overline{OE}_4$ input.

Programming multiple NMC27C51s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C51s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{OE}_4$ input (with $\overline{OE}_2$ high) programs the paralleled NMC27C51s.

PROGRAM INHIBIT

Programming multiple NMC27C51s in parallel with different data is also easily accomplished. Except for $\overline{OE}_4$ all like inputs (including $\overline{OE}_1/V_{PP}$, $\overline{OE}_2$ and OE_3 of the paralleled NMC27C51s may be in common. A TTL low level applied to an NMC27C51s $\overline{OE}_4$ input (with the other control pins at the appropriate levels) will program that NMC27C51 while keeping the same pin high on the others inhibits programming.

TABLE I. Mode Selection

Mode \ Pins	$\overline{OE}_1/V_{PP}$ (23)	$\overline{OE}_2/\overline{VFY}$ (22)	OE_3 (21)	$\overline{OE}_4/\overline{PGM}$ (20)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5V	D_{OUT}
Program	12.75V	V_{IH}	X	V_{IL}	6.25V	D_{IN}
Program Verify (Mode 1)	12.75V	V_{IL}	V_{IH}	V_{IH}	6.25V	D_{OUT} V_{OH} if Blank
Program Verify (Mode 2)	12.75V	V_{IL}	V_{IH}	V_{IL}	6.25V	D_{OUT} V_{OL} if Blank
Program Inhibit	12.75V	V_{IH}	X	V_{IH}	6.25V	Hi-Z
Deselect	V_{IH}	V_{IH}	V_{IL}	V_{IH}	5V	Hi-Z

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. Verifying in the read mode may not ensure that the bits have been programmed with adequate margins. To guarantee adequate margins the device should be verified in the verify mode. In this mode each transistor of the memory cell is checked against a reference cell. Verify mode is entered with $\overline{OE1}/V_{PP}$ at 12.75V, $\overline{OE2}$ at V_{IL} and OE_3 at V_{IH}. $\overline{OE4}$ is at V_{IH} and the data read for verify mode 1, and $\overline{OE4}$ is at V_{IL} for verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell.

Manufacturer's Identification Code

The NMC27C51 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C51 is "8343", where "83" designates that it is made by National Semiconductor, and "43" designates it as a 128k part.

The code is accessed by applying 12V ±0.5V to address pin A13. Addresses A1–A12, $\overline{OE1}$, $\overline{OE2}$, and OE_3 and $\overline{OE4}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Erasure Characteristics

The erasure characteristics of the NMC27C51 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C51's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C51 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C51 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C51 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

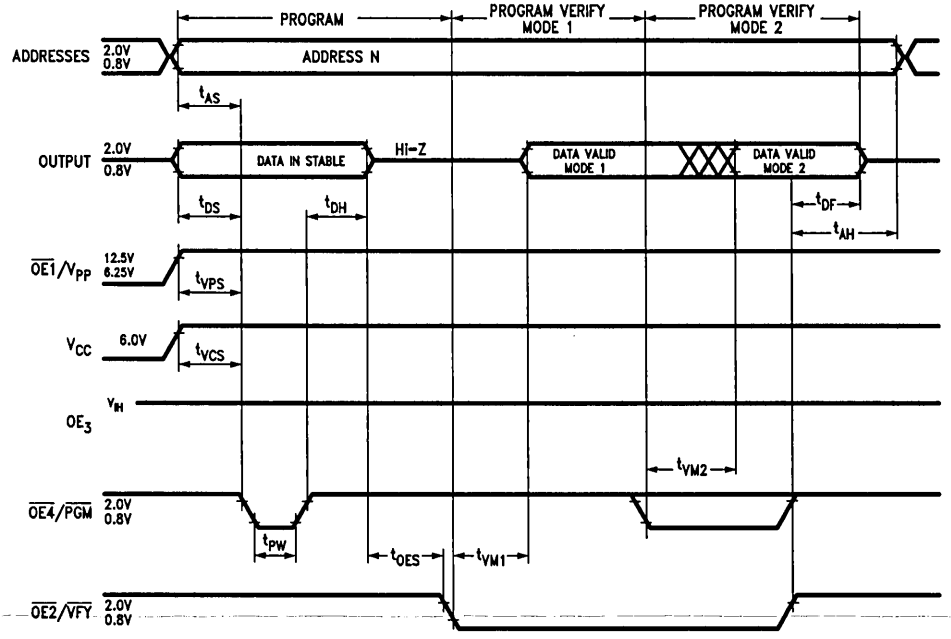
TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	0	1	0	0	0	0	1	1	43

TABLE III. Minimum NMC27C51 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Programming Waveforms (Note 3)



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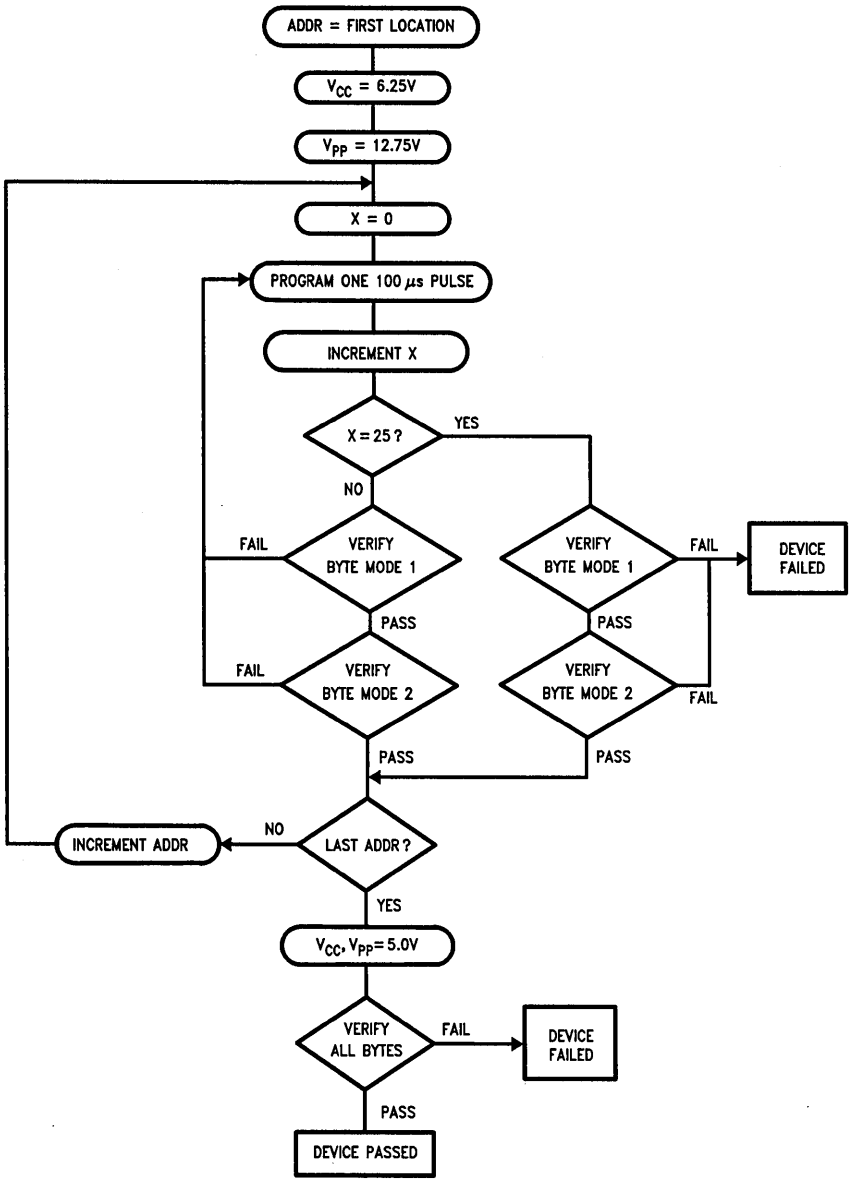
Fast Programming Algorithm Flow Chart



TL/D/9184–6

FIGURE 1

National Semiconductor

NMC27C53 Very High Speed Version 262,144-Bit (32k x 8) UV Erasable CMOS PROM Pin Compatible with 256k Bipolar PROMs

General Description

The NMC27C53 is a very high-speed 256k, UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C53 is designed to operate with a single +5V power supply with ±10% tolerance.

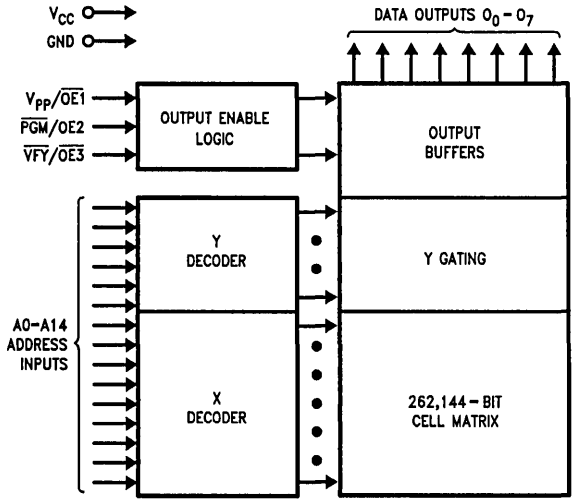
The NMC27C53 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Clocked sense amps and two transistor memory cell for fast access time down to 55 ns
- Low CMOS power consumption
  — Active power: 275 mW max
- Performance compatible to current high speed microprocessors
- Pin compatible with 256k bipolar PROMs
- Single 5V power supply
- Fast and reliable programming (100 μs for most bytes)
- Static operation for NMC27C53—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control
- High current CMOS level output driver

Block Diagram



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Pin Names

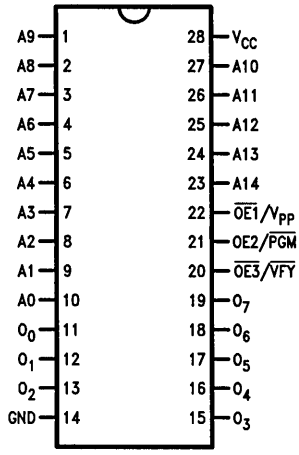
A0–A14	Address
OE1–OE3	Output Enables
O_0–O_7	Outputs
$\overline{PGM}$	Program
$\overline{VFY}$	Verify

4

Connection Diagram

27C51	27C49
A9	
A8	
A7	A7
A6	A6
A5	A5
A4	A4
A3	A3
A2	A2
A1	A1
A0	A0
O_0	O_0
O_1	O_1
O_2	O_2
GND	GND

NMC27C53Q
Dual-In-Line Package



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27C49	27C51
	V_{CC}
	A10
V_{CC}	A11
A8	A12
A9	A13
A10	$\overline{OE1}/V_{PP}$
$\overline{OE}/V_{PP}$	$OE2/\overline{VFY}$
A11	$\overline{OE3}$
$A12/\overline{PGM}$	$\overline{OE4}/\overline{PGM}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C53 pins.

Order Number NMC27C53Q
See NS Package Number J28AQ

Ordering Information

Commercial Temp Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C53Q55	55
NMC27C53Q70	70
NMC27C53Q90	90

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A13 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND−0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
$\overline{OE1}/V_{PP}$ and A13 Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{OE1}$, $\overline{OE3} = V_{IH}$, or OE2 = V_{IL}			1	μA
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 7)	V_{CC} Current (Active) TTL Inputs	f = 20 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		30	70	mA
I_{CC2} (Note 7)	V_{CC} Current (Active) CMOS Inputs	f = 20 MHz Inputs = V_{CC} or GND, I/O = 0 mA		25	50	mA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 16 mA			0.40	V
V_{OH1}	Output High Voltage	I_{OH} = −2.5 mA (Note 8)	3.5			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA (Note 8)	V_{CC} − 0.1			V

AC Electrical Characteristics

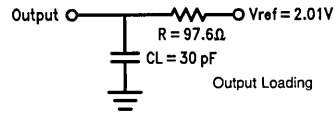
Symbol	Parameter	Conditions	NMC27C53						Units
			Q55		Q70		Q90		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{OE1}$, $\overline{OE3}$ = V_{IL}, OE2 = V_{IH}		55		70		90	ns
t_{OE}	OE to Output Delay			25		30		40	ns
t_{DF}	OE Disable to Output Float (Note 3)		0	25	0	30	0	40	ns
t_{OH}	Output Hold from Addresses, $\overline{OE1}$, OE2 or $\overline{OE3}$, Whichever Occurred First	$\overline{OE1}$ = $\overline{OE3}$ = V_{IL} OE2 = V_{IH}	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.0V to 3.0V
Output Load (Note 9)	R = 97.6Ω C_L = 30 pF
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V



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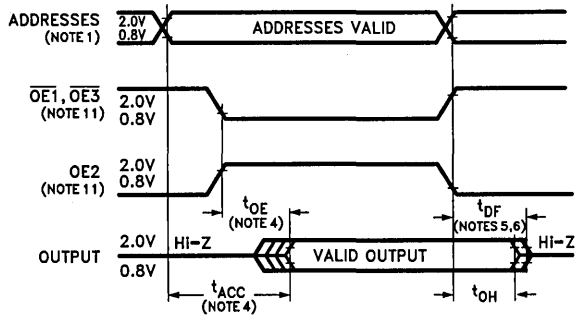
AC Waveforms (Notes 7, 8 & 11)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = 25°C$ and normal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: OE/$\overline{OE}$ true may be delayed up to $t_{ACC} - t_{OE}$ after address change without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 6: TRI-STATE may be attained by any OE signal.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 9: C_L: 30 pF includes fixture capacitance.

Note 10: Inputs can undershoot −2.0V for a maximum of 20 ns.

Note 11: For the output to be in Low-Z all OE/$\overline{OE}$ inputs must be in their logical true states, i.e., $\overline{OE1}$, $\overline{OE3}$ must be at V_{IL} and OE2 must be at V_{IH}. If any or all of these inputs are not at their logical true level then the outputs will be in Hi-Z.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	OE2 Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		50	ns
t_{PW}	Program Pulse Width		95	100	105	μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	OE2 = V_{IL}			60	mA
I_{CC}	V_{CC} Supply Current				60	mA
t_{VM1}	$\overline{OE3}$ to Data Valid (Verify Mode1)	$\overline{OE1}/V_{PP}$ = V_{PP}, OE2 = V_{IH}			0.1	μs
t_{VM2}	OE2 to Data Valid (Verify Mode2)	$\overline{OE1}/V_{PP}$ = V_{PP}, $\overline{OE3}$ = V_{IL}			0.1	μs
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

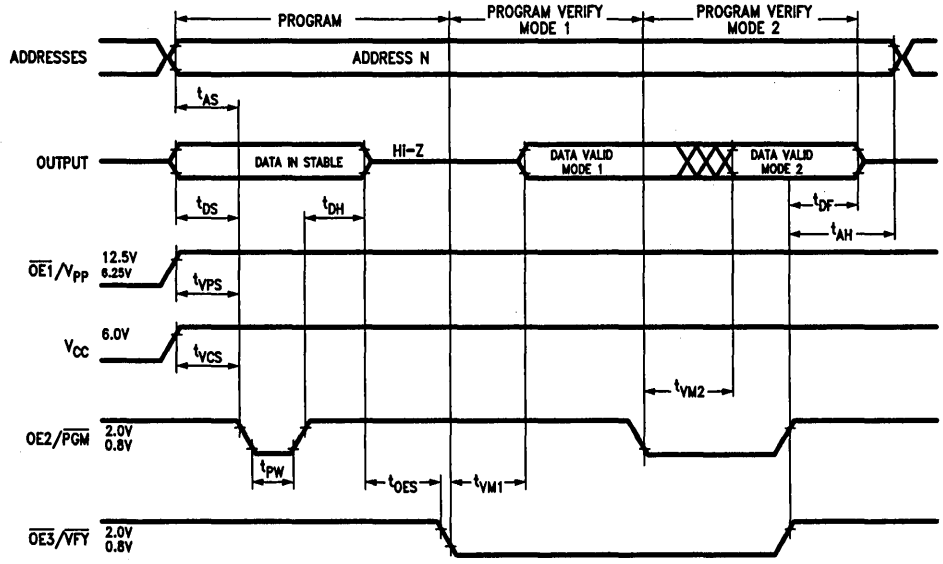
Note 1: National's standard product warranty applies only to devices programmed to the specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C53 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

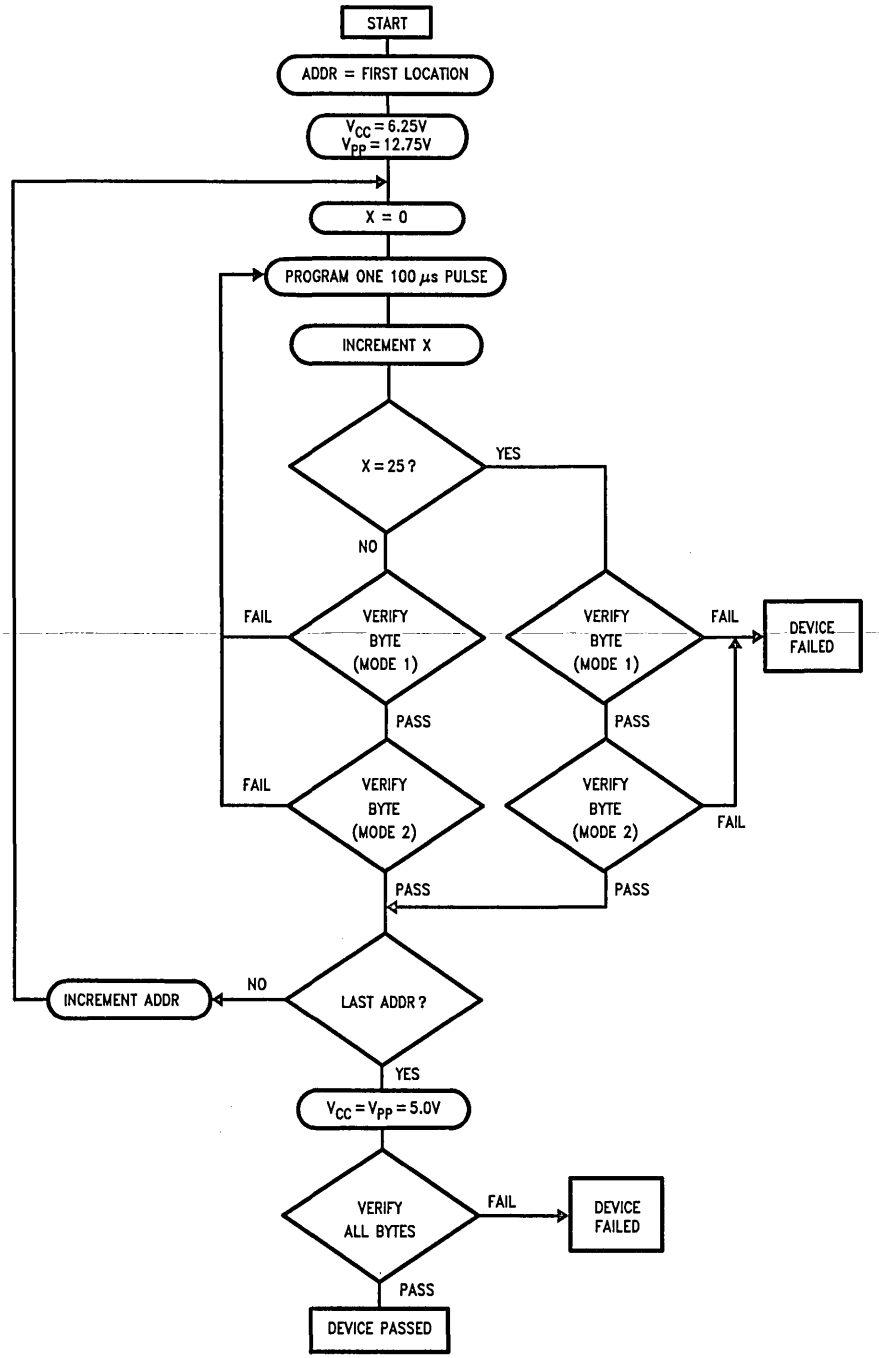
Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not tested or guaranteed.

Programming Waveforms (Note 3)



TL/D/9718–5

Fast Programming Algorithm Flow Chart



TL/D/9718-6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C53 are listed in Table I. It should be noted that all inputs for the six modes may be at TTL levels. The power supplies required are V_{PP} and V_{CC}. The V_{CC} power supply must be at 6.25V during the four programming modes, and at 5V in the other two modes. The $\overline{OE1}/V_{PP}$ pin must be at 12.75V in the programming and verify mode, and V_{IL} in the read mode.

READ MODE

The NMC27C53 has three select functions, both of which must be logically active in order to obtain data at the outputs. Data is available at the falling edges of $\overline{OE1}$ and $\overline{OE3}$ and the rising edge of OE2, assuming that the addresses have been stable for at least $t_{ACC}-t_{OE}$. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the specified voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

OUTPUT OR-TYING

Because NMC27C53s are usually used in larger memory arrays, National has provided a 3-line control function that accommodates this use of multiple memory connections. The 3-line control function allows for complete assurance that output bus contention will not occur. All Output Enables are functionally equivalent.

PROGRAMMING

CAUTION: Exceeding 14V on pin 22 ($\overline{OE1}/V_{PP}$) will damage the NMC27C53.

The NMC27C53 has a new memory cell which contributes greatly to its speed. The cell has two transistors which supply data to two data lines. When programmed, one or the other of the two transistors is programmed. When accessed the memory cell will discharge one of the two data lines, providing a differential voltage. This differential signal is then applied through pass devices to a true differential sense amplifier.

Initially, all memory cells are totally unprogrammed. In an unprogrammed state both transistors source the same current through the data lines and thus no differential is produced. Because of this, any attempt to read data in the read mode from an unprogrammed device will result in arbitrary outputs.

The NMC27C53 is in the program mode when $\overline{OE1}/V_{PP}$ is raised to 12.75V.

During programming the OE2 pin functions as the $\overline{PGM}$ pin which controls the programming pulse width (t_{PW}) and the $\overline{OE3}$ pin functions as the $\overline{VFY}$ pin which is to be held at V_{IL} during program verify.

To verify that a device is totally blank, the verify mode must be entered. In the verify mode each transistor of the memory cell is checked against a reference cell. By toggling OE2 both transistors in the cell are checked. For a totally unprogrammed deviced in the verify mode all outputs will be at a "1" state for OE2 = V_{IH} and at a "0" state for OE2 = V_{IL}.

It is required that at least a 0.1 μF capacitor be placed across $\overline{OE1}/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed are applied 8 bits in parallel to the data output pins. The levels required for the address, clock, and data inputs are TTL.

When the addresses, clocks, and data are stable, an active low, TTL program pulse is applied to the OE2 input. A program pulse must be applied to each address location that is to be programmed. A memory cell has been completely programmed when data from both verify modes matches the input data. The NMC27C53 is programmed with the fast programming algorithm shown in *Figure 1*. Each address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC27C53 must not be programmed with a DC signal applied to the OE2 input.

Programming multiple NMC27C53s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C53s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$/OE2 input (with $\overline{OE3}$ high) programs the paralleled NMC27C53s.

PROGRAM INHIBIT

Programming multiple NMC27C53s in parallel with different data is also easily accomplished. Except for OE2 all like inputs (including $\overline{OE1}/V_{PP}$ and $\overline{OE3}$) of the paralleled NMC27C53s may be in common. A TTL low level applied to an NMC27C53s OE2/$\overline{PGM}$ input (with the other control pins at the appropriate levels) will program that NMC27C53 while keeping the same pin high on the others inhibits programming.

TABLE I. Mode Selection

Mode \ Pins	$\overline{OE1}/V_{PP}$ (22)	OE2/$\overline{PGM}$ (21)	$\overline{OE3}/\overline{VFY}$ (20)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IH}	V_{IL}	5V	D_{OUT}
Program	12.75V	V_{IL}	V_{IH}	6.25V	D_{IN}
Program Verify (Mode 1)	12.75V	V_{IH}	V_{IL}	6.25V	D_{OUT} (V_{OH} if Blank)
Program Verify (Mode 2)	12.75V	V_{IL}	V_{IL}	6.25V	D_{OUT} (V_{OL} if Blank)
Program Inhibit	12.75V	V_{IH}	V_{IH}	6.25V	Hi-Z
Deselect	V_{IH}	V_{IL}	V_{IH}	5V	Hi-Z

Functional Description (Continued)

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. Verifying in the read mode may not ensure that the bits have been programmed with adequate margins. To guarantee adequate margins the device should be verified in the verify mode. In this mode each transistor of the memory cell is checked against a reference cell. Verify mode is entered with $\overline{OE1}/V_{PP}$ at 12.75V and $\overline{OE3}/V_{IL}$ with OE2 at V_{IH}, the data read for verify mode 1, and at $OE2/\overline{PGM} = V_{IL}$, verify mode 2. The data read in both modes must be the same as the expected data for a completely programmed cell.

Manufacturer's Identification Code

The NMC27C53 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is sorted in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C53 is "83C4", where "83" designates that it is made by National Semiconductor, and "C4" designates it is a 256k part.

The code is accessed by applying 12V ±0.5V to address pin A13. Addresses A1–A8, A10–A12, A14, $\overline{OE1}$, OE2 and $\overline{OE3}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Erasure Characteristics

The erasure characteristics of the NMC27C53 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C53's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C53 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C53 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C53 erasure time for various light intensities. An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.)

Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete ereaure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of devices. The supply current, I_{CC}, has two segments that are of interest to the system designer—the active current level and the transient current peaks that are produced by voltage transitions on the input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	0	0	1	1	83
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

TABLE III. Minimum NMC27C53 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

DM77/87SR474
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR474 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR474 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

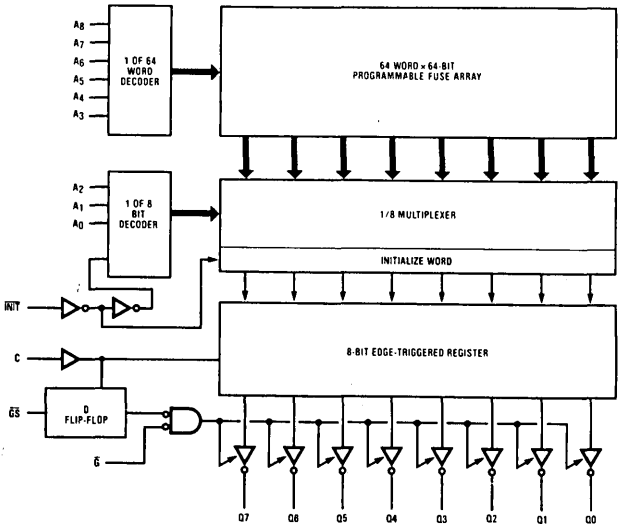
The DM77/87SR474 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows, providing a $\overline{CLEAR}$ function when not programmed.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable synchronous register INITIALIZE
- 24-pin, 300 mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Pinout compatible with DM77SR181 (1k x 8) Registered PROM for future expansion

Block Diagram



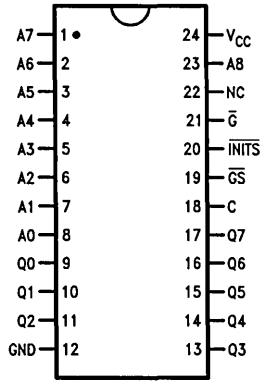
TL/D/9201–1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INIT}$	Initialize
NC	No Connection
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line-Package

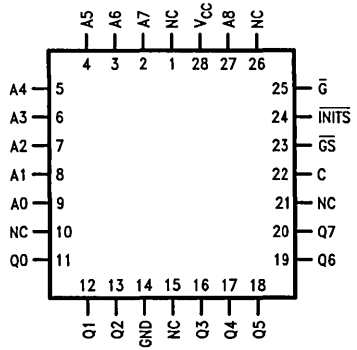


TL/D/9201–2

Top View

Order Number DM77/87SR474J, 474BJ
DM87SR474N, 474BN
See NS Package Number J24A or N24A

Plastic Chip Carrier (PLCC)



TL/D/9201–3

Top View

Order Number DM87SR474V, 474BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM87SR474BJ	35
DM87SR474J	50
DM87SR474BN	35
DM87SR474N	50
DM87SR474BV	35
DM87SR474V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM77SR474BJ	40
DM77SR474J	55

4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR474	55	20		50	20		ns
		SR474B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{INITS}$ to C (High) Setup Time		30	20		25	20		ns
$t_{H(\overline{INITS})}$	$\overline{INITS}$ to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR474		15	30		15	27	ns
		SR474B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Output Active (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Active (High or Low)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Output Inactive (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Inactive (TRI-STATE)			15	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR476
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

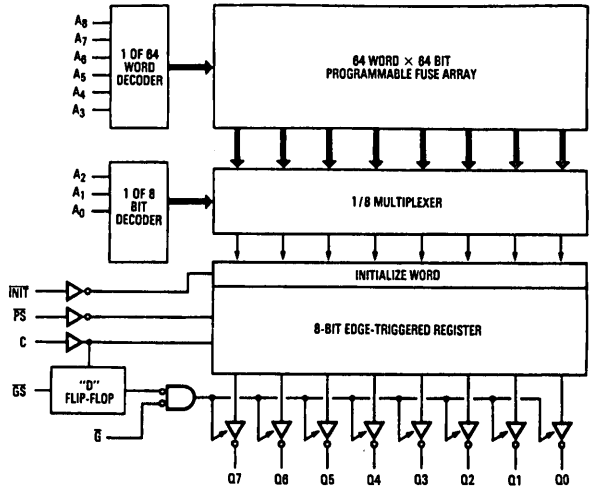
The DM77SR476 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows $\overline{PS}$ loads ones into the output registers when brought low.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S25
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameter's guaranteed over temperature
- Preset input

Block Diagram



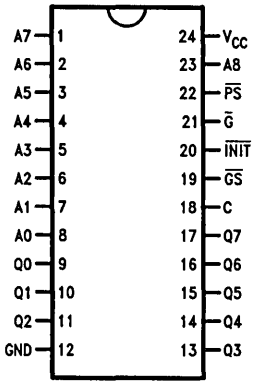
TL/D/9202–1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INIT}$	Initialize
$\overline{PS}$	Preset
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagrams

Dual-In-Line Package

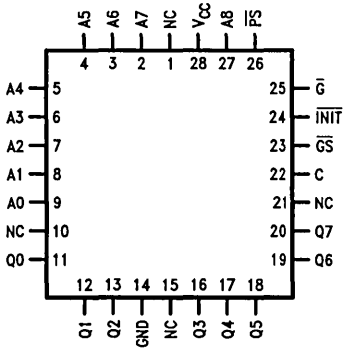


TL/D/9202-2

Top View

Order Number DM77/87SR476J, 476BJ, DM87SR476N or 476BN
See NS Package Number J24A or N24A

Plastic Chip Carrier (PLCC)



TL/D/9202-3

Top View

Order Number DM87SR476V or 476BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM87SR476BJ	35
DM87SR476J	50
DM87SR476BN	35
DM87SR476N	50
DM87SR476BV	35
DM87SR476V	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM77SR476BJ	40
DM77SR476J	55

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD to be determined

Note 1: Absolute Maximum Ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR476, 476B			DM87SR476, 476B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurements, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR476, 476B			DM87SR476, 476B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR476	55	20		50	20		ns
		SR476B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR476		15	30		15	27	ns
		SR476B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{PS})}$	Delay from $\overline{PS}$ (Low) to Output (High)			20	40		20	30	ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	40		20	30	ns
$t_{WL(\overline{PS})}$	$\overline{PS}$ Pulse Width (Low)		15	10		15	10		ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		15	10		15	10		
$t_{S(\overline{PS})}$	$\overline{PS}$ Recovery (High) to C (High)		25	10		20	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to C (High)		25	10		20	10		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZL(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR27
(512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR27 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

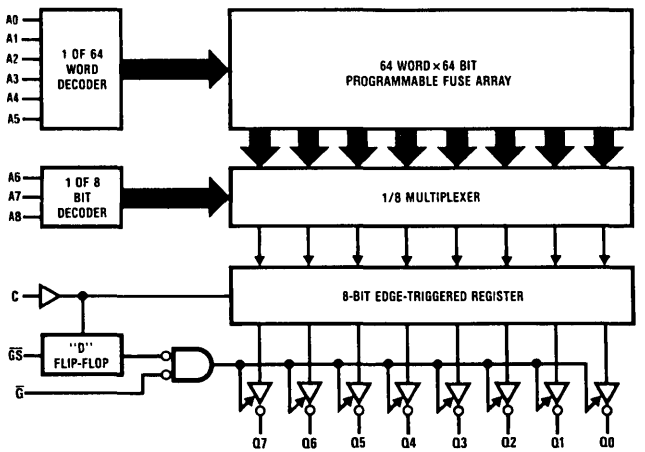
Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with Am27S27
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 22-pin 400-mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



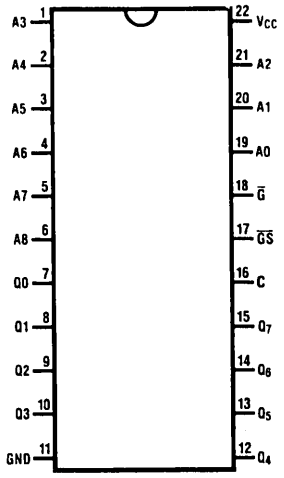
TL/D/6686–1

Pin Names

A0–A8	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
Q0–Q7	Outputs
V_{CC}	Power Supply

Connection Diagram

Dual-In-Line Package



Top View

TL/D/6686–2

Order Number DM77/87SR27J, DM77/87SR27BJ, DM87SR27N or DM87SR27BN
See NS Package Number J22A or N22A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM87SR27BJ	35
DM87SR27J	50
DM87SR27BN	35
DM87SR27N	50

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to C Setup Time (ns)
DM77SR27BJ	40
DM77SR27J	55

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 1)	−0.5V to +7.0V
Input Voltage (Note 1)	−1.2V to +5.5V
Output Voltage (Note 1)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operations should be limited to those conditions specified under DC Electrical Characteristics.

Operating Conditions

Supply Voltage (V_{CC})	
Military	4.5V to 5.5V
Commercial	4.75V to 5.25V
Ambient Temperature (T_A)	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Logical "0" Input Voltage	0V to 0.8V
Logical "1" Input Voltage	2.0V to 5.5V

DC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise specified

Symbol	Parameter	Test Conditions	DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR27	55	20		50	20		ns
		SR27B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR27		15	30		15	27	ns
		SR27B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		25	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Programming Parameters Do not test or you may program the device

Symbol	Parameter	Test Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current While Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4	4.2	V
V_{CCVH}	Required High V_{CC} for Verification		5.8	6	6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Functional Description

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

Functional Description (Continued)

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

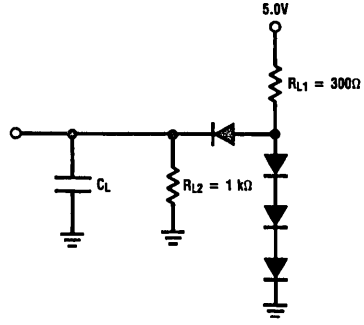
DM77/87SR27 Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at ambient temperatures between 15 and 30 degrees Celsius.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedures must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. Synchronous chip Enable $\overline{GS}$ should be held low throughout the entire programming procedure.
   b) Increase V_{CC} from nominal 10.5V (±0.5V) with a slew rate between 1.0 V/μs and 10 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 V/μs to 10 V/μs. This voltage may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time.)
   d) Enable the device by taking the chip Enable $\overline{G}$ to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through e for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enable device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

AC Test Load



TL/D/6686–3

National Semiconductor

DM77/87SR181
(1024 x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This device is organized as 1024-words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

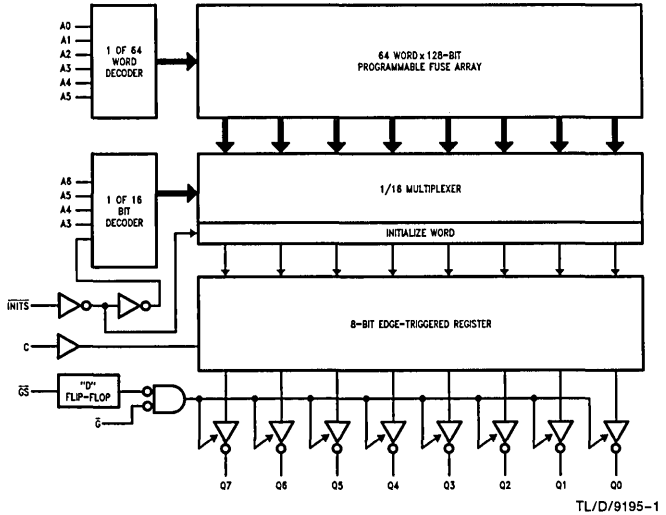
The DM77/87SR181 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register initialize
- 24-pin, 300 mil package
- 40 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



TL/D/9195–1

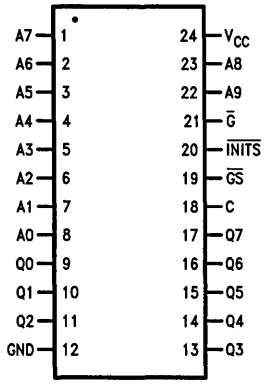
Pin Names

A0–A9	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INITS}$	Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

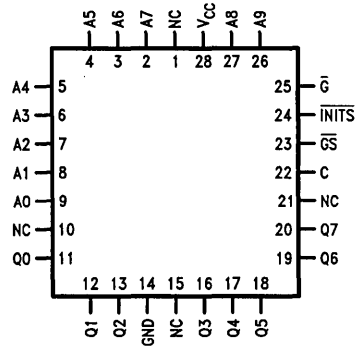


TL/D/9195-2

Top View

Order Number DM77/87SR181J or DM87SR181N
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9195-3

Top View

Order Number DM87SR181V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number
DM87SR181J
DM87SR181N
DM87SR181V

Military Temp Range (−55°C to +125°C)

Parameter/Order Number
DM77SR181J

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD rating to be determined.

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at those values.

Note 2: These limits do not apply during programming. For the programming settings, refer to the programming instructions.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	175		115	175	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	C_L = 30 pF	50	20		40	20		ns
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{INITS}$ to C (High) Setup Time		35	20		30	20		ns
$t_{H(\overline{INITS})}$	$\overline{INITS}$ to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)			15	30		15	20	ns
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		15	0		15	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)	C_L = 30 pF		20	30		20	25	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)	C_L = 5 pF (Note 1)		20	30		20	25	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Note: All typical values are for V_{CC} = 5V, T_A = 25°C.

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR183
(1k x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR183 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 1024 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR183 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

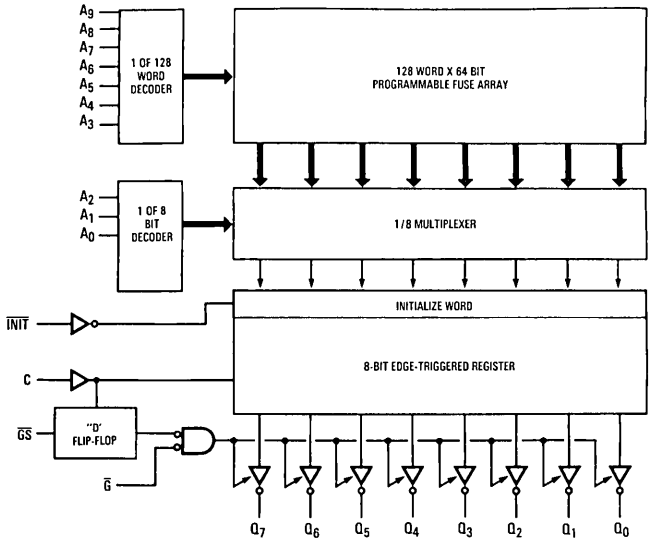
The DM77/87SR183 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S35
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



TL/D/8351–1

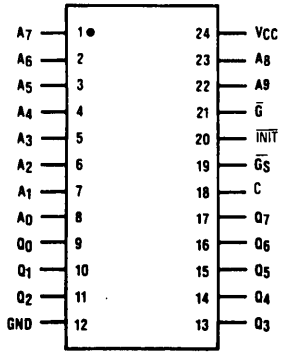
Pin Names

A0–A9	Addresses
C	Clock
$\overline{G}$	Output Enable
GND	Ground
$\overline{GS}$	Synchronous Output Enable
$\overline{INIT}$	Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

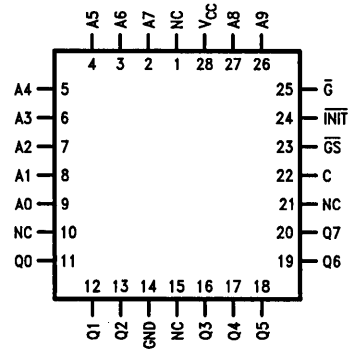


TL/D/8351-2

Top View

Order Number DM77/87SR183J, 183BJ, DM87SR183N or 183BN
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/8351-8

Top View

Order Number DM87SR183V or 183BV
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM87SR183BJ	35
DM87SR183J	40
DM87SR183BN	35
DM87SR183N	40
DM87SR183BV	35
DM87SR183V	40

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM77SR183BJ	40
DM77SR183J	45

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD rating to be determined	

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		135	185		135	185	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	SR183	45	20		40	20		ns
		SR183B	40	20		35	20		
$t_{H(A)}$	Address to C (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)	SR183		15	30		15	25	ns
		SR183B		15	25		15	20	
$t_{WH(C)}$ $t_{WL(C)}$	C Width (High or Low)		20	10		15	10		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time		15	0		15	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	35		20	30	ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		30	10		25	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to C (High)		20	10		20	10		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			20	35		20	30	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metallization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR191 (2k x 8) 16k-Bit Registered TTL PROM

General Description

The DM77/87SR191 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 2k words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR191 also offers maximum flexibility for memory expansion and data bus control by providing either synchronous or asynchronous output enables. When using the asychronous chip select function, all outputs will go "OFF" when $\overline{G}$ is held high. The output will be enabled when $\overline{G}$ is held low. When architecturally programmed to synchronous chip select, all outputs will go "OFF" synchronous to the clock if $\overline{GS}$ is held high before the rising edge of the clock. The output will synchronously be enabled if held low before the rising edge of the clock. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A10. During the set-up time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

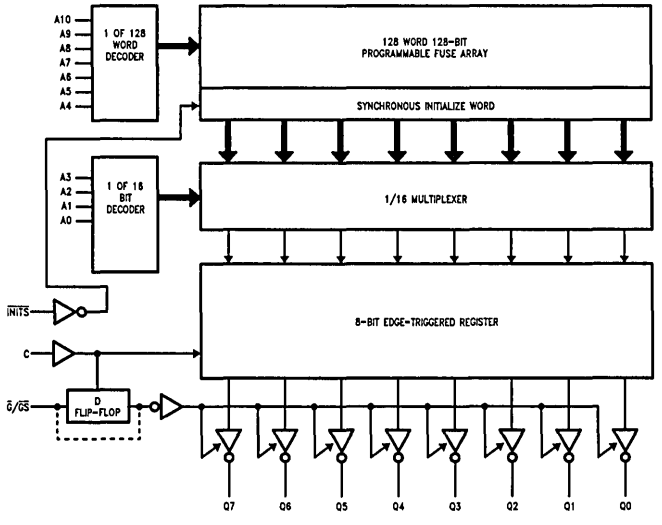
The DM77SR191 also features an initialize $\overline{INITS}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INITS}$. With the synchronous initialize function of the SR191, the initialize word is loaded into the master flip-flop when $\overline{INITS}$ is brought low and appears on the output during the rising edge of the clock. The unprogrammed state of the initialize word is all lows.

The function of chip select is shipped from the factory as an asynchronous $\overline{G}$ function and must be architecturally programmed to perform the synchronous function, $\overline{GS}$.

Features

- SR191 functionally compatible with AM27S47
- On-chip, edge-triggered registers.
- Architecturally programmable asynchronous/synchronous chip select.
- Single pin INITIALIZE
- 24-pin, 300 mil thin-dip package.
- 25 ns addresses setup and 15 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



TL/D/5512–1

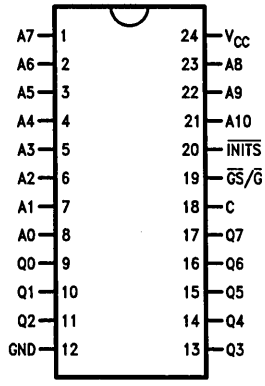
Pin Names

A0–A10	Addresses
C	Clock
GND	Ground
$\overline{GS}/\overline{G}$	Synchronous Output Enable
$\overline{INITS}$	Synchronous Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package

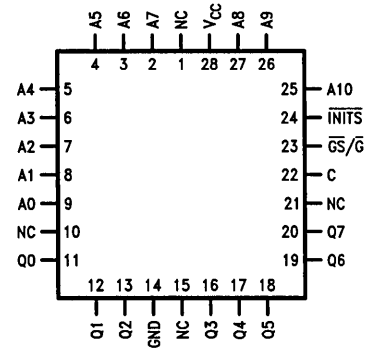


TL/D/5512-2

Top View

Order Number DM77/87SR191J or DM87SR191N
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/5512-3

Top View

Order Number DM87SR191V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM87SR191J	18
DM87SR191N	18
DM87SR191V	18

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time
DM77SR191J	25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (10 seconds)	300°C

ESD rating to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR191			DM87SR191			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		140	190		140	190	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	DM77SR191			DM87SR191			Units
		Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	25	12		18	12		ns
$t_{H(A)}$	Address to C (High) Hold Time	0	−3		0	−3		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)		6	15		6	10	ns
$t_{WH(C)}$	Clock Width High	8	3		5	3		ns
$t_{WL(C)}$	Clock Width Low	12	6		9	6		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time (Note 5)	15	2		10	2		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Time (Note 5)	5	−2		5	−2		ns
$t_{H(\overline{INITS})}$	$\overline{INITS}$ to C (High) Hold Time		−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{INITS}$ to C (High) Setup Time	15	5		15	5		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low) (Note 5)		6	20		6	15	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High) (Note 6)		6	20		6	15	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE) (Note 5)		6	20		6	15	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE) (Note 6)		6	20		6	15	ns

Note 5: Applies only when asynchronous ENABLE ($\overline{GS}$) function is used.

Note 6: Applies only when synchronous ENABLE ($\overline{G}$) function is used.

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To data, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti-W) fuse links designed to program efficiently with only 10.5V applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

DM77/87SR193
(2k x 8) 16k-Bit Registered TTL PROM

General Description

The DM77/87SR193 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 2k words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR193 also offers maximum flexibility for memory expansion and data bus control by providing either synchronous or asynchronous output enables. When using the asynchronous chip select function, all outputs will go "OFF" when $\overline{G}$ is held high. The output wil be enabled when $\overline{G}$ is held low. When architecturally programmed to synchronous chip select, all outputs will go "OFF" synchronous to the clock if $\overline{GS}$ is held high before the rising edge of the clock. The output will synchronously be enabled if held low before the rising edge of the clock. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A10. During the set-up time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

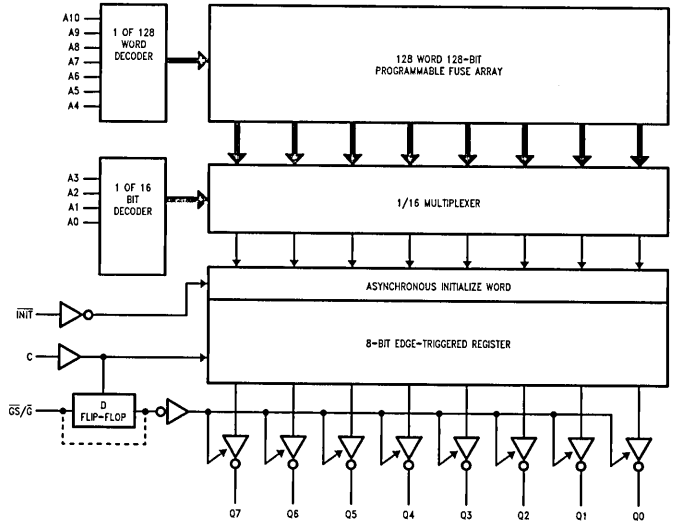
The DM77SR193 also features an initialize $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. When using the asynchronous initialize SR193, the initialize word is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the initialize word is all lows.

The function of chip select is shipped from the factory as an asynchronous $\overline{G}$ function and must be architecturally programmed to perform the synchronous function, $\overline{GS}$.

Features

- SR193 compatible with AM27S45
- On-chip, edge-triggered registers
- Architecturally programmable asynchronous/synchronous chip select
- Single pin INITIALIZE
- 24 pin, 300 mil thin-DIP package
- 25 ns addresses setup and 15 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



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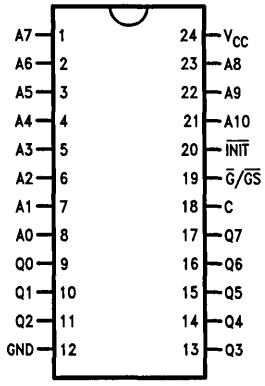
Pin Names

A0–A10	Addresses
C	Clock
$\overline{G}/\overline{GS}$	Output Enable
GND	Ground
$\overline{INIT}$	Initialize
Q0–Q7	Outputs
V_{CC}	Power Supply

4

Connection Diagrams

Dual-In-Line Package



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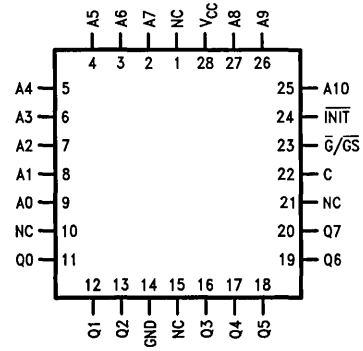
Top View

Order Number DM77/87SR193J, 193N
See NS Package Number J24A or N24A

Plastic Leaded Chip Carrier (PLCC)



TL/D/9711-3

Top View

Order Number DM87SR193V
See NS Package Number V28A

Ordering Information

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM87SR193J	18
DM87SR193N	18
DM87SR193V	18

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Min Address to CLK Setup Time (ns)
DM77SR193J	25

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

ESD rating to be determined

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR193			DM87SR193			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		140	190		140	190	mA
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	DM77SR193			DM87SR193			Units
		Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to C (High) Setup Time	25	12		18	12		ns
$t_{H(A)}$	Address to C (High) Hold Time	0	−3		0	3		ns
$t_{PHL(C)}$ $t_{PLH(C)}$	Delay from C (High) to Output (High or Low)		6	15		6	10	ns
$t_{WH(C)}$	C Width High	8	3		5	3		ns
$t_{WL(C)}$	C Width Low	12	6		9	6		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to C (High) Setup Time (Note 5)	15	2		10	2		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to C (High) Time (Note 5)	5	−2		5	−2		ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)		8	20		8	15	ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)	10	5		10	5		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (Low or High) to C (High) (Note 6)	15	6		15	6		ns
$t_{PZL(C)}$ $t_{PZH(C)}$	Delay from C (High) to Active Output (High or Low) (Note 5)		6	20		6	15	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High) (Note 6)		6	20		6	15	ns
$t_{PLZ(C)}$ $t_{PHZ(C)}$	Delay from C (High) to Inactive Output (TRI-STATE) (Note 5)		6	20		6	15	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE) (Note 6)		6	20		6	15	ns

Note 5: Applies only when asynchronous ENABLE ($\overline{GS}$) function is used.

Note 6: Applies only when synchronous ENABLE ($\overline{G}$) function is used.

Functional Description

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti-W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti-W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

TITANIUM-TUNGSTEN FUSES

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A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5V, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

National Semiconductor

Bipolar PROM Devices in Plastic Leaded Chip Carriers (PLCC)

Introduction of Surface Mount Technology

Recent years have seen rapid advances in microcircuit technology. The integrated circuits of the 1980's are more complex than the circuit boards of the 1960's. It is evident that the next decade will bring demands for packages with higher lead counts and closer lead spacing, both to support the greater system density sought by designers.

National Semiconductor Corporation is committed to surface mount devices, for they provide the most practical solution to these needs. Geared to development of high-complexity semiconductor chips National has placed great emphasis on package development and introducing plastic leaded chip carriers with various number of leads as surface mounted components.

Features of Surface Mount Devices

Surface mount devices have additional features compared to molded Dual-In-Line Packages (DIP):

1. Compact design that saves space during assembly.
2. Mounting on both sides of the substrate.
3. Easier handling and excellent reliability.
4. Automation of the assembly process.
5. Lower board manufacturing costs.
6. Improved operating speed.
7. Increased board density and reduced weight.

Applications

Surface mount devices can be used where substrate size, as well as weight and thickness are limited. The surface mount device can also be used in areas where conventional packages cannot be used. Areas of application include; portable video cassette recorders, video cameras, hand-held computers, personal computers, electronic toys, car electronics, cameras, telephones, and various telecommunication equipment.

Products in PLCC

National Semiconductor has a broad Family of high performance PROMs. All the PAL and PROM products presently offered in DIP packages will now be available in the PLCC (plastic leaded chip carrier) package including the 15 ns industries fastest PAL.

Advantages of PLCC

1. Permits automated assembly.
2. Lower manufacturing costs.
3. Smaller PLCC size, reduces board density and weight.
4. Lower noise and improved frequency response resulting from shorter circuit paths. Automated assembly ensures accurate component placement which improves reliability and provides more consistent product quality.

Additional Information

National Semiconductor offers a variety of technical briefs covering surface mount topics. These include:

STAR™ Tape-and-Reel Shipping System
Order Number 113635

Getting Started in Surface Mount (Equipment Suppliers)
Order Number 570435

A Basic Guide to Surface Mounting of Electronic Components
Order Number 113615

Reliability Report: Small Outline Packages
Order Number 570430

Reliability Report: Plastic Chip Carrier
Order Number 980040

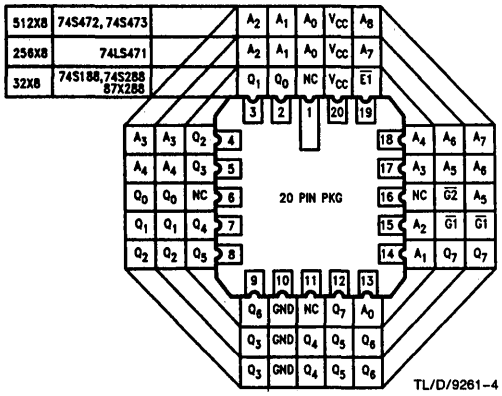
Surface Mount Technology Notebook
Order Number 980020

Plastic Chip Carrier Technology
Order Number 113295

PROM

Series-20 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S188 OC DM74S288 TS	256	32 × 8	35	25	—	110	16	20
PL87X288 TS	256	32 × 8	—	—	15	140	16	
DM74S287 TS DM74S387 OC	1K	256 × 4	50	30	—	130	16	
DM74S570 OC DM74S571 TS	2K	512 × 4	55 55	45 45	— 35	130	16	
DM74LS471 TS	2K	256 × 8	60	—	—	100	20	
DM74S572 OC DM74S573 TS	4K	1,024 × 4	60 60	45 45	— 35	140 140	18 18	
DM74S472 TS DM74S473 OC	4K	512 × 8	60 55	45 45	35 —	155 155	20 20	
DM87S184 OC DM87S185 TS	8K	2048 × 4	55 55	45 45	— 35	140 140	18 18	



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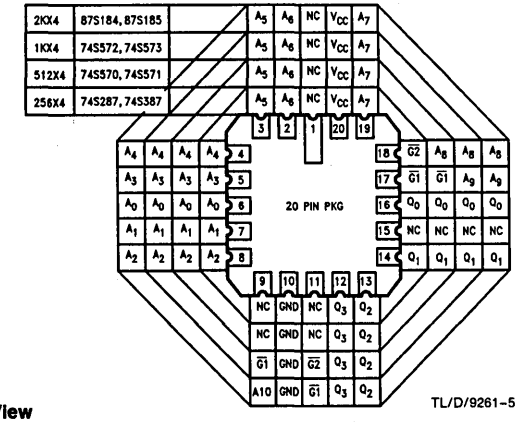

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Top View

Series-24 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PLCC pins
			STD	A-Series	B-Series			
DM74S474 TS DM74S475 OC	4K	512 × 8	65	45	35	170	24	28
DM87SR474 REG DM87SR476 REG	4K	512 × 8	50*	—	35*	170	24	
DM87S180 OC DM87S181 TS DM87SR181 REG DM87SR183 REG	8K	1024 × 8	55 55 40* 40*	— 45 — 35*	— — — —	170	24	
DM87SR191 REG DM87SR193 REG	16K		25* 25*	— —	— —			

*setup time

Plastic Leaded Chip Carrier

1KX8	87S180, 87S181
512X8	74S474, 74S475

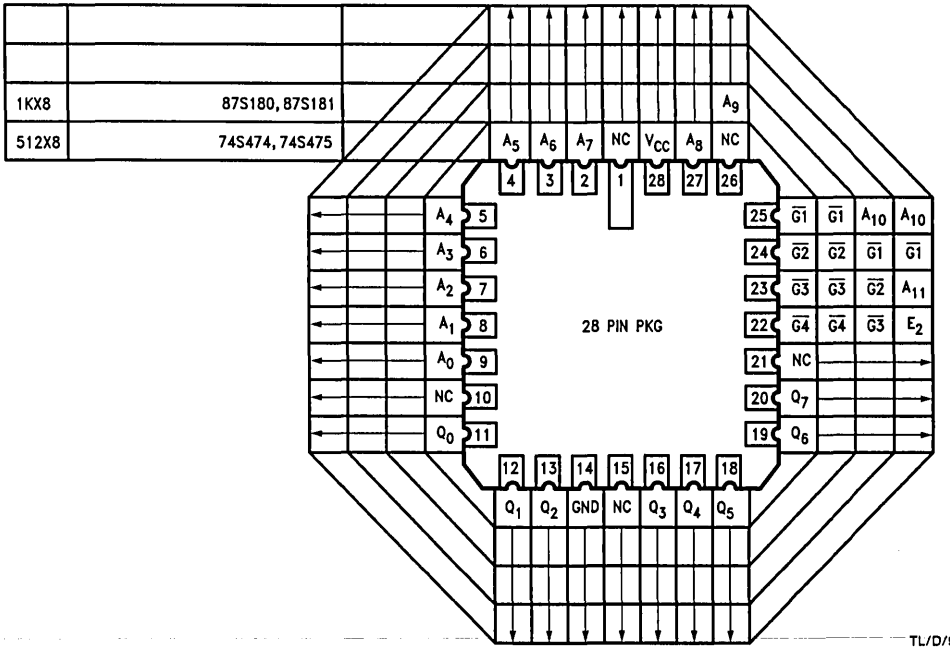

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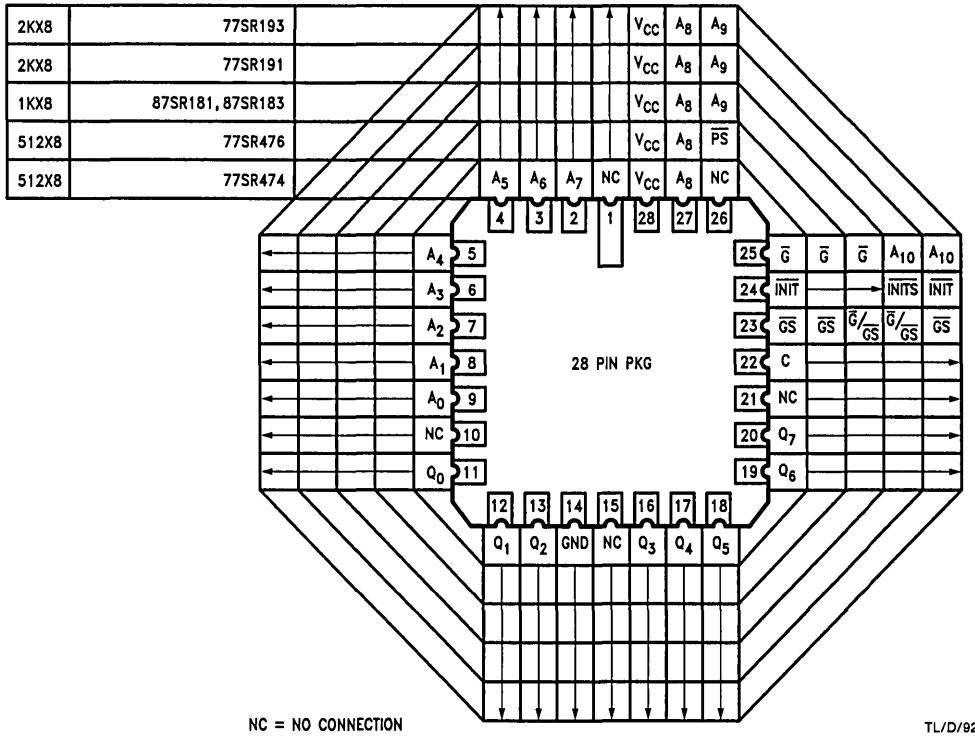
FIGURE 5. Bipolar PROM Pinout

Plastic Leaded Chip Carrier

2KX8	77SR193
2KX8	77SR191
1KX8	87SR181, 87SR183
512X8	77SR476
512X8	77SR474



NC = NO CONNECTION

TL/D/9261-7

FIGURE 6. Bipolar Registered PROM Pinout

4

Programming Support

PROM devices may be programmed with hardware and software readily available in the market. Most programmer manufacturers will offer a PLCC adapter which will fit in existing equipment. For the availability of PLCC adapter please check with your programmer manufacturer.

Programming Equipment

1. Data I/O
2. Structured Design
3. Stag
4. Dig Elec
5. Kontron
6. Prolog
7. Citel

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T_1 = 100 ns Min.

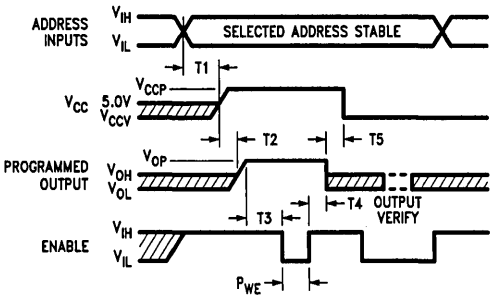
T_2 = 5 μs Min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})

T_3 = 100 ns Min.

T_4 = 100 ns Min.

T_5 = 100 ns Min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.



NOTE: ENABLE WAVEFORM FOR AN ACTIVE LOW ENABLE. SOME PROMS HAVE MORE THAN ONE CHIP ENABLE. HOLD ALL OTHER ENABLE(S) TO ACTIVE STATE(S).

TL/00/2506-1

Registered PROM Programming Procedure

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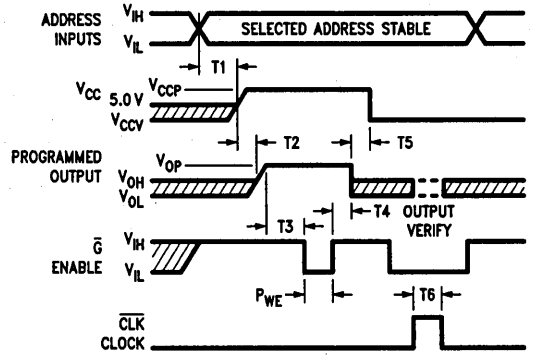
1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. $\overline{GS}$ is held low during the entire programming time.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable ($\overline{G}$) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) The initialize word is programmed by setting $\overline{INIT}$ input to a logic low and programming the initialize word output by output in the same manner as any other address. This can be accomplished by inverting the highest order address input from the PROM programmer and applying it to the $\overline{INIT}$ input.
   g) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   h) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVH}	Required High V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCVL}	Required Low V_{CC} for Verification*		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

*See DM87SR191/193 and DM77SR191/193 for correct voltage.

Programming Waveforms Registered PROM

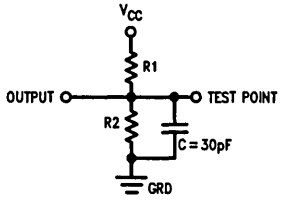


TL/00/2506-2

T_1 = 100 ns Min.
T_2 = 5 μs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)
T_3 = 100 ns Min.
T_4 = 100 ns Min.
T_5 = 100 ns Min.
T_6 = 50 ns Min.

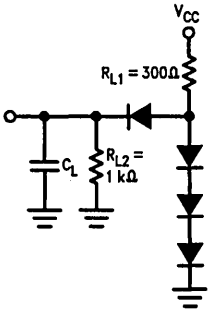
Standard Test Loads

Non-Registered PROMs



TL/00/2506-3

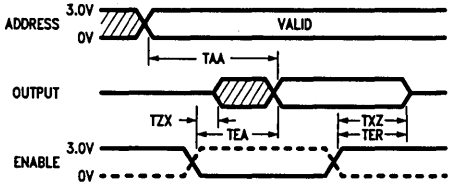
Registered PROMs



TL/00/2506-8

Switching Time Waveforms

Non-Registered PROM



TL/00/2506-4

*Device input waveform characteristics are;
Repetition rate = 1 MHz
Source impedance = 50Ω
Rise and Fall times = 2.5 ns max.
(1.0 to 2.0 volt levels)

*TAA is measured with stable enable inputs.

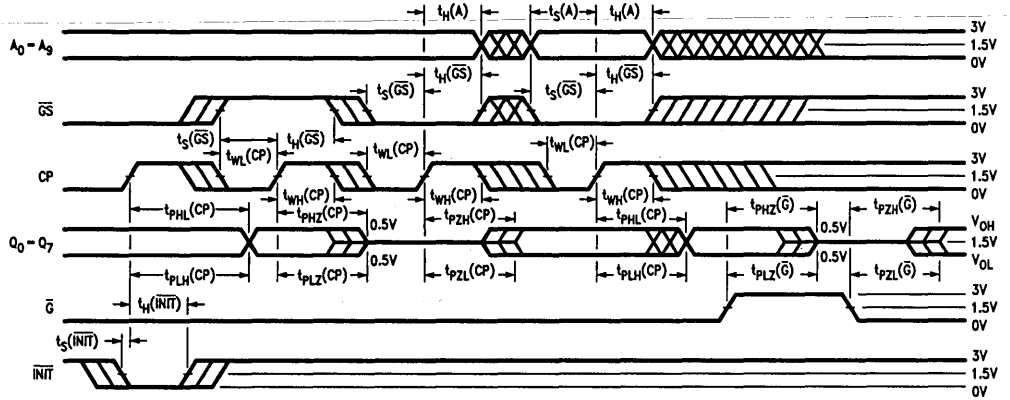
*TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.

*For I_{OL} = 16 mA, R1 = 300Ω and R2 = 600Ω

*for I_{OL} = 12 mA, R1 = 400Ω and R2 = 800Ω.

*"C" includes scope and jig capacitance.

Switching Waveforms Registered PROM



TL/00/2506-5

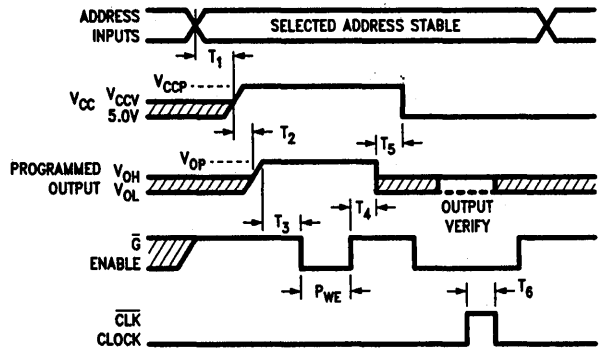
Key To Timing Diagram

Waveform	Inputs	Outputs	Waveform	Inputs	Outputs
	Must Be Steady	Will Be Steady		Don't Care: Any Change Permitted	Changing: State Unknown
	May Change from H to L	Will Be Changing from H to L		Does Not Apply	Center Line Is High Impedance "OFF" State
	May Change from L to H	Will Be Changing from L to H			

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8 5.8	4.0 6.0	4.2 6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM



TL/00/2506-9

T_1 = 100 ns Min.
T_2 = 5 μs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)
T_3 = 100 ns Min.
T_4 = 100 ns Min.
T_5 = 100 ns Min.
T_6 = 50 ns Min.

Approved Programmers for NSC PROMs

Manufacturer	System #
DATA I/O	5/17/19/29A
PRO-LOG	M910,M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C Parametric and Functionality	25°C	0.05	D.C Parametric and Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

Isoplanar-Z Junction Fuse Principles and Programming

National Semiconductor
Application Note 525

Conventional fusible link bipolar PROMs and programmable logic devices are based upon two dimensional matrices of electrically conductive thin film fusible elements of materials such as nichrome, titanium tungsten, platinum silicide or polysilicon. Each of these thin film technologies has its own unique advantages and disadvantages but all have in common the fact that fuses lie flat on the surface of the silicon and therefore occupy a significant portion of silicon area. Cell area has become increasingly important as device densities have grown from 4K to 64K. Manufacturing cost, yields and performance are all directly related to die size which is a strong function of cell area. Previously, reductions in cell area have been accomplished primarily through improvements in photolithographic techniques. Such techniques have been pushed to their limits to produce high density, cost effective programmable memories and logic. The need to shrink cell sizes, especially in higher density devices, is placing severe strains on the manufacturability of thin film fuses.

Junction fuses are the emerging solution to the inherent problems posed by thin film fuses. A junction fuse is simply a PN junction programmable cell. The emitter-base junction of a floating base NPN transistor acts as the fuse element. Because fuses are single vertical transistors (hence the often used name of vertical fuses), they occupy minimal silicon area. The entire fuse structure can essentially be modeled as two diodes connected back-to-back. Before programming, a high impedance (open) path exists between the emitter and collector. The emitter-base diode is reverse biased, preventing read currents from passing through the fuse. During programming, the emitter-base junction is shorted out, leaving a forward biased base-collector (B-C) diode. This diode now appears as a low impedance (closed) path. The fuse junction lies beneath the surface of the silicon so all of the potential thin film fuse related failure modes such as metal migration (growback), freeze out, corrosion, marginally opened fuses and passivation scattering have been eliminated.

The major problem encountered in early P–N junction programmable junction fuse development was the requirement of a large cell programming current (typically 200 mA per cell). This large current meant that large transistors were needed in the peripheral programming circuitry. The gain in array size reduction due to small cells was offset by the need for a larger peripheral programming circuitry which, in turn, translated to larger overall die size and higher die cost. The costs were such that, despite their reliability advantages, these devices were never widely commercially accepted.

The most straightforward method to achieve reductions in cell programming current is to use small emitter cells. A small emitter cell increases the effective current density at the emitter-base junction therefore decreasing the overall energy required to program the cell. To reduce emitter size and programming currents without the use of advanced photolithographic equipment, National adopted a simple solution, use a walled emitter cell and an oxide isolated Isoplanar process. With oxide isolation, emitter sizes are defined by the oxide opening and as a result are self aligned, easing manufacturing tolerances.

The main advantages of the Isoplanar-Z process are due to the use of oxide encroachment. The cell emitter is defined using standard photolithography. The surrounding oxide is then laterally grown, shrinking the emitter area and decreasing the effective cell size. Very small self aligned emitter-base junction areas can be achieved quite easily with the encroachment technique. An added benefit of oxide encroachment is that the higher thermal resistivity of the silicon dioxide which surrounds the cells, as compared to silicon, reduces heat loss during programming. This thermal insulation effect further reduces the current required to program a cell. Typical programming currents of 60 mA or below are easily achieved using the Isoplanar-Z process.

Results of reliability and programming yield testing have been excellent. Data have demonstrated typical programming yields in excess of 99% on a 16,384-bit PROM and no cell related failures in over 63 billon cell hours of life test.

PROGRAMMING A JUNCTION FUSE

Programming a junction fuse is accomplished by driving a controlled current through the emitter of the cell, inducing avalanche breakdown of the emitter-base junction. Heat locally generated at the reverse biased junction causes the Aluminum-Silicon interface to reach the Al-Si eutectic solidus (melting) temperature of approximately 575°C. The electrically conductive aluminum eutectic then diffuses down through the emitter to the emitter-base junction, forming a permanent short.

The amount of energy required to program a cell is dependent upon encroachment variations. Different methods can be used to supply the varying amount of energy required to program junction fuses. One method is a pulse-read technique, whereby a series of energy pulses of increasing magnitude or duration are applied to the cell. Each pulse applies a specific amount of energy to the cell's emitter-base junction, successively heating the junction until the cell emitter reaches the Aluminum-Silicon eutectic temperature. Once this temperature is reached, migration occurs and the junction shorts. A read is performed after each pulse to detect if the fuse has blown. If additional energy is needed to program any cell, more pulses are applied until the cell blows.

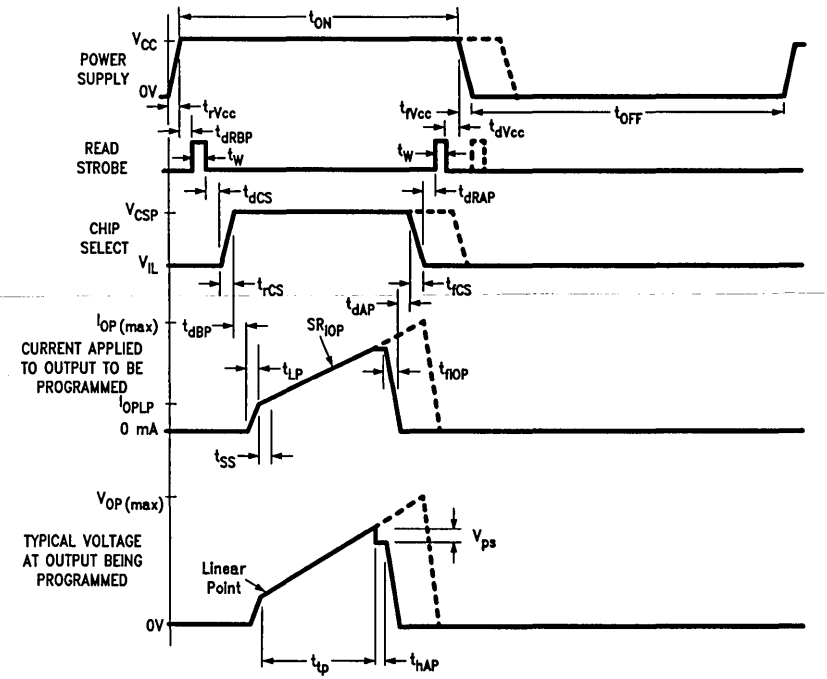
National has approved a current-pulse technique for users with digital requirements. In this method, differences in required programming energy are accounted for by increasing the current amplitude of each subsequent current pulse until programming is achieved. A read is performed after each pulse. This cycle is continued until the cell is programmed. Refer to the Programming Timing Diagram and Programming Specifications for Current-Pulse Programming.

National originally developed a self adjusting current ramp programming technique which delivers the optimum current needed to program each individual cell. With the self adjust-

ing technique a steadily increasing current ramp is applied to a cell until a shorted junction is detected. The exact moment when the junction actually shorts can be sensed by a sharp drop in the voltage across the cell. This voltage drop occurs because the reverse biases E-B diode is no longer in series with the programming path.

Once the moment of programming has been detected, National incorporates the use of a programming ramp "post hold time". The rise in programming current is halted at the level which was required to cause a blow, held for a precise time interval, and then turned off. This means that the amount of additional energy applied to a cell is totally governed by the amount of current required to program that cell, which is in turn dependent upon cell size. Therefore each cell's additional energy pulse is custom tailored for that specific cell. Experimental data shows that a carefully chosen post hold time can insure a very uniform cell resistance regardless of cell size. The self adjusting current ramp programming scheme allows consistent, repeatable programming and uniform cell resistance, overcoming any effects of process variations on a particular product or differences in cell sizes across product lines. Refer to the Programming Timing Diagram and Programming Specifications for Current-Ramp Programming.

CURRENT-RAMP PROGRAMMING TIMING DIAGRAM



TL/D/9670–1

CURRENT-RAMP PROGRAMMING SPECIFICATIONS (Note 4)

Symbol	Parameter	Characteristics	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Power Supply Voltage	Typical I_{CC} at 6.5V = 250 mA	6.4	6.5	6.6	V
$t_{r\,V_{CC}}$	Power Supply Rise Time (Note 3)		0.2	2.0		μs
$t_{f\,V_{CC}}$	Power Supply Fall Time		0.2	2.0		μs
t_{ON}	V_{CC} ON Time	See Programming Timing Diagram	(Note 1)			
t_{OFF}	V_{CC} OFF Time		(Note 2)			
	Duty Cycle for V_{CC}	$t_{ON}/(t_{OFF} + t_{ON})$			50	%
READ STROBE						
t_{dRBP}	Read Delay before Programming	Initial Check		3.0		μs
t_w	Fuse Read Time			1.0		μs
$t_{d\,V_{CC}}$	Delay to V_{CC} OFF			1.0		μs
t_{dRAP}	Delay to Read after Programming	Verify		3.0		μs
CHIP SELECT						
V_{CSP}	Chip Select Programming Voltage		20.0	20.0	22.0	V
I_{CSP}	Chip Select Program Current Limit		175	180	185	mA
V_{IL}	Input Voltage LOW		0	0	0.4	V
V_{IH}	Input Voltage HIGH		2.4	5.0	5.0	V
t_{dCS}	Delay to Chip Deselect			1.0		μs
t_{rCS}	Chip Select Pulse Rise Time		3.0	4.0		μs
t_{dAP}	Delay to Chip Select Time		0.2	1.0		μs
t_{fCS}	Chip Select Pulse Fall time		0.1	0.1	1.0	μs
CURRENT RAMP						
I_{OPLP}	Programming Current Linear Point	Point after Which the Programming Current Ramp Must Rise at a Linear Slew Rate		10	20	mA
$I_{OP\,(Max)}$	Output Programming Current Limit	Apply Current Ramp to Selected Output	155	160	165	mA
$V_{OP\,(Max)}$	Output Programming Voltage Limit		24	25	26	V
SR_{IOP}	Current Slew Rate	Constant after Linear Point	0.9	1.0	1.1	mA/μs
V_{PS}	Blow Sense Voltage		0.7			V
t_{dBP}	Delay to Programming Ramp	V_{CSP} Must be at Minimum	2.0	3.0		μs
t_{LP}	Time to Reach Linear Point		0.2	1.0	10	μs
t_{SS}	Program Sense Inhibit		2.0	3.0	10	μs
t_{tp}	Time to Program Fuse		3.0		150	μs
t_{hAP}	Programming Ramp Hold Time	After Fuse Programs	1.4	1.5	1.6	μs
t_{fIOP}	Program Ramp Fall Time			0.1	0.2	μs

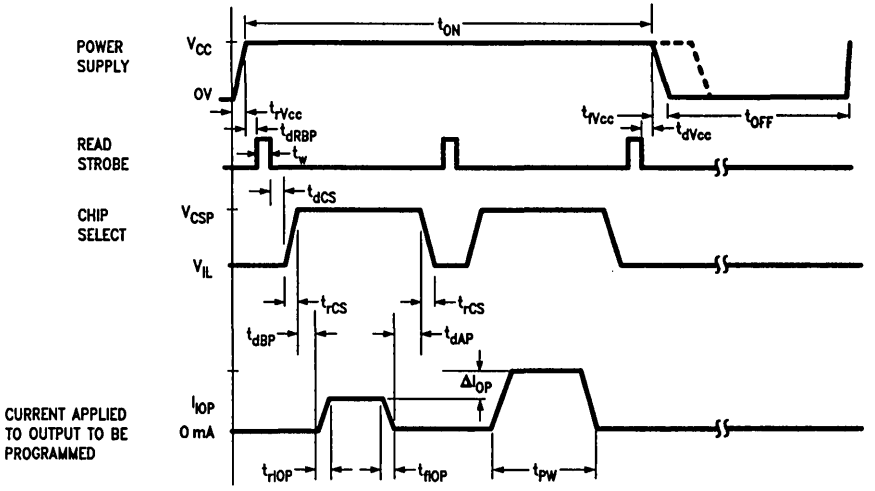
Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temperature T_C = +25°C ±10°C.

CURRENT-PULSE PROGRAMMING TIMING DIAGRAM



TL/D/9670–2

CURRENT-PULSE PROGRAMMING SPECIFICATIONS (Note 4)

Symbol	Parameter	Characteristics	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Power Supply Voltage	Typical I_{CC} at 6.5V = 250 mA	6.4	6.5	6.6	V
$t_{r\,V_{CC}}$	Power Supply Rise Time (Note 3)		0.2	2.0		μs
$t_{f\,V_{CC}}$	Power Supply Fall Time		0.2	2.0		μs
t_{ON}	V_{CC} ON Time	See Programming Timing Diagram	(Note 1)			
t_{OFF}	V_{CC} OFF Time		(Note 2)			
	Duty Cycle for V_{CC}	$t_{ON}/(t_{OFF} + t_{ON})$			50	%
READ STROBE (Note 5)						
t_{dRBP}	Read Delay before Programming	Initial Check		3.0		μs
t_w	Fuse Read Time			1.0		μs
$t_{d\,V_{CC}}$	Delay to V_{CC} OFF			1.0		μs
t_{dRAP}	Delay to Read after Programming	Verify		3.0		μs
CHIP SELECT						
V_{CSP}	Chip Select Programming Voltage		20.0	20.0	22.0	V
I_{CSP}	Chip Select Program Current Limit		175	180	185	mA
V_{IL}	Input Voltage LOW		0	0	0.4	V
V_{IH}	Input Voltage HIGH		2.4	5.0	5.0	V
t_{dCS}	Delay to Chip Deselect			1.0		μs
t_{rCS}	Chip Select Pulse Rise Time		3.0	4.0		μs
t_{dAP}	Delay to Chip Select Time		0.2	1.0		μs
t_{fCS}	Chip Select Pulse Fall Time		0.1	0.1	1.0	μs
PROGRAMMING CURRENT-PULSE TRAIN						
I_{IOP}	Initial Current Pulse	93Z565		40.0	40.0	mA
$I_{OP\,(Max)}$	Output Programming Current Limit	Apply Current Pulse to Selected Output	155	160	165	mA
$V_{OP\,(Max)}$	Output Programming Voltage Limit		24	25	26	V
t_{RIOP}	Programming Pulse Rise Time		160	100	100	mA/μs
t_{dBP}	Delay to Initial Programming Pulse	V_{CSP} Must be at Minimum	2.0	3.0		μs
t_{PW}	Programming Pulse Widths		8.0	9.0	10.0	μs
t_{fIOP}	Programming Pulse Fall Time (Note 3)		0.1	0.1	0.2	μs
ΔI_{OP}	Current Pulse Step Increase		5.0	10.0	10.0	mA
	Duty Cycle for Programming Pulses	Each Successive Pulse is Increased by I_{OP}	10	50	50	%

Note 1: Total time V_{CC} is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.

Note 2: t_{OFF} is equal to or greater than t_{ON}.

Note 3: Rise and fall times are from 10% to 90%.

Note 4: Recommended programming temperature T_C = +25°C ±10°C.

Note 5: Proceed to next address after read strobe indicates programmed cell.

Section 5

ECL I/O Static RAMs

Section 5 Contents

National Semiconductor

ECL I/O Static RAM Selection Guide

Part Number	Organization (Word x Bit)	Pins	Access (ns)	Temperature Range
100K LEVEL:				
100145DC	16 x 4	24	7	0°C to +85°C
100145FC	16 x 4	24	7	0°C to +85°C
100415DC10	1K x 4	16	10	0°C to +85°C
100415FC10	1K x 4	16	10	0°C to +85°C
100415LC10	1K x 4	16	10	0°C to +85°C
100422DC5	256 x 4	24	5	0°C to +85°C
100422DC7	256 x 4	24	7	0°C to +85°C
100422DC10	256 x 4	24	10	0°C to +85°C
100422FC5	256 x 4	24	5	0°C to +85°C
100422FC7	256 x 4	24	7	0°C to +85°C
100422FC10	256 x 4	24	10	0°C to +85°C
100422LC10	256 x 4	24	10	0°C to +85°C
10K LEVEL:				
10145ADC	16 x 4	16	9	0°C to +75°C
10145AFC	16 x 4	16	9	0°C to +75°C
10402DC	16 x 4	16	6	0°C to +75°C
10402FC	16 x 4	16	6	0°C to +75°C
10415ADC	1K x 1	16	10	0°C to +75°C
10415DC10	1K x 1	16	10	0°C to +75°C
10415FC10	1K x 1	16	10	0°C to +75°C
10422DC5	256 x 4	24	5	0°C to +75°C
10422DC7	256 x 4	24	7	0°C to +75°C
10422DC10	256 x 4	24	10	0°C to +75°C
10422FC5	256 x 4	24	5	0°C to +75°C
10422FC7	256 x 4	24	7	0°C to +75°C
10422FC10	256 x 4	24	10	0°C to +75°C

National Semiconductor

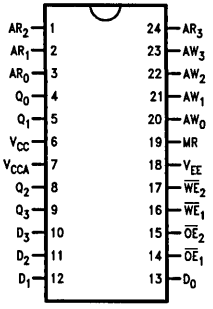
100145 16 x 4-Bit Register File Random Access Memory

General Description

The 100145 is a 64-bit register file organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the Write mode and the latches are in a Hold mode. When either $\overline{WE}$ input is HIGH, the circuit is in the Read mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active-LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches, and forces the outputs LOW.

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



TL/D/9638-1

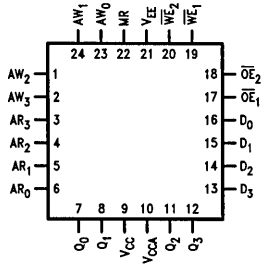
Top View

Order Number 100145DC
See NS Package Number J24E*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

24-Pin Ceramic Flatpak



TL/D/9638-2

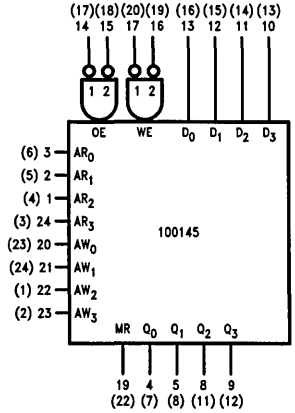
Top View

Order Number 100145FC
See NS Package Number W24B*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

Logic Symbol



TL/D/9638-3

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

AR_0–AR_3	Read Address Inputs
AW_0–AW_3	Write Address Inputs
$\overline{WE}_1$, $\overline{WE}_2$	Read Enable Inputs (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)
D_0–D_3	Data Inputs
MR	Master Reset Input
Q_0–Q_3	Data Outputs

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C	Output Current (DC Output High)	−50 mA
Maximum Junction Temperature (T_J)	+175°C	Operating Range (Note 1)	−5.7V to −4.2V
Supply Voltage Range	−7V to +0.5V	Lead Temperature (Soldering, 10 seconds)	300°C
Input Voltage (DC)	V_{EE} to +0.5V		

DC Electrical Characteristics V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	−1025	−880	mV
V_{OL}	Output Low Voltage			−1810	−1620	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1035		mV
V_{OLC}	Output Low Voltage				−1610	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1165	−880	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1810	−1475	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5		µA

DC Electrical Characteristics V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50Ω to −2V	−1020		−870	mV
V_{OL}	Output Low Voltage			−1810		−1605	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1030			mV
V_{OLC}	Output Low Voltage					−1595	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1150		−870	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1810		−1475	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5			µA
I_{IH}	Input HIGH Current All Inputs	V_{IN} = $V_{IH(max)}$				240	µA
I_{EE}	Power Supply Current	Inputs Open		−247	−170		mA

Note 1: Parametric values specified at −4.8V to −4.2V.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: The maximum address access time is guaranteed to be the worst case bit in memory using a pseudo random testing pattern.

DC Electrical Characteristics $V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C$ to $+85°C$ (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50Ω to −2V	−1035		−880	mV
V_{OL}	Output Low Voltage			−1830		−1620	mV
V_{OHC}	Output High Voltage	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$		−1045			mV
V_{OLC}	Output Low Voltage					−1610	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1165		−880	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1830		−1490	mV
I_{IL}	Input Low Current	$V_{IN} = V_{IL(min)}$		0.5			μA
I_{IH}	Input HIGH Current All Inputs	$V_{IN} = V_{IH(max)}$				240	μA
I_{EE}	Power Supply Current	Inputs Open		−247	−170		mA

Notes on preceding page.

AC Characteristics $V_{EE} = -4.2V$ to $-4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C$ to $+85°C$

Symbol	Parameters	Conditions	Min	Max	Units
ACCESS/RECOVERY TIMING					
t_{AA}	Address Access (Note 3)	*Figures 3* and *5a*	2.20	7.00	ns
t_{OR}	Output Recovery	*Figures 3* and *5e*	1.00	3.20	ns
t_{OD}	Output Disable		1.00	3.20	ns
READ TIMING					
t_{RSA1}	Address Setup	*Figures 3* and *5b*	1.0		ns
t_{WEQ}	Output Delay		2.00	5.5	ns
OUTPUT LATCH TIMING					
t_{RSA2}	Address Setup	*Figures 3* and *5c*	5.50		ns
t_{RHA}	Address Hold	*Figures 3* and *5d*	0.10		ns
WRITE TIMING					
t_{WSA}	Address Setup	t_W = 6.0 ns *Figures 3* and *6*	0.10		ns
t_{WHA}	Address Hold		1.0		ns
t_{WSD}	Data Setup		1.0		ns
t_{WHD}	Data Hold		1.0		ns
t_W	Write Pulse Width, LOW		5.5		ns
MASTER RESET TIMING					
t_M	Reset Pulse Width, LOW	*Figures 3* and *7*	5.0		ns
t_{MHW}	$\overline{WE}$ Hold to Write		7.0		ns
t_{MQ}	Output Disable	*Figures 3* and *7*	3.0		ns
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.50	2.30	ns

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Block Diagram

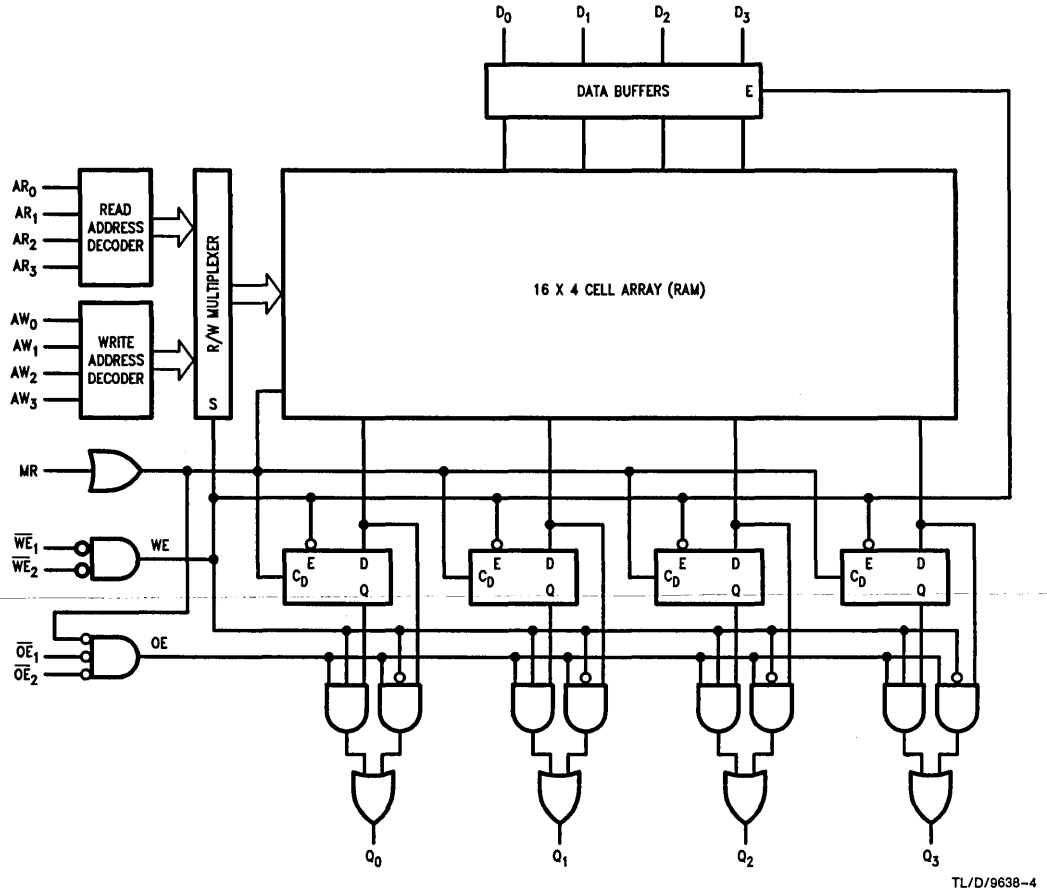


FIGURE 1. Logic Diagram

Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

AC Test Conditions

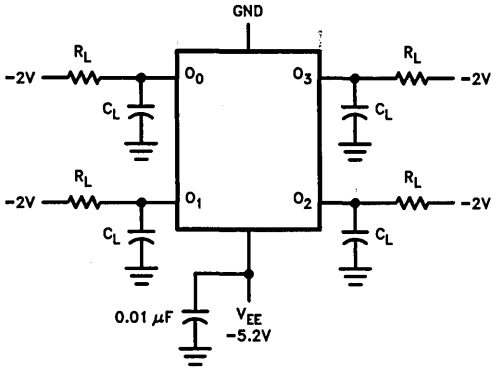


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FIGURE 2. AC Test Circuit

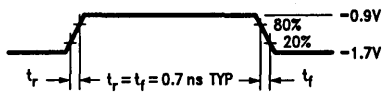

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FIGURE 3. Input Levels

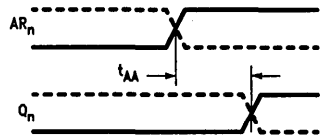
Notes:

All Timing Measurements Referenced to 50% of Input Levels.

C_L = 3 pF including Fixture and Stray Capacitance.

R_L = 50Ω to −2.0V.

Timing Diagrams



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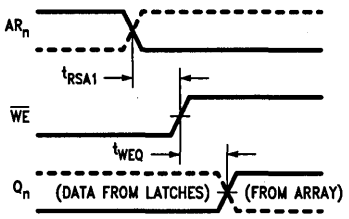
4a. Address Access Time ($\overline{WE}_1$ or $\overline{WE}_2$ = HIGH; $\overline{OE}_1$ = $\overline{OE}_2$ = LOW)



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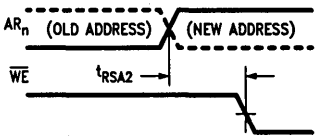
4b. Address Setup Time before $\overline{WE}$, to Ensure Minimum Delay (Unpulsed $\overline{WE}$ = $\overline{OE}_1$ = $\overline{OE}_2$ = LOW)



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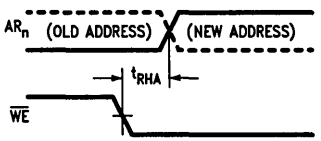
4c. Address Setup Time to Ensure Latching Data from New Address (Unpulsed $\overline{WE}$ = LOW)



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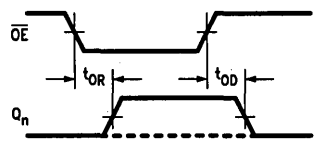
4d. Address Hold Time to Ensure Latching Data from Old Address (Unpulsed $\overline{WE}$ = LOW)



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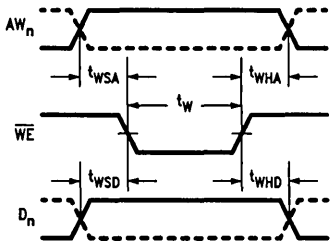
4e. Output Recovery/Disable Times, $\overline{OE}$ to Q_n (Unpulsed $\overline{OE}$ = LOW)

FIGURE 4. Read Timing

Timing Diagrams (Continued)



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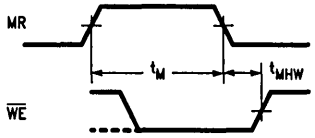
Address and Data Setup and Hold Times: Write Pulse Width (Unpulsed $\overline{WE}$ = LOW)

FIGURE 5. Write Timing



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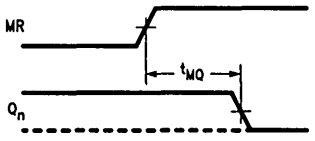
6a. Reset Pulse Width; $\overline{WE}$ Hold Time for Subsequent Writing (Address Already Setup, Unpulsed $\overline{WE}$ = LOW)



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6b. Output Reset Delay, MR to Q_n

FIGURE 6. Master Reset Timing

National Semiconductor

100415 1024 x 1-Bit Random Access Memory

General Description

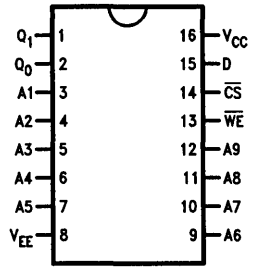
The 100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as an active-LOW Chip Select line.

Features

- Address access time—10 ns max
- Chip select access time—5.0 ns max
- Open-emitter output for easy memory expansion
- Power dissipation—0.79 mW/bit typ
- Power dissipation decreases with increasing temperature
- Polyamide die coat for alpha immunity

Connection Diagrams

16-Pin Ceramic Flatpak



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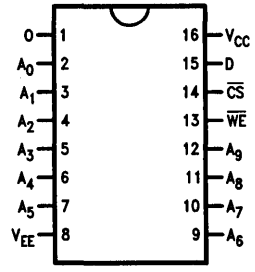
Top View

Order Number 100415FC10
See NS Package Number W16A*

16-Pin Ceramic Dual-In-Line Package



TL/D/9639–2

Top View

Order Number 100415DC10
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C
Supply Voltage Range	−7V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−50 mA
Operating Range (Note 1)	−5.7V to −4.2V
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.*

DC Electrical Characteristics V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	−1025	−880	mV
V_{OL}	Output Low Voltage			−1810	−1620	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1035		mV
V_{OLC}	Output Low Voltage				−1610	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1165	−880	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1810	−1475	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5		μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(max)}$			220	μA
I_{EE}	Power Supply Current	Inputs and Output Open		−200		mA

DC Electrical Characteristics V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	−1020	−870	mV
V_{OL}	Output Low Voltage			−1810	−1605	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1030		mV
V_{OLC}	Output Low Voltage				−1595	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1150	−870	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1810	−1475	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5		μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(max)}$			220	μA
I_{EE}	Power Supply Current	Inputs and Output Open		−200		mA

DC Electrical Characteristics V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50Ω to −2V	−1035	−880	mV
V_{OL}	Output Low Voltage			−1830	−1620	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1045		mV
V_{OLC}	Output Low Voltage				−1610	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1165	−880	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1830	−1490	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5		μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(max)}$			220	μA
I_{EE}	Power Supply Current	Inputs and Output Open		−200		mA

AC Performance Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = GND, Output Load = 50Ω and 3 pF to −2.0V, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ TIMING						
t_{ACS}	Chip Select Access Time	*Figures 5a, 5b*			5.0	ns
t_{RCS}	Chip Select Recovery Time				5.0	ns
t_{AA}	Address Access Time (Note 3)				10	ns
WRITE TIMING						
t_W	Write Pulse Width to Guarantee Writing (Note 4)	*Figure 6*	7			ns
t_{WSD}	Data Setup Time prior to Write		1.0			ns
t_{WHD}	Data Hold Time after Write		2.0			ns
t_{WSA}	Address Setup Time Prior to Write (Note 4)		1.0			ns
t_{WHA}	Address Hold Time after Write		2.0			ns
t_{WSCS}	Chip Select Setup Time Prior to Write		1.0			ns
t_{WHCS}	Chip Select Hold Time after Write		2.0			ns
t_{WS}	Write Disable Time				5.0	ns
t_{WR}	Write Recovery Time				10	ns
t_r	Output Rise Time	Measured between 20% and 80% or 80% and 20%		0.7		ns
t_f	Output Fall Time			0.7		ns
C_{IN}	Input Pin Capacitance	Measured with a Pulse Technique		4.0	5.0	pF
C_{OUT}	Input Pin Capacitance			7.0	8.0	pF

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Note 1: Parametric values specified at −4.8V to −4.2V.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating range.

Note 3: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 4: t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Logic Diagram

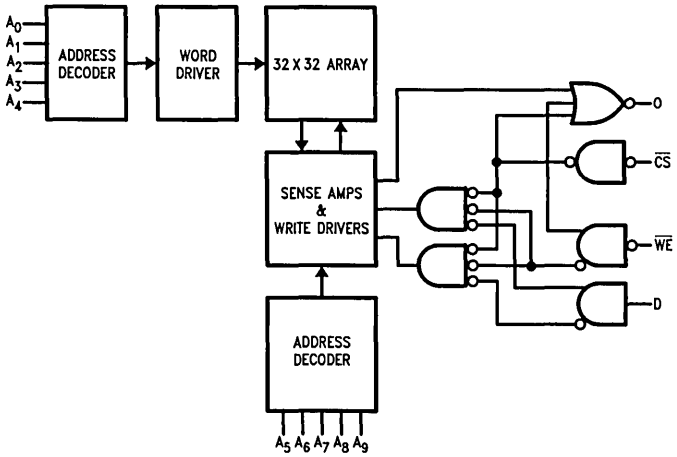


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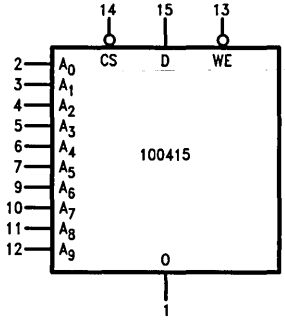
FIGURE 1

Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

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FIGURE 2

AC Test Conditions

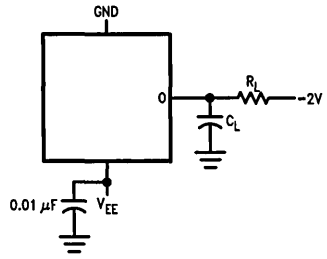

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FIGURE 3. AC Test Circuit

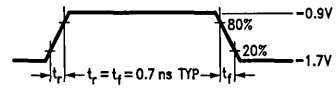

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FIGURE 4. Input Levels

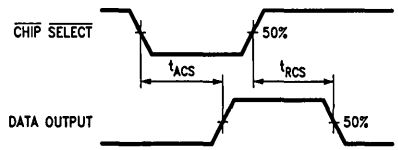
Notes:

All Timing Measurements Referenced to 50% of Input Levels.

C_L = 3 pF including Fixture and Stray Capacitance.

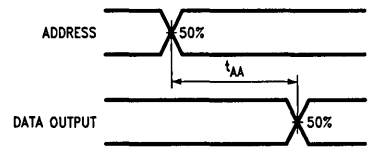
R_L = 50Ω to −2.0V.

Read Mode



TL/D/9639-6

5a. Read Mode Propagation Delay for Chip Select



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5b. Read Mode Propagation Delay from Address

FIGURE 5. Read Mode Timing

Write Mode

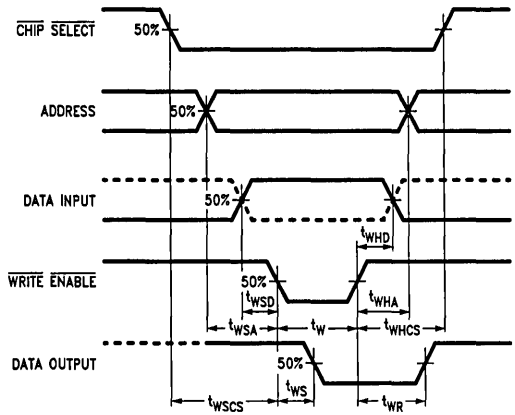

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FIGURE 6. Write Mode Timing

Note:

Timing Diagram represents on solution which results in an optimun cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Functional Description

The 100415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

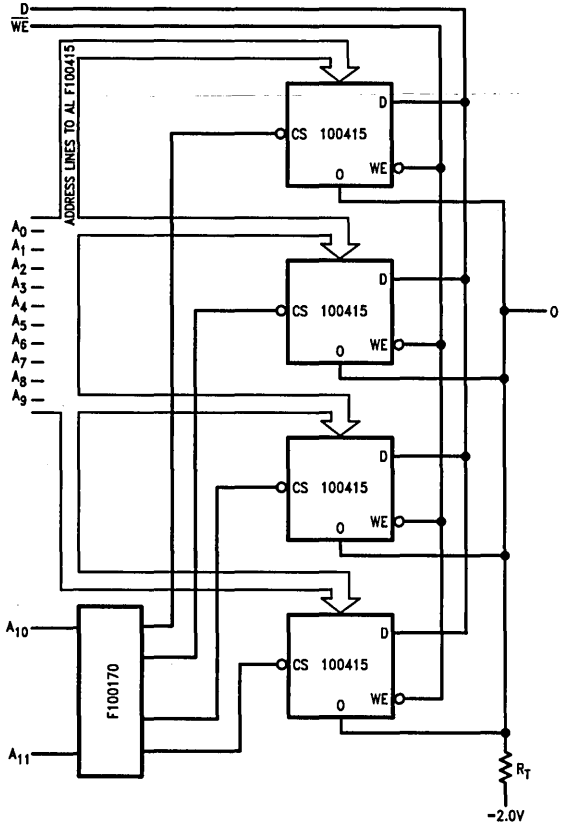
The output of the 100415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several 100415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50Ω pull-down resistor to −2V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = −0.9V (Nominal)
L = LOW Voltage Levels = −1.7V (Nominal)
X = Don't Care
Data = Previously stored data

Typical Application



TL/D/9639–9

FIGURE 7. 4096-Word x n-Bit System

National Semiconductor

100422 256 x 4-Bit Static RAM 10 ns, 7 ns, 5 ns

General Description

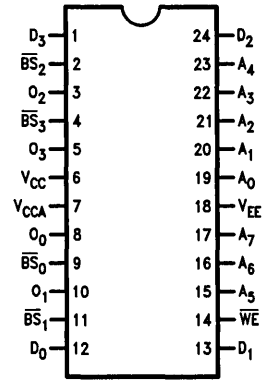
The 100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device features full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as four active-LOW Bit Select lines.

Features

- Address access time—5 ns/7 ns/10 ns max
- Bit select access time—4 ns/5 ns/5 ns max
- Four bits can be independently selected
- Open-emitter outputs for easy memory expansion
- Polyimide die coat for alpha immunity

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



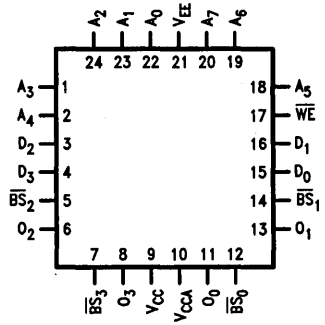
TL/D/9643-2

Top View

Order Number 100422DC5, 100422DC7 or 100422DC10
See NS Package Number J24E*

*For most current package information, contact product marketing.

24-Pin Ceramic Flatpak



TL/D/9643-3

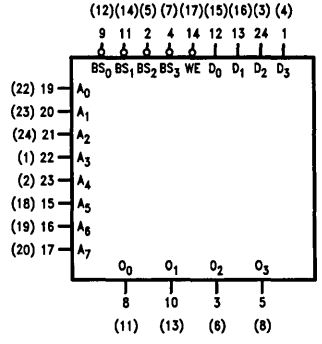
Top View

Order Number 100422FC5, 100422FC7 or 100422FC10
See NS Package Number W24B*

*For most current package information, contact product marketing.

Optional Processing, QR = Burn-In

Logic Symbol



TL/D/9643-1

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS_0}$–$\overline{BS_3}$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Supply Voltage Range	−7V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−50 mA
Operating Range (Note 1)	−5.7V to −4.2V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	−1025	−880	mV
V_{OL}	Output LOW Voltage			−1810	−1620	mV
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1035		mV
V_{OLC}	Output LOW Voltage				−1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed High Signal for All Inputs		−1165	−880	mV
V_{IL}	Input LOW Voltage	Guaranteed Low Signal for All Inputs		−1810	−1475	mV
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(min)}$		0.5		μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IL(max)}$			220	μA
I_{EE}	Power Supply Current (5 ns) (7 ns) (10 ns)	All Inputs and Outputs Open		−230 −200 −200		mA

Note 1: Parametric values specified at −4.8V to −4.2V.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating range.

Note 3: The maximum address access time is guaranteed to be for the worst-case single bit in the memory using a pseudorandom testing pattern.

Note 4: t_W measured at t_{WSA} = min, t_{WSA} measured at t_W = min.

DC Electrical Characteristics V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	−1020	−870	mV
V_{OL}	Output LOW Voltage			−1810	−1605	mV
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1030		mV
V_{OLC}	Output LOW Voltage				−1595	mV
V_{IH}	Input HIGH Voltage	Guaranteed High Signal for All Inputs		−1150	−870	mV
V_{IL}	Input LOW Voltage	Guaranteed Low Signal for All Inputs		−1810	−1475	mV
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(min)}$		0.5		μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IL(max)}$			220	μA
I_{EE}	Power Supply Current (5 ns) (7 ns) (10 ns)	All Inputs and Outputs Open		−230 −200 −200		mA

DC Electrical Characteristics V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50Ω to −2V	−1035		−880	mV
V_{OL}	Output Low Voltage			−1830		−1620	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$		−1045			mV
V_{OLC}	Output Low Voltage					−1610	mV
V_{IH}	Input High Voltage	Guaranteed High Signal for All Inputs		−1165		−880	mV
V_{IL}	Input Low Voltage	Guaranteed Low Signal for All Inputs		−1830		−1490	mV
V_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		0.5			μA
V_{IH}	Input HIGH Current All Inputs	V_{IN} = $V_{IH(max)}$				240	μA
V_{EE}	Power Supply Current	Inputs Open		−247	−170		mA

AC Performance Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, Output Load. See *Figure 1*, T_C = 0°C to +85°C

Symbol		Parameter	5 ns		7 ns		10 ns		Units	Notes
Standard	Common		Min	Max	Min	Max	Min	Max		
READ TIMING										
t_{BSLQV}	t_{ABS}	Bit Select Access Time		4.0		5.0		5.0	ns	*Figure 3*
t_{BSHQL}	t_{RBS}	Bit Select Recovery Time		4.0		5.0		5.0	ns	
t_{AVQV}	t_{AA}	Address Access Time (Note 3)		5.0		7.0		10.0	ns	
WRITE TIMING										
t_{WLWH}	t_W	Write Pulse Width (Note 4)	3.5		5.0		7.0		ns	*Figure 4*
t_{DVWL}	t_{WSD}	Data Setup Time	2.0		1.0		1.0		ns	
t_{WHDX}	t_{WHD}	Data Hold Time	1.0		1.0		1.0		ns	
t_{AVWL}	t_{WSA}	Address Setup Time (Note 4)	1.0		1.0		1.0		ns	
t_{WHAX}	t_{WHA}	Address Hold Time	1.0		1.0		1.0		ns	
t_{BSLWL}	t_{WSBS}	Bit Select Setup Time	1.0		1.0		1.0		ns	
t_{WHBSH}	t_{WHBS}	Bit Select Hold Time	1.0		1.0		1.0		ns	
t_{WLQL}	t_{WS}	Write Disable Time		4.0		5.0		5.0	ns	
t_{WHQV}	t_{WR}	Write Recovery Time		5.0		7.0		7.0	ns	

Note 1: Parametric values specified at −4.8V to −4.2V.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating range.

Note 3: The maximum address access time is guaranteed to be for the worst-case single bit in the memory using a pseudorandom testing pattern.

Note 4: t_W measured at t_{WSA} = min, t_{WSA} measured at t_W = min.

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Functional Description

The 100422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at D_0–D_3 is written into the address location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The outputs are inactive (LOW) during that portion of the write cycle when Write Enable and Bit Select are true (LOW).

Truth Table

Inputs			Output	Mode
$\overline{BS}_n$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D and O, but all have common $\overline{WE}$

H = HIGH Voltage Level = − 0.9V (Nominal)

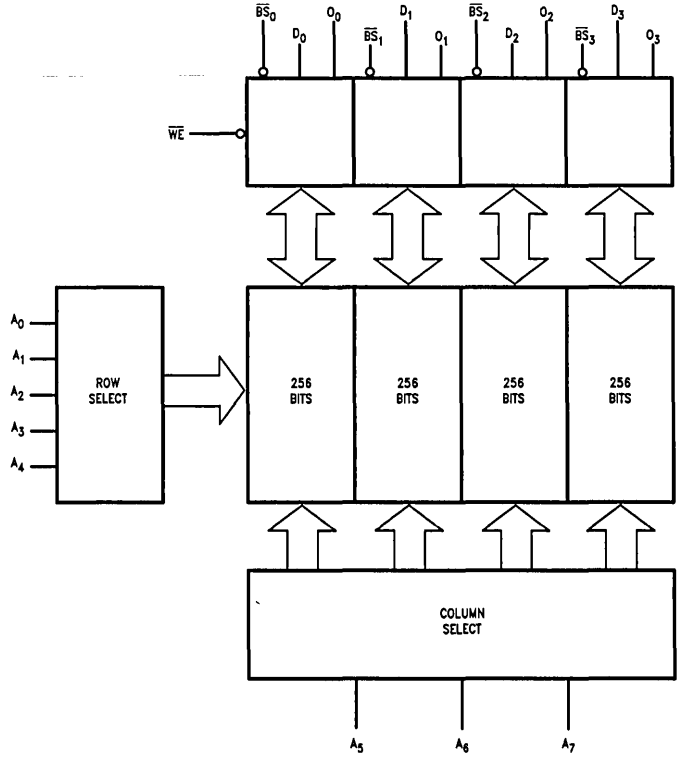
L = LOW Voltage Levels = −1.7V (Nominal)

X = Don't Care

Data = Previously Stored Data

The outputs of the 100422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In may applications it is desirable to tie the outtputs of several 100422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50Ω pull-down resistor to −2V or an equivalent network must be used to provide a LOW at the output.

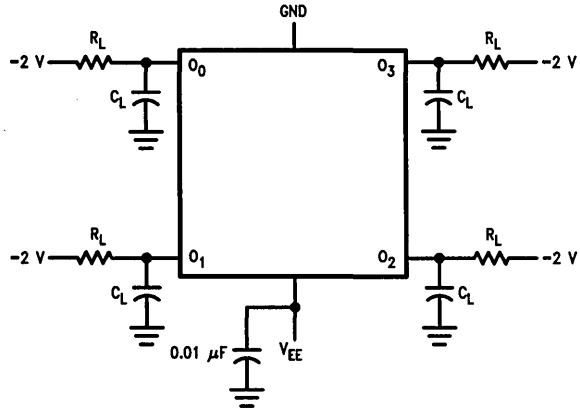
Logic Diagram



TL/D/9643–5

FIGURE 1. Logic Diagram

AC Test Conditions



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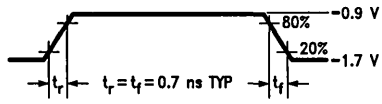
Notes:
All Timing Measurements Referenced to 50% of Input Levels
$C_L \leq 5$ pF including Fixture and Stray Capacitance
$R_L = 50\Omega$ to $-2.0V$

FIGURE 2. AC Test Circuit



TL/D/9643–7

FIGURE 3. Input Levels

Read Mode

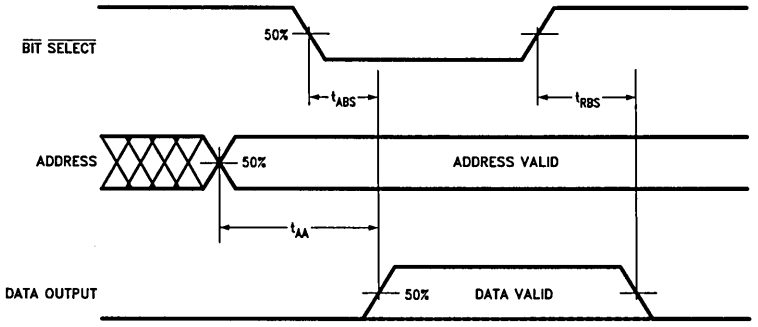


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FIGURE 4. Read Mode Propagation Delay

Write Mode

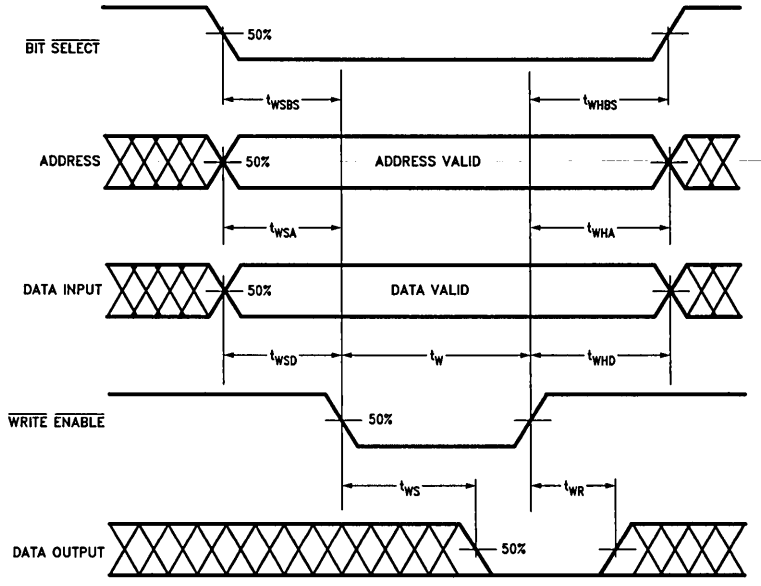

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FIGURE 5. Write Mode Timing

National Semiconductor

10145A
16 x 4 Register File (Random Access Memory)

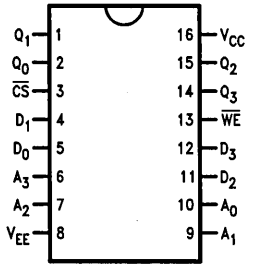
General Description

The 10145A is a high-speed 64-bit Random Access Memory organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select (CS) and Write Enable (WS) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Connection Diagram

16-Pin Ceramic Dual-In-Line Package



TL/D/9742–2

Top View

Order Number 10145ADC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select
A_0–A_3	Address
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enables
Q_0–Q_3	Data Outputs

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Guaranteed Operating Ranges

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.46V	−5.2V	−4.94V
Case Temperature (T_C)	0°C		+75°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

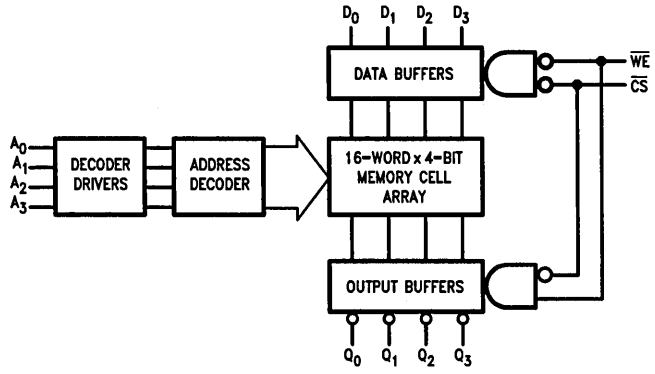
DC Electrical Characteristics V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +75°C (Note)

Symbol	Parameter	Conditions		Min	Max	Unit	T_C
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2.0V	−1000 −960 −900	−840 −810 −720	mV	0°C +25°C +75°C
V_{OL}	Output LOW Voltage			−1870 −1850 −1830	−1665 −1650 −1625	mV	0°C +25°C +75°C
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		−1020 −980 −920		mV	0°C +25°C +75°C
V_{OLC}	Output LOW Voltage				−1645 −1630 −1605	mV	0°C +25°C +75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage HIGH for All Inputs		−1145 −1105 −1045	−840 −810 −720	mV	0°C +25°C +75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage LOW for All Inputs		−1870 −1850 −1830	−1490 −1475 −1450	mV	0°C +25°C +75°C
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(min)}$		0.5	170	μA	+25°C
I_{IH}	Input HIGH Current $\overline{CS}$, A_0–A_3 $\overline{WE}$, D_0–D_3	V_{IN} = $V_{IH(max)}$			 200 220	μA	
I_{EE}	Power Supply Current	Inputs and Outputs OPEN		−150		mA	

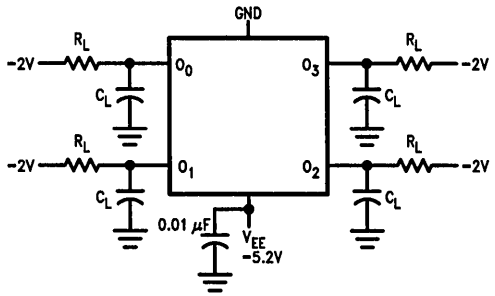
Note: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Logic Diagrams

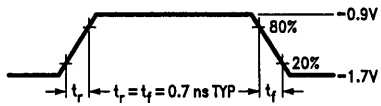


TL/D/9742-4



TL/D/9742-5

FIGURE 1. AC Test Circuit



TL/D/9742-6

FIGURE 2. Input Levels

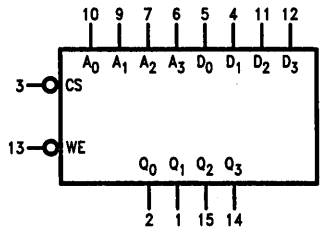
Notes:

All Timing Measurements Referenced to 50% of Input Levels

C_L = 3 pF including Fixture and Stray Capacitance

R_L = 50Ω to −2.0V

Logic Symbol



TL/D/9742-1

V_{CC} = Pin 16

V_{EE} = Pin 8

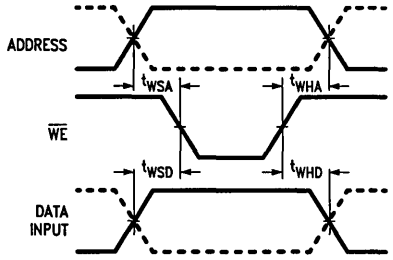
AC Performance Characteristics V_{EE} = −5.2V ±5%, V_{CC} = GND, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Access/Recovery Times					
t_{ACS}	Chip Select Access	*Figures 1* and *4*		4.5	6.0	ns
t_{RCS}	Chip Select Recovery			4.5	6.0	ns
t_{AA}	Address Access (Note)			6.5	9.0	ns
	Write Setup Times					
t_{WSD}	Data	*Figures 1* and *3*	4.5	3.0		ns
t_{WSCS}	Chip Select		4.5	2.5		ns
t_{WSA}	Address		3.5	1.5		ns
	Write Hold Times					
t_{WHD}	Data		0	−0.5		ns
t_{WHCS}	Chip Select		0.5	0		ns
t_{WHA}	Address		1.0	−1.0		ns
t_{WR}	Write Recovery Time	*Figures 1* and *4*		4.5	6.0	ns
t_{WS}	Write Disable Time			4.5	6.0	ns
t_W	Write Pulse Width, Min	*Figures 1* and *3*	4.0	2.5		ns
t_{CS}	Chip Select Pulse Width, Min		4.0	2.5		ns
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	*Figures 1* and *4*	0.5	2.5	3.9	ns

Note: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

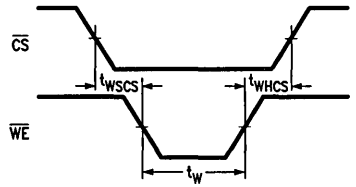
Write Modes

Write Enable Strobe Address and Data Input Set-Up and Hold Times ($\overline{CS}$ = LOW)



TL/D/9742-7

Chip Select Set-Up and Hold Times

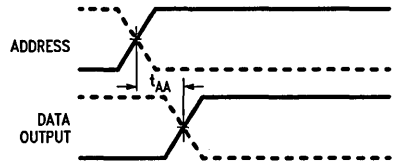


TL/D/9742-8

FIGURE 3

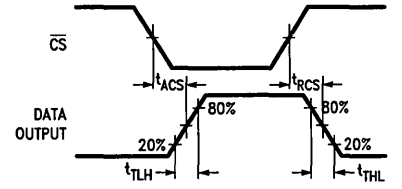
Read Modes

Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW) Address Access Time



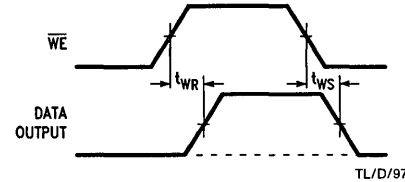
TL/D/9742-9

Chip Select Input to Data Output ($\overline{WE}$ = HIGH) Chip Select Access and Recovery Times



TL/D/9742-10

Write Enable Input to Data Output ($\overline{CS}$ = LOW) Write Recovery, Disable Times



TL/D/9742-11

FIGURE 4

National Semiconductor

10402 16 x 4-Bit Register File (Random Access Memory)

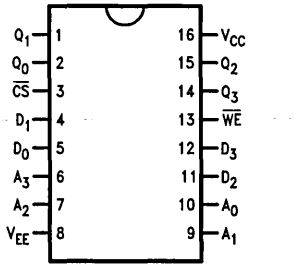
General Description

The 10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, i.e., the memory is non-inverting.

Connection Diagrams

16-Pin Ceramic Dual-In-Line Package



TL/D/9640-2

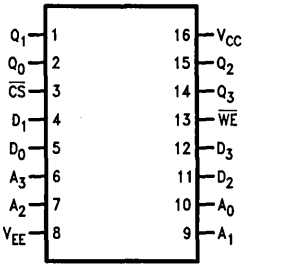
Top View

Order Number 10402DC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Flatpack



TL/D/9640-3

Top View

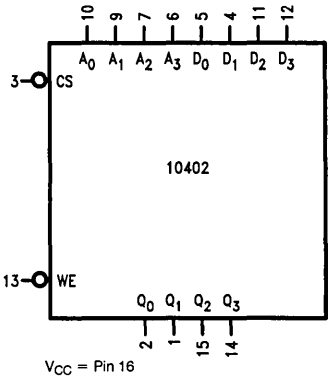
Order Number 10402FC
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select Input
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0–Q_3	Data Outputs



V_{CC} = Pin 16
V_{EE} = Pin 8

TL/D/9640-1

FIGURE 1. Logic Symbol

5

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Guaranteed Operating Ranges

	Min	Max	Units
Supply Voltage (V_{CC})	−5.46	−4.94	V
Case Temperature (T_C)	0	+75	°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Electrical Characteristics V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +75°C (Note)

Symbol	Parameter	Conditions		T_C	Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2V	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Low Voltage			0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Low Voltage			0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input High Voltage	Guaranteed Input Voltage High for All Inputs		0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Low Voltage	Guaranteed Input Voltage Low for All Inputs		0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		+25°C	0.5	170	μA
I_{IH}	Input HIGH Current All Inputs	V_{IN} = $V_{IH(max)}$		0°C		300	μA
I_{EE}	Power Supply Current	Inputs Open		0°C	−170	−70	mA

Note: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

AC Performance Characteristics

V_{EE} = −5.2V ±5%, V_{CC} = GND, Applies to Flatpack and DIP Packages

Symbol	Parameter	Conditions	T_C = 0°C		T_C = 25°C		T_C = 75°C		Unit
			Min	Max	Min	Max	Min	Max	
ACCESS/RECOVERY TIMING									
t_{ACS}	Chip Select Access	*Figures 3* and *6*		3.30		3.50		3.80	ns
t_{RCS}	Chip Select Recovery			3.30		3.50		3.80	ns
t_{AA}	Address Access (Note)			5.00		5.30		6.00	ns
WRITE TIMING, SETUP									
t_{WSD}	Data	*Figures 3* and *5*	0.50		0.50		0.80		ns
t_{WSCS}	Chip Select	T_W = 6 ns	1.50		1.50		1.50		ns
t_{WSA}	Address		1.00		1.00		1.00		ns
WRITE TIMING, HOLD									
t_{WHD}	Data	*Figures 3* and *5*	0.50		0.50		0.50		ns
t_{WHCS}	Chip Select	T_W = 6 ns	0.50		0.50		0.50		ns
t_{WHA}	Address		2.50		2.50		2.50		ns
t_{WR}	Write Recovery Time	*Figures 3* and *6*		4.00		4.00		4.50	ns
t_{WS}	Write Disable Time			3.00		3.00		3.50	ns
t_W	Write Pulse Width, (LOW)	*Figures 3* and *5*	2.50		2.50		3.00		ns
t_{CS}	Chip Select Pulse Width, (LOW)		2.50		2.50		3.00		ns
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	*Figures 3* and *6*	0.50	1.70	0.50	1.70	0.50	1.70	ns

Note: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

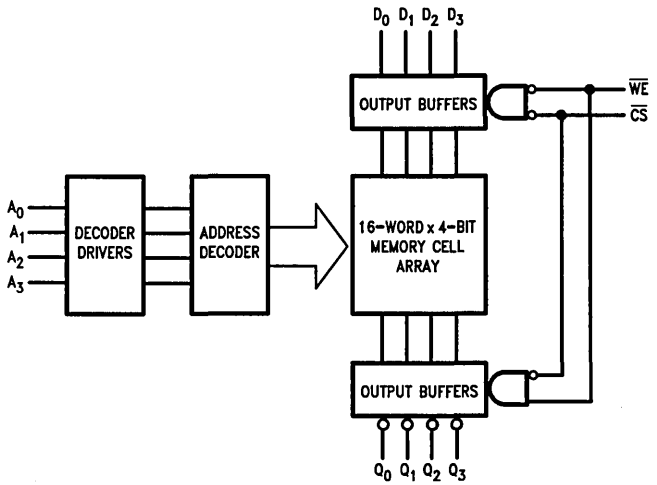


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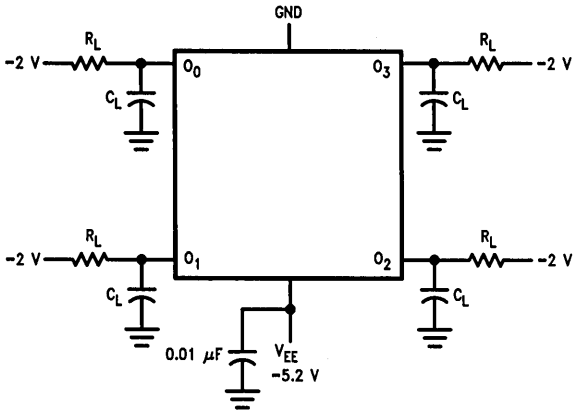
FIGURE 2. Logic Diagram

AC Test Circuit



TL/D/9640-5

Notes:

All timing measurements referenced to 50% of input levels

C_L = 3 pF including fixture and stray capacitance

R_L = 50Ω to −2.0V

FIGURE 3

Input Levels

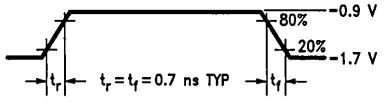


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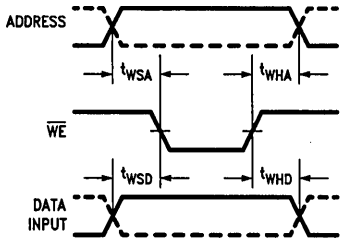
FIGURE 4

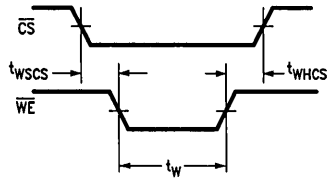
Write Modes

Write Enable Strobe



TL/D/9640-7

FIGURE 5. Address and Data Input Setup and Hold Times ($\overline{CS}$ = LOW)



TL/D/9640-8

FIGURE 5a. Chip Select Setup and Hold Times

Read Modes

Address Input to Data Output
($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)

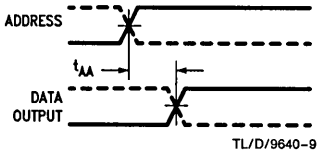


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FIGURE 6. Address Access Time

Chip Select Input to Data Output
($\overline{WE}$ = HIGH)

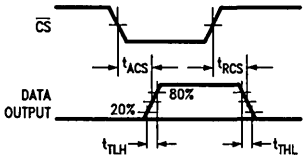

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FIGURE 6a. Chip Select Access and Recovery Times

Write Enable Input to Data Output
($\overline{CS}$ = LOW)

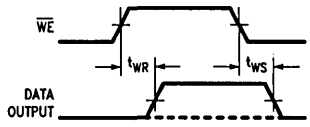

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FIGURE 6b. Write Recovery, Disable Times

National Semiconductor

10415 1024 x 1-Bit Static Random Access Memory

General Description

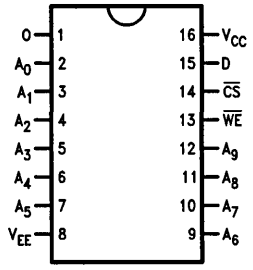
The 10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

Features

- Address access time—10 ns max
- Chip select access time—5 ns max
- Open-emitter output for easy memory expansion
- Power dissipation—0.92 mW/Bit Typ
- Power dissipation decreases with increasing temperature
- Polyimide die coat for alpha immunity

Connection Diagrams

16-Pin Ceramic Dual-In-Line Package



TL/D/9641-2

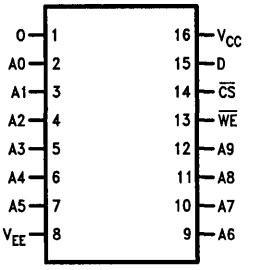
Top View

Order Number 10415DC10
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Ceramic Flatpack



TL/D/9641-11

Top View

Order Number 10415FC10
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Guaranteed Operating Ranges

	Min	Typ	Max	Units
Supply Voltage (V_{EE})	−5.46	−5.2	−4.94	V
Case Temperature (T_C)	0°		+75°	°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Electrical Characteristics V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +75°C (Note 1)

Symbol	Parameter	Conditions		T_C	Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2.0V	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Low Voltage			0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Low Voltage			0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input High Voltage	Guaranteed Input Voltage High for All Inputs		0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Low Voltage	Guaranteed Input Voltage Low for All Inputs		0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(max)}$			220	μA	
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_9, D	V_{IN} = $V_{IL(min)}$		0.5 −50	170	μA	
I_{EE}	Power Supply Current	Inputs and Output Open		−200		mA	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 3: T_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

AC Performance Characteristics

V_{EE} = −5.2V ± 5%, V_{CC} = GND, Output Load = 50Ω and 3 pF to −2.0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	10415		Units
			Min	Max	
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 5a, 5b*		5.0	ns
t_{RCS}	Chip Select Recovery Time			5.0	ns
t_{AA}	Address Access Time (Note 2)			10	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 3)	*Figure 6*	7.0		ns
t_{WSD}	Data Setup Time Prior to Write		1.0		ns
t_{WHD}	Data Hold Time after Write		2.0		ns
t_{WSA}	Address Setup Time Prior to Write (Note 3)		1.0		ns
t_{WHA}	Address Hold Time after Write		2.0		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		1.0		ns
t_{WHCS}	Chip Select Hold Time after Write		2.0		ns
t_{WS}	Write Disable Time			5.0	ns
t_{WR}	Write Recovery Time			10	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	Output Rise Time	Measured between 20% and		0.7		ns
t_f	Output Fall Time	80% or 80% and 20%		0.7		ns
C_{IN}	Input Pin Capacitance	Measured with a Pulse		4.0	5.0	pF
C_{OUT}	Output Pin Capacitance	Technique		7.0	8.0	pF

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpack are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 3: T_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Functional Description

The 10415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

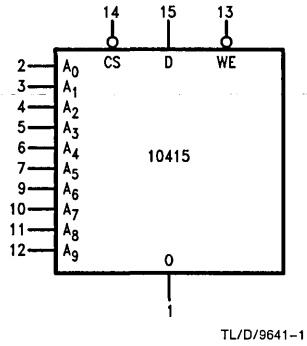
The output of the 10415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several 10415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50Ω pull-down resistor to −2V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = HIGH Voltage Levels = 0.9V (Nominal)
L = LOW Voltage Levels = 1.7V (Nominal)
X = Don't Care
Data = Previously stored data

Logic Symbol

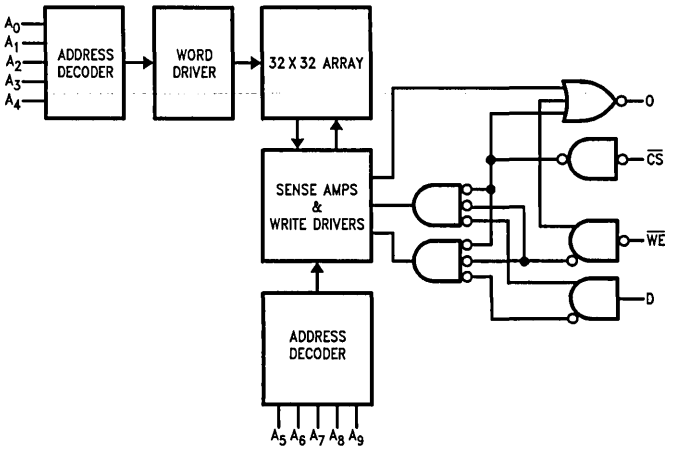


TL/D/9641–1

V_{CC} = Pin 16
V_{EE} = Pin 8

FIGURE 1

Logic Diagram



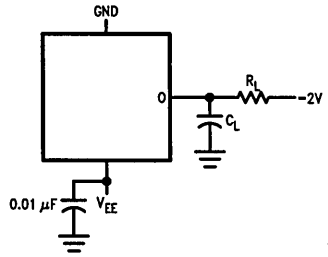
TL/D/9641–3

FIGURE 2

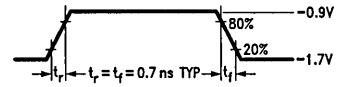
Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_{0-A9}	Address Inputs
D	Data Input
O	Data Output

AC Test Conditions



TL/D/9641–4



TL/D/9641–5

FIGURE 4. Input Levels

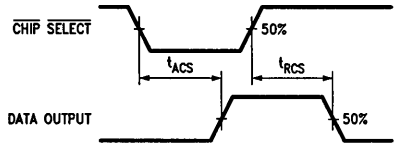
Notes:

All Timing Measurements Referenced to 50% of Input Levels.

C_L = 3 pF including Fixture and Stray Capacitance.

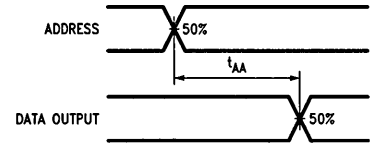
R_L = 50Ω to −2.0V.

FIGURE 3. AC Test Circuit



TL/D/9641–6

5a. Read Mode Propagation Delay from Chip Select



TL/D/9641–7

5b. Read Mode Propagation Delay from Address

FIGURE 5. Read Mode Timing

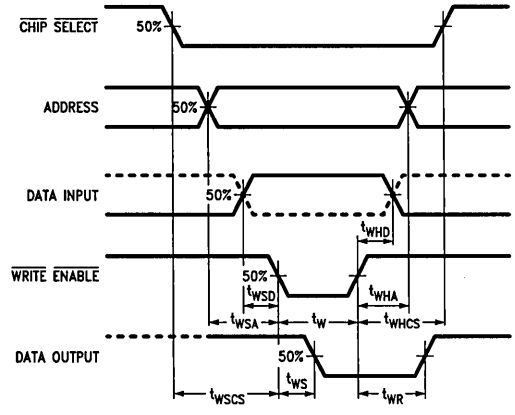


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FIGURE 6. Write Mode Timing

Note: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Typical Application

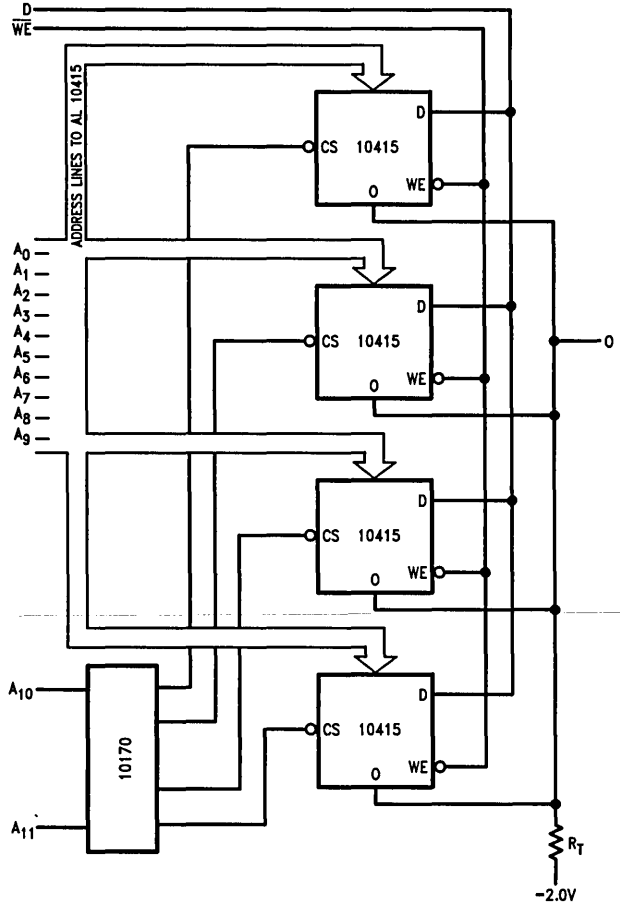


FIGURE 7. 4096-Word x n-Bit System

National Semiconductor

10422 256 x 4-Bit Static RAM 10 ns, 7 ns, 5 ns

General Description

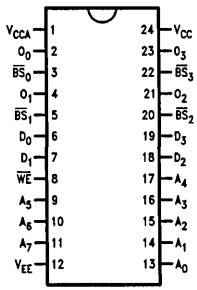
The 10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control, and buffer storage applications. The device features full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as four active-LOW Bit Select lines.

Features

- Address access time—5 ns/7 ns/ 10 ns Max
- Bit select access time—4 ns/5 ns/5 ns Max
- Four bits can be independently selected
- Open-emitter outputs for easy memory expansion
- Polyimide die coat for alpha immunity

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



TL/D/9642–2

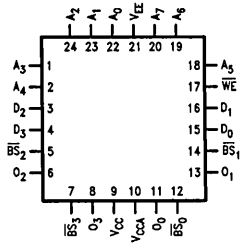
Top View

Order Number 10422DC5, 10422DC7 or 10422DC10
See NS Package Number J24E*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

24-Pin Flatpak



TL/D/9642–3

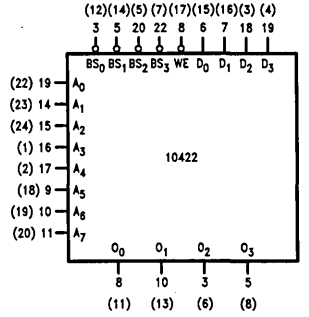
Top View

Order Number 10422FC5, 10422FC7 or 10422FC10
See NS Package Number W24B*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

Logic Symbol



TL/D/9642–1

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

Symbol	Description
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0$–$\overline{BS}_3$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+175°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Guaranteed Operating Ranges

	Min	Typ	Max	Units
Supply Voltage (V_{EE})	−5.46	−5.2	−4.94	V
Case Temperature (T_C)	0		+75	°C

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Electrical Characteristics V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +75°C (Note)

Symbol	Parameter	Conditions		T_C	Min	Max	Units
V_{OH}	Output High Voltage	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50Ω to −2.0V	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Low Voltage			0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output High Voltage	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$		0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Low Voltage			0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input High Voltage	Guaranteed Input Voltage High for All Inputs		0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Low Voltage	Guaranteed Input Voltage Low for All Inputs		0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IL}	Input Low Current	V_{IN} = $V_{IL(min)}$		+25°C	0.5	170	μA
I_{IH}	Input HIGH Current	V_{IN} = $V_{IL(max)}$				220	μA
I_{EE}	Power Supply Current (5 ns) (7 ns) (10 ns)	All Inputs and Outputs Open			 −230 −200 −200		 mA

Note: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

AC Performance Characteristics

V_{EE} = −5.2V ±5%, V_{CC} = V_{CCA} = GND, Output Load—See *Figure 1*, T_C = 0°C to +75°C

Symbol		Parameter	5 ns		7 ns		10 ns		Units	Notes
Standard	Common		Min	Max	Min	Max	Min	Max		
READ TIMING										
t_{BSLQV}	t_{ABS}	Bit Select Access Time		4.0		5.0		5.0	ns	*Figure 3*
t_{BSHQL}	t_{RBS}	Bit Select Recovery Time		4.0		5.0		5.0	ns	
t_{AVQV}	t_{AA}	Address Access Time (Note 1)		5.0		7.0		10.0	ns	
WRITE TIMING										
t_{WLWH}	t_W	Write Pulse Width (Note 2)	3.5		5.0		7.0		ns	*Figure 4*
t_{DVWL}	t_{WSD}	Data Setup Time	1.0		1.0		1.0		ns	
t_{WHDX}	t_{WHD}	Data Hold Time	1.0		1.0		1.0		ns	
t_{AVWL}	t_{WSA}	Address Setup Time (Note 2)	1.0		1.0		1.0		ns	
t_{WHAX}	t_{WHA}	Address Hold Time	1.0		1.0		1.0		ns	
t_{BSLWL}	t_{WSBS}	Bit Select Setup Time	1.0		1.0		1.0		ns	
t_{WHBSH}	t_{WHBS}	Bit Select Hold Time	1.0		1.0		1.0		ns	
t_{WLQL}	t_{WS}	Write Disable Time	4.0			5.0		5.0	ns	
t_{WHQV}	t_{WR}	Write Recovery Time	5.0			7.0		7.0	ns	

All ECL RAM products (except for Register File RAMs) in ceramic packages: dual-in-line, and flatpak are polyimide die-coated to decrease sensitivity to alpha particles emitted primarily by the seal glass and ceramic of the package.

Note 1: The maximum address access time is guaranteed to be for the worst-case single bit in the memory using a pseudorandom testing pattern.

Note 2: t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Functional Description

The 10422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at D_0–D_3 is written into the address location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(Min)}$ plus $t_{W(Min)}$ plus $t_{WHD(Min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The outputs are inactive (LOW) during that portion of the write cycle when Write Enable and Bit Select are true (LOW).

The outputs of the 10422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several 10422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50Ω pull-down resistor to −2V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{BS}_n$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

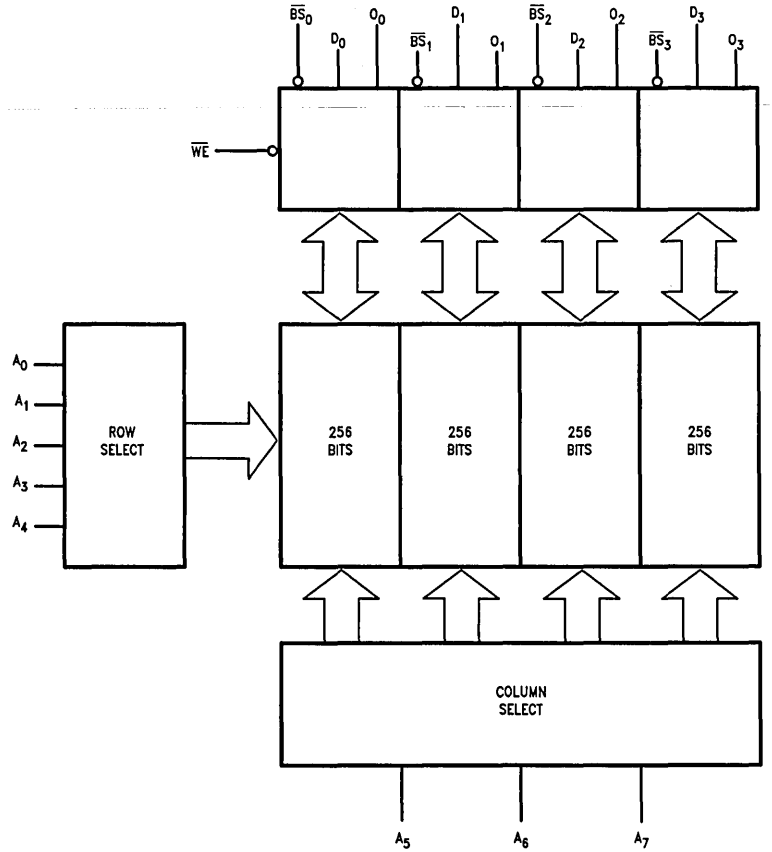
Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$

H = HIGH Voltage Levels = −0.9V (Nominal)

L = LOW Voltage Levels = −1.7V (Nominal)

X = Don't Care

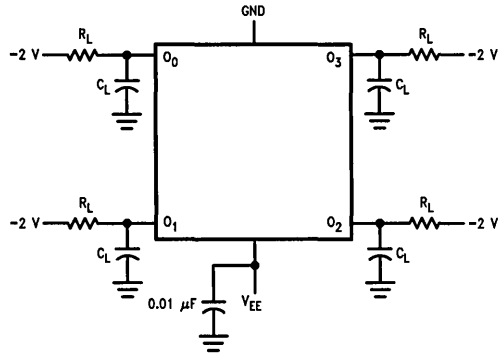
Data = Previously Stored Data



TL/D/9642–4

FIGURE 1. Logic Diagram

AC Test Conditions



TL/D/9642-5

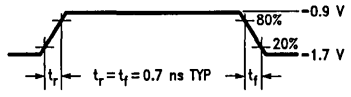
Notes:

All Timing Measurements Referenced to 50% of Input Levels.

$C_L \leq 5$ pF including Fixture and Stray Capacitance.

$R_L = 50\Omega$ to -2.0V.

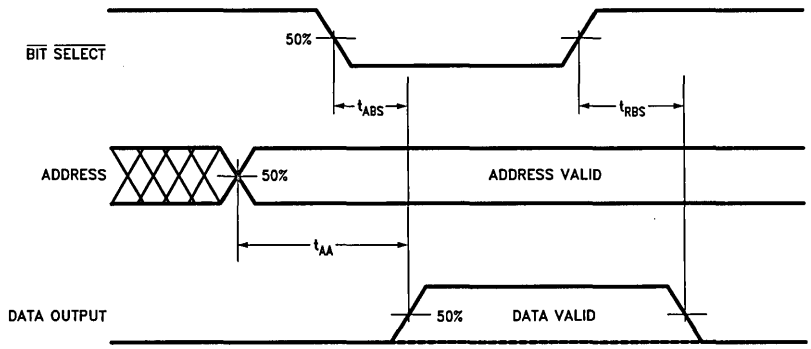
FIGURE 2. AC Test Circuit



TL/D/9642-6

FIGURE 3. Input Levels

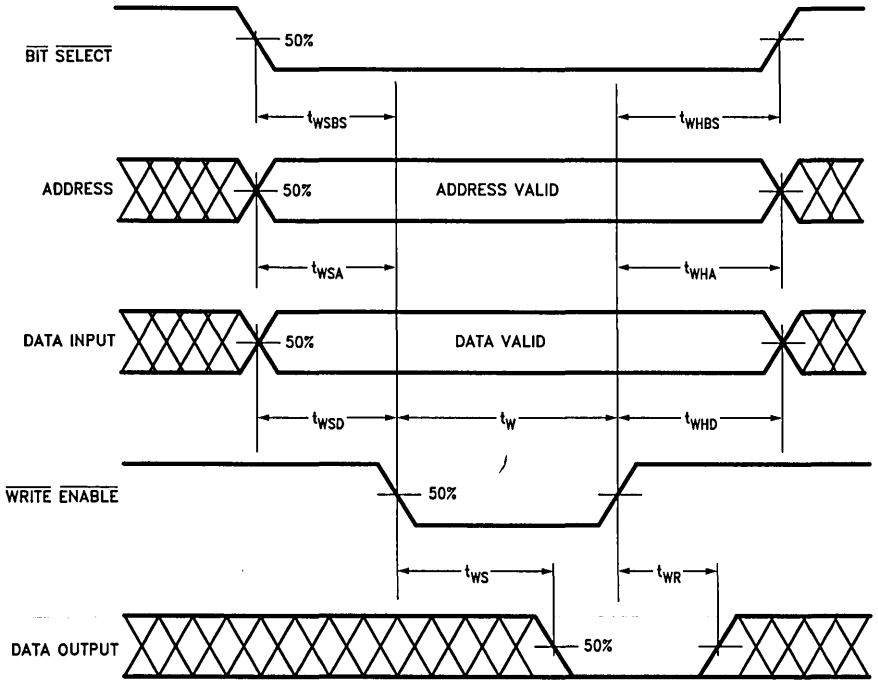
Read Mode



TL/D/9642-8

FIGURE 4. Read Mode Propagation Delay

Write Mode



TL/D/9642–9

FIGURE 5. Write Mode Timing

National Semiconductor

PRELIMINARY

NM100500 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit

General Description

The NM100500 is a 262,144-bit fully static, asyncronous, random access memory organized as 262,144 words by 1 bit. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pin (Q). The output pin will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

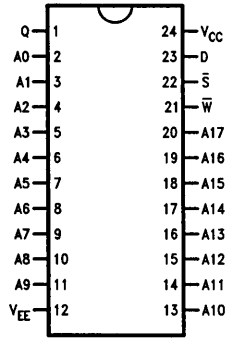
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pin will then be written into the memory address specified on the address pins (A0–A17).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100k ECL I/O
- Power supply −4.2V to −4.8V
- Low power dissipation <1W
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 24-pin flatpak

Connection Diagrams

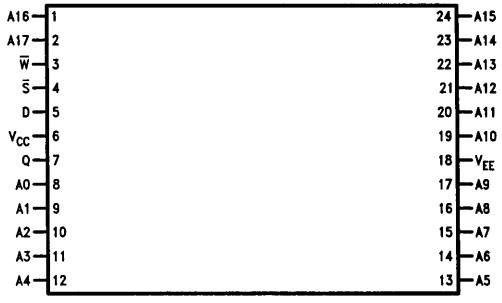
400 Mil Ceramic DIP



TL/D/9708–1

Top View

365 x 535 Ceramic Flatpak (30 Mil Lead Pitch)



TL/D/9708–2

Top View

Pin Names

A0–A17	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q	Data Out
D	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

Above which useful life may be impaired

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Referrence Levels	50% of Input
AC Test Circuit	*Figure 2*

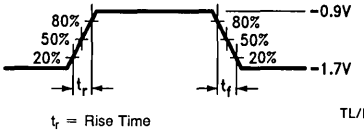
Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

DC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{OHC}	Output HIGH Voltage	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$, Loading with 50Ω to −2.0V	−1025		mV
V_{OLC}	Output LOW Voltage			−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(Min)}$		220	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Max)}$	−50	170	μA
I_{EE}	Power Supply Current	f_o = 50 MHz	−200		mA

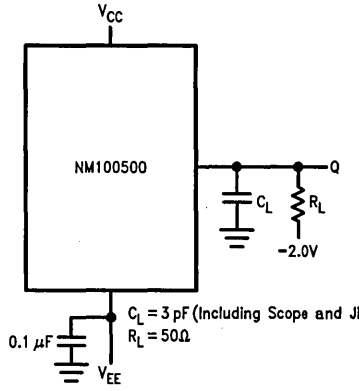
All voltages are referenced to V_{CC} pin = 0V.



TL/D/9708-3

t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels



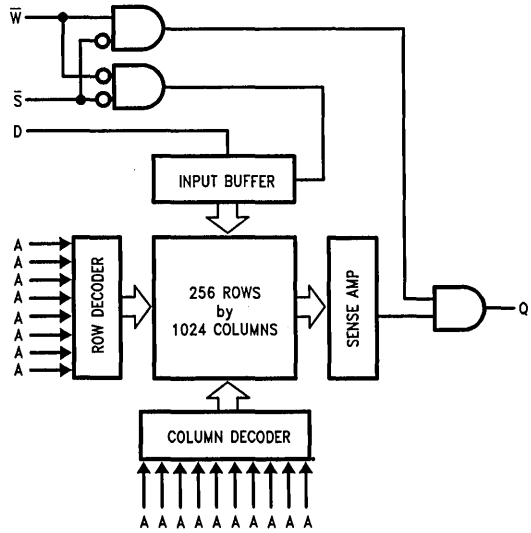
TL/D/9708-4

FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram



TL/D/9708–5

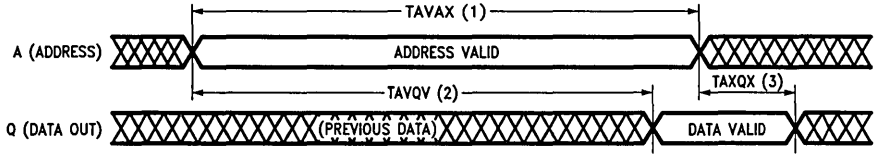
Read Cycles

AC Timing Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	NM100500-15		NM100500-18		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4	ns

Read Cycle 1

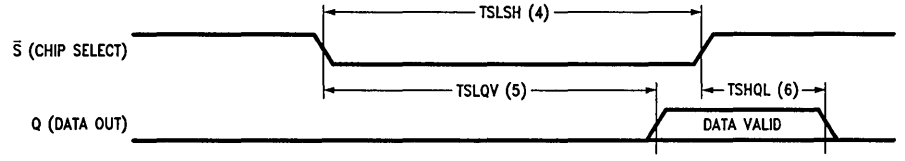
Where $\overline{S}$ is active prior to or within TAVQV–TSLQV after address valid.



TL/D/9708–6

Read Cycle 2

Where address is valid a minimum of TAVQV–TSLQV prior to $\overline{S}$ becoming active.



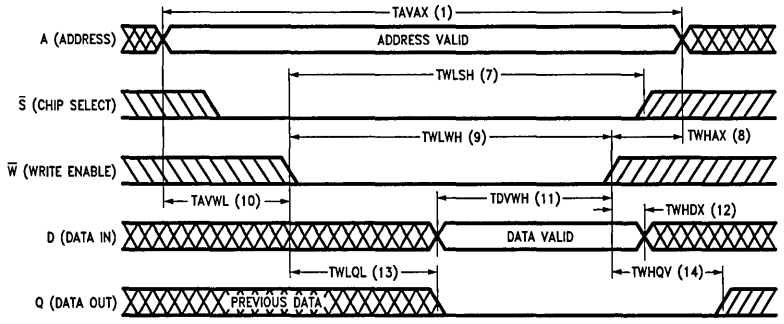
TL/D/9708–7

Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics $V_{EE} = -4.2V$ to $-4.8V$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

No.	Symbol		Parameter	NM100500-15		NM100500-18		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		2		ns
11	TDVWH		Data Valid to Write HIGH	10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		15		18	ns



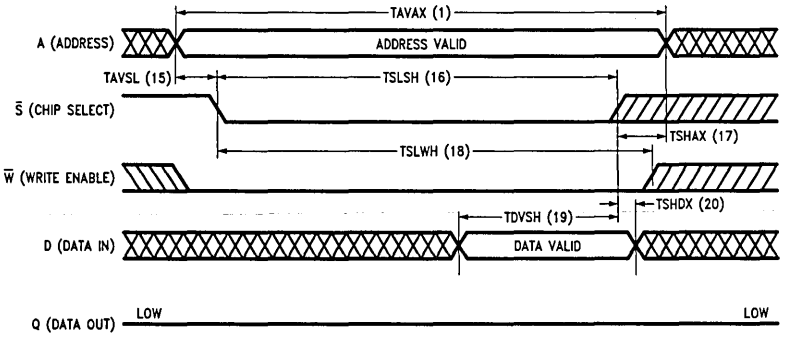
TL/D/9708-8

Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has identical specifications to write cycle 1 with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics $V_{EE} = -4.2V$ to $-4.8V$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

No.	Symbol		Parameter	NM100500-15		NM100500-18		Units
	Std.	Alt.		Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		3		ns



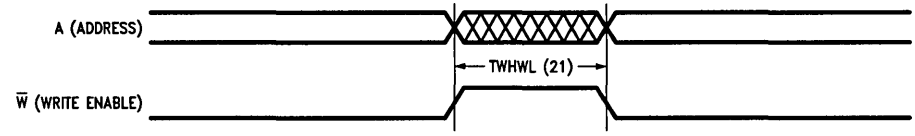
TL/D/9708-9

Consecutive Write Cycles

AC Timing Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C

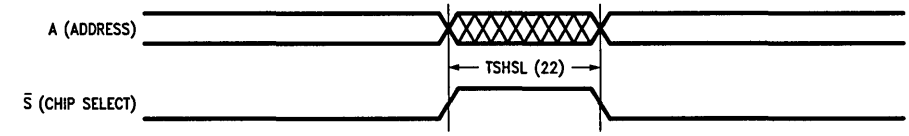
No.	Symbol		Parameter	NM100500-15		NM100500-18		Units
	Std.	Alt.		Min	Max	Min	Max	
21	TWHWL	/TWP	Write Enable HIGH to Write Enable LOW	4		4		ns
22	TSHSL	/TSP	Chip Select HIGH to Chip Select LOW	4		4		ns

Minimum Write Pulse Disable



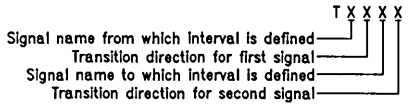
TL/D/9708–10

Minimum Select Pulse Disable



TL/D/9708–11

Standard Timing Parameter Abbreviations



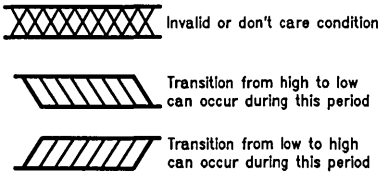
TL/D/9708–12

The transition definitions used in this data sheet are.

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.



TL/D/9708–13

Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM100500	0°C to +85°C	24 Pin Ceramic DIP	NM100500D15/18
NM100500	0°C to +85°C	24 Pin Flatpak	NM100500F15/18

National Semiconductor

PRELIMINARY

NM5100 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit

General Description

The NM5100 is a 262,144-bit fully static, asyncronous, random access memory organized as 262,144 words by 1 bit. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5100 operates with a supply voltage of −5.2V ±5%, yet the input and output voltage levels are temperature compensated 100k ECL compatible.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pin (Q). The output pin will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

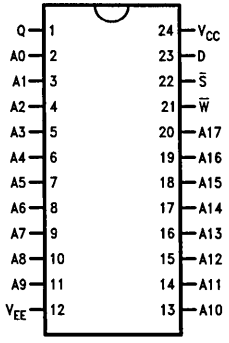
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pin will then be written into the memory address specified on the address pins (A0–A17).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100k ECL I/O
- Power supply −5.2V ±5%
- Low power dissipation <1.1W
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 24-pin flatpack

Connection Diagrams

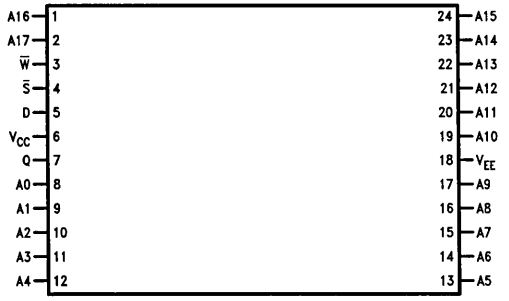
400 Mil Ceramic DIP



TL/D/9451–1

Top View

365 x 535 Ceramic Flatpack (30 Mil Lead Pitch)



TL/D/9451–2

Top View

Pin Names

A0–A17	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q	Data Out
D	Data In
V_{CC}	Ground
V_{EE}	Power

Absolute Maximum Ratings

Above which useful life may be impaired

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Referrence Levels	50% of Input
AC Test Circuit	*Figure 2*

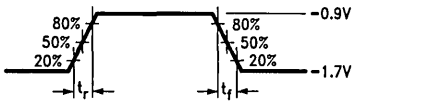
Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

DC Electrical Characteristics V_{EE} = −5.2V ±5%, V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$, Loading with 50Ω to −2.0V	−1025		mV
V_{OLC}	Output LOW Voltage			−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mA
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(Min)}$		220	μA
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(Max)}$	−50	170	μA
I_{EE}	Power Supply Current	f_O = 50 MHz	−200		mA

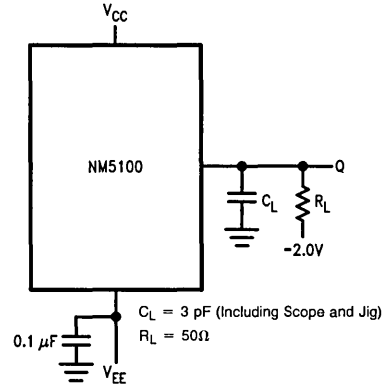
All voltages are referenced to V_{CC} pin = 0V.



TL/D/9451-3

t_R = Rise Time
t_F = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels



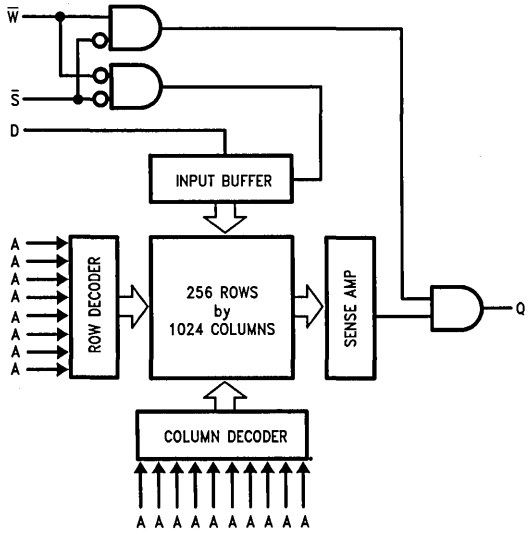
TL/D/9451-4

FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram



TL/D/9451–5

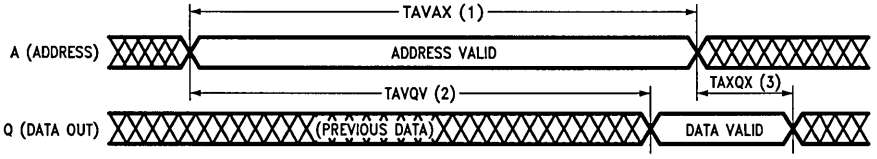
Read Cycles

AC Timing Characteristics $V_{EE} = -5.2V \pm 5\%$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

No.	Symbol		Parameter	NM5100-15		NM5100-18		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4	ns

Read Cycle 1

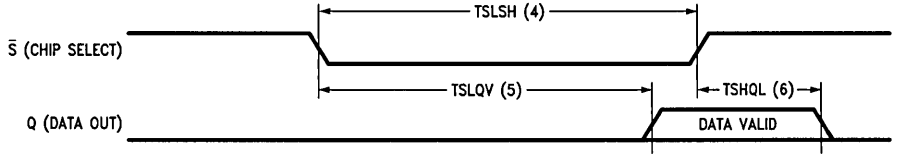
Where $\overline{S}$ is active prior to or within TAVQV-TSLQV after address valid.



TL/D/9451–6

Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.



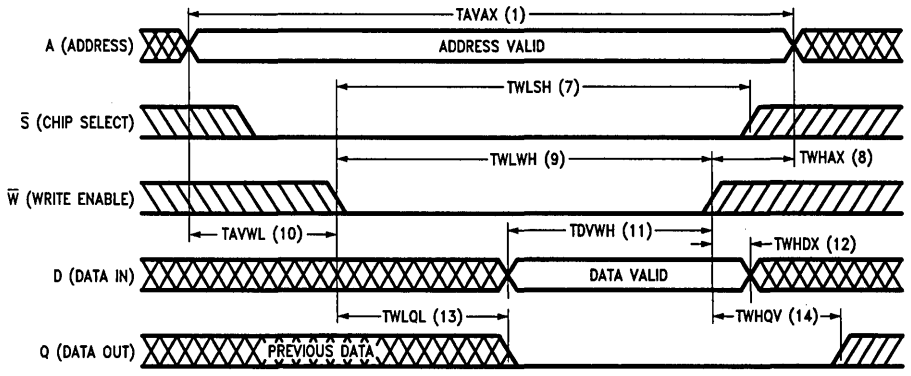
TL/D/9451–7

Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics $V_{EE} = -5.2V \pm 5\%$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

No.	Symbol		Parameter	NM5100-15		NM5100-18		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		2		ns
11	TDVWH		Data Valid to Write HIGH	10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		15		18	ns



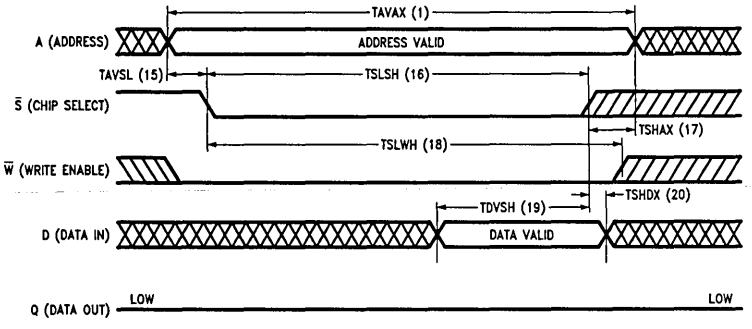
TL/D/9451-8

Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has identical specifications to write cycle 1 with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics $V_{EE} = -5.2V \pm 5\%$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

No.	Symbol		Parameter	NM5100-15		NM5100-18		Units
	Std.	Alt.		Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		3		ns



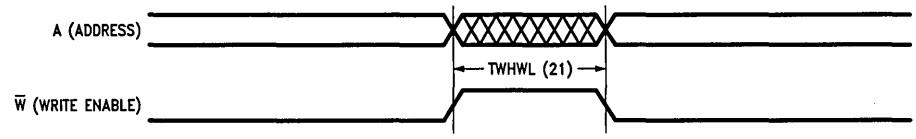
TL/D/9451–9

Consecutive Write Cycles

AC Timing Characteristics $V_{EE} = -5.2V \pm 5\%$, V_{CC} = Ground, $T_C = 0°C$ to $+85°C$

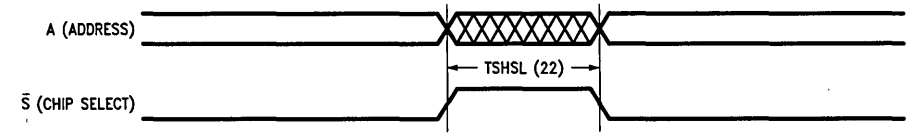
No.	Symbol		Parameter	NM5100-15		NM5100-18		Units
	Std.	Alt.		Min	Max	Min	Max	
21	TWHWL	/TWP	Write Enable HIGH to Write Enable LOW	4		4		ns
22	TSHSL	/TSP	Chip Select HIGH to Chip Select LOW	4		4		ns

Minimum Write Pulse Disable



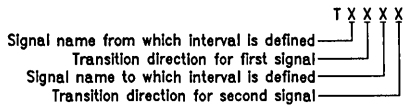
TL/D/9451-10

Minimum Select Pulse Disable



TL/D/9451-11

Standard Timing Parameter Abbreviations



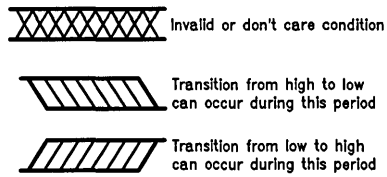
TL/D/9451-12

The transition definitions used in this data sheet are.

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.



TL/D/9451-13

Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM5100	0°C to +85°C	24 Pin Ceramic DIP	NM5100D15/18
NM5100	0°C to +85°C	24 Pin Flatpack	NM5100F15/18

National Semiconductor

ADVANCE INFORMATION

NM100494/NM4494
64k BiCMOS SRAM 16k x 4

General Description

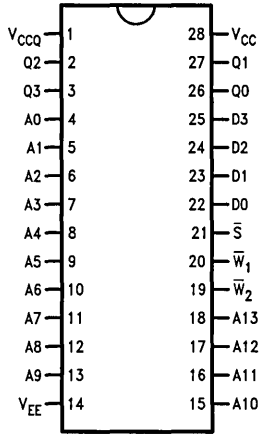
The NM100494/NM4494 are 65,536-bit fully static, asynchronous random access memories organized as 16,384 words by 4 bits. The NM100494/NM4494 are based on National's advanced one micron BiCMOS process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of this high performance technology and a speed optimized circuit design results in a very high-speed memory device.

Features

- 12 ns T_{AA}, T_{WC} over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated 100k ECL I/O
- Low power dissipation—less than 1W @ 50 MHz
- Soft error rates less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS process technology
- 200 mA latch-up immunity
- 28-pin ceramic DIP/28-pin ceramic flatpak
- NM100494: power supply = −4.2V to −4.8V
- NM4494: power supply = −5.2V ± 5%

Connection Diagrams

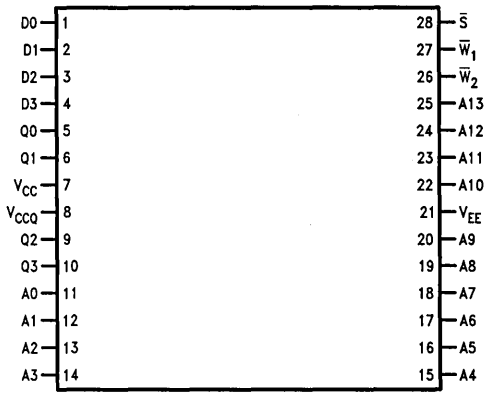
28-Pin Ceramic DIP



TL/D/9744-1

Top View

28-Pin Ceramic Flatpak (30 Mil Lead Pitch)



TL/D/9744-2

Top View

5

National Semiconductor

ADVANCE INFORMATION

NM100504/NM5104
256k BiCMOS SRAM 64k x 4

General Description

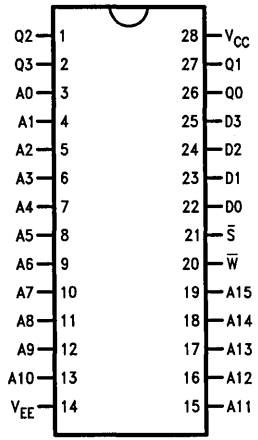
The NM100504/NM5104 are 262,144-bit fully static, asynchronous, random access memories organized as 65,536 words by 4 bits. The NM100504/NM5104 are based on National's advanced one micron BiCMOS process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of this high performance technology and a speed optimized circuit design results in a very high-speed memory device.

Features

- 15 ns T_{AA}, T_{WC} over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100k ECL I/O
- Low power dissipation < 1W @ 50 MHz
- Soft error rates less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS process technology
- 200 mA latch-up immunity
- 28-pin ceramic DIP/28-pin ceramic flatpak
- NM100504: power supply = −4.2V to −4.8V
- NM5104: power supply = −5.2V ±5%

Connection Diagrams

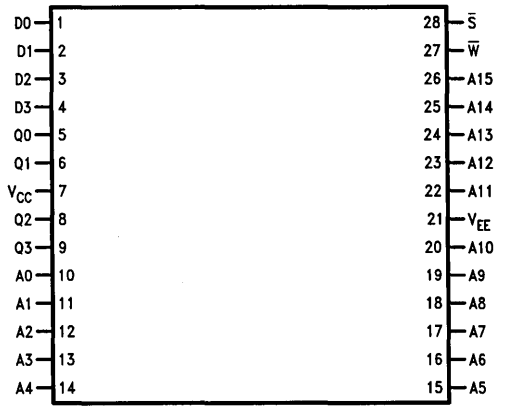
28-Pin Ceramic DIP



TL/D/9745-1

Top View

28-Pin Ceramic Flatpak (30 Mil Lead Pitch)



TL/D/9745-2

Top View

National Semiconductor

ADVANCE INFORMATION

NM100490/NM4490
64k BiCMOS SRAM 64k x 1

General Description

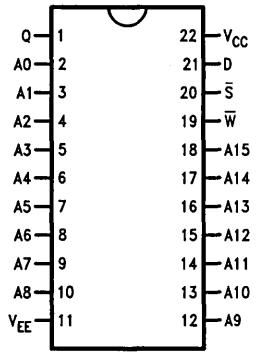
The NM100490/NM4490 are 65,536-bit fully static, asynchronous, random access memories organized as 65,536 words by 1 bit. The NM100490/NM4490 are based on National's advanced one micron BiCMOS process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of this high performance technology and a speed optimized circuit design results in a very high-speed memory device.

Features

- 12 ns T_{AA}, T_{WC} over the commercial temperature range
- Balanced read and write cycles.
- Write cycle timing allows for 33% of cycle time for system skew.
- Temperature compensated F100k ECL I/O
- Low power dissipation < 1W
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS process technology
- 200 mA latch-up immunity
- 22-pin ceramic DIP
- NM100490: Power supply = −4.2V to −4.8V
- NM4490: Power supply = −5.2V to ±5%

Connection Diagram

22-Pin Ceramic DIP



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Top View

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Section 6

TTL I/O Static RAMs

Section 6 Contents

National Semiconductor

TTL I/O-MOS Static RAM Selection Guide

Part Number	Organization	Outputs	Pins	Access Time	Temperature Range
TTL I/O STATIC RAMS					
DM54S189	16 x 4	TS	16	50	−55°C to +125°C
DM54S189A	16 x 4	TS	16	30	−55°C to +125°C
DM74S189	16 x 4	TS	16	35	0°C to +70°C
DM74S189A	16 x 4	TS	16	25	0°C to +70°C
DM74S289	16 x 4	OC	16	35	0°C to +70°C
93415	1k x 1	OC	16	45 60	0°C to +70°C −55°C to +125°C
93415A	1k x 1	OC	16	30 40	0°C to +70°C −55°C to +125°C
93415-25	1k x 1	OC	16	25	−55°C to +125°C
93415-20	1k x 1	OC	16	20	0°C to +70°C
93L415	1k x 1	OC	16	60 70	0°C to +70°C −55°C to +125°C
93L415A	1k x 1	OC	16	45 50	0°C to +70°C −55°C to +125°C
93L415-25	1k x 1	OC	16	25	−55°C to +125°C
93L415-20	1k x 1	OC	16	20	0°C to +70°C
93422	256 x 4	TS	22	45 60	0°C to +70°C −55°C to +125°C
93422A	256 x 4	TS	22	35 45	0°C to +70°C −55°C to +125°C
93L422	256 x 4	TS	22	60 75	0°C to +70°C −55°C to +125°C
93L422A	256 x 4	TS	22	45 55	0°C to +70°C −55°C to +125°C
93L422-30	256 x 4	TS	22	30	−55°C to +125°C
93L422-25	256 x 4	TS	22	25	0°C to +70°C
93425	1k x 1	TS	16	45 60	0°C to +70°C −55°C to +125°C
93425A	1k x 1	TS	16	30 40	0°C to +70°C −55°C to +125°C
93425-25	1k x 1	TS	16	25	−55°C to +125°C
93425-20	1k x 1	TS	16	20	0°C to +70°C
93L425	1k x 1	TS	16	60 70	0°C to +70°C −55°C to +125°C

TTL I/O-MOS Static RAM Selection Guide (Continued)

Part Number	Organization	Outputs	Pins	Access Time	Temperature Range
TTL I/O STATIC RAMS (Continued)					
93L425A	1k x 1	TS	16	45 50	0°C to +70°C −55°C to +125°C
93L425-25	1k x 1	TS	16	25	−55°C to +125°C
93L425-20	1k x 1	TS	16	20	0°C to +70°C
93479	256 x 9	TS	22	45 60	0°C to +70°C −55°C to +125°C
93479A	256 x 9	TS	22	35 45	0°C to +70°C −55°C to +125°C
MOS STATIC RAMS					
NMC2147H	4k x 1	TS	18	70	0°C to +70°C
NMC2147H-3	4k x 1	TS	18	55	0°C to +70°C
NMC2147H-2	4k x 1	TS	18	45	0°C to +70°C
NMC2147H-1	4k x 1	TS	18	35	0°C to +70°C
NMC2147H-3L	4k x 1	TS	18	55	0°C to +70°C
NMC2148H	1k x 4	TS	18	70	0°C to +70°C
NMC2148H-3	1k x 4	TS	18	55	0°C to +70°C
NMC2148H-2	1k x 4	TS	18	45	0°C to +70°C
NMC2148H-1	1k x 4	TS	18	70	0°C to +70°C
NMC2148H-3L	1k x 4	TS	18	55	0°C to +70°C
1600A-55	64k x 1	TS	22	55	−55°C to +125°C
1600A-45	64k x 1	TS	22	45	−55°C to +125°C
NM1600-35 1600A-35	64k x 1	TS	22	35	0°C to +70°C −55°C to +125°C
NM1600-30 1600A-30	64k x 1	TS	22	30	0°C to +70°C −55°C to +125°C
NM1600-25	64k x 1	TS	22	25	0°C to +70°C
1601A-55	64k x 1	TS	22	55	−55°C to +125°C
1601A-45	64k x 1	TS	22	45	−55°C to +125°C
NM1601-35 1601A-35	64k x 1	TS	22	35	0°C to +70°C −55°C to +125°C
NM1601-30 1601A-30	64k x 1	TS	22	30	0°C to +70°C −55°C to +125°C
NM1601-25	64k x 1	TS	22	25	0°C to +70°C
1620-55	16k x 4	TS	22	55	−55°C to +125°C
1620-45	16k x 4	TS	22	45	−55°C to +125°C
NM1620-35 1620-35	16k x 4	TS	22	35	0°C to +70°C −55°C to +125°C
NM1620-30 1620-30	16k x 4	TS	22	30	0°C to +70°C −55°C to +125°C
NM1620-25	16k x 4	TS	22	25	0°C to +70°C
1621-55	16k x 4	TS	22	55	−55°C to +125°C

TTL I/O-MOS Static RAM Selection Guide (Continued)

Part Number	Organization	Outputs	Pins	Access Time	Temperature Range
MOS STATIC RAMS (Continued)					
1621-45	16k x 4	TS	22	45	−55°C to +125°C
NM1621-35 1621-35	16k x 4	TS	22	35	0°C to +70°C −55°C to +125°C
NM1621-30 1621-30	16k x 4	TS	22	30	0°C to +70°C −55°C to +125°C
1621-25	16k x 4	TS	22	25	0°C to +70°C
1624-55	16k x 4	TS	24	55	−55°C to +125°C
1624-45	16k x 4	TS	24	45	−55°C to +125°C
NM1624-35 1624-35	16k x 4	TS	24	35	0°C to +70°C −55°C to +125°C
NM1624-30 1624-30	16k x 4	TS	24	30	0°C to +70°C −55°C to +125°C
NM1624-25	16k x 4	TS	24	25	0°C to +70°C
1625-55	16k x 4	TS	24	55	−55°C to +125°C
1625-45	16k x 4	TS	24	45	−55°C to +125°C
NM1625-35 1625-35	16k x 4	TS	24	35	0°C to +70°C −55°C to +125°C
NM1625-30 1625-30	16k x 4	TS	24	30	0°C to +70°C −55°C to +125°C
NM1625-25	16k x 4	TS	24	25	0°C to +70°C
EDGE-TRIGGERED REGISTERS					
DM75S68	16k x 4	TS	16	55	−55°C to +125°C
DM75S68A	16k x 4	TS	16	45	−55°C to +125°C
DM85S68	16k x 4	TS	16	40	0°C to +70°C
DM85S68A	16k x 4	TS	16	24	0°C to +70°C

National Semiconductor

DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE® RAM DM54S189A/DM74S189A High Speed 64-Bit TRI-STATE RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM74S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S189 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

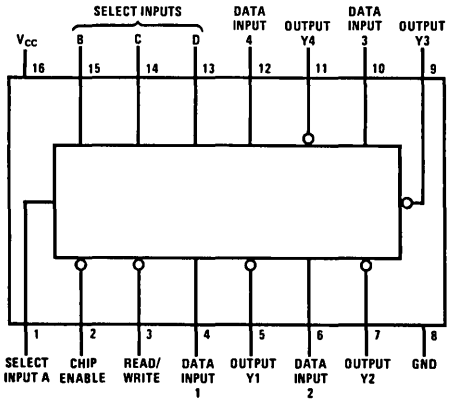
The fast access time of the DM74S189A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM74S189A outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (S189A)
  - Access from chip-enable input 17 ns max
  - Access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads (S189, S189A)
- DM74S289 are functionally equivalent and have open-collector outputs
- DM54SXXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



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Top View

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Order Number DM54S189J, DM54S189AJ, DM74S189J, DM74S189AJ, DM74S189N or DM74S189AN
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

DM54S189, DM74S189 Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		V
I_{CEX}	High Level Output Current Open Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V	DM54S189, DM74S189	−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V	DM54S189, DM74S189			50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V	DM54S189, DM74S189	−50			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S189 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189(A)	4.5	5.5	V
DM74S189(A)	4.75	5.25	V
Temperature (T_A)			
DM54S189(A)	−55	+125	°C
DM74S189(A)	0	+70	°C

DM54S189A, DM74S189A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189A	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189A	2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−20		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM54S189A, DM74S189A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189A			DM74S189A			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			11	25		11	17	ns
t_{CZL}	Output Enable Time to Low Level				11	25		11	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189(A) and across the 0°C to +70°C range for the DM74S189(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

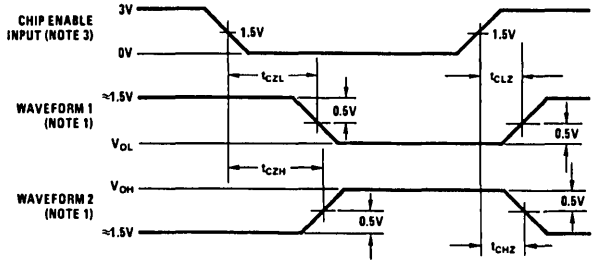
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

DM54S189(A), DM74S189(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



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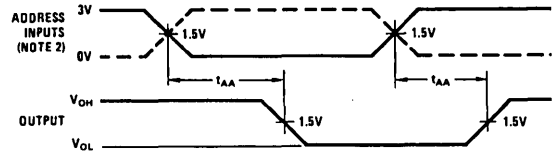
Access Time from Address Inputs



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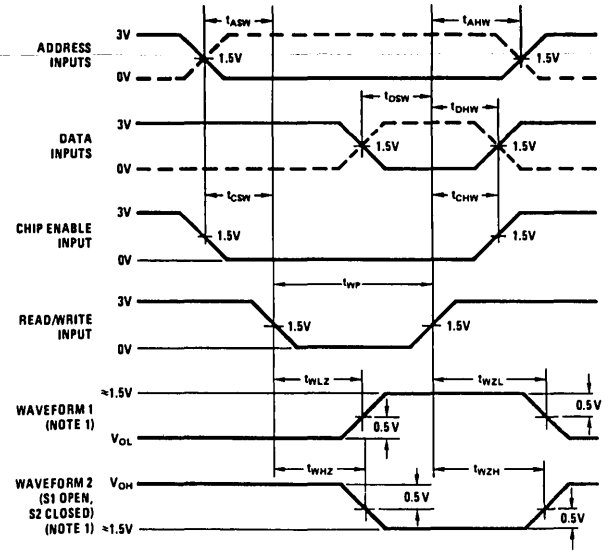
Write Cycle



TL/D/9232-4

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} = \approx 50\Omega$.

Block Diagram

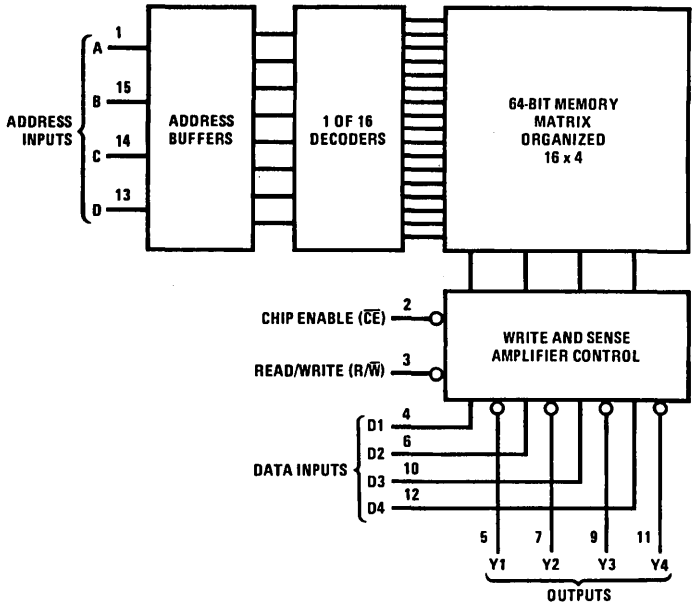


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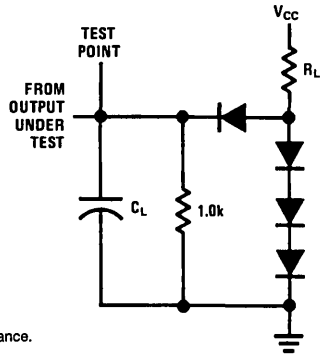
FIGURE 3

AC Test Circuits

DM54S189(A)/DM74S189(A)



C_L includes probe and jig capacitance.
All diodes are 1N3064.

TL/D/9232–6

FIGURE 4

National Semiconductor

DM74S289
64-Bit (16 x 4) Open-Collector RAM TRI-STATE® RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S289 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

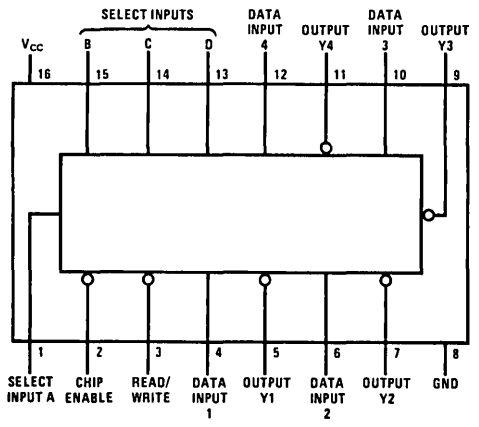
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

Features

- Commercial address access time 25 ns
- Features open-collector output
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74S289J or DM74S289N
See NS Package Number J16A or N16E

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM74S289	4.75	5.25	V
Temperature (T_A)			
DM74S289	0	+70	°C

DM74S289 Electrical Characteristics

Over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −6.5 mA	2.4	3.2		V
I_{CEX}	High Level Output Current	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA				0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{CC}	Supply Current (Note 4)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S289 Switching Characteristics

Over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM74S289 Min	DM74S289 Typ (Note 2)	DM74S289 Max	Units
t_{AA}	Access Time from Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω *(Figure 4)*		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			12	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	20	ns
t_{WLH}	Disable Time from Read/Write				13	25	ns
t_{WP}	Width of Enable Pulse (Read/Write Low)			25			ns
t_{ASW}	Setup Time *(Figure 2)*	Address to Read/Write		0			ns
t_{DSW}		Data to Read/Write		25			ns
t_{CSW}		Chip-Enable to Read/Write		0			ns
t_{AHW}	Hold Time *(Figure 2)*	Address from Read/Write		0			ns
t_{DHW}		Data from Read/Write		0			ns
t_{CHW}		Chip-Enable from Read/Write		0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.

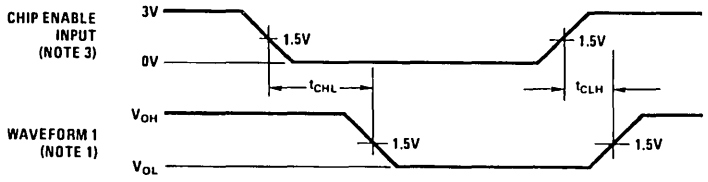
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to −70°C range for the DM74S189/289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: I_{CC} is measured with all inputs grounded, and the outputs open.

DM74S289 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



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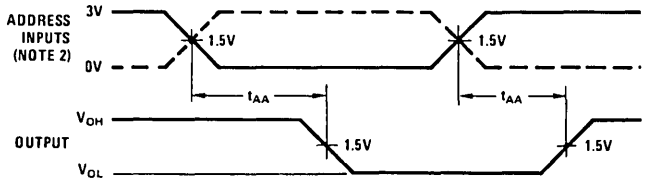
Access Time from Address Inputs



TL/D/9693-3

Write Cycle

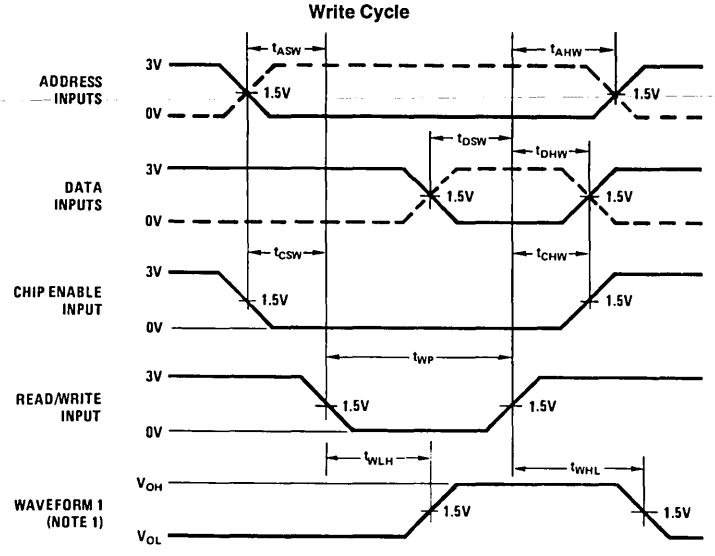


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FIGURE 2

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. PRR ≤ 1 MHz and $Z_{OUT} = 50\Omega$.

Block Diagram

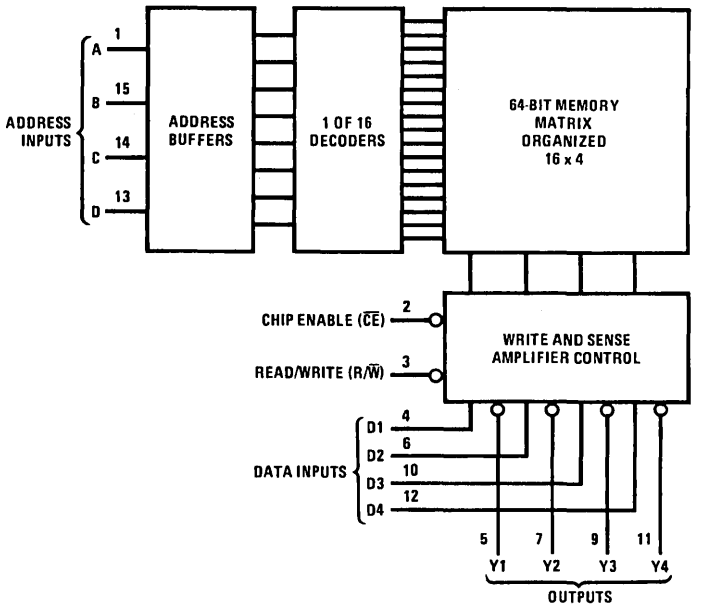

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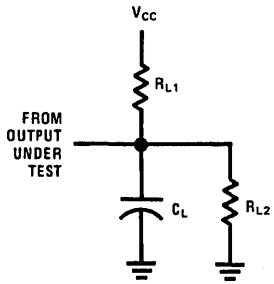
FIGURE 3

AC Test Circuit



TL/D/9693–6

National Semiconductor

93415/93L415 1024 x 1-Bit Static Random Access Memory

General Description

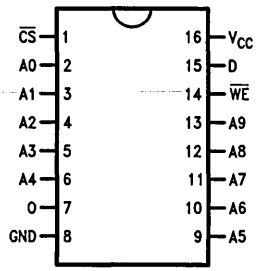
The 93415 is a 1024-bit read write Random Access Memory RAM, organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- Commercial address access time
  93415—25 ns to 60 ns max
- Military address access time
  93415—30 to 70 ns max
- Low power version also available (93L415)
- Features open collector output
- Power dissipation decreases with increasing temperature

Connection Diagrams

16-Pin DIP



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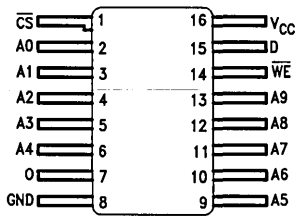
Top View

Order Number 93415ADC, 93415DC, 93415DC25, 93415DMQB, 93415DMQB30, 93415DMQB40, 93415APC, 93415PC, 93415PC25, 93L415ADC, 93L415DC, 93L415DC35, 93L415DMQB, 93L415DMQB50, 93L415APC, 93L415PC, 93L415PC35, 93L415DMQB, 93L415DMQB40 or 93L415DMQB50
See NS Package Numbers J16A* and N16E*

*For most current package information, contact product marketing.

16-Pin Flatpak



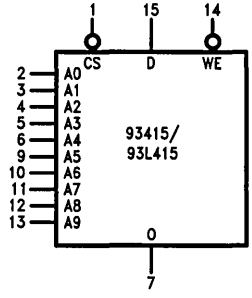
TL/D/9671–2

Top View

Order Number 93415FMQB, 93415FMQB30, 93415FMQB40, 93L415FMQB, 93L415FMQB40 or 93L415FMQB50
See NS Package Number W16A*

*For most current package information, contact product marketing.
Optional Processing QR = Burn-In

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

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Pin Names

$\overline{CS}$	Chip Select Input Active LOW
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input Active LOW
D	Data Input
O	Data Output

6

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1			V	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)
I_{IL}	Input LOW Current		−180	−300	μA	V_{CC} = Max, V_{IN} = 0.4V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = Max, V_{OUT} = 4.5V
I_{CC}	Power Supply Current		65	65 75 125 135	mA mA mA mA	93L415-Commercial 93L415-Military 93415-Commercial 93415-Military

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering 10 sec.)	300°C
Maximum Junction Temperature (T_j)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level (2.4V)
L = LOW Voltage Level (0.45V)
X = Don't Care (HIGH or LOW)

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

Commercial

AC Electrical Characteristics (Note 6) V_{CC} = 5.0 ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	93415-25		93415-30 93415A		93415-45 93415		Units	Conditions
		Min	Max	Min	Max	Min	Max		
READ TIMING									
t_{ACS}	Chip Select Access Time		15		20		35	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		15		20		35	ns	
t_{AA}	Address Access Time (Note 7)		25		30		45	ns	
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 8)	20		20		35		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write (Note 8)	5		5		5		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		15		20		35	ns	
t_{WR}	Write Recovery Time		15		20		40	ns	
t_{WR}	Write Recovery Time (93415A)				25			ns	

Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	93415-30		93415-40 93415A		93415-60 93415		Units	Conditions
		Min	Max	Min	Max	Min	Max		
READ TIMING									
t_{ACS}	Chip Select Access Time		20		25		40	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		20		25		50	ns	
t_{AA}	Address Access Time (Note 7)		30		40		60	ns	
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 8)	25		25		40		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write (Note 8)	5		10		15		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		20		25		50	ns	

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Tested under static condition only.

Note 5: Functional testing done at input levels $V_{IH} = V_{OL(Max)}$ (0.45V) and $V_{IH} = V_{OH(Min)}$ (2.4V).

Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 8: t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Commercial

AC Electrical Characteristics (Note 6) V_{CC} = 5.0 ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	93L415-35		93L415-45 93L415A		93L415-60 93L415		Units	Conditions
		Min	Max	Min	Max	Min	Max		
READ TIMING									
t_{ACS}	Chip Select Access Time		25		30		40	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		40	ns	
t_{AA}	Address Access Time (Note 7)		25		45		60	ns	
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 8)	20		35		45		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write (Note 4)	5		5		10		ns	
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		30		35		45	ns	

Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	93L415-40		93L415-50 93L415A		93L415-70 93L415		Units	Conditions
		Min	Max	Min	Max	Min	Max		
READ TIMING									
t_{ACS}	Chip Select Access Time		30		35		45	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		50	ns	
t_{AA}	Address Access Time (Note 7)		40		50		70	ns	
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 8)	35		40		50		ns	*Figure 4*
t_{WSD}	Data Setup Time Prior to Write	5		5		10		ns	
t_{WHD}	Data Hold Time after Write	5		5		10		ns	
t_{WSA}	Address Setup Time Prior to Write (Note 8)	10		10		10		ns	
t_{WHA}	Address Hold Time after Write	5		5		10		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		10		ns	
t_{WS}	Write Enable to Output Disable		25		30		45	ns	
t_{WR}	Write Recovery Time		30		40		55	ns	

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Tested under static condition only.

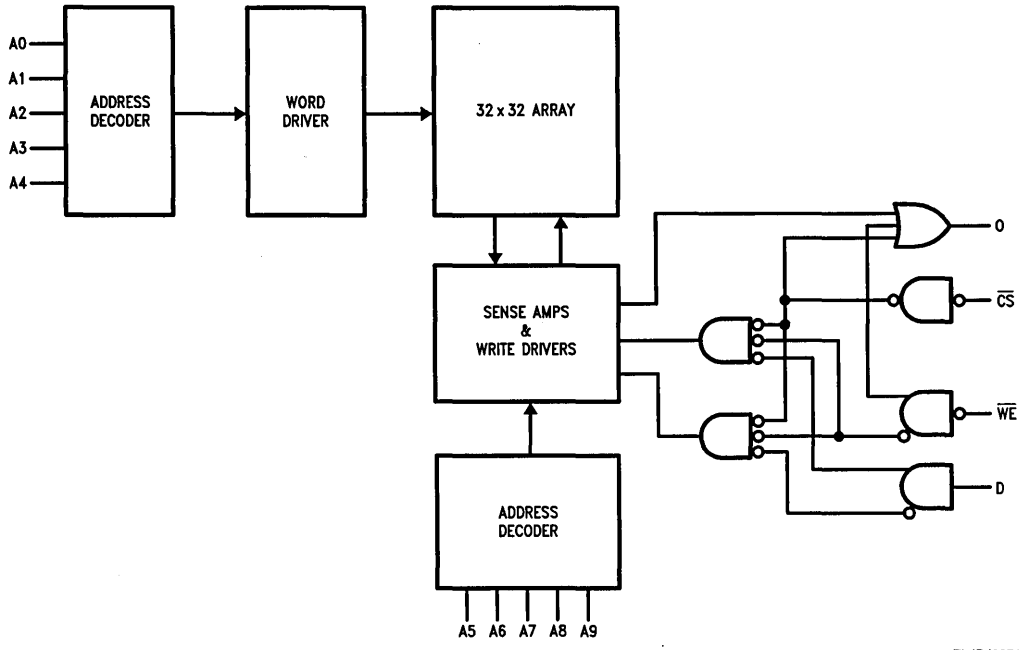
Note 5: Functional testing done at input levels $V_{IH} = V_{OL(Max)}$ (0.45V) and $V_{IH} = V_{OH(Min)}$ (2.4V).

Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 8: t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9671–4

Functional Description

The 93415 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 through A9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93415 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A0 through A9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

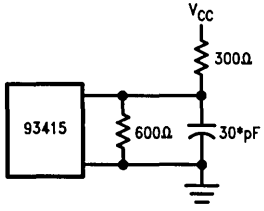
$$\frac{V_{CC}\,(Max)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(Min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

One Unit Load = 40 μA HIGH/1.6 mA LOW.

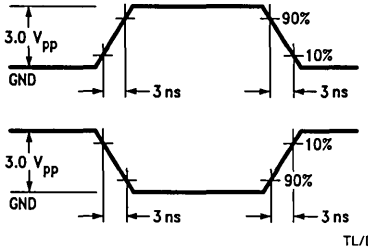
FO_{MAX} = 5 UL.



TL/D/9671-5

*Includes jig and probe capacitance

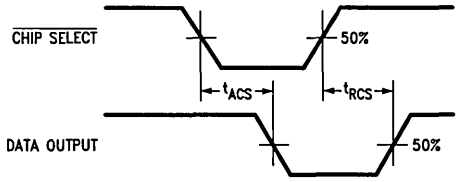
FIGURE 1. AC Test Circuit



TL/D/9671-6

FIGURE 2. AC Test Input Levels

a. Read Mode Propagation Delay from Chip Select



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b. Read Mode Propagation Delay from Address

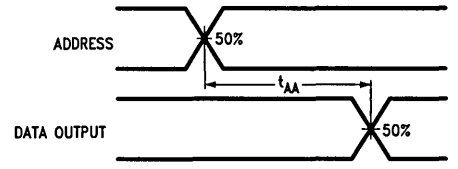

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FIGURE 3. Read Mode Timing

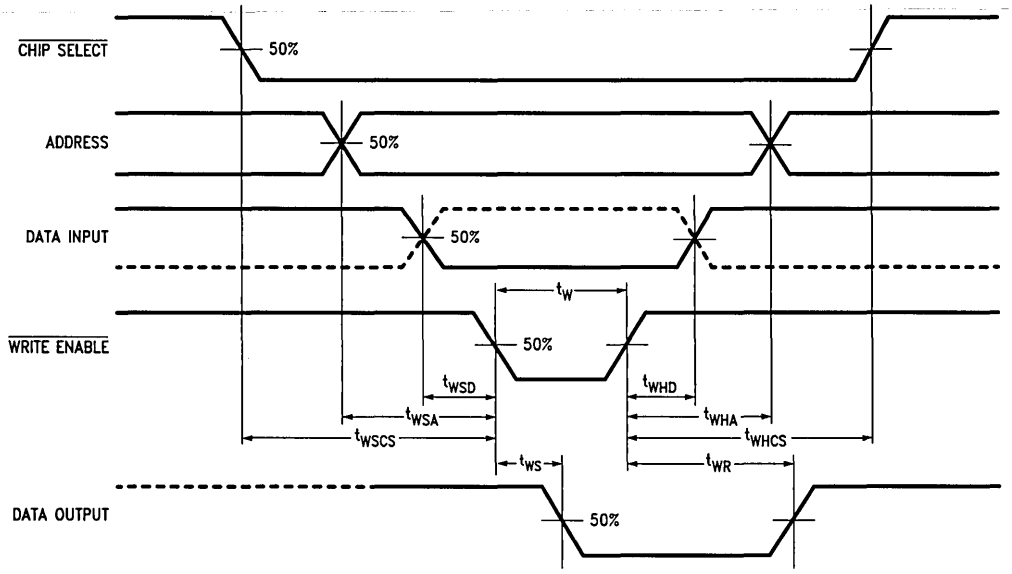

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FIGURE 4. Write Mode Timing

Notes:

Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Input voltage levels for worst case AC test are 3.0/0.0V.

National Semiconductor

ADVANCE INFORMATION

93L415A 1024 x 1-Bit Static Random Access Memory

General Description

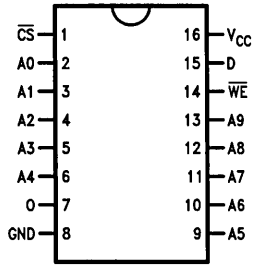
The 93L415A is a 1024-bit read write Random Access Memory RAM, organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

Features

- New design to replace old 93415/93L415
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L415A 25 ns max
- Military address access time
  93L415A 30 ns max
- Features open collector output
- Power dissipation decreases with increasing temperature

Connection Diagrams

16-Pin DIP



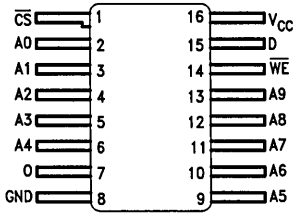
TL/D/10003-1

Top View

Order Number 93L415ADC, 93L415ADMQB or 93L415APC
See NS Package Number J16A* and N16E*

*For most current package information, contact product marketing.

16-Pin Flatpak



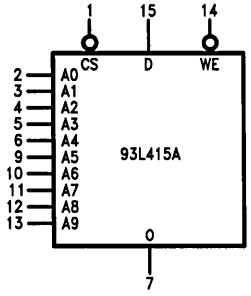
TL/D/10003-2

Top View

Order Number 93L415AFMQB
See NS Package Number W16A*

*For most current package information, contact product marketing.

Logic Symbol



TL/D/10003-3

V_{CC} = Pin 16
GND = Pin 8

Pin Names

$\overline{CS}$	Chip Select Input Active LOW
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input Active LOW
D	Data Input
O	Data Output

National Semiconductor

93422
256 x 4-Bit Static Random Access Memory

General Description

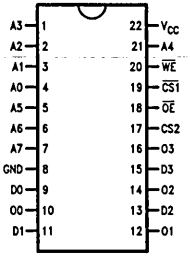
The 93422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

Features

- Commercial address acces time
  - — 93422—35 ns to 45 ns Max
  - — 93422A
- Military address access time
  - — 93422—45 to 60 ns Max
  - — 93422A
- Fully TTL compatible
- Features TRI-STATE® outputs
- Power dissipation decreases with increasing temperature

Connection Diagrams

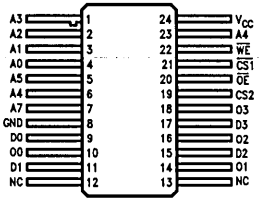
22-Pin DIP



TL/D/9672-1

Top View
Order Number 93422DC, 93422ADC, 93422PC, 93422APC, 93422DMQB or 93422ADMQB
See NS Package Numbers J22A and N22A*

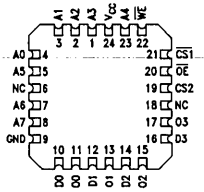
24-Pin Flatpak



TL/D/9672-2

Top View
Order Number 93422FMQB or 93422AFMQB
See NS Package Number W24C*

24-Pin Leadless Chip Carrier



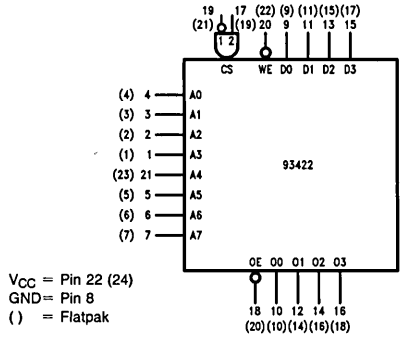
TL/D/9672-4

Top View
Order Number 93422LMQB or 93422ALMQB
NS Package Number E24B*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Logic Symbol



V_{CC} = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

TL/D/9672-3

Pin Names

A0–A7	Address Inputs
D0–D3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O0–O3	Data Outputs

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Absolute Maximum Ratings:

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temp. (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

DC Electrical Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8 mA			0.3	0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)		2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)				0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−150	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V			1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA			−1.0	−1.5	V
I_{OZH} I_{OZL}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V				50 −50	μA
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max (Note 7)		−10		−70	mA
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND All Outputs Open	Commercial			120	mA
			Military			130	

Commercial

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3c)*		30		30	ns
t_{ZRCS}	Chip Select to HIGH Z			30		30	ns
t_{AOS}	Output Enable Access Time			30		30	ns
t_{ZROS}	Output Enable to HIGH Z			30		30	ns
t_{AA}	Address Access Time (Note 8)			35		45	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	25		30		ns
t_{WSD}	Data Setup Time Prior to Write		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			35		35	ns
t_{WR}	Write Recovery Time			35		40	ns

Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3c)*		35		45	ns
t_{ZRCS}	Chip Select to HIGH Z			35		45	ns
t_{AOS}	Output Enable Access Time			35		45	ns
t_{ZROS}	Output Enable to HIGH Z			35		45	ns
t_{AA}	Address Access Time (Note 8)			45		60	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	35		40		ns
t_{WSD}	Data Setup Time Prior to Write		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			40		45	ns
t_{WR}	Write Recovery Time			40		50	ns

Note 1: Either input voltage limit or input current limit sufficient to protecting inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} − $V_{OL\ (max)}$ (0.45V), V_{IH} − $V_{OH\ (min)}$ (2.4V).

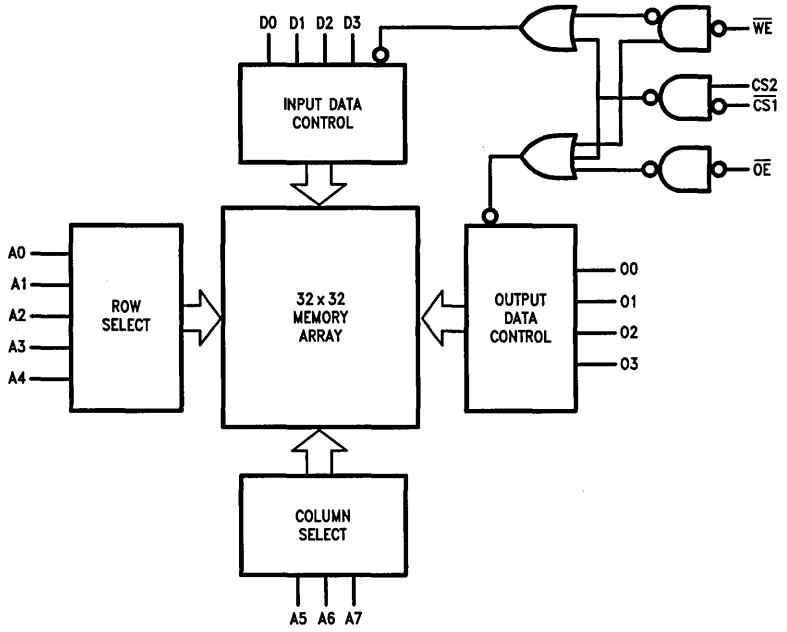
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9672–5

Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	TRI-STATE	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4V)
L = LOW Voltage Level (0.45V)
X = Don't Care (HIGH or LOW)
HIGH Z = High-Impedance

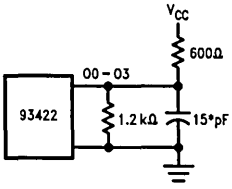
Functional Description

The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A0–A7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D0–D3 is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least t_{WSD} (Min) plus t_W (Min) plus t_{WHD} (Min) to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O0–O3).

The 93422 has TRI-STATE outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.



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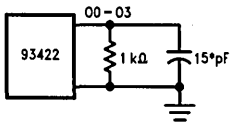
Load A



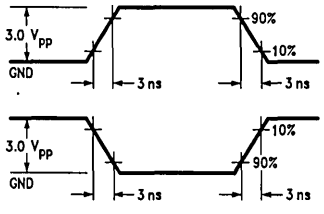
TL/D/9672-7

Load B

*Includes jig and probe capacitance.

Note: Load A is used for all production testing.

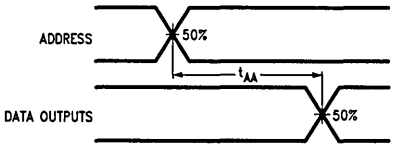
FIGURE 1. AC Test Output Load



TL/D/9672-8

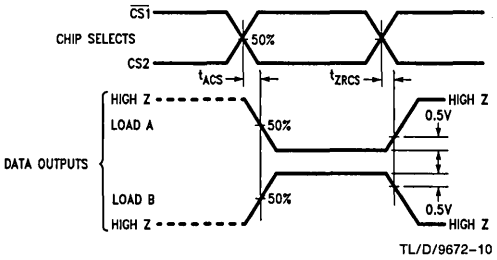
FIGURE 2. AC Test Input Levels

a. Read Mode Propagation Delay from Address



TL/D/9672-9

b. Read Mode Propagation Delay from Chip Select



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c. Read Mode Propagation Delay from Output Enable

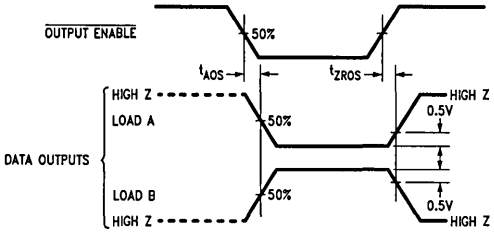

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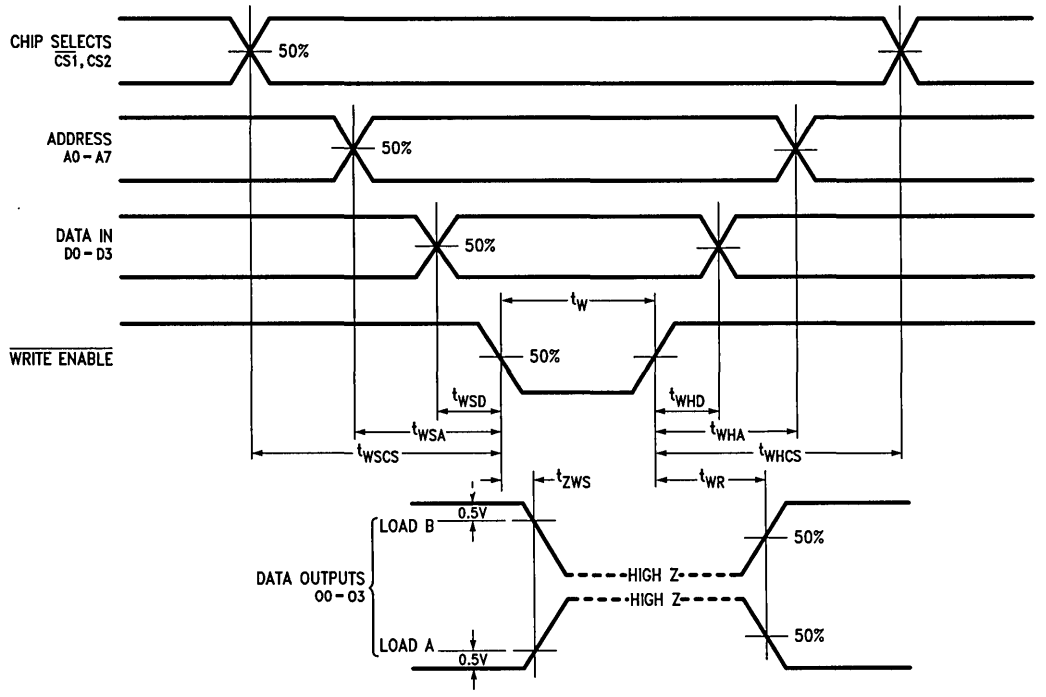
FIGURE 3. Read Mode Timing

6



TL/D/9672–12

Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V/0.0V.

FIGURE 4. Write Mode Timing

National Semiconductor

93L422
256 x 4-Bit Static Random Access Memory

General Description

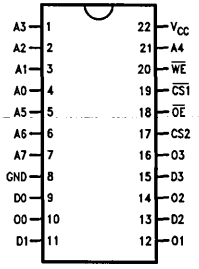
The 93L422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

Features

- Commercial address access time
  93L422—45 ns to 60 ns max
- Military address access time
  93L422—55 ns to 75 ns max
- Fully TTL compatible
- Features TRI-STATE® outputs
- Power dissipation decreases with increasing temperature
- Standard processing includes burn-in

Connection Diagrams

22-Pin DIP

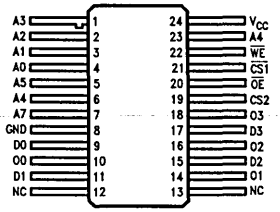


TL/D/9673-1

Top View

Order Number 93L422DC, 93L422ADC, 93L422PC, 93L422APC, 93L422DMQB or 93L422ADMQB
See NS Package Number J22A* or N22A*

24-Pin Flatpak

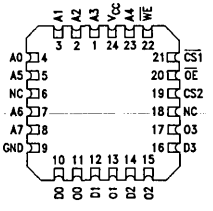


TL/D/9673-2

Top View

Order Number 93L422FMQB or 93L422AFMQB
See NS Package Number W24C*

24-Pin Leadless Chip Carrier



TL/D/9673-4

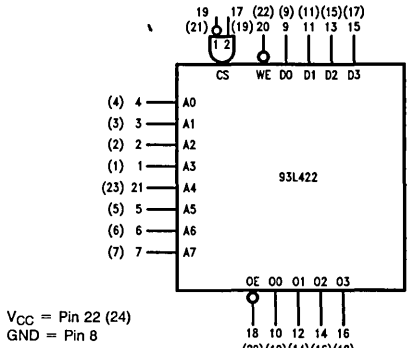
Top View

Order Number 93L422LMQB or 93L422ALMQB
See NS Package Number E24B*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

Logic Symbol



V_{CC} = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

TL/D/9673-3

Pin Names

A0–A7	Address Inputs
D0–D3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O0–O3	Data Outputs

6

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8 mA				0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)		2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)				0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−150	−300	μA
I_{IH}	Input HIGH Curent	V_{CC} = Max, V_{IN} = 4.5V			10	40	μA
I_{IHE}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}				10	mA
V_{IO}	Input Diode Cramp Voltage	V_{CC} = Max, I_{IN} = −10 mA			−1.0	−1.5	V
I_{OZH} I_{OZL}	Output Current HIGH Z	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V				50 −50	μA
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max (Note 7)		−10		−70	mA
I_{CC}	Power Supply Current	Commercial Military	V_{CC} = Max, All Inputs GND All Outputs Open		65	80 90	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Commercial

Symbol	Parameter	Conditions	A		STD		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b, 3c*		30		35	ns
t_{ZRCS}	Chip Select to HIGH Z			30		35	ns
t_{AOS}	Output Enable Access Time			30		35	ns
t_{ZROS}	Output Enable to HIGH Z			30		35	ns
t_{AA}	Address Access Time (Note 8)			45		60	ns

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IH} = $V_{OL\ (max)}$ (0.45V) and V_{IH} = $V_{OH\ (min)}$ (2.4V).

Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} Min t_{WSA} measured at t_W Min.

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C (Continued)

Commercial (Continued)

Symbol	Parameter	Conditions	A		STD		Units
			Min	Max	Min	Max	
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*		30	45		ns
t_{WSD}	Data Setup Time Prior to Write		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			35		40	ns
t_{WR}	Write Recovery Time			40		45	ns

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Military

Symbol	Parameter	Conditions	A		STD		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b, 3c*		40		45	ns
t_{ZRCS}	Chip Select to HIGH Z			40		45	ns
t_{AOS}	Output Enable Access Time			40		45	ns
t_{ZROS}	Output Enable to HIGH Z			40		45	ns
t_{AA}	Address Access Time (Note 8)			55		75	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*	40		55		ns
t_{WSD}	Data Setup Time Prior to Write		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			45		45	ns
t_{WR}	Write Recovery Time			50		50	ns

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels $V_{IH} = V_{OL\ (max)}$ (0.45V) and $V_{IH} = V_{OH\ (min)}$ (2.4V).

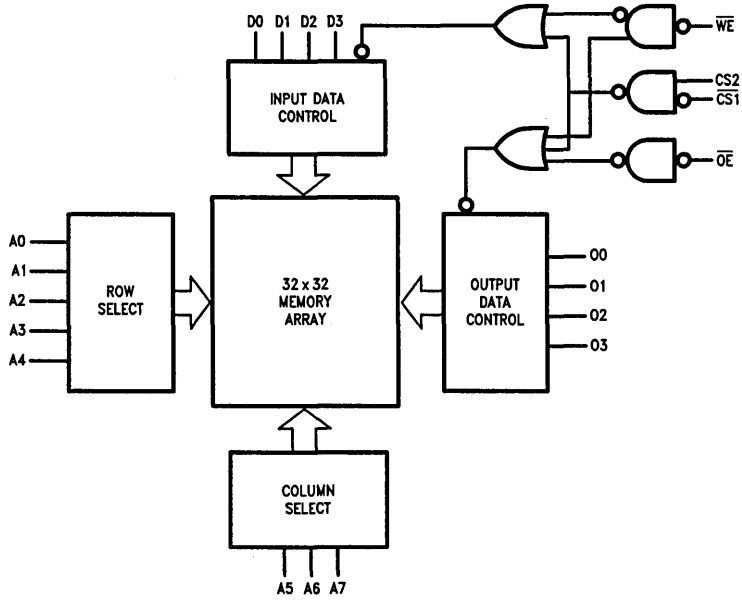
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} Min t_{WSA} measured at t_W Min.

Logic Diagram



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Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS}_1$	CS_2	$\overline{WE}$	TRI-STATE	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High-Impedance

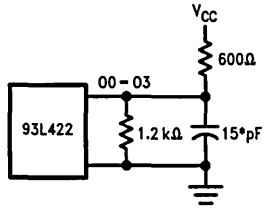
Functional Description

The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address A0–A7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

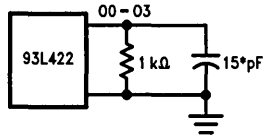
The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D0–D3 is written into the address location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD\ (Min)}$ plus $t_{W\ (Min)}$ plus $t_{WHD\ (Min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected Non-inverted data is then presented at the outputs (O0–O3).

The 93L422 has TRI-STATE outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.



TL/D/9673-6

Load A



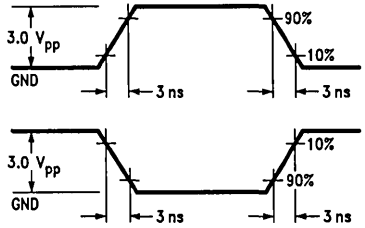
TL/D/9673-7

Load B

*Includes jig and probe capacitance

Note: Load A is used for all production testing

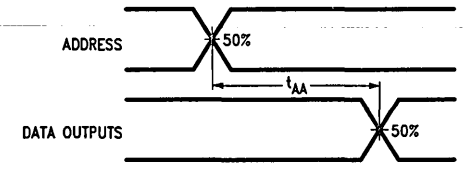
FIGURE 1. AC Test Output Load



TL/D/9673-8

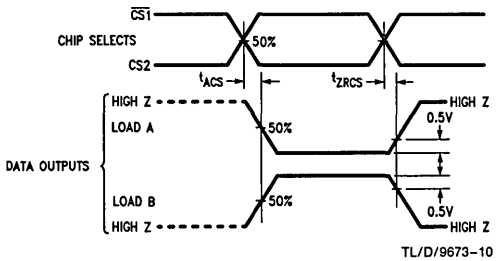
FIGURE 2. AC Test Input Levels

3a. Read Mode Propagation Delay from Address



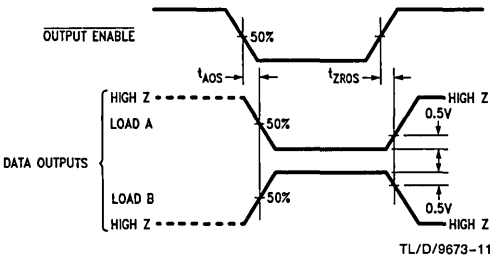
TL/D/9673-9

3b. Read Mode Propagation Delay from Chip Select



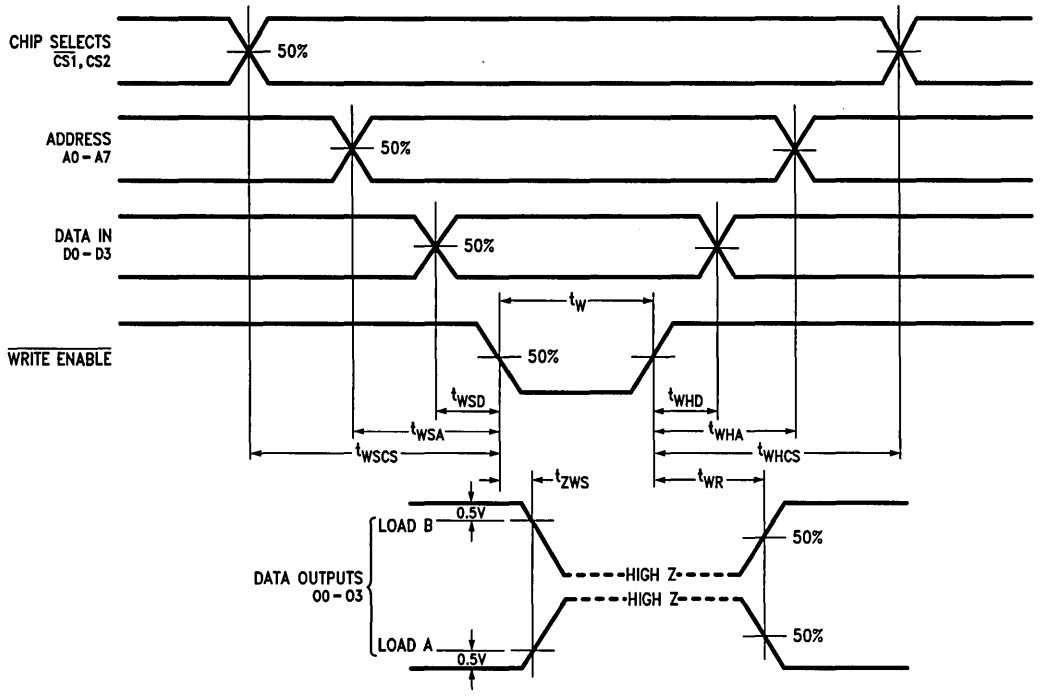
TL/D/9673-10

3c. Read Mode Propagation Delay from Output Enable



TL/D/9673-11

FIGURE 3. Read Mode Timing



TL/D/9673–12

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimum cycle time Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V–0V.

National Semiconductor

ADVANCE INFORMATION

93L422A
256 x 4-Bit Static Random Access Memory

General Description

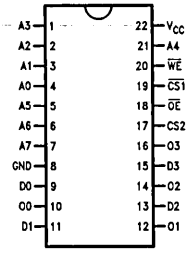
The 93L422A is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

Features

- New design to replace old 93422/93L422
- Improved ESD threshold
- Alpha hard without die coat
- Commercial address access time
  93L422A — 25 ns max
- Military address access time
  93L422A — 30 ns max
- Fully TTL compatible
- Features TRI-STATE® outputs
- Power dissipation decreases with increasing temperature

Connection Diagrams

22-Pin DIP

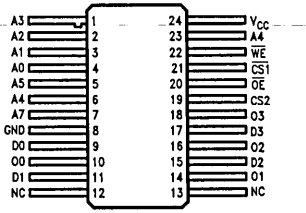


TL/D/9996-1

Top View

Order Number 93L422ADC, 93L422APC or 93L422ADMQB
See NS Package Number J22A* or N22A*

24-Pin Flatpak

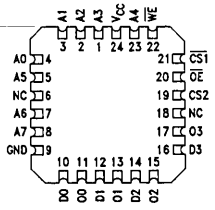


TL/D/9996-2

Top View

Order Number 93L422AFMQB
See NS Package Number W24C*

24-Pin Leadless Chip Carrier



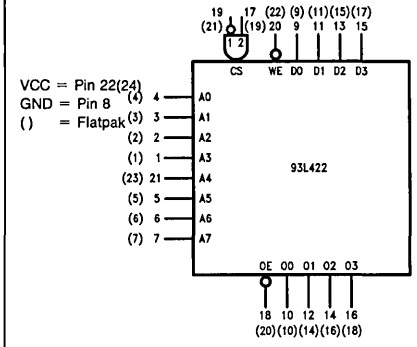
TL/D/9996-4

Top View

Order Number 93L422ALMQB
See NS Package Number ???

*For most current package information, contact product marketing

Logic Symbol



TL/D/9996-3

Pin Names

A0–A7	Address Inputs
D0–D3	Data Inputs
$\overline{CS}_1$	Chip Select Input (Active LOW)
CS_2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O0–O3	Data Outputs

6

National Semiconductor

93425/93L425
1024 x 1-Bit Static Random Access Memory

General Description

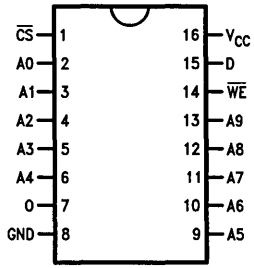
The 93425 is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output as well as an active LOW Chip Select line.

Features

- Commercial address access time 953425—20 to 60 ns max
- Military address access time 93425—30 to 70 ns max
- Low power version also available (93L425)
- Features TRI-STATE® output
- Power dissipation decreases with increasing temperature
- Standard processing includes burn-in

Connection Diagram

16-Pin DIP



TL/D/9674-1

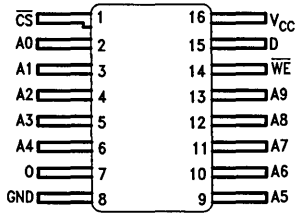
Top View

Order Number 93425DC, 93425ADC, 93425DC25, 93425DMQB, 93425DMQB40, 93425DMQB50, 93425PC, 93425APC, 93425PC25, 93L425DC, 93L425ADC, 93L425DC25, 93L425DMQB, 93L425DMQB40, 93L425DMQB50, 93L425PC, 93L425APC or 93L425PC25
See NS Package Number J16A* or N16E*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Flatpak



TL/D/9674-2

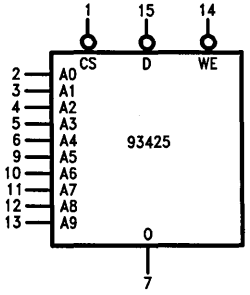
Top View

Order Number 93425FMQB, 93425AFMQB, 93L425FMQB40, 93L425FMQB, 93L425AFMQB or 93L425FMQB50
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

TL/D/9674-3

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1			V	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Max, I_{OH} = −5.2 mA
I_{IL}	Input LOW Current		−180	−300	μA	V_{CC} = Max, V_{IN} = 0.4V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, V_{IN} = −10 mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V
I_{OS}	Output Current Short Circuit to Ground (Note 7)			−100	mA	V_{CC} = Max, (Note 7)
I_{CC}	Power Supply Current		60	65 75 125 135	mA mA mA mA	93L425 Commercial 93L425 Military 93425 Commercial 93425 Military

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V. T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = $V_{OL\ Max}$ (0.45V), V_{IH} = $V_{OH\ Min}$ (2.4V).

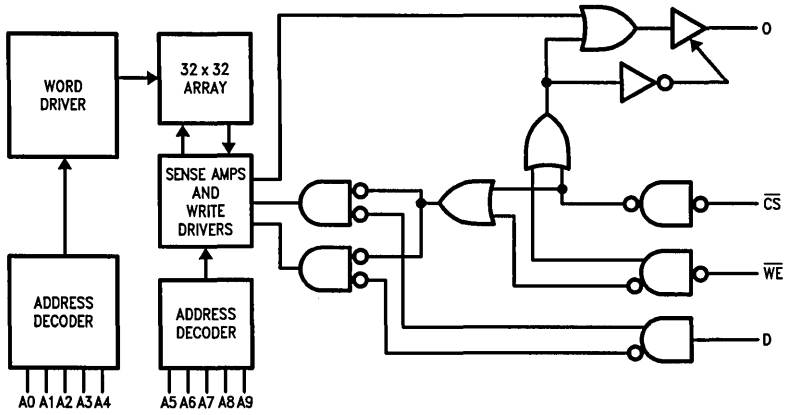
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9674–4

Functional Description

The 93425 is a fully decoded 1024-bit read write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0–A9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93425 are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A0 through A9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

The 93425 has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	H	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write 0
L	L	H	HIGH Z	Write 1
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High Impedance State

Commercial

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	93425-25		93425-30 93425A		93425-45 93425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		15		20		35	ns
t_{ZRCS}	Chip Select to HIGH Z			15		20		35	ns
t_{AA}	Address Access Time (Note 8)			25		30		45	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	20		20		35		ns
t_{WSD}	Data Setup Time prior to Write		5		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			15		20		35	ns
t_{WR}	Write Recovery Time			15		20		40	ns
t_{WR}	Write Recovery Time (93425A)					25			ns

Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	Conditions	93425-25		93425-40 93425A		93425-60 93425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		20		25		45	ns
t_{ZRCS}	Chip Select to HIGH Z			20		25		50	ns
t_{AA}	Address Access Time (Note 8)			30		40		60	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	25		25		40		ns
t_{WSD}	Data Setup Time prior to Write		5		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		10		15		ns
t_{WHA}	Address Hold Time after Write		5		5		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			20		25		45	ns
t_{WR}	Write Recovery Time			20		25		50	ns

Notes on preceding page.

Commercial

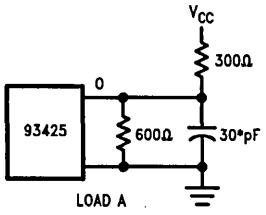
AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	93L425-35		93L425-45 93L425A		93L425-60 93L425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		25		30		40	ns
t_{ZRCS}	Chip Select to HIGH Z			25		30		40	ns
t_{AA}	Address Access Time (Note 8)			35		45		60	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figures 4a, 4b)*	30		35		45		ns
t_{WSD}	Data Setup Time prior to Write		5		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		5		10		ns
t_{WHA}	Address Hold Time after Write		5		5		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			20		25		45	ns
t_{WR}	Write Recovery Time			30		35		45	ns

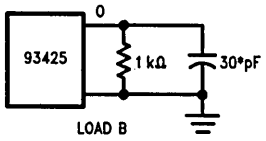
Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	Conditions	93L425-40		93L425-50 93L425A		93L425-70 93L425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		30		35		45	ns
t_{ZRCS}	Chip Select to HIGH Z			25		30		50	ns
t_{AA}	Address Access Time (Note 8)			40		50		70	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figures 4a, 4b)*	35		40		50		ns
t_{WSD}	Data Setup Time prior to Write		5		5		10		ns
t_{WHD}	Data Hold Time after Write		5		5		10		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		10		10		10		ns
t_{WHA}	Address Hold Time after Write		5		5		10		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		10		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			25		30		45	ns
t_{WR}	Write Recovery Time			25		40		55	ns



TL/D/9674-5

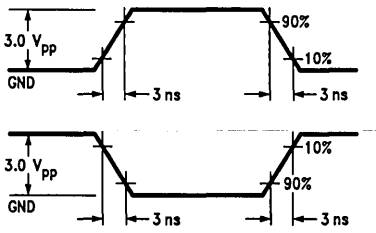


TL/D/9674-6

Note: Load A is used for all production testing.

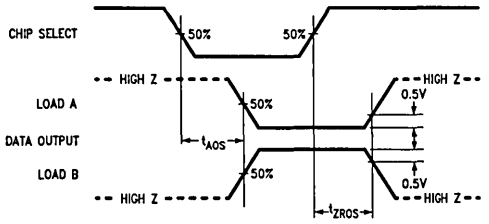
*Includes jig and probe capacitance

FIGURE 1. AC Test Output Load



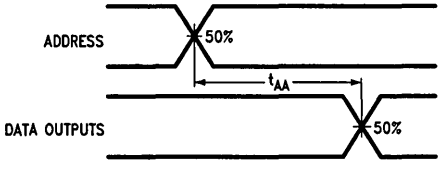
TL/D/9674-7

FIGURE 2. AC Test Input Levels



TL/D/9674-8

3a. Read Mode Propagation Delay from Chip Select

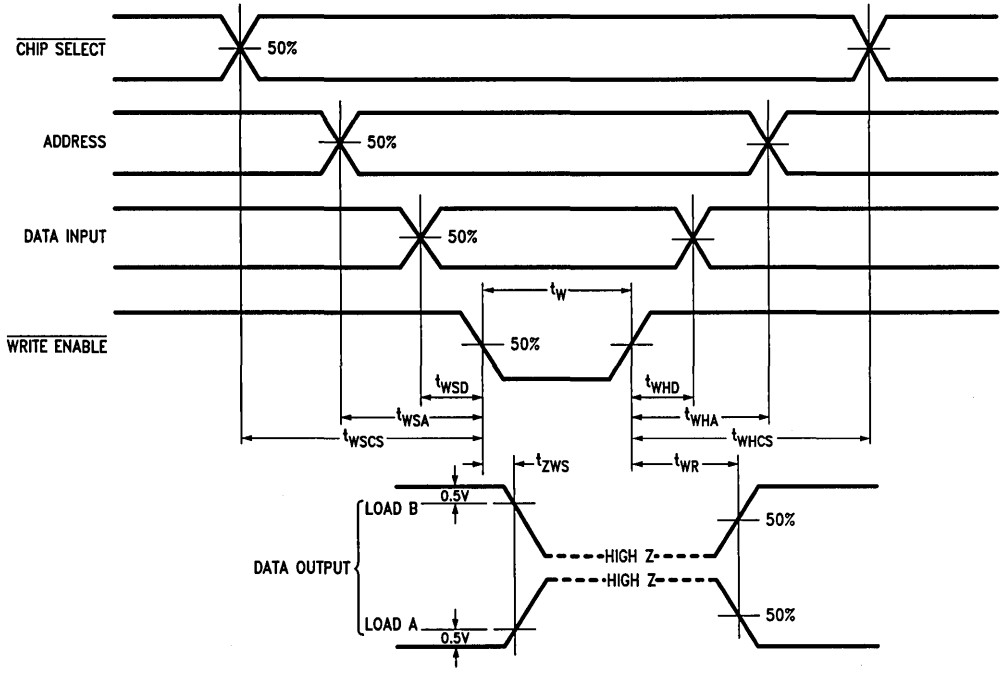


TL/D/9674-9

3b. Read Mode Propagation Delay from Address

FIGURE 3. Read Mode Timing

6



TL/D/9674–10

Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0/0.0V.

FIGURE 4. Write Mode Timing

National Semiconductor

ADVANCE INFORMATION

93L425A
1024 x 1-Bit Static Random Access Memory

General Description

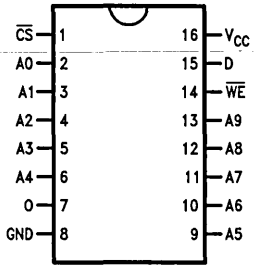
The 93L425A is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output as well as an active LOW Chip Select line.

Features

- New design to replace old 93L425/93425
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L425A 25 ns max
- Military address access time
  93L425A 30 ns max
- Features TRI-STATE® output
- Power dissipation decreases with increasing temperature

Connection Diagram

16-Pin DIP



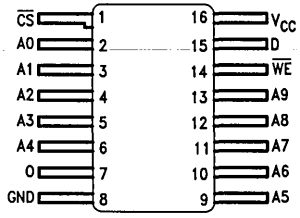
TL/D/10004-1

Top View

Order Number 93L425ADC, 93L425ADMQB or 93L425APC
See NS Package Number J16A* or N16E*

*For most current package information, contact product marketing.

16-Pin Flatpak



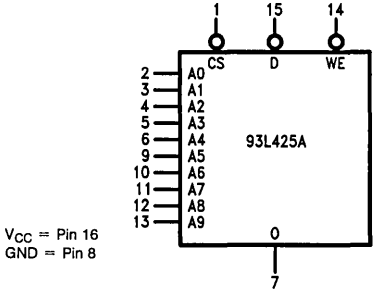
TL/D/10004-2

Top View

Order Number 93L425AFMQB
See NS Package Number W16A*

*For most current package information, contact product marketing.

Logic Symbol



TL/D/10004-3

Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A0–A9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

6

National Semiconductor

93479
256 x 9-Bit Static Random Access Memory

General Description

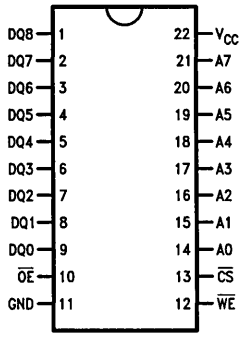
The 93479 is a 2304-bit read/write Random Access Memory (RAM), organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

Features

- Commercial address time
  93479—45 ns max
  93479A—35 ns max
- Military address access time
  93479—60 ns max
  93479A—45 ns max
- Common data input/output
- Features TRI-STATE® output

Connection Diagrams

22-Pin Ceramic DIP



TL/D/9675-1

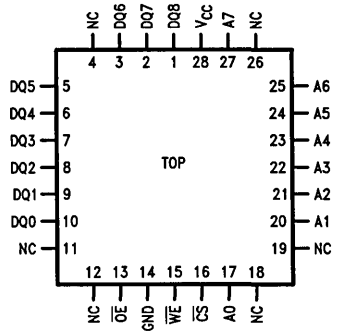
Top View

Order Number 93479DC, 93479ADC, 93479DMQB or 93479ADMQB
See NS Package Number J22A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn In

28-Pin LCC



TL/D/9675-3

Top View

Order Number 93479LMQB or 93479ALMQB
See NS Package Number E28A*

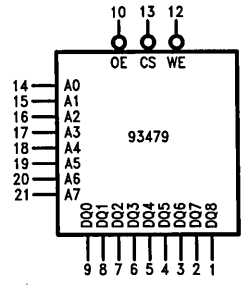
*For most current package information, contact product marketing.

Optional Processing QR = Burn In

Pin Names

A0–A7	Address Inputs
DQ0–DQ8	Data Input Outputs
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
NC	No Connect

Logic Symbol



V_{CC} = Pin 22
GND = Pin 11

TL/D/9675-2

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Notes 1, 2)	−0.5V to V_{CC} (RAMs) −1.5V to V_{CC} (PROMs)
Voltage Applied to Outputs (Notes 2, 3) (Output HIGH)	−0.5V to +5.5V (RAMs) −1.5V to +5.5V (PROMs)
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V. T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = $V_{OL\ (Max)}$ (0.45V), V_{IH} = $V_{OH\ (Min)}$ (2.4V).

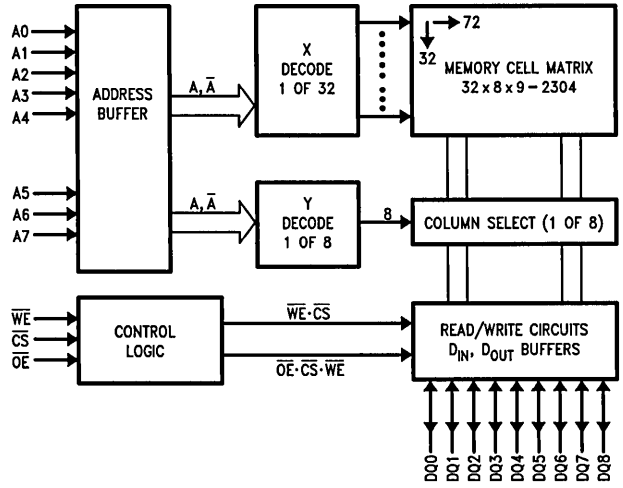
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9675–4

Functional Description

The 93479 is a fully decoded 2304-bit random access memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address A0–A7.

The Chip Select input provides for memory array expansion. For larger memories the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected and the output disabled, the data at DQ0–DQ8 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected and the output enabled. Non-inverted data is then presented at the outputs DQ0–DQ8.

The 93479 has TRI-STATE outputs which provide an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-ups provide drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

Truth Table

Inputs			Data In/Out DQ0–DQ8	Mode
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$		
X	H	X	HIGH Z	Output Disabled
H	X	X	HIGH Z	R W Disabled
L	L	H	Data Out	Read
L	H	L	Data In	Write

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.5V
X = Don't Care HIGH or LOW
HIGH Z = High Impedance State

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA				0.5	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2 mA		2.4			V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)		2.1			V
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V			−250	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V			1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V			 −50	50 −400	μA μA
V_C	Input Diode Clamp Voltage	V_{CC} = Max, V_{IN} = −10 mA			−1.0	−1.5	V
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max, (Note 7)				−70	mA
I_{CC}	Power Supply Current	Commercial Military	V_{CC} = Max All Inputs GND			185 200	mA

Commercial

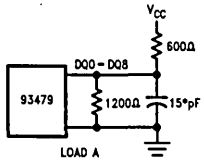
AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		25		25	ns
t_{ZRCS}	Chip Select to HIGH Z			25		25	ns
t_{AOS}	Output Enable Access Time			25		25	ns
t_{ZROS}	Output Enable to HIGH Z			25		25	ns
t_{AA}	Address Access Time (Note 8)			35		45	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	25		25		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		25		25		ns
t_{WHD}	Data Hold Time after Write		5		5		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		5		5		ns
t_{WHA}	Address Hold Time after Write		5		5		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		ns

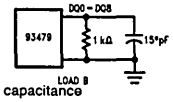
Military

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%. GND = 0V. T_C = −55°C to +125°C

Symbol	Parameter	Conditions	A		Std		Units
			Min	Max	Min	Max	
READ TIMING							
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b, 3d)*		30		40	ns
t_{ZRCS}	Chip Select to HIGH Z			30		40	ns
t_{AOS}	Output Enable Access Time			30		40	ns
t_{ZROS}	Output Enable to HIGH Z			30		40	ns
t_{AA}	Address Access Time (Note 8)			45		60	ns
WRITE TIMING							
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figure 4)*	40		40		ns
t_{SO}	Output Enable Setup Time		5		5		ns
t_{HO}	Data Enable Hold Time		5		5		ns
t_{WSD}	Data Setup Time Prior to Write		50		50		ns
t_{WHD}	Data Hold Time after Write		10		10		ns
t_{WSA}	Address Setup Time Prior to Write (Note 9)		10		10		ns
t_{WHA}	Address Hold Time after Write		10		10		ns
t_{WSCS}	Chip Select Setup Time Prior to Write		10		10		ns
t_{WHCS}	Chip Select Hold Time after Write		10		10		ns



TL/D/9675-5

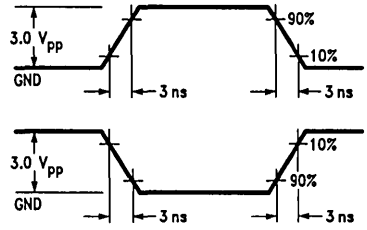


*Includes jig and probe capacitance

TL/D/9675-6

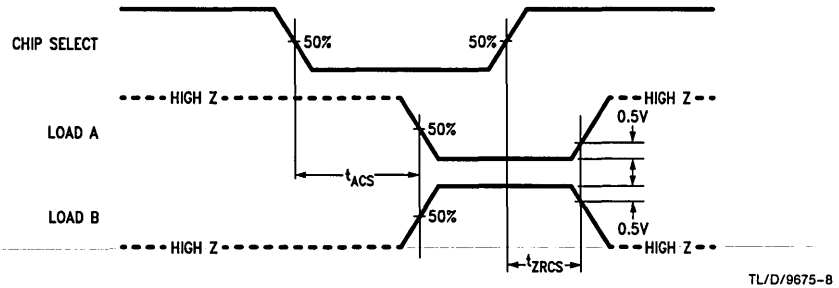
Note: Load A is used for all production testing.

FIGURE 1. AC Test Load Output Load



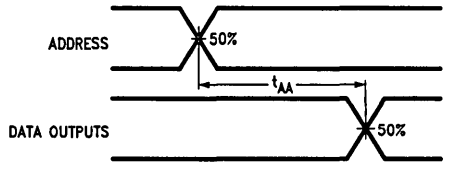
TL/D/9675-7

FIGURE 2. AC Test Input Levels



TL/D/9675-8

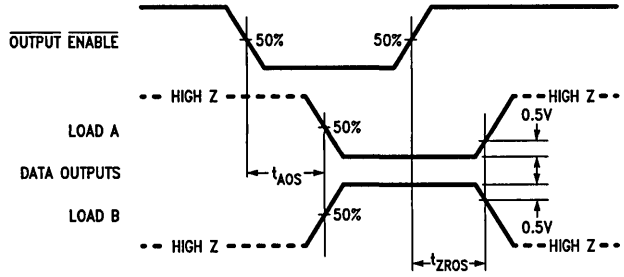
a. Read Mode Propagation Delay from Chip Select to Output



TL/D/9675-9

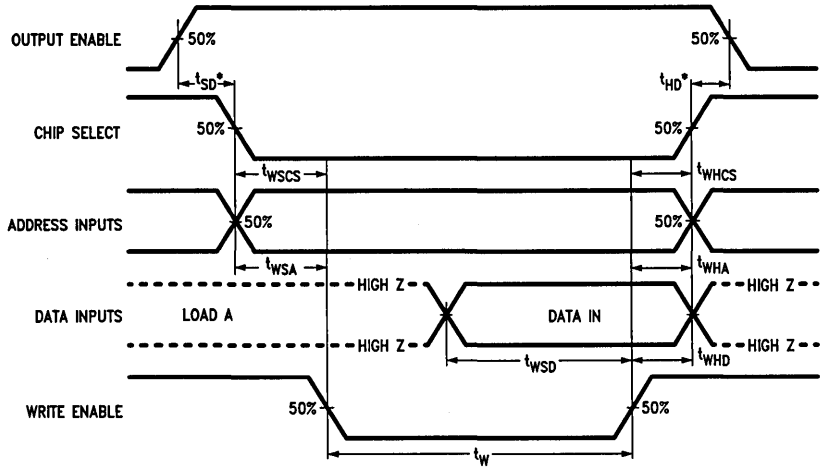
b. Read Mode Propagation Delay from Address to Output

FIGURE 3. Read Mode Timing



TL/D/9675–10

c. Read Mode Propagation Delay from Output Enable
FIGURE 3. Read Mode Timing (Continued)



TL/D/9675–11

*These timing parameters are only necessary to guarantee High Z state during the entire write cycle.

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0/0.0V.

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

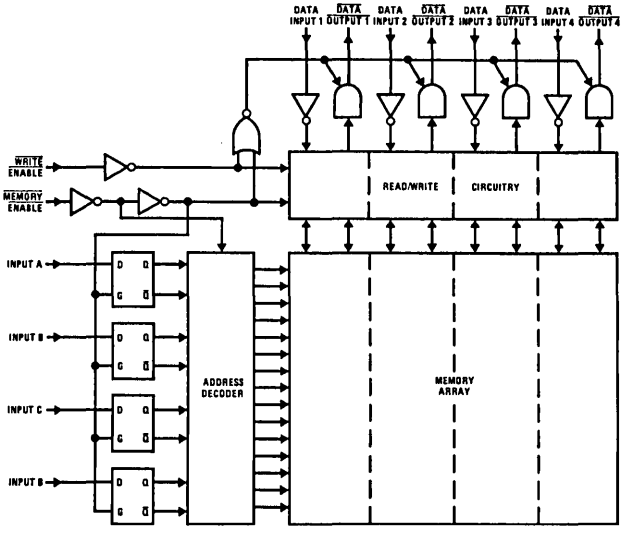
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

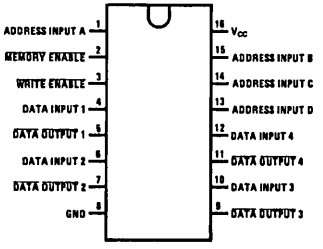
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100 nW/package (typ.)
■ Fast access time	130 ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5888–1

Dual-In-Line Package



Top View TL/F/5888–2

Order Number MM54C89* or MM74C89*

*Please look into Section 8, Appendix D for availability of various package types.

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C89	$-55°C$ to $+125°C$
MM74C89	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = +10\ \mu A$ $V_{CC} = 10V$, $I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		-0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC} = 15V$, $V = 15V$ $V_{CC} = 15V$, $V_O = 0V$	 -1.0	0.005 -0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = +360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = +360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from Memory Enable	$V_{CC} = 5V$ $V_{CC} = 10V$		270 100	500 220	ns ns
t_{ACC}	Access Time from Address Input	$V_{CC} = 5V$ $V_{CC} = 10V$		350 130	650 280	ns ns
t_{SA}	Address Setup Time	$V_{CC} = 5V$ $V_{CC} = 10V$	150 60			ns ns
t_{HA}	Address Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	60 40			ns ns
t_{ME}	Memory Enable Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$	400 150	250 90		ns ns

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SR}	Write Enable Setup Time for a Read	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0			ns ns
t_{WS}	Write Enable Setup Time for a Write	$V_{CC} = 5V$ $V_{CC} = 10V$			t_{ME} t_{ME}	ns ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5V$, $t_{WS} = 0$ $V_{CC} = 10V$, $t_{WS} = 0$	300 100	160 60		ns ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{SD}	Data Input Setup	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25			ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5V$, $C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$		180 −85	300 120	ns ns
t_{1H}, t_{0H}	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 50V$, $C_L = 5$ pF, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$		180 85	300 120	ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics* Guaranteed across the specified temperature range, $C_L = 50$ pF

Parameter	Conditions	MM54C89 $T_A = -55°C$ to $+125°C$		MM74C89 $T_A = -40°C$ to $+85°C$		Units
		Min	Max	Min	Max	
t_{PD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		700 310 250		600 265 210	ns ns ns
t_{ACC}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		910 400 320		780 345 270	ns ns ns
t_{SA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	210 90 70		180 80 60		ns ns ns
t_{HA}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	80 55 45		70 50 40		ns ns ns
t_{ME}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	560 210 170		480 180 150		ns ns ns
t_{WE}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	420 140 110		360 120 100		ns ns ns
t_{HD}	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$	70 35 30		60 30 25		ns ns ns

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics*

Guaranteed across the specified temperature range, C_L = 50 pF (Continued)

Parameter	Conditions	MM54C89 T_A = −55°C to +125°C		MM74C89 T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	
t_{SD}	V_{CC} = 5V	70		60		ns
	V_{CC} = 10V	35		30		ns
	V_{CC} = 15V	30		25		ns
t_{1H}, t_{0H}	V_{CC} = 5V		420		360	ns
	V_{CC} = 10V, C_L = 5 pF		170		145	ns
	V_{CC} = 15V, R_L = 10 kΩ		135		115	ns

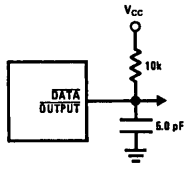
*AC Parameters are guaranteed by DC correlated testing.

Truth Table

ME	WE	Operation	Condition of Outputs
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

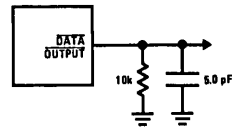
AC Test Circuits

t_{0H}



TL/F/5888–4

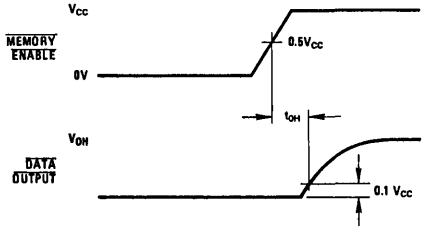
t_{1H}



TL/F/5888–3

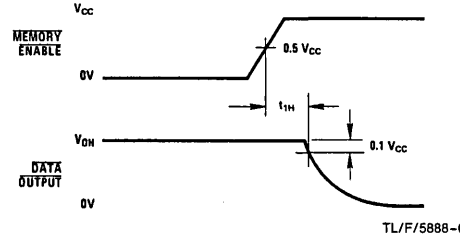
Switching Time Waveforms

t_{0H}



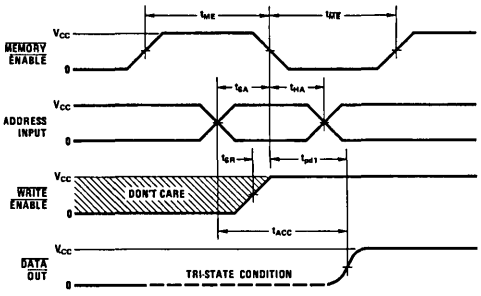
TL/F/5888–5

t_{1H}



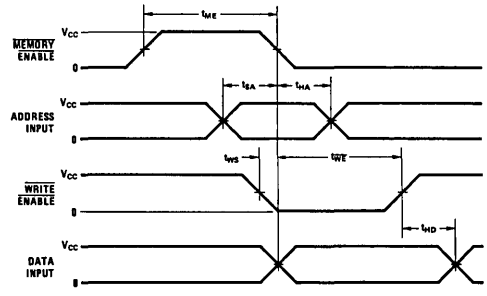
TL/F/5888–6

Read Cycle



TL/F/5888–7

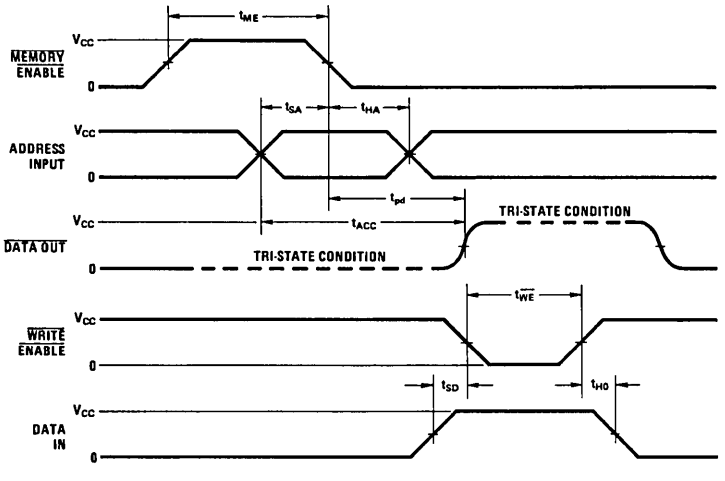
Write Cycle



TL/F/5888–8

Switching Time Waveforms (Continued)

Read Modify Write Cycle



TL/F/5888–9

Note: t_r = 60 ns
t_f = 10 ns

6

National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

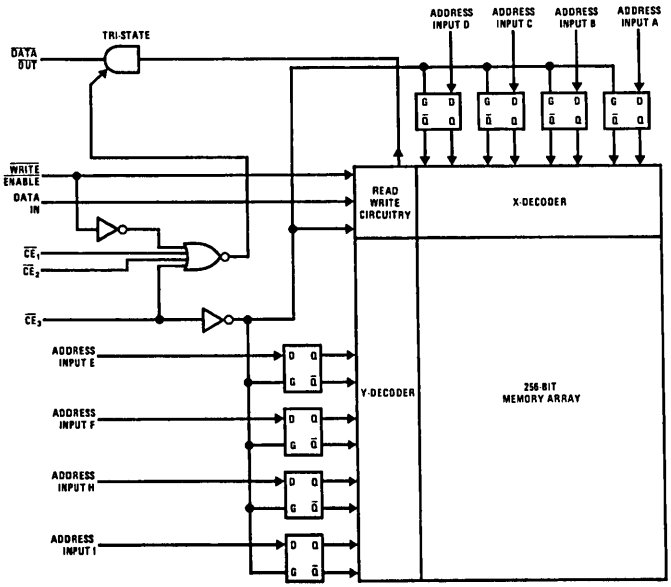
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

Features

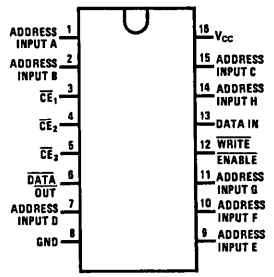
■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

Logic and Connection Diagrams



TL/F/5903–1

Dual-In-Line Package



TL/F/5903–2

Top View

Order Number MM54C200* or MM74C200*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range (T_A)	
MM54C200	$-55°C$ to $+125°C$
MM74C200	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC}=5V, I_O=-10 μA V_{CC}=10V, I_O=-10 μA	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC}=5V, I_O=+10 μA V_{CC}=10V, I_O=+10 μA			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC}=15V, V_{IN}=15V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC}=15V, V_{IN}=0V	-1	-0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.1	600	μA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC}=4.5V, I_O=-1.6 mA 74C V_{CC}=4.75V, I_O=-1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O=1.6 mA 74C V_{CC} = 4.75V, I_O=1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC}=5V, V_{OUT}=0V T_A=25°C	-4 -1.8	-6		mA mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC}=10V, V_{OUT}=0V T_A=25°C	-16 -1.5	-25		mA mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC}=5V, V_{OUT}=V_{CC} T_A=25°C	5	8		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC}=10V, V_{OUT}=V_{CC} T_A=25°C	20	30		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ACC}	Access Time from Address	$V_{CC} = 5V$ $V_{CC} = 10V$		450 200	900 400	ns ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5V$ $V_{CC} = 10V$		360 120	700 300	ns ns
t_{pCE1}	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5V$ $V_{CC} = 10V$		250 85	700 200	ns ns
t_{SA}	Address Setup Time	$V_{CC} = 5V$ $V_{CC} = 10V$	200 100	80 30		ns ns
t_{HA}	Address Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25	15 5.0		ns ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$	300 150	160 70		ns ns
t_{CE}	$\overline{CE}_3$ Pulse Widths	$V_{CC} = 5V$ $V_{CC} = 10V$	400 160	200 80		ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

AC Electrical Characteristics* $C_L = 50$ pF

Symbol	Parameter	Conditions	MM54C200 $T_A = -55°C$ to $+125°C$		MM74C200 $T_A = -40°C$ to $+85°C$		Units
			Min	Max	Min	Max	
t_{ACC}	Access Time from Address	$V_{CC} = 5V$ $V_{CC} = 10V$		1200 520		1100 480	ns ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5V$ $V_{CC} = 10V$		950 400		850 360	ns ns
$t_{pd\overline{CE1}}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5V$ $V_{CC} = 10V$		650 300		600 275	ns ns
t_{SA}	Address Setup Time	$V_{CC} = 5V$ $V_{CC} = 10V$	250 120		250 120		ns ns
t_{HA}	Address Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	100 50		100 50		ns ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$	450 225		400 200		ns ns
t_{CE}	Disable Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$	500 250		460 230		ns ns
t_{HD}	Data Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 25		50 25		ns ns

*AC Parameters are guaranteed by DC correlated testing.

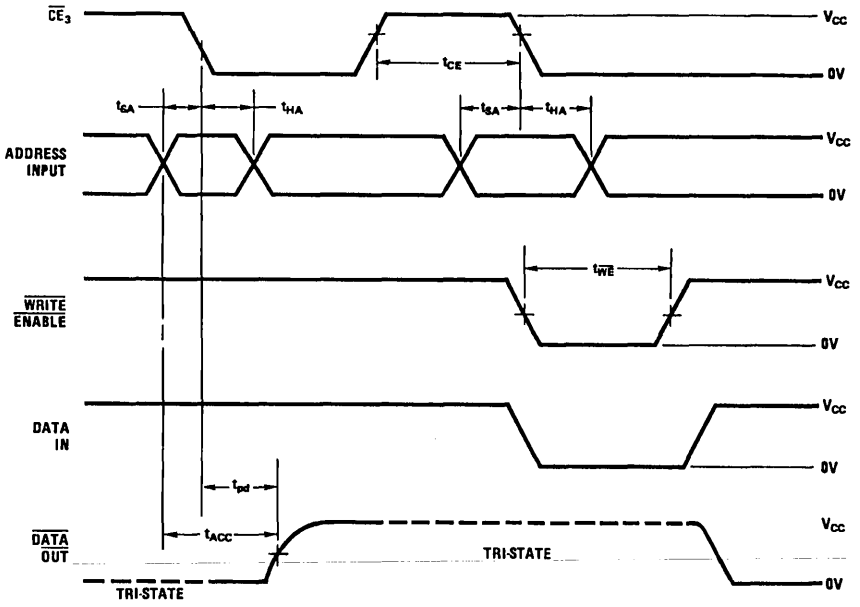
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

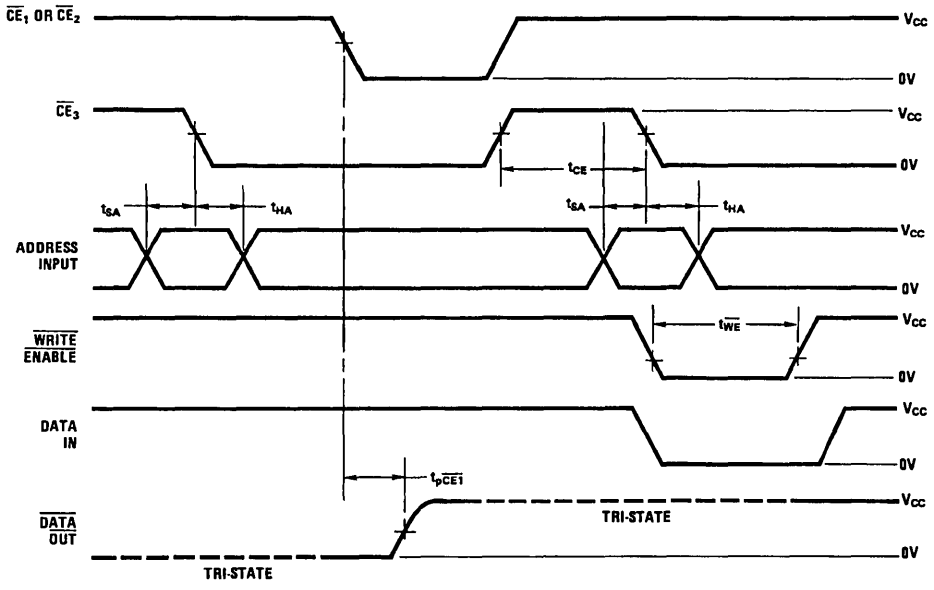
Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



TL/F/5903–3

Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



TL/F/5903–4

Note: Used for fast access time in bused systems.

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4-bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of the 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

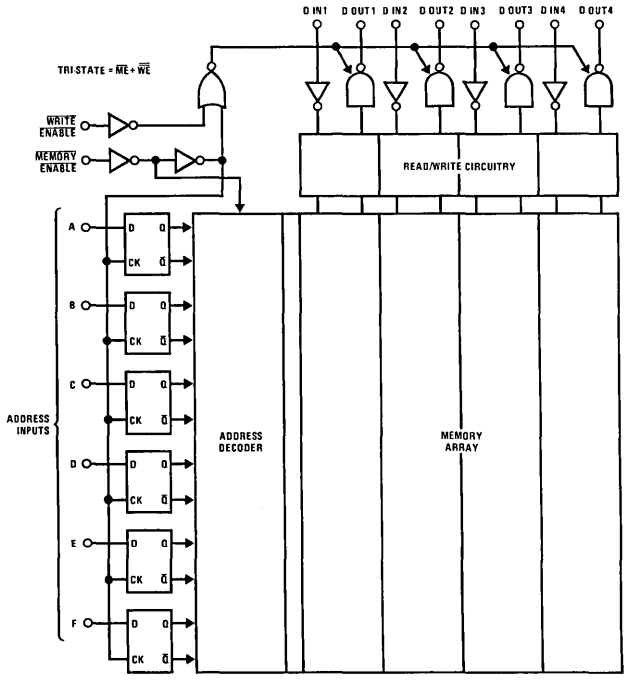
Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

Features

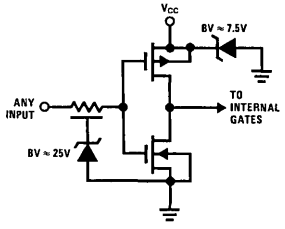
- Supply voltage range — 3.0V to 5.5V
- High noise immunity — 0.45V_{CC} (typ.)
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package (typ.) (chip enabled or disabled)
- Fast access time — 250 ns (typ.) at 5.0V
- TRI-STATE outputs
- High voltage inputs

Logic Diagrams



TL/F/5914–1

Input Protection



TL/F/5914–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Output Pin	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Input Pin	$-0.3V$ to $+15V$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum (V_{CC})	6.0V
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

DC Electrical Characteristics

Min/Max limits apply accross the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 15V$ $V_{IN} = 5V$		0.005 0.005	2.0 1.0	μA μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−1.0	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -150\ \mu A$ $I_O = -400\ \mu A$	$V_{CC} - 0.5$ 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.4	V
I_{OZ}	Output Current in High Impedance State	$V_O = 5V$ $V_O = 0V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 5V$		5.0	300	μA

AC Electrical Characteristics* $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF

Symbol	Parameter	Min	Typ	Max	Units
t_{ACC}	Access Time from Address		250	500	ns
t_{pd}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

AC Electrical Characteristics* (Continued) $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 50$ pF

Symbol	Parameter	MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75V$ to $5.25V$		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

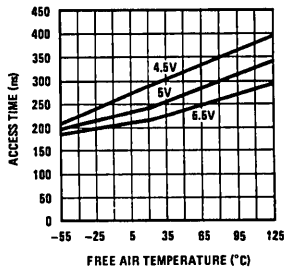
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: See AC test circuits for t_{1H}, t_{0H}.

Typical Performance Characteristics

Typical Access Time vs Ambient Temperature

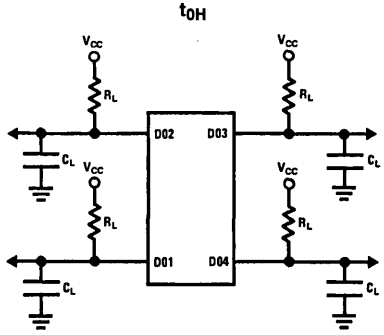


TL/F/5914–4

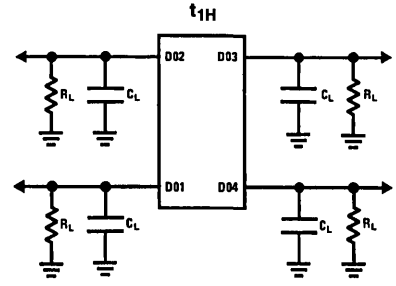
Truth Table

$\overline{ME}$	$\overline{WE}$	Operation	Outputs
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

AC Test Circuits



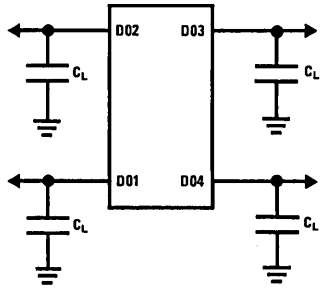
TL/F/5914–5



TL/F/5914–6

AC Test Circuits (Continued)

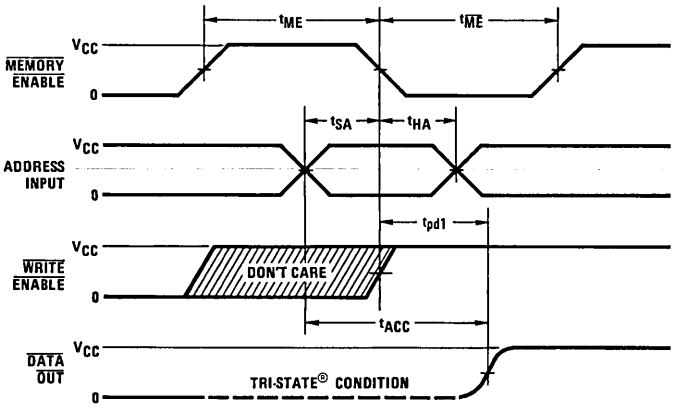
All Other AC Tests



TL/F/5914–7

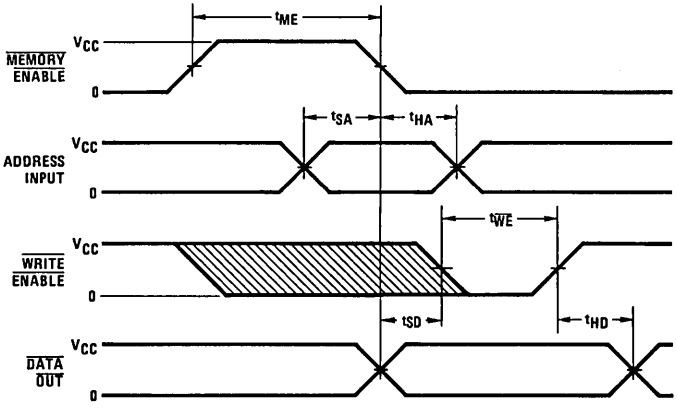
Switching Time Waveforms

Read Cycle
(See Note 1)



TL/F/5914–8

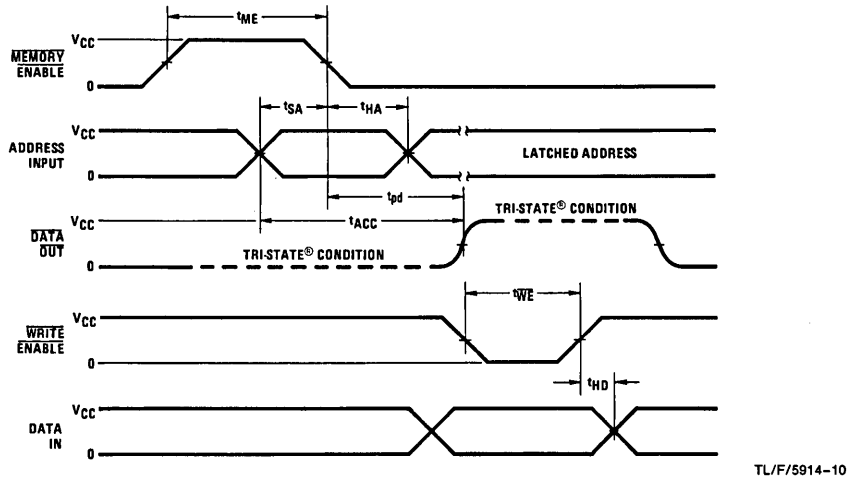
Write Cycle
(See Note 1)



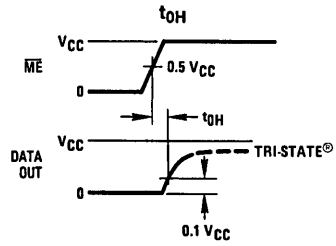
TL/F/5914–9

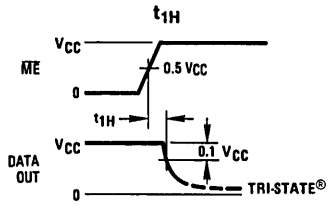
Switching Time Waveforms (Continued)

Read Modify Write Cycle
(See Note 1)



TL/F/5914–10





TL/F/5914–12

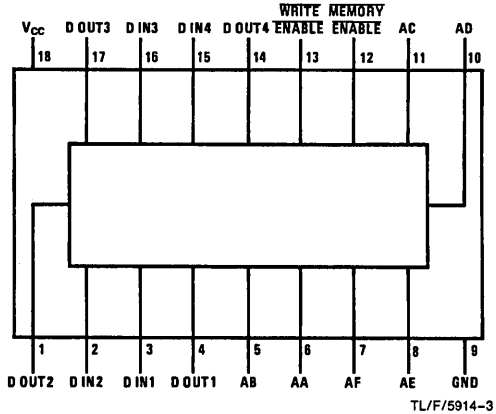
TL/F/5914–11

Note 1: MEMORY ENABLE must be brought high for t_{ME} nanoseconds between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

Connection Diagram

Dual-In-Line Package



TL/F/5914–3

Top View

Order Number MM54C910* or MM74C910*

*Please look into Section 8, Appendix D
for availability of various package types.

National Semiconductor

MM54C989/MM74C989
64-Bit (16 x 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines. a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

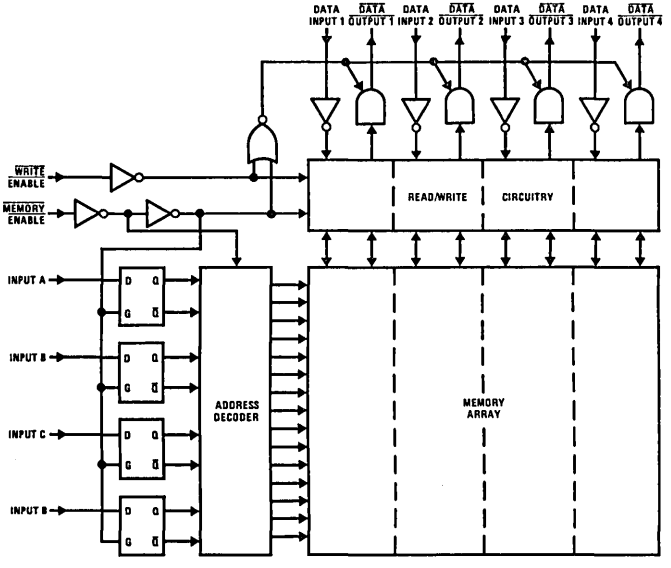
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

Features

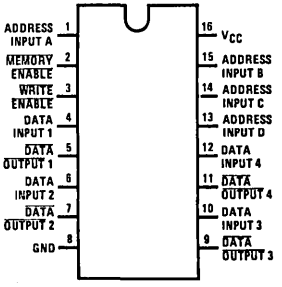
◘ Wide supply voltage range	3.0V to 5.5V
◘ Guaranteed noise margin	1.0V
◘ High noise immunity	0.45 V_{CC} (typ.)
◘ Low power TTL compatibility	Fan out of 2 driving 74L
◘ Input address register	
◘ Low power consumption	250 nW/package (typ.) @ V_{CC} = 5V
◘ Fast access time	140 ns (typ.) at V_{CC} = 5V
◘ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5925–1

Dual-In-Line Package



TL/F/5925–2

Top View

Order Number
MM54C989* or MM74C989*

*Please look into Section 8, Appendix D
*for availability of various package types.

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range		3.0V/3V	
Standby V_{CC} Range		1.5V/3V	

DC Electrical Characteristics MM54C989/MM74C989

Min/Max limits apply across the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$ $I_O = -150\ \mu A$	2.4 $V_{CC} - 0.5$			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 360\ \mu A$			0.4	V
I_{OZ}	Output Current in High Impedance State	$V_O = 5V$ $V_O = 0V$	 −1	0.005 −0.005	1	μA μA
I_{CC}	Supply Current Active (Note 1)*	$\overline{ME} = 0V$, $V_{CC} = 5V$		0.05	150	μA
I_{CC}	Supply Current (Stand-By)	$\overline{ME} = 5V$			3	μA

Note 1*: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

AC Electrical Characteristics* MM54C989/MM74C989

$T_A = 25°C$, $V_{CC} = 5V$, $C_L = 50$ pF

Symbol	Parameter	Min	Typ	Max	Units
t_{ACC}	Access Time from Address		140	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, $C_L = 5$ pF, $R_L = 10$k, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

AC Electrical Characteristics* (Continued)

MM54C989: $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF
MM74C989: $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.75V$ to $5.5V$, $C_L = 50$ pF

Symbol	Parameter	MM54C989		MM74C989		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, (Note 4)		200		200	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

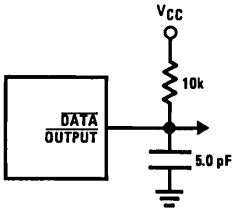
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

$\overline{ME}$	$\overline{WE}$	Operation	Condition of Outputs
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

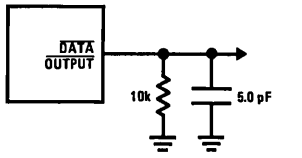
AC Test Circuits

t_{0H}



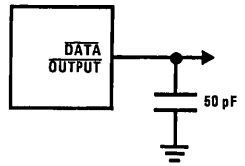
TL/F/5925–3

t_{1H}



TL/F/5925–4

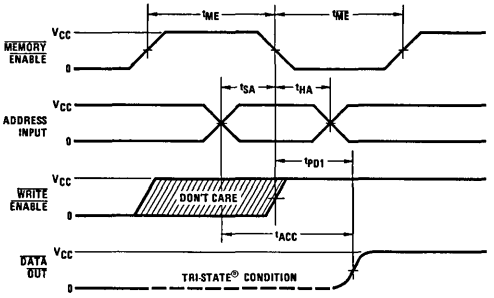
All Other AC Tests



TL/F/5925–5

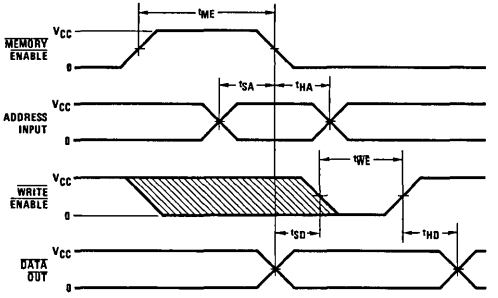
Switching Time Waveforms

Read Cycle (Note 1)*



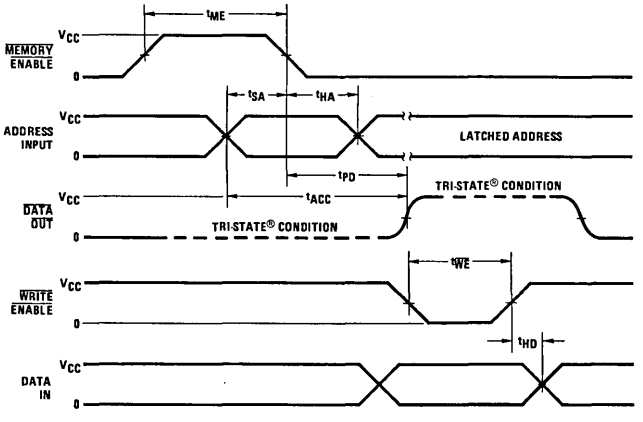
TL/F/5925–6

Write Cycle (Note 1)*



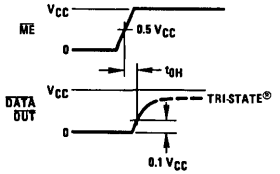
TL/F/5925–7

Read-Modify-Write Cycle (Note 1)*



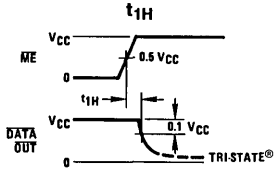
TL/F/5925–8

t_{0H}



TL/F/5925–9

t_{1H}



TL/F/5925–10

Note 1*: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

NMC2147H 4096 x 1-Bit Static RAM

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

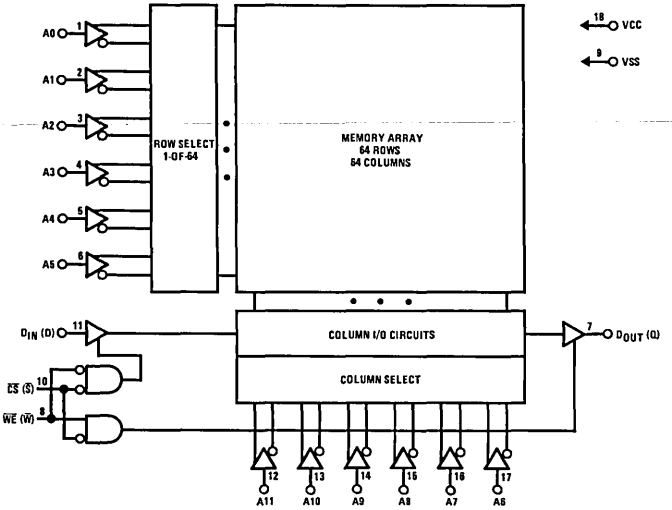
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

Features

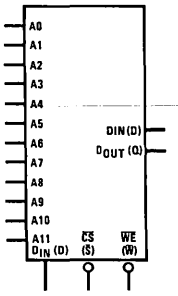
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*



TL/D/5257-1

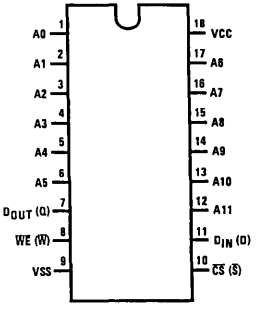
Logic Symbol*



TL/D/5257-2

Connection Diagram*

Dual-In-Line Package



TL/D/5257-3

Top View

Pin Names*

A0–A11	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
D_{IN} (D)	Data In
D_{OUT} (Q)	Data Out
V_{CC}	Power (5V)
V_{SS}	Ground

Order Number NMC2147HJ-1, NMC2147HJ-2, NMC2147HJ-3, or NMC2147HJ-3L
See NS Package Number J18A

*The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−65°C to +135°C
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table*

$\overline{CS}$ (S)	$\overline{WE}$ ($\overline{W}$)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50		50	μA
VIL	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180		160	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30		20	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Level (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See *Figure 1*

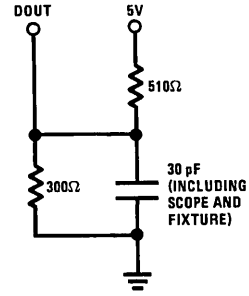


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FIGURE 1. Output Load

*Symbols in parentheses are proposed industry standard.

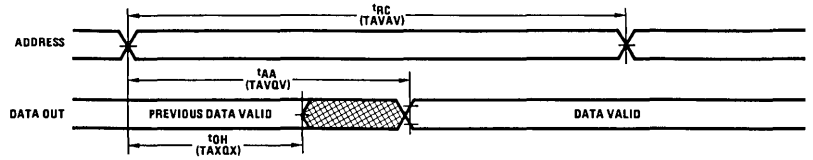
Read Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV—ns)	35	45	55	55	70
Active Current (ICC—mA)	180	180	180	125	160
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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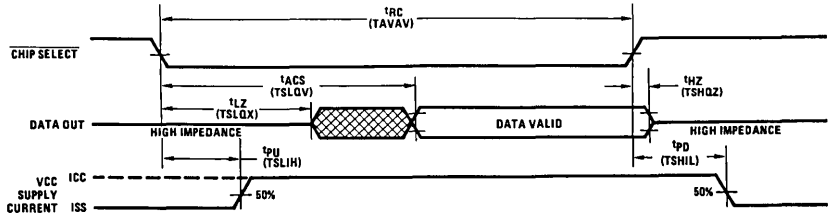
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

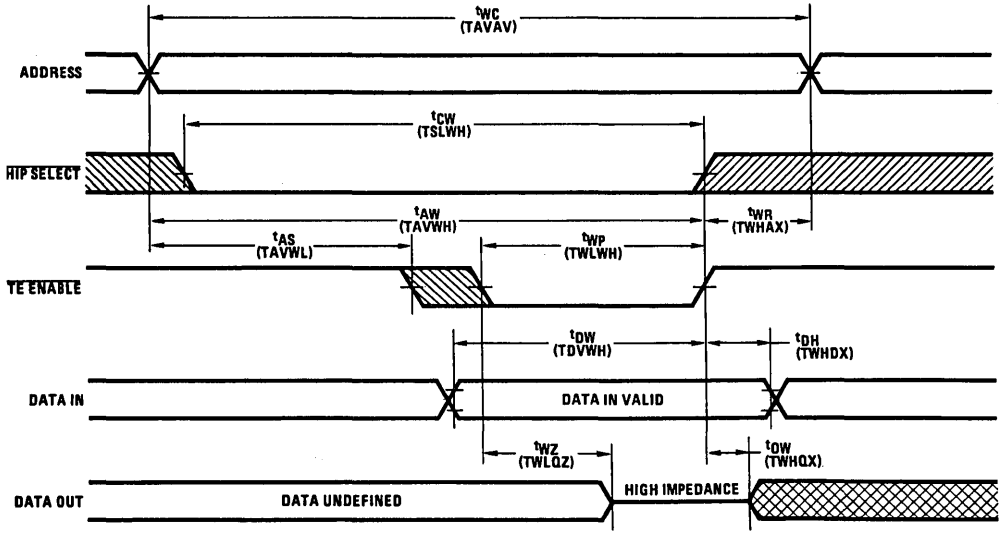
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t_{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

Write Cycle Waveforms* (Note 6)

Write Cycle 1 (Write Enable Limited)



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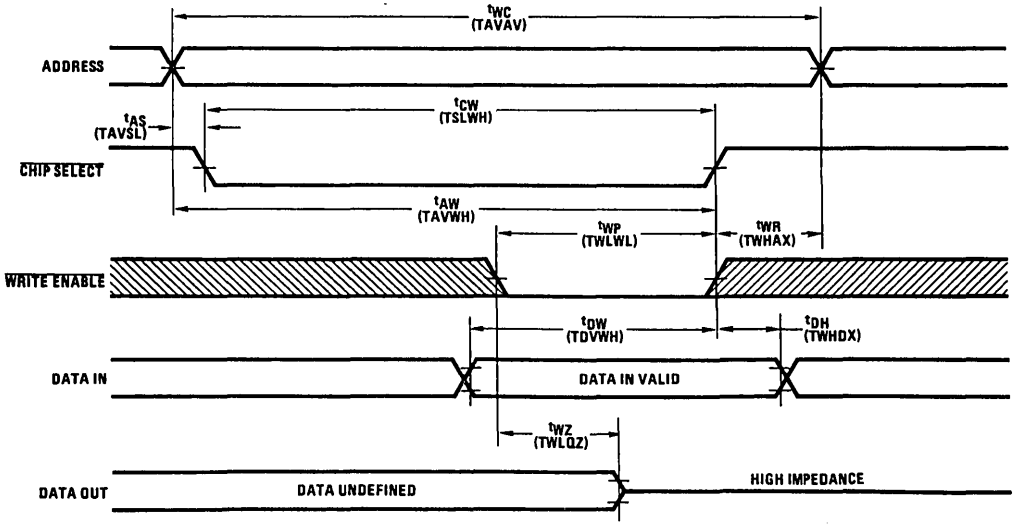
Write Cycle Waveforms* (Note 6)

Write Cycle 2 (Chip Select Limited)



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Note 6: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*The symbols in parentheses are proposed industry standard.

National Semiconductor

NMC2148H 1024 x 4-Bit Static RAM

General Description

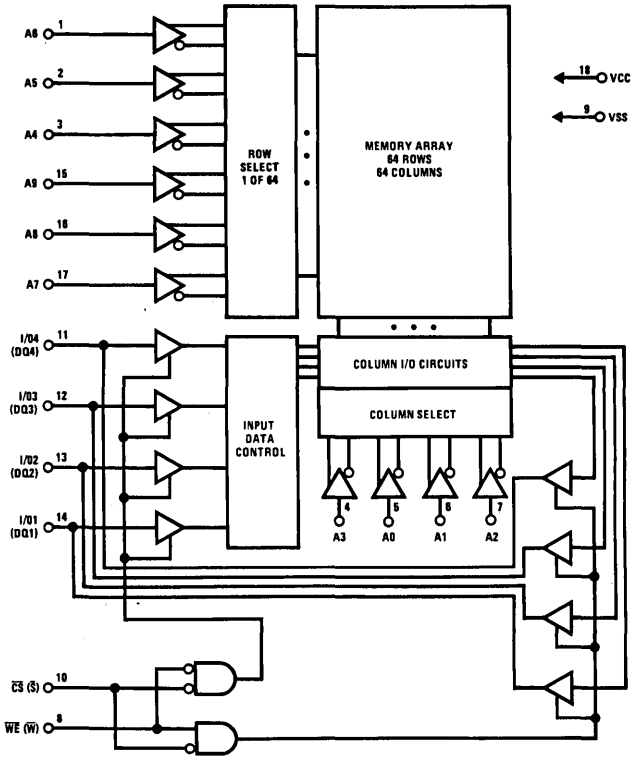
The NMC2148H is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

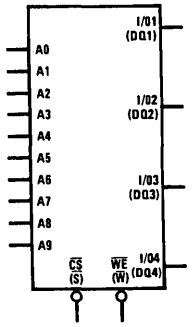
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 45 ns access time
- TRI-STATE® output for bus interface
- Common data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Block Diagram*



TL/D/7404-1

Logic Symbol*



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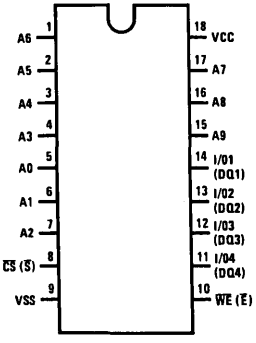
Connection Diagram*

Dual-In-Line Package



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Top View

Pin Names*

A0–A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
1/01–1/04 (DQ1–DQ4)	Data Input/Output
VCC	Power (5V)
VSS	Ground

*Symbols in parentheses are proposed industry standard.

Order Number NMC2148HJ-L, NMC2148HJ-3L, NMC2148HJ, NMC2148HJ-2 or NMC2148HJ-3
See NS Package Number J18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin with Respect to VSS	−3.5V to +7V
Storate Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	Mode	Power
H	X	Hi-Z	Standby	Standby
L	L	H	Write 1	Active
L	L	L	Write 0	Active
L	H	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2148H-L NMC2148H-3L		NMC2148H NMC2148H-2 NMC2148H-3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50	μA
VIL	Input Low Voltage		−2.5	0.8	−2.5	0.8	V
VIH	Input High Voltage		2.1	6.0	2.1	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40	mA
|IOS|	Output Short Circuit Current	VOUT = GND to VCC		250		250	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
CI/O	Input/Output Capacitance	VI/O = 0V		7	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8V and 2.0V
Output Load	See *Figure 1*

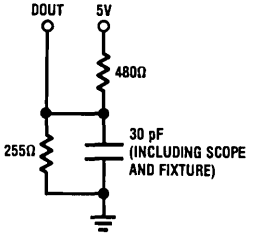

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FIGURE 1. Output Load

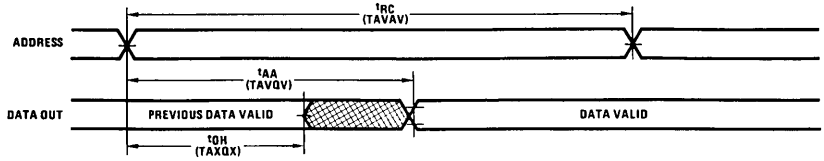
Read Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	45		55		70		ns
t_{AA}	TAVQV	Address Access Time		45		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Notes 4 and 5)		45		55		70	ns
t_{ACS2}	TLSQV2	Chip Select Access Time (Notes 4 and 6)		55		65		80	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 7)	20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 7)	0	20	0	20	0	20	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		30		30		30	ns

Max Access/Current	NMC2148H-2	NMC2148H-3	NMC2148H	NMC2148H-3L	NMC2148H-L
Access (TAVQV—ns)	45	55	70	55	70
Active Current (ICC—mA)	180	180	180	125	125
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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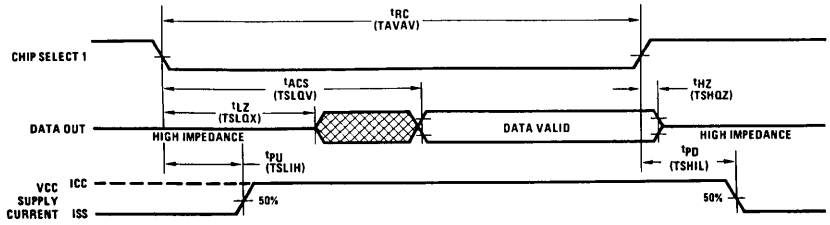
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Chip deselected longer than 55 ns.

Note 6: Chip deselected less than 55 ns.

Note 7: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

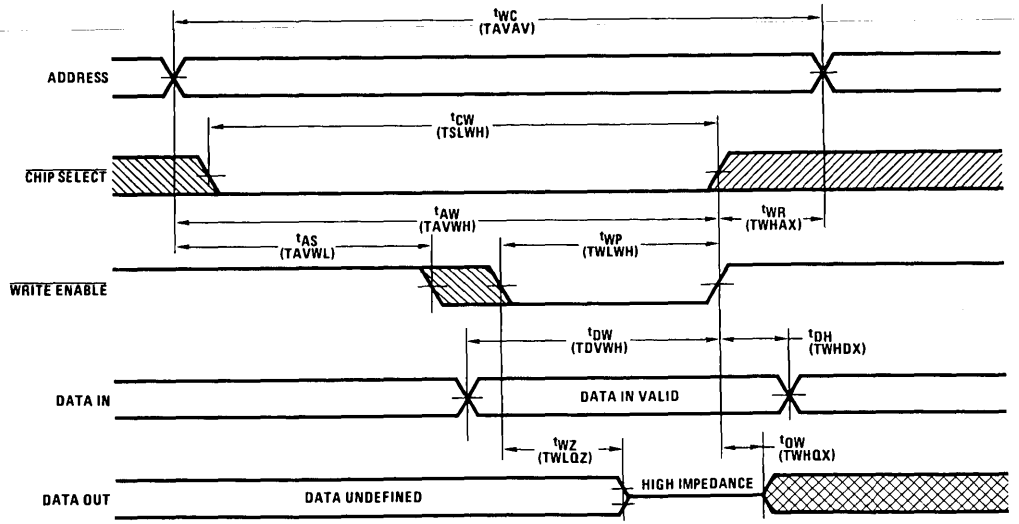
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	40		50		65		ns
t_{AW}	TAVWH	Address Valid to End of Write	40		50		65		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	35		40		50		ns
t_{WR}	TWHAX	Write Recovery Time	5		5		5		ns
t_{DW}	TDVWH	Data Set-Up Time	20		20		25		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 7)	0	15	0	20	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 7)	0		0		0		ns

Write Cycle Waveforms* (Note 8)

Write Cycle 1 (Write Enable Limited)



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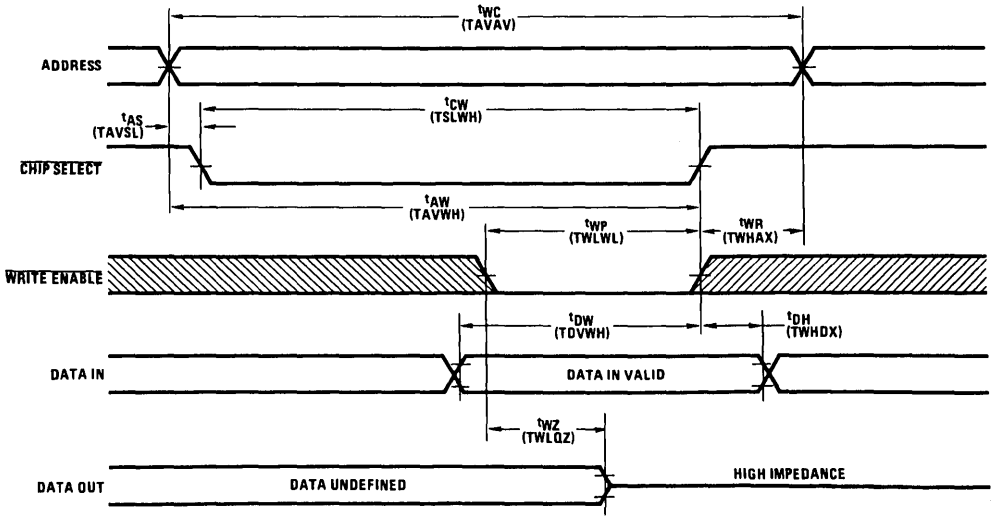
Write Cycle Waveforms* (Note 8) (Continued)

Write Cycle 2 (Chip Select Limited)



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Note 8: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simulataneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*Symbols in parentheses are proposed industry standard.

National Semiconductor

NM1600/NM1601
65,536 x 1-Bit Static RAM

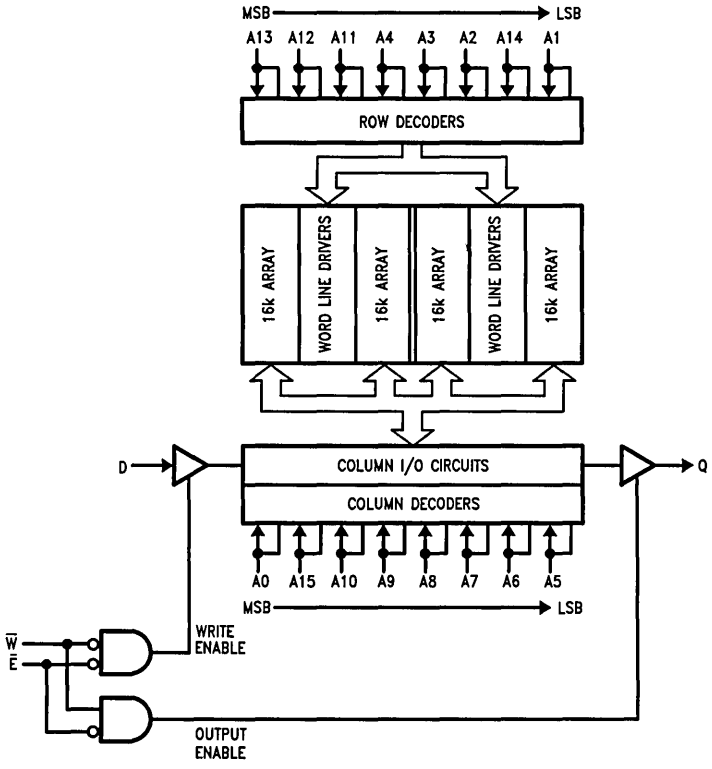
General Description

The NM1600/NM1601 is a 65,536-bit fully-static, asynchronous, random access memory organized as 65,536 words by 1-bit per word. The NM1600/NM1601 is based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology, with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device. The NM1601 is identical to the NM1600 with the additional feature of power down for low power battery backup.

Features

- Fast address access times: 25 ns/30 ns/35 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Separate data input and TRI-STATE® output
- Available in 22-pin DIP, PDIP or LCC
- Low power dissipation (data retention NM1601) I_{CCDR} = 50 μA Max. (2.0V ≤ V_{DR} ≤ 3.0V)
- Data retention supply voltage NM1601: 2.0V to 5.5V

Functional Block Diagram



TL/D/9676–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2V$ to $V_{CC} + 2V$
Storage Temperaure	$-65°C$ to $+150°C$
Operating Temperature	$0°C$ to $+70°C$
Power Dissipation	1.0W
Continuous Output Current	25 mA
Average Input or Output Current (Averaged over any 1 μs time interval)	25 mA

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions $T_A = 0°C$ to $+70°C$

	Min	Max	Units
Input HIGH Voltage (V_{IH})	2.2	$V_{CC} + 0.5$	V
Input LOW Voltage (V_{IL})	-1*	0.8	V

All voltages are referenced to V_{SS} pin = 0V.

*The device will withstand undershoots to $-3V$ of 20 ns duration.

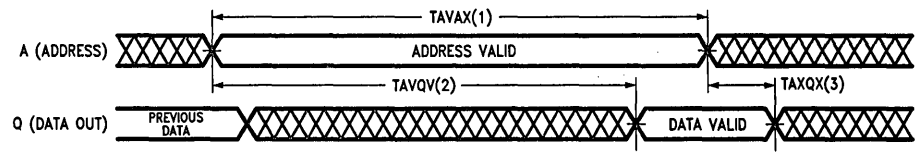
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN}

No.	Symbol		Parameter	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
READ CYCLES										
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	25		30		35		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		25		30		35	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	22		27		30		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		22		27		30	ns
6	TELQX	TLZ	Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Note 9)	0	10	0	12	0	15	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		25		27		30	ns

Timing Waveforms

Read Cycle 1



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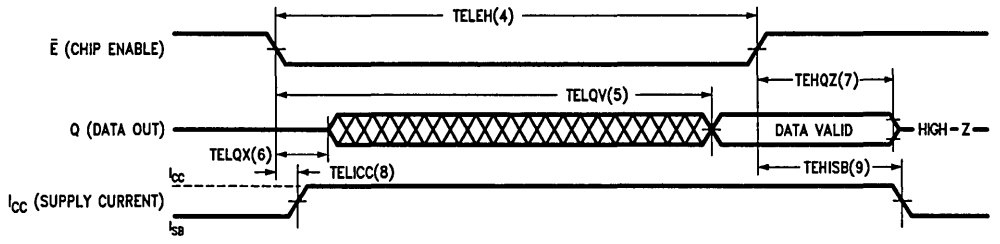
Access is under address control where $\overline{E}$ is active prior to or within 5 ns of address change. $\overline{W}$ = HIGH.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol		Parameter	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1										
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	25		30		35		ns
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write (Notes 7 & 12)	0		0		0		ns
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		ns
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Note 9)	0	9	0	12	0	12	ns
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		ns

Timing Waveforms (Continued)

Read Cycle 2



TL/D/9676-8

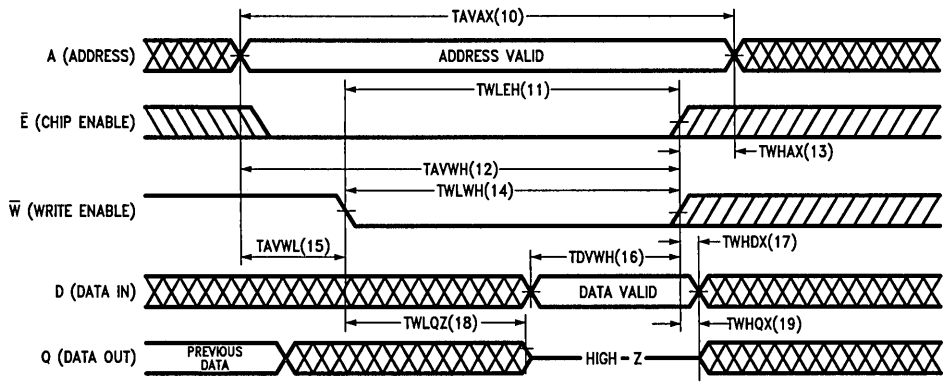
Where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active (LOW). $\overline{W}$ = HIGH.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol		Parameter	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2										
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		ns
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		ns

Timing Waveforms (Continued)

Write Cycle 1



TL/D/9676–9

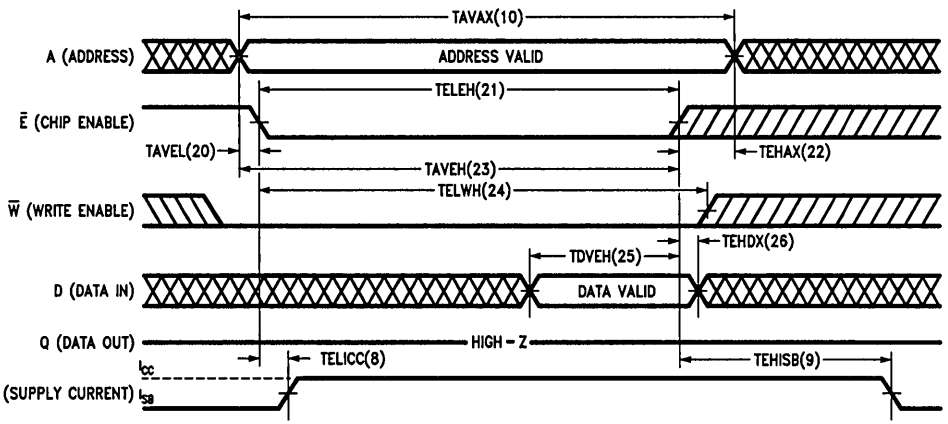
This write cycle is $\overline{W}$ controlled, where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out may become active, requiring observance of TWLQZ to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$

Symbol	Parameter		Conditions	NM1600-25/255 NM1601-25/255		NM1600-30 NM1601-30		NM1600-35 NM1601-35		Units
				Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current		$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2	μA
I_{LO}	Output Leakage Current		$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current		Min Read Cycle Time Duty Cycle = 100% Output Open		90		90		80	mA
I_{SB1}	Standby Supply Current		$\overline{E} = V_{IH}$, (Note 1)		25		25		25	mA
I_{SB2}	Full Standby Supply Current	NM1600	(Note 2)		15		15		15	mA
		NM1601	(Note 2)		5		5		5	
V_{OL}	Output LOW Voltage		$I_{OL} = 8.0$ mA		0.4		0.4		0.4	V
V_{OH1}	Output HIGH Voltage		$I_{OH1} = -4.0$ mA	2.4		2.4		2.4		V
V_{OH2}	Output HIGH Voltage		$I_{OH2} = -0.05$ mA	$V_{CC} - 0.4$		$V_{CC} - 0.4$		$V_{CC} - 0.4$		V
V_{CC}	Supply Voltage		Except Data Retention Mode	-25		4.5	5.5	4.5	5.5	V
				4.5	5.5					
				-255						
				4.75	5.5					

Timing Waveforms (Continued)

Write Cycle 2



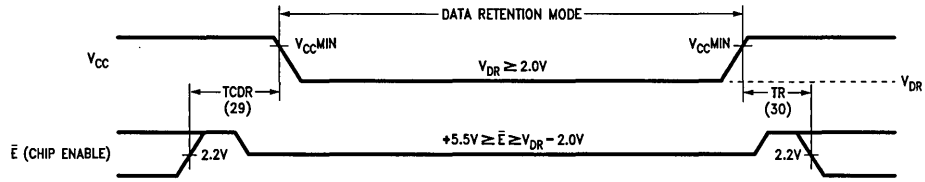
TL/D/9676–10

This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (TRI-STATE) at the beginning of the write cycle, precluding potential data contention in common I/O applications.

Data Retention Characteristics (NM1601 only) $T_A = 0°C$ to $+70°C$, $V_{CC} = 2.0V$ to $5.5V$

No.	Symbol	Parameter	Conditions	Min	Max	Units
27	V_{DR}	V_{CC} Voltage for Data Retention	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$	2.0	5.5	V
28	I_{CCDR}	Data Retention Current (Note 14)	$V_{DR} = 3.0V$, $T_A = 0°C$ to $+70°C$		50	µA
			$V_{DR} = 2.0V$, $T_A = 0°C$ to $+70°C$		35	µA
29	TCDR	Chip Disable to Data Retention Time (Note 4)		0		ns
30	TR	Recovery Time (Notes 4 & 13)		t_{AVAX}		ns

Data Retention Waveform



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Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \le \overline{E} \le V_{CC} + 0.2V$, and all other inputs, (including the data inputs) at steady state and satisfying one of two conditions: Either, $V_{CC} - 0.2V \le V_{IN} \le V_{CC} + 0.2V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operation voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active). Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ± 500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2*. This parameter is sampled, not 100% tested.

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outisde specified switching levels of transition times.

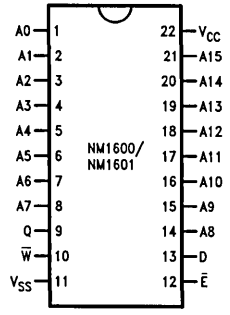
Note 12: Timing specifications of Data Setup to End of Write, Data Hold After End of Write, and Address Hold After End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ or $5.5V$.

Connection Diagrams

22-Pin DIP (J) and PDIP (N)



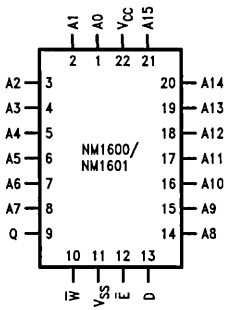
TL/D/9676–1

Top View

Order Number*
NM1600J25, NM1600J255, NM1600J30, NM1600J35, NM1600N25, NM1600N255, NM1600N30, NM1600N35, NM1601J25, NM1601J255, NM1601J30, NM1601J35, NM1601N25, NM1601N255, NM1601N30 or NM1601N35
See NS Package Number D22D* or N22B*

*Call factory for package outlines and dimensions.

22-Pin LCC (E)



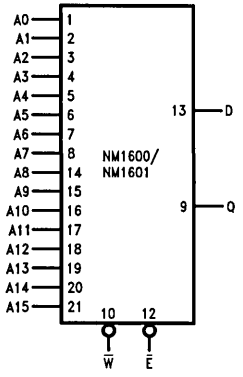
TL/D/9676–2

Top View

Order Number*
NM1600E25, NM1600E255, NM1600E30, NM1600E35, NM1601E25, NM1601E255, NM1601E30 or NM1601E35
See NS Package Number E22A*

*Call factory for package outlines and dimensions.

Logic Symbol



TL/D/9676–3

Pin Names

A_0–A_{15}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0V)
V_{SS}	Ground (0V)

6

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Reference Levels	1.5V
Output Load	(See *Figures 1* and *2*)

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$.

Truth Table

Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care

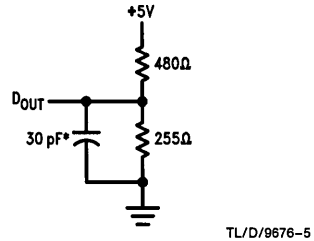


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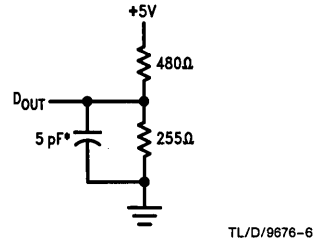
FIGURE 1. Output Load



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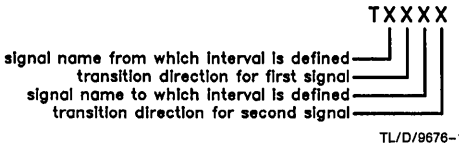
*including scope and jig.

FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)

STANDARD TIMING PARAMETER ABBREVIATIONS



TL/D/9676–11

The transition definitions used in this data sheet are:

H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

TL/D/9676–12

INVALID or Don't Care.

TL/D/9676–13

Transition from HIGH to LOW level, may occur any time during this period.

TL/D/9676–14

Transition from LOW to HIGH level, may occur any time during this period.

National Semiconductor

1600A/1601A 65,536 x 1-Bit Static RAM Military Temperature Range

General Description

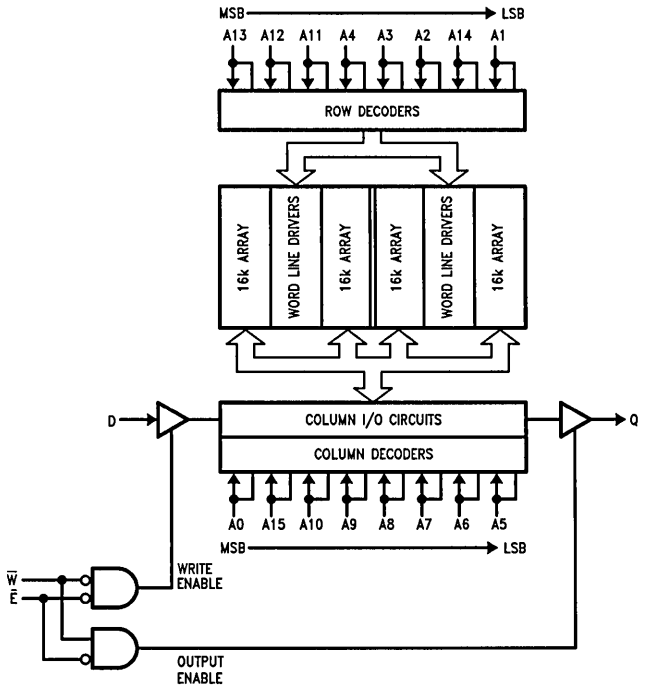
The 1600A/1601A is a 65,536-bit fully-static, asynchronous, random access memory organized as 65,536 words by 1-bit per word. The 1600A/1601A is based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device.

The 1601A is identical to the 1600A with the additional feature of power down for low power battery backup applications. Both parts are processed in full compliance with MIL-STD-883.

Features

- Fast address access times: 30 ns/35 ns/45 ns/55 ns/70 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Separate data input and TRI-STATE® output
- Available in 22-pin DIP or LCC
- Single +5V Operation (±10%)
- Low power dissipation (data retention 1601A): I_{CCDR} = 5 μA Max. (V_{DR} = 2.0V), I_{CCDR} = 8 μA Max. (V_{DR} = 3.0V) @ 25°C
- Data retention supply voltage 1601A: 2.0V to 5.5V
- Polyamide die coat for alpha immunity

Functional Block Diagram



TL/D/9677–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2.0V$ to $V_{CC}+2V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$-55°C$ to $+125°C$
Power Dissipation	1.0W
Continuous Output Current	25 mA
Average Input or Output Current (Averaged over any 1 μs time interval.)	25 mA
Thermal Resistance	
θ Side-Brazed DIP	15°C/W
θ JC LCC	20°C/W

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions $T_C = -55°C$ to $+125°C$

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Input HIGH Voltage (V_{IH})	2.2		$V_{CC}+0.5$	V
Input LOW Voltage (V_{IL})	-1*		0.8	V

All Voltages are referenced to V_{SS} pin = 0V.

*The device will meet $-1V$ or -50 mA whichever occurs first without latching up. The device will also withstand undershoots to $-3V$ of 20 ns duration.

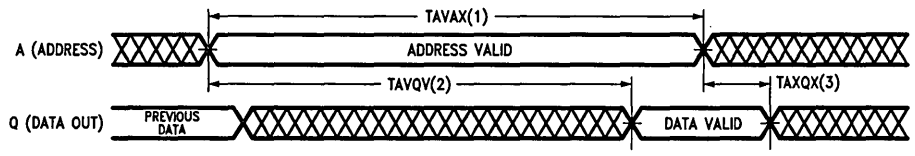
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	1600A-30 1601A-30		1600A-35 1601A-35		1600A-45 1601A-45		1600A-55 1601A-55		1600A-70 1601A-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
READ CYCLES														
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	30		35		45		55		70		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		30		35		45		55		70	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	27		30		40		50		50		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		27		30		40		50		50	ns
6	TELQX	TLZ	Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Notes 4 & 9)	0	12	0	15	0	15	0	20	0	20	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		27		30		40		50		50	ns

Timing Waveforms

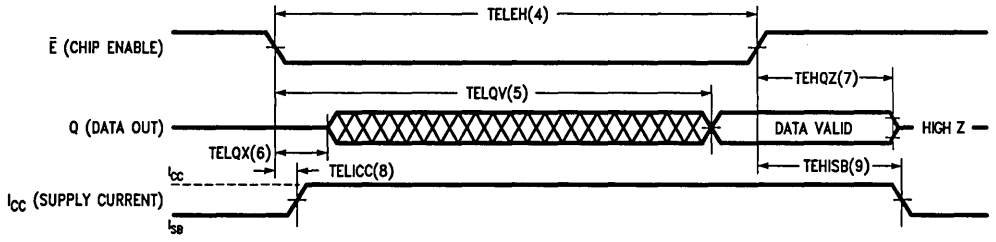
Read Cycle 1



TL/D/9677-7

Access is under address control where $\overline{E}$ is active prior to or within 5 ns of address change. $\overline{W} = V_{IH}$.

Read Cycle 2



TL/D/9677-8

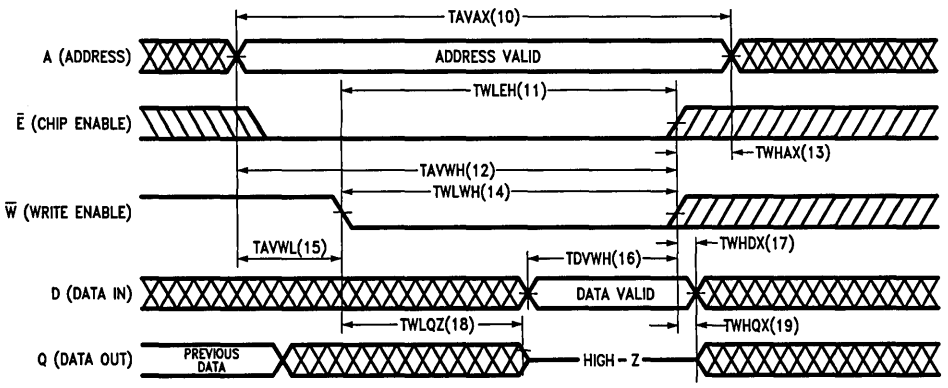
Access is under $\overline{E}$ control where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active. $\overline{W} = V_{IH}$, address remains valid at least TELQV after $\overline{E}$ transitions LOW.

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ (Continued)

No.	Symbol		Parameter	1600A-30 1601A-30		1600A-35 1601A-35		1600A-45 1601A-45		1600A-55 1601A-55		1600A-70 1601A-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1														
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	30		35		45		55		70		ns
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write (Notes 7 & 12)	0		0		0		2		5		ns
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		2		5		ns
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable (Notes 4 & 9)	0	12	0	12	0	15	0	18	0	20	ns
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		5		5		ns

Timing Waveforms (Continued)

Write Cycle 1



TL/D/9677-9

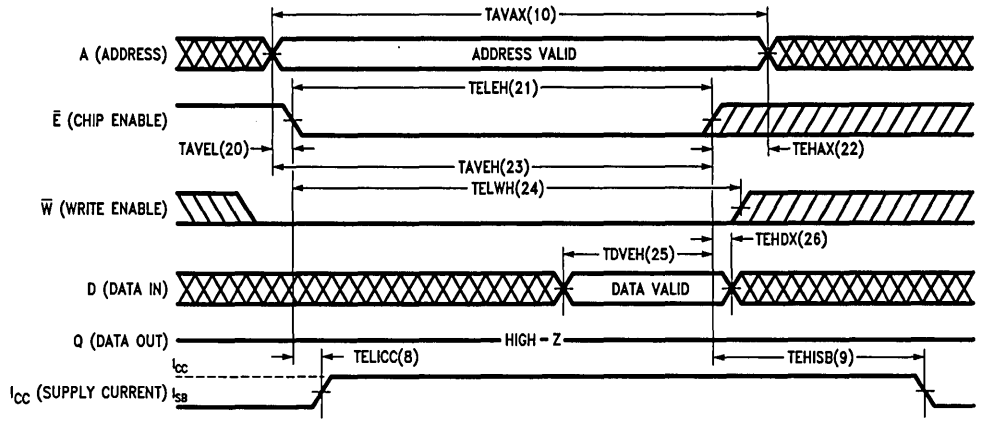
This write cycle is $\overline{W}$ controlled, where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out may become active, requiring observance of TWLQZ to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ (Continued)

No.	Symbol		Parameter	1600A-30 1601A-30		1600A-35 1601A-35		1600A-45 1601A-45		1600A-55 1601A-55		1600A-70 1601A-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2														
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		2		5		ns
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		2		5		ns

Timing Waveforms (Continued)

Write Cycle 2



TL/D/9677-10

This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (TRI-STATE) at the beginning of the write cycle, precluding potential data contention in common I/O applications.

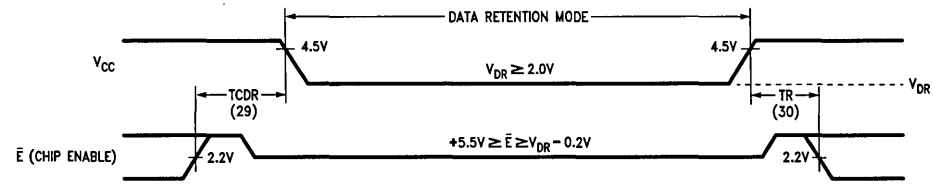
DC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter		Conditions	1600A-30 1601A-30		1600A-35 1601A-35		1600A-45 1601A-45		1600A-55 1601A-55		1600A-70 1601A-70		Units
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current (except DQ)		$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2		±2		±2	μA
I_{LO}	Output Leakage Current (DQ)		$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current		Min Read Cycle Time Duty Cycle = 100% Output Open		105		90		80		80		80	mA
I_{SB1}	Standby Supply Current		$\overline{E} = V_{IH}$, (Note 1)		25		25		25		25		25	mA
I_{SB2}	Full Standby Supply Current	1600A	(Note 2)		15		15		15		15		15	mA
		1601A	(Note 2)		5		5		5		5		5	
V_{OL}	Output LOW Voltage		$I_{OL} = 8.0$ mA		0.4		0.4		0.4		0.4		0.4	V
V_{OH}	Output HIGH Voltage		$I_{OH} = -4.0$ mA	2.4		2.4		2.4		2.4		2.4		V
V_{OH}	Output HIGH Voltage		$I_{OH} = -0.05$ mA	$V_{CC}-0.4$		$V_{CC}-0.4$		$V_{CC}-0.4$		$V_{CC}-0.4$		$V_{CC}-0.4$		V

Data Retention Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 2.0V$ to $5.5V$

No.	Symbol	Parameter	Conditions		Min	Max	Units
27	V_{DR}	V_{CC} Voltage for Data Retention	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$		2.0	5.5	V
28	I_{CCDR}	Data Retention Current (Note 14)	$V_{DR} = 2.0V$	$T_C = -55°C$ to $+25°C$		5	μA
				$T_C = -55°C$ to $+125°C$		200	μA
			$V_{DR} = 3.0V$	$T_C = -55°C$ to $+25°C$		8	μA
				$T_C = -55°C$ to $+125°C$		400	μA
29	TCDR	Chip Disable to Data Retention Time	(Note 4)		0		ns
30	TR	Recovery Time	(Notes 4 & 13)		TAVAX		ns

Data Retention Waveform



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Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \leq \overline{E} \leq V_{CC} + 0.2V$, and all other inputs, (including the data inputs at steady state and satisfying one of two conditions: Either, $V_{CC} - 0.2V \leq V_{IN} \leq V_{CC} + 0.2V$ or $V_{SS} - 0.2V \leq V_{IN} \leq V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active) and remain valid at least TELQV after $\overline{E}$ transitions LOW. Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ± 500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2.*

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.

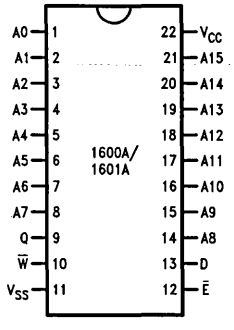
Note 12: Timing specifications of Data Setup to End of Write, Data Hold After End of Write, and Address Hold After End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ and $V_{IN} = V_{DR}$.

Connection Diagrams

22-Pin DIP

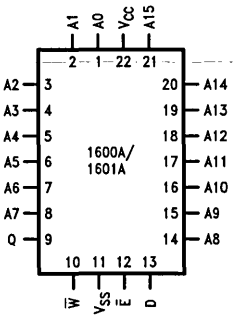


TL/D/9677–1

Top View

See NS Package Number D22D*

22-Pin LCC

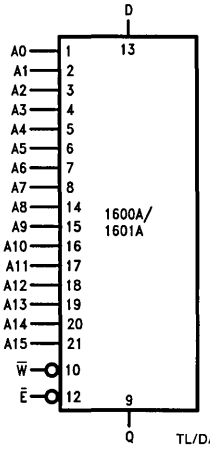


TL/D/9677–2

Top View

See NS Package Number E22A*

Logic Symbol



TL/D/9677–3

Pin Names

A0–A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
V_{CC}	Power (5.0V)
V_{SS}	Ground (0V)

Order Number

1600ADMQB30, 1601ADMQB30
1600ADMQB35, 1601ADMQB35
1600ADMQB45, 1601ADMQB45
1600ADMQB55, 1601ADMQB55
1600ADMQB70, 1601ADMQB70
1600ALMQB30, 1601ALMQB30
1600ALMQB35, 1601ALMQB35
1600ALMQB45, 1601ALMQB45
1600ALMQB55, 1601ALMQB55
1600ALMQB70 or 1601ALMQB70

*For most current package information, contact product marketing.

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Reference Levels	1.5V
Output Load	(See *Figures 1* and *2*)

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

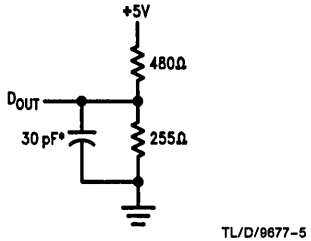
Effective capacitance calculated from the equation.

$$C = \frac{\Delta Q}{\Delta V} \text{ where } \Delta V = 3V$$

Truth Table

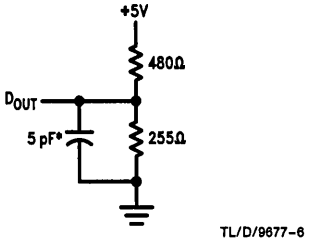
Mode	$\overline{E}$	$\overline{W}$	D	Q	Power Level
Standby	H	X	X	HIGH Z	Standby
Read	L	H	X	D	Active
Write	L	L	D	HIGH Z	Active

HIGH Z = High impedance
D = Valid data bit
X = Don't care



TL/D/9677-5

FIGURE 1. Output Load



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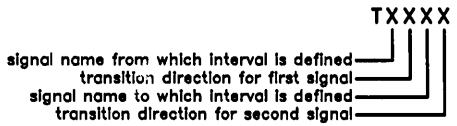
*Including scope and jig.

FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)

STANDARD TIMING PARAMETER ABBREVIATIONS



TL/D/9677-11

The transition definitions used in this data sheet are:

H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

TL/D/9677-12

INVALID or Don't Care.

TL/D/9677-13

Transition from HIGH to LOW level, may occur any time during this period.

TL/D/9677-14

Transition from LOW to HIGH level, may occur any time during this period.

National Semiconductor

NM1620/NM1621
16,384 x 4-Bit Static RAM

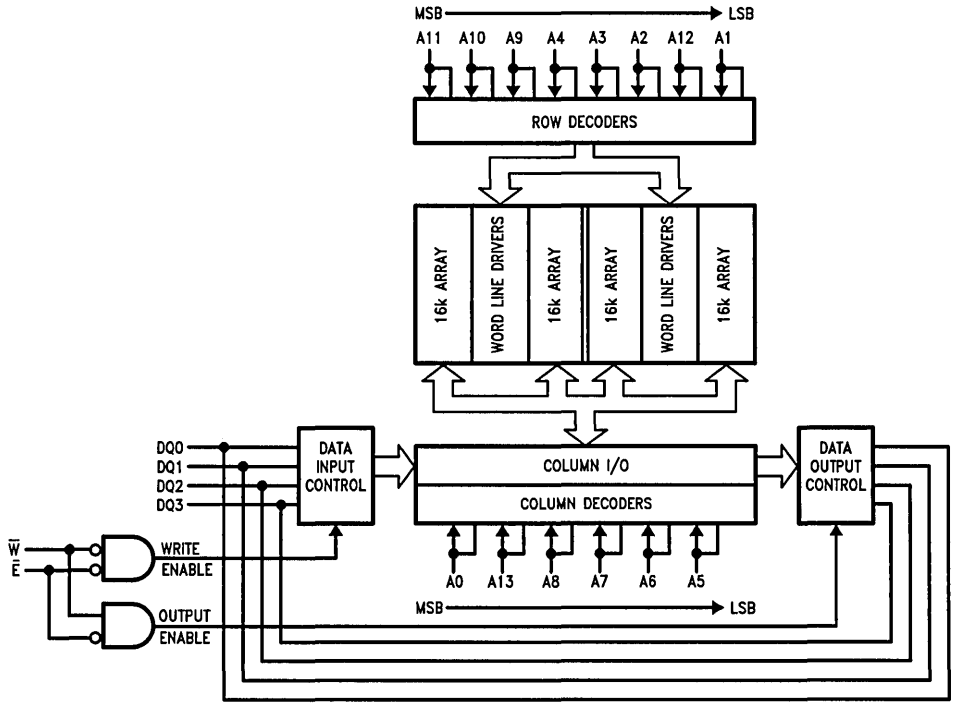
General Description

The NM1620/NM1621 is a 65,536-bit fully-static, asynchronous, random access memory organized as 16,384 words by 4 bits per word. The NM1620/NM1621 is based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device. The NM1621 is identical to the NM1620 with the additional feature of power down for low power battery backup applications.

Features

- Fast address access times: 25 ns/30 ns/35 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Common I/O (TRI-STATE® output)
- Available in 22-Pin DIP, PDIP or LCC
- Low power dissipation (data retention F1621).
  I_{CCDR} = 35 μA maximum (V_{DR} = 2.0V)
  I_{CCDR} = 50 μA maximum (V_{DR} = 3.0V)
- Data retention supply voltage NM1621:
  2.0V to 5.5V

Functional Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2.0V$ to $V_{CC}+2V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$0°C$ to $+70°C$
Power Dissipation	1.0W
Continuous Output Current Per Output	25 mA
Average Input or Output Current (Averaged over any 1 μs time interval.)	25 mA

Recommended Operating Conditions $T_A = 0°C$ to $+70°C$

	Min	Max	Units
Input HIGH Voltage (V_{IH})	2.2	$V_{CC}+0.5$	V
Input LOW Voltage (V_{IL})	-1*	0.8	V

All Voltages are referenced to V_{SS} pin = 0V.

*The device will withstand undershoots to $-3.0V$ of 20 ns duration.

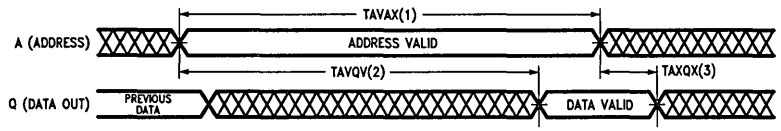
Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN}

No.	Symbol		Parameter	NM1620-25/255 NM1621-25/255		NM1620-30 NM1621-30		NM1620-35 NM1621-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
READ CYCLES										
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	25		30		35		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		25		30		35	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	22		27		30		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		22		27		30	ns
6	TELQX	TLZ	Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Note 9)	0	10	0	12	0	15	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		25		27		30	ns

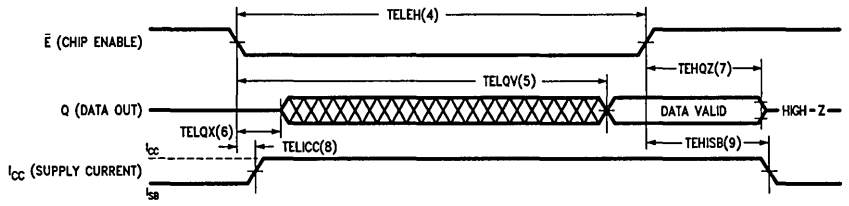
Read Cycle 1



TL/D/9678-7

Access is under address control where $\overline{E}$ is active prior to or within 5 ns of address change. $\overline{W}$ = HIGH.

Read Cycle 2



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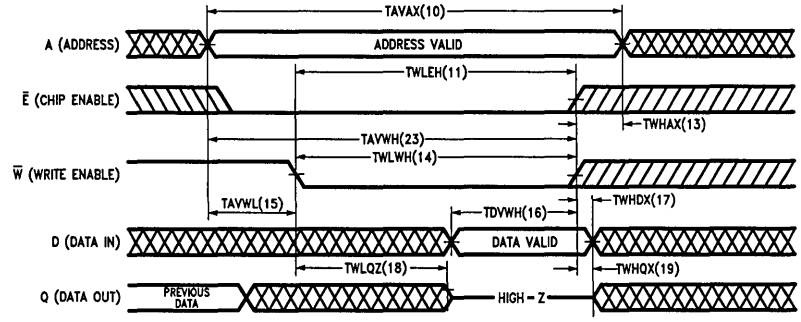
Access is under $\overline{E}$ control where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active. $\overline{W}$ = HIGH. Address remains valid at least TELQV after $\overline{E}$ transitions LOW.

6

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol		Parameter	NM1620-25/255 NM1621-25/255		NM1620-30 NM1621-30		NM1620-35 NM1621-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1										
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	25		30		35		ns
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		ns
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Note 9)	0	9	0	12	0	12	ns
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		ns

Write Cycle 1



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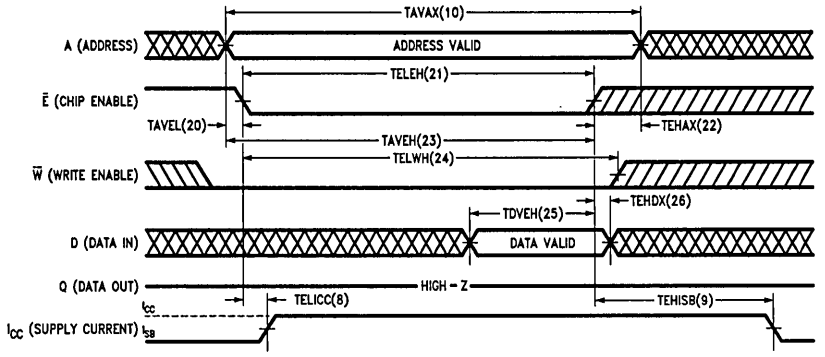
$\overline{W}$ controlled, where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data bus DQ may become active (Q), requiring observance of TWLQZ to avoid data bus contention. At the end of the write cycle the data bus may become active (Q) if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CCMAX}$ to V_{CCMIN} (Continued)

No.	Symbol		Parameter	NM1620-25/255 NM1621-25/255		NM1620-30 NM1621-30		NM1620-35 NM1621-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2										
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		ns
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		ns

Write Cycle 2



TL/D/9678–10

This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (3 state) at the beginning of the write cycle, precluding potential data bus contention.

6

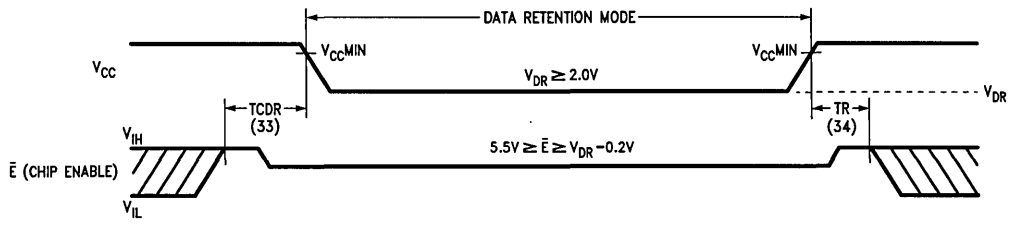
DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{SS} = 0V$

Symbol	Parameter		Conditions	NM1620-25/255 NM1621-25/255		NM1620-30 NM1621-30		NM1620-35 NM1621-35		Units
				Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current (Except DQ)		$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2	μA
I_{LO}	Output Leakage Current (DQ)		$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current		Min Read Cycle Time Duty Cycle = 100% Output Open		120		100		90	mA
I_{SB1}	Standby Supply Current		$\overline{E} = V_{IH}$, (Note 1)		25		25		25	mA
I_{SB2}	Full Standby Supply Current	NM1620	(Note 2)		15		15		15	mA
		NM1621			5		5		5	
V_{OL}	Output LOW Voltage		I_{OL} = 8.0 mA All Outputs Under Load		0.4		0.4		0.4	V
V_{OH1}	Output HIGH Voltage		$I_{OH1} = -4.0$ mA All Outputs Under Load	2.4		2.4		2.4		V
V_{OH2}	Output HIGH Voltage		$I_{OH2} = -0.05$ mA	$V_{CC} - 0.4$		$V_{CC} - 0.4$		$V_{CC} - 0.4$		V
V_{CC}	Supply Voltage		Except Data Retention Mode	**-25**		4.5	5.5	4.5	5.5	V
				4.50	5.5					
				-255						
				4.75	5.5					

Data Retention Characteristics (NM1625 only) $T_C = 0°C$ to $+70°C$, $V_{CC} = 2.0V$ to $5.5V$

No.	Symbol	Parameter	Conditions		Min	Max	Units
31	V_{DR}	V_{CC} Voltage for Data Retention (Note 15)	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$		2.0	5.5	V
32	I_{CCDR}	Data Retention Current (Note 14)	$V_{DR} = 2.0V$	$T_A = 0°C$ to $+70°C$		35	μA
			$V_{DR} = 3.0V$	$T_A = 0°C$ to $+70°C$		50	
33	TCDR	Chip Disable to Data Retention Time (Note 4)			0		ns
30	TR	Recovery Time (Notes 4 & 13)			TAVAX		ns

Data Retention Waveform



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Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \leq \overline{E} \leq V_{CC} + 0.2V$, and all other inputs, (including the data inputs) at steady state and satisfying one of two conditions: Either, $V_{CC} - 0.2V \leq V_{IN} \leq V_{CC} + 0.2V$ or $V_{SS} - 0.2V \leq V_{IN} \leq V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active). Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ± 500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2*. This parameter is sampled, not 100% tested.

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.

Note 12: Timing specifications of Data Setup to End of Write, Data Hold After End of Write, and Address Hold After End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

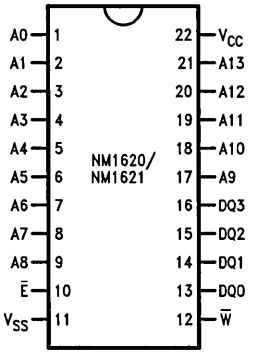
Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ and $V_{IN} = V_{DR}$.

Note 15: V_{IN} applies to all inputs other than $\overline{E}$ and DQ_0–DQ_3. Input conditions for DQ_0–DQ_3 are $V_{SS} - 0.2V \leq DQ \leq V_{SS} + 0.2V$ or $V_{CC} - 0.2V \leq DQ \leq V_{CC} + 0.2V$.

Connection Diagrams

22-Pin DIP (J) and PDIP (N)



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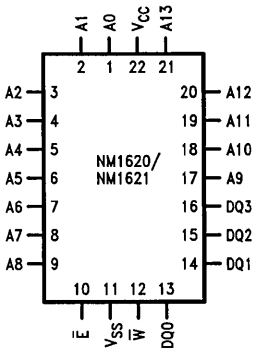
Top View

Order Number NM1620J25, NM1620J255, NM1620J30, NM1620J35, NM1620N25, NM1620N255, NM1620N30, NM1620N35, NM1621J25, NM1621J255, NM1621J30, NM1621J35, NM1621N25, NM1621N255, NM1621N30 or NM1621N35
See NS Package Number D22D* or N22B*

22-Pin LCC (E)



TL/D/9678–2

Top View

Order Number NM1620E25, NM1620E255, NM1620E30, NM1620E35, NM1621E25, NM1621E255, NM1621E30 or NM1621E35
See NS Package Number E22A*

*Call factory for current package outlines and dimensions.

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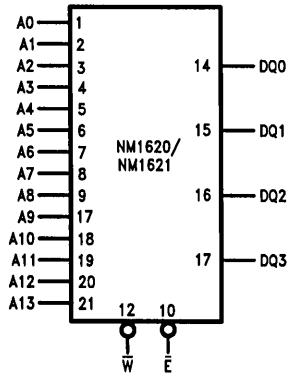
Logic Symbol



TL/D/9678–3

Pin Names

A_0–A_{13}	Address Inputs
$\overline{E}$	Chip Enable Bar
$\overline{W}$	Write Enable Bar
DQ_O–DQ_3	Data Inputs/Outputs
V_{CC}	Power (+5.0V)
V_{SS}	Ground (0V)

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	(See *Figures 1* and *2*)

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation.

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

Truth Table

Mode	$\overline{E}$	$\overline{W}$	DQ_X	Power Level
Standby	H	X	HIGH Z	Standby
Read	L	H	Q	Active
Write	L	L	D	Active

HIGH Z = High impedance
D = Valid data in
X = Don't care
Q = Valid data out

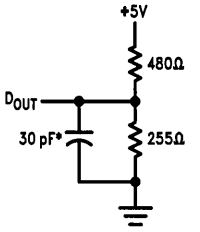


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FIGURE 1. Output Load

*including scope and jig.

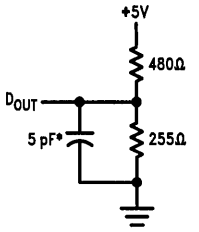

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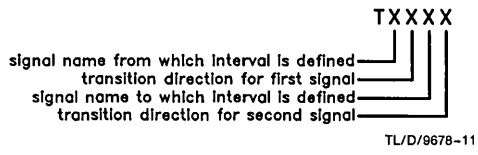
FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)

STANDARD TIMING PARAMETER ABBREVIATIONS



TL/D/9678–11

The transition definitions used in this data sheet are:

H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

TL/D/9678–12

INVALID or Don't Care.

TL/D/9678–13

Transition from HIGH to LOW level, may occur any time during this period.

TL/D/9678–14

Transition from LOW to HIGH level, may occur any time during this period.

National Semiconductor

1620/1621
16,384 x 4-Bit Static RAM
Military Temperature Range

General Description

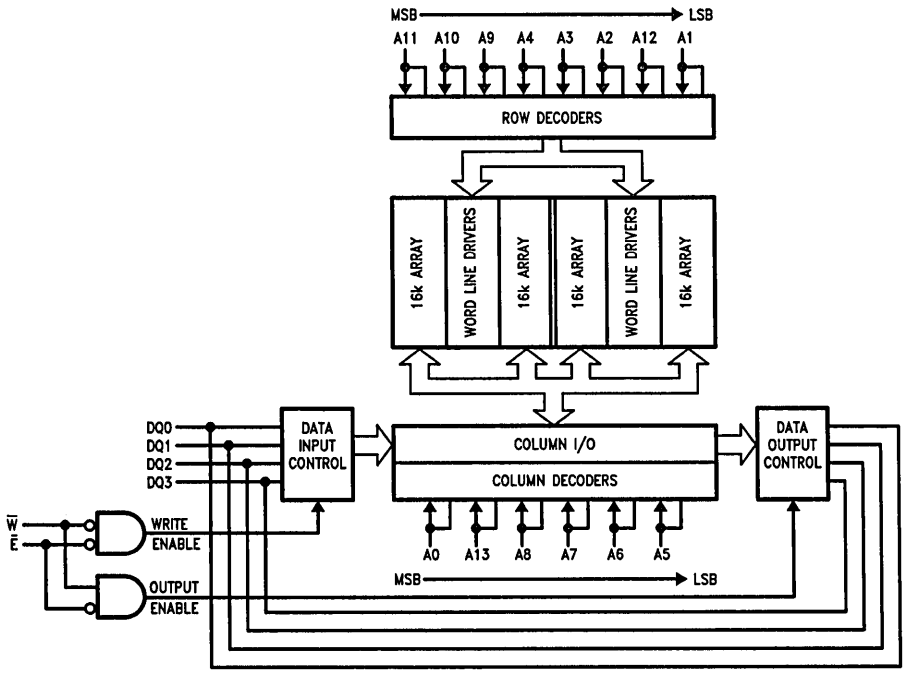
The 1620 is a 65,536-bit fully-static, asynchronous, random access memory organized as 16,384 words by 4-bits per word. The 1620 is based on an advanced, isoplaner, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device.

The 1621 is identical to the 1620 with the additional feature of power-down for low power battery back-up applications. Both parts are processed in full compliance with MIL-STD-883.

Features

- Fast address access times: 30 ns/35 ns/45 ns/55 ns/70 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Common I/O (TRI-STATE®) output
- Available in 22-pin DIP or LCC
- Single +5V operation (±10%)
- Low power dissipation (data retention 1621): I_{CCDR} = 5 μA max (V_{DR} = 2.0V), I_{CCDR} = 8 μA max (V_{DR} = 3.0V) @ 25°C
- Data retention supply voltage 1621 2.0V to 5.5V
- Polyamide die coat for alpha immunity

Functional Block Diagram



TL/D/9680–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2V$ to $V_{CC} + 2V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$-55°C$ to $+125°C$
Power Dissipation	1.0W
Continuous Output Current Per Output	±25 mA
Average Input or Outut Current (Averaged Over Any 1 μs Time Interval)	±25 mA
Thermal Resistance (Junction to Case)	
θJC Side-Braze DIP	15°C/W
θJC LCC	20°C/W

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions $T_C = -55°C$ to $+125°C$

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Input HIGH Voltage (V_{IH})	2.2		$V_{CC} + 0.5$	V
Input LOW Voltage (V_{IL})	−1*		0.8	V

All voltages are referenced to V_{SS} pin = 0V.

*The device will meet −1V or −50 mA whichever occurs first without latching up. The device will also withstand undershoots of −3.0V of 20 ns duration.

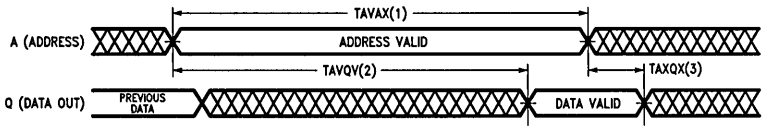
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_C = 55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	1620-30 1621-30		1620-35 1621-35		1620-45 1621-45		1620-55 1621-55		1620-70 1621-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
READ CYCLE														
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time) (Note 7)	30		35		45		55		70		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		30		35		45		55		70	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable High (Note 6)	27		30		40		50		50		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		27		30		40		50		50	ns
6	TELQX	TLZ	(Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Notes 4 & 9)	0	12	0	15	0	15	0	20	0	20	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		27		30		40		50		50	ns

Timing Waveforms

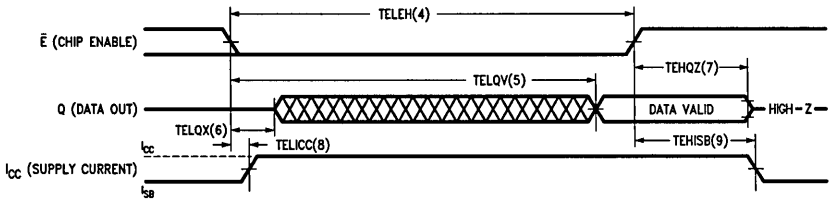
Read Cycle 1



TL/D/9680–7

Access is under address control where $\overline{E}$ is active prior to or within 5 ns after address change. $\overline{W} = V_{IH}$

Read Cycle 2



TL/D/9680–8

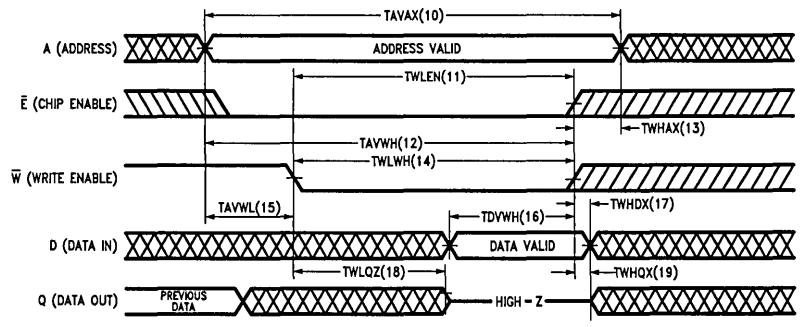
Access is under $\overline{E}$ control where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active. $\overline{W} = V_{IH}$, address remains valid at least TELQV after $\overline{E}$ transitions LOW.

AC Electrical Characteristics $T_C = 55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	1620-30 1621-30		1620-35 1621-35		1620-45 1621-45		1620-55 1621-55		1620-70 1621-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1														
10	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	30		35		45		55		70		ns
11	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
12	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
13	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
14	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
15	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		2		5		ns
16	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
17	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Note 7 & 12)	0		0		0				5		ns
18	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Notes 9 & 4)	0	12	0	12	0	15	0	18	0	20	ns
19	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		5		5		ns

Timing Waveforms (Continued)

Write Cycle 1



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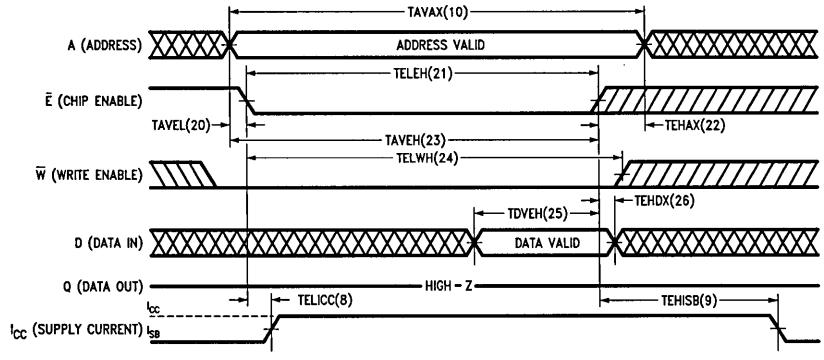
$\overline{W}$ controlled, where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data bus DQ may become active (Q), requiring observance of TWLQZ to avoid data bus contention. At the end of the write cycle the data bus may become active (Q) if $\overline{W}$ becomes active (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).

AC Electrical Characteristics $T_C = 55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ (Continued)

No.	Symbol		Parameter	1620-30 1621-30		1620-35 1621-35		1620-45 1621-45		1620-55 1621-55		1620-70 1621-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2														
20	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		2		5		ns
21	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
22	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
23	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
24	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
25	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
26	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		2		5		ns

Timing Waveforms (Continued)

Write Cycle 2



TL/D/9680–10

This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). In this write cycle the data out remains in the high impedance state (3 state) at the beginning of the write cycle, precluding potential data bus contention.

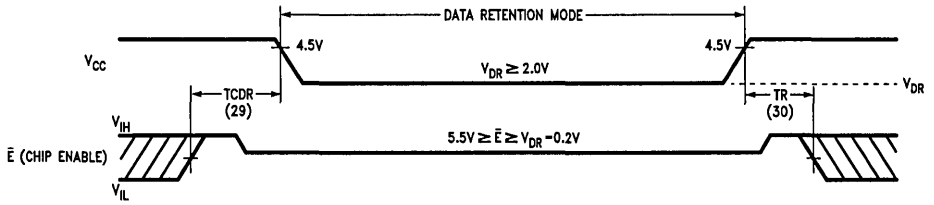
DC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter		Conditions	1620-30 1621-30		1620-35 1621-35		1620-45 1621-45		1620-55 1621-55		1620-70 1621-70		Units
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current (Except DQ)		$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2		±2		±2	µA
I_{LO}	Output Leakage Current (DQ)		$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10		±10		±10	µA
I_{CC}	Dynamic Operating Supply Current		Min Read Cycle Time Duty Cycle = 100% Output Open		120		100		90		110		80	mA
I_{SB1}	Standby Supply Current		$\overline{E} = V_{IH}$ (Note 1)		25		25		25		25		25	mA
I_{SB2}	Full Standby Supply Current	1620	(Note 2)		15		15		15		15		15	mA
		1621	(Note 2)		5		5		5		5		5	mA
V_{OL}	Output LOW Voltage		$I_{OL} = 8.0$ mA. All Outputs Under Load		0.4		0.4		0.4		0.4		0.4	V
V_{OH}	Output HIGH Voltage		$I_{OH} = -4.0$ mA. All Outputs Under Load	2.4		2.4		2.4		2.4		2.4		V
V_{OH}	Output HIGH Voltage		$I_{OH} = -0.05$ mA Other Outputs Open	V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V

Data Retention Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 2.0V$ to $5.5V$

No.	Symbol	Parameter	Conditions		Min	Max	Units
27	V_{DR}	V_{CC} Voltage for Data Retention	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$ (Note 15)		2.0	5.5	V
28	I_{CCDR}	Data Retention Current (Note 14)	$V_{DR} = 2.0V$	$T_C = -55°C$ to $+25°C$		5	μA
				$T_C = -55°C$ to $+125°C$		200	μA
			$V_{DR} = 3.0V$	$T_C = -55°C$ to $+25°C$		8	μA
				$T_C = -55°C$ to $+125C°$		400	μA
29	TCDR	Chip Disable to Data Retention Time (Note 4)			0		ns
30	TR	Recovery Time (Notes 4 & 13)			TAVAX		ns

Data Retention Waveform



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Note 1: Standby current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition. $V_{CC} - 0.2V \le \overline{E} \le V_{CC} + 0.2V$, and all other inputs, (including the data inputs at steady state and satisfying one of two conditions. Either $V_{CC} - 0.2V \le V_{IN} \le V_{CC} + 0.2V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active) and remain valid at least TELQV after $\overline{E}$ transitions LOW. Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{WE}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at ±500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2.*

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.

Note 12: Timing specifications of Data Setup to End of Write, Data Hold after End of Write, and Address Hold after End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition (HIGH) (inactive) is a Don't Care.

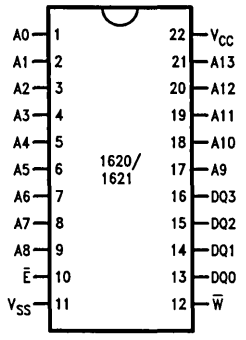
Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ and $V_{IN} = V_{DR}$.

Note 15: V_{IN} applies to all inputs other than $\overline{E}$ and DQ_0–DQ_3. Input conditions for DQ_0–DQ_3 are: $V_{SS} - 0.2V \le DQ \le V_{SS} + 0.2V$ or $V_{CC} - 0.2V \le DQ \le V_{CC} + 0.2V$.

Connection Diagrams

22-Pin DIP



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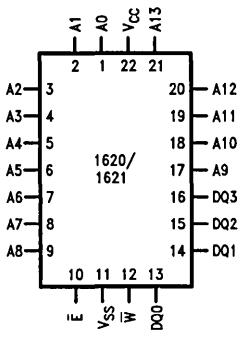
Top View

NS Package Number D24D*

22-Pin LCC

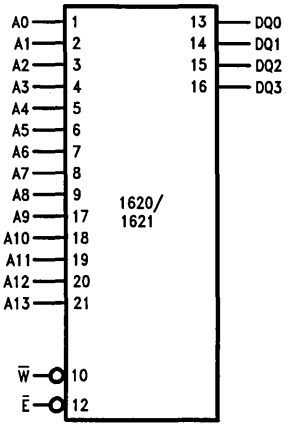


TL/D/9680–2

Top View

NS Package Number E22A*

Logic Symbol



TL/D/9680–3

Pin Names

A_0–A_{13}	Address Inputs
$\overline{E}$	Chip Enable Bar
$\overline{W}$	Write Enable Bar
DQ_0–DQ_3	Data Inputs/Outputs
V_{CC}	Power (+5.0V)
V_{SS}	Ground (0V)

Order Number
1620DMQB30, 1621DMQB30,
1620DMQB35, 1621DMQB35,
1620DMQB45, 1621DMQB45,
1620DMQB55, 1621DMQB55,
1620DMQB70, 1621DMQB70,
1620LMQB30, 1621LMQB30,
1620LMQB35, 1621LMQB35,
1620LMQB45, 1621LMQB45,
1620LMQB55, 1621LMQB55,
1620LMQB70, 1621LMQB70

*For most current package information, contact product marketing.

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	(See *Figures 1* and *2*)

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

Truth Table

Mode	$\overline{E}$	$\overline{W}$	DQ_X	Power Level
Standby	H	X	HIGH Z	Standby
Read	L	H	Q	Active
Write	L	L	D	Active

HIGH Z = High impedance
D = Valid data in
X = Don't care
Q = Valid data out

6

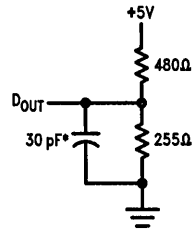


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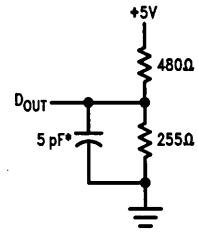
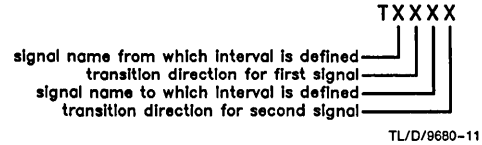
FIGURE 1. Output Load



TL/D/9680–6

FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX)

STANDARD TIMING PARAMETERS ABBREVIATIONS



TL/D/9680–11

The transition definitions used in this data sheet are:

H = transition to high state.

L = transition to low state.

V = transition to valid state.

X = transition to invalid or don't care condition.

Z = transition to off (high impedance condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

TL/D/9680–12

INVALID or Don't Care.

TL/D/9680–13

Transition from HIGH to LOW level may occur any time during this period.

TL/D/9680–14

Transition from LOW to HIGH level may occur any time during this period.

National Semiconductor

NM1624/NM1625
16,384 x 4-Bit Static RAM

General Description

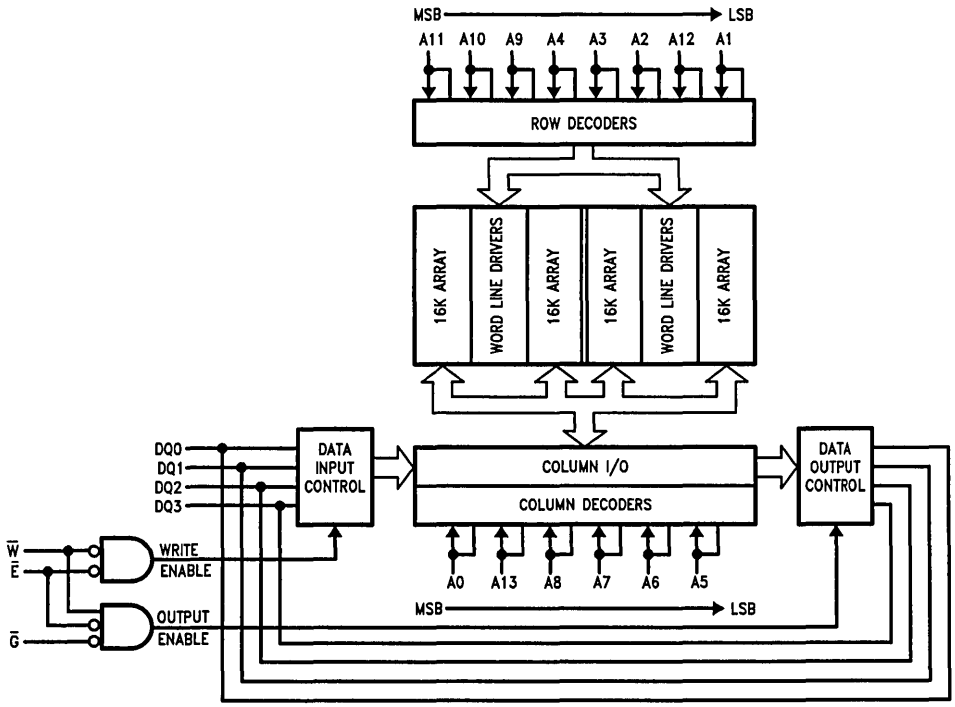
The NM1624/NM1625 are 65,536-bit fully-static, asynchronous, random access memories organized as 16,384 words by 4-bits per word. The NM1624/NM1625 are based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device.

The NM1625 is identical to the NM1624 with the additional feature of power-down for low power battery back-up applications.

Features

- Output enable access times: 10 ns/12 ns/15 ns
- Fast address access times: 25 ns/30 ns/35 ns (maximum)
- Enable read access faster than address access
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Common I/O (TRI-STATE® output)
- Available in 24-pin DIP, PDIP, or 28-pin LCC
- Low power dissipation (data retention NM1625)
  I_{CCDR} = 35 μA max (V_{DR} = 2.0V),
  I_{CCDR} = 50 μA max (V_{DR} = 3.0V)
- Data retention supply voltage NM1625: 2.0V to 5.5V

Functional Block Diagram



TL/D/9679–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2.0V$ to $V_{CC} + 2V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$0°C$ to $+70°C$
Power Dissipation	1.0W
Continuous Output Current per Output	25 mA
Average Input or Output Current (Averaged over Any 1 μs Time Interval)	25 mA

Recommended Operating Conditions $T_A = 0°C$ to $+70°C$

	Min	Max	Units
Input HIGH Voltage (V_{IH})	2.2	$V_{CC} + 0.5$	V
Input LOW Voltage (V_{IL})	−1*	0.8	V

All voltages are referenced to V_{SS} pin = 0V.

*The device will withstand undershoots to −3.0V of 20 ns duration.

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

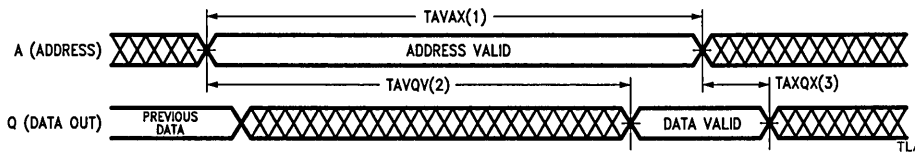
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CC\,MIN}$ to $V_{CC\,MAX}$

No.	Symbol		Parameter	NM1624-25/255 NM1625-25/255		NM1624-30 NM1625-30		NM1624-35 NM1625-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
READ CYCLES										
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	25		30		35		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		25		30		35	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	22		27		30		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		22		27		30	ns
6	TELQX	TLZ	(Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Note 9)	0	10	0	12	0	15	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		25		27		30	ns
10	TGLQV	TOE	Output Enable LOW to Output Valid (Output Enable Access)		10		12		15	ns
11	TGLQX	TOLZ	Output Enable LOW to Output Invalid (Output Enable to Output Active) (Note 4)	0		0		0		ns
12	TGHQZ	TOHZ	Output Enable HIGH to Output High Z (Output Enable Off to Output High Z) (Note 9)		10		12		15	ns
13	TGHQX		Output Enable HIGH to Output Invalid (Output Hold Time) (Note 4)	0		0		0		ns

Timing Waveforms

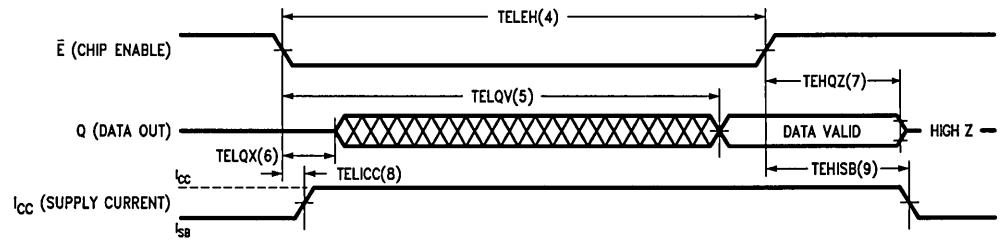
Read Cycle 1



TL/D/9679-8

Access is under address control where $\overline{E}$ is active prior to 5 ns of address change. $\overline{W}$ = HIGH, $\overline{G}$ = LOW.

Read Cycle 2

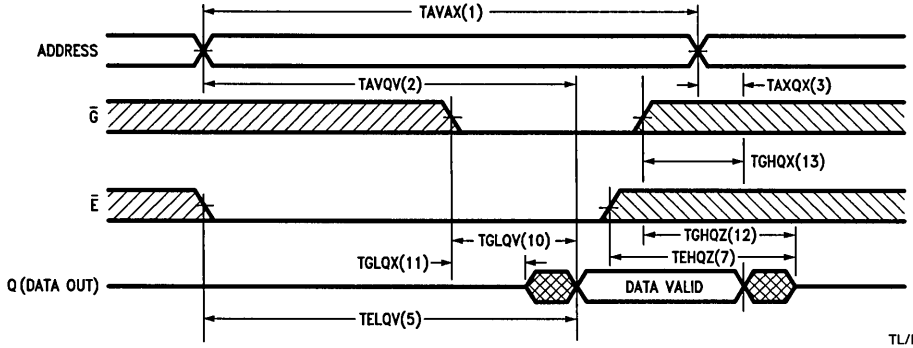


TL/D/9679-9

Access is under $\overline{E}$ control where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active (LOW). $\overline{W}$ = HIGH, $\overline{G}$ = LOW. Address remains valid at least TELQV after $\overline{E}$ transitions LOW.

Timing Waveforms (Continued)

Read Cycle 3



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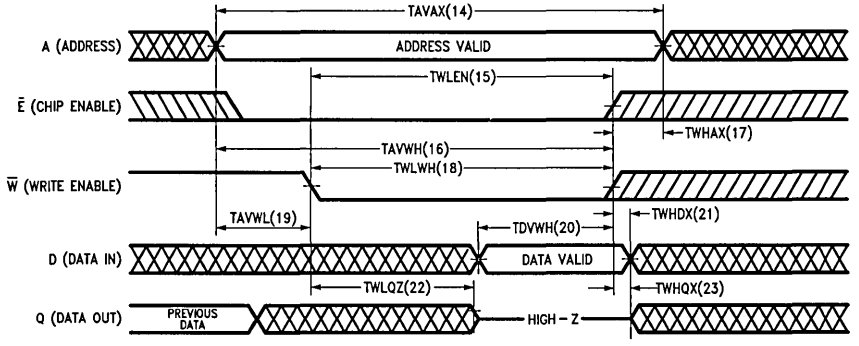
Access is under $\overline{G}$ control. $\overline{W}$ = HIGH.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$ (Continued)

No.	Symbol		Parameter	NM1624-25/255 NM1625-25/255		NM1624-30 NM1625-30		NM1624-35 NM1625-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1										
14	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	25		30		35		ns
15	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
16	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
17	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
18	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
19	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		ns
20	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
21	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
22	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Note 9)	0	9	0	12	0	12	ns
23	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		ns

Timing Waveforms (Continued)

Write Cycle 1



TL/D/9679–11

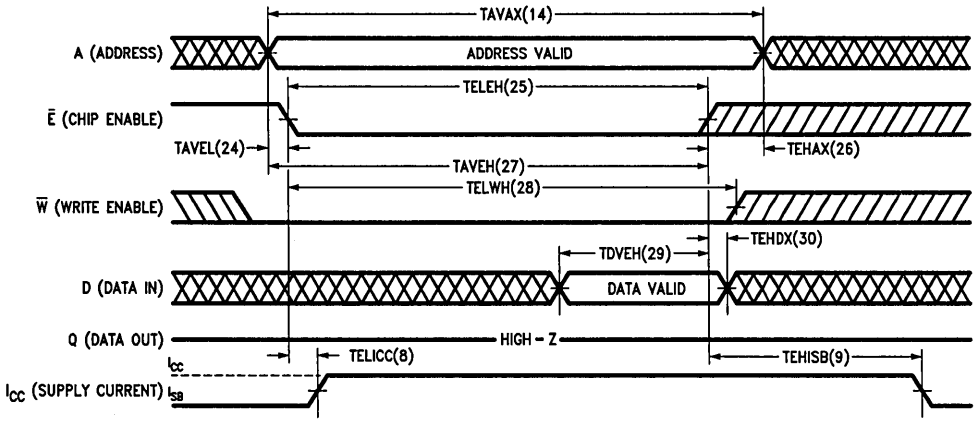
$\overline{W}$ controlled where $\overline{E}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). $\overline{G}$ = HIGH. In this write cycle the data bus DQ may become active (Q), requiring observance of TWLQZ to avoid data bus contention. At the end of the write cycle the data bus may become active (Q) if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{E}$ becoming inactive (HIGH).

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$ (Continued)

No.	Symbol		Parameter	NM1624-25/255 NM1625-25/255		NM1624-30 NM1625-30		NM1624-35 NM1625-35		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2										
24	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		ns
25	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
26	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		ns
27	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	19		22		25		ns
28	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	19		22		25		ns
29	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		10		12		ns
30	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		ns

Timing Waveforms (Continued)

Write Cycle 2



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This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). $\overline{G} = V_{IH}$. In this write cycle the data out remains in the high impedance state (TRI-STATE) at the beginning of the write cycle, precluding potential data bus contention.

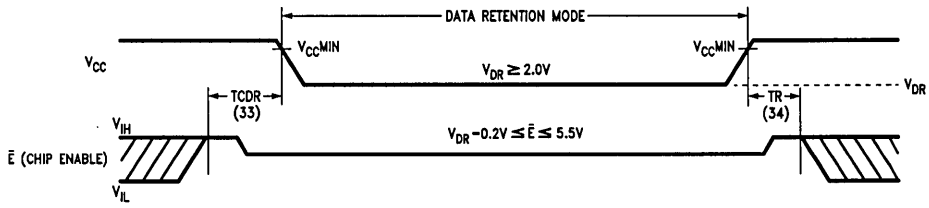
DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{SS} = 0V$

Symbol	Parameter		Conditions	NM1624-25/255 NM1625-25/255		NM1624-30 NM1625-30		NM1624-35 NM1625-35		Units
				Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current (Except DQ)		$V_{SS} \le V_{IN} \le V_{CC}$		±2		±2		±2	μA
I_{LO}	Output Leakage Current (DQ)		$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current		Min Read Cycle Time Duty Cycle = 100% Output Open		120		100		90	mA
I_{SB1}	Standby Supply Current		$\overline{E} = V_{IH}$ (Note 1)		25		25		25	mA
I_{SB2}	Full Standby Supply Current	NM1624	(Note 2)		15		15		15	mA
		NM1625			5		5		5	
V_{OL}	Output LOW Voltage		I_{OL} = 8.0 mA All Outputs under Load		0.4		0.4		0.4	V
V_{OH1}	Output HIGH Voltage		I_{OH1} = −4.0 mA All Outputs under Load	2.4		2.4		2.4		V
V_{OH2}	Output HIGH Voltage		I_{OH2} = −0.05 mA Other Outputs Open	$V_{CC}-0.4$		$V_{CC}-0.4$		$V_{CC}-0.4$		V
V_{CC}	Operating Supply		Except Data Retention Mode	**-25**						
				4.5	5.5	4.5	5.5	4.5	5.5	V
				-255						
				4.75	5.5					

Data Retention Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 2.0V$ to $5.5V$ (NM1625 only)

No.	Symbol	Parameter	Conditions		Min	Max	Units
31	V_{DR}	V_{CC} Voltage for Data Retention (Note 15)	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$		2.0	5.5	V
32	I_{CCDR}	Data Retention Current (Note 14)	V_{DR} = 2.0V	T_A = 0°C to 70°C		35	μA
			V_{DR} = 3.0V	T_A = 0°C to 70°C		50	
33	TCDR	Chip Disable to Data Retention Time (Note 4)			0		ns
34	TR	Recovery Time (Notes 4 & 13)			TAVAX		ns

Data Retention Waveform



TL/D/9679–13

Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \leq \overline{E} \leq V_{CC} + 0.2V$, and all other inputs, (including the data inputs) at steady state and satisfying one of two conditions. Either $V_{CC} - 0.2V \leq V_{IN} \leq V_{CC} + 0.2V$ or $V_{SS} - 0.2V \leq V_{IN} \leq V_{SS} + 0.2V$. This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before, or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active). Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ±500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2.* This parameter is sampled, not 100% tested.

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.

Note 12: Timing specifications of Data Setup to End of Write, Data Hold after End of Write, and Address Hold after End of Write are all referenced to the time when the first of $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

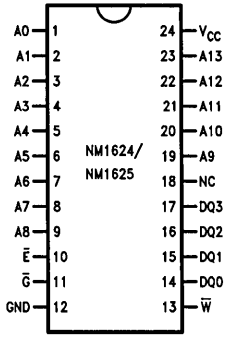
Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ and $V_{IN} = V_{DR}$.

Note 15: V_{IN} applies to all inputs other than $\overline{E}$ and DQ_0–DQ_3. Input conditions for DQ_0–DQ_3 are: $V_{SS} - 0.2V \leq DQ \leq V_{SS} + 0.2V$ or $V_{CC} - 0.2V \leq DQ \leq V_{CC} + 0.2V$.

Connection Diagrams

24-Pin DIP (J) and PDIP (N)

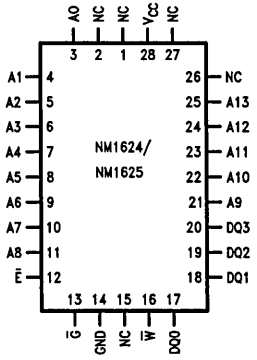


TL/D/9679-1

Top View

Order Number NM1624J25, NM1624J255, NM1624J30, NM1624J35, NM1624N25, NM1624N255, NM1624N30, NM1624N35, NM1625J25, NM1625J255, NM1625J30, NM1625J35, NM1625N25, NM1625N255, NM1625N30 or NM1625N35
See NS Package Number D24H* or N24D*

28-Pin LCC (E)



TL/D/9679-2

Top View

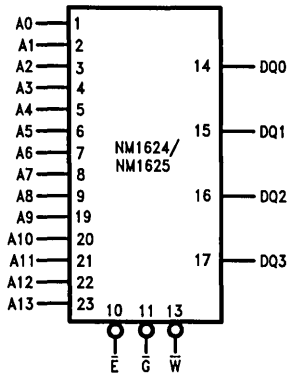
Order Number NM1624E25, NM1624E255, NM1624E30, NM1624E35, NM1625E25, NM1625E255, NM1625E30 or NM1625E35
See NS Package Number E28B

Pin Names

A_0–A_{13}	Address Inputs
$\overline{E}$	Chip Enable Bar
$\overline{W}$	Write Enable Bar
$\overline{G}$	Output Enable Bar
DQ_0–DQ_3	Data Inputs/Outputs
V_{CC}	Power (+5.0V)
V_{SS}	Ground (0V)
NC	No Connect

Logic Symbols

DIP, PDIP



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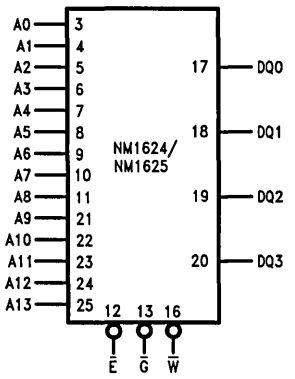
LCC



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AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See *Figures 1* and *2*

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

Truth Table

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ_X	Power Level
Standby	H	X	X	High Z	Standby
Read	L	H	L	Q_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	L	X	D_{IN}	Active

High Z = High impedance
D = Valid data bit in
X = Don't care
Q = Valid data bit out

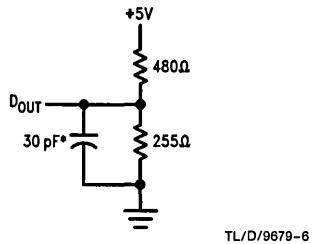

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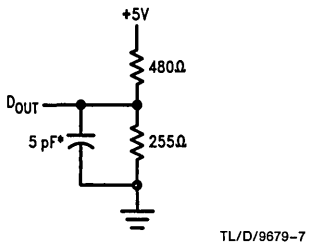
FIGURE 1. Output Load



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*including scope and jig

FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX, TGHQX, TGLQX, TGHQZ)

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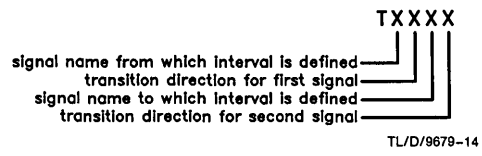
STANDARD TIMING PARAMETER ABBREVIATIONS



TL/D/9679–14

The transition definitions used in this data sheet are:

H = transition to high state.

L = transition to low state.

V = transition to valid state.

X = transition to invalid or don't care condition.

Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

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INVALID or Don't Care

TL/D/9679–16

Transition from HIGH to LOW level may occur any time during this period

TL/D/9679–17

Transition from LOW to HIGH level may occur any time during this period

National Semiconductor

1624/1625
16,384 x 4-Bit Static RAM
Military Temperature Range

General Description

The 1624/1625 are 65,536-bit fully-static, asynchronous, random access memories organized as 16,384 words by 4-bits per word. The 1624/1625 are based on an advanced, isoplanar, oxide-isolation CMOS process. The process utilizes fully-implanted CMOS technology with sub-2 micron design rules and tantalum silicide gate electrodes for high performance. The combination of this high-performance technology, and speed-optimized circuitry results in a very high-speed memory device.

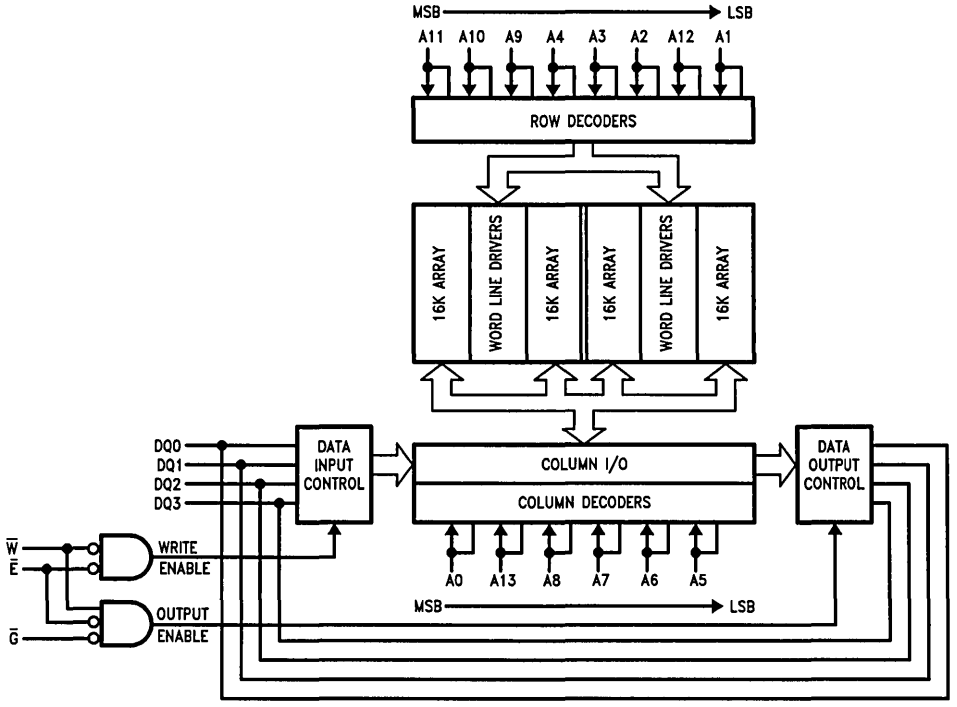
The 1625 is identical to the 1624 with the additional feature of power-down for low power battery back-up applications.

Both parts are processed in full compliance with MIL-STD-883.

Features

- Output enable access times: 12 ns/15 ns/20 ns/25 ns (maximum)
- Fast address access times: 30 ns/35 ns/45 ns/55 ns/70 ns (maximum)
- Minimum write cycle time, including moderate system timing skews, equal to minimum read cycle time
- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- No internal clocks—high speed achieved without address transition detection circuitry
- All inputs and outputs directly TTL compatible
- Common I/O (TRI-STATE®) output
- Available in 24-pin DIP or 28-pin LCC
- Single +5V operation (±10%)
- Low power dissipation (data retention 1625):
  I_{CCDR} = 5 μA max (V_{DR} = 2.0V), 25°C
  I_{CCDR} = 8 μA max (V_{DR} = 3.0V), 25°C
- Data retention supply voltage 1625: 2.0V to 5.5V
- Polyamide die coat for alpha immunity

Functional Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Input or Output Pin with Respect to V_{SS}	$-2.0V$ to $V_{CC} + 2V$
Storage Temperature	$-65°C$ to $+150°C$
Operating Temperature	$-55°C$ to $+125°C$
Power Dissipation	1.0W
Continuous Output Current per Output	
Average Input or Output Current	± 25 mA
(Averaged over Any 1 μs Time Interval)	± 25 mA
Maximum Junction Temperature (T_J)	150°C
Thermal Resistance (Junction to Case)	
θJC Side-Braze DIP	15°C/W
θJC LCC	20°C/W

Note: *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions $T_C = -55°C$ to $+125°C$

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Input HIGH Voltage (V_{IH})	2.2		$V_{CC} + 0.5$	V
Input LOW Voltage (V_{IL})	−1*		0.8	V

All voltages are referenced to V_{SS} pin = 0V.

*The device will meet −1V or −50 mA whichever occurs first without latching up. The device will also withstand undershoots of −3.0V of 20 ns duration.

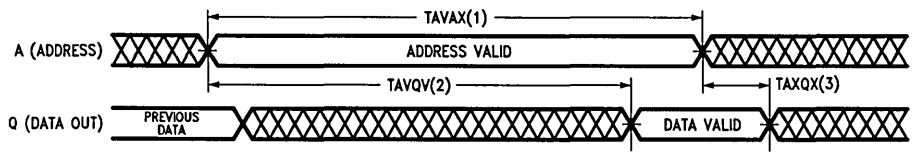
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to the high-impedance circuit.

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

No.	Symbol		Parameter	1624-30 1625-30		1624-35 1625-35		1624-45 1625-45		1624-55 1625-55		1624-70 1625-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
READ CYCLES														
1	TAVAX	TRC	Address Valid to Address Invalid (Read Cycle Time)	30		35		45		55		70		ns
2	TAVQV	TAA	Address Valid to Output Valid (Address Access Time) (Note 5)		30		35		45		55		70	ns
3	TAXQX	TOH	Address Invalid to Output Invalid (Output Hold Time)	5		5		5		5		5		ns
4	TELEH	TRC	Chip Enable LOW to Chip Enable HIGH (Note 6)	27		30		40		50		50		ns
5	TELQV	TACS	Chip Enable LOW to Output Valid (Chip Enable Access Time) (Note 6)		27		30		40		50		50	ns
6	TELQX	TLZ	(Chip Enable LOW to Output Low Z (Chip Enable to Output Active) (Note 4)	5		5		5		5		5		ns
7	TEHQZ	THZ	Chip Enable HIGH to Output High Z (Chip Disable to Output Disable) (Notes 9 & 4)	0	12	0	15	0	15	0	20	0	20	ns
8	TELICC	TPU	Chip Enable LOW to Operating Supply Current (Note 4)	0		0		0		0		0		ns
9	TEHISB	TPD	Chip Enable HIGH to Standby Current (Note 4)		27		30		40		50		50	ns
10	TGLQV	TOE	Output Enable LOW to Output Valid (Output Enable Access)		12		15		20		25		25	ns
11	TGLQX	TOLZ	Output Enable LOW to Output Invalid (Output Enable to Output Active) (Note 4)	0		0		0		0		0		ns
12	TGHQZ	TOHZ	Output Enable HIGH to Output High Z (Output Enable Off to Output High Z) (Notes 9 & 4)		12		15		15		20		20	ns
13	TGHQX		Output Enable HIGH to Output Invalid (Output Hold Time) (Note 4)	0		0		0		0		0		ns

Timing Waveforms

Read Cycle 1



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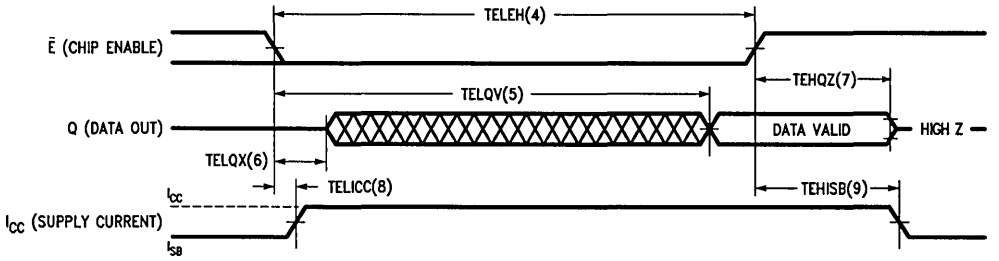
Access is under address control where $\overline{E}$ is active prior to 5 ns after address change. $\overline{W} = V_{IH}$, $\overline{G} = V_{IL}$.

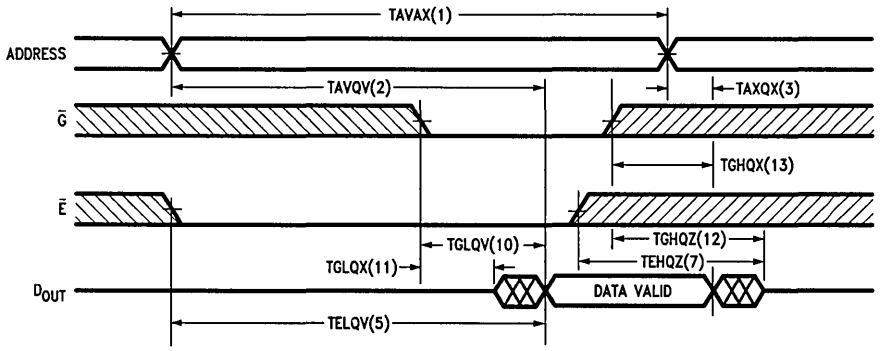
Read Cycle 2



TL/D/9681–9

Access is under $\overline{E}$ control where address is valid a minimum of 5 ns prior to $\overline{E}$ becoming active. $\overline{W} = V_{IH}$, address remains valid at least TELQV after $\overline{E}$ transitions LOW.

Read Cycle 3



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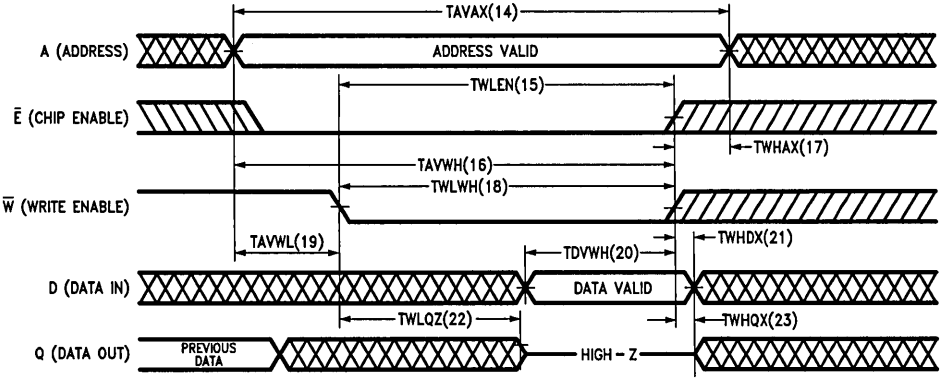
Access is under $\overline{G}$ control. $\overline{W}$ = HIGH.

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ (Continued)

No.	Symbol		Parameter	1624-30 1625-30		1624-35 1625-35		1624-45 1625-45		1624-55 1625-55		1624-70 1625-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 1														
14	TAVAX	TWC	Address Valid to Address Invalid (Write Cycle Time)	30		35		45		55		70		ns
15	TWLEH	TWP	Write LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
16	TAVWH	TAW	Address Valid to Write HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
17	TWHAX	TAH	Write HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
18	TWLWH	TWP	Write LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
19	TAVWL	TAS	Address Valid to Write LOW (Address Setup to Beginning of Write) (Notes 7 & 8)	0		0		0		2		5		ns
20	TDVWH	TDS	Data Valid to Write HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
21	TWHDX	TDH	Write HIGH to Data Don't Care (Data Hold after End of Write) (Notes 7 & 12)	0		0		0		2		5		ns
22	TWLQZ	TWZ	Write LOW to Output High Z (Write Enable to Output Disable) (Notes 9 & 4)	0	12	0	12	0	15	0	18	0	20	ns
23	TWHQX	TOW	Write HIGH to Output Don't Care (Output Active after End of Write) (Note 4)	5		5		5		5		5		ns

Timing Waveforms (Continued)

Write Cycle 1



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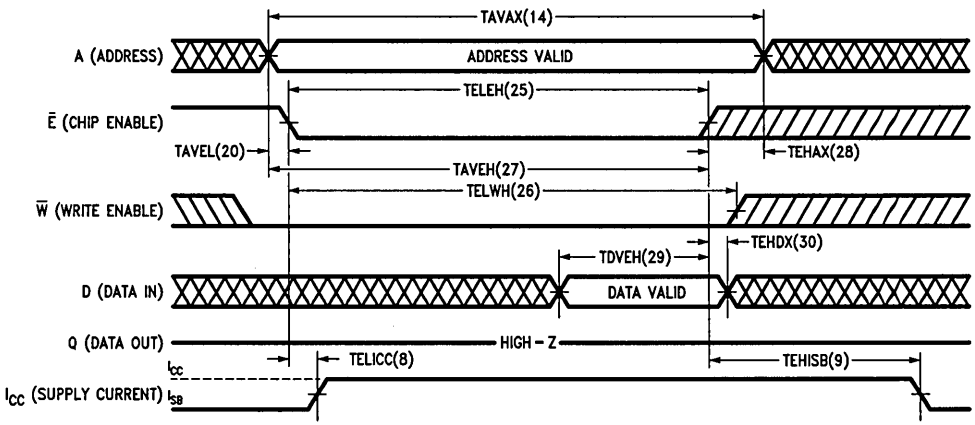
W̄ controlled where Ē is active (LOW) prior to W̄ becoming active (LOW). If $\bar{G} = V_{IL}$ in this write cycle, the data bus DQ may become active (Q), requiring observance of TWLQZ to avoid data bus contention. At the end of the write cycle the data bus may become active (Q) if W̄ becomes inactive (HIGH) prior to Ē becoming inactive (HIGH).

AC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ (Continued)

No.	Symbol		Parameter	1624-30 1625-30		1624-35 1625-35		1624-45 1625-45		1624-55 1625-55		1624-70 1625-70		Units
	Standard	Alternate		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
WRITE CYCLE 2														
24	TAVEL	TAS	Address Valid to Chip Enable LOW (Address Setup) (Notes 7 & 8)	0		0		0		2		5		ns
25	TELEH	TWP	Chip Enable LOW to Chip Enable HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
26	TEHAX	TAH	Chip Enable HIGH to Address Don't Care (Address Hold after End of Write) (Notes 7 & 12)	5		0		0		2		5		ns
27	TAVEH	TAW	Address Valid to Chip Enable HIGH (Address Setup to End of Write) (Note 7)	22		25		30		35		35		ns
28	TELWH	TWP	Chip Enable LOW to Write HIGH (Write Pulse Width) (Notes 7 & 10)	22		25		30		35		35		ns
29	TDVEH	TDS	Data Valid to Chip Enable HIGH (Data Setup to End of Write) (Notes 7 & 12)	10		12		12		15		15		ns
30	TEHDX	TDH	Chip Enable HIGH to Data Don't Care (Data Hold) (Notes 7 & 12)	0		0		0		2		5		ns

Timing Waveforms (Continued)

Write Cycle 2



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This write cycle is $\overline{E}$ controlled, where $\overline{W}$ is active (LOW) prior to, or coincident with, $\overline{E}$ becoming active (LOW). $\overline{G} = V_{IH}$. In this write cycle the data out remains in the high impedance state (3 state) at the beginning of the write cycle, precluding potential data bus contention.

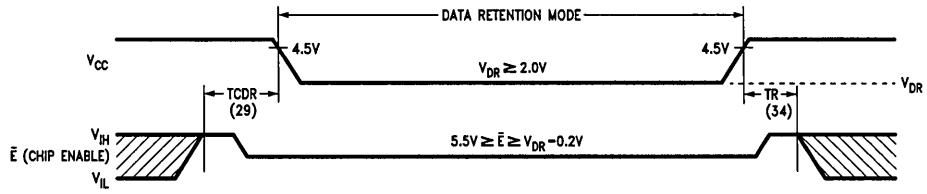
DC Electrical Characteristics $T_C = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Conditions		1624-30 1625-30		1624-35 1625-35		1624-45 1625-44		1624-55 1625-55		1624-70 1625-70		Units
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
I_{LI}	Input Leakage Current (Except DQ)	$V_{SS} \le V_{IN} \le V_{CC}$			±2		±2		±2		±2		±2	μA
I_{LO}	Output Leakage Current (DQ)	$\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$ $V_{SS} \le V_{OUT} \le V_{CC}$			±10		±10		±10		±10		±10	μA
I_{CC}	Dynamic Operating Supply Current	Min Read Cycle Time Duty Cycle = 100% Output Open			120		100		90		110		110	mA
I_{SB1}	Standby Supply Current	$\overline{E} = V_{IH}$ (Note 1)			25		25		25		25		25	mA
I_{SB2}	Full Standby Supply Current	(Note 2)	1624		15		15		15		15		15	mA
			1625		5		5		5		5		5	
V_{OL}	Output LOW Voltage	$I_{OL} = 8.0$ mA All Outputs under Load			0.4		0.4		0.4		0.4		0.4	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0$ mA All Outputs under Load		2.4		2.4		2.4		2.4		2.4		V
		$I_{OH} = -0.05$ mA Other Outputs Open		V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V_{CC} −0.4		V

Data Retention Characteristics T_C −55°C to +125°C, V_{CC} = 2.0V to 5.5V

No.	Symbol	Parameter	Conditions		Min	Max	Units
31	V_{DR}	V_{CC} Voltage for Data Retention (Note 15)	$V_{CC} - 0.2V \le \overline{E} \le +5.5V$ $V_{CC} - 0.2V \le V_{IN} \le +5.5V$ or $V_{SS} - 0.2V \le V_{IN} \le V_{SS} + 0.2V$		2.0	5.5	V
32	I_{CCDR}	Data Retention Current (Note 14)	$V_{DR} = 2.0V$	$T_C = -55°C$ to $+25°C$		5	μA
				$T_C = -55°C$ to $+125°C$		200	μA
			$V_{DR} = 3.0V$	$T_C = -55°C$ to $+25°C$		8	μA
				$T_C = -55°C$ to $+125°C$		400	μA
33	TCDR	Chip Disable to Data Retention Time (Note 4)			0		ns
34	TR	Recovery Time (Notes 4 & 13)			TAVAX		ns

Data Retention Waveform



TL/D/9681–13

Note 1: Standby supply current (TTL) is measured with $\overline{E}$ HIGH (chip deselected) and inputs steady state at valid V_{IL} or V_{IH} levels.

Note 2: Full standby supply current (CMOS) is measured with the enable bar input satisfying the condition: $V_{CC} - 0.2V \leq \overline{E} \leq V_{CC} + 0.2V$, and all other inputs, (including the data inputs at steady state and satisfying one of two conditions. Either $V_{CC} - 0.2V \leq V_{IN} \leq V_{CC} + 0.2V$ or $V_{SS} - 0.2V \leq V_{IN} \leq V_{SS} + 0.2V$). This condition results in a significant reduction in current in the input buffers and consequently a lower overall current level.

Note 3: Operation to specifications guaranteed 2.0 ms after V_{CC} reaches minimum operating voltage.

Note 4: This parameter is sampled, not 100% tested.

Note 5: Address Access Time (Read Cycle 1) assumes that $\overline{E}$ occurs before or within 5 ns after addresses are valid. Timing considerations are referenced to the edges of Address Valid.

Note 6: Enable Access Time (Read Cycle 2) assumes that addresses are valid at least 5 ns prior to $\overline{E}$ transitioning LOW (active) and remain valid at least TELQV after $\overline{E}$ transitions LOW. Timing considerations are then referenced to the LOW (active) transitioning edge of $\overline{E}$.

Note 7: A write condition exists only during intervals where both $\overline{W}$ and $\overline{E}$ are LOW (active). The internal Write starts when the second of these signals becomes LOW (active). The internal Write ends when either of these signals transitions HIGH (inactive).

Note 8: Address setup to beginning of write is measured from the time when the last address input becomes valid to the time when the second of the two signals ($\overline{E}$ or $\overline{W}$) becomes LOW (active). The timing of the first signal ($\overline{W}$ or $\overline{E}$) to transition LOW (active) is a Don't Care.

Note 9: Transition to the high-impedance state is measured at a ±500 mV change from a valid V_{OH} of V_{OL} steady state voltage with the loading specified in *Figure 2.*

Note 10: Write pulse width is measured from the time when the last of the two signals $\overline{E}$ and $\overline{W}$ becomes LOW (active) to the time of the first of $\overline{E}$ or $\overline{W}$ to transition HIGH (inactive).

Note 11: For rise or fall times greater than 3 ns, the timing relationships can no longer be specified to the time when inputs cross the 1.5V level. This is a characteristic of any CMOS device operated outside specified switching levels or transition times.

Note 12: Timing specifications of Data Setup to End of Write, Data Hold after End of Write, and Address Hold after End of Write are all referenced to the time when the first $\overline{E}$ or $\overline{W}$ transitions HIGH (inactive). The timing of the second signal ($\overline{W}$ or $\overline{E}$) to transition HIGH (inactive) is a Don't Care.

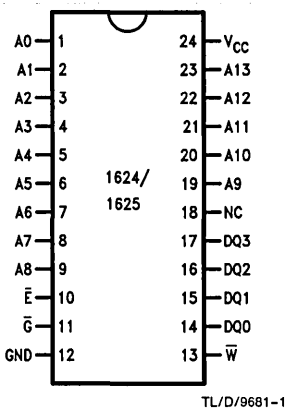
Note 13: TAVAX = Read Cycle Timing.

Note 14: I_{CCDR} is tested with $V_{IN} = 0V$ and $V_{IN} = V_{DR}$.

Note 15: V_{IN} applies to all inputs other than $\overline{E}$ and DQ_0–DQ_3. Input conditions for DQ_0–DQ_3 are: $V_{SS} - 0.2V \leq DQ \leq V_{SS} + 0.2V$ or $V_{CC} - 0.2V \leq DQ \leq V_{CC} + 0.2V$.

Connection Diagrams

24-Pin DIP

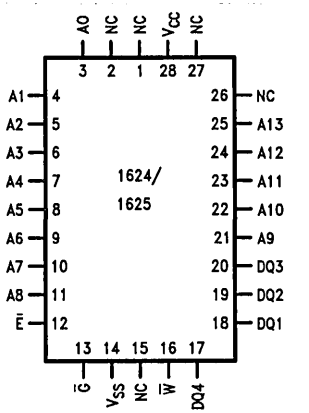


TL/D/9681–1

Top View

NS Package Number D24H*

28-Pin LCC



TL/D/9681–2

Top View

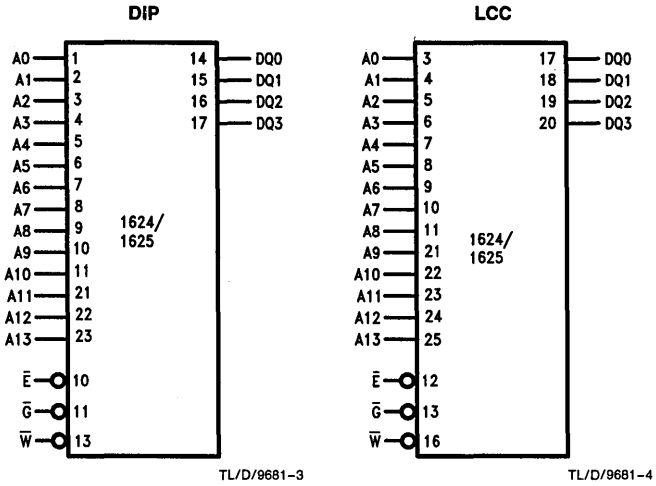
NS Package Number E28B*

*For most current package information, contact product marketing.

Order Number

1624DMQB30, 1625DMQB30
1624DMQB35, 1625DMQB35
1624DMQB45, 1625DMQB45
1624DMQB55, 1625DMQB55
1624DMQB70, 1625DMQB70
1624LMQB30, 1625LMQB30
1624LMQB35, 1625LMQB35
1624LMQB45, 1625LMQB45
1624LMQB55, 1625LMQB55
1624LMQB70, 1625LMQB70

Logic Symbols



Pin Names

A0–A13	Address Inputs
$\overline{E}$	Chip Enable Bar
$\overline{W}$	Write Enable Bar
$\overline{G}$	Output Enable Bar
DQ0–DQ3	Data Inputs/Outputs
V_{CC}	Power (+5.0V)
V_{SS}	Ground (0V)

AC Test Conditions (Notes 3 & 11)

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See *Figures 1* and *2*

Capacitance (Note 4)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	7	pF

Effective capacitance calculated from the equation

$C = \frac{\Delta Q}{\Delta V}$ where $\Delta V = 3V$

Truth Table

Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ_X	Power Level
Standby	H	X	X	High Z	Standby
Read	L	H	L	Q_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	L	X	D_{IN}	Active

High Z = High impedance
D = Valid data bit in
X = Don't care
Q = Valid data bit out

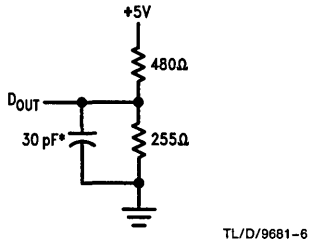


FIGURE 1. Output Load

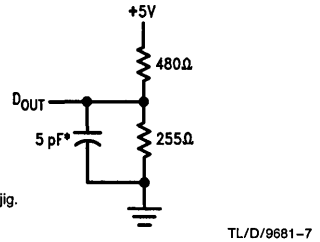
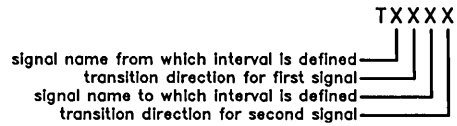


FIGURE 2. Output Load (for TEHQZ, TELQX, TWLQZ, TWHQX, TGHQX, TGHQZ, TGLQX)

STANDARD TIMING PARAMETER ABBREVIATIONS



TL/D/9681–14

The transition definitions used in this data sheet are:

H = transition to high state.
L = transition to low state.
V = transition to valid state.
X = transition to invalid or don't care condition.
Z = transition to off (high impedance) condition.

TIMING VALUES

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for each device parameter. Those timing parameters which state a minimum value do so because the system must supply at least that much time, even though most devices don't require that full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory (like access times) are specified as a maximum time because the device will never provide the data later than this stated value, and will usually provide it much sooner than this.

TL/D/9681–15

INVALID or Don't Care

TL/D/9681–16

Transition from HIGH to LOW level may occur any time during this period

TL/D/9681–17

Transition from LOW to HIGH level may occur any time during this period

National Semiconductor

DM75S68/DM85S68/DM75S68A/DM85S68A
16 x 4 Edge Triggered Registers

General Description

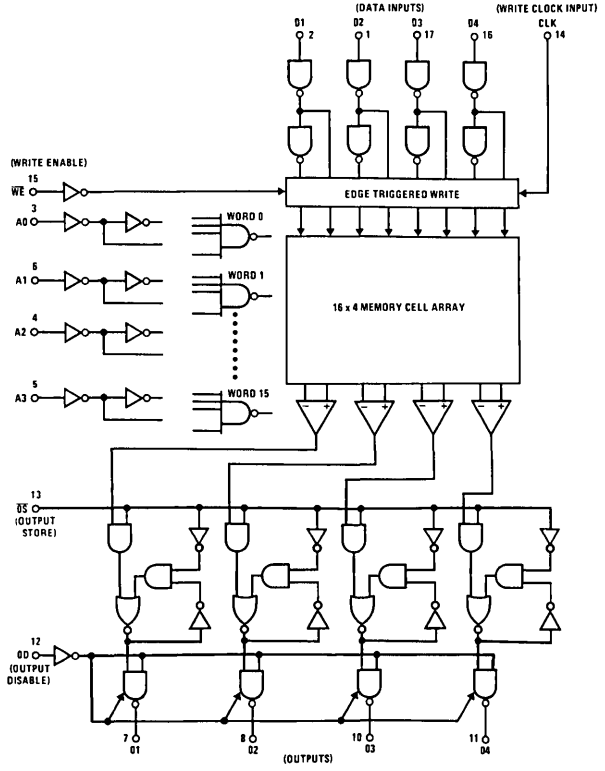
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—20 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

Logic and Block Diagram



TL/F/9233–1

Pin Names

A_0–A_3	Address Inputs
D_1–D_4	Data Inputs
0_1–0_4	Data Outputs
$\overline{WE}$	Write Enable
CLK	Write Clock Input
$\overline{OS}$	Output Store
OD	Output Disable

O_D	$\overline{W_E}$	CLK	$\overline{O_S}$	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	⌐	X	Write Data	Dependent on State of OD and $\overline{OS}$
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Inpedance State

0 = Low Level
1 = High Level
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM85S68/DM85S68A	4.75	5.25	V
DM75S68/DM75S68A	4.5	5.5	V
Temperature, T_A			
DM85S68/DM85S68A	0	70	°C
DM75S68/DM75S68A	−55	+125	°C

Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68/DM75S68A	2.4			V
			I_{OH} = −5.2 mA, DM85S68/DM85S68A	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM75S68/DM75S68A			0.5	V
			DM85S68/DM85S68A			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V	Clock Input			−500	μA
			All Others			−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC}= Max	V_O = 2.4V			+40	μA
			V_O = 0.5V			−40	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68/DM75S68A and across the 0°C to +70°C range for the DM85S68/DM85S68A. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics over recommended operating range of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZH}	Output Enable to High Level			40		35		40		35	ns
t_{ZL}	Output Enable to Low Level			30		24		30		24	ns
t_{HZ}	Output Disable Time from High Level			35		15		35		15	ns
t_{LZ}	Output Disable Time from Low Level			35		18		35		18	ns
t_{AA}	Access Time	Address to Output		55		40		45		24	ns
t_{OSA}		Output Store to Output		35		30		35		20	ns
t_{CA}		Clock to Output		50		40		50		35	ns

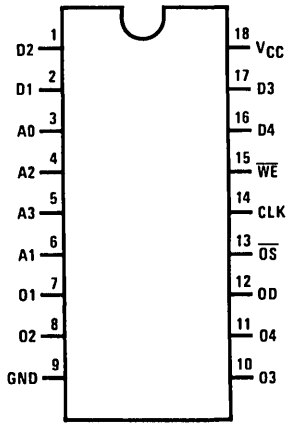
Switching Characteristics

over recommended operating range of T_A and V_{CC} unless otherwise noted (Continued)

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ASC}	Set-Up Time	Address to Clock	25		15		25		15		ns
t_{DSC}		Data to Clock	15		5		15		5		ns
t_{ASOS}		Address to Output Store	40		30		40		10		ns
t_{WESC}		Write Enable Set-Up Time	10		5		10		5		ns
t_{OSSC}		Store before Write	15		10		15		10		ns
t_{AHC}	Hold Time	Address from Clock	15		10		15		10		ns
t_{DHC}		Data from Clock	20		15		20		15		ns
t_{AHOS}		Address from Output Store	10		5		10		2		ns
t_{WEHC}		Write Enable Hold Time	20		15		20		10		ns

Connection Diagram

Dual-In-Line Package

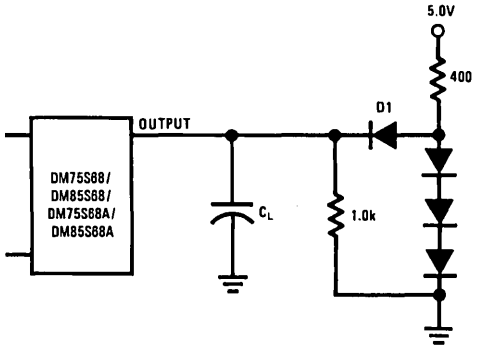


TL/F/9233–2

Top View

Order Number DM75S68J, DM85S68J, DM85S68N, DM75S68AJ, DM85S68AJ or DM85S68AN
See NS Package Number J18A or N18A

AC Test Circuit and Switching Time Waveforms

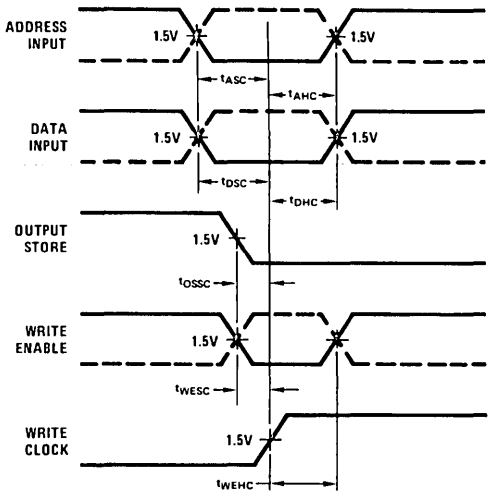


C_L = 5.0 pF for t_{HZ}, t_{LZ}
C_L = 30 pF for all others
C_L includes probe and jig capacitance
All diodes are 1N3064

TL/L/9233-3

Write Cycle

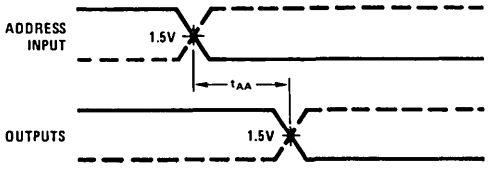
Clock Set-Up and Hold Time



TL/L/9233-4

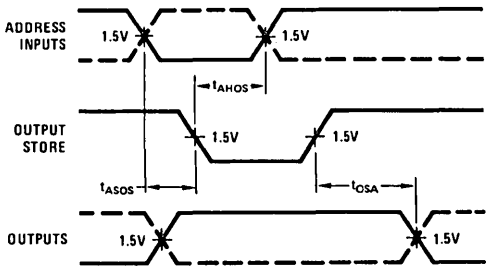
Read Cycle

Address to Output Access Time



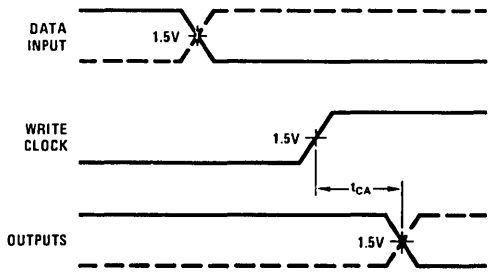
TL/L/9233-6

Output Store Access, Set-Up and Hold Time



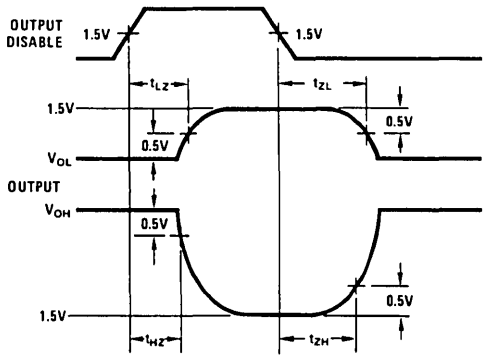
TL/L/9233-7

Clock to Output Access



TL/L/9233-5

Output Disable and Enable Time



TL/L/9233-8

Note: Input waveforms supplied by pulse generator having the following characteristics: V=3.0V, $t_R \leq 2.5$ ns, PRR≤1.0 MHz and Z_{OUT} = 50M.

National Semiconductor

PRELIMINARY

DM75/85X431 64 x 8 No-Fall-Through FIFO Memory

General Description

The device is a first-in-first-out (FIFO) sequential memory organized as 64 words by 8 bits. Data words written into the device are later read from a separate bus in the same order as entered but at an independent rate. Write and read operations may occur concurrently and at any time with respect to each other. The FIFO is a no-fall-through (NFT) type in which new input data becomes available for output in less time than the minimum write/read cycle period.

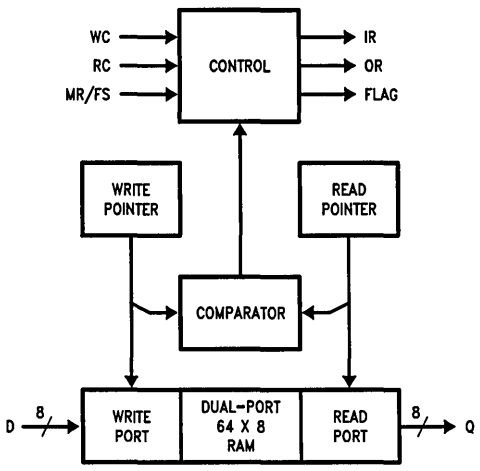
Features

- 64 x 8-bit FIFO memory
- No fall-through delay (first word propagates to output in less than one cycle period)
- 35 MHz write and 50 MHz read clock frequencies
- Totally independent asynchronous write and read clocks
- Cascadable in depth and/or width (requiring no external hardware)
- Status outputs indicate full, empty and partially-filled conditions
- 24-pin 0.3" wide DIP package
- TTL I/O signal levels
- Single +5V supply

Applications

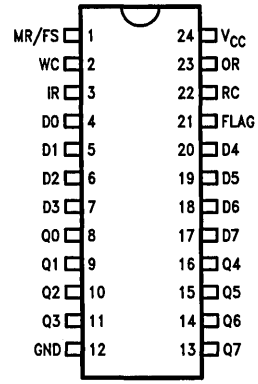
- Data rate translator for computer peripheral controller, eg. disc, tape, printer, graphic display, etc.
- Data rate translator for telecommunications or data communications controller (including local area network)
- ADC or DAC interface buffer for real-time DSP
- Real-time data acquisition buffer
- Variable length shift register for real-time signal delay
- Variable length pipeline register for multiprocessing, DSP, graphics, image analysis, etc.

Block and Connection Diagrams



TL/D/8676-1

Dual-In-Line Package



TL/D/8676-2

Top View

Order Numbers DM75/85X431J or DM85X431N
NS Package Numbers J24F or N24C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} 7V

Input Voltage 7V

Off-State Output Voltage 5.5V

Storage Temperature −65°C to +150°C

ESD Susceptibility (Note 5) To Be Determined

Electrical Characteristics Over Operating Conditions DM75/DM85X431

Symbol	Parameter	Conditions		Guaranteed Limits			Units
				Min	Typ	Max	
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min,	I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max,	V_I = 0.45V			−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max,	V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max,	V_I = 5.5V			1.0	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8 mA for Q Outputs I_{OL} = 4 mA for IR, OR and FLAG Outputs			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −0.9 mA for Q Outputs I_{OH} = −0.6 mA for IR, OR and FLAG Outputs	2.4			V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max,	V_O = 0V	−30		−80	mA
I_{CC}	Supply Current	V_{CC} = Max Inputs Low, Outputs Open			200	230	mA

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Operating Conditions (Note 3)

Symbol	Parameter	DM75X431			DM85X431			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	−55		+125	0		+70	°C
f_{WC}	Write Frequency				35	40	35	MHz
f_{RC}	Read Frequency				50		50	MHz
t_{WWH}	WC Pulse Width High					12	15	ns
t_{WWL}	WC Pulse Width Low					7	10	ns
t_{SDW}	Input Data Setup					13	17	ns
t_{HDW}	Input Data Hold Time					0	5	ns
t_{WRH}	RC Pulse Width High					7	10	ns
t_{WRL}	RC Pulse Width Low					7	10	ns
t_{WM}	Master Reset Pulse Width (Note 4)					38	50	ns
t_{RMW}	Reset Recovery Time					38	50	ns

Note 2: Ambient Temperature.

Note 3: Since the FIFO is a very high speed device, care must be taken in the design of the hardware. Proper device grounding and supply decoupling are crucial to the correct operation of the FIFO.

Note 4: Minimum time between any two consecutive transitions on the MR/FS input.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Initial Conditions	DM75X431			DM85X431			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PRQ}	RC to Data Output						20	27	ns
t_{PWOH}	WC to OR High	Empty, RC = H					15	20	ns
t_{PWIH}	WC Falling to IR High	< 63 Words					11	15	ns
t_{PWHIL}	WC Rising to IR Low	< 63 Words					11	15	ns
t_{PWLIL}	WC Falling to IR Low	63 Words, RC = H					11	15	ns
t_{PRIH}	RC to IR High	Full, WC = L					15	20	ns
t_{PROH}	RC to OR High	> 1 Word					13	18	ns
t_{PROL}	RC to OR Low						10	14	ns
t_{PRIL}	RC Falling to IR Low	63 Words, WC = H					13	18	ns
t_{PWFH}	WC to FLAG High						27	36	ns
t_{PRFL}	RC to FLAG Low						27	36	ns
t_{PDQ}	Transparent D to Q	Empty, WC = H					34	45	ns
t_{PWQ}	WC Rising to Q	Empty					34	45	ns
t_{PMIH}	MR to IR High	Full					28	38	ns
t_{PMOL}	MR to OR Low						15	20	ns
t_{PMFL}	MR to FLAG Low						28	38	ns

Pin Description

V_{CC} Supply voltage.

D0–D7 8-bit data input bus.

Q0–Q7 8-bit data output bus (non-inverted).

WC Write Clock input—latches in data word from D-bus on a high-to-low transition (except when FIFO is full). Data enters the memory while WC is high.

RC Read Clock input—presents next data word onto Q-bus on a low-to-high transition (except when FIFO is empty).

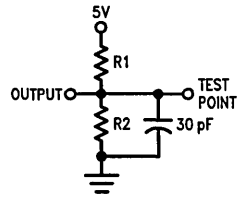
IR Input Ready status output—when high indicates FIFO is ready for another write cycle, ie., FIFO is not full. IR is forced low whenever WC is high (except during 64th write cycle) to accommodate cascading.

OR Output Ready status output—when high indicates FIFO is ready for another read cycle, ie., FIFO is not empty. OR is forced low whenever RC is low to accommodate cascading.

MR/FS Master Reset/FLAG Select input—resets the FIFO to the empty state (internal pointers reset to zero) on either a low-to-high or high-to-low transistion. The state of the MR/FS input during operation selects the waveform to be presented on the FLAG status output.

FLAG Intermediate status FLAG output—if MR/FS input is low, then a high output on FLAG indicates FIFO is at least one quarter filled (16 or more words remaining in memory). If MR/FS is high, then a high output on FLAG indicates FIFO is at least three quarters filled (48 or more words remaining).

Standard Test Load



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I_{OL}	R1	R2
8 mA	560Ω	1100Ω
4 mA	1100Ω	2200Ω

Input Pulse Amplitude = 3V

Input Rise and Fall Time (10%–90%) = 2.5 ns

Measurements made at 1.5V

Functional Description

The NFT FIFO is implemented using a 64 x 8-bit RAM with separate write and read ports. The write port is addressed by the write pointer and the read port by the read pointer. While the WC input is high, a data word on the D inputs is written into the write port of the RAM. The write pointer (initially zero) is incremented on the falling edge of WC, thus concluding a write cycle. The RAM contents addressed by the read pointer (also initially zero) are always presented on the Q outputs. Thus the first word appears on the Q outputs as it is being written. The rising edge of RC increments the read pointer which then accesses the next data word from the RAM's read port.

When the value of the write pointer equals the read pointer, then the FIFO is empty, ie., any data words which had been written have also been read. When the value of the write pointer exceeds the read pointer by 64, then the FIFO is full, ie., the next RAM location into which data should be written contains the oldest word that has not yet been read.

The IR and OR status outputs indicate the full and empty conditions, respectively. When WC is brought low at the end of a write cycle, IR would go high if the FIFO is still not full. If the FIFO becomes full, IR would become low until a vacant

Functional Description (Continued)

RAM location is made available resulting from a read operation (or the Master Reset is activated). WC should remain low until IR goes high. If WC is brought high while IR is still low, then the entire write cycle would be ignored, the RAM contents and write pointer remaining unchanged.

IR is usually driven low whenever WC is high in order to accommodate cascading as described later. However, during the final write cycle (in which the last vacant location is being written) IR would remain high if and as long as RC is high. This is to provide sufficient cycle times to guarantee the proper transfer of data between cascaded devices while reading.

The OR output would go high after the rising edge of RC if the FIFO remains not empty. OR is initially low following a reset until the first word is written into the FIFO. RC should remain high until OR goes high. If RC is brought low before OR goes high, then the read cycle would be inhibited and the next rising edge of RC would not increment the read pointer.

The FIFO resets to the empty state (write and read pointers reset to zero) on either the rising or falling edge of the MR/FS input. Following a reset, IR will be high, provided WC is low, OR and FLAG will be low. WC and RC may be in either state when a reset occurs.

If WC is high following a reset, the first write cycle would not commence until after WC is returned low (a high output on IR must be observed before the FIFO performs any write cycle). Likewise, if RC is low following a reset, the first read cycle would not commence until RC is returned high and a high output is observed on OR (returning RC high does not advance the read pointer).

The FIFO may be operated while the MR/FS input is held either low or high. The state of the MR/FS input during operation selects one of two waveforms to appear on the FLAG status output.

If the FIFO is operated while the MR/FS input is held low, then the FLAG output would indicate when the FIFO is at least one quarter filled, i.e., when the write pointer value exceeds the read pointer by at least 16. If the FIFO is operated while MR/FS is high, then FLAG would indicate when the FIFO is at least three quarters filled, as shown in the following truth table:

# WORDS STORED	FLAG OUTPUT	
	MR/FS = L	MR/FS = H
0–15	L	L
16–47	H	L
48–64	H	H

The FLAG output remains stable throughout all write and read cycles which do not cross the above boundaries. Note that the FLAG waveform selection cannot be switched without resetting the FIFO.

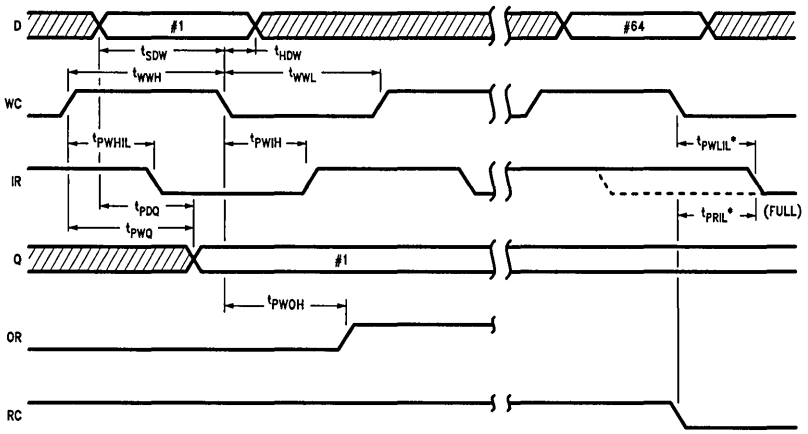
In a system, MR/FS may be connected to either a normally-low or normally-high system reset signal. Even though the FIFO responds to input transitions, conventional system reset pulses, including wakeup circuits, would produce desired results.

FIFO buffers wider than 8 bits can be implemented by connecting multiple chips in parallel. For 64 × 8n configurations, the IR, OR and FLAG status information can be taken from any one of the chips since there is no fall-through delay which may otherwise cause output skew between chips.

FIFO buffers deeper than 64 words can also be implemented by connecting multiple chips in series. To do this, the Q, OR and RC lines of one chip are connected to the D, WC and IR lines, respectively, of the next chip in the series (see "Cascading Devices" block diagram). When the first word is written into the first chip, the resulting rising edge of its OR initiates a write cycle into the second chip, which in turn produces a read cycle from the first chip. The handshaking signals passed over the OR/WC and RC/IR connections between each adjacent pair of chips causes the data word to be passed from one chip to the next until it settles onto the outputs of the last chip in the series. See "Cascaded Write Cycle Waveform" diagram.

As the buffer fills, each chip, beginning with the last, becomes full. A buffer consisting of n chips connected in series can store 63n + 1 words. This is because the last word written into each full chip (except the first chip) remains on the outputs of the previous chip. Each time a word is read from the last chip, one word is transferred down from each of the previous chips (or until an empty chip is encountered). See "Cascaded Read Cycle Waveform".

Write Cycle Timing Waveform



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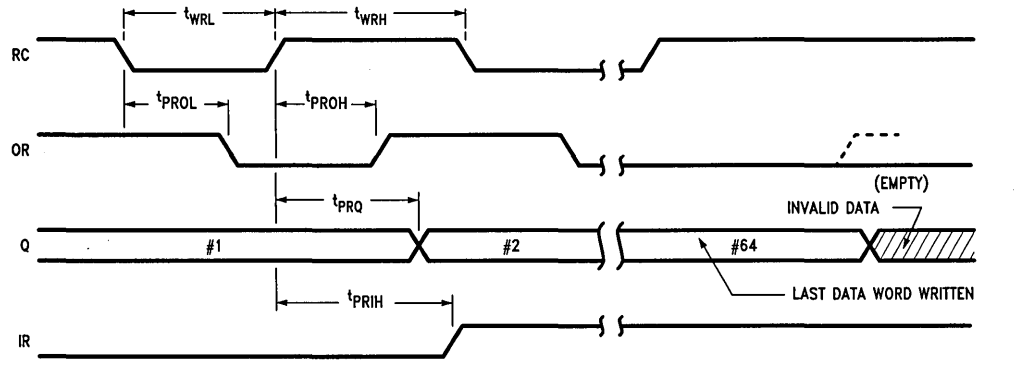
*IR goes low following the first of these two events.

Functional Description (Continued)

Since the control signals and data are passed from chip to chip in a serially cascaded buffer, some fall-through delay is introduced between the input of the first chip and the output of the last. The delay increases with the number of chips cascaded serially.

Chips can be cascaded both serially and in parallel to produce deeper and wider buffers (as shown in "Cascading Devices" block diagram). However, due to the resulting chip-level fall-through delays, it may be necessary to AND-gate the IR outputs of the first level of chips, as with the OR outputs of the last level.

Read Cycle Timing Waveform



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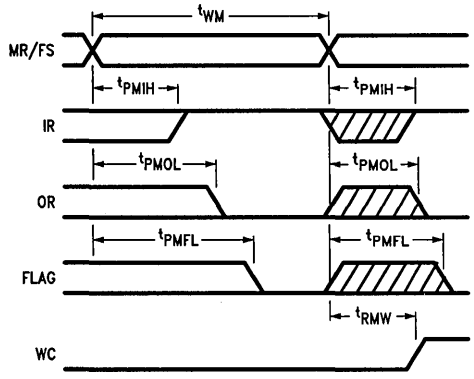
Master Reset Timing Waveform



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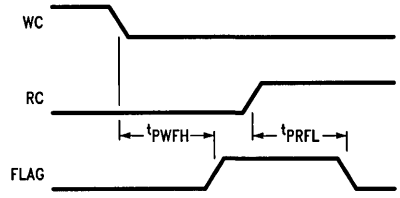
Flag Output Timing Waveform



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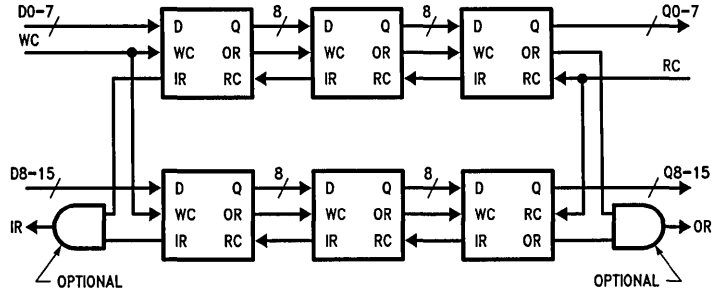
Cascading Devices
(190 × 16 Bit FIFO)



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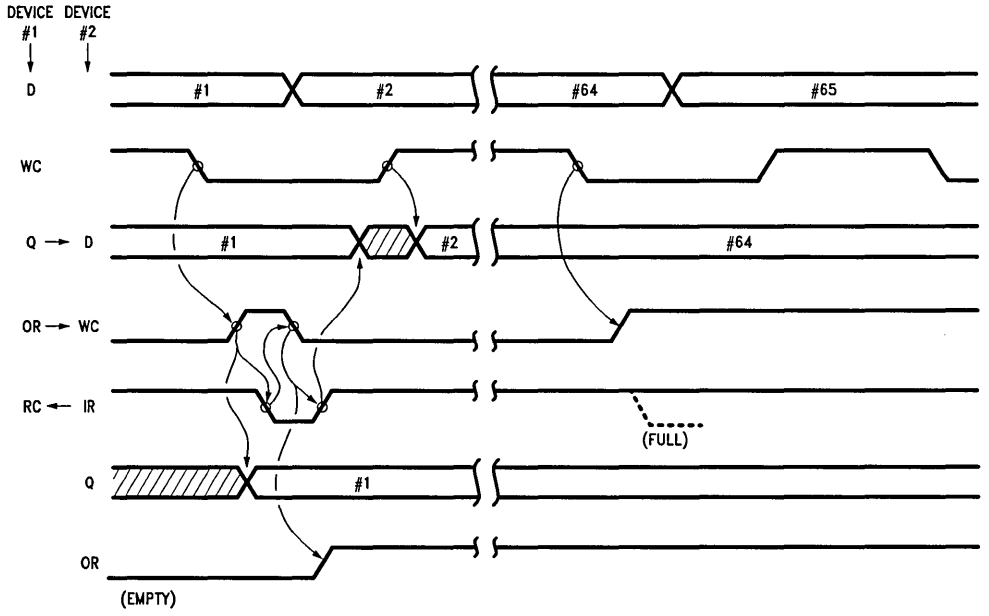
Functional Description (Continued)

Write Cycle Waveform For Two Devices Cascaded Serially



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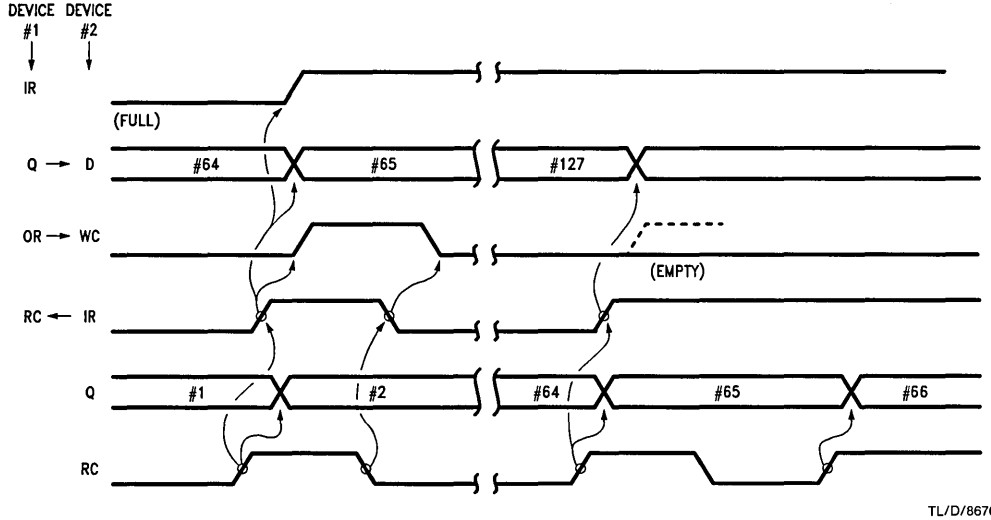
Read Cycle Waveform For Two Devices Cascaded Serially



TL/D/8676–10

National Semiconductor

PRELIMINARY

DM75/85X432 128 x 4, DM75/85X433 128 x 5, No-Fall-Through FIFO Memories

General Description

The device is a first-in-first-out (FIFO) sequential memory organized as 128 words by either 4 or 5 bits. Data words written into the device are later read from a separate bus in the same order as entered but at an independent rate. Write and read operations may occur concurrently and at any time with respect to each other. The FIFO is a no-fall-through (NFT) type in which new input data becomes available for output in less time than the minimum write/read cycle period.

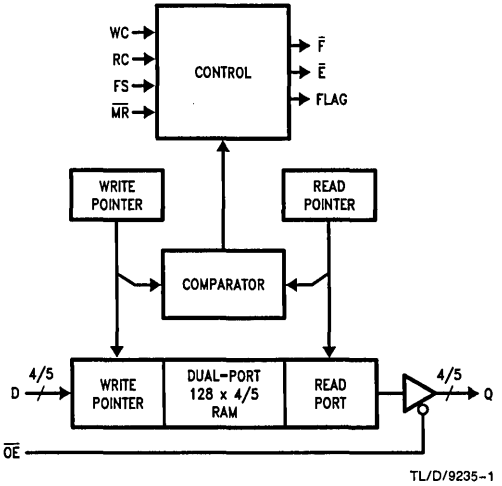
Features

- 128 x 4/5 bit FIFO memory
- No fall-through delay (first word propagates to output in less than one cycle period)
- 35 MHz write and 50 MHz read clock frequencies
- Totally independent asynchronous write and read clocks
- 16 mA TRI-STATE® data outputs for bus drive capability
- Status outputs indicate full, empty and partially-filled conditions
- 18/20 pin 0.3" wide DIP package
- TTL I/O signal levels
- Single +5V supply

Applications

- Data rate translator for computer peripheral controller, eg. disc, tape, printer, graphic display, etc.
- Data rate translator for telecommunications or data communications controller (including local area network)
- ADC or DAC interface buffer for real-time DSP
- Real-time data acquisition buffer
- Variable length shift register for real-time signal delay
- Variable length pipeline register for multiprocessing, DSP, graphics, image analysis, etc.

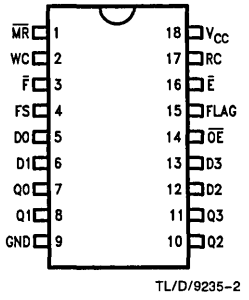
Block and Connection Diagrams



TL/D/9235-1

Dual-In-Line Package

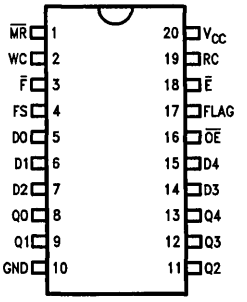
DM75/85X432



TL/D/9235-2

Order Number DM75/85X432J or DM85X432N See NS Package Number J18A or N18A

DM75/85X433



TL/D/9235-3

Order Number DM75/85X433J or DM85X433N See NS Package Number J20A or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 4)	To Be Determined

Electrical Characteristics Over Operating Conditions DM75/DM85X432/433

Symbol	Parameter	Conditions		Guaranteed Limits Min	Guaranteed Limits Max	Units
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IH}	High-Level Input Voltage			2		V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.45V			−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16 mA for Q Outputs I_{OL} = 4 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs		0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2.6 mA for Q Outputs I_{OL} = −0.6 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs	2.4		V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max, V_O = 0V		−30	−80	mA
I_{OZH}	High Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OH} = 2.7V			20	μA
I_{OZL}	Low Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OL} = 0.4V			−20	μA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Low, Outputs Open			265	mA

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Operating Conditions (Note 3)

Symbol	Parameter	DM75X432/433 Min	DM75X432/433 Max	DM85X432/433 Min	DM85X432/433 Max	Units
V_{CC}	Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	−55	+125	0	+70	°C
t_{WWH}	WC Pulse Width High			10		ns
t_{WWL}	WC Pulse Width Low			15		ns
t_{SDW}	Input Data Setup			15		ns
t_{HDW}	Input Data Hold Time			0		ns
t_{WRH}	RC Pulse Width High			10		ns
t_{WRL}	RC Pulse Width Low			10		ns
t_{WM}	Master Reset Pulse Width					ns
t_{RMW}	Reset Recovery Time					ns

Note 2: Ambient Temperature.

Note 3: Since the FIFO is a very high speed device, care must be taken in the design of the hardware. Proper device grounding and supply decoupling are crucial to the correct operation of the FIFO.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Initial Conditions	DM75X432/433		DM85X432/433		Units
			Min	Max	Min	Max	
f_{WC}	Write Frequency					35	MHz
f_{RC}	Read Frequency					35	MHz
t_{PRQ}	RC to Data Output					20	ns
t_{PWF}	WC Rising to $\overline{F}$ Low	127 Words				15	ns
t_{PWE}	WC Rising to $\overline{E}$ High	Empty				15	ns
t_{PRE}	RC Rising to $\overline{E}$ Low	1 Word				15	ns
t_{PRF}	RC Rising to $\overline{F}$ High	Full				15	ns
t_{PWI}	WC Rising to FLAG High					20	ns
t_{PRI}	RC Rising to FLAG Low					20	ns
t_{SRW}	RC Rising Before WC	Full					ns
t_{SWR}	WC Rising Before RC	Empty					ns
t_{PDQ}	Transparent D to Q	Empty, WC = Low				30	ns
t_{PWQ}	WC Falling to Q	Empty				30	ns
t_{PMF}	MR to $\overline{F}$ High	Full				30	ns
t_{PME}	MR to $\overline{E}$ Low					30	ns
t_{PMI}	MR to FLAG Low					30	ns
t_{PZX}	Output Enable					20	ns
t_{PXZ}	Output Disable					20	ns

Pin Description

V_{CC} +5V supply.

D_0–$D_{3/4}$ 4/5-bit data input bus.

Q_0–$Q_{3/4}$ 4/5-bit data output bus (TRI-STATE non-inverted).

WC **Write Clock Input**—latches in a data word from D-bus on a low-to-high transition (except when FIFO is full). Data enters the memory while WC is low.

RC **Read Clock Input**—presents next data word onto Q-bus on a low-to-high transition (except when FIFO is empty).

$\overline{E}$ **Empty Status Output**—goes low when last word is read from FIFO (or when FIFO is reset); goes high when first word is written into an empty FIFO.

$\overline{F}$ **Full Status Output**—goes low when FIFO becomes full following a write; goes high when a read cycle creates a vacancy (or when FIFO is reset).

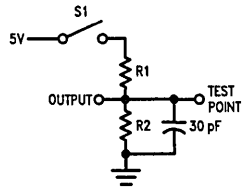
FLAG **Intermediate Status Flag Output**—high while FIFO is at least ¼ filled (32 or more words remaining in memory) if the FS input is low, or while FIFO is at least 3/4 filled (96 or more words) if FS is high; otherwise FLAG remains low.

FS **Flag Select Input**—selects FIFO word-count threshold for FLAG output (32 if low, 96 if high).

$\overline{MR}$ **Master Reset Input**—resets the FIFO to the empty state (internal pointers reset to zero) while low (level sensitive).

$\overline{OE}$ **Output Enable Input**—when low, enables output on the Q data bus; disables when high.

Standard Test Load



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I_{OL}	R1	R2
16 mA	300Ω	600Ω
4 mA	1100Ω	2200Ω

Input Pulse Amplitude = 3V

Input Rise and Fall Time (10%–90%) = 2.5 ns

t_{PHZ} measurement made at V_{OH} − 0.5V, t_{PLZ} measurement made at V_{OL} + 0.5V, all other measurements made at 1.5V.

Functional Description

The NFT FIFO is implemented using a 128 X 4/5-bit RAM with separate write and read ports. The write port is addressed by the write pointer and the read port by the read pointer. While the WC input is low, a data word on the D inputs is written into the write port of the RAM. The write pointer (initially zero) is incremented on the rising edge of WC, thus concluding a write cycle.

The RAM contents addressed by the read pointer (also initially zero) are presented on the Q outputs whenever the $\overline{OE}$ input is low (Q bus outputs are disabled when $\overline{OE}$ is high). Thus the first word may appear on the Q outputs as it is being written. The rising edge of RC increments the read pointer which then accesses the next data word from the RAM's read port. (Each pointer automatically wraps around from the last to the first RAM location.)

When the value of the read pointer becomes equal to the write pointer due to a read cycle, then the FIFO is empty, ie. any data words which had been written have also been read. When the value of the write pointer exceeds the read pointer by 128 due to a write cycle, then the FIFO is full, ie. the next RAM location into which data should be written contains the oldest word that has not yet been read.

The $\overline{E}$ and $\overline{F}$ status outputs indicate the empty and full conditions, respectively. Initially (following a reset) $\overline{F}$ is high. When WC is brought high at the end of any write cycle, $\overline{F}$ would go low if the FIFO becomes full; otherwise it remains high (without glitches). When the FIFO is full, $\overline{F}$ remains low until a vacant RAM location is made available resulting from a read operation (or the Master Reset is activated). $\overline{F}$ goes high after the rising edge of RC which creates the first vacancy.

Writing is inhibited while $\overline{F}$ is low. If WC is brought low while $\overline{F}$ was still low, new data would not begin to be written into the RAM until after a read cycle causes $\overline{F}$ to go high (WC must then remain low long enough to complete the write cycle). Any low-to-high transitions on WC while $\overline{F}$ is low are ignored (write pointer not incremented).

Initially (followinig a reset) the $\overline{E}$ output is low. $\overline{E}$ remains low while the FIFO is empty until the first write cycle is completed. $\overline{E}$ goes high after the rising edge of WC concluding the first write cycle. When RC is brought high at the end of any read cycle, $\overline{E}$ would go low if the FIFO becomes emtpy; otherwise it remains high (without glitches).

Reading is inhibited while $\overline{E}$ is low. Any low-to-high transitions on RC while $\overline{E}$ is low are ignored (read pointer not incremented). While the FIFO is empty, the Q outputs (if enabled) would either be in an indetermined state if WC is high, or would reflect D input data as it is written into the memory if WC is low.

The FIFO is reset to the empty state (write and read pointers reset to zero) while the $\overline{MR}$ input is low. WC and RC inputs are ignored and may be in either state during a reset. If WC is low following a reset, it should remain low long enough to complete the write cycle.

The FS input selects the waveform to appear on the FLAG output. When FS is low, then the FLAG output indicates when the FIFO is at least one quarter filled (i.e., when the write pointer value exceeds the read pointer by at least 32). When FS is high, then FLAG indicates when the FIFO is at least three quarters filled (write pointer exceeds read pointer by at least 96). The FLAG output remains stable (without glitches) except following the write or read cycle which changes the FIFO's status with respect to the selected threshold.

It is recommended that the FS input be changed only while the FIFO is empty or full. If FS is changed while the FIFO contains between 32 and 96 words, the FLAG output may not change to reflect the accurate status until a threshold is crossed.

FLAG Output Truth Table:

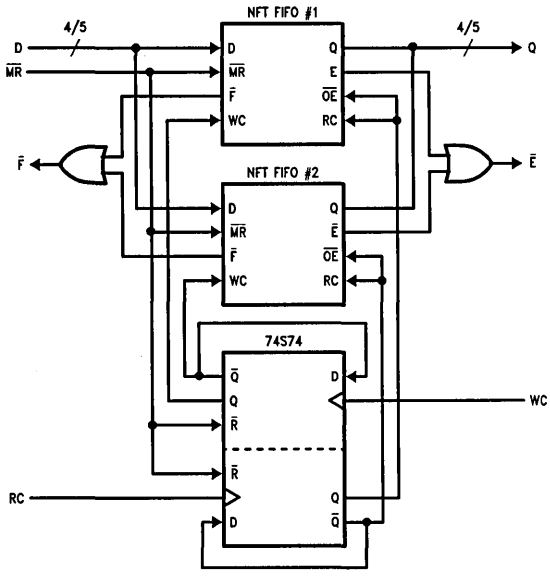
# Words Stored	FLAG Output	
	FS = L	FS = H
0–31	L	L
32–95	H	L
96–128	H	H

FIFO buffers wider than 4 or 5 bits can be implemented by connecting multiple chips in parallel. The $\overline{E}$, $\overline{F}$ and FLAG status information can be taken from any one of the chips since there is no fall-through delay which may otherwise cause output skew between chips.

FIFO buffers deeper than 128 words could also be implemented by connecting the D and Q lines of multiple devices in parallel and alternating the WC and RC clocks between each of the devices in turn (the $\overline{OE}$ input of each device must then be connected to its own RC input). For example, a 256 x 4/5 FIFO buffer could be implemented using two FIFO chips plus a dual D-type flip-flop (eg. 74S74) as shown in the diagram, "External Cascading". Cascading more than two devices (depth greater than 256) requires more sophisticated logic to generate the alternating WC and RC clocks; registered programmable logic devices may be useful for this. Note that when cascading in this manner, there are no additional delays introduced. Also, the threshold boundaries for the FLAG output are proportional to the number of devices cascaded.

Functional Description (Continued)

External Cascading (256 x 4/5 FIFO)



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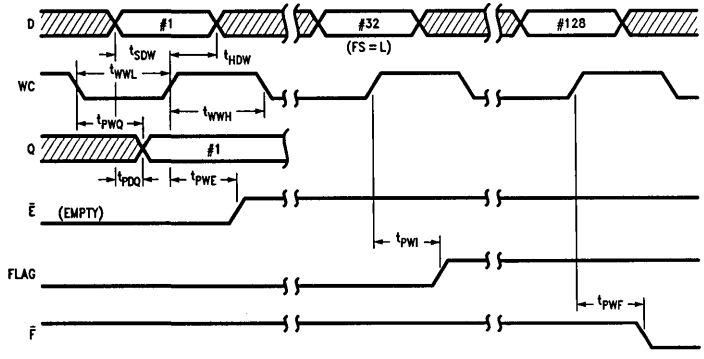
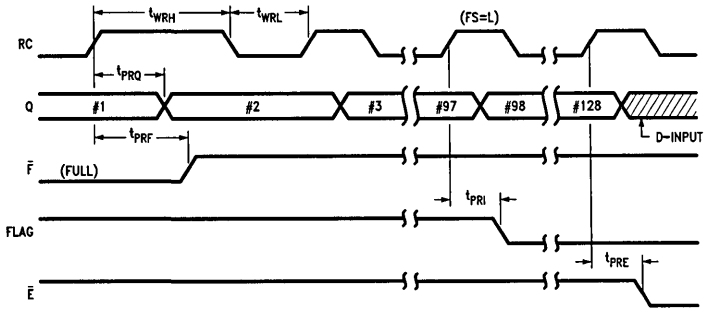
Write Cycle Timing



TL/D/9235–6

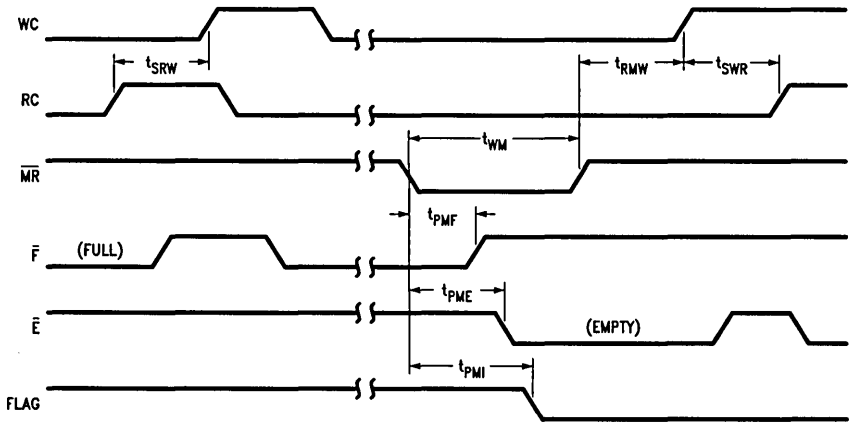
Read Cycle Timing



TL/D/9235–7

Functional Description (Continued)

Reset and Miscellaneous Timing



TL/D/9235–8

Section 7

Memory Modules

Section 7 Contents

National Semiconductor

ADVANCE INFORMATION

NM1002109/NM2109
256k x 9-Bit Static RAM Module

General Description

The NM1002109/NM2109 is a hermetic, low profile 2.25 Mbit fully static asynchronous random access ECL memory module organized as 262,144 words by 9 bits. The module is based on National's advanced one micron BiCMOS III process thus bringing high density CMOS to performance driven ECL designs. The module consists of nine hermetically packaged 256 k-bit ECL SRAMs and associated decoupling chip capacitors surface mounted on a 72-pin multilayer substrate specifically designed for minimum signal skews, cross-talk, and propagation delays. Configured in either SIMM (leadless) for applications requiring socketing for simplified field expansion/replacement or ZIP (leaded) for direct through hole mounting, the NM1002109/NM2109 combines state of the art performance and memory density to satisfy the memory intensive applications of tomorrow.

The address and control busses for the NM1002109/NM2109 are designed to provide connections at each end of the module (as in A0/A0') to facilitate signal termination on the motherboard and shorten/simplify signal routing in the user's system. This bus configuration also provides the capability to daisy chain more than one module together by serially routing the bus signals to the next module.

Reading the memory is accomplished by taking the select ($\overline{S}$ or $\overline{S}'$) pin LOW while the write enable ($\overline{W}$ or $\overline{W}'$) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q). The output pins will remain inactive (LOW) if either the select ($\overline{S}$ or $\overline{S}'$) pin is HIGH or the write enable ($\overline{W}$ or $\overline{W}'$) pin is LOW.

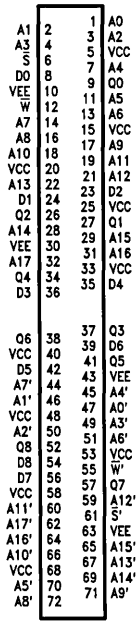
Writing to the module is accomplished by having the select ($\overline{S}$ or $\overline{S}'$) and the write enable ($\overline{W}$ or $\overline{W}'$) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A17 or A0'–A17').

Features

- 256k x 9 high performance fully asynchronous SRAM module
- Fast TAA, TWC over the commercial temperature range (17 ns and 20 ns speed grades)
- Dual address & control pins for daisy chaining or signal termination
- Access speeds maintained when address and control signals are propagated from either end of the module
- Temperature compensated F100K ECL I/O
- Low noise, controlled impedance (50Ω) substrate
- Multiple power/ground connections interspersed between signal pins, and on-board decoupling for each device, for improved noise immunity and signal clarity
- Separate internal power/ground planes for low-inductance power connections
- Hermetic high-rel device packaging
- Available in SIMM (socket compatible) or ZIP-leaded versions
- Ideal for high speed EDP; super & mini-super computer applications
- Low mounting profile for closer board to board spacing
- NM1002109
  Power supply: −4.2V to −4.8V operation
  Power dissipation: less than 8.7W
- NM2109
  Power supply: −5.2V ±5% operation
  Power dissipation: less than 10W

Connection Diagram

**72-Pin ZIP*
72-Pin SIMM***



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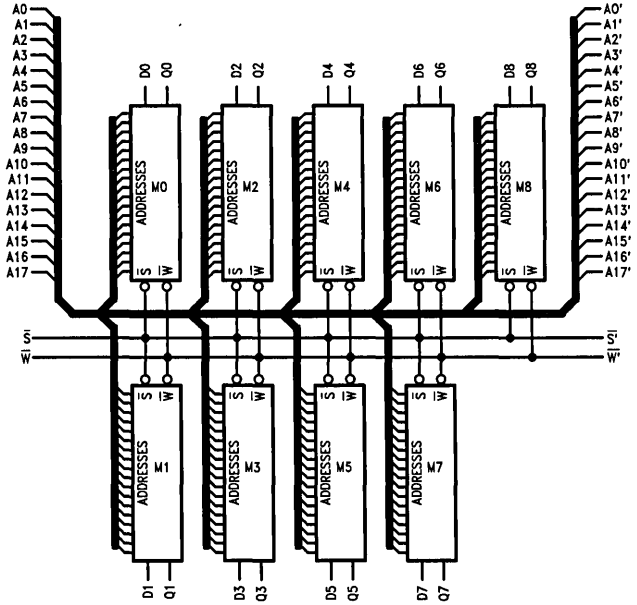
Top View

*For most current package information, contact product marketing.

Functional Block Diagram



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Absolute Maximum Ratings

Above which useful life may be impaired

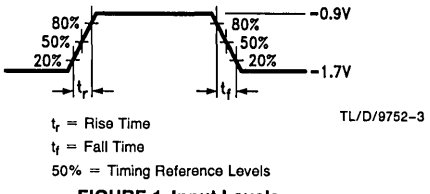
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall Times	0.7 ns
Output Timing Referrence Levels	50% of Input
AC Test Circuit	*Figure 2*

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.



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t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels

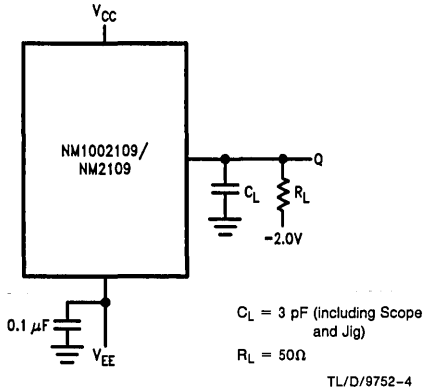

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FIGURE 2. AC Test Circuit

DC Electrical Characteristics

NM1002109: V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C
NM2109: V_{EE} = −5.2V ±5%, V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(Max)}$ or $V_{IH(Max)}$, Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{OHC}	Output HIGH Voltage	V_{IN} = $V_{IH(Min)}$ or $V_{IH(Min)}$, Loading with 50Ω to −2.0V	−1025		mV
V_{OLC}	Output LOW Voltage			−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = $V_{IH(Max)}$		2.0	mA
I_{IL}	Input LOW Current	V_{IN} = $V_{IL(Min)}$	−0.450	1.550	mA
I_{EE}	Power Supply Current	f_0 = 50 MHz	−1.800		A

All voltages are referenced to V_{CC} pin = 0V.

Capacitance

Symbol	Parameter	Max	Units
C_{INA}	Address Input Pins	TBD	pF
C_{INW}	Write Enable Pins	TBD	pF
C_{INS}	Select Pins	TBD	pF
C_{IND}	Data Input Pins	TBD	pF
C_{OUT}	Data Output Pins	TBD	pF

Truth Table

$\overline{S}$	$\overline{W}$	D_X	Q_X	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

7

Read Cycles

AC Timing Characteristics*

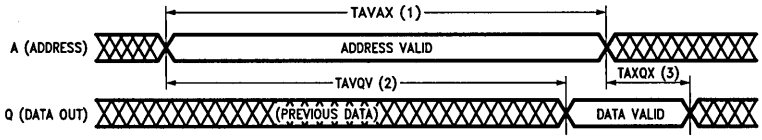
NM1002109: V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C
NM2109: V_{EE} = −5.2V ±5%, V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	NM1002109-17 NM2109-17		NM1002109-20 NM2109-20		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	17		20		ns
2	TAVQV	TAA	Address Valid to Output Valid		17		20	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		ns
4	TSLSH	TRC	Select LOW to Select HIGH	7		7		ns
5	TSLQV	TACS	Select LOW to Output Valid		7		7	ns
6	TSHQL	TRCS	Select HIGH to Output LOW		6		6	ns

*All timings measured to 50% levels.

Read Cycle 1

Where $\overline{S}$ is active prior to or within TAVQV−TSLQV after address valid.



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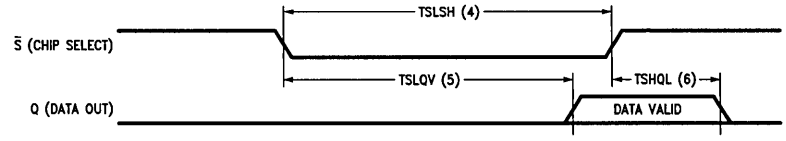
Read Cycle 2

Where address is valid a minimum of TAVQV−TSLQV prior to $\overline{S}$ becoming active.



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Write Cycle 1

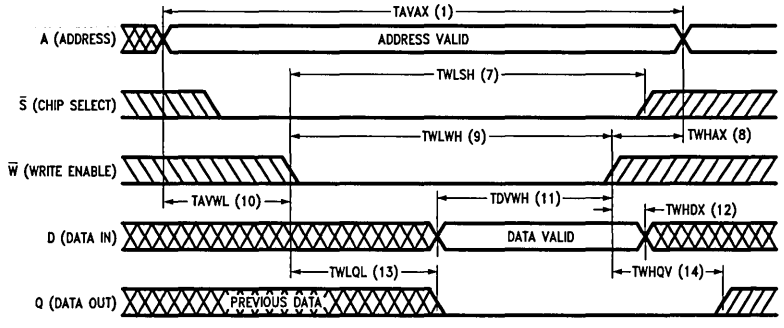
This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics*

NM1002109: V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C
NM2109: V_{EE} = −5.2V ±5%, V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	NM1002109-17 NM2109-17		NM1002109-20 NM2109-20		Units
	Std.	Alt.		Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	17		20		ns
7	TWLSH		Write Enable LOW to Select HIGH	10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		2		ns
11	TDVWH		Data Valid to Write HIGH	10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	2		5		ns
13	TWLQL	TWS	Write LOW to Output LOW		7		7	ns
14	TWHQV	TWR	Write HIGH to Output Valid		17		20	ns

*All timings measured to 50% levels.



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Write Cycle 2

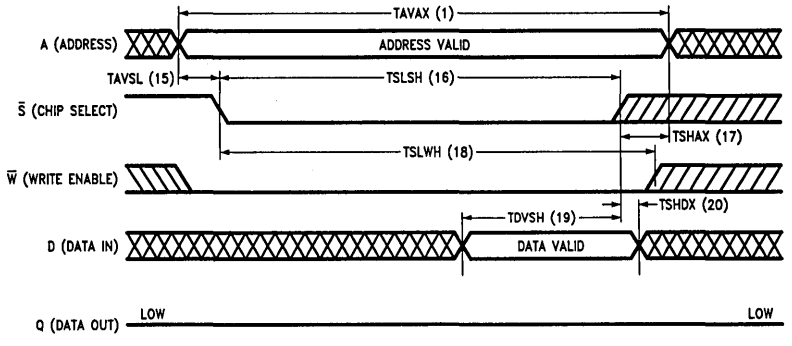
This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has identical specifications to write cycle I with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics*

NM1002109: V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C
NM2109: V_{EE} = −5.2V ±5%, V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	NM1002109-17 NM2109-17		NM1002109-20 NM2109-20		Units
	Std.	Alt.		Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Select LOW	0		2		ns
16	TSLSH		Select LOW to Select HIGH	10		12		ns
17	TSHAX	TWHA	Select HIGH to Address Don't Care	0		3		ns
18	TSLWH		Select LOW to Write Enable HIGH	10		12		ns
19	TDVSH		Data Valid to Select HIGH	10		14		ns
20	TSHDX	TWHD	Select HIGH to Data Don't Care	2		5		ns

*All timings measured to 50% levels.



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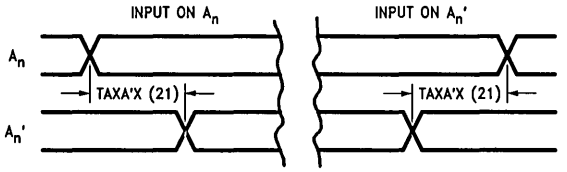
Propagation Delays

AC Timing Characteristics: NM1002109: V_{EE} = −4.2V to −4.8V, V_{CC} = Ground, T_C = 0°C to +85°C
NM2109: V_{EE} = −5.2V ±5%, T_C = 0°C to +85°C, V_{CC} = Ground

No.	Symbol		Parameter	NM1002109-17		NM1002109-20		Units
	Std.	Alt.		Min	Max	Min	Max	
21	TAXAX	TPDA	Propagation Delay (Address Bus)		2		2	ns
22	TWXWX	TPDW	Propagation Delay ($\overline{\text{Write Enable}}$)		2		2	ns
23	TSXSX	TPDS	Propagation Delay ($\overline{\text{Select}}$)		2		2	ns

Address Bus Delays



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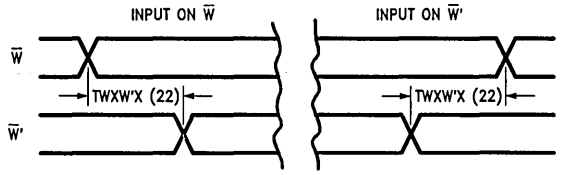
$\overline{\text{WRITE}}$ Line Delays



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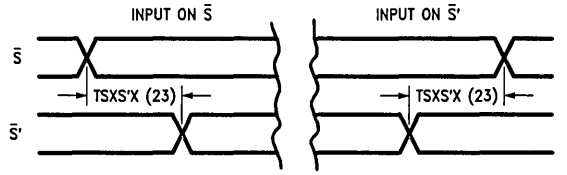
$\overline{\text{SELECT}}$ Line Delays



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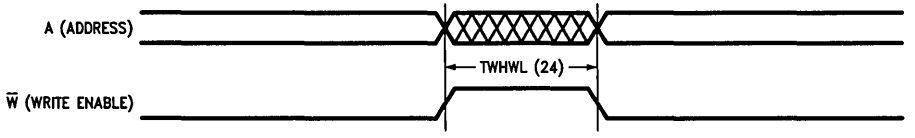
AC Timing Characteristics: Consecutive Write Cycles.

NM1002109: T_C = 0°C to +85°C, V_{EE} = −4.2V to − 4.8V, V_{CC} = Ground
NM2109: V_{EE} = −5.2V ±5%, T_C = 0°C to +85°C, V_{CC} = Ground

No.	Symbol		Parameter	NM1002109-17 NM2109-17		NM1002109-20 NM2109-20		Units
	Std.	Alt.		Min	Max	Min	Max	
24	TWHWL	$\overline{TWP}$	Write Enable HIGH to Write Enable LOW	5		5		ns
25	TSHSL	$\overline{TSP}$	Select HIGH to Select LOW	5		5		ns

Consecutive Write Cycles

Minimum Write Pulse Disable



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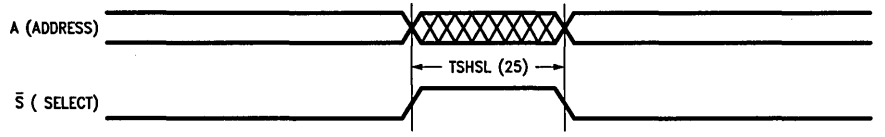
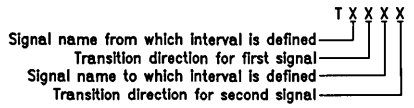
Minimum Select Pulse Disable



TL/D/9752-9

Standard Timing Parameter Abbreviations



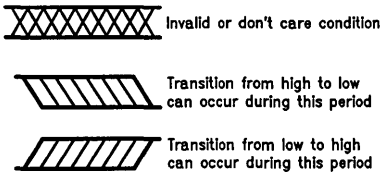
TL/D/9752-10

The transition definitions used in this data sheet are:

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

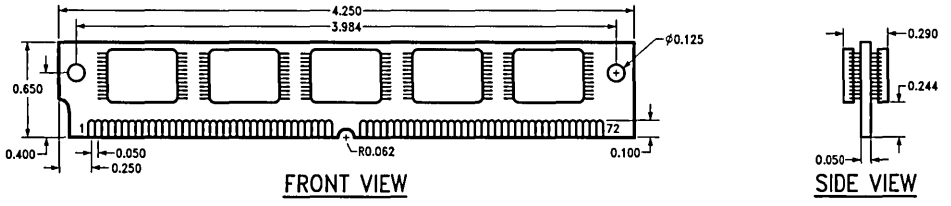
TIMING EXPLANATIONS

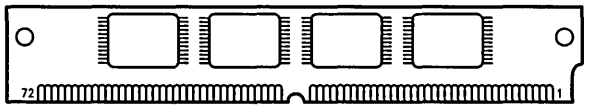
The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.



TL/D/9752-11

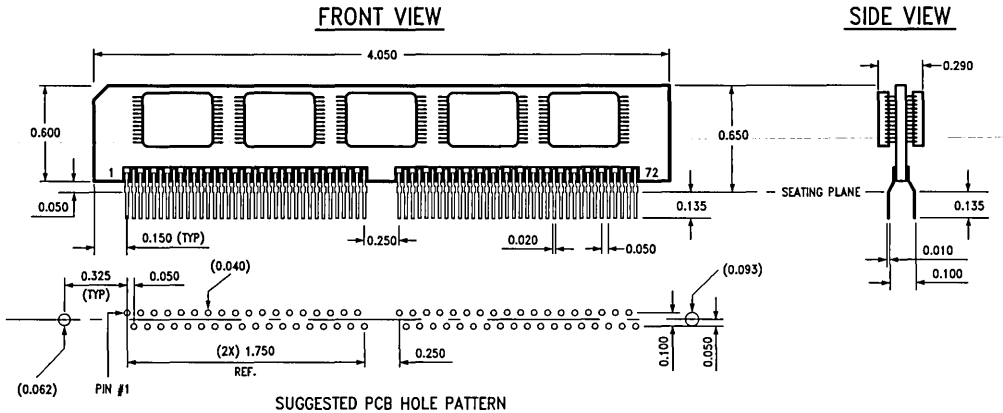
Physical Dimensions inches (millimeters)





TL/D/9752-12

NM1002109/NM2109 Package Dimensions (72-Pin SIMM Version)*



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NM1002109/NM2109 Package Dimensions (72-Pin ZIP Version)*

*For most current package information, contact product marketing.

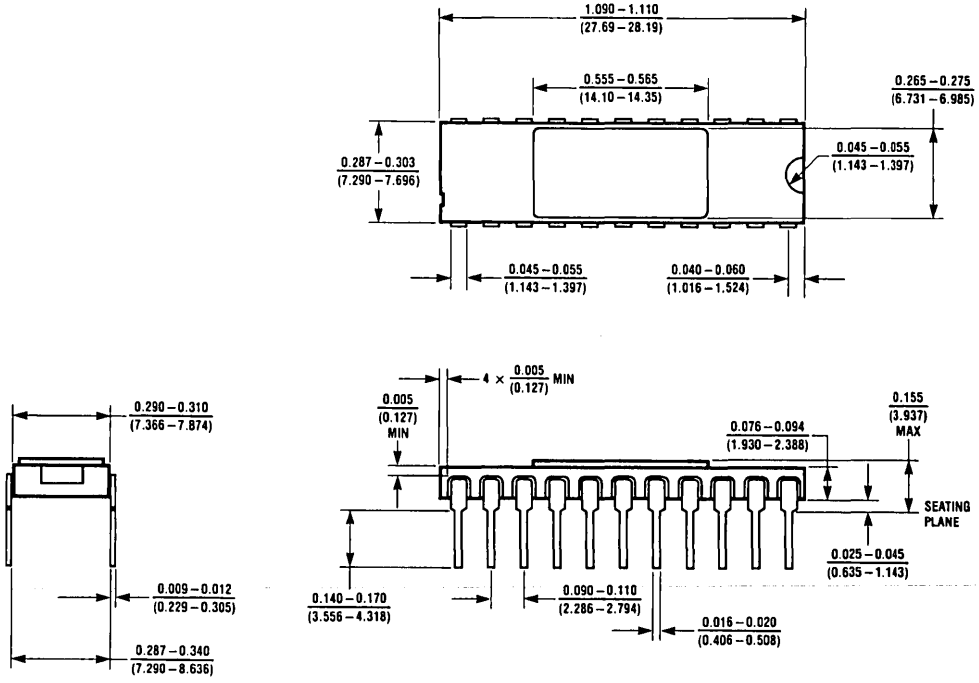
Section 8

Physical Dimensions

Section 8 Contents

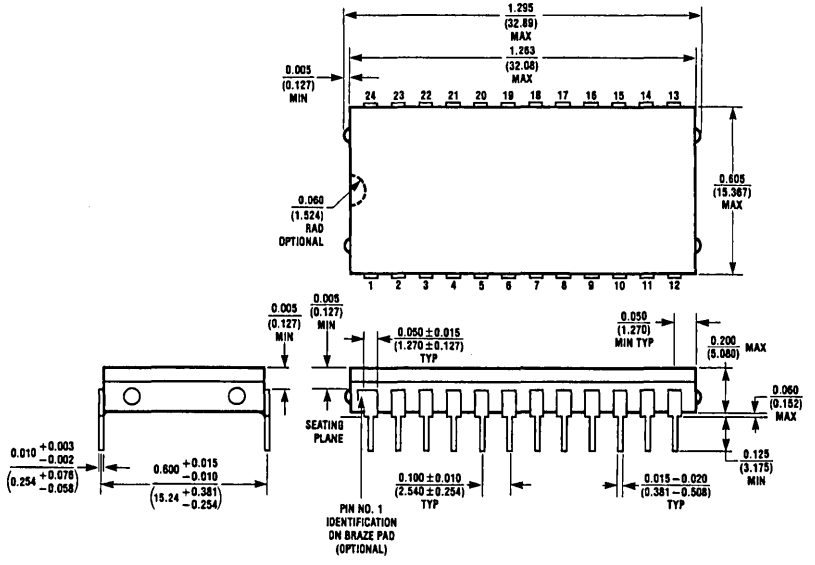
National Semiconductor

All dimensions are in inches (millimeters)



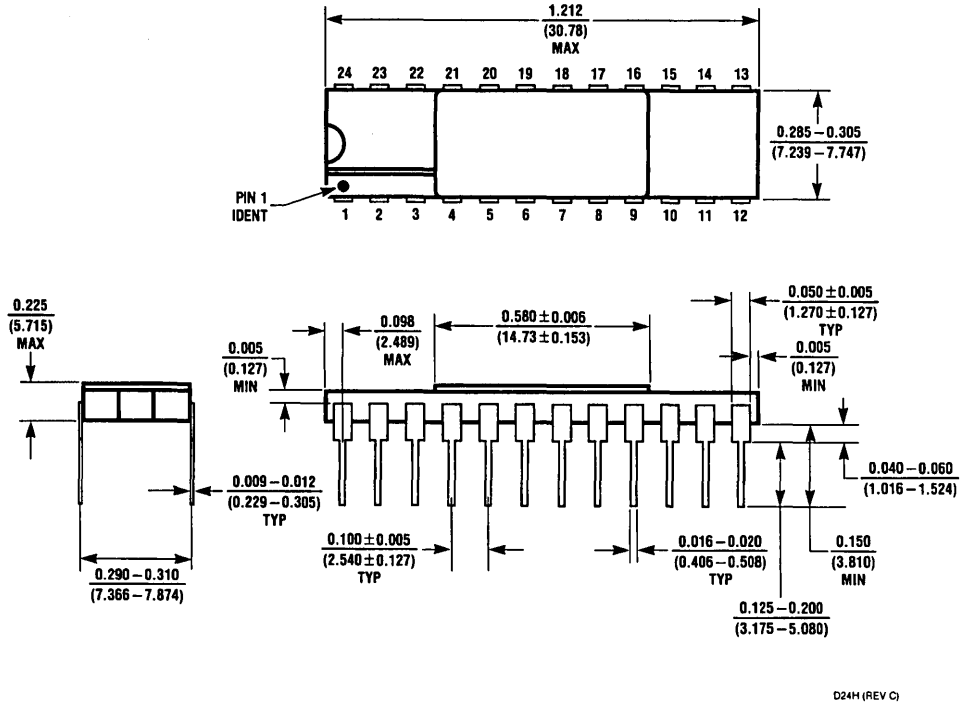
D22D (REV D)

NS Package D22D

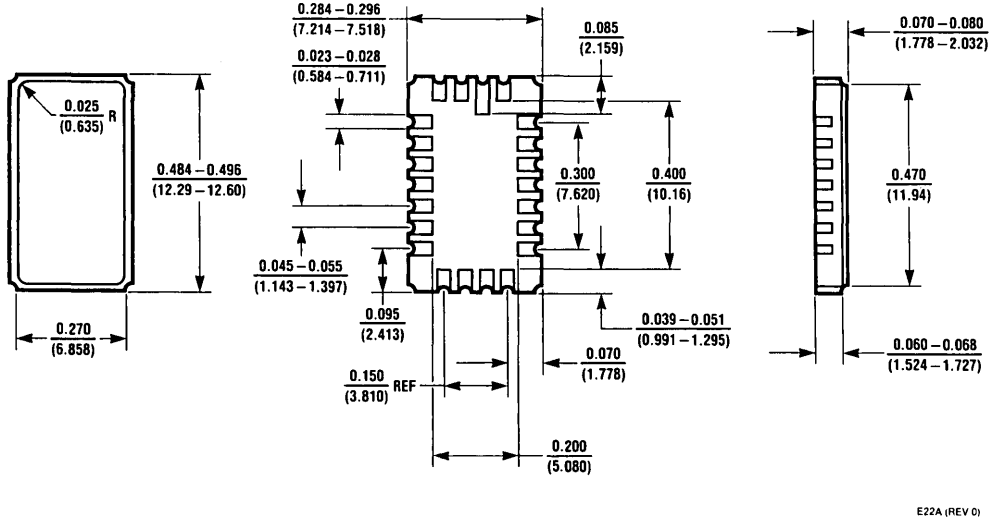


D24D (REV E)

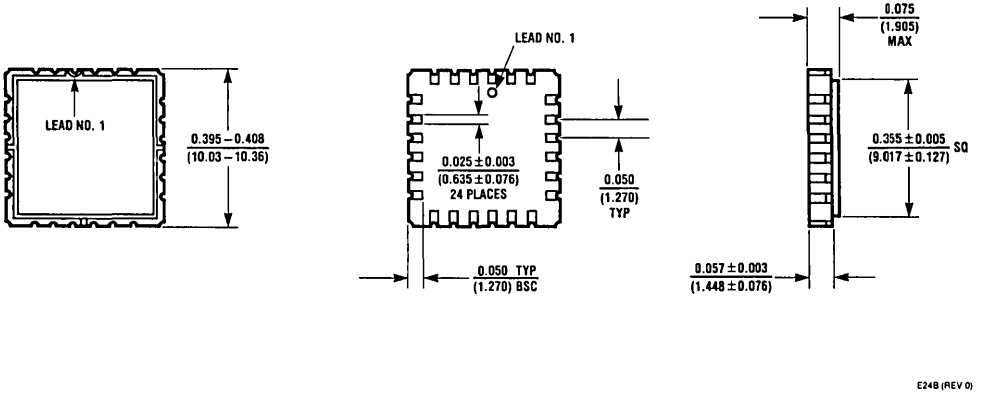
NS Package D24D



NS Package D24H

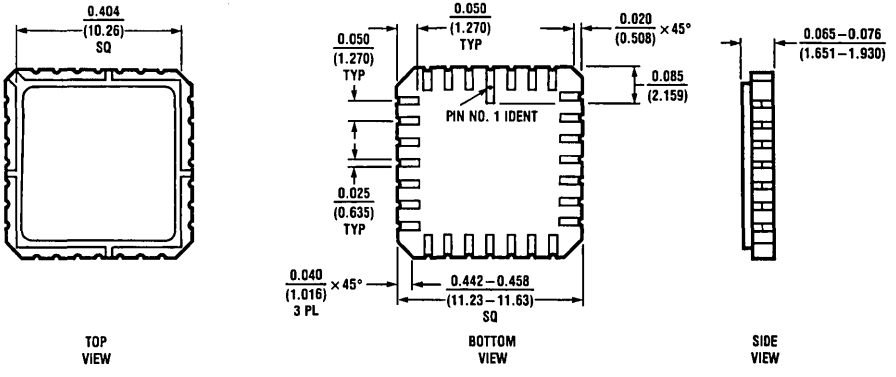


NS Package E22A



E24B (REV 0)

NS Package E24B



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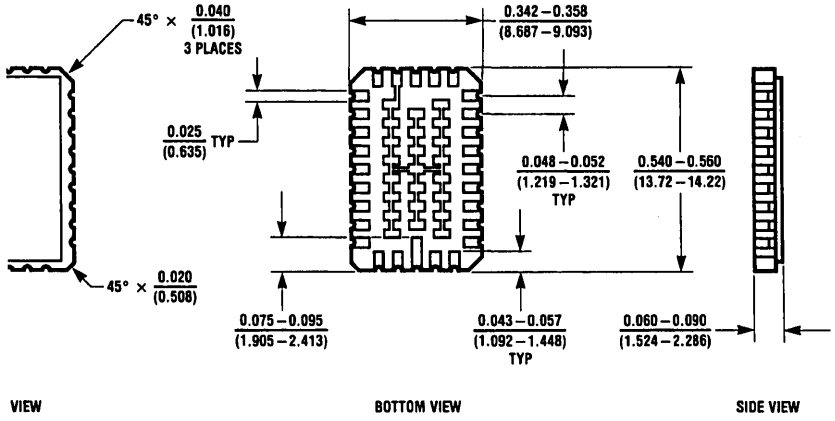

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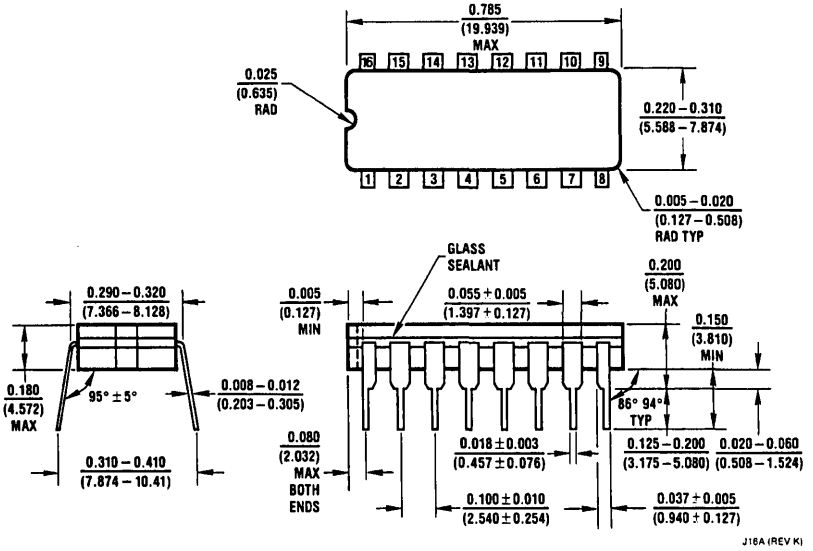

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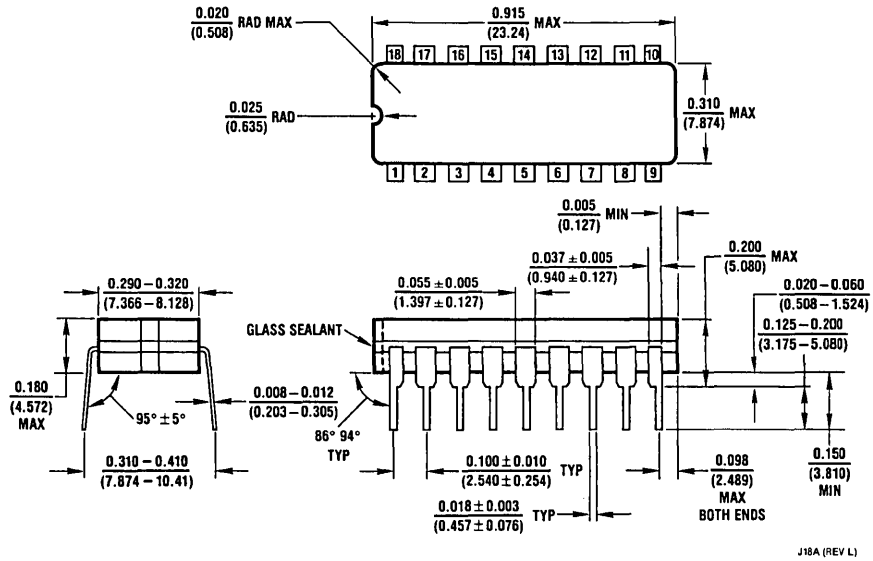

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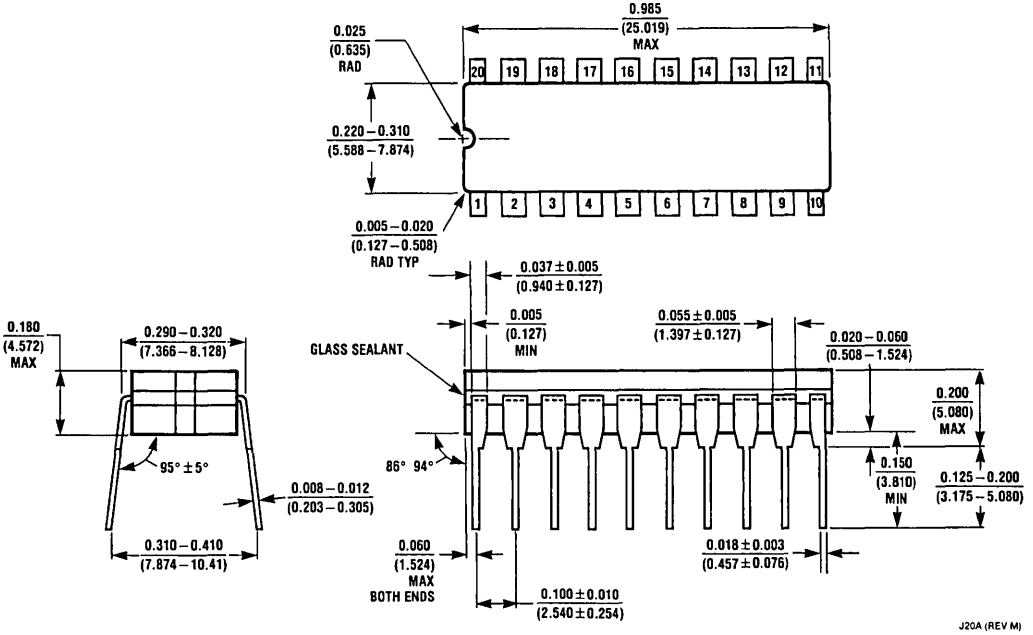

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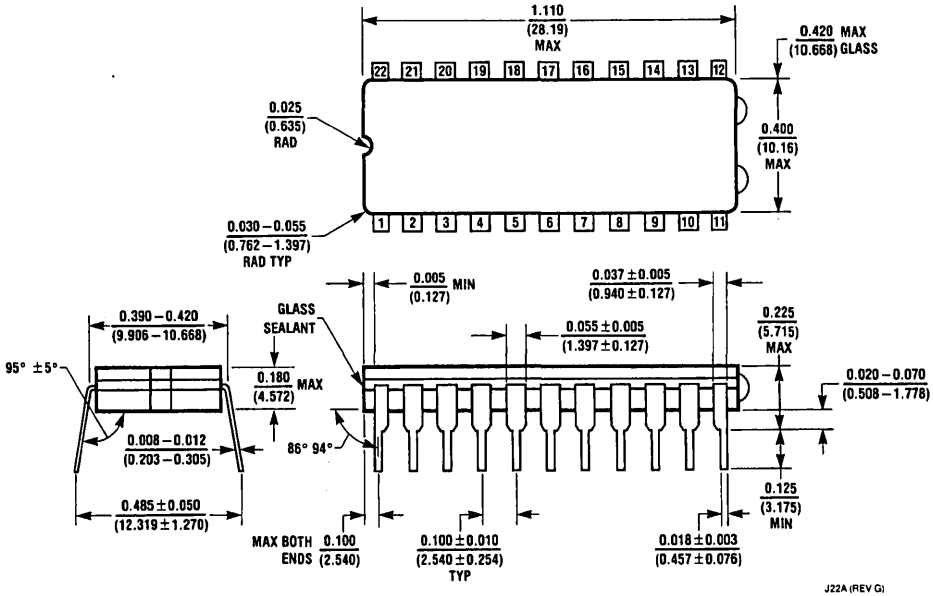

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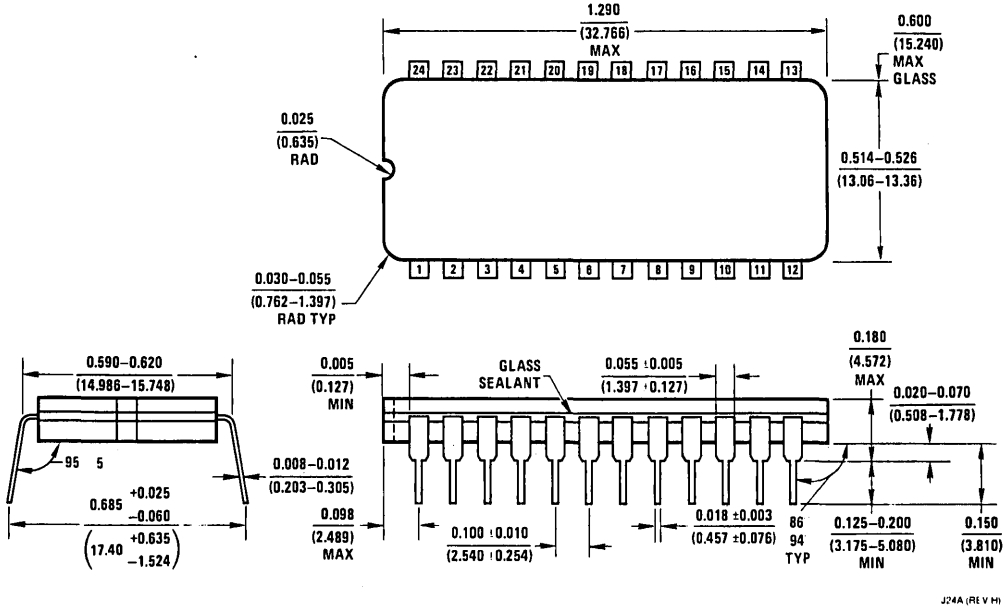

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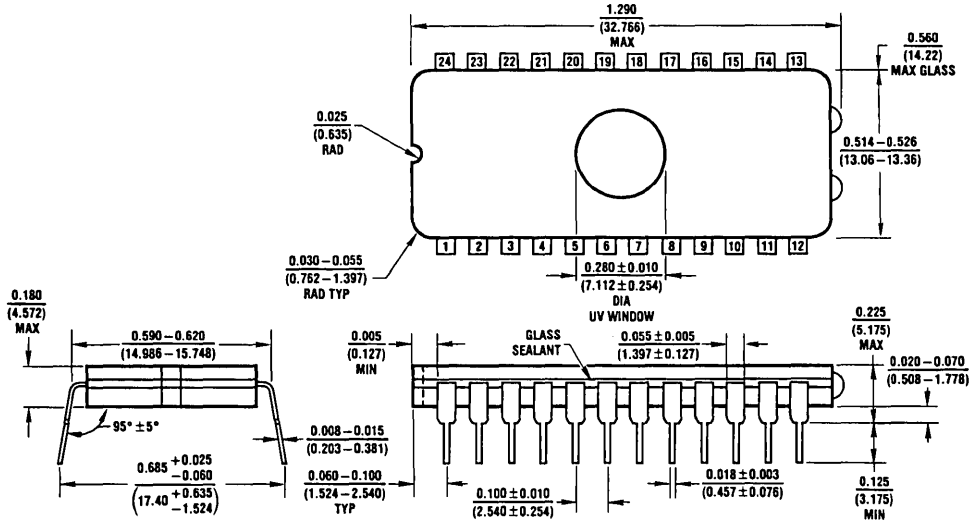

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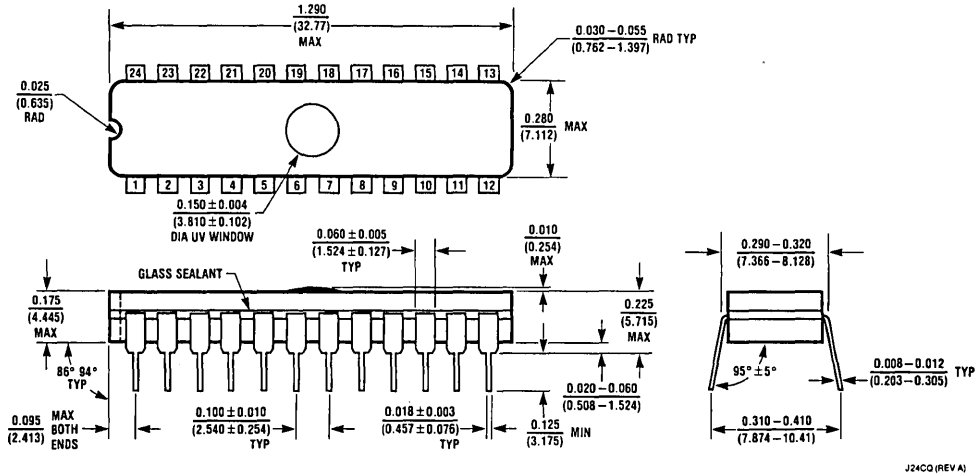

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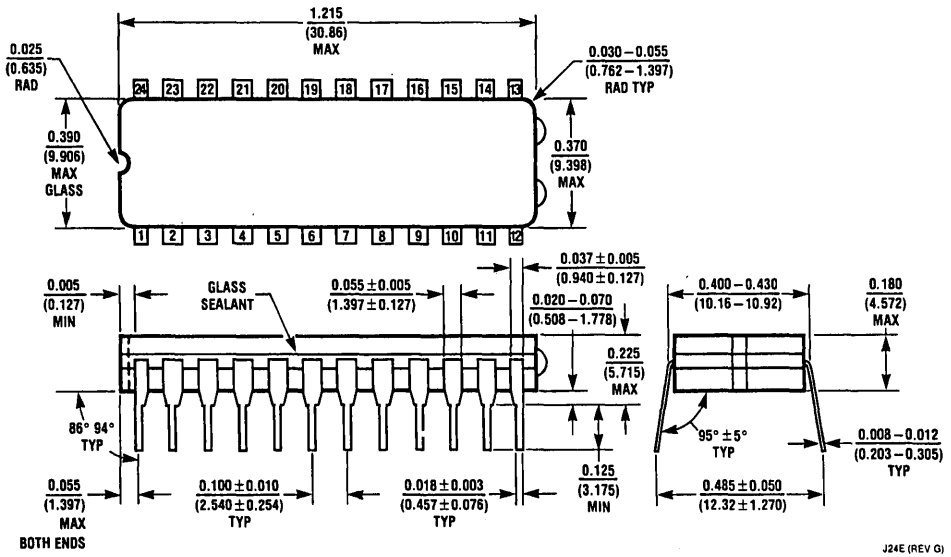

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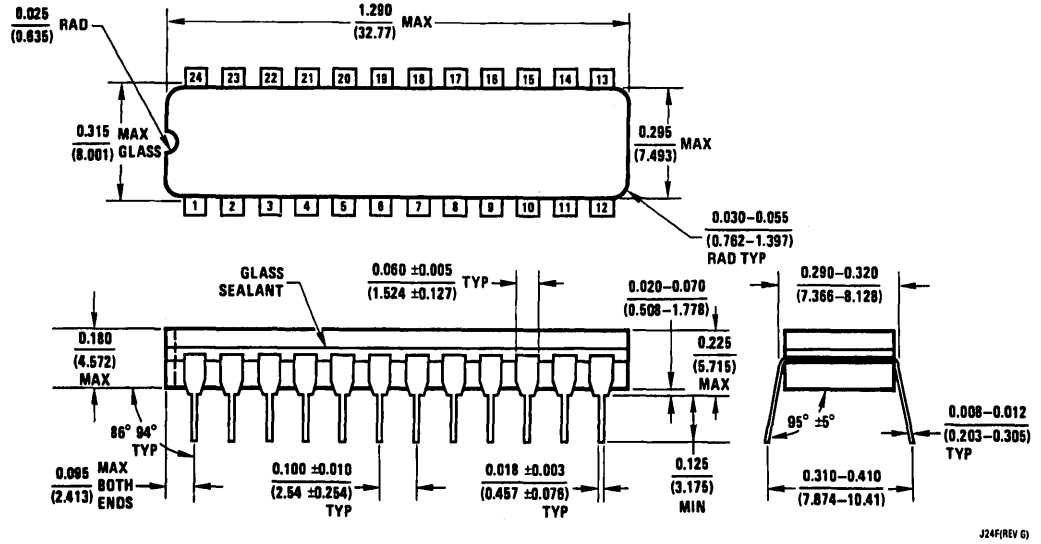

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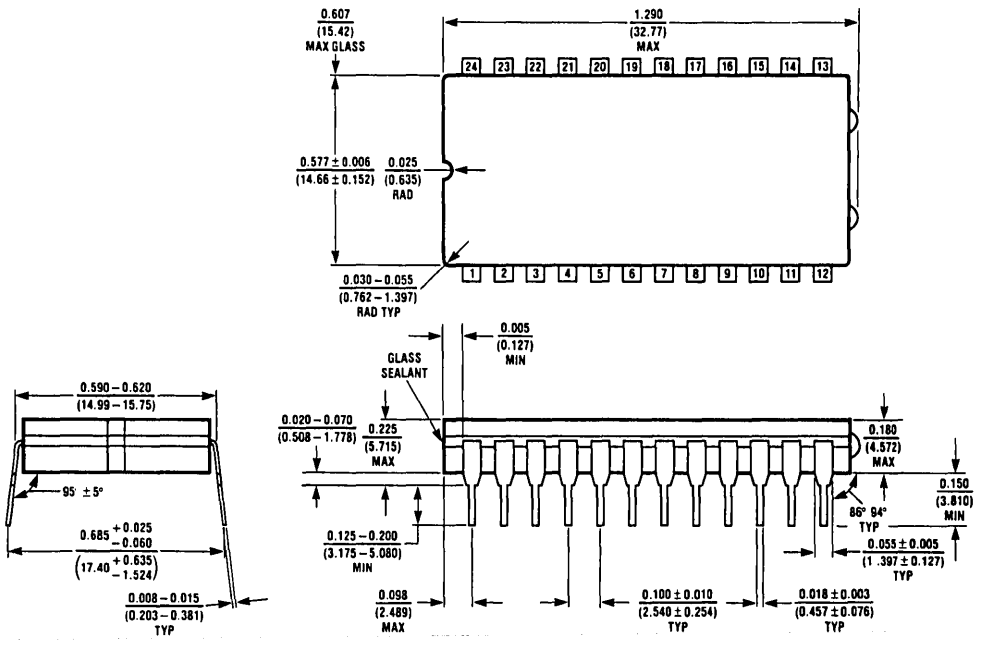

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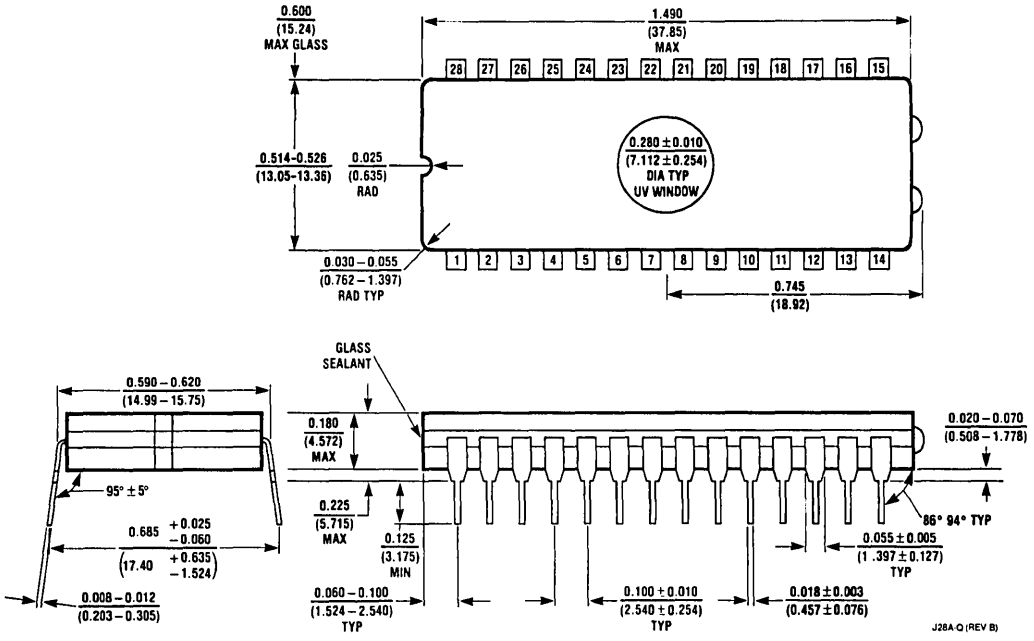

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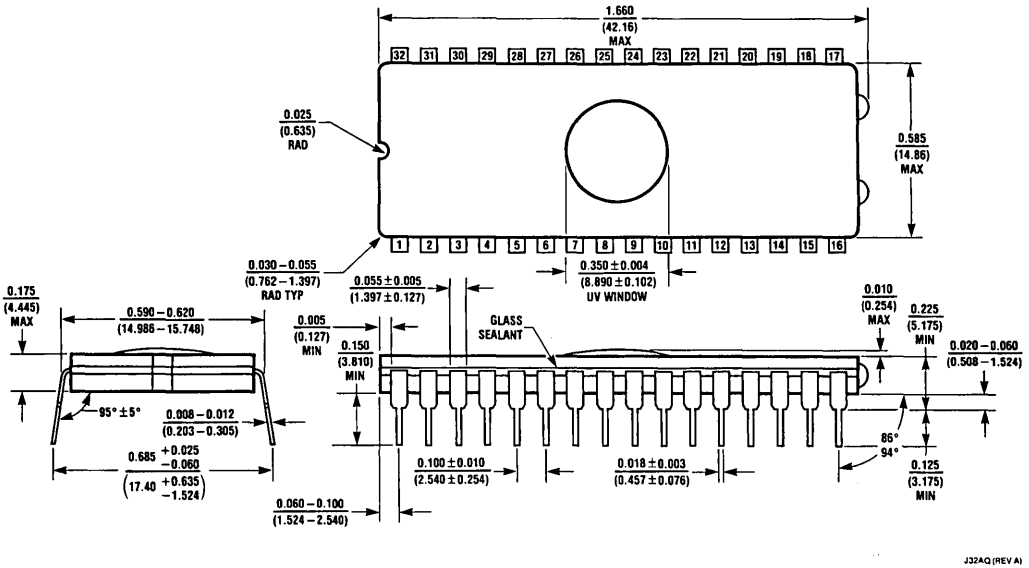

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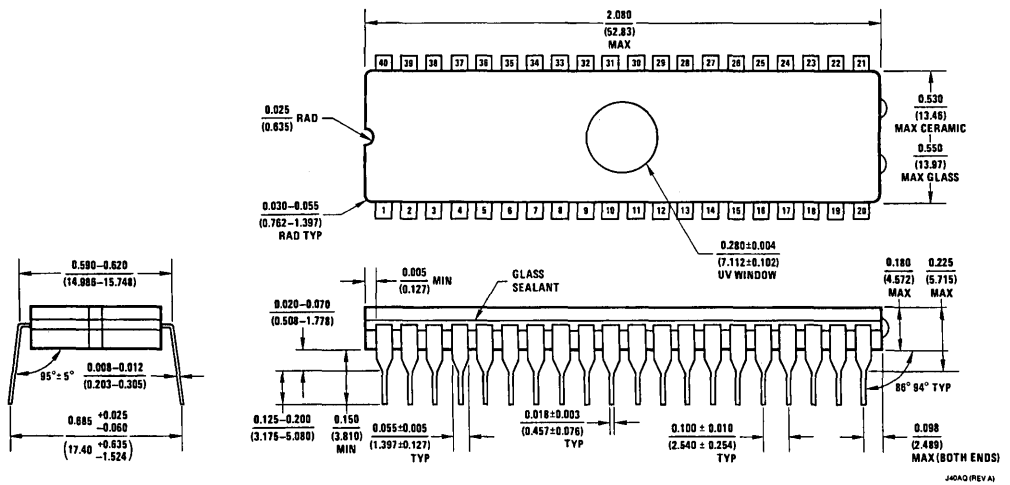

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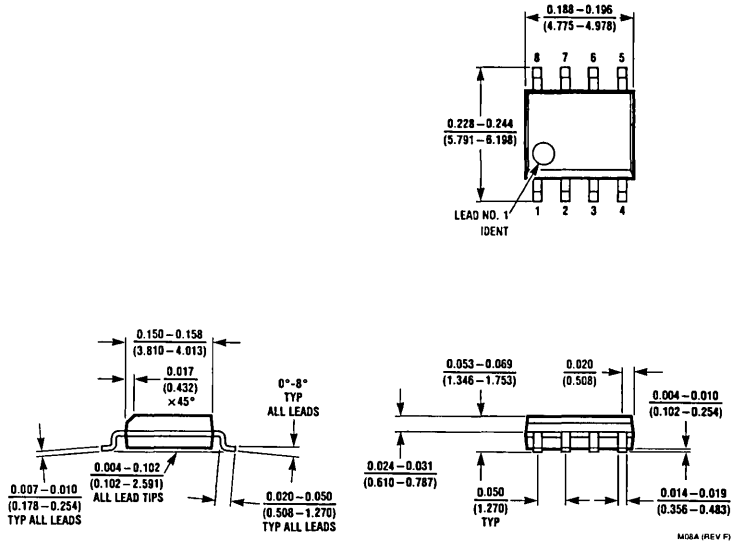

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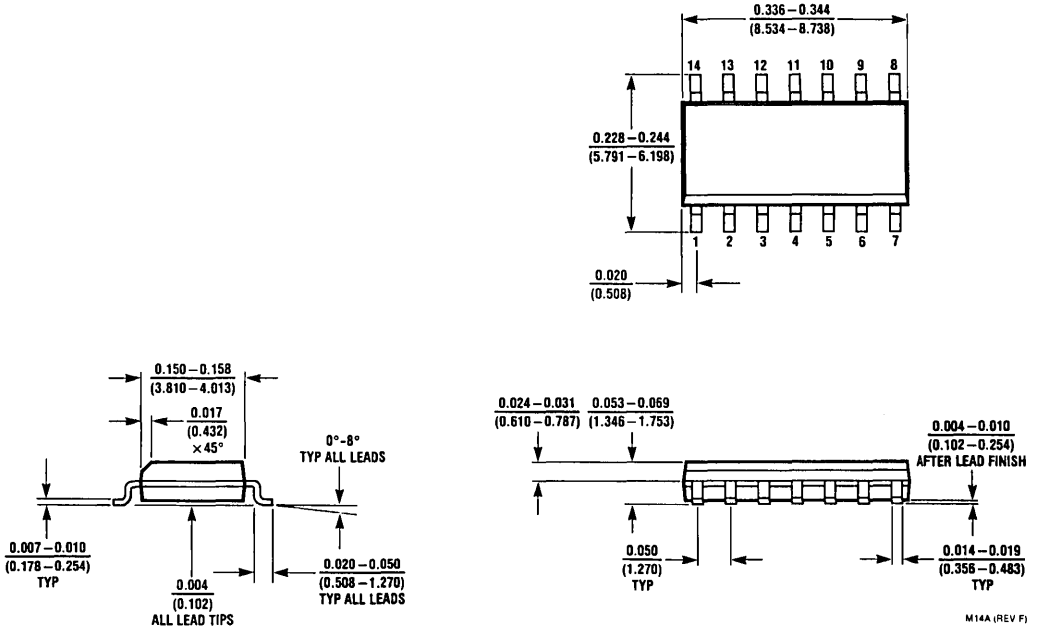

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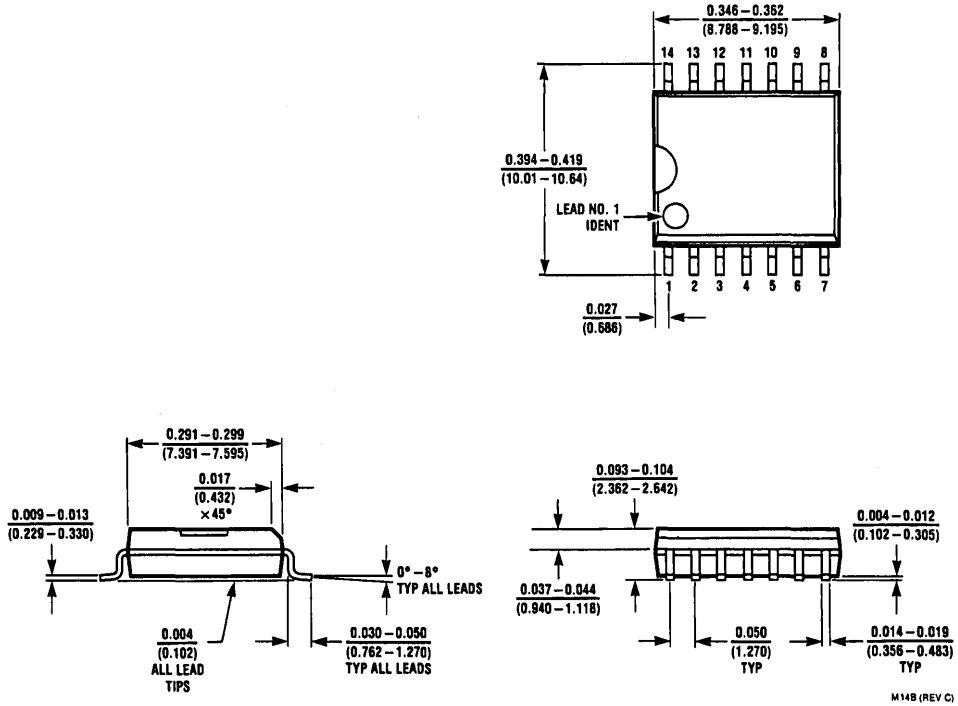

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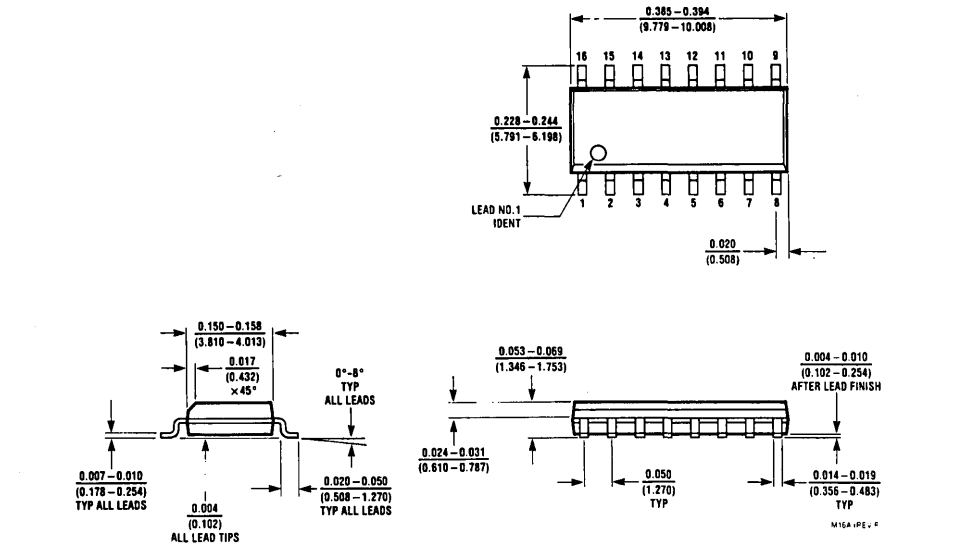

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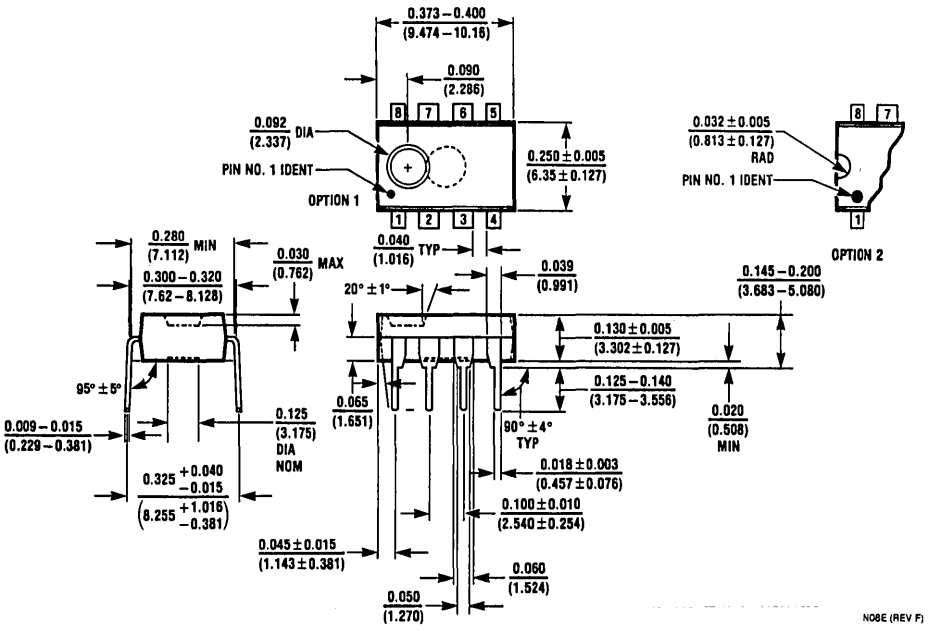

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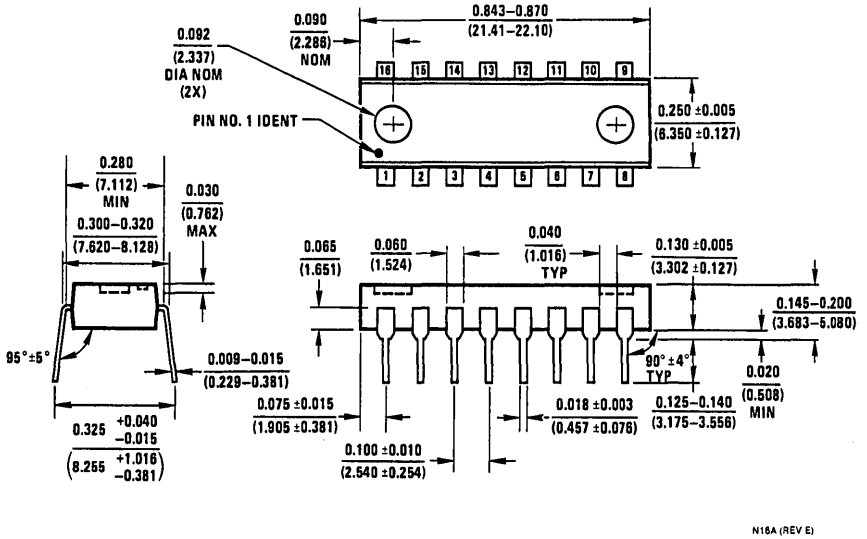

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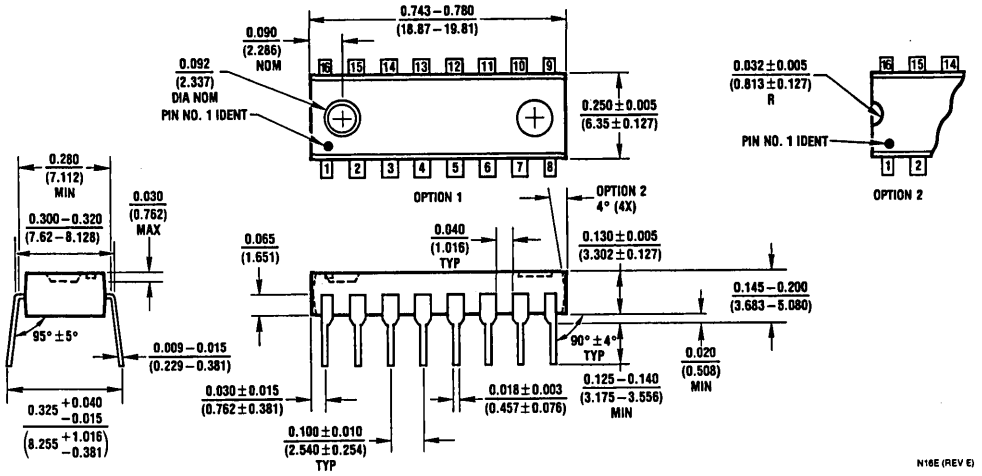

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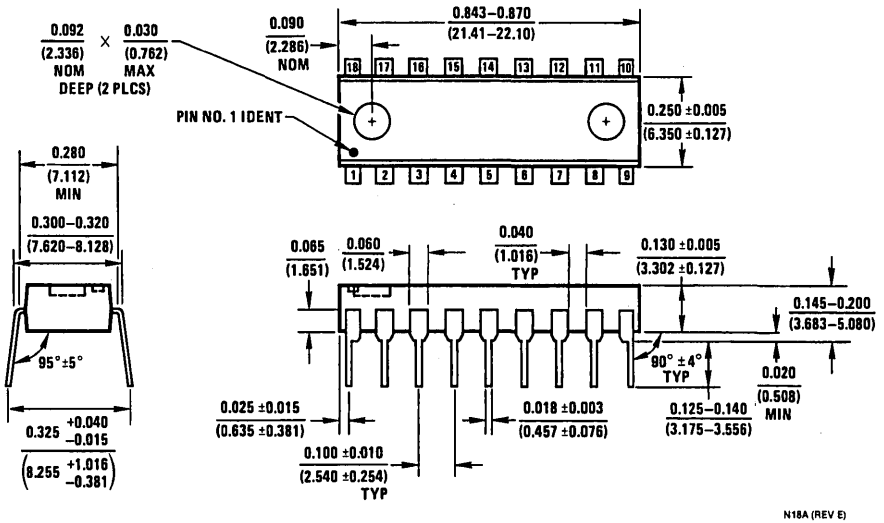

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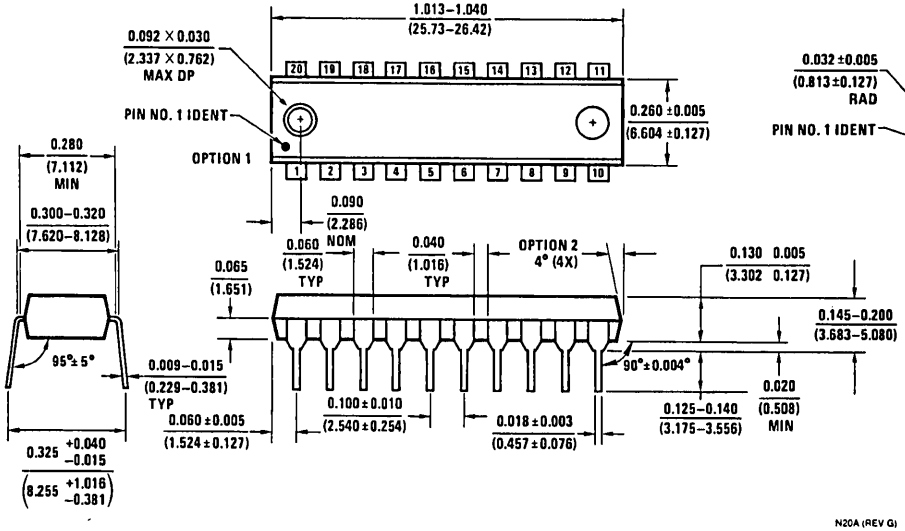

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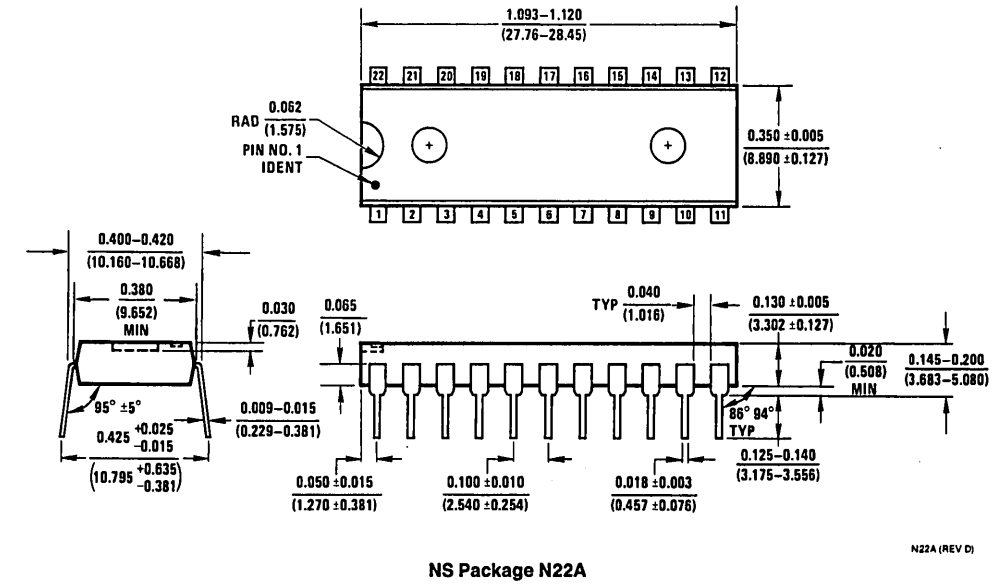

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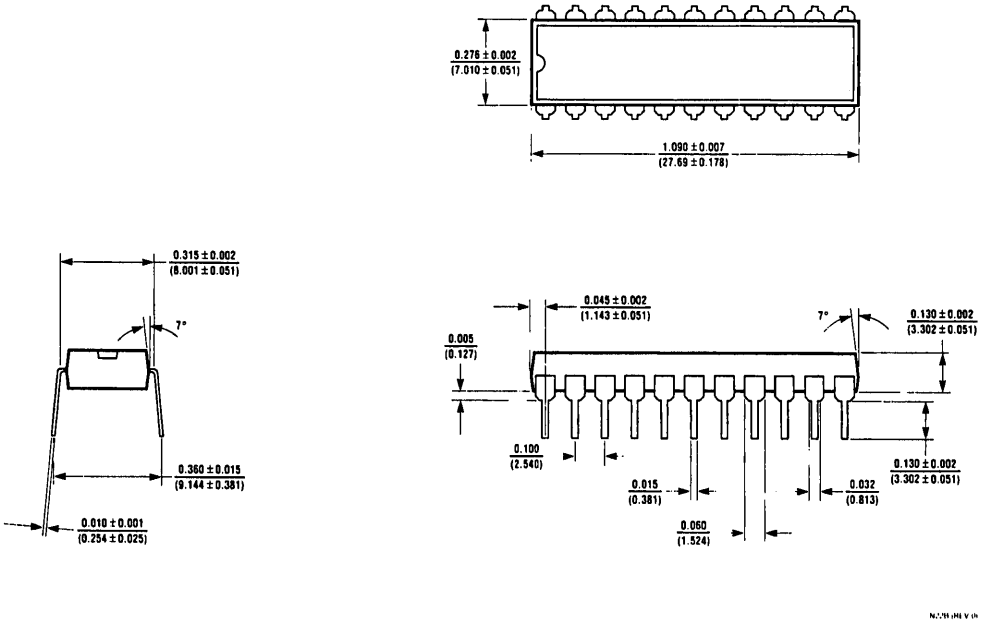

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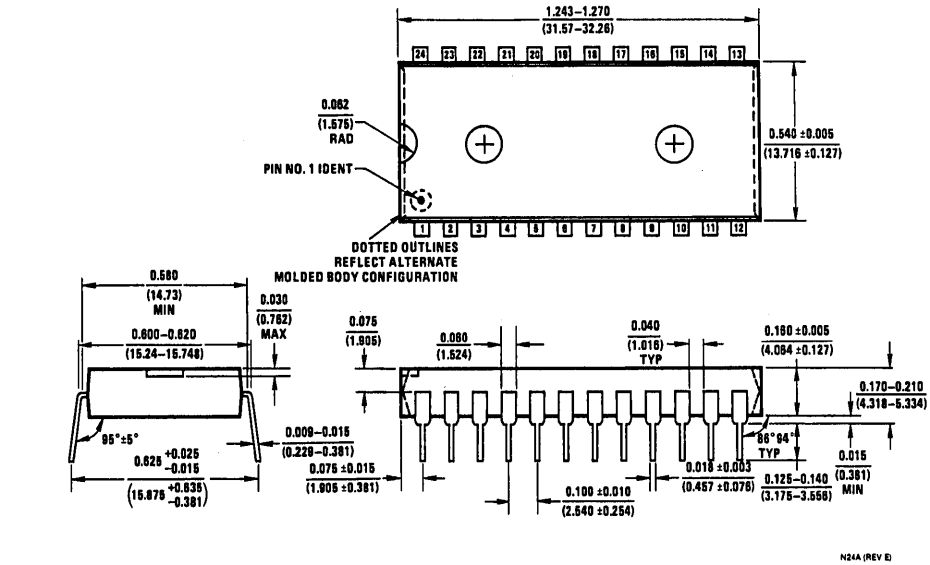

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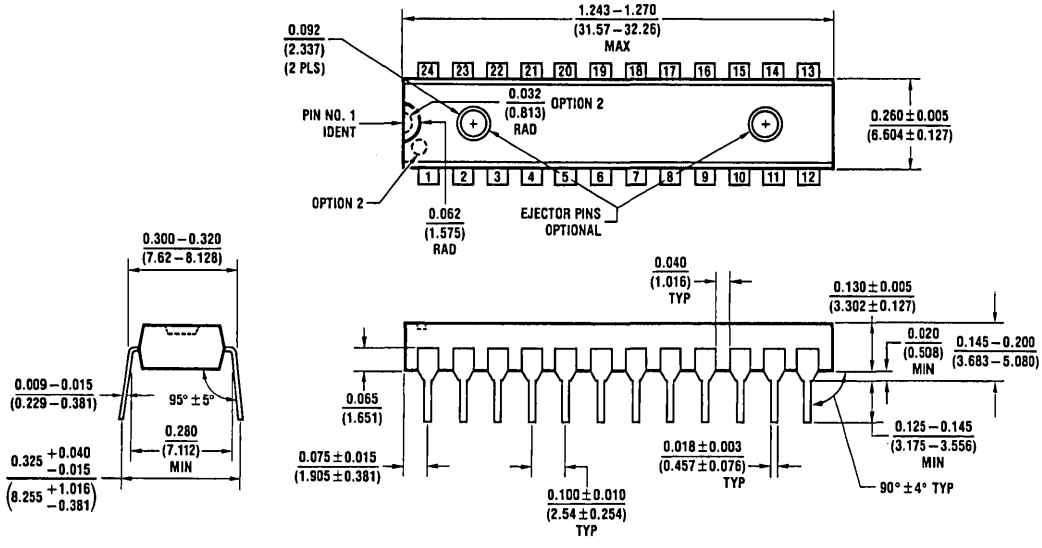

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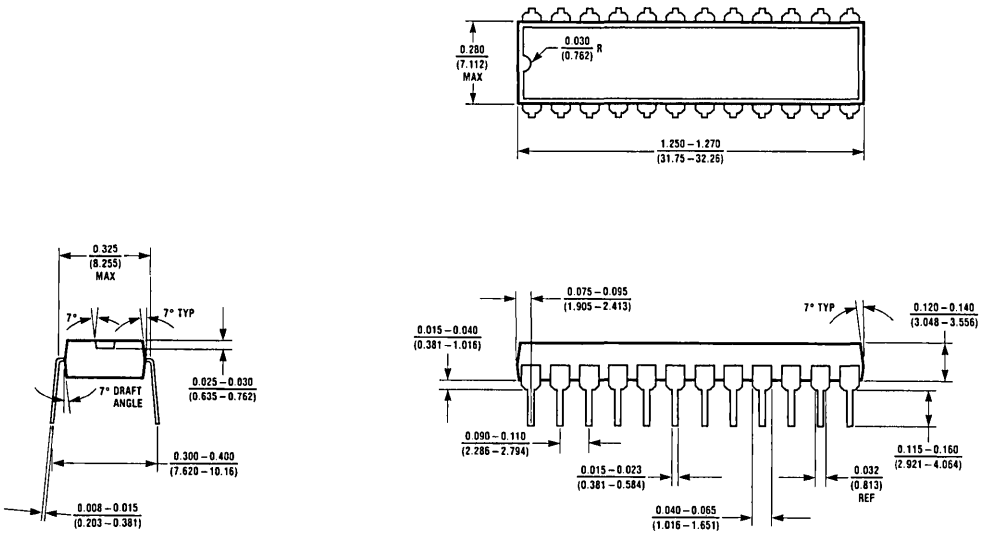

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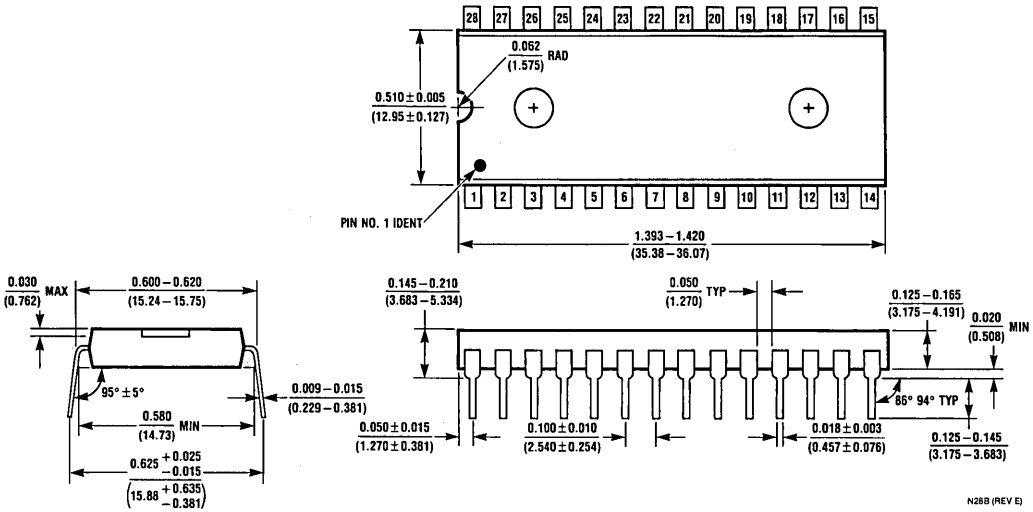

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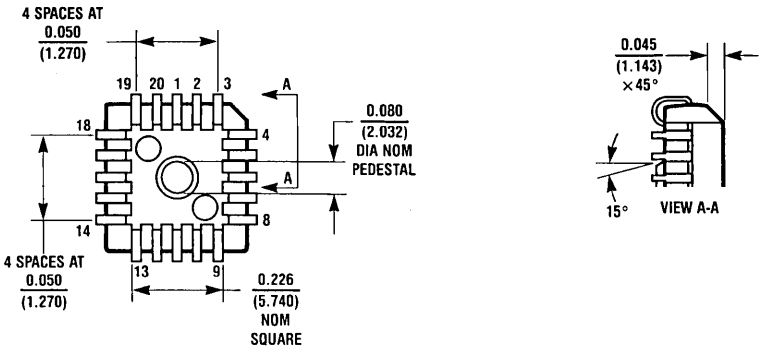

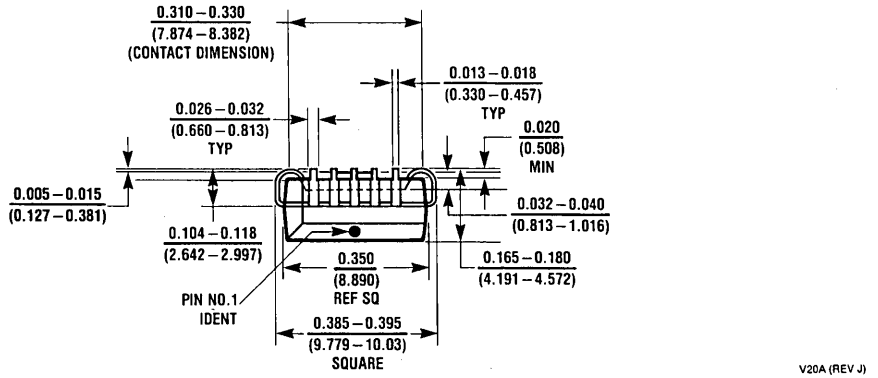

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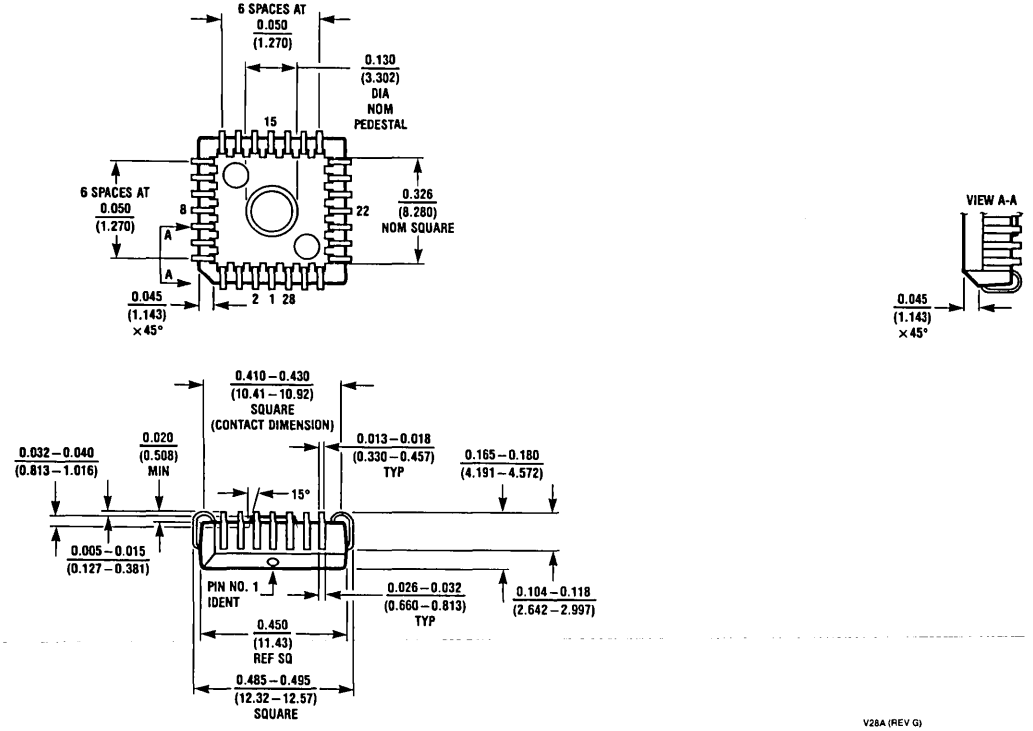

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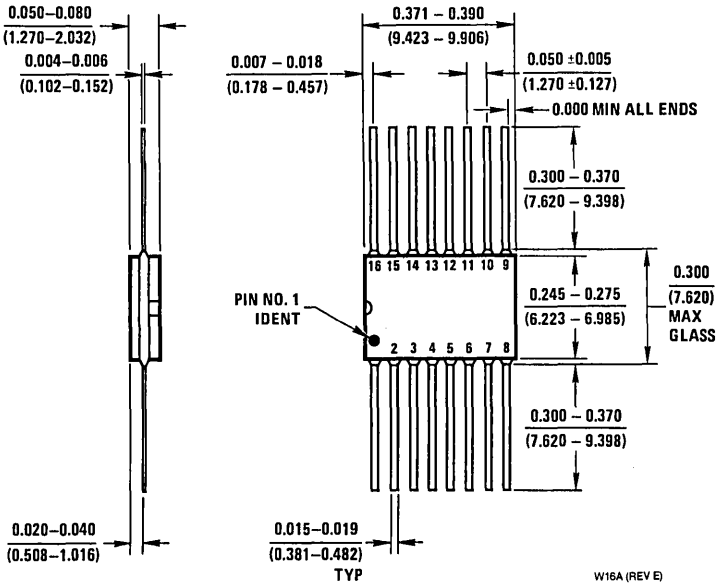

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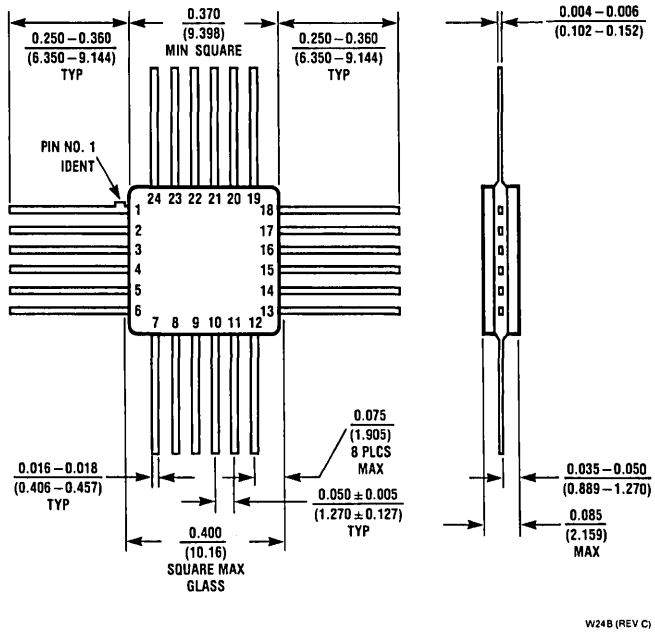

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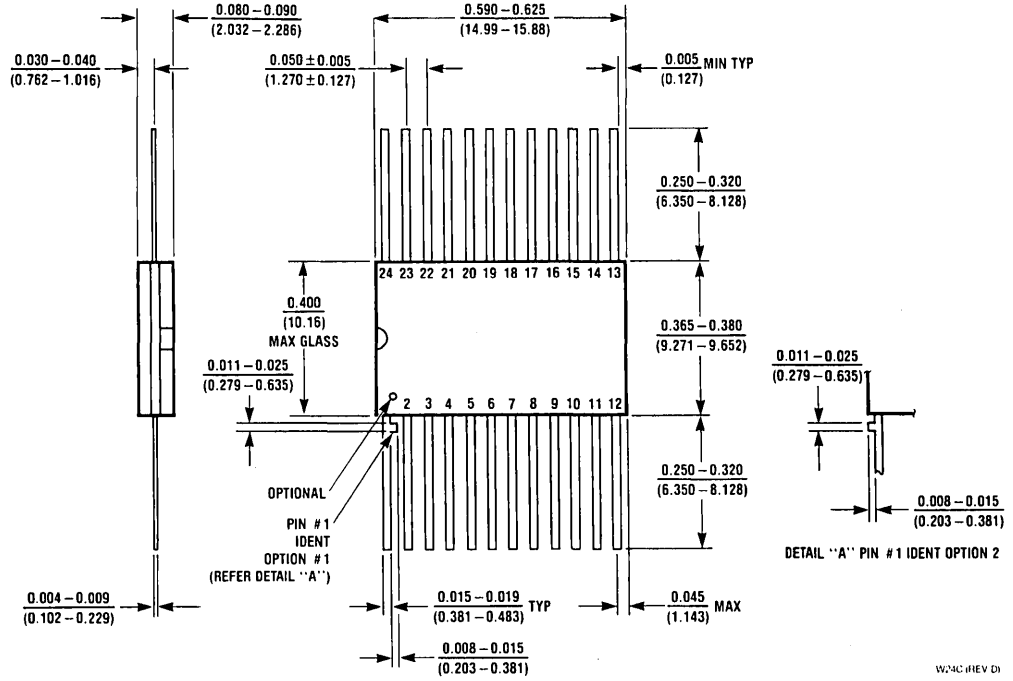

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NOTES

NOTES

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