400072

National Semiconductor Corporation

Non-Volatile Memory Databook

- *CMOS EPROMs*
- *EEPROMs*
- *BIPOLAR PROMs*

1987 Non-Volatile Memory Databook National Semiconductor

Non-Volatile Memory
DATABOOK

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Introduction to the Non-Volatile Memory Family

National Semiconductor looks at memory the way you do.

Some of your systems require non-volatile memory with lightning-fast address-access times for high-speed micro-control storage. To meet those needs, there is National's Bipolar PROM Family.

For systems that require non-volatile memory with low power consumption, reprogrammability, and microprocessor speeds, there is our CMOS EPROM Family.

Where in-circuit, remote-programmable memory can give you the design flexibility and end product advantage you need, National provides you with a family of EEPROMS.

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Section 1

CMOS EPROMs

Section 1 Contents

CMOS EPROMs Non-Volatile Memory Selection Guide

Part No.	Org.	Size	No. of Pins	Access Time	Prog. Volt.	PS Tol.	Power (mW) Active/SBY	Temp Range
NMC27C16BQ35	2k x 8	16k	24	350	13	5%	26.25/0.53	0°C to +70°C
NMC27C16BQE35	2k x 8	16k	24	350	13	5%	26.25/0.53	−40°C to +85°C
NMC27C32BQ200	4k x 8	32k	24	200	13	10%	27.5/0.55	0°C to +70°C
NMC27C32BQ350	4k x 8	32k	24	350	13	10%	27.5/0.55	0°C to +70°C
NMC27C32BQE200	4k x 8	32k	24	200	13	10%	27.5/0.55	−40°C to +85°C
NMC27C32BQE350	4k x 8	32k	24	350	13	10%	27.5/0.55	−40°C to +85°C
NMC27C64Q15	8k x 8	64k	28	150	13	5%	55/0.55	0°C to +70°C
NMC27C64Q150	8k x 8	64k	28	150	13	10%	55/0.55	0°C to +70°C
NMC27C64Q200	8k x 8	64k	28	200	13	10%	55/0.55	0°C to +70°C
NMC27C64Q250	8k x 8	64k	28	250	13	10%	55/0.55	0°C to +70°C
NMC27C64Q300	8k x 8	64k	28	300	13	10%	55/0.55	0°C to +70°C
NMC27C64QE200	8k x 8	64k	28	200	13	10%	55/0.55	−40°C to +85°C
NMC27C64QM250	8k x 8	64k	28	250	13	10%	55/0.55	−55°C to +125°C
NMC27C256Q17	32k x 8	256k	28	170	13	5%	55/0.55	0°C to +70°C
NMC27C256Q200	32k x 8	256k	28	200	13	10%	55/0.55	0°C to +70°C
NMC27C256Q250	32k x 8	256k	28	250	13	10%	55/0.55	0°C to +70°C
NMC27C256Q300	32k x 8	256k	28	300	13	10%	55/0.55	0°C to +70°C
NMC27C256QE250	32k x 8	256k	28	250	13	10%	55/0.55	−40°C to +85°C
NMC27C256QM250	32k x 8	256k	28	250	13	10%	55/0.55	−55°C to +125°C
NMC27C256QM350	32k x 8	256k	28	350	13	10%	55/0.55	−55°C to +125°C
NMC27C256BQ90	32k x 8	256k	28	90	12.5	10%	220/0.55	0°C to +70°C
NMC27C256BQ120	32k x 8	256k	28	120	12.5	10%	220/0.55	0°C to +70°C
NMC27C256BQ150	32k x 8	256k	28	150	12.5	10%	220/0.55	0°C to +70°C
NMC27C256BQ200	32k x 8	256k	28	200	12.5	10%	220/0.55	0°C to +70°C
NMC27C256BQE120	32k x 8	256k	28	120	12.5	10%	220/0.55	−40°C to +85°C
NMC27C256BQM150	32k x 8	256k	28	150	12.5	10%	220/0.55	−55°C to +125°C

Part No.	Org.	Size	No. of Pins	Access Time	Prog. Volt.	PS Tol.	Power (mW) Active/SBY	Temp Range
NMC27C512Q250	64k x 8	512k	28	250	13	10%	55/0.55	0°C to +70°C
NMC27C512Q300	64k x 8	512k	28	300	13	10%	55/0.55	0°C to +70°C
NMC27C512Q350	64k x 8	512k	28	350	13	10%	55/0.55	0°C to +70°C
NMC27C512QE250	64k x 8	512k	28	250	13	10%	55/0.55	−40°C to +85°C
NMC27C512QM350	64k x 8	512k	28	350	13	10%	55/0.55	−55°C to +125°C
NMC27C512AQ90	64k x 8	512k	28	90	12.5	10%	220/0.55	0°C to +70°C
NMC27C512AQ120	64k x 8	512k	28	120	12.5	10%	220/0.55	0°C to +70°C
NMC27C512AQ150	64k x 8	512k	28	150	12.5	10%	220/0.55	0°C to +70°C
NMC27C512AQ200	64k x 8	512k	28	200	12.5	10%	220/0.55	0°C to +70°C
NMC27C512AQE120	64k x 8	512k	28	120	12.5	10%	220/0.55	−40°C to +85°C
NMC27C512AQM150	64k x 8	512k	28	150	12.5	10%	220/0.55	−55°C to +125°C
NMC27C1024Q90	64k x 16	1024k	40	90	12.5	10%	275/0.55	0°C to +70°C
NMC27C1024Q120	64k x 16	1024k	40	120	12.5	10%	275/0.55	0°C to +70°C
NMC27C1024Q150	64k x 16	1024k	40	150	12.5	10%	275/0.55	0°C to +70°C
NMC27C1024Q200	64k x 16	1024k	40	200	12.5	10%	275/0.55	0°C to +70°C
NMC27C1024QE120	64k x 16	1024k	40	120	12.5	10%	275/0.55	−40°C to +85°C
NMC27C1024QM150	64k x 16	1024k	40	150	12.5	10%	275/0.55	−55°C to +125°C
NMC27C1023Q90	128 x 8	1024k	32	90	12.5	10%	275/0.55	0°C to +70°C
NMC27C1023Q120	128 x 8	1024k	32	120	12.5	10%	275/0.55	0°C to +70°C
NMC27C1023Q150	128 x 8	1024k	32	150	12.5	10%	275/0.55	0°C to +70°C
NMC27C1023Q200	128 x 8	1024k	32	200	12.5	10%	275/0.55	0°C to +70°C
NMC27C1023QE120	128 x 8	1024k	32	120	12.5	10%	275/0.55	−40°C to +85°C
NMC27C1023QM150	128 x 8	1024k	32	150	12.5	10%	275/0.55	−55°C to +125°C

National Semiconductor Corporation

PRELIMINARY

One-Time-Programmable EPROMs

National Semiconductor plans to introduce the following EPROMs in a plastic One-Time-Programmable package in 1987:

NMC27C32BN
NMC27C64N
NMC27C256BN
NMC27C512AN
NMC27C1023N
NMC27C1024N

The One-Time-Programmable EPROM, or OTP, is an EPROM packaged in a molded plastic package without a quartz window. This part is particularly advantageous for users of the EPROM who are in high volume production, as opposed to those who use it for pattern experimentation and proto-typing. National can produce the OTP very economically because neither a quartz window nor a hermetically sealed package is required.

Since the OTP does not have a quartz window to expose the chip to UV light, the device cannot be erased. It therefore can only be programmed once by the user.

The plastic OTP EPROM has the additional advantage as a production part that it works well in automatic insertion equipment.

National Semiconductor has earned an excellent reputation in the industry for product reliability. The OTP EPROM will be produced with the same stringent reliability standards as other National products.

National Semiconductor Corporation

PRELIMINARY

NMC27C16B 16,384-Bit (2048 x 8) UV Erasable CMOS PROM

General Description

The NMC27C16B is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C16B is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

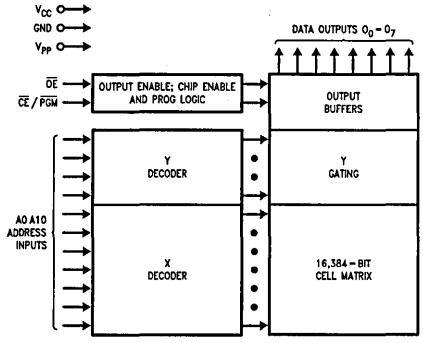
Features

- Clocked sense amps for fast access—350 ns
- Low CMOS power consumption
  Active power: 26.25 mW max
  Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C16BQE), −40°C to +85°C
- Pin compatible to MM2716 and National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block and Connection Diagrams

Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect



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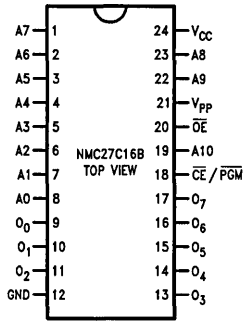
27C256 27256	27C128 27128	27C64 2764	27C32 2732
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package



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27C32 2732	27C64 2764	27C128 27128	27C256 27256
	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16 pins.

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND −0.6V
V_{PP} Supply Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Operating Conditions (Note 7)

Temperature Range	
NMC27C16BQ35	0°C to +70°C
NMC27C16BQE35	−40°C to +85°C
V_{CC} Power Supply	+5V ±5%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Condition	NMC27C16B 350,E350		Units
			Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{OE} = \overline{OE} = V_{IL}$	0		ns

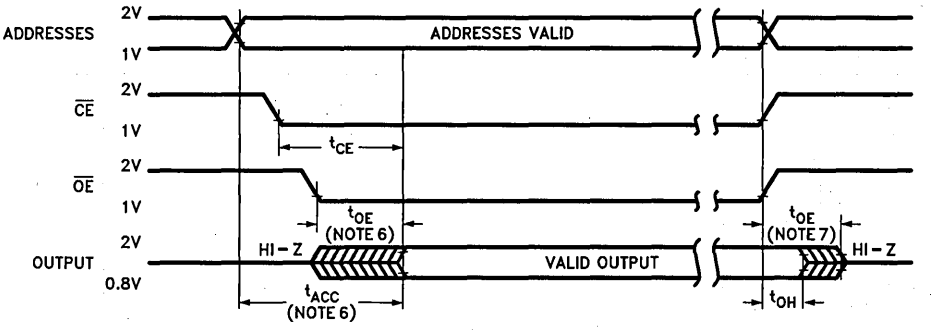
Capacitance (Note 5) (T_A = +25°C, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 20 ns	Inputs	1V and 2V
Input Pulse Levels	0.8V to 2.2V	Outputs	0.8V and 2V

AC Waveforms (Note 2)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for T_A = +25°C and nominal supply voltages.

Note 5: This paramenter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

Programming Characteristics

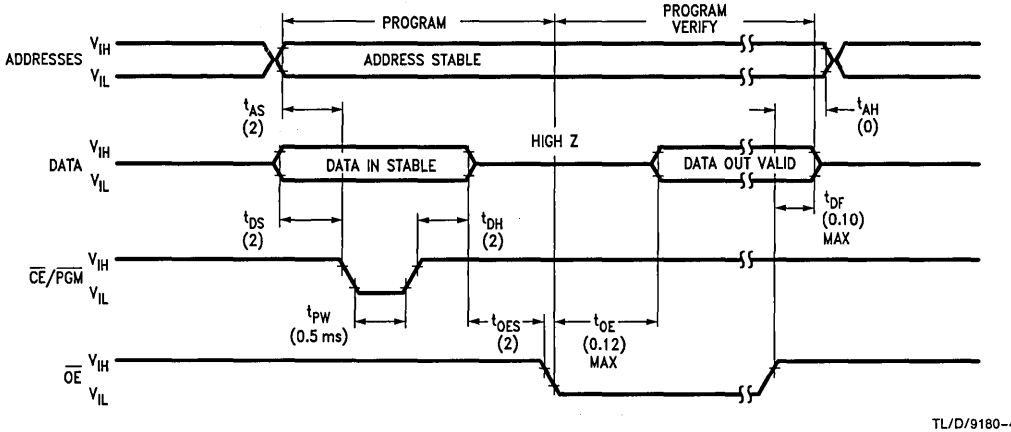
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.2V to 13.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}	0		100	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}			120	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.2V to 13.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

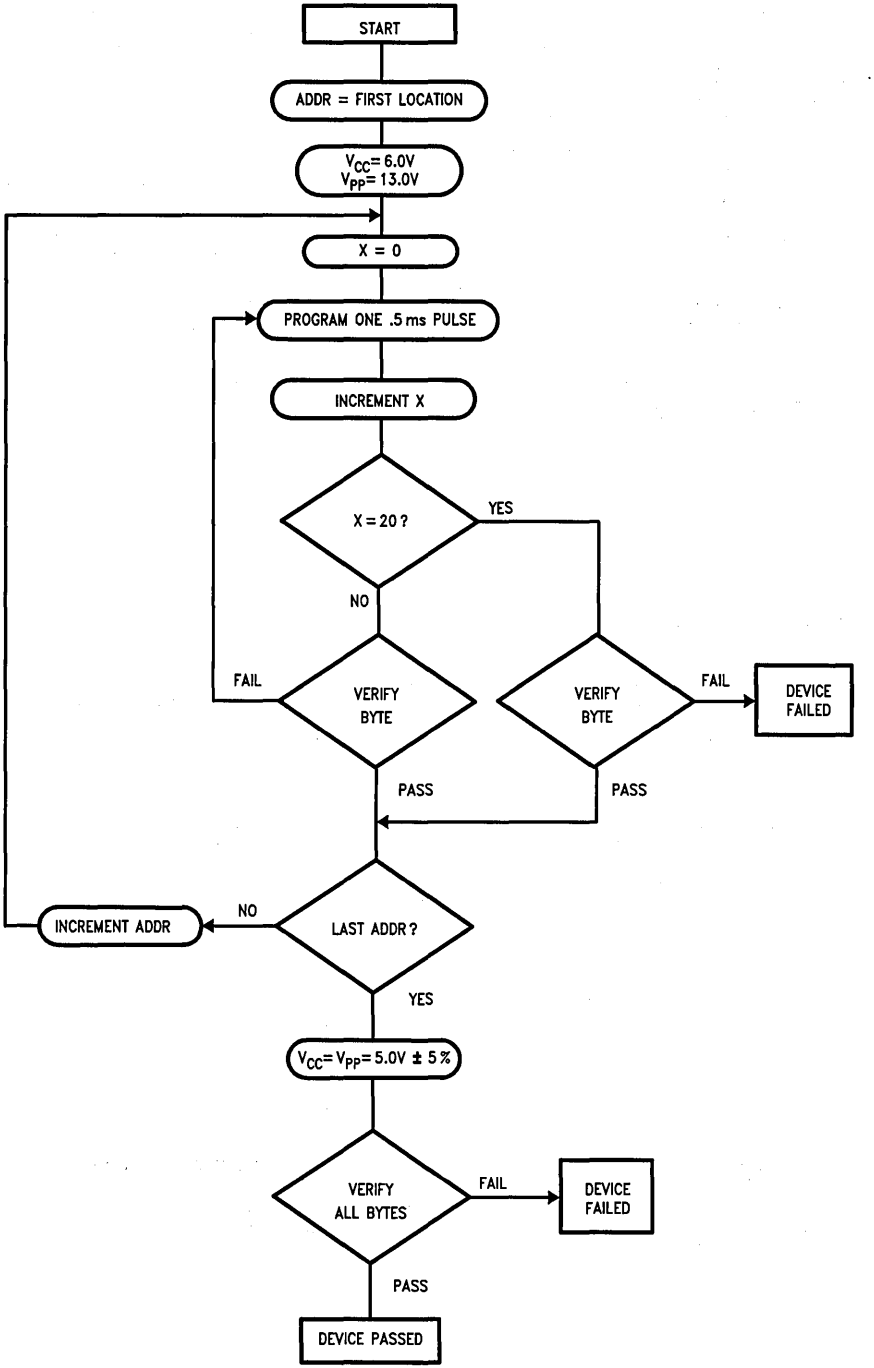
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C16B must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/9180–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C16B are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}. The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C16B is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C16B must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27C16B in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27C16Bs.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11), (13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	13.0	6	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0	6	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0	6	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C16Bs may be common. A TTL low level program pulse applied to an NMC27C16B's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 13.0V will program that NMC27C16B. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other NMC27C16Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. Except during programming and program verify, V_{PP} must be at V_{CC}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C16B in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C16B is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a mimimum of 15W-sec/cm^2.

The NMC2716B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C32B 32,768-Bit (4k x 8) UV Erasable CMOS PROM

General Description

The NMC27C32B is a high-speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over the Extended Temperature Range.

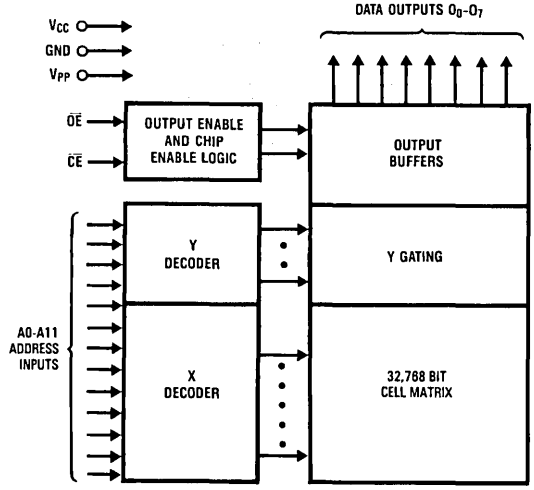
The NMC27C32B is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-ploy silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 200 ns
- Low CMOS power consumption
  - — Active Power 27.5 mW max
  - — Standby Power 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C32BQE), −40°C to 85°C, available
- Pin compatible with NMOS 32k EPROMS
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



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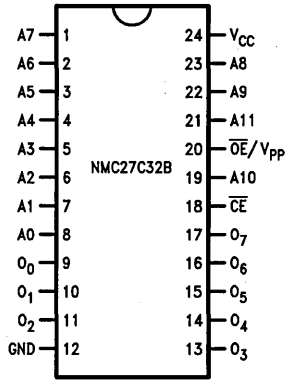
Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/ Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C56 27256	27C128 27128	27C64 2764	27C16 2716
V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package



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Top View

27C16 2716	27C64 2764	27C128 27128	27C256 27256
	V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$	V_{CC} A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
VPP	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pins.

See NS Package Number J24A-Q

Commercial Temp Range (0°C to +70°C)

$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
NMC27C32BQ200	200
NMC27C32BQ350	350

Extended Temp Range (−40°C to +85°C)

$V_{CC} = 5V \pm 10\%$

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200
NMC27C32BQE350	350

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3V to GND −0.6V
V_{PP} Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Operating Conditions (Note 7)

Temperature Range	
NMC27C32BQ200, 350	0°C to +70°C
NMC27C32BQE200, E350	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 1 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 1 MHz Inputs = V_{CC} or GND, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B 200, E200		NMC27C32B 350, E350		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load 1 TTL Gate and C_L = 100 pF (Note 9)

Input Rise and Fall Times ≤20 ns

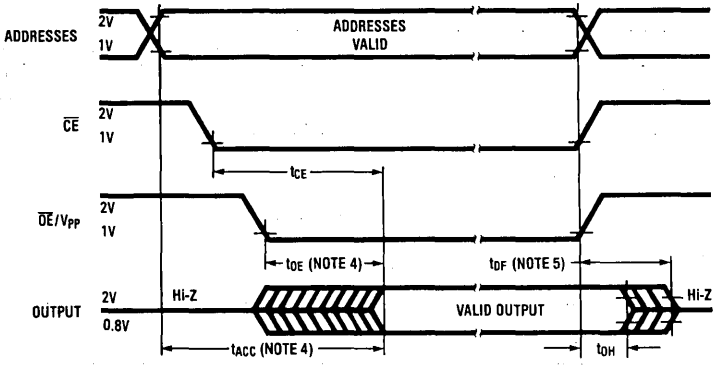
Input Pulse Levels 0.45V to 2.4V

Timing Measurement Reference Level

Inputs 1V and 2V

Outputs 0.8V and 2V

AC Waveforms



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without inpacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.

C_L: 100 pF includes fixture capacitance.

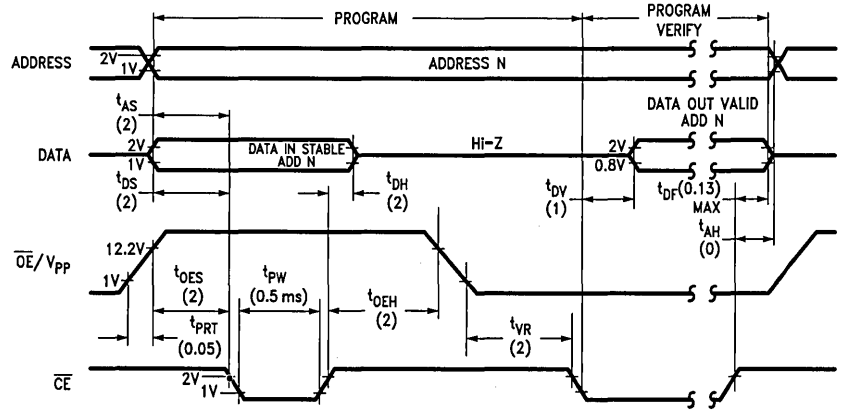
Programming Characteristics $T_A = +25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$ $V_{PP} = 12.2 - 13.3V$ (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{VR}	V_{PP} Recovery Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DV}	Data Valid From $\overline{CE}$	$\overline{CE} = \overline{OE} = V_{IL}$			1	μs
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.2 − 13.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

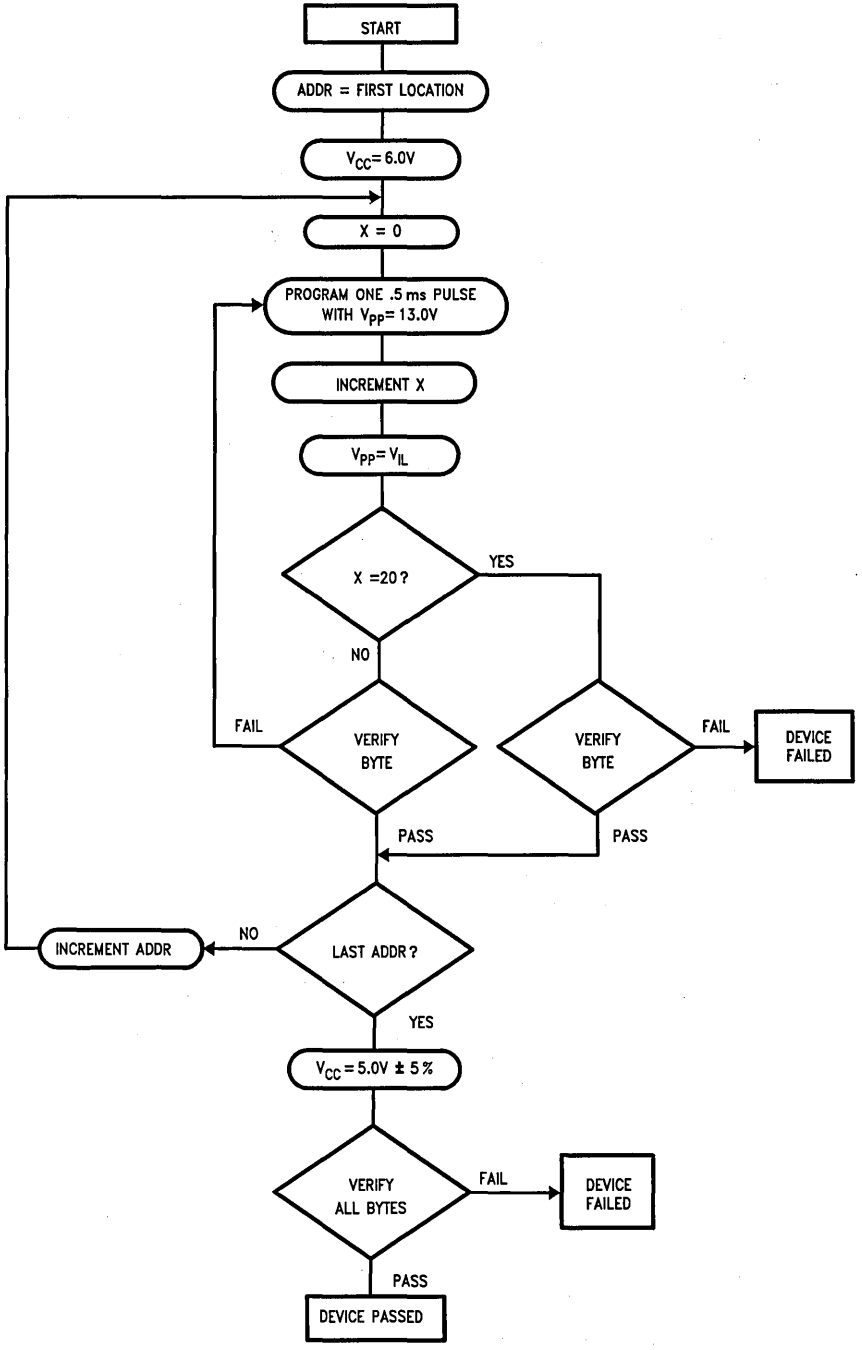
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32B must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/8827–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C32B are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 13V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast acces time. V_{CC} should therefore the maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 26.3 mW to 0.53 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) The lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V or pin 20 (V_{PP}) will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 13V. It is required that at least a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C32B is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	V_{IL}	13	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	6	D_{OUT}
Program Inhibit	V_{IH}	13	6	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 13.0V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F61", where "8F" designates that it is made by National Semiconductor, and "61" designates a 32k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C32B in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C32B is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C32B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	1	1	0	0	0	0	1	61

TABLE III. Minimum NMC27C32B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C64
65,536-Bit (8k x 8) UV Erasable CMOS PROM

General Description

The NMC27C64 is a high-speed 64k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

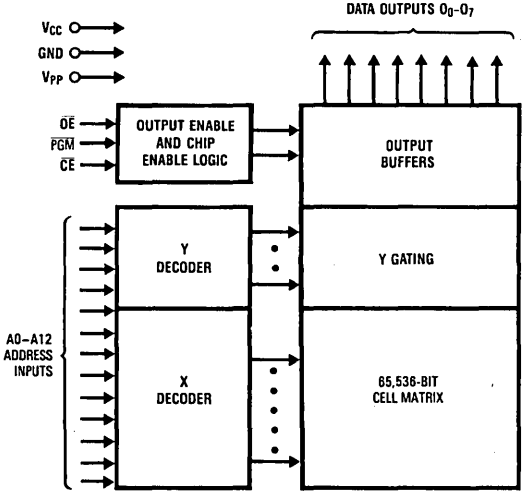
The NMC27C64 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 150 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C64QE), −40°C to 85°C, and military temperature range (NMC27C64QM), −55°C to 125°C, available
- Pin compatible with NMOS 64k EPROMS
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/8634-1

Pin Names

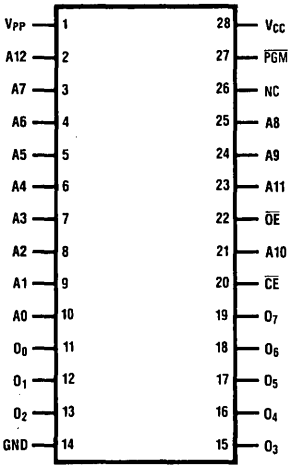
A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



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27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Order Number NMC27C64Q
See NS Package Number J28A-Q

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±5%

Parameter/Order Number	Access Time (ns)
NMC27C64Q15	150

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q150	150
NMC27C64Q200	200
NMC27C64Q250	250
NMC27C64Q300	300

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE200	200

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QM200	200
NMC27C64QM250	250

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3V to GND −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q15, Q150, 200, 250, 300	0°C to +70°C
NMC27C64QE200	−40°C to +85°C
NMC27C64QM200, M250	−55°C to +125°C
V_{CC} Power Supply except NMC27C64Q15	+5V ±10% +5V ±5%

READ OPERATION

DC Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = 2.4V or 0.45V, I/O = 0 mA		5	20	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64 15, 150 E150		NMC27C64 200, E200 M200		NMC27C64 250 M250		NMC27C64 300		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$		60		60		70		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	0	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		0		ns

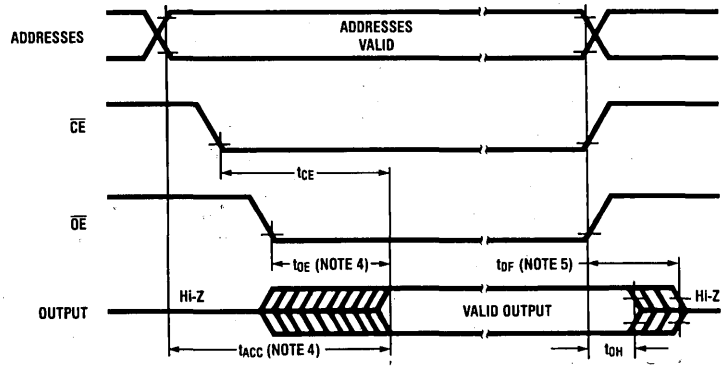
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤20 ns	Inputs	1V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms



TL/D/8634–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.

CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics $T_A = +25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$ $V_{PP} = 12.2-13.3V$ (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{CES}	$\overline{CE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$			150	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

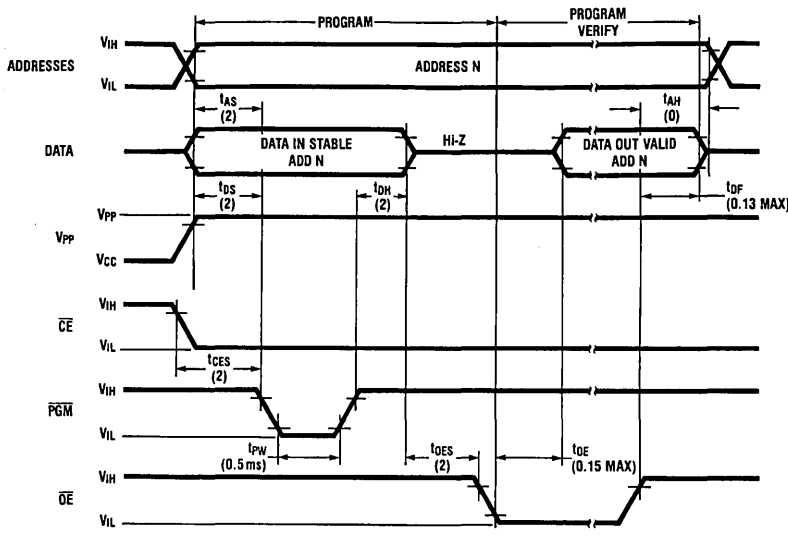
AC Test Conditions

V_{CC}	6V ±0.25V
V_{PP}	12.2−13.3V
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



TL/D/8634-4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

t_{OE} and t_{DF} are characteristics of the device but must be accommodated by the programmer.

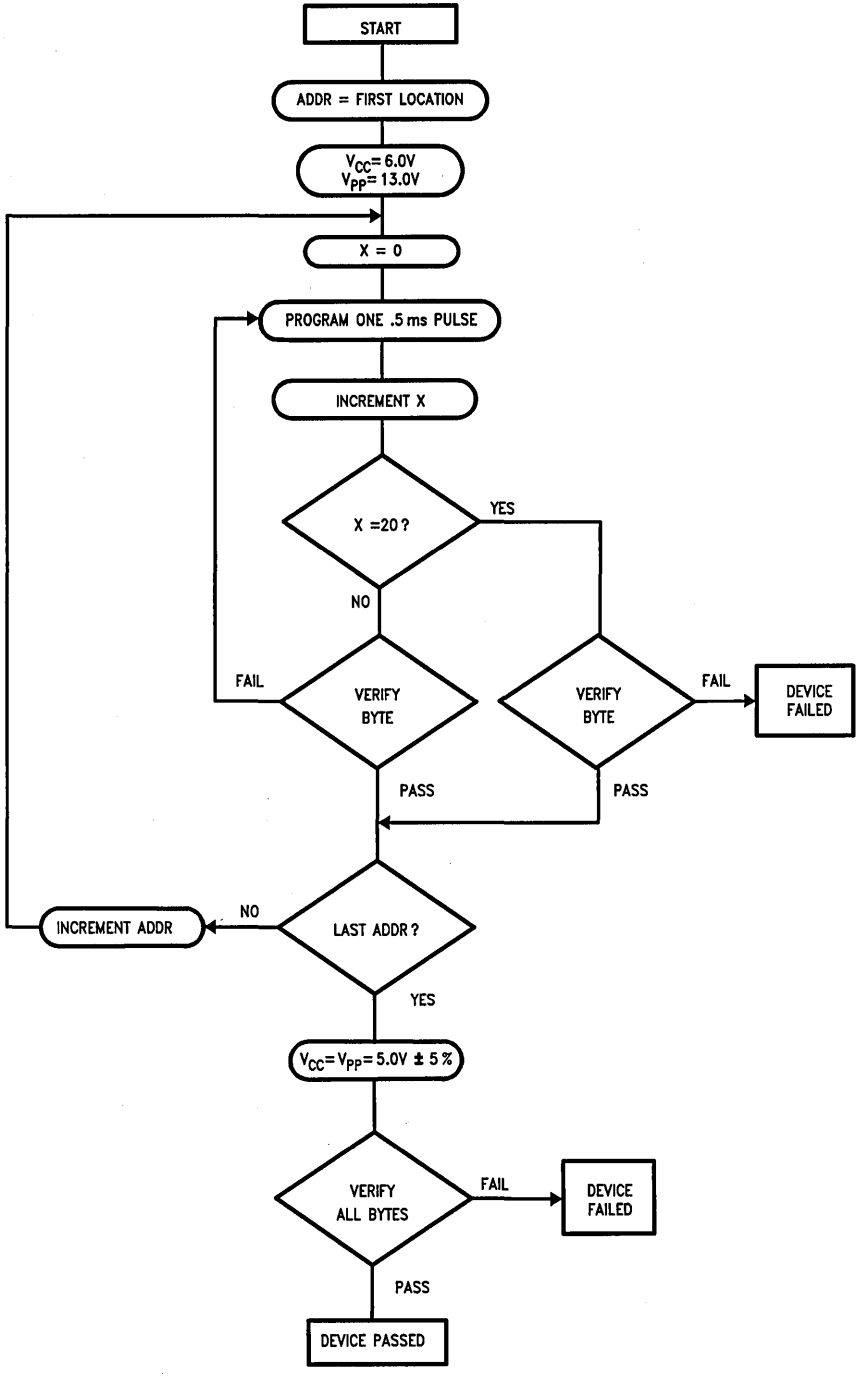
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C64 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

INTERACTIVE PROGRAMMING FLOW CHART



TL/D/8634–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, and after each erasure, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programed at any time—either individually, sequentially, or at random. The NMC27C64 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5	5	D_{OUT}
Standby	V_{IH}	X	X	5	5	Hi-Z
Program	V_{IL}	V_{IH}	Pulsed V_{IH} to V_{IL}	13.0	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13.0	6	D_{OUT}
Program Inhibit	V_{IH}	X	X	13.0	6	Hi-Z

X can be either V_{IL} or V_{IH}

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's $\overline{CE}$ input with V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. Except during programming and program verify, V_{PP} must be at V_{CC}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C64 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C64 is to be exposed to these types of lighting conditions for extended periods of time, opaque lables should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C64 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27CP128
131,072-Bit (16k x 8) UV Erasable CMOS PROM

General Description

The NMC27CP128 is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27CP128 is designed to operate with a single +5V power supply with ±10% tolerance.

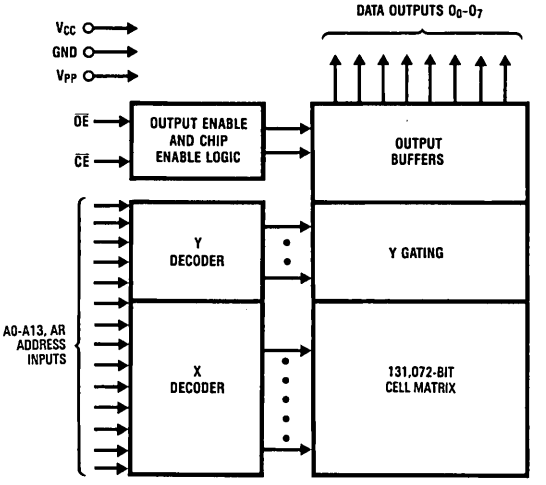
The NMC27CP128 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 200 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/8805-1

Pin Names

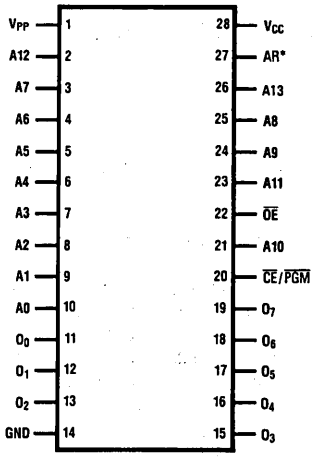
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
AR	Block Select

1

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



TL/D/8805–2

27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

*AR held at V_{IH}

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27CP128 pins.

Order Number NMC27CP128Q
See NS Package Number J28A–Q

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27CP128Q200	200
NMC27CP128Q250	250
NMC27CP128Q300	300

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC}+0.3V to GND−0.6V
ESD rating is to be determined.	
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range NMC27CP128Q200, 250, 300	0°C to +70°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{PP}	V_{PP} Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}/\overline{PGM}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE}/\overline{PGM} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC}−0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27CP128 200		NMC27CP128 250		NMC27CP128 300		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}/\overline{PGM}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}/\overline{PGM} = V_{IL}$		60		70		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}/\overline{PGM} = V_{IL}$	0	60	0	60	0	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}/\overline{PGM}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$	0		0		0		ns

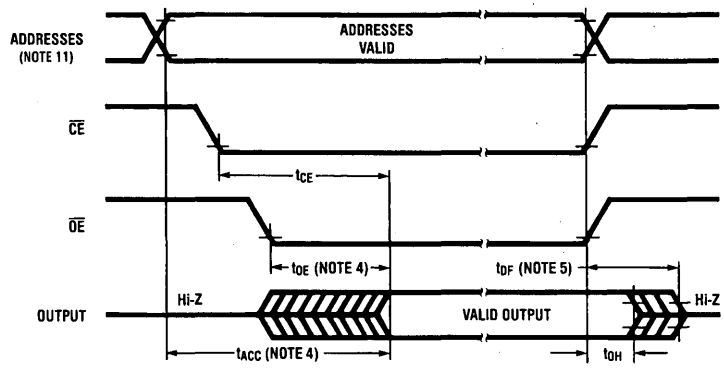
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤20 ns	Inputs	1V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms



TL/D/8805–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}/\overline{PGM}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}/\overline{PGM}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Note 11: AR held at V_{IH}.

Programming Characteristics

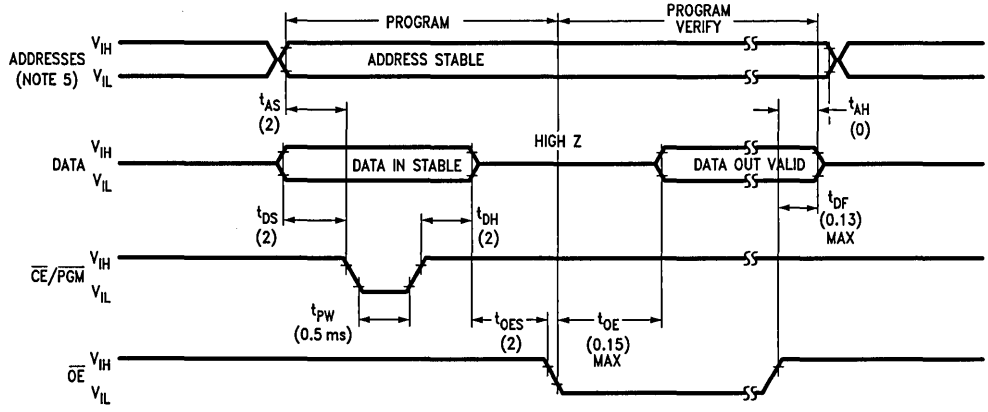
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.2V to 13.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}	0		130	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}			150	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.2V to 13.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



TL/D/8805-4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

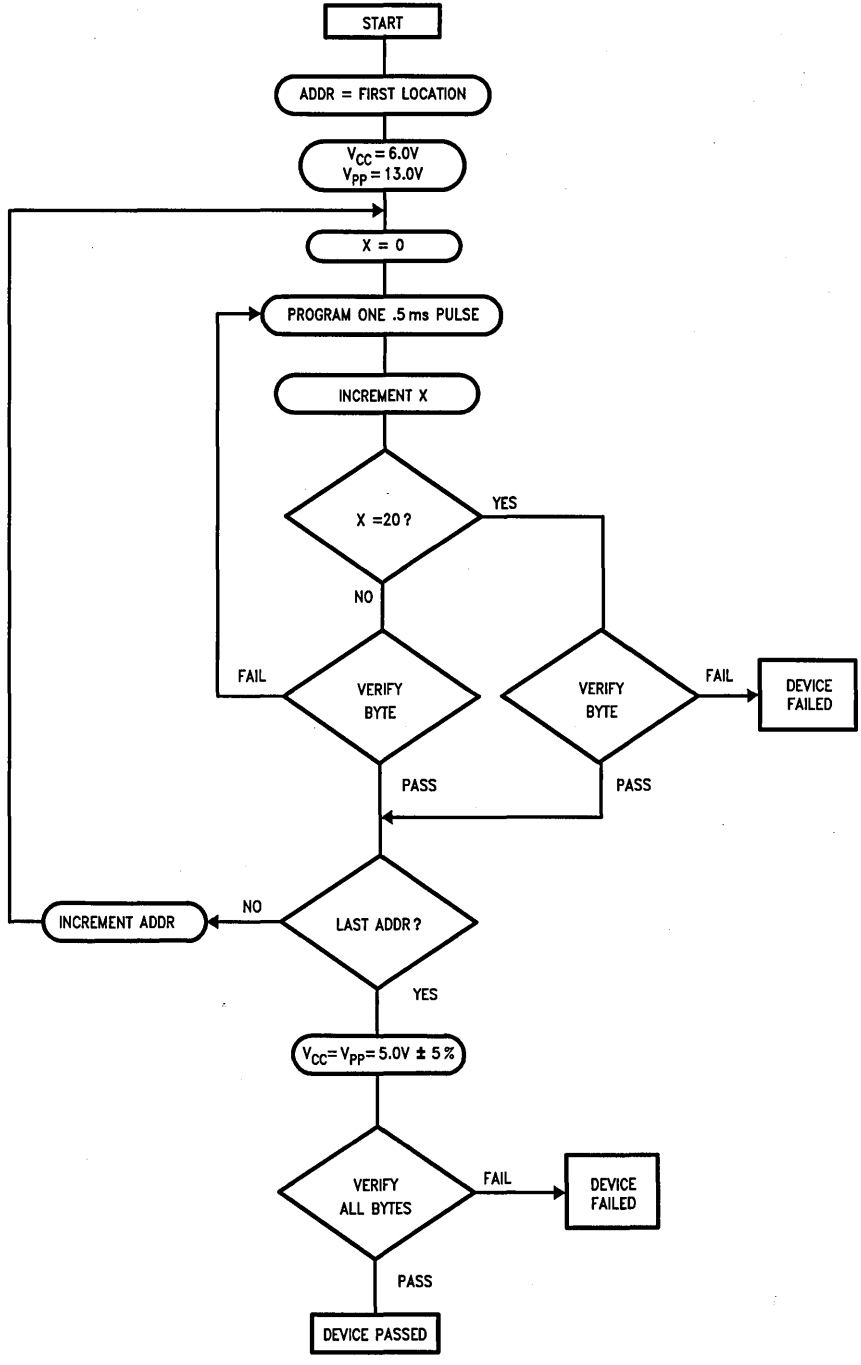
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27CP128 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Note 5: AR held at V_{IH}.

Interactive Programming Flow Chart



TL/D/8805–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27CP128 are listed in Table I. It should be noted that all inputs for the five modes may be at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27CP128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27CP128 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27CP128 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27CP128s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27CP128.

Initially, and after each erasure, all bits of the NMC27CP128 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27CP128 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs may be TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27CP128 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). In either case, since the NMC27CP128 employs the last 131,072 bits of a 262, 144 bit memory array, programming must be started at address 16, 384 to provide correct data read. Only the interactive programming method has been tested. The NMC27CP128 must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27CP128s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27CP128s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27CP128s.

The NMC27CP128 is a partial NMC27C256 and therefore is not program compatible with most 128K EPROMs.

The Manufacturer's Identification Code should not be used for programming control of the NMC27CP128.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	13.0	6	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0	6	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0	5	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27CP128s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel NMC27CP128 may be common. A low level $\overline{CE}/\overline{PGM}$ input selects the devices to be programmed. A high level $\overline{CE}/\overline{PGM}$ input inhibits the other devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. Except during programming and program verify, V_{PP} must be at V_{CC}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27CP128 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27CP128 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27CP128 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27CP128's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27CP128 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27CP128 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27CP128 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27CP128 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C128C 131,072-Bit (16k x 8) UV Erasable CMOS PROM (Very High Speed Version)

General Description

The NMC27C128C are very high-speed 128k UV erasable and electrically reprogrammable CMOS EPROMs, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C128C are designed to operate with a single +5V power supply with ±10% tolerance.

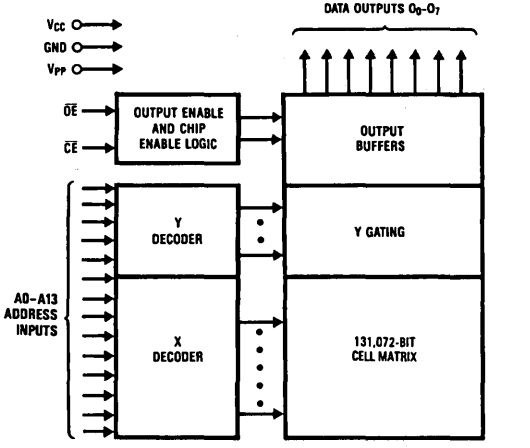
The NMC27C128C are packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

The EPROMs are fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

- Access time down to 45 ns, two transistor memory cell
- Low CMOS power consumption
  —Active Power: 360 mW max
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with NMOS 128k EPROMs

Block Diagram



TL/D/9185-1

Pin Names

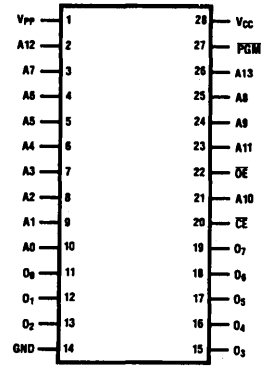
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/9185–2

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C128C pins.

Order Number NMC27C128CJ
See NS Package Number J28AQ

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C128BQ45	45
NMC27C128BQ55	55
NMC27C128BQ70	70

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C256
262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256 is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

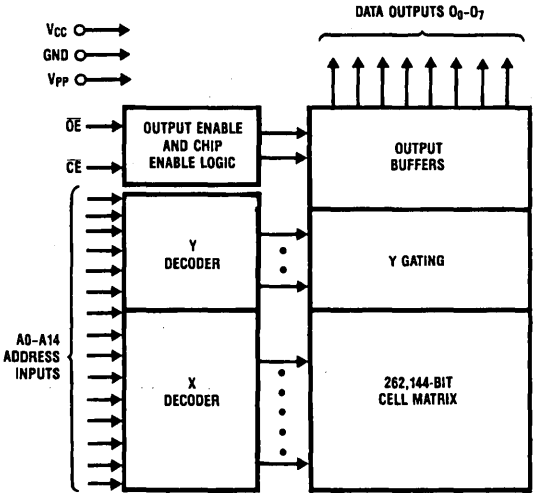
The NMC27C256 is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 170 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C256QE), −40°C to 85°C, and military temperature range (NMC27C256QM), −55°C to 125°C, available
- Pin compatible with NMOS 256k EPROMS
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/7512-1

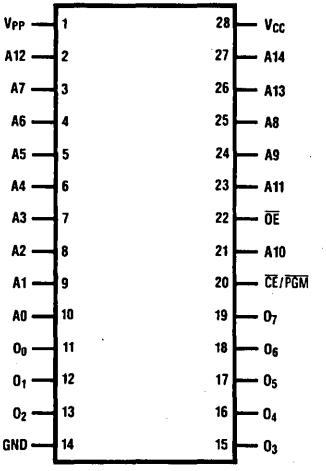
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



TL/D/7512–2

27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256 pins.

Order Number NMC27C256Q
See NS Package Number J28A–Q

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±5%

Parameter/Order Number	Access Time
NMC27C256Q17	170

V_{CC} = 5V±10%

Parameter/Order Number	Access Time
NMC27C256Q200	200
NMC27C256Q250	250
NMC27C256Q300	300

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C256QE250	250

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V±10%

Parameter/Order Number	Access Time
NMC27C256QM250	250
NMC27C256QM350	350

COMMERCIAL TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3 to GND −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range	0°C to +70°C
V_{CC} Power Supply	
NMC27C256Q17	5V±5%
NMC27C256Q200, 250, 300	5V±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256 17		NMC27C256 200		NMC27C256 250		NMC27C256 300		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	60		105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

MILITARY AND EXTENDED TEMPERATURE RANGE

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	Operating Temp Range
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3V to GND −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C256QE250	−40°C to +85°C
NMC27C256QM250, M350	−55°C to +125°C
V_{CC} Power Supply	5V ± 10%

READ OPERATION

DC Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHZ Inputs = V_{CC} or GND I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OH} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256 E250 M250		NMC27C256 M350		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		250		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

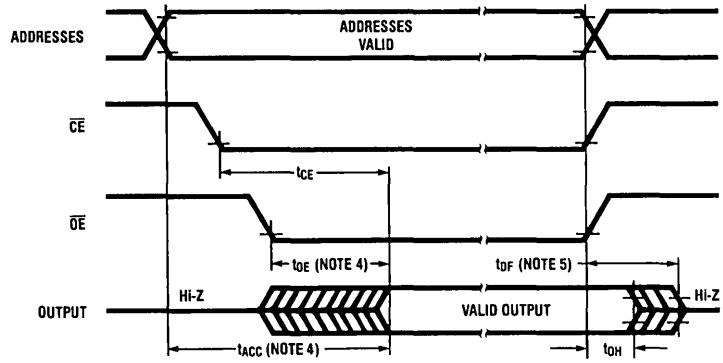
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 9)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤20 ns	Inputs	1V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms



TL/D/7512–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics

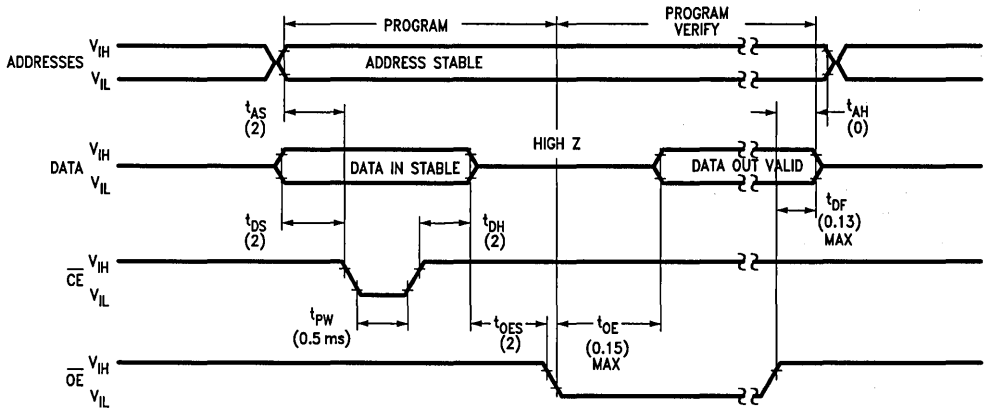
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.2V to 13.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}	0		130	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/\overline{PGM}$ = V_{IL}			150	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.2V to 13.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



TL/D/7512–4

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

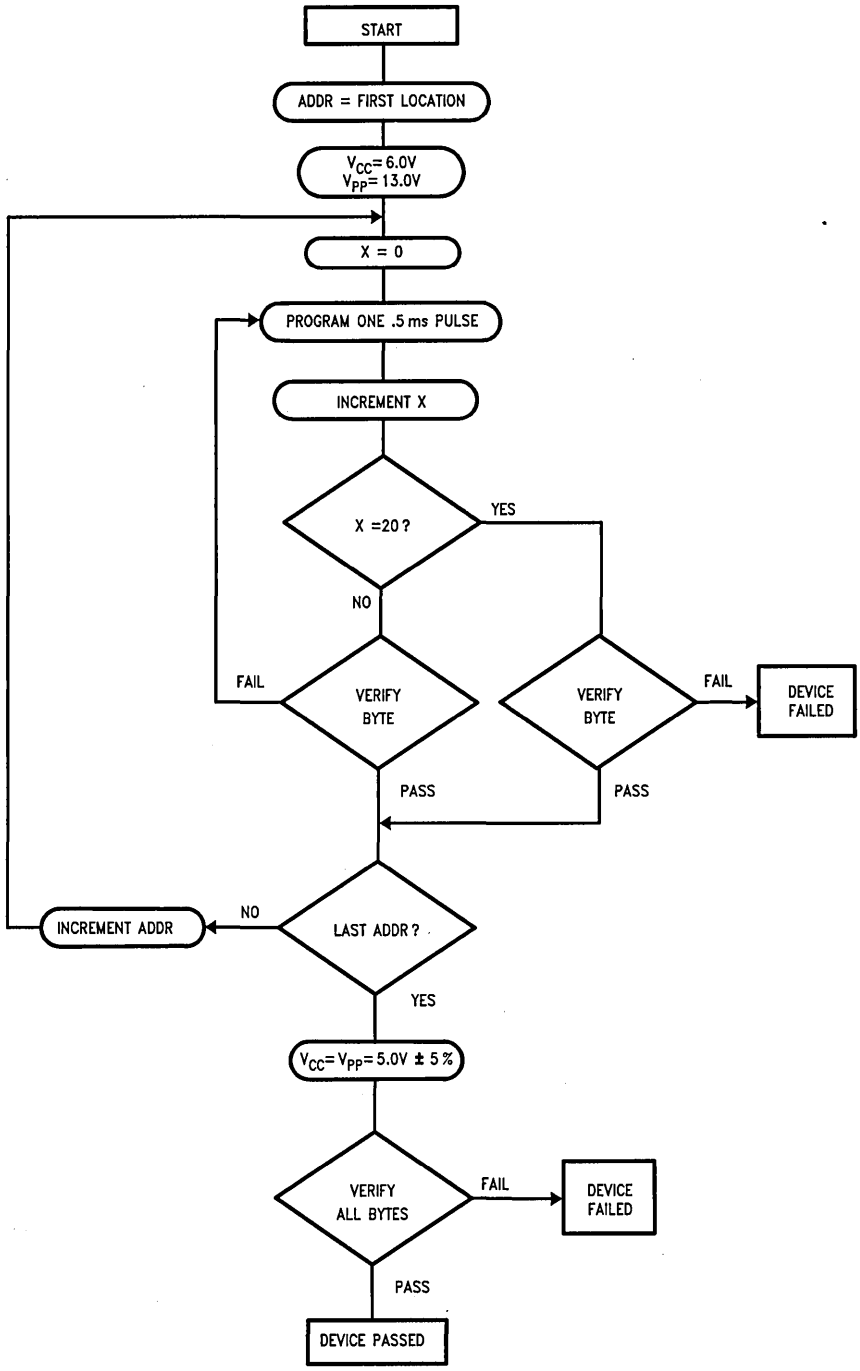
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C256 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

INTERACTIVE PROGRAMMING FLOW CHART



TL/D/7512–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C256 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C256 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C256 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C256.

Initially, and after each erasure, all bits of the NMC27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C256 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C256 must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27C256s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	13.0	6	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0	6	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0	6	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C256s may be common. A TTL low level program pulse applied to an NMC27C256's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 13.0V will program that NMC27C256. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. Except during programming and program verify, V_{PP} must be at V_{CC}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C256 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C256 is to be exposed to these types of lighting conditions for extended periods of time, opaque lables should be placed over the NMC27C256's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C256 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C256 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C256B High Speed Version 262,144-Bit (32k x 8) UV Erasable CMOS PROM

General Description

The NMC27C256B is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256B is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

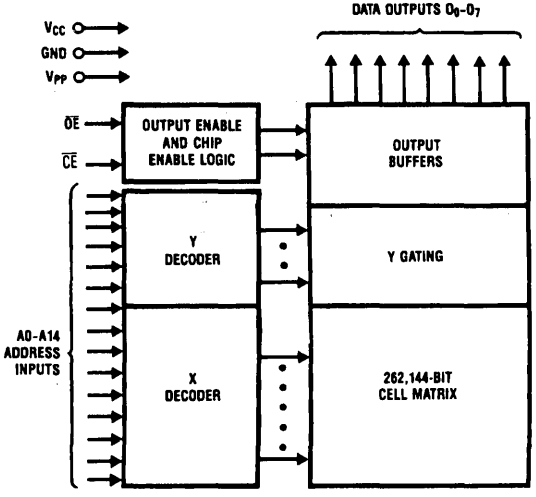
The NMC27C256B is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

These EPROMs are fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 90 ns
- Low CMOS power consumption
  - — Active Power: 220 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800 CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C256BQE), −40°C to 85°C, and military temperature range (NMC27C256BQM), −55°C to 125°C, available
- Pin compatible with NMOS 256k EPROMS
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation for NMC27C256B—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/9125–1

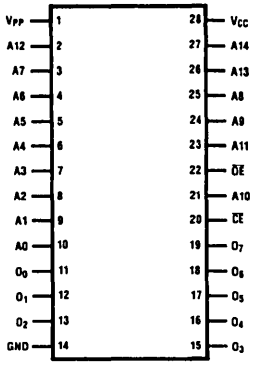
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C128 27128	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/9125–2

Order Number NMC27C256BQ
See NS Package Number J28A-Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256B pins.

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQ90	90
NMC27C256BQ120	120
NMC27C256BQ150	150
NMC27C256BQ200	200

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQE120	120

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C256BQM150	150

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages and A9 with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3 to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+13.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

ESD Rating to be determined.

Operating Conditions (Note 7)

V_{CC} Power Supply	5V ±10%
Temperature Range	
NMC27C256BQ90, 120, 150, 200	0°C to +70°C
NMC27C256BQE120	−40°C to +85°C
NMC27C256BQM150	−55°C to +125°C

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHZ All Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	60	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	40	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Ouput Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C256B 90		NMC27C256B 120 E120		NMC27C256B 150 M150		NMC27C256B 200		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		40		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	40	0	50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

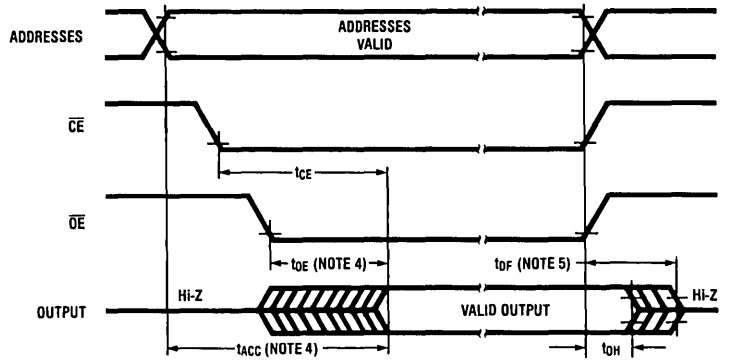
Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms



TL/D/9125–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V.

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.

CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics

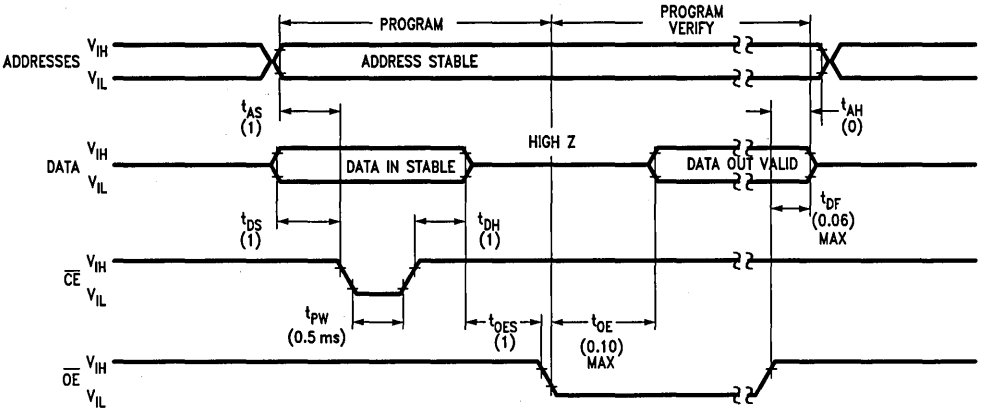
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5 ±0.3V (Notes 2, 3, 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	CE = V_{IL}	0		60	ns
t_{OE}	Output Enable to Output Delay	CE = V_{IL}			100	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	CE = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Input Pulse Levels	0.45V to 2.4V
V_{PP}	12.5 ±0.3V	Timing Measurement Reference Level	
Input Rise and Fall Times	≤5 ns	Inputs	1V and 2V
		Outputs	0.8V and 2V

Programming Waveforms (Note 3)



TL/D/9125–5

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

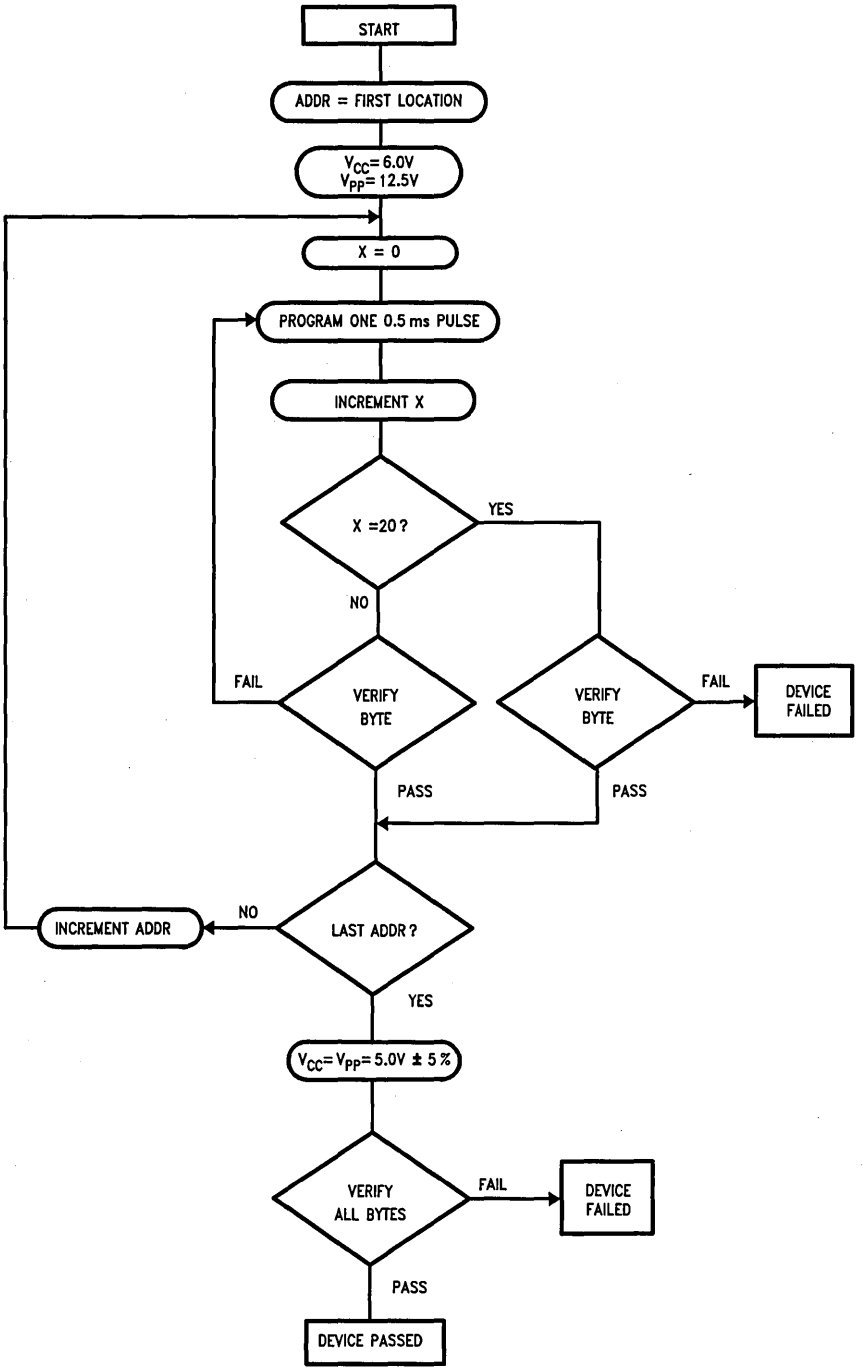
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C256B must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 13V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/9125–6

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C256B are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.5V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C256B has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The NMC27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C256B are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 13V on pin 1 (V_{PP}) will damage the NMC27C256B.

Initially, and after each erasure, all bits of the NMC27C256B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C256B are in the programming mode when the V_{PP} power supply is at 12.5V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C256B is designed to be programmed in either of

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (ALE)* (20)	$\overline{OE}$ (22)	V_P (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	12.5	6	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.5	6	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.5	6	Hi-Z

Functional Description (Continued)

two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C256B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C256B in parallel with the same data can be easily acccomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C256B may be connected together when they are programmed with the same data. A low level TTL pulse applied; to the $\overline{CE}$ input programs the paralleled NMC27C256B.

Program Inhibit

Programming multiple NMC27C256B in parallel with different data is also easily accomplished. Except $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C256B may be common. A TTL low level program pulse applied to an NMC27C256B $\overline{CE}$ input with V_{PP} at 12.5V will program that NMC27C256B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C256B from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Manufacturer's Identification Code

The NMC27C256B has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C256B is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 11.4V to 12.0V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C256B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C256B in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. Opaque labels should be placed over the NMC27C256B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C256B is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C256B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C256B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	0_7 (12)	0_6 (13)	0_5 (14)	0_4 (15)	0_3 (16)	0_2 (17)	0_1 (18)	0_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IL}	0	0	0	0	0	1	0	0	04

Functional Description (Continued)

TABLE III. Minimum NMC27C256B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C512
524,288-Bit (64k x 8) UV Erasable CMOS PROM

General Description

The NMC27C512 is a high-speed 512k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C512 is designed to operate with a single +5V power supply with ±5% or ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

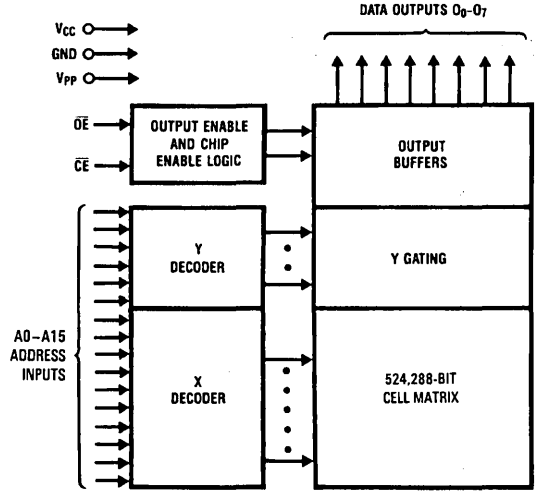
The NMC27C512 is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 200 ns
- Low CMOS power consumption
  - — Active Power: 55 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C512QE), −40°C to 85°C, and military temperature range (NMC27C512QM), −55°C to 125°C, available
- Pin compatible with NMOS 512k EPROMS
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/8754–1

Pin Names

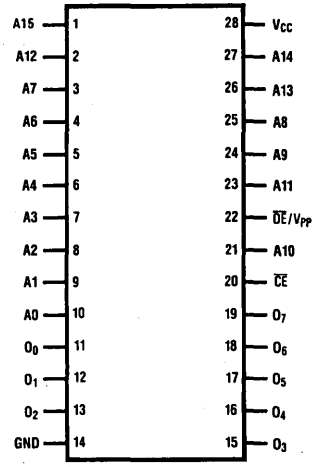
A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/ Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

1

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/8754–2

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512 pins.

See NS Package Number J28A–Q

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±5%

Parameter/Order Number	Access Time
NMC27C512Q20	200

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C512Q250	250
NMC27C512Q300	300
NMC27C512Q350	350

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C512QE250	250

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time
NMC27C512QM350	350

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	Operating Temp Range
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC}+0.3 to GND−0.6V
V_{PP} and A9 Supply Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C512Q20,250,300,350	0°C to 70°C
NMC27C512QE250	−40°C to +85°C
NMC27C512QM350	−55°C to +125°C
V_{CC} Power Supply	5V ±10%
except NMC27C512Q20	5V ±5%

ESD rating is to be determined.

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512 20		NMC27C512 250, E250		NMC27C512 300		NMC27C512 350 M350		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = = V_{IL}		200		250		300		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		350	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60		105		105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

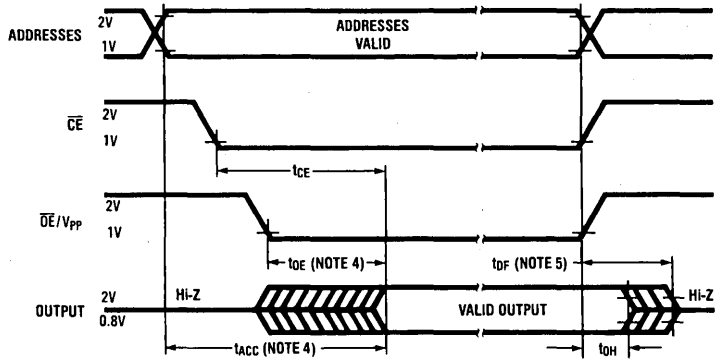
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤20 ns	Inputs	1V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms



TL/D/8754-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

CL: 100 pF includes fixture capacitance.

Programming Characteristics

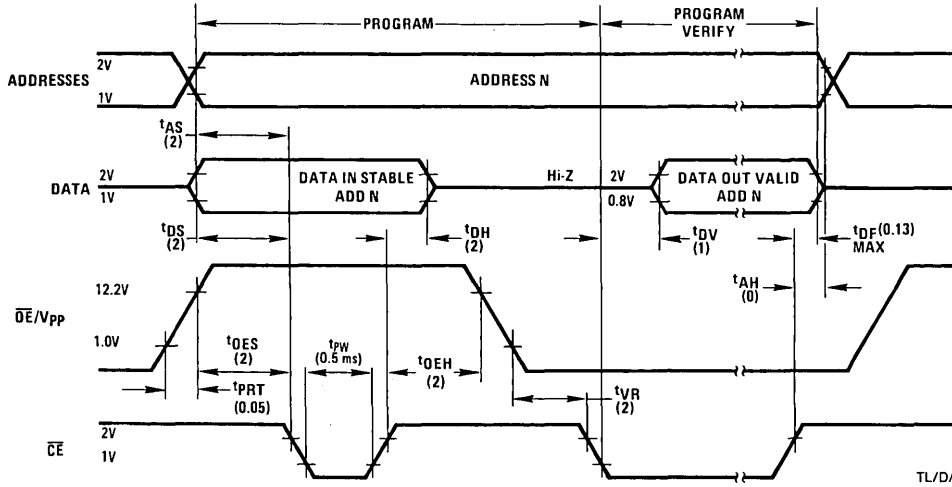
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.2V to 13.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$ = V_{IL}	0		130	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{PP}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}			1	μs
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		2			μs

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.2V to 13.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

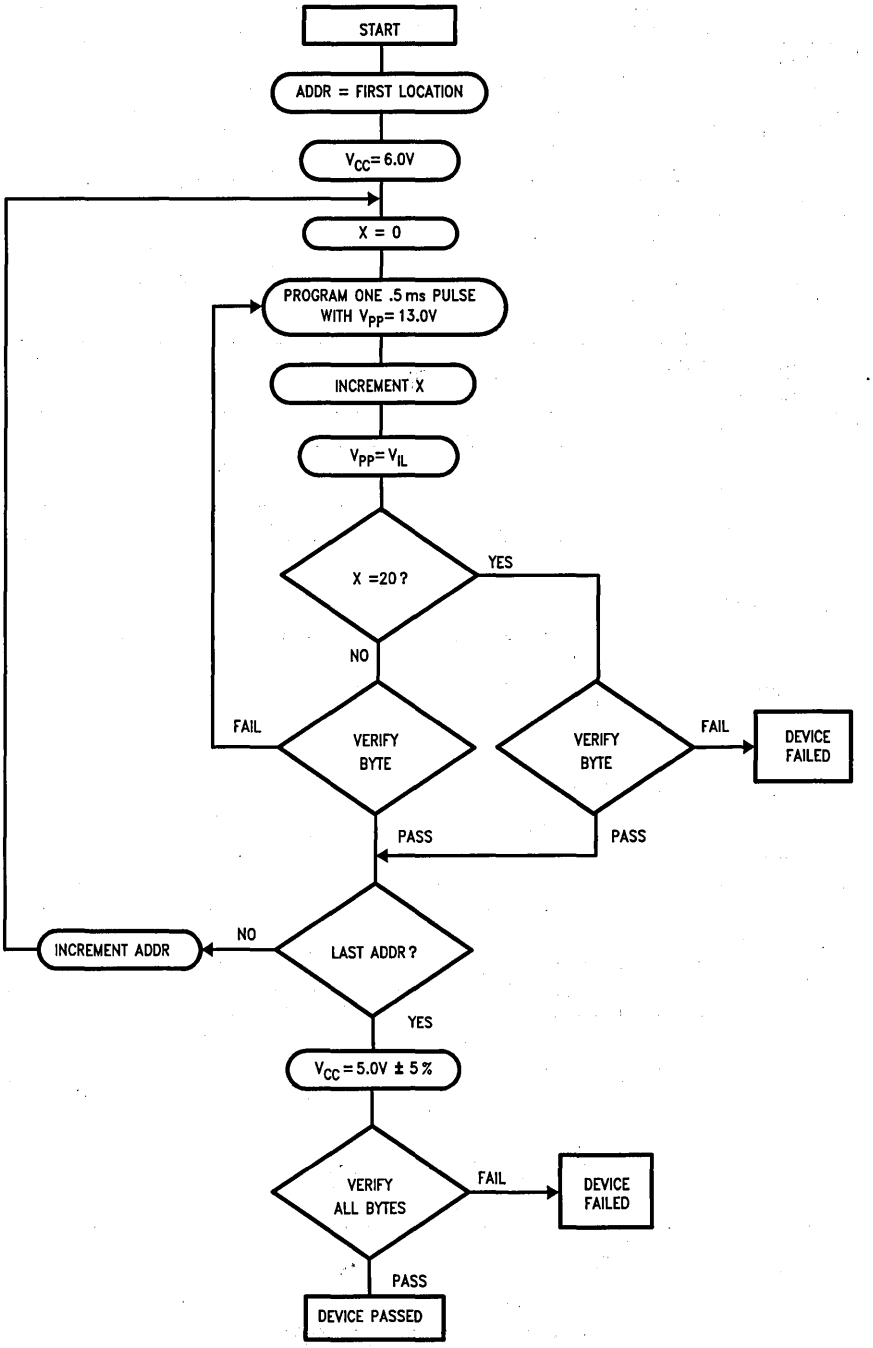
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C512 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

INTERACTIVE PROGRAMMING FLOW CHART



TL/D/8754–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C512 are listed in Table I. It should be noted that all inputs for the five modes may be at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes. The $\overline{OE}/V_{PP}$ pin must be at 13V in the programming mode, and at V_{IL} in the read and verify mode.

Read Mode

The NMC27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C512 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C512s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (V_{PP}) will damage the NMC27C512.

Initially, and after each erasure, all bits of the NMC27C512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512 is in the programming mode when $\overline{OE}/V_{PP}$ is at 13.0V. It is required that at least a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location that is to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C512 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C512 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C512s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C512s.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{PP}	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	6	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	6	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C512s may be common. A TTL low level program pulse applied to an NMC27C512's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 13.0V will program that NMC27C512. A TTL high level $\overline{CE}$ input inhibits the other NMC27C512 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with $\overline{OE}/V_{PP}$ at V_{IL}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C512 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C512 is "8F45", where "8F" designates that it is made by National Semiconductor, and "45" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only posible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C512 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C512 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. Opaque lables should be placed over the NMC27C512's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C512 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C512 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C512 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	1	0	0	0	1	0	1	45

TABLE III. Minimum NMC27C512 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C512A 524,288-Bit (64k x 8) UV Erasable CMOS PROM

General Description

The NMC27C512A is a high-speed 512k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C512A is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

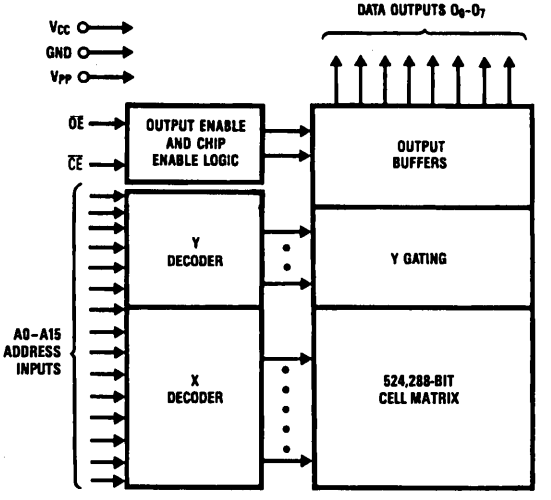
The NMC27C512A is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

These EPROMs are fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 90 ns
- Low CMOS power consumption
  - — Active Power: 220 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800 CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C512AQE120), −40°C to 85°C, and military temperature range (NMC27C512AQM150), −55°C to 125°C, available
- Pin compatible with NMOS 512k EPROMS
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



TL/D/9181-1

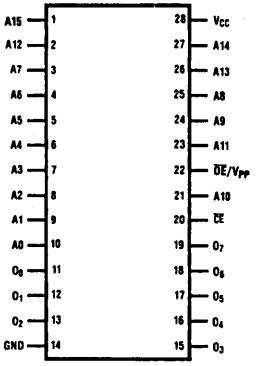
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



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27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}/V_{PP}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Order Number NMC27C512AQ
See NS Package Number J28A-Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C512A pins.

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQ90	90
NMC27C512AQ120	120
NMC27C512AQ150	150
NMC27C512AQ200	200

Extended Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQE120	120

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C512AQM150	150

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages and A9 with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3 to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+13.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

ESD Rating to be determined.

Operating Conditions (Note 7)

V_{CC} Power Supply	5V ±10%
Temperature Range	
NMC27C512AQ90, 120, 150, 200	0°C to +70°C
NMC27C512AQE120	−40°C to +85°C
NMC27C512AQM150	−55°C to +125°C

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHZ All Inputs = V_{IH} or V_{IL} I/O = 0 mA		15	50	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Ouput Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C512A 90		NMC27C512A 120 E120		NMC27C512A 150 M150		NMC27C512A 200		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		40		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	40	0	50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

1

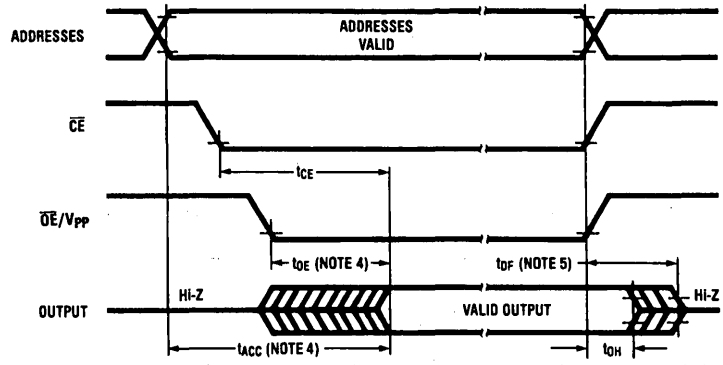
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 9)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms



TL/D/9181–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) −0.10V.

Low to TRI-STATE, the measured V_{OL1} (DC) +0.10V.

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to $V_{CC} + 0.3V$ to avoid latch-up and device damage.

Note 9: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.

CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics

T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5 ±0.3V (Notes 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$ = V_{IL}	0		60	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}$ = V_{IL}			200	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{PP}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

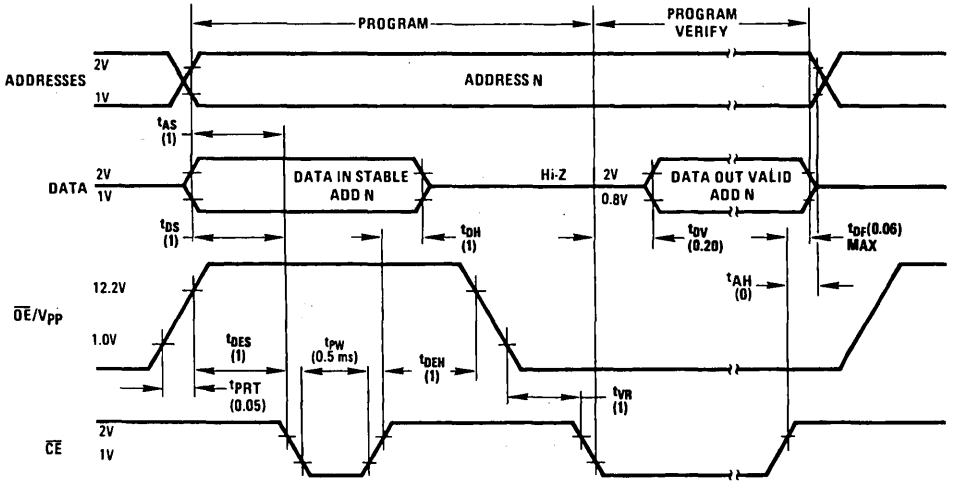
AC Test Conditions

V_{CC}	6V ±0.25V
V_{PP}	12.5 ±0.3V
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

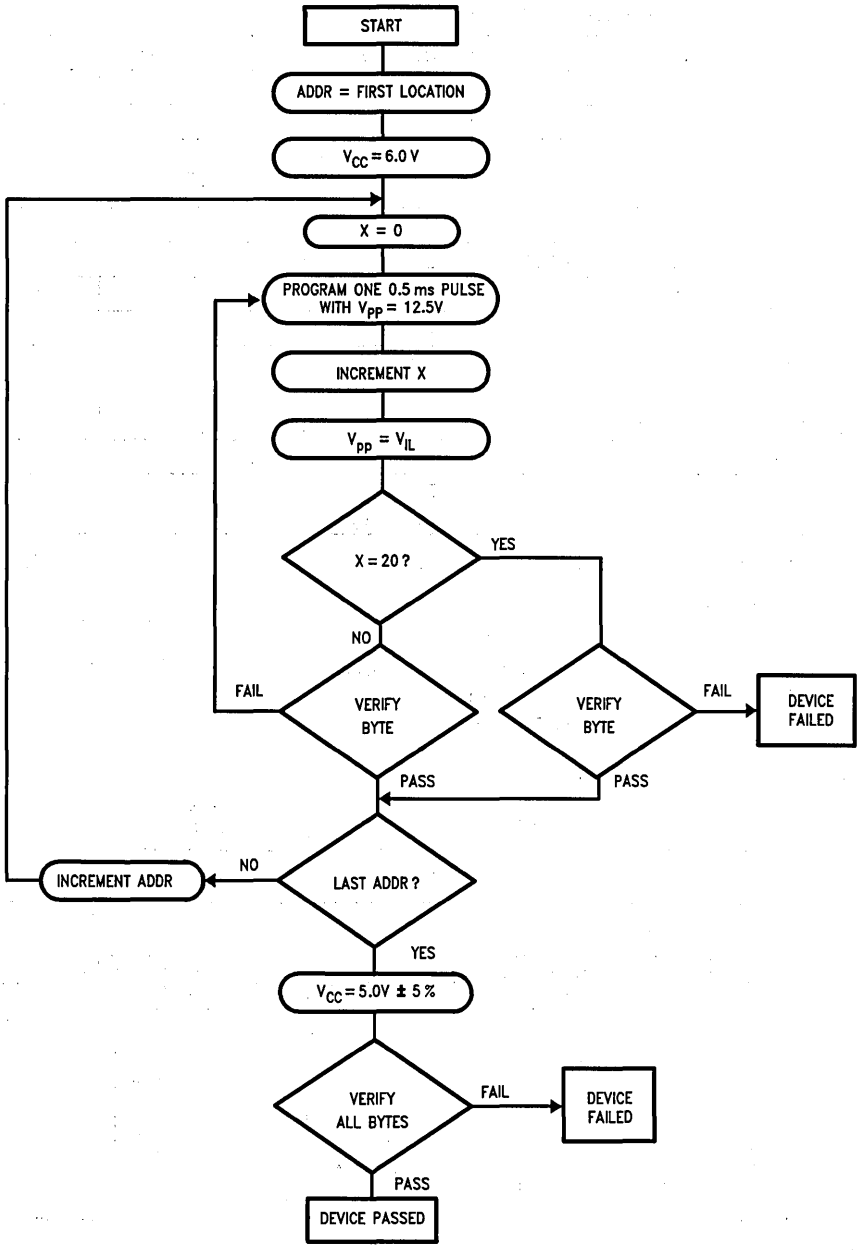
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 13V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/9181–6

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C512A are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.5V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C512A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C512A has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The NMC27C512A is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C512A are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 13V on pin 1 (V_{PP}) will damage the NMC27C512A.

Initially, and after each erasure, all bits of the NMC27C512A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C512A is in the programming mode when the V_{PP} power supply is at 12.5V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{PP}	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	6	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	6	Hi-Z

Functional Description (Continued)

NMC27C512A is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C512A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C512A in parallel with the same data can be easily acccomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C512A may be connected together when they are programmed with the same data. A low level TTL pulse applied; to the $\overline{CE}$ input programs the paralleled NMC27C512A.

Program Inhibit

Programming multiple NMC27C512A in parallel with different data is also easily accomplished. Except $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C512A may be common. A TTL low level program pulse applied to an NMC27C512A $\overline{CE}$ input with V_{PP} at 12.5V will program that NMC27C512A. A TTL high level $\overline{CE}$ input inhibits the other NMC27C512A from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Manufacturer's Identification Code

The NMC27C512A have a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC27C512A is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256k part.

The code is accessed by applying 11.4V to 12.0V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C512A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C512A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. Opaque labels should be placed over the NMC27C512A window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C512A is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C512A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C512A erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IL}	0	0	0	0	0	1	0	0	04

Functional Description (Continued)

TABLE III. Minimum NMC27C512A Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

ADVANCED INFORMATION

microCMOS

NMC27C1023
1,048,576-Bit (128k x 8) UV Erasable CMOS PROM

General Description

The NMC27C1023 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C1023 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over Extended and Military Temperature Ranges.

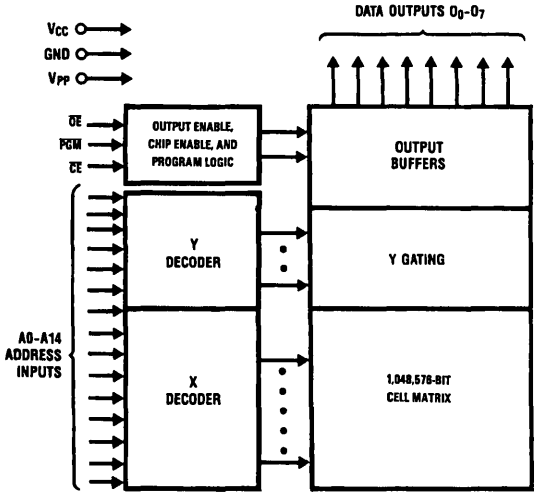
The NMC27C1023 is packaged in a 32-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

These EPROMs are fabricated with National's proprietary, time proven microCOMS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 90 ns
- Low CMOS power consumption
  - — Active Power: 165 mW max
  - — Standby Power: 0.55 mW max
- Performance compatible to NSC800 CMOS microprocessor
- Single 5V power supply
- Extended temperature range (NMC27C1023QE120), −40°C to 85°C and military temperature range (NMC27C1023QM150), −55°C to 125°C, available
- Pin compatible with NMOS bytewide 1024k EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



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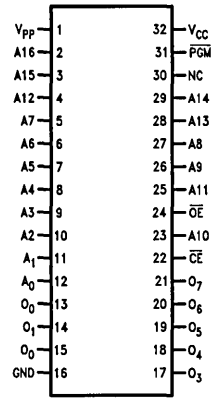
Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C64 2764
A15	V_{PP}	V_{PP}	V_{PP}
A12	A12	A12	A12
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND



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27C64 2764	27C128 27128	27C256 27256	27C512 27512
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$	A14	A14
NC	A13	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Order Number NMC27C1023Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C1023 pins.

Commercial Temperature Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1023Q90	90
NMC27C1023Q120	120
NMC27C1023Q150	150
NMC27C1023Q200	200

Extanded Temp Range (−40°C to +85°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1023QE120	120

Military Temp Range (−55°C to +125°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1023QM150	150

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages and A9 with Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} + 0.3 to GND − 0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+13.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

ESD Rating to be determined.

Operating Conditions (Note 7)

V_{CC} Power Supply	5V ±10%
Temperature Range	
NMC27C1023Q90, 120, 150, 200	0°C to +70°C
NMC27C1023QE120	−40°C to +85°C
NMC27C1023QM150	−55°C to + 125°C

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	60	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	40	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C1023 90		NMC27C1023 120 E120		NMC27C1023 150 M150		NMC27C1023 200		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		40		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	40	0	50		60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

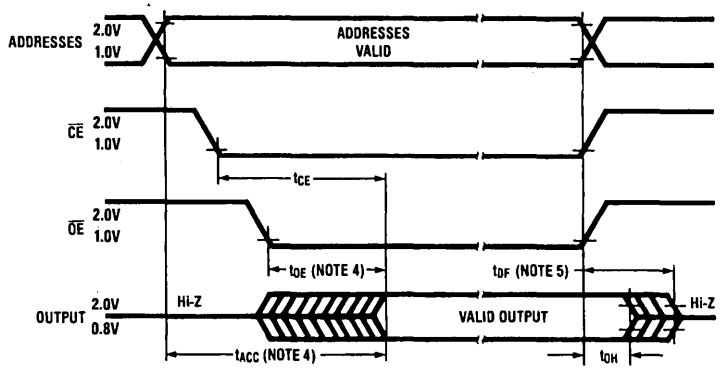
Capacitance T_A = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load C_L = 100 pF	1 TTL Gate and (Note 9)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms



TL/D/9182–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for T_A = +25°C and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{OHZ} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.

C_L: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics

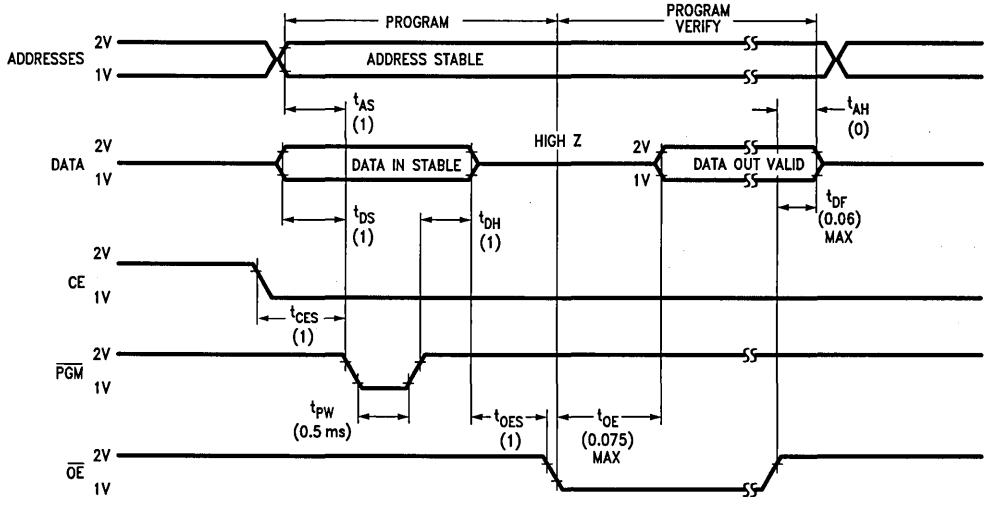
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5 ±0.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		1			μs
t_{OES}	$\overline{OE}$ Set-Up Time		1			μs
t_{DS}	Data Set-Up Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CES}	$\overline{CE}$ Set-Up Time		1			μs
t_{ACC}	Address to Output Delay				200	ns
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$ = V_{IL}	0		60	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}			75	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply During Programming Pulse	$\overline{CE}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Input Pulse Levels	0.45V to 2.4V
V_{PP}	12.5V ±0.3V	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 5 ns	Inputs	1V and 2V
		Outputs	0.8V and 2V

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

T_{OE} and T_{DF} are characteristics of the device but must be accommodated by the programmer.

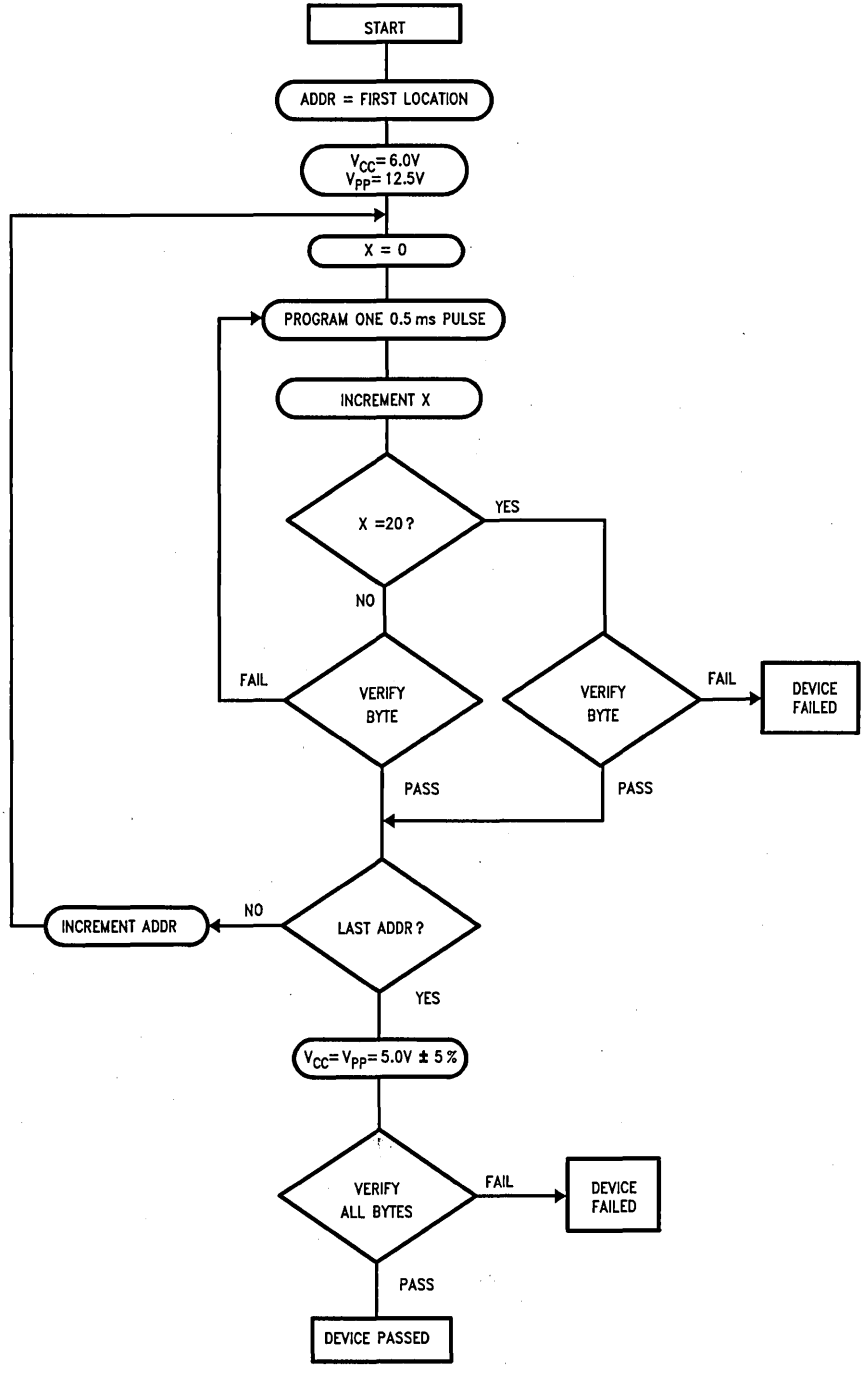
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 13V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/9182-6

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C1023 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.5V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C1023 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C1023 have a standby mode which reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The NMC27C1023 are placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C1023 are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 13V on the V_{PP} or A9 pin will damage the NMC27C1023.

Initially, and after each erasure, all bits of the NMC27C1023 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C1023 is in the programming mode when the V_{PP} power supply is at 12.5V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C1023 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C1023 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C1023 in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C1023 may be connected together when they are programmed with the same data. A low level TTL pulse applied to he $\overline{PGM}$ input programs the paralleled NMC27C1023.

Program Inhibit

Programming multiple NMC27C1023 in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C1023 may be common. A TTL low level program pulse applied to an NMC27C1023 $\overline{PGM}$ input with V_{PP} at 12.5V will program that NMC27C1023. A TTL high level $\overline{CE}$ input inhibits the other NMC27C1023 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Manufacturer's Identification Code

The NMC27C1023 have a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

Functional Description (Continued)

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs (13–15, 17–21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5	Hi-Z
Program	V_{IL}	V_{IH}	⊓	11.5	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	11.5	6	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	11.5	6	Hi-Z

TABLE II. Manufacturer's Identification Code

Pins	A_0 (12)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	1	1	0	86

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C1023 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1Megabit byte-wide part.

The code is accessed by applying 11.4V to 12.0V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C1023 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C1023 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. Opaque labels should be placed over the NMC27C1023 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C1023 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C1023 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C1023 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designe)—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE III. NMC27C1023 Minimum Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C1024
1,048,576-Bit (64k x 16) UV Erasable CMOS PROM

General Description

The NMC27C1024 is a high-speed 1024k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C1024 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

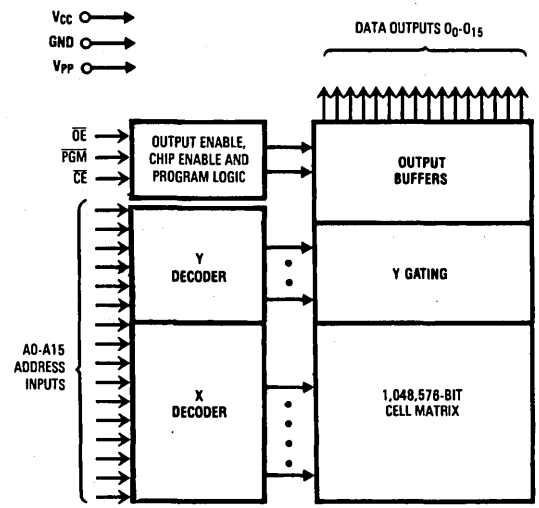
The NMC27C1024 is packaged in a 40-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 90 ns
- Low CMOS power consumption
  - — Active Power: 275 mW max
  - — Standby Power: 550 μW max
- Performance compatible to 16-bit and 32-bit microprocessors
- Single 5V power supply
- Extended temperature range (NMC27C1024QE120), −40°C to +85°C, and military temperature range (NMC27C1024QM150), −55°C to +125°C, available
- Pin compatible with NMOS wordwide 1024k EPROMs
- Fast and reliable programming (0.5 ms for most bytes)
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output

Block Diagram



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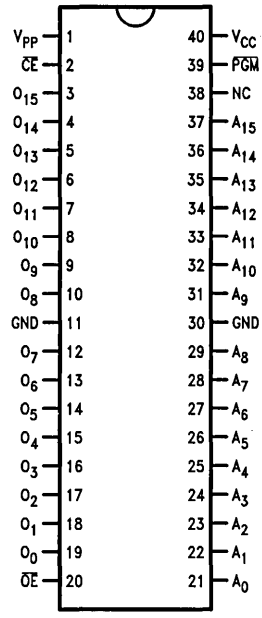
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
$\overline{PGM}$	Program
NC	No Connect

Connection Diagram

Dual-In-Line Package



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Order Number NMC27C1024Q
See NS Package Number J40A

Commercial Temp Range (0°C to +70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C1024Q90	90
NMC27C1024Q120	120
NMC27C1024Q150	150
NMC27C1024Q200	200

V_{CC} = 5V ±10% Extended Temperature (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)
NMC27C1024QE120	120

V_{CC} = 5V ±10% Military Temperature Range (−55°C to +125°C)

Parameter/Order Number	Access Time (ns)
NMC27C1024QM150	150

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages except A9 Respect to Ground	+6.5V to −0.6V
All Output Voltages with Respect to Ground	V_{CC} +0.3 to GND−0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground	+13.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Operating Conditions (Note 7)

Temperature Range	
NMC27C1024Q90, 120, 150, 200	0°C to +70°C
NMC27C1024QE120	−40°C to +85°C
NMC27C1024QM150	−55°C to +125°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 10)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		20	70	mA
I_{CC2} (Note 10)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		15	50	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} −0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C1024 90		NMC27C1024 120 E120		NMC27C1024 150 M150		NMC27C1024 200		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		40		50		60		75	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	40	0	40	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

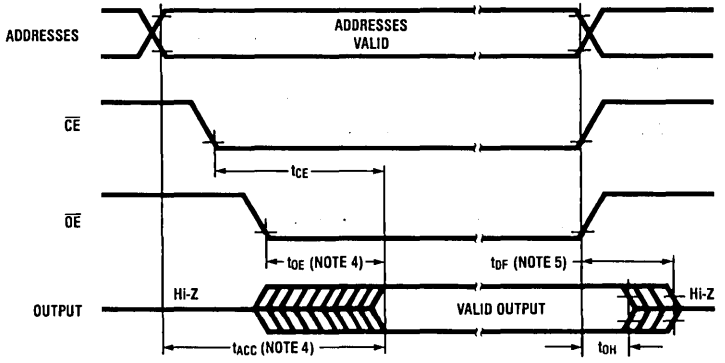
Capacitance $T_A = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	15	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 9)	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 5 ns	Inputs	1V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:

High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V

Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to V_{CC} +0.3V to avoid latch-up and device damage.

Note 9: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
CL: 100 pF includes fixture capacitance.

Note 10: V_{PP} may be connected to V_{CC} except during programming.

Programming Characteristics

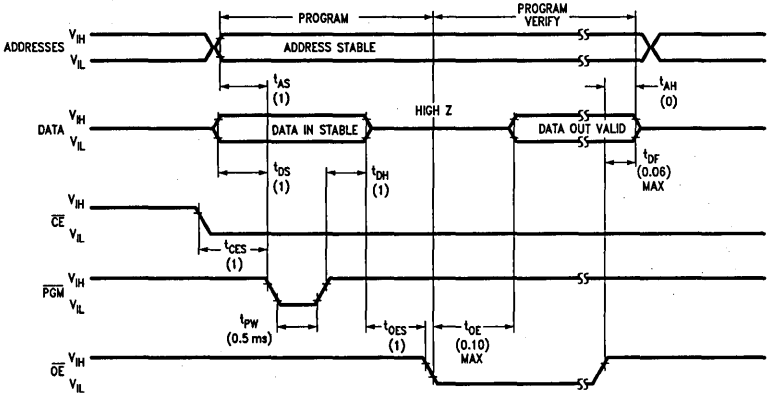
T_A = +25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5 ±0.3V (Notes 2, 3, & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		1			μs
t_{OES}	$\overline{OE}$ Set-Up Time		1			μs
t_{DS}	Data Set-Up Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CES}	$\overline{CE}$ Set-Up Time		1			μs
t_{ACC}	Address to Output Delay				250	ns
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$ = V_{IL}	0		60	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}			100	ns
t_{PW}	Program Pulse Width		0.5	0.5	10	ms
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$ = V_{IL}			30	mA
I_{CC}	V_{CC} Supply Current				10	mA

AC Test Conditions

V_{CC}	6V ±0.25V	Timing Measurement Reference Level	
V_{PP}	12.5V ±0.3V	Inputs	1V and 2V
Input Rise and Fall Times	≤ 20 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

Programming Waveforms (Note 3)



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Note: All times shown in parentheses are minimum and in μs unless otherwise specified. T_{OE} and T_{DF} are characteristics of the device but must be accommodated by the programmer.

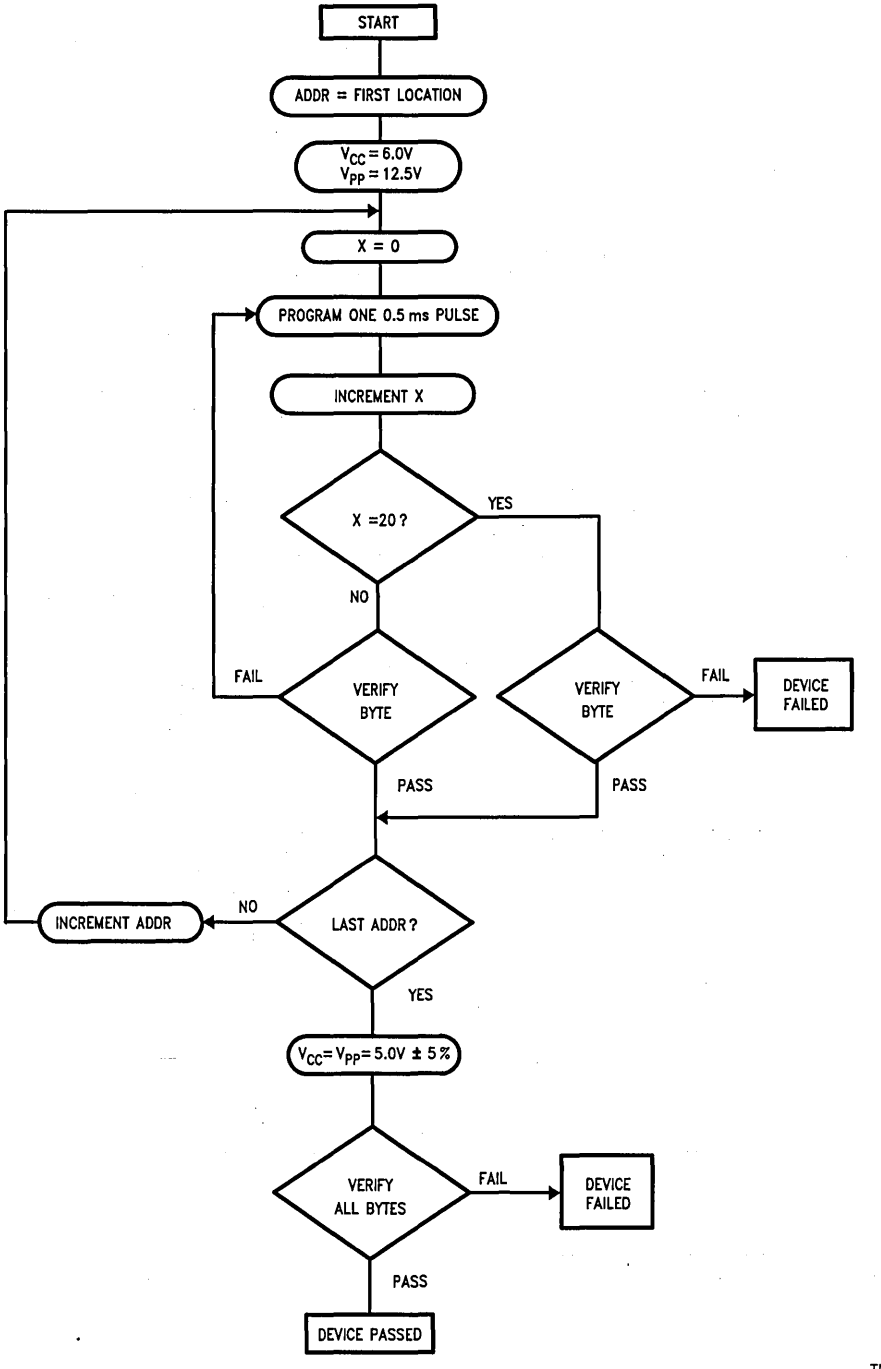
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C1024 must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 13V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 13V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested at nominal power supply voltages.

Interactive Programming Flow Chart



TL/D/8806–5

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C1024 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.5V during the three programming modes, and must be at 5V in the other two modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other two modes.

Read Mode

The NMC27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C1024 has a standby mode which reduces the active power dissipation by over 99.7%, from 275 mW to 0.55 mW. The NMC27C1024 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C1024s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 2) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 13V on the V_{PP} or A9 pin will damage the NMC27C1024.

Initially, and after each erasure, all bits of the NMC27C1024 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C1024 is in the programming mode when the V_{PP} power supply is at 12.5V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the PGM input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27C1024 is designed to be programmed in either of two ways: single pulse programming, where each address is programmed with a 10 ms pulse; or interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Only the interactive programming method has been tested. The NMC27C1024 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C1024s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel NMC27C1024s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C1024s.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	V_{PP} (1)	V_{CC} (40)	Outputs (3-10, 12-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	V_{CC}	5	Hi-Z
Program	V_{IL}	V_{IH}	⊓	12.5	6	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.5	6	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	12.5	6	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C1024s may be common. A TTL low level program pulse applied to an NMC27C1024's $\overline{CE}$ input with V_{PP} at 12.5V will program that NMC27C1024. A TTL high level $\overline{CE}$ input inhibits the other NMC27C1024s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.5V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Manufacturer's Identification Code

The NMC27C1024 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NMC27C1024 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Meg part.

The code is accessed by applying 11.4V to 12.0V to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C1024 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C1024 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. Opaque labels should be placed over the NMC27C1024s window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C1024 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C1024 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C1024 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

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The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk, capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (21)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	1	0	1	1	0	D6

TABLE III. Minimum NMC27C1024 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C49 65, 536-Bit (8k x 8) UV Erasable CMOS PROM (Very High Speed Version) Pin Compatible with 64k Bipolar PROMS

General Description

The NMC27C49 is a high-speed 64k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C49 is designed to operate with a single +5V power supply with ±10% tolerance.

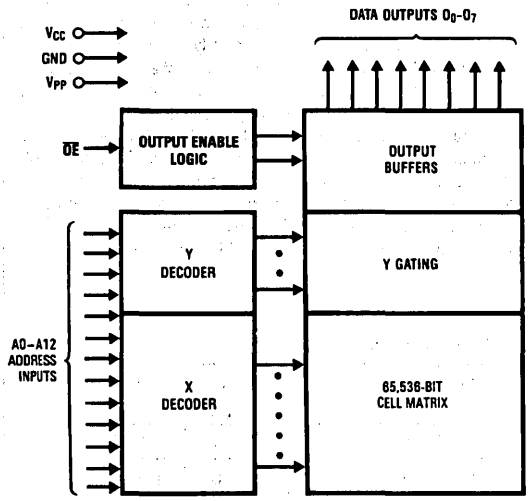
The NMC27C49 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory call is used for speed enhancement.

Features

- Access time down to 45 ns. Two transistor memory cell
- Low CMOS power consumption
  —Active Power: 360 mW max
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with 64k Bipolar PROMS

Block Diagram

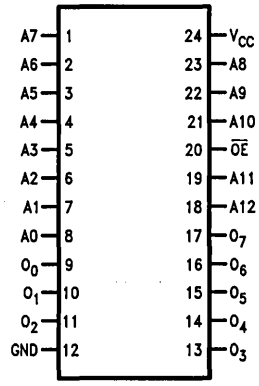


TL/D/9186-1

Pin Names

A0–A12	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Dual-In-Line Package



TL/D/9186-2

Order Number NMC27C49Q
See NS Package Number J24AQ

Commercial Temp Range (0°C to 70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C49Q45	45
NMC27C49Q55	55
NMC27C49Q70	70

National Semiconductor Corporation

PRELIMINARY

microCMOS

NMC27C51 131,072-Bit (16k x 8) UV Erasable CMOS PROM (Very High Speed Version) Pin Compatible With 128k Bipolar PROMs

General Description

The NMC27C51 is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C51 is designed to operate with a single +5V power supply with ±10% tolerance.

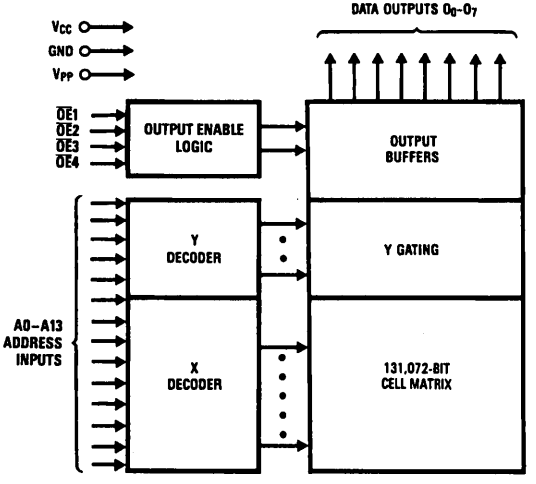
The NMC27C51 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven microCMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability. A two transistor memory cell is used for speed enhancement.

Features

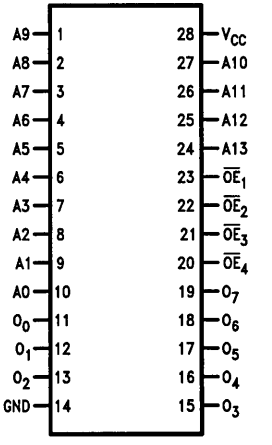
- Access time down to 45 ns, two transistor memory cell
- Low CMOS power consumption
  — Active Power: 360 mW max
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Pin compatible with 128k Bipolar PROMs

Block and Connection Diagrams



TL/D/9184-1

Dual-In-Line Package



TL/D/9184-2

Order Number NMC27C51
See NS Package Number J28AQ

Commercial Temp Range (0°C to 70°C)

V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C51Q45	45
NMC27C51Q55	55
NMC27C51Q70	70

Pin Names

A0–A13	Addresses
$\overline{OE}1$–$\overline{OE}4$	Output Enables
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

CMOS EPROM and SRAM Output Circuit Characteristics

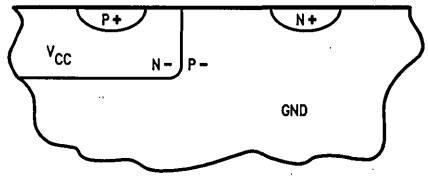
National Semiconductor Corp.
Application Brief 31
Jim Brennan

INTRODUCTION

National offers a selection of Static RAM's and UV erasable PROM's fabricated with microCMOS silicon gate technology. These integrated circuits share the same output driver design; a design that has electrical characteristics different from the usual CMOS output design.

LATCH-UP PRECAUTIONS

The structure of CMOS IC's (*Figure 1.*) intrinsically is similar to the PNPN structure of SCR's. If a junction becomes sufficiently forward-biased, the resulting minority-carrier injection can set off regenerative PNPN firing and thus cause large supply currents (100's of milliamperes) which will pull down V_{CC}.



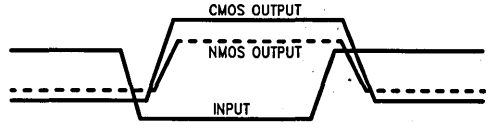
TL/D/9121-1

FIGURE 1

Latch-up cannot occur if the output terminals are prevented from being driven more than 0.5V beyond the supply-voltage range. This is not always possible, particularly when the outputs are attached to a system buss. Therefore, these products were designed utilizing NMOS for both pull-down and pull-up output devices, thus absolutely preventing any possibility of latch-up being induced by output voltages.

CHARACTERISTICS OF NMOS OUTPUT DRIVERS

Figure 2 compares the switching response of a CMOS output and of a NMOS output. Two differences can be observed from the switching waveforms; 1) the CMOS design is faster when switching from low to high, and 2) the output high level (V_{OH}) of the CMOS design is higher.



TL/D/9121-2

FIGURE 2

In a memory system composed of MOS RAM's or EPROM's the load is capacitive and not resistive. *Figure 3* compares the switching response of a CMOS output and NMOS output driving capacitive loads of 10 pF, 50 pF, and 100 pF. The switching waveforms show that the fall times are comparable, but most obvious is the rise time of the CMOS output—much faster than that of the NMOS output.

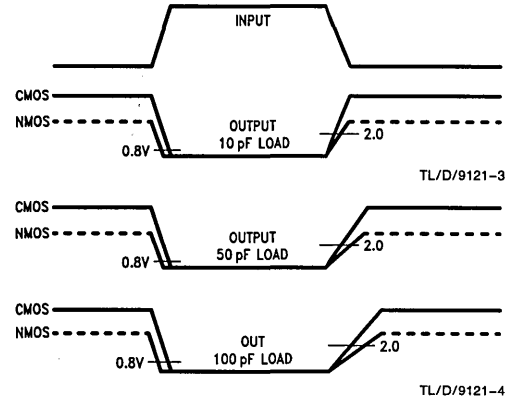


FIGURE 3. Switching Response with Capacitive Load

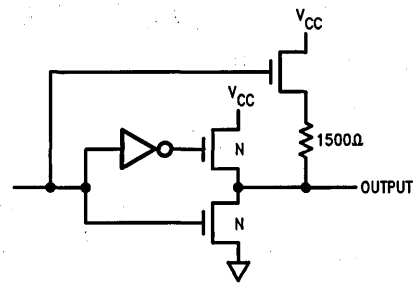
The high and low voltage levels of the CMOS output design are directly set by the supply-voltage, V_{CC} and GND. However, for the NMOS output design, the high level is approximately one-threshold voltage lower than V_{CC}. The low level is at GND, same as the CMOS design. It is this difference that accounts for the noticeable changes in the memory access time as the supply-voltage, operating temperature and output capacitance loading are varied. This is of no significant consequence, since the memory access times are guaranteed (by testing) at the worst-case conditions.

ACTUAL OUTPUT DESIGN

Measurement of the DC output levels on these integrated circuits would lead to the conclusion that the output design is CMOS. Measurement of the switching times under varing capacitance loads and supply voltage would lead to the conclusion that the output design is NMOS.

Both conclusions are correct!

The output design, shown in *Figure 4*, uses NMOS for both the pull-down and pull-up devices. These devices give sufficient current source or sink capability to achieve desired memory access times under maximum specified capacitance loading while preventing latch-up possibilities. In order to give a higher output level (V_{OH}) for CMOS system compatibility, a PMOS device is also included in parallel with the NMOS pull-up device. Latch-up is prevented by the isolation of the output terminal from the PMOS device by a 1500Ω polysilicon resistor.



TL/D/9121–5

FIGURE 4. Actual Output Design

For a list of EPROM products utilizing this output design, refer to AN472, Programming National UV EPROMs.

Programming National UV EPROMs

National Semiconductor Corp.
Application Note 472
Merrill Johnson

INTRODUCTION

National Semiconductor is a broad-based supplier of low power CMOS EPROMs. CMOS EPROMs are programmed the same way NMOS EPROMs are programmed. CMOS and NMOS EPROMs are pin compatible in programming mode and in read mode. National EPROMs are superior to most competitive EPROMs on the market because the power drain is much lower with the CMOS process and also the access time is faster due to the clocked sense amp design. The parts are designed to interface with CMOS and TTL circuitry. Table I is a quick reference index for NSC CMOS EPROM programming algorithms.

TABLE I. CMOS EPROM Product Line

Density	Device Type	Programming Technique
16k	NMC27C16	25V Single Pulse—50 ms
16k	NMC27C16H	25V Single Pulse—10 ms
16k	NMC27C16B*	13V Interactive Programming 0.5 ms pulses
32k	NMC27C32	25V Single Pulse—50 ms
32k	NMC27C32H	25V Single Pulse—10 ms
32k	NMC27C32B*	13V Interactive Programming 0.5 ms pulses
64k	NMC27C64	13V Interactive Programming 0.5 ms pulses
128k	NMC27CP128	13V Interactive Programming 0.5 ms pulses
256k	NMC27C256	13V Interactive Programming 0.5 ms pulses
512k	NMC27C512*	13V Interactive Programming 0.5 ms pulses

*Future Product

EPROM PROGRAMMERS

The majority of the problems with EPROMs are programming related. The biggest cause of these problems is programmers not being equipped to program specific vendors' devices.

With National's older product lines, 27C16, 27C16H, 27C32, and 27C32H, customers have relatively few programming problems. This is because most 16k and 32k EPROMs on the market are programmed the same way, i.e., each byte in memory is programmed with a single 50 ms pulse, and the V_{PP} programming voltage is 25V. Thus a programmer manufacturer can use one programming routine for most vendor's parts. Furthermore these parts are quite mature and many programmer manufacturers have had time to develop the proper programming routines.

The EPROMs which have recently been introduced by National and other vendors do not have the same inter-company consistancy of the older parts. Different companies have different programming voltages and companies generally have their own unique interactive programming algorithms. Therefore, the EPROM manufacturers have to work directly with the programmer manufacturers to incorporate the proper hardware and programming routines for the specific EPROMs they are building.

The programmer manufacturers who are currently set up to program National EPROMs are listed in Table II. This list will expand significantly in the future as other programmer manufacturers develop the capability. The list does not include those which can program the older 16k and 32k devices because the majority of programmers in the field are capable of programming these parts.

National has evaluated the Data I/O, Stag, and EPRO programmers in-house and verified proper operation. Undoubtedly there are other programmers in the field which work as well.

A user who does not have a programmer which can program National parts can generally find a distributor in close proximity who has a Data I/O programmer. Distributors will usually provide programming service, particularly if the EPROMs were purchased from them.

NATIONAL INTERACTIVE PROGRAMMING ALGORITHM

All National EPROMs listed in Table I, with the exception of the 27C16, 27C16H, 27C32, and 27C32H are programmed with the National interactive programming algorithm, shown in *Figure 1.* A customer can also program with a single pulse of 10 ms. However, this is much slower and the National production testing is only done with the interactive algorithm. In either case the V_{PP} programming voltage must be 12.2V-13.3V. The programming efficiency is a strong function of V_{PP} programming voltage so 13.0V or more is recommended for fast programming.

TABLE II. Programmer Manufacturers with National EPROM Programming Capability

Prgmr. Mnfr.	Model No.	Earliest Software Revision	Product
Data I/O	UniPak 2	V10	27C64, 27CP128, 27C256
	UniPak 2B	V10	27C64, 27CP128, 27C256
	120A/121A	V10	27C64, 27CP128, 27C256
	1000	V03	27C32B, 27C64, 27CP128, 27C256
	1000	V05	27C32B, 27C64, 27CP128, 27C256, 27C512
	201	V01	27C64, 27C256
	280	V01	27C64, 27C256
Epro	124	National	27C64, 27CP128, 27C256, 27C512
Stag	PP 39	10	27C64, 27C256, 27C512
	PP 40	3	27C64, 27C256, 27C512
	PP 41-42	1	27C64, 27C256, 27C512
	ZM2000	24	27C64, 27C256, 27C512

The interactive programming algorithm programs a byte with a 0.5 ms pulse, and then does a verify to determine if that byte was fully programmed. If it was not, the program pulse is repeated and again verified. This is done up to a maximum of 20 times, but most bytes will program with a single pulse. A marginally programmed memory cell will read as unprogrammed if the V_{CC} voltage is high. Thus the verify is done with V_{CC} at 6.0V which is a guardband of the 5.5V maximum operating voltage. This insures that the EPROM memory cells are fully charged. All parts are tested in the production screen and guaranteed to program with a maximum of 20 pulses.

It should be noted that the preliminary data sheets for the 27C64 and 27C256 parts show a programming algorithm with a maximum of 100 pulses and a single pulse program width of 50 ms. These values have been changed to 20 pulses and 10 ms respectively in the 1987 Data Book and the production screening reflects these changes.

MANUFACTURER'S IDENTIFICATION CODE

The 27C32B, 27C64, 27C512, and a later design revision of the 27C256 all have a manufacturer's identification code to aid in programming. The code, shown in Table III, is two bytes wide and it identifies the manufacturer and the device type. The first two digits, designate the manufacturer and the next two digits designate the device type. The first two digits, "8F", designate National Semiconductor as the manufacturer.

The code is accessed by applying 12V to address pin A9. Addresses A1–A8, A10 and above, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at $20 \pm 5°C$.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code. The Data I/O and Stag programmers listed above can operate with or without the code control.

TABLE III. Manufacturer's Identification Code

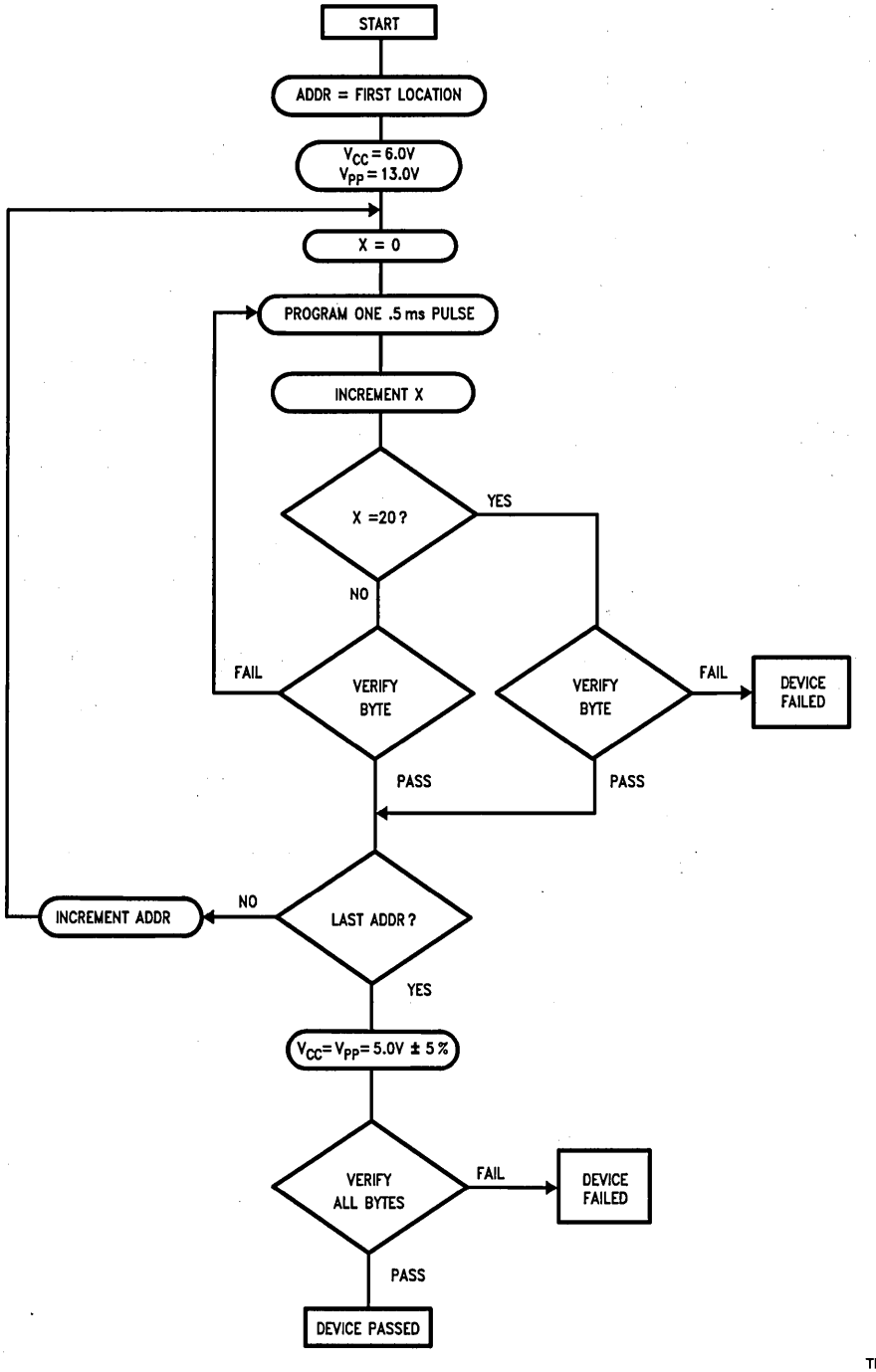
Device Type	Code
27C32B	8F61
27C64	8FC2
27C256	8FC4
27C512	8F45

USING OTHER PROGRAMMERS

If a customer is using a programmer which National has verified to work properly, he should rarely have problems. If he is using another brand and is encountering difficulties he can try to determine the cause. Some of the common problems which have been experienced are discussed here.

V_{CC} and V_{PP} pins must have proper bypassing. High frequency capacitors, typically 0.1 μF, must be placed very close to each EPROM socket shunting V_{CC} and V_{PP} noise to ground. The noise is generated by the EPROM as well as by the system. In the quiescent mode the device draws power supply current in the micro-amp range. The current jumps to several milli-amps when an input transition occurs. This large current change will load down the power supply without proper bypassing. Noise can easily bring the power supply out of specification. The voltage levels should be checked with an oscilloscope so high frequency noise can be detected and also because the power supplies sometimes power down intermittently during programming.

Input voltage levels must also be within specification. (V_{IL} = 0.8V and V_{IH} = 2.0V). Inputs (including data pins) must not have noise transients which cause a polarity change or go beyond the power supply rails. A common problem on inputs is latch-up. If the input voltage level goes above V_{CC} or



TL/D/9120–1

FIGURE 1. Interactive Programming Flow Chart

below ground an SCR latch-up can occur which will either cause the part to malfunction or to be permanently damaged. A small transient of a few ns can trigger latch-up, and the heavy latch-up current will destroy the part if the system does not have proper current limiting. If the problem occurs it will likely happen on the data pins (other inputs can withstand larger transients). Latch-up can be detected by adding high frequency diodes on the suspected pins which will forward bias when the pins go above V_{CC} or below ground. If the problem goes away with the diodes, latch-up is likely its cause.

The EPROM sense amps are clocked for fast access time. This means that V_{CC} must be maintained at operating voltage during verify. If V_{CC} temporarily drops below the specified voltage (but not to ground) an address transition must be performed after the drop to insure proper output data during verify. (If a V_{CC} drop occurs and an address transition is not added, the part can usually be made to verify properly by covering the quartz window.)

EPROM programmers have malfunctioned due to output signals cross-coupling back to input pins. A fast output level change will feed back to an input and cause it to change state, changing the output again, and thus causing oscillations. This problem can be corrected by isolating the outputs from the inputs, stabilizing the inputs, or slowing down the output transition.

Problems can occur if the socket has power applied during device insertion. However hot socket insertion is not as common with programmers now as it has been in the past.

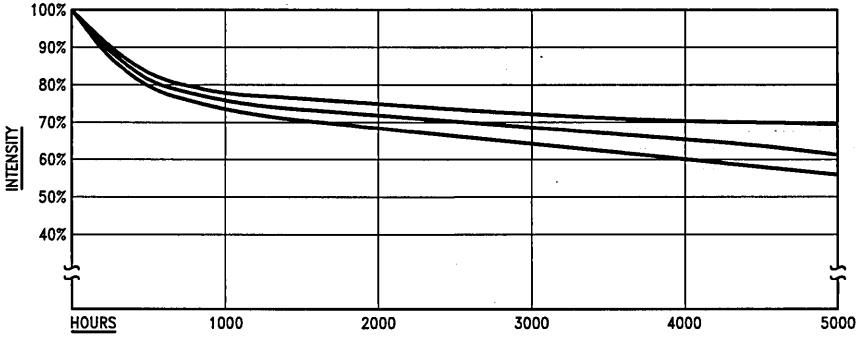
Electro-static discharge, (from the programmer or the operator), can damage parts. This normally happens on input pins and can easily be detected by checking input leakage current, which will be increased if the part has been damaged with a static charge. The production screen accurately tests and guarantees all parts to have less than 10 μa leakage on any input or output pin, and any part with more leakage current has probably seen a static charge.

Some erasure problems can look like a programming problem. If a part is partially erased it will usually be detected during the programmer's initial blank check, but sometimes it will not be detected until the verify after program, or until the part is being read in a system. A partially erased memory cell has some residual charge on the floating gate as opposed to being totally discharged. A low V_{CC} voltage is more sensitive to this residual charge than a high V_{CC} voltage. The initial blank check is typically done at 5.0V V_{CC}, the verify after program is 4.75V, and the part operates in the system down to 4.5V.

National performs a calibrated erase during production screening and guarantees parts will erase with a minimum ultraviolet light dosage of 15W-sec/cm^2 (2537 Angstrom wavelength). This means about 21 minutes in an eraser with a lamp intensity of 12,000 μw/cm^2. Most erasure problems are caused by degradation of light bulbs in the erasure system. Light bulbs lose their intensity with age, as shown in *Figure 2.* After the first 1000 hours of operation the bulbs typically degrade down to about 75% of their original intensity. If the customer does not compensate for this change with increased erasure time he will not give the parts a calibrated erase.

It does not harm an EPROM to over erase for a few hours. Thus, if uncertain about the lamp intensity the safe thing to do is erase two or three times the minimum erase time.

If further help is needed with programming, contact the factory.



TL/D/9120–2

FIGURE 2. Aging Characteristics of Erasure Bulbs

Section 2

EEPROMs

Section 2 Contents

EEPROM Non-Volatile Memory Selection Guide

Part Number	Org.	Size Bits				Power Act/Stby	Temperature
NMC9306	16 x 16	256	8N,	14SO*	SERIAL	10 mA/3 mA	0°C to +70°C
NMC9306E	16 x 16	256	8N		SERIAL	12 mA/4 mA	−40°C to +85°C
NMC9306M	16 x 16	256	8N		SERIAL	14 mA/5 mA	−55°C to +125°C
NMC9307	16 x 16	256	8N		SERIAL	10 mA/3 mA	0°C to +70°C
NMC9307E	16 x 16	256	8N		SERIAL	12 mA/4 mA	−40°C to +85°C
NMC9346	64 x 16	1024	8N,	14SO*	SERIAL	12 mA/3 mA	0°C to +70°C
NMC9346E	64 x 16	1024	8N		SERIAL	14 mA/4 mA	−40°C to +85°C
NMC9346M	64 x 16	1024	8N		SERIAL	15 mA/5 mA	−55°C to +125°C
NMC93CS06	16 x 16	256	8N,	14SO	SERIAL	2.5 mA/0.1 mA	0°C to +70°C
NMC93CS06E	16 x 16	256	8N,		SERIAL	5 mA/0.2 mA	−40°C to +85°C
NMC93CS06M	16 x 16	256	8N,		SERIAL	5 mA/0.2 mA	−55°C to +125°C
NMC93CS26	32 x 16	512	8N,	14SO	SERIAL	2.5 mA/0.1 mA	0°C to +70°C
NMC93CS26E	32 x 16	512	8N,		SERIAL	5 mA/0.2 mA	−40°C to +85°C
NMC93CS26M	32 x 16	512	8N,		SERIAL	5 mA/0.2 mA	−55°C to +125°C
NMC93CS46	64 x 16	1024	8N,	14SO	SERIAL	2.5 mA/0.1 mA	0°C to +70°C
NMC93CS46E	64 x 16	1024	8N,		SERIAL	5 mA/0.2 mA	−40°C to +85°C
NMC93CS46M	64 x 16	1024	8N,		SERIAL	5 mA/0.2 mA	−55°C to +125°C
NMC93CS56	128 x 16	2048	8N,	14SO	SERIAL	2.5 mA/0.1 mA	0°C to +70°C
NMC93CS56E	128 x 16	2048	8N,		SERIAL	5 mA/0.2 mA	−40°C to +85°C
NMC93CS56M	128 x 16	2048	8N,		SERIAL	5 mA/0.2 mA	−55°C to +125°C
NMC93CS66	256 x 16	4096	8N,	14SO	SERIAL	2.5 mA/0.1 mA	0°C to +70°C
NMC93CS66E	256 x 16	4096	8N,		SERIAL	5 mA/0.2 mA	−40°C to +85°C
NMC93CS66M	256 x 16	4096	8N,		SERIAL	5 mA/0.2 mA	−55°C to +125°C
NMC98C10	128 x 8	1024	18N		MUX	10 mA/0.1 mA	0°C to +70°C
NMC98C40	512 x 8	4096	18N		MUX	10 mA/0.1 mA	0°C to +70°C

*Contact factory for SO8 availability.

National Semiconductor Corporation

NMC9306 256-Bit Serial Electrically Erasable Programmable Memory (5V Only)

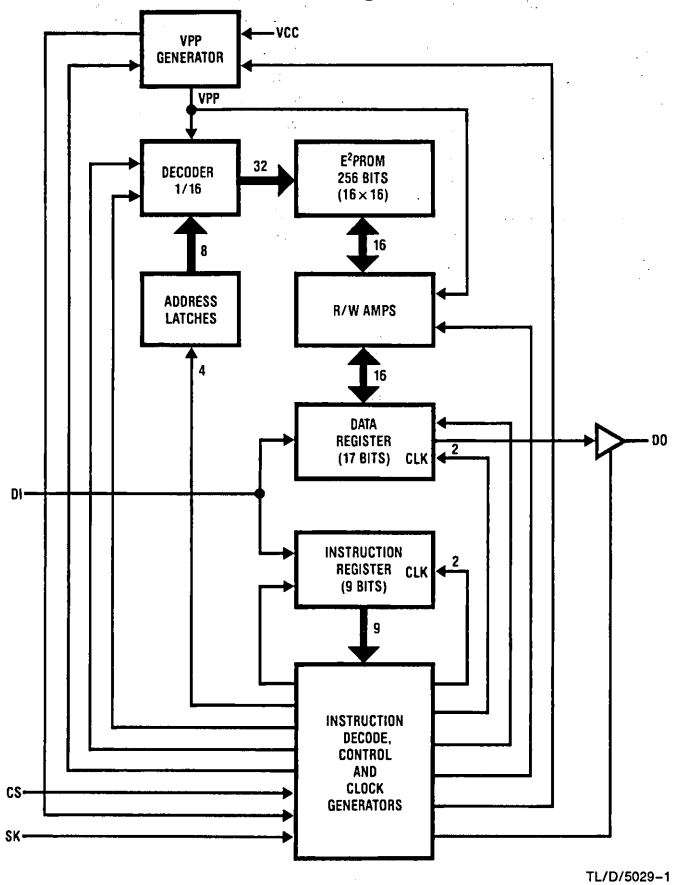
General Description

The NMC9306 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

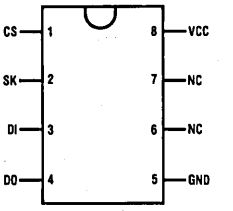
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/5029–1

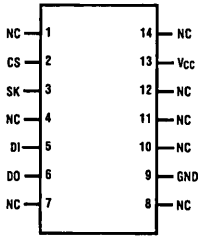
Dual-In-Line Package



TL/D/5029–10

Top View
Order Number NMC9306N
See NS Package Number N08E

SO Package



TL/D/5029–2

Top View
Order Number NMC9306M
See NS Package Number M14B

Note: Contact factory for S08 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9306/COP494	0°C to +70°C
Ambient Storage Temperature	
with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics 0°C ≤TA≤ 70°C, V_{CC}=5V±10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC}=5.5V, CS=1			10	mA
Standby Current (I_{CC2})	V_{CC}=5.5V, CS=0			3	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC}+1	V
Output Voltage Levels					
V_{OL}	I_{OL}=2.1 mA			0.4	V
V_{OH}	I_{OH}=−400 μA	2.4			V
Input Leakage Current	V_{IN}=5.5V			10	μA
Output Leakage Current	V_{OUT}=5.5V, CS=0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL=100 pF				
DO t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V			2	μs
t_{PD0}	V_{IL}=0.45V, V_{IH}=2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

NMC9306/COP494 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9306/COP494 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. after a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

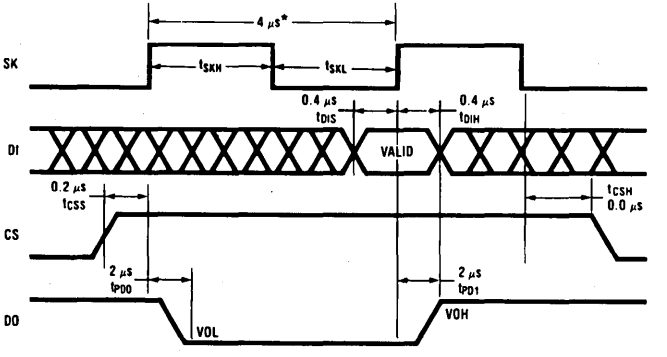
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

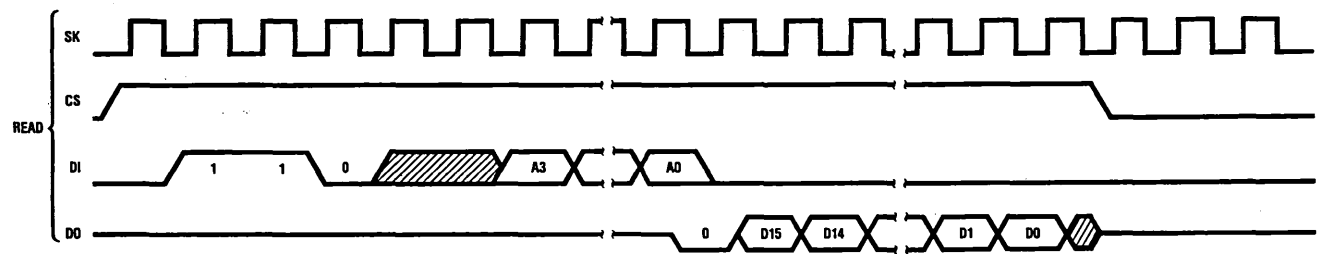
Timing Diagrams



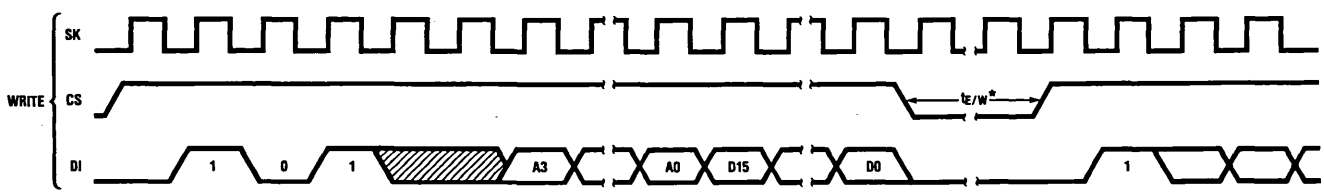
TL/D/5029–3

*This is the minimum SK period

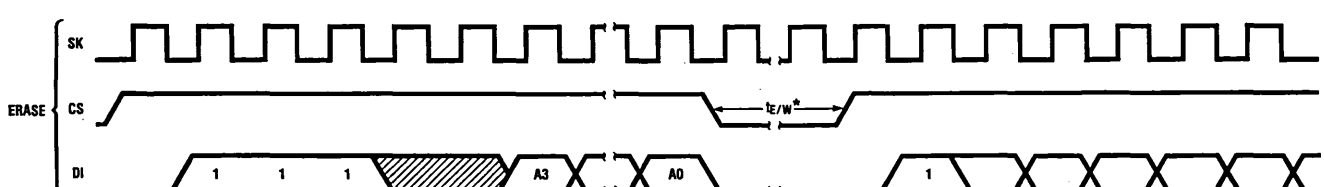
Synchronous Data Timing



TL/D/5029–4



TL/D/5029–5

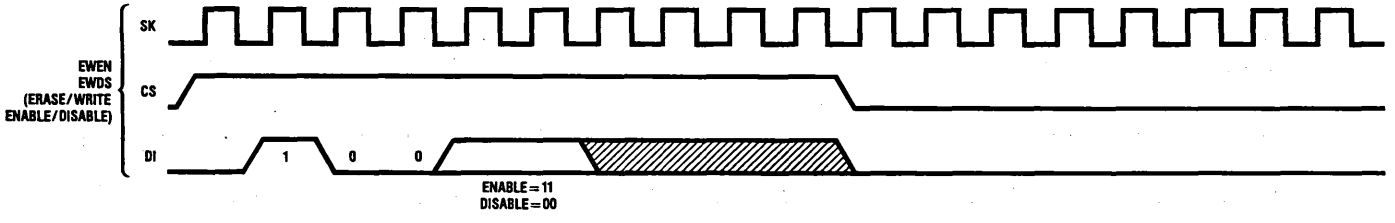


TL/D/5029–6

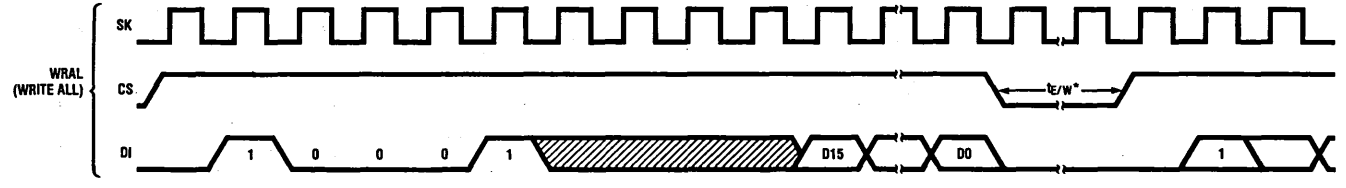
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing

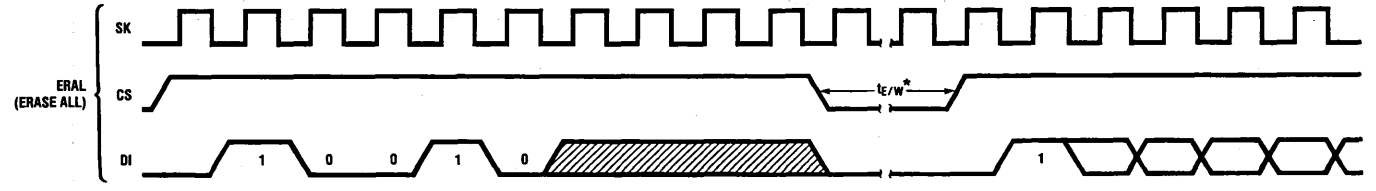
Timing Diagrams (Continued)



TL/D/5029–7



TL/D/5029–8



TL/D/5029–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor Corporation

NMC9306E 256-Bit Serial Electrically Erasable Programmable Memory (5V Only)

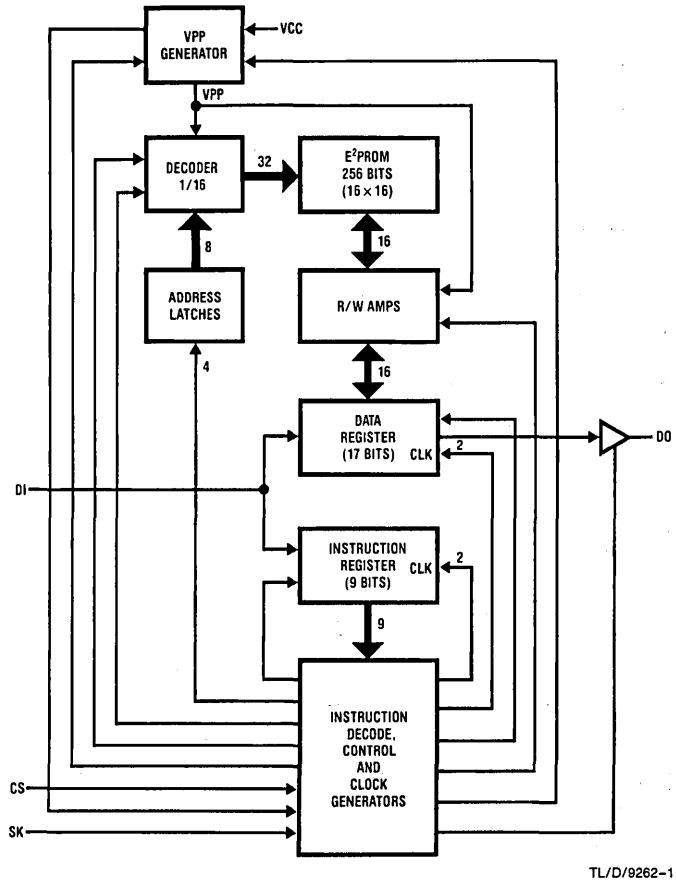
General Description

The NMC9306E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E²PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

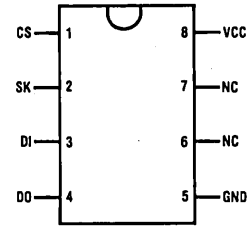
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/9262–1

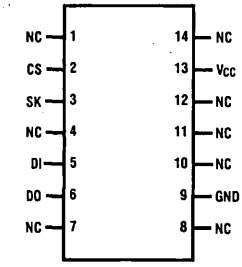
Dual-In-Line Package



TL/D/9262–2

Top View
Order Number NMC9306EN

SO Package



TL/D/9262–3

Top View
Order Number NMC9306EM
See NS Package N08E or M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

2

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9306E	0°C to +70°C
Ambient Storage Temperature	
with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics $-40°C \leq TA \leq +85°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	$V_{CC}=5.5V$, CS=1			12	mA
Standby Current (I_{CC2})	$V_{CC}=5.5V$, CS=0			4	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		$V_{CC}+1$	V
Output Voltage Levels					
V_{OL}	$I_{OL}=2.1$ mA			0.4	V
V_{OH}	$I_{OH}=-400\ \mu A$	2.4			V
Input Leakage Current	$V_{IN}=5.5V$			10	μA
Output Leakage Current	$V_{OUT}=5.5V$, CS=0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL=100 pF				
DO t_{PD1}	$V_{OL}=0.8V$, $V_{OH}=2.0V$			2	μs
t_{PD0}	$V_{IL}=0.45V$, $V_{IH}=2.40V$			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

NMC9306E has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9306E is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

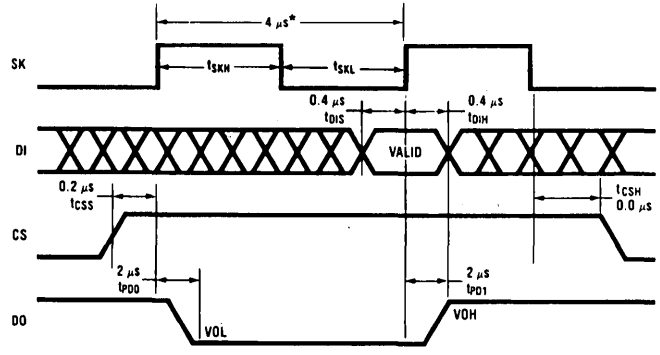
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

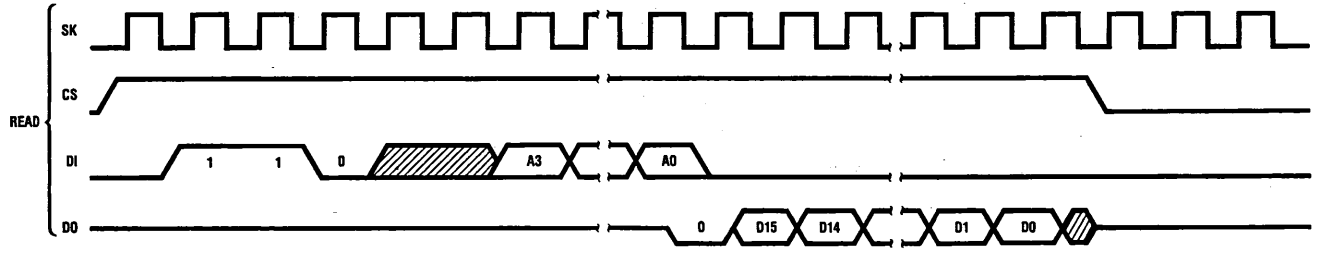


TL/D/9262–4

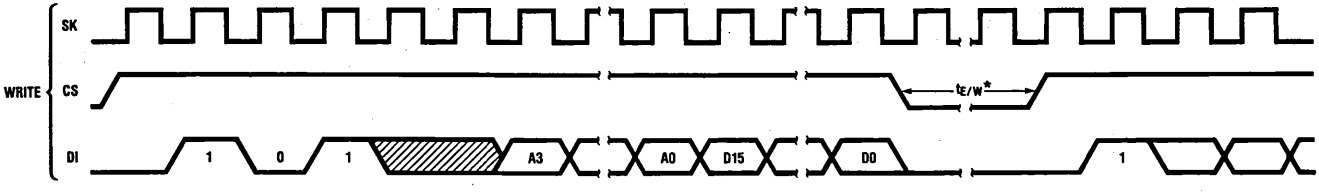
*This is the minimum SK period

Synchronous Data Timing

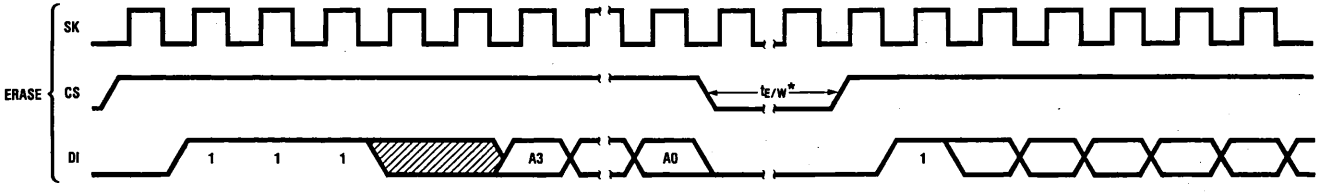
Timing Diagrams (Continued)



TL/D/9262–5



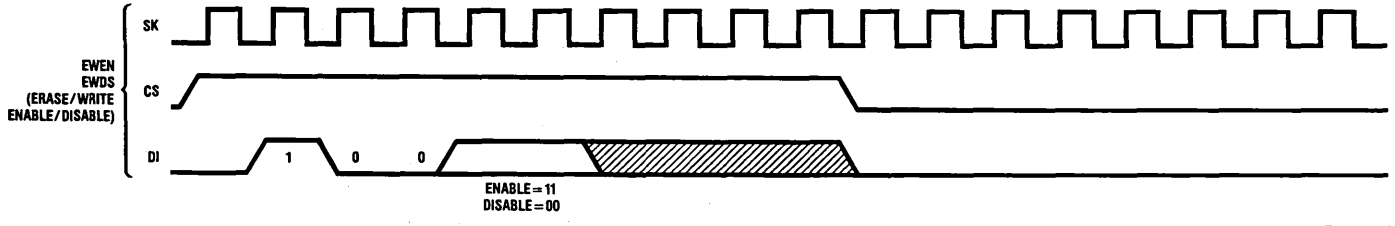
TL/D/9262–6



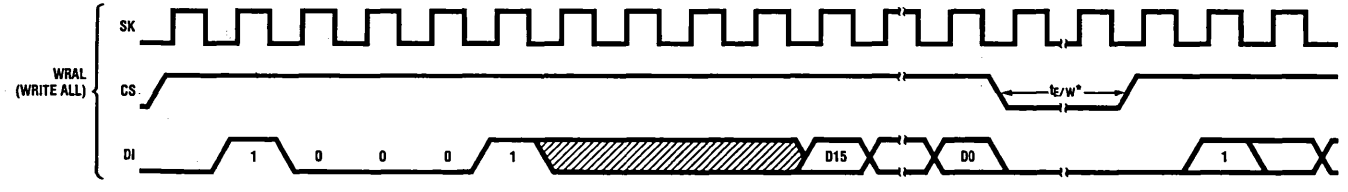
TL/D/9262–7

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

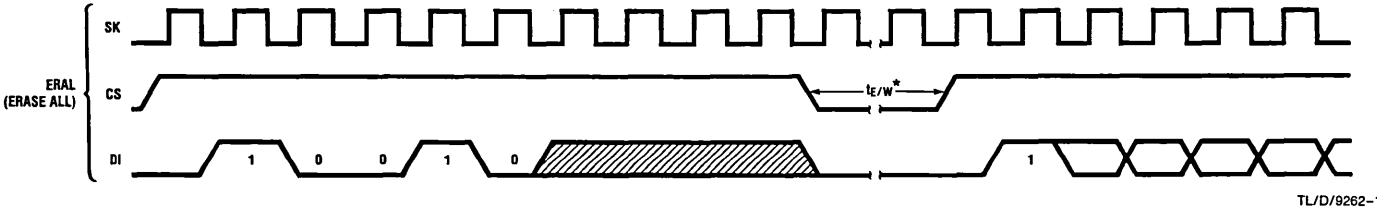
Instruction Timing



TL/D/9262–8



TL/D/9262–9



TL/D/9262–10

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor Corporation

NMC9306MN 256-Bit Serial Electrically Erasable Programmable Memory (Mill. Temp.)

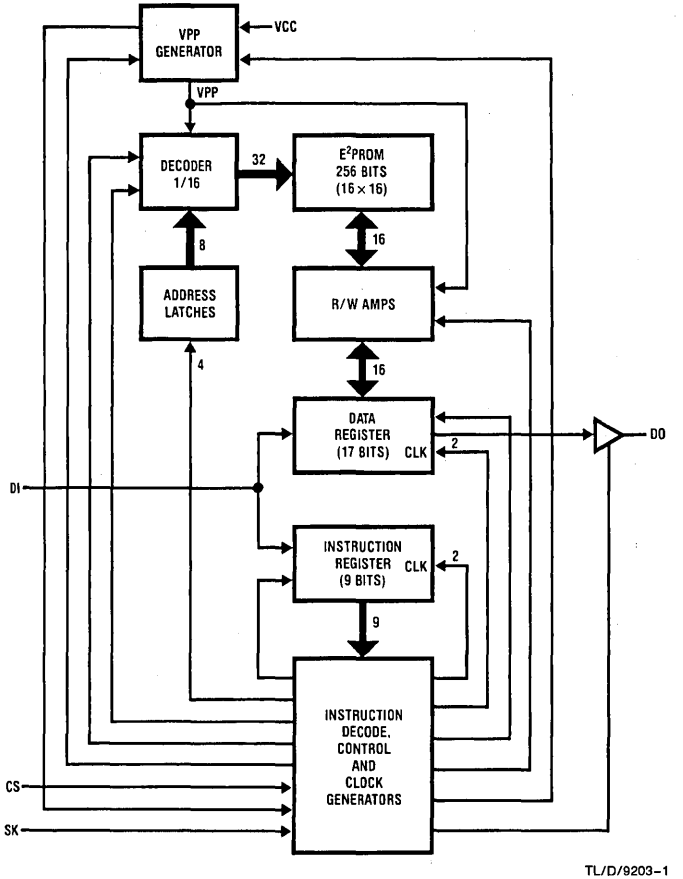
General Description

The NMC9306MN is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306MN has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

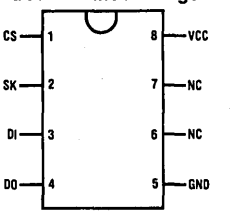
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/9203–1

Dual-In-Line Package



TL/D/9203–2

Top View

Order Number NMC9306MN
See NS Package N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9306MN (Mill. Temp.)	−55°C to +125°C
Ambient Storage Temperature	
with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics −55°C ≤TA≤ +125°C, V_{CC}=5V±10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC}=5.5V, CS=1			14	mA
Standby Current (I_{CC2})	V_{CC}=5.5V, CS=0			5	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC}+0.5	V
Output Voltage Levels					
V_{OL}	I_{OL}=2.1 mA			0.4	V
V_{OH}	I_{OH}=−400 μA	2.4			V
Input Leakage Current	V_{IN}=5.5V			10	μA
Output Leakage Current	V_{OUT}=5.5V, CS=0			10	μA
SK Frequency		0		200	kHz
SK HIGH TIME t_{SKH} (Note 2)		2			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL=100 pF				
DO t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V			2	μs
t_{PD0}	V_{IL}=0.45V, V_{IH}=2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 5 μs. e.g. if t_{SKL} = 2 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

NMC9306MN has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9306MN is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. after a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

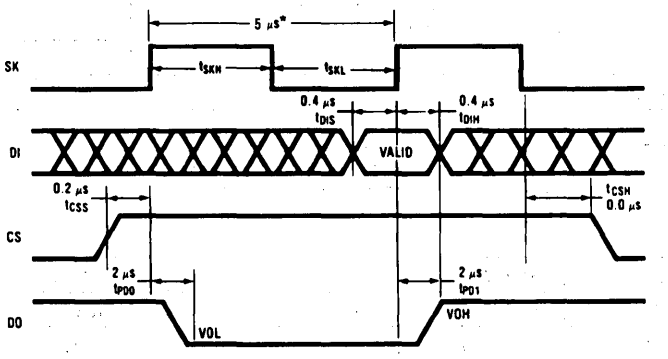
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

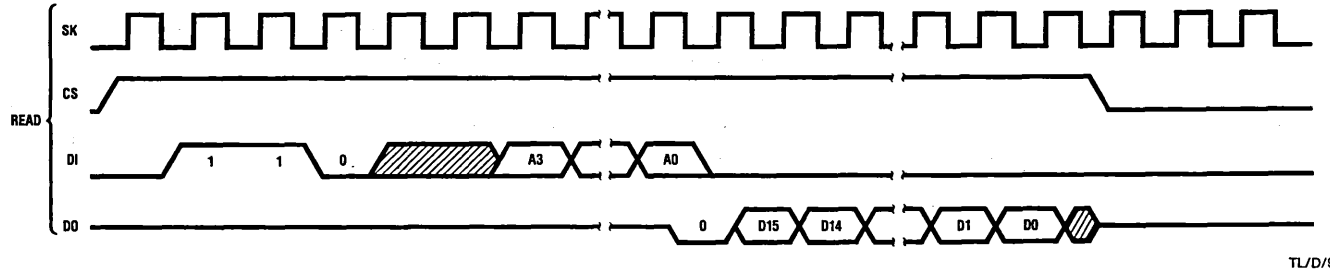
Timing Diagrams



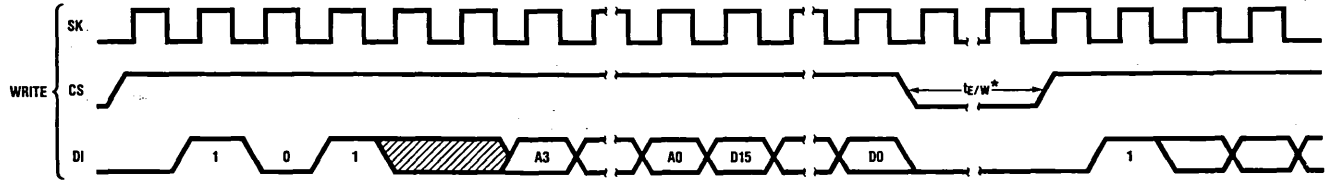
TL/D/9203–3

*This is the minimum SK period

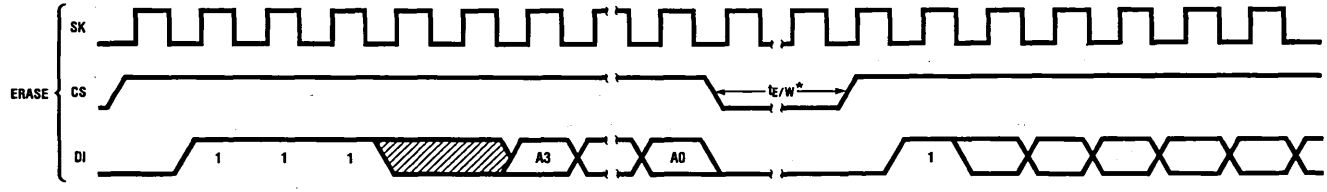
Synchronous Data Timing



TL/D/9203–4



TL/D/9203–5

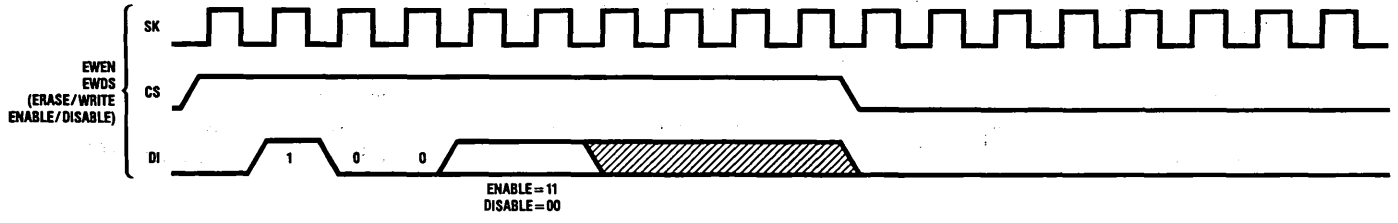


TL/D/9203–6

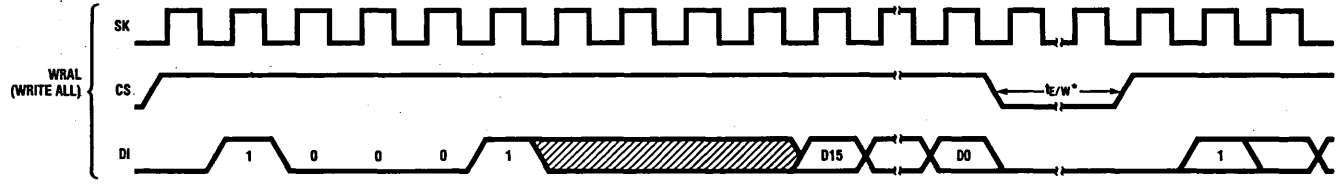
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing

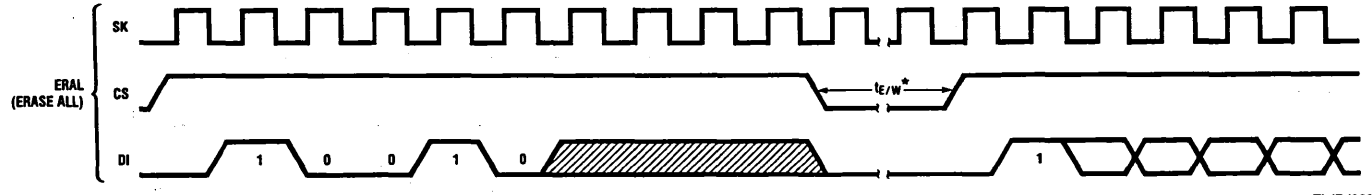
Timing Diagrams (Continued)



TL/D/9203–7



TL/D/9203–8



TL/D/9203–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor Corporation

PRELIMINARY

NMC9307 256-Bit Serial Electrically Erasable Programmable Memory (5V Only)

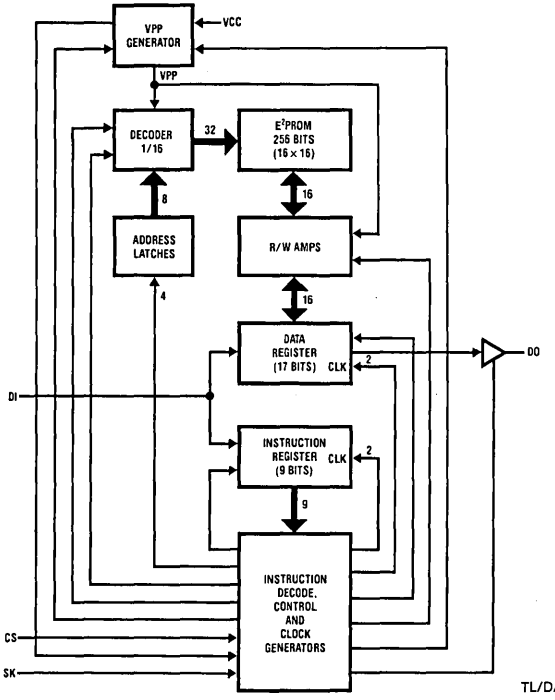
General Description

The NMC9307 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Bulk programming instructions (chip erase, chip write) can be enabled or disabled by the user for enhanced data protection. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9307 has been designed to meet applications requiring up to 10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

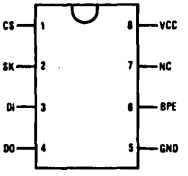
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/9204–1

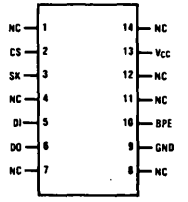
Dual-In-Line Package



TL/D/9204–2

Top View
Order Number NMC9307N
See NS Package Number N08E

SO Package



TL/D/9204–3

Top View
Order Number NMC9307M
See NS Package Number M14B

Note: Contact factory for SO8 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9307	0°C to +70°C
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics 0°C ≤TA≤ 70°C, V_{CC}=5V±10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC}=5.5V, CS=1			10	mA
Standby Current (I_{CC2})	V_{CC}=5.5V, CS=0			3	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC}+1	V
Output Voltage Levels					
V_{OL}	I_{OL}=2.1 mA			0.4	V
V_{OH}	I_{OH}=−400 μA	2.4			V
Input Leakage Current	V_{IN}=5.5V			10	μA
Input Leakage Current	V_{IN}=0 to 5.5V				
PINS 1, 2, 3				±10	μA
PIN 6				±50	μA
Output Leakage Current	V_{OUT}=5.5V, CS=0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL=100 pF				
DO t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V			2	μs
t_{PD0}	V_{IL}=0.45V, V_{IH}=2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

The NMC9307 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9307 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. The NMC9307 is organized as sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. after a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction. The chip erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., data is not changed.

CHIP WRITE (Note 4)

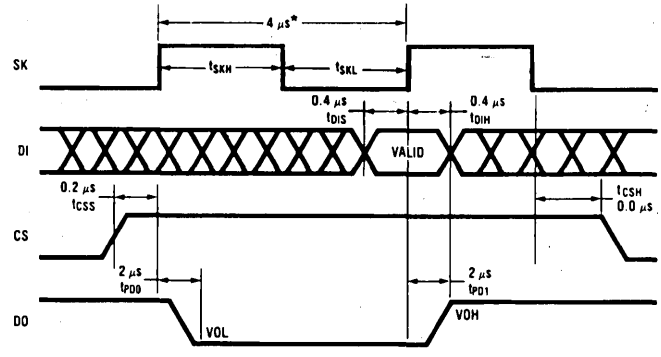
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

The chip write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e., the array data is not changed.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

Synchronous Data Timing

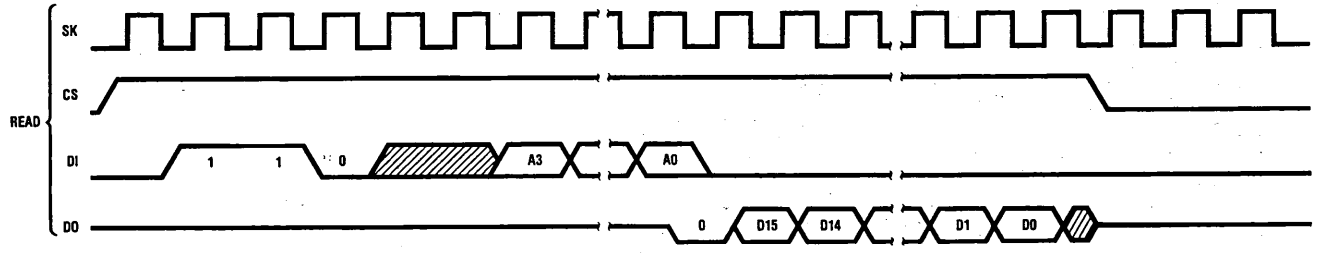


TL/D/9204–4

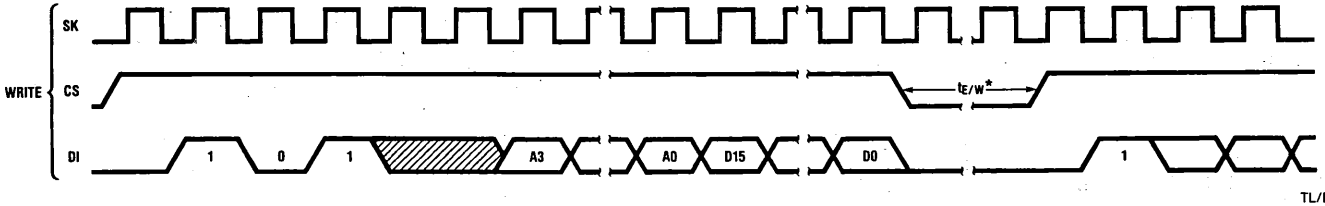
*This is the minimum SK period

Timing Diagrams (Continued)

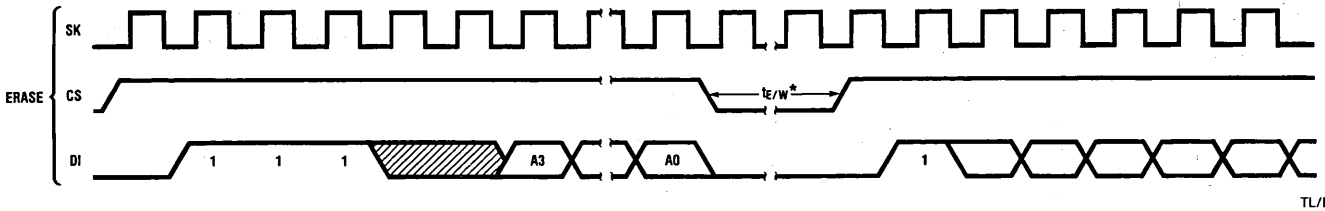
Instruction Timing



TL/D/9204–5



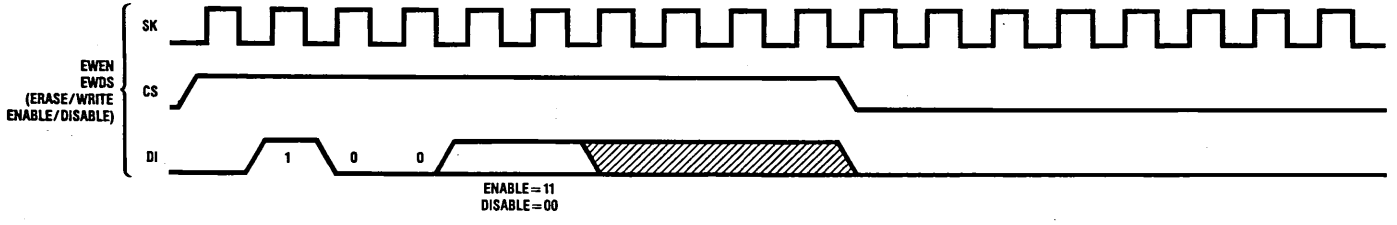
TL/D/9204–6



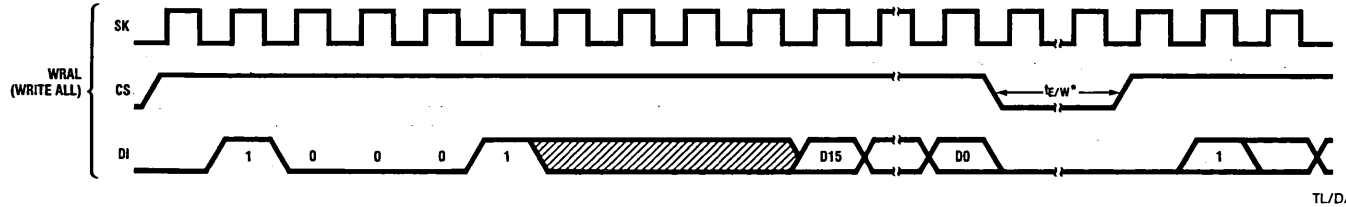
TL/D/9204–7

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

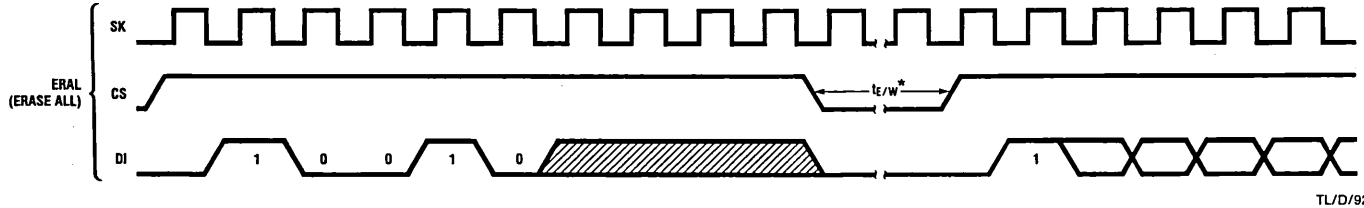
Instruction Timing (Continued)



TL/D/9204–8



TL/D/9204–9



TL/D/9204–10

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

National Semiconductor Corporation

NMC9307E 256-Bit Serial Electrically Erasable Programmable Memory (5V Only)

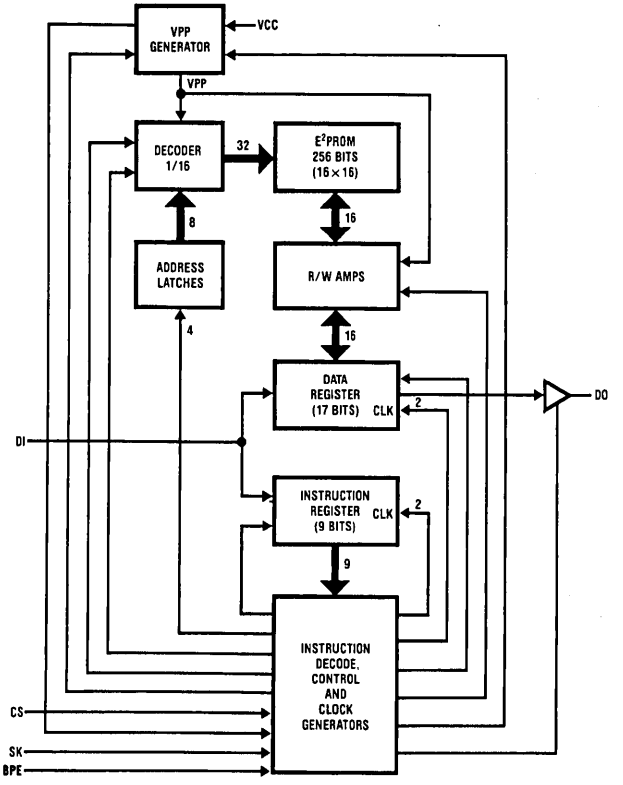
General Description

The NMC9307E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Bulk programming instructions (chip erase, chip write) can be enabled or disabled by the user for enhanced data protection. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9307E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

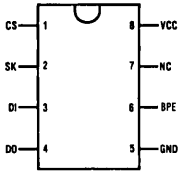
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Bulk programming enable/disable for enhanced data protection

Block and Connection Diagrams



TL/D/8383-1

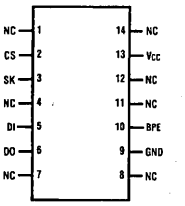
Dual-In-Line Package



TL/D/8383-10

Top View
Order Number NMC9307EN
See NS Package Number N08E

SO Package



TL/D/8383-2

Top View
Order Number NMC9307EM
See NS Package Number M14B

Note 1: Contact factory for SO8 availability.

Note 2: Contact factory for availability of extended temperature SO.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
BPE	Bulk Program Enable
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9307E	−40°C to +85°C
Ambient Storage Temperature	−65°C to +125°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics $-40°C \le TA \le +85°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	$V_{CC} = 5.5V$, $C_S = 1$			12	mA
Standby Current (I_{CC2})	$V_{CC} = 5.5V$, $C_S = 0$			4	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		$V_{CC} + 1$	V
Output Voltage Levels					
V_{OL}	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	$I_{OH} = -400\ \mu A$	2.4			V
Input Leakage Current	$V_{IN} = 0$ to 5.5V				
PINS 1, 2, 3				±10	μA
PIN 6				±50	μA
Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$			2	μs
t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g. if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (tcs) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	BPE	Comments
READ	1	10XX	A3A2A1A0		X	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15–D0	X	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0		X	Erase register A3A2A1A0
EWEN	1	0011	XXXX		X	Erase/write enable
EWDS	1	0000	XXXX		X	Erase/write disable
ERAL (Note 5)	1	0010	XXXX		V_{IH}/OPEN	Erase all registers
WRAL (Note 5)	1	0001	XXXX	D15–D0	V_{IH}/OPEN	Write all registers

NMC9307E has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address of 1 of 16, 16-bit registers.

Functional Description

The NMC9307E is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical '1' before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes he DO pin is in TRI-STATE®, eliminating bus contention.

The bulk programming instructions (ERAL, WRAL) are enabled or disabled by the PBE pin. The BPE pin at V_{IH} enables execution of these instructions. The BPE pin at V_{IL} causes these instructions to be ignored. If the BPE pin is not connected, it is pulled up to V_{CC} by an on-chip pull-up and the bulk programming instructions are enabled. Execution of the EWEN, EWDS, READ and byte programming instructions (ERASE, WRITE) are independent of the state of the BPE pin.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by the low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction. The chip erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

CHIP WRITE (Note 4)

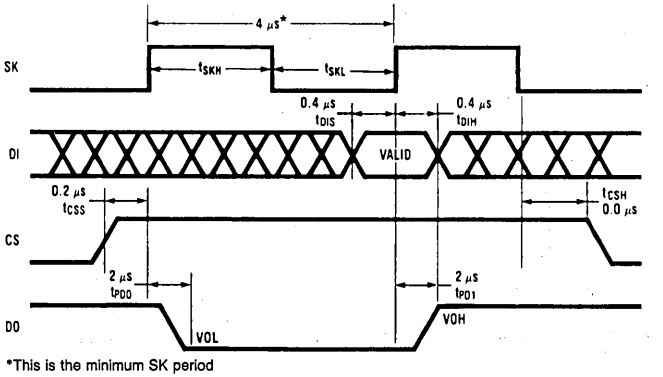
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction. The chip write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e. start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Note 5: The ERAL and WRAL instructions are ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

Timing Diagrams

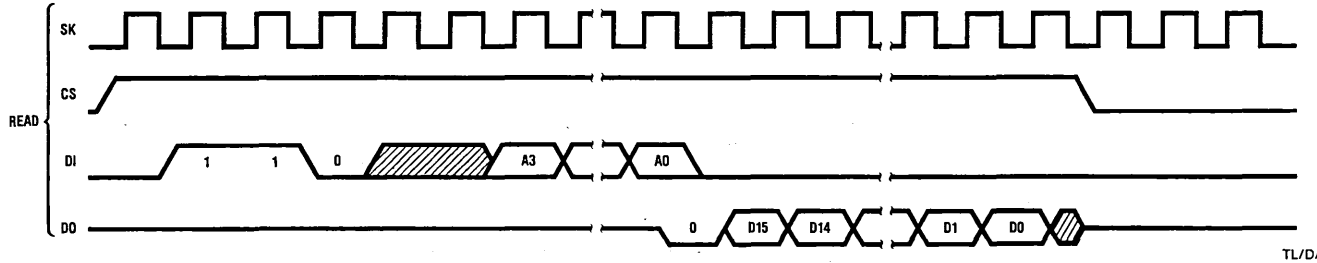
Synchronous Data Timing



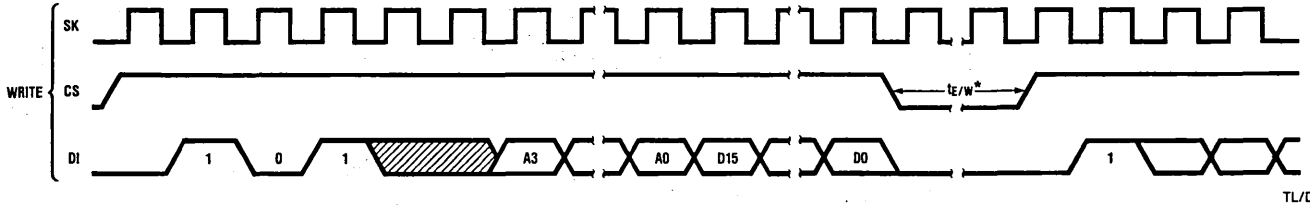
*This is the minimum SK period

TL/D/8383–3

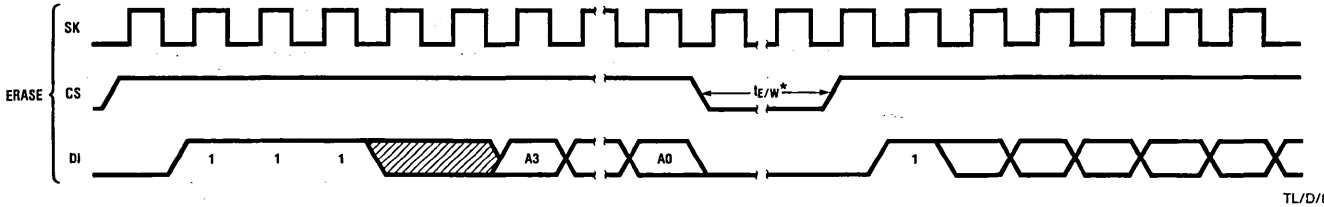
Instruction Timing



TL/D/8383–4



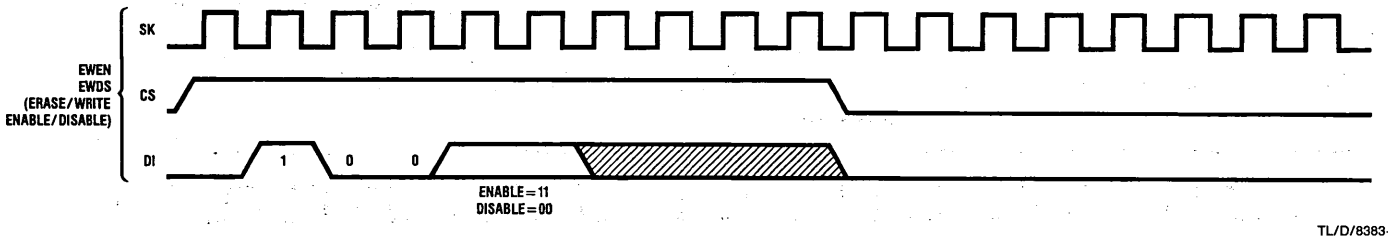
TL/D/8383–5



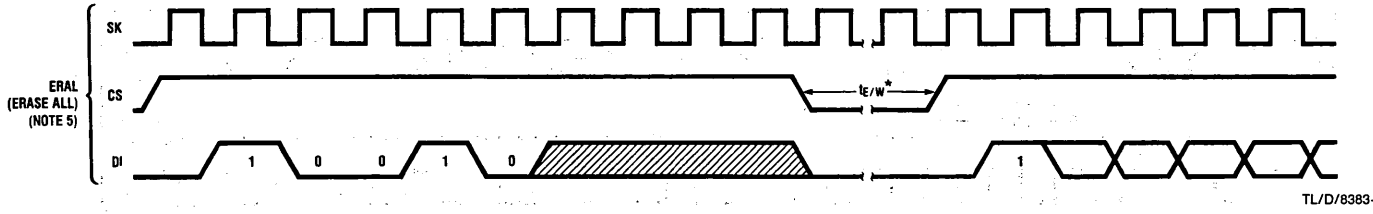
TL/D/8383–6

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

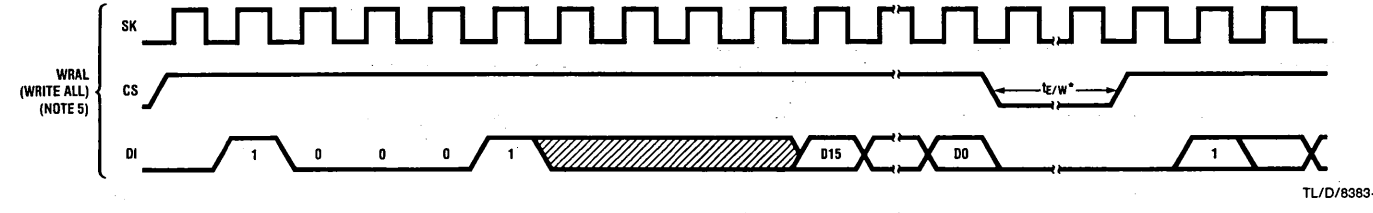
Instruction Timing (Continued)



TL/D/8383–7



TL/D/8383–8



TL/D/8383–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 5: The ERAL and WRAL instructions are ignored if the BPE pin is at VIL, i.e. the array data is not changed.

National Semiconductor Corporation

PRELIMINARY

NMC9346 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

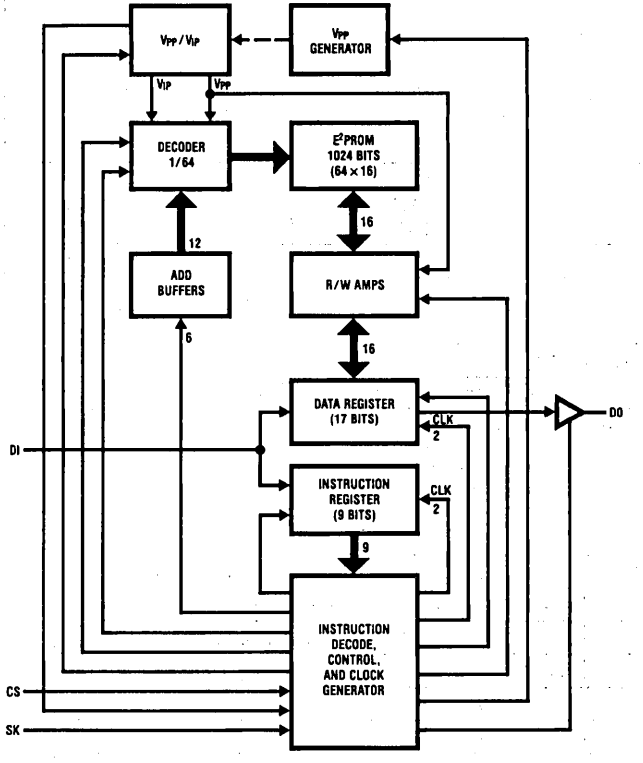
General Description

The NMC9346 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

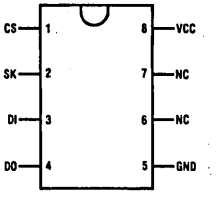
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



TL/D/9205-1

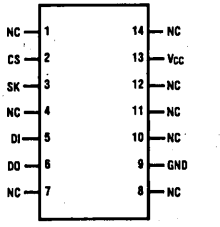
Dual-In-Line Package



TL/D/9205-2

Top View
Order Number NMC9346N
See NS Package Number N08E

SO Package



TL/D/9205-3

Top View

Order Number NMC9346M
See NS Package Number M14B

Note: Contact factory for SO8 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage Relative to GND +6V to −0.3V

Ambient Operating Temperature 0°C to +70°C

Ambient Storage Temp. −65°C to +125°C

Lead Temperature (Soldering, 10 seconds) 300°C

ESD rating is to be determined.

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1 $V_{CC} = 5.5V$		12 12	mA mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+1$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
	SK Frequency		0	250	kHz
t_{SKH}	SK High Time (Note 2)		1		μs
t_{SKL}	SK Low Time (Note 2)		1		μs
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L = 100$ pF			
$t_{pd}1$	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
$t_{pd}0$		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μs
t_{0H}, t_{IH}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g., if $t_{SKL} = 1\ \mu s$ then the minimum $t_{SKH} = 3\ \mu s$ in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9346

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9346 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. The NMC9346 is organized as sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

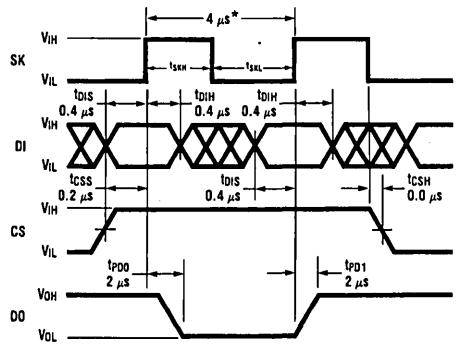
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

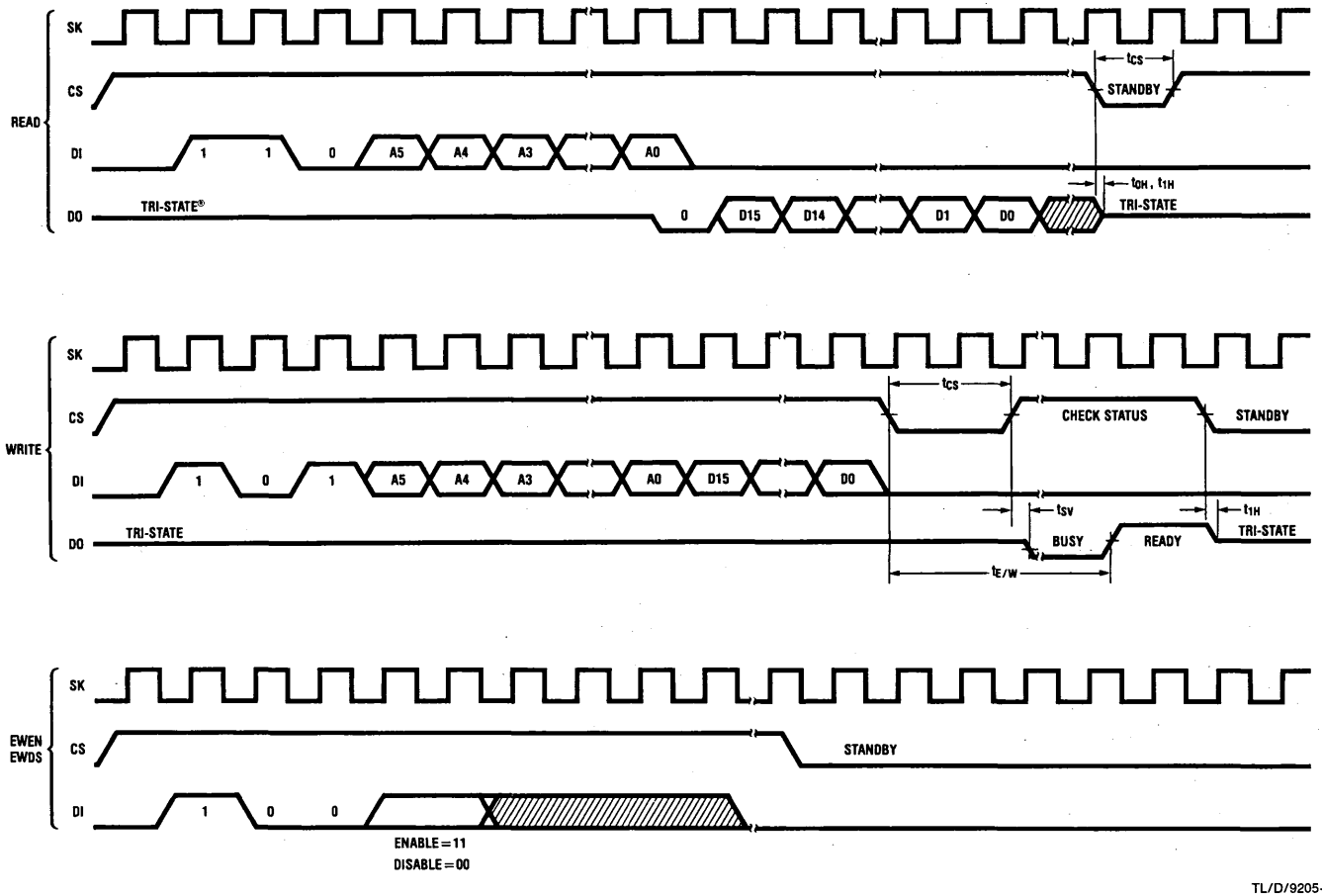
Synchronous Data Timing



TL/D/9205–4

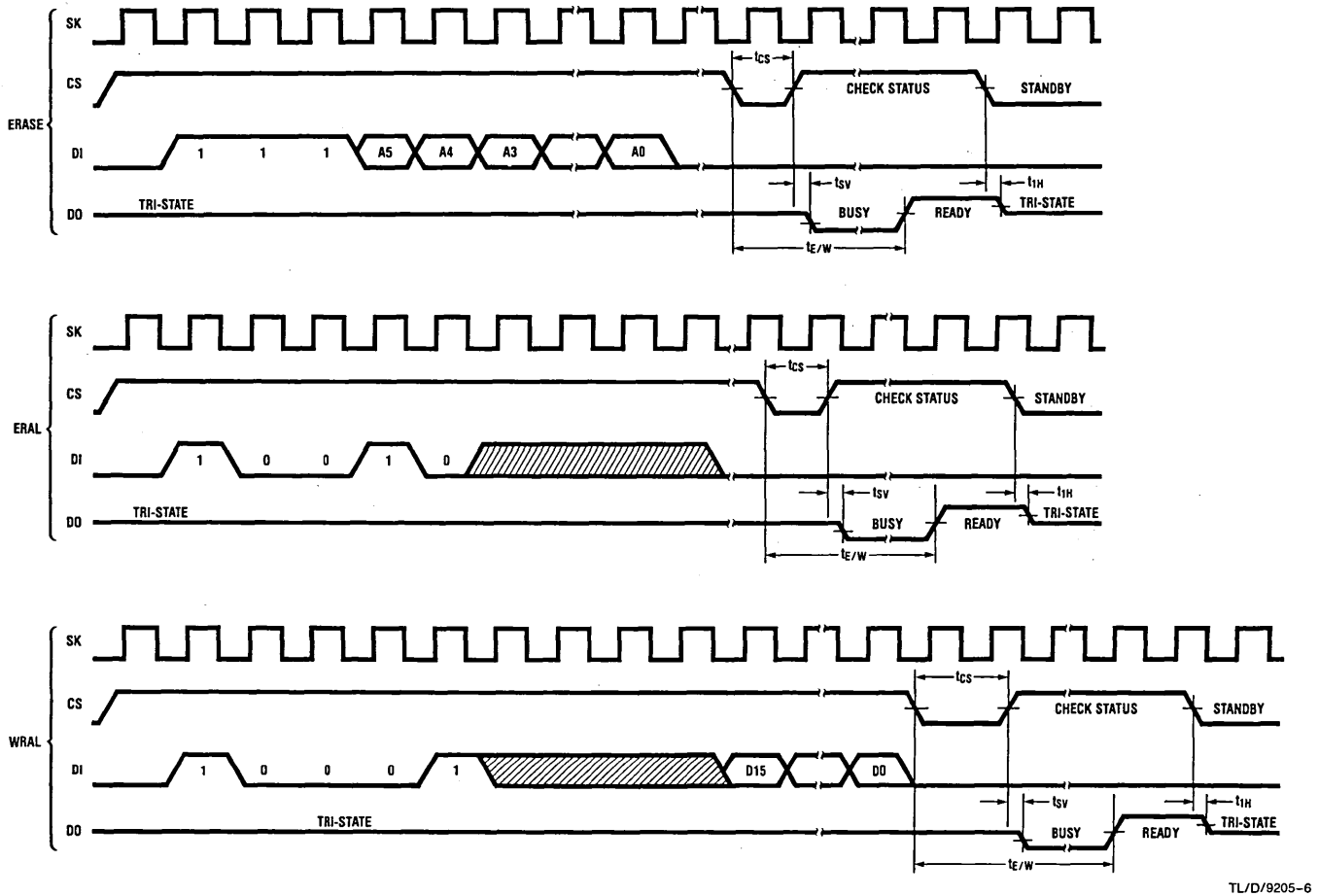
*This is the minimum SK period.

Instruction Timing



TL/D/9205–5

Instruction Timing



TL/D/9205–6

National Semiconductor Corporation

PRELIMINARY

NMC9346E 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

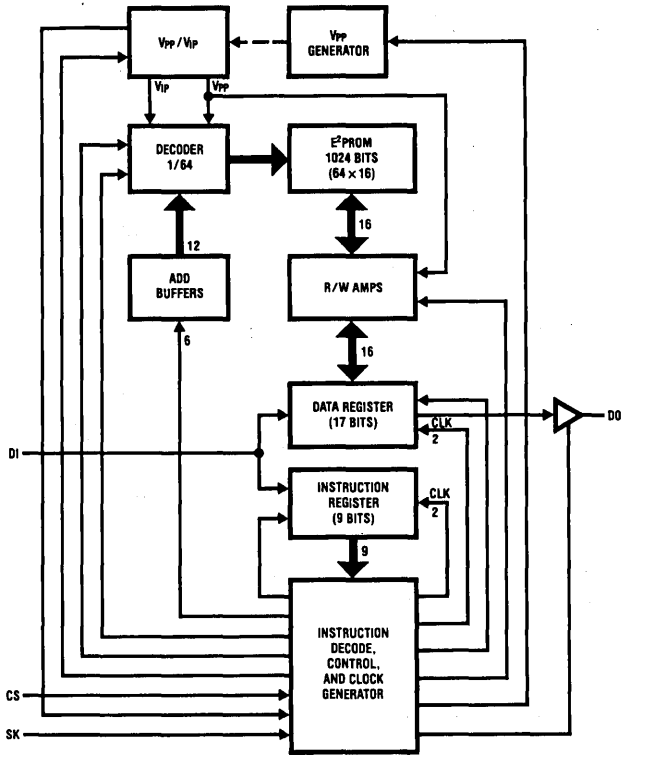
General Description

The NMC9346E is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346E has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

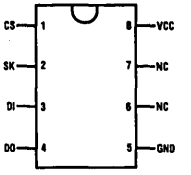
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



TL/D/9206-1

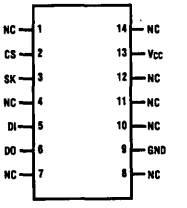
Dual-In-Line Package



TL/D/9206-2

Top View
Order Number NMC9346EN
See NS Package Number N08E

SO Package



TL/D/9206-3

Top View

Order Number NMC9346EM
See NS Package Number M14B

Note 1: Contact factory for SO8 availability.

Note 2: Contact factory for availability of extended temperature SO.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage Relative to GND +6V to −0.3V

Ambient Operating Temperature −40°C to +85°C

Ambient Storage Temp. −65°C to +125°C

Lead Temperature (Soldering, 10 seconds) 300°C

ESD rating is to be determined.

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1 $V_{CC} = 5.5V$		14 14	mA mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		4	mA
V_{IL} V_{IH}	Input Voltage Levels		−0.1 2.0	0.8 $V_{CC}+1$	V V
V_{OL} V_{OH}	Output Voltage Levels	$I_{OL} = 2.1$ mA $I_{OH} = -400\ \mu A$	 2.4	0.4	V V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
 t_{SKH} t_{SKL}	SK Frequency SK High Time (Note 2) SK Low Time (Note 2)		0 1 1	250	kHz μs μs
 t_{CSS} t_{CSH} t_{DIS} t_{DIH}	Inputs CS DI		 0.2 0 0.4 0.4		 μs μs μs μs
 $t_{pd}1$ $t_{pd}0$	Output DO	$C_L = 100$ pF $V_{OL} = 0.8V$, $V_{OH} = 2.0V$ $V_{IL} = 0.45V$, $V_{IH} = 2.40V$		 2 2	 μs μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μs
t_{0H}, t_{IH}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g., if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9346E

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9346E has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346E is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

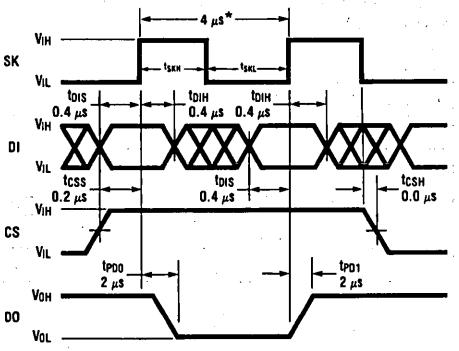
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

Synchronous Data Timing



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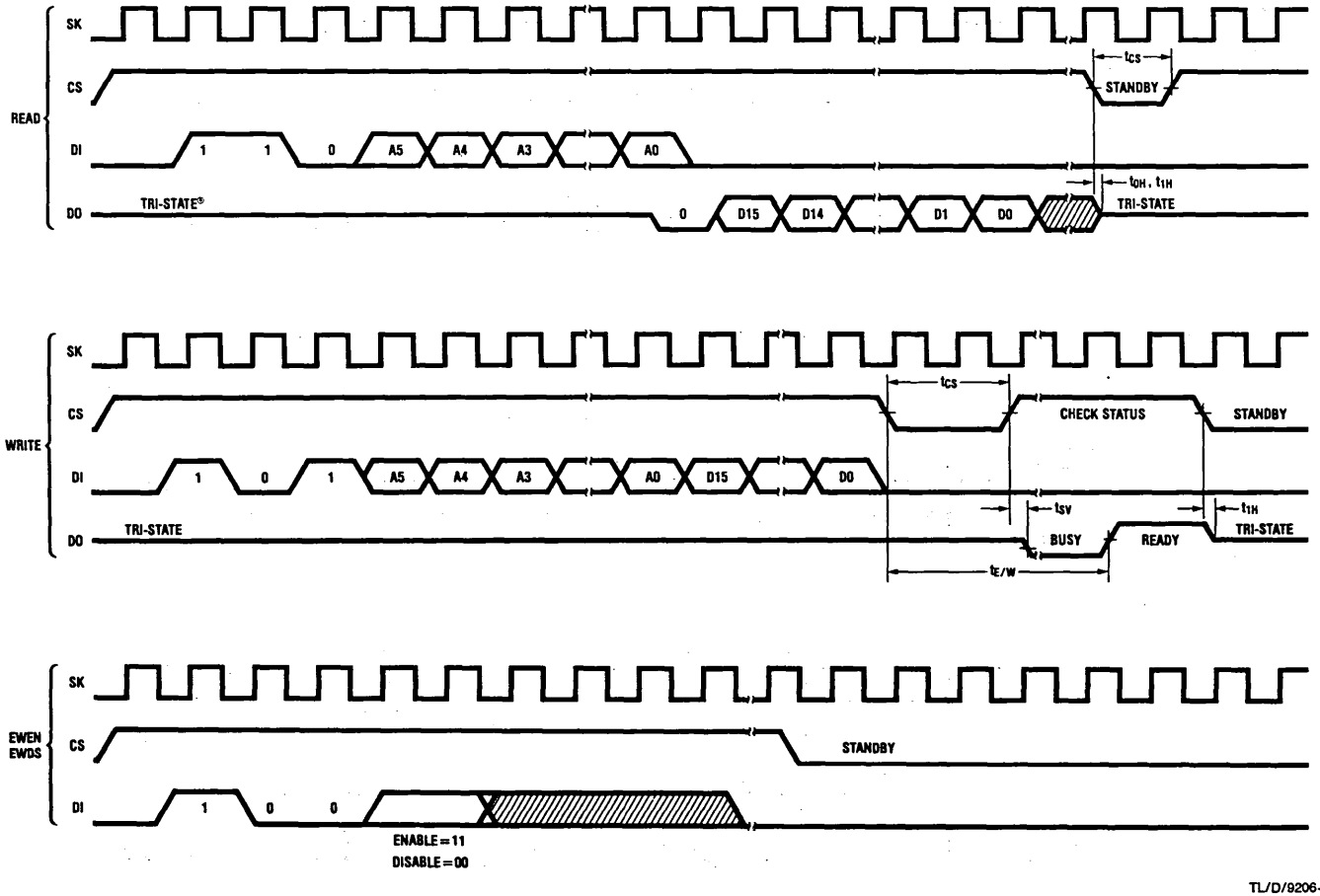
*This is the minimum SK period.

Instruction Timing



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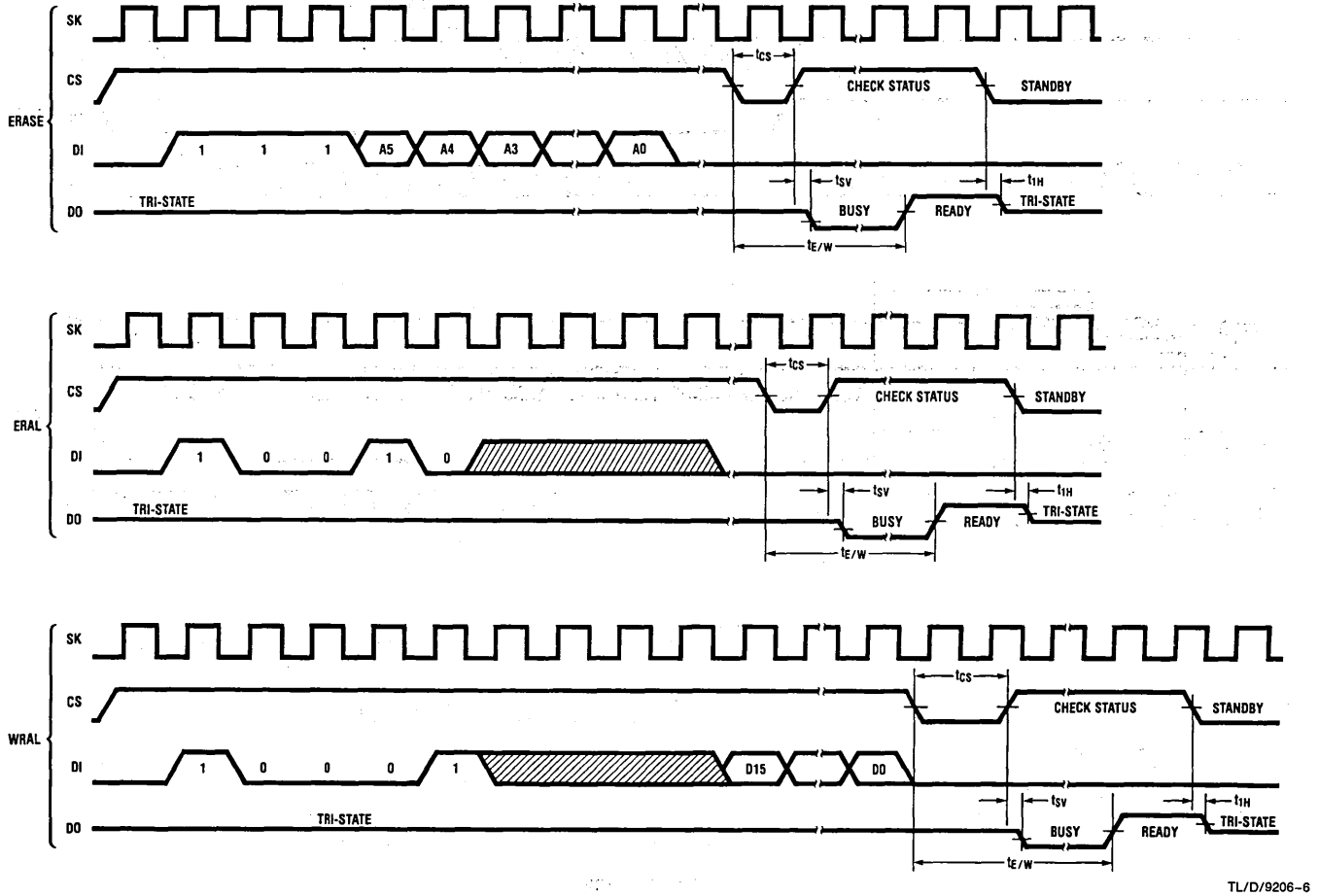
Instruction Timing



TL/D/9206–6

National Semiconductor Corporation

PRELIMINARY

NMC9346MN 1024-Bit Serial Electrically Erasable Programmable Memory (Mill Temp)

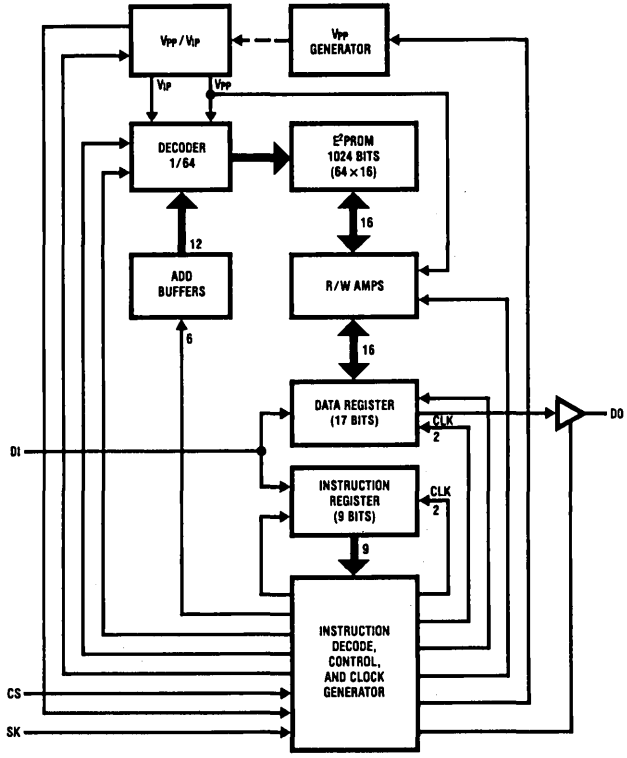
General Description

The NMC9346MN is a 1024-bit non-volatile, sequential E^2PROM, fabricated using advanced N-channel E^2PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346MN has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

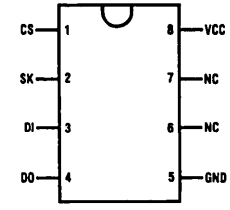
- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



TL/D/9207–1

Dual-In-Line Package



TL/D/9207–2

Top View

Order Number NMC9346MN
See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage Relative to GND +6V to −0.3V

Ambient Operating Temperature −55°C to +125°C

Ambient Storage Temp. −65°C to +125°C

Lead Temperature (Soldering, 10 seconds) 300°C

ESD rating is to be determined.

DC and AC Electrical Characteristics $-55°C \le T_A \le +125°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC}=5.5V$, CS=1, SK=1 $V_{CC}=5.5V$		15 15	mA mA
I_{CC2}	Standby Current	$V_{CC}=5.5V$, CS=0		5	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+0.5$	V
	Output Voltage Levels				
V_{OL}		$I_{OL}=2.1$ mA		0.4	V
V_{OH}		$I_{OH}=-400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN}=5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=5.5V$, CS=0		10	μA
	SK Frequency		0	200	kHz
t_{SKH}	SK High Time (Note 2)		2		μs
t_{SKL}	SK Low Time (Note 2)		1		μs
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L=100$ pF			
t_{pd1}	DO	$V_{OL}=0.8V$, $V_{OH}=2.0V$		2	μs
t_{pd0}		$V_{IL}=0.45V$, $V_{IH}=2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			12	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L=100$ pF		1	μs
t_{0H}, t_{IH}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 5 μs. e.g., if $t_{SKL} = 2$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9346MN

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9346MN has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346MN is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. The NMC9346MN is organized as sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

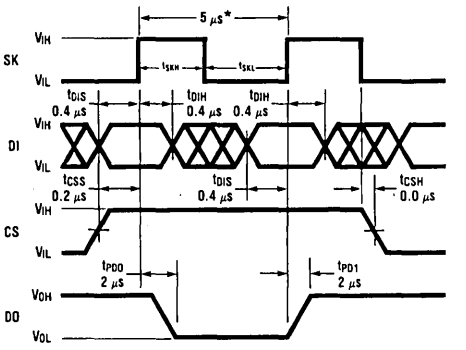
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

Synchronous Data Timing



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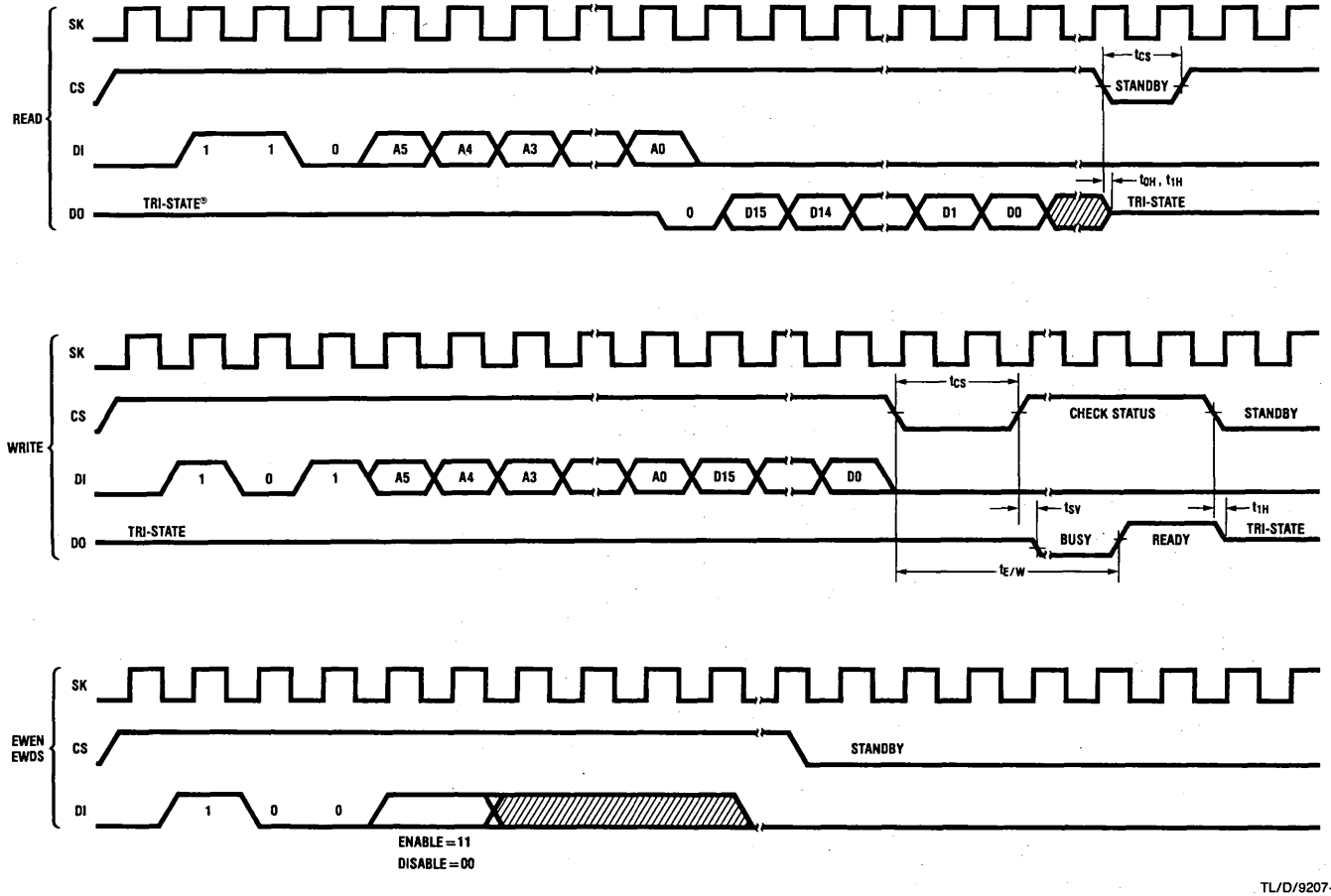
*This is the minimum SK period.

Instruction Timing



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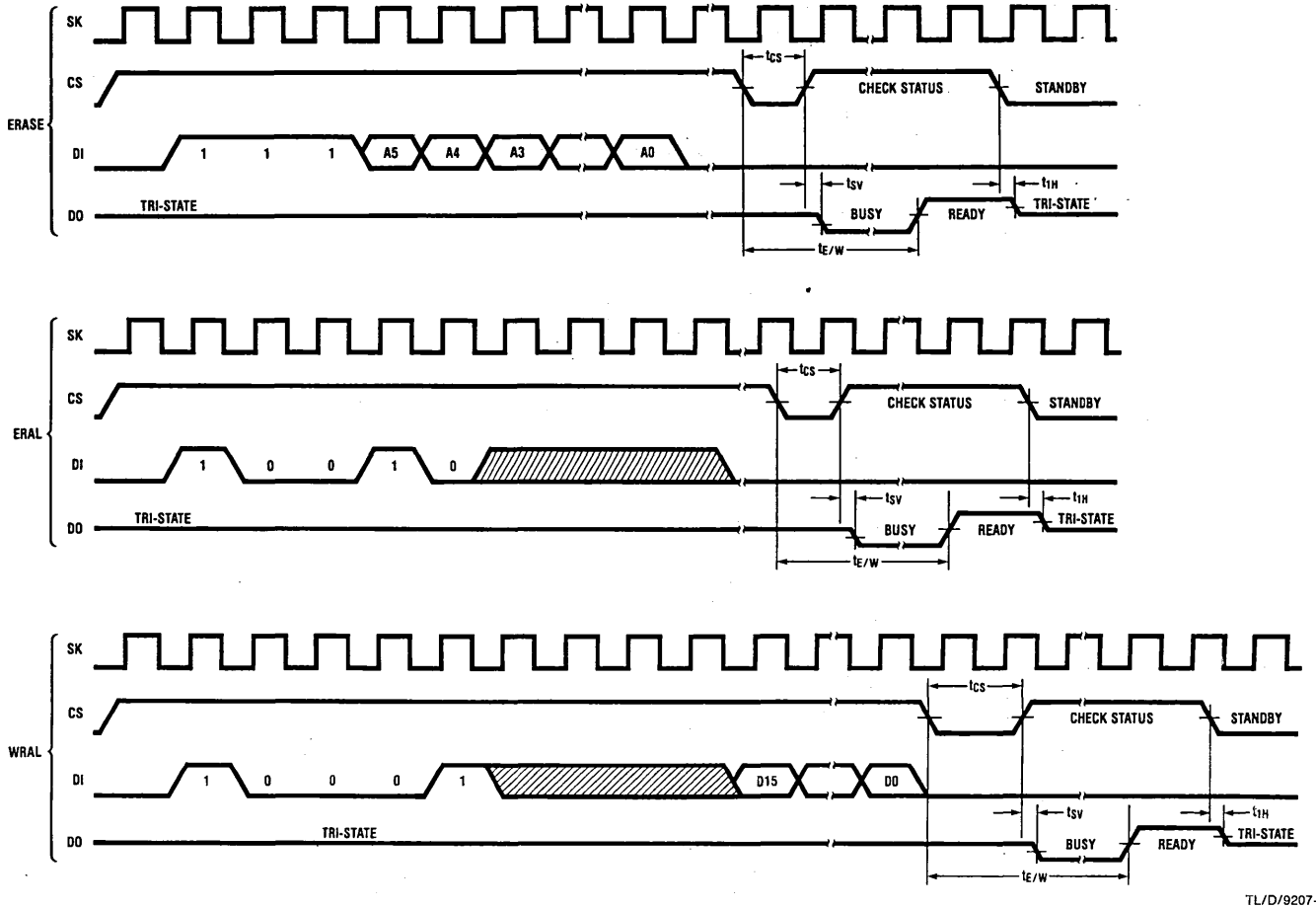
Instruction Timing



TL/D/9207–5

National Semiconductor Corporation

PRELIMINARY

NMC93CS06/NMC93CS26/NMC93CS46 256-Bit/512-Bit/1024-Bit Serial Electrically Erasable Programmable Read Only Memories (EEPROM)

General Description

The NMC93CS06/NMC93CS26/NMC93CS46 are external memories with 256/512/1024 bits of read/write memory divided into 16/32/64 registers of 16 bits each. N registers ($N \leq 16$, $N \leq 32$ or $N \leq 64$) can be protected against data modification by programming into a special on-chip register called the memory 'protect register' the address of the first register to be protected. This address can be 'locked' into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the 'protect register' will be aborted.

The 'read' instruction loads the address of the first register to be read into an 8-bit address pointer. Then the data is clocked out serially on the 'DO' pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 256/512/1024 bits. Thus, the NMC93CS06/NMC93CS26/NMC93CS46 can be viewed as a non-volatile shift register.

The 'write' cycle is completely self-timed and includes an automatic register erase so that no separate erase cycle is required. The 'write' cycle is only enabled when pin 6 (program enable) is held 'high'. If the address of the register to be written is less than the address in the 'protect register' then the data is written 16 bits at a time into one of the 16/32/64 data registers. If 'CS' is brought 'high' following the initiation of a 'write' cycle the 'DO' pin indicates the ready/busy status of the chip.

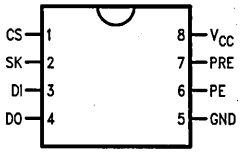
National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 10 years.

Features

- Write protection in user defined section of memory
- Typical active current 1 mA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- Microwire compatible serial I/O
- Self-timed programming cycle with autoerase
- Device status signal during programming mode
- Sequential register read
- Over 10 years data retention

Connection Diagrams

PIN OUT:
Dual-In-Line Package



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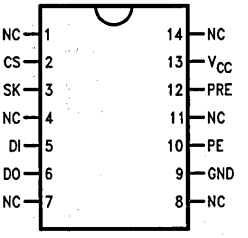
Top View

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:
SO Package



TL/D/9208–2

Top View

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Order Number NMC93CS06N, NMC93CS26N, NMC93CS46N, NMC93CS06EN, NMC93CS26EN, NMC93CS46EN, NMC93CS06MN, NMC93CS26MN or NMC93CS46MN
See Package Number M14A or N08E

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Ambient Operating Temperature
- NMC93CS06/NMC93CS26/ NMC93CS46: −10°C to +80°C
- NMC93CS06E/NMC93CS26E/ NMC93CS46E: −50°C to +95°C
- NMC93CS06M/NMC93CS26M/ NMC93CS46M (Mil. Temp.): −65°C to +125°C

Ambient Storage Temperature: −65°C to +150°C

All Input or Output Voltages with Respect to Ground: +6.5V to −0.3V

Lead Temperature (Soldering, 10 sec.): +300°C

ESD rating to be determined.

DC and AC Electrical Characteristics

$-40°C < T_A < +85°C$ E, $-55°C < T_A < +125°C$ M $0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = V_{IH}, SK = 1 MHz		2 4 4	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = V_{IH}, SK = 1 MHz		3 6 6	mA
I_{CC3}	Standby Current	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M		0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 2)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 2)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	(Note 3)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	50 100 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06/NMC93CS26/NMC93CS46 NMC93CS06E/NMC93CS26E/NMC93CS46E NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to SK	50 100 100		ns

DC and AC Electrical Characteristics

$0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$ (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS06/NMC93CS26/NMC93CS46	Relative to SK	50		
		NMC93CS06E/NMC93CS26E/NMC93CS46E		100		ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M		100		
t_{DIS}	DI Setup Time	NMC93CS06/NMC93CS26/NMC93CS46	Relative to SK	100		
		NMC93CS06E/NMC93CS26E/NMC93CS46E		200		ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M		200		
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS06/NMC93CS26/NMC93CS46	Relative to CS	250		
		NMC93CS06E/NMC93CS26E/NMC93CS46E	Relative to CS	500		ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M	Relative to CS	500		
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS06/NMC93CS26/NMC93CS46	Relative to SK	100		
		NMC93CS06E/NMC93CS26E/NMC93CS46E		200		ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M		200		
t_{PD1}	Output Delay to "1"	NMC93CS06/NMC93CS26/NMC93CS46			500	
		NMC93CS06E/NMC93CS26E/NMC93CS46E	AC Test		1000	ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M			1000	
t_{PD0}	Output Delay to "0"	NMC93CS06/NMC93CS26/NMC93CS46			500	
		NMC93CS06E/NMC93CS26E/NMC93CS46E	AC Test		1000	ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M			1000	
t_{SV}	CS to Status Valid	NMC93CS06/NMC93CS26/NMC93CS46			500	
		NMC93CS06E/NMC93CS26E/NMC93CS46E	AC Test		1000	ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M			1000	
t_{DF}	CS to DO in TRI-STATE®	NMC93CS06/NMC93CS26/NMC93CS46	$CS = V_{IL}$		100	
		NMC93CS06E/NMC93CS26E/NMC93CS46E	AC Test		200	ns
		NMC93CS06M/NMC93CS26M/NMC93CS46M			200	
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

$T_A = 25°C$, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

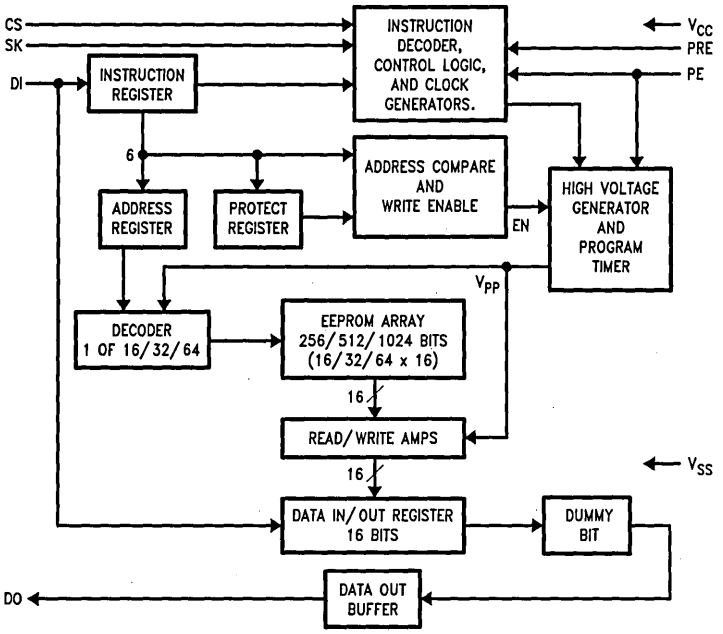
Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Block Diagram



TL/D/9208–3

Instruction Set for the NMC93CS06, NMC93CS26 and NMC93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when "protect register" is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in "protect register".
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into "protect register". Thereafter, memory addresses ≥ the address in "protect register" are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the "protect register" cannot be altered.

Functional Description

The NMC93CS06, NMC93CS26, and NMC93CS46 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8-bits carry the op code and the 6-bit address for selection of 1 of 16, 32, or 64 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin **MUST** be held "high" while loading the instruction. Following the PRREAD instruction the 6-bit address stored in the memory "protect register" is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held "high" while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the "protect register" and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the "Protect Register" the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the "Protect Register" must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

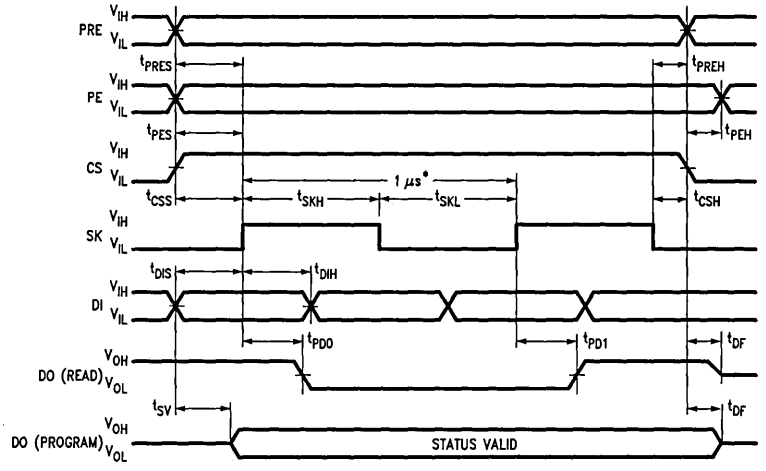
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the "Protect Register" unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing



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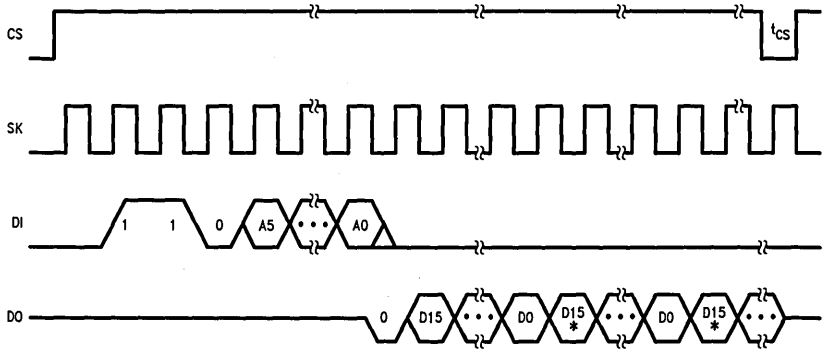
*This is the minimum SK period (See Note 2).

READ†:
PRE = 0, PE = X

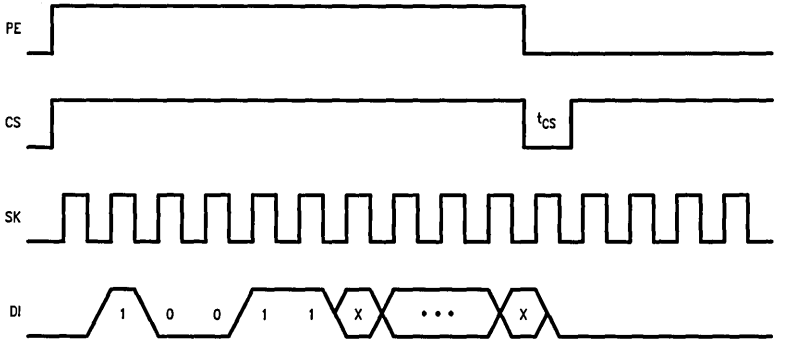


TL/D/9208–5

- Address bit A5 becomes a "don't care" for NMC93CS26
- Address bits A5 and A4 become "don't cares" for NMC93CS06

*The memory automatically cycles to the next register.

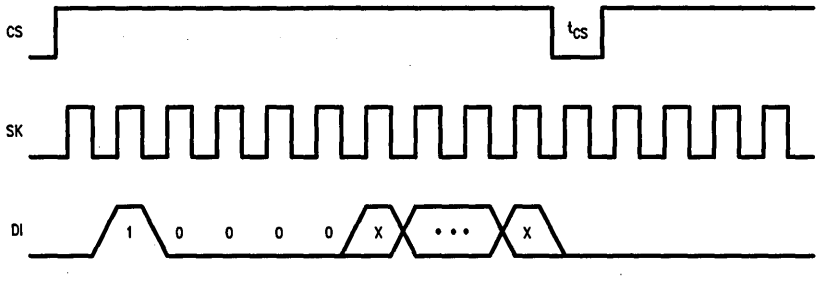
WEN:
PRE = 0, D0 = TRI-STATE



TL/D/9208–6

Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE



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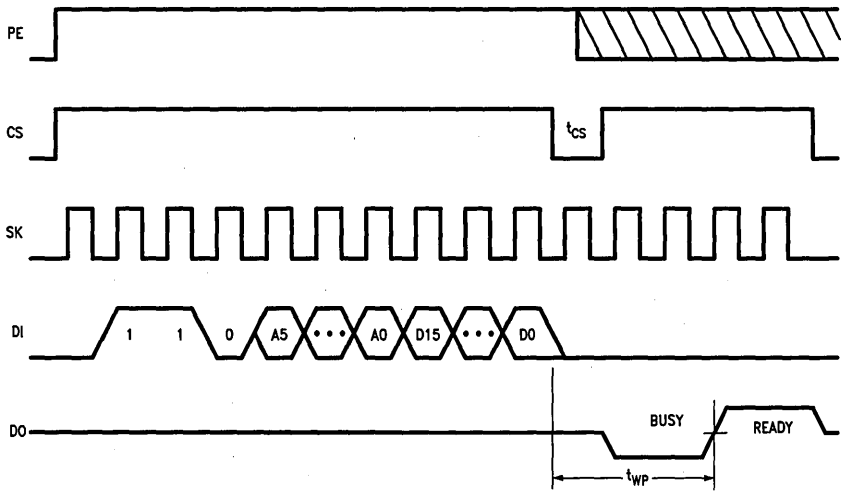
WRITE*:
PRE = 0

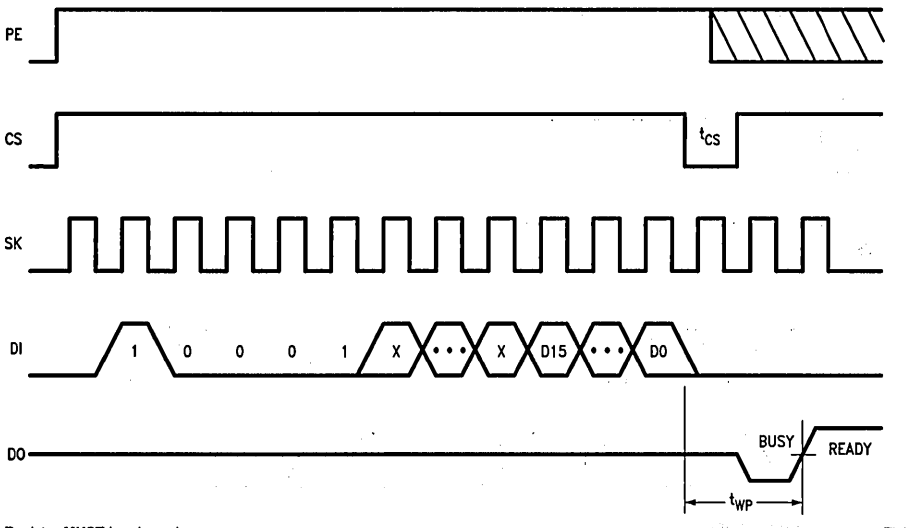


TL/D/9208-8

*
- Address bit A5 becomes a "don't care" for NMC93CS26
- Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

WRALL*:
PRE = 0



*Protect Register **MUST** be cleared.

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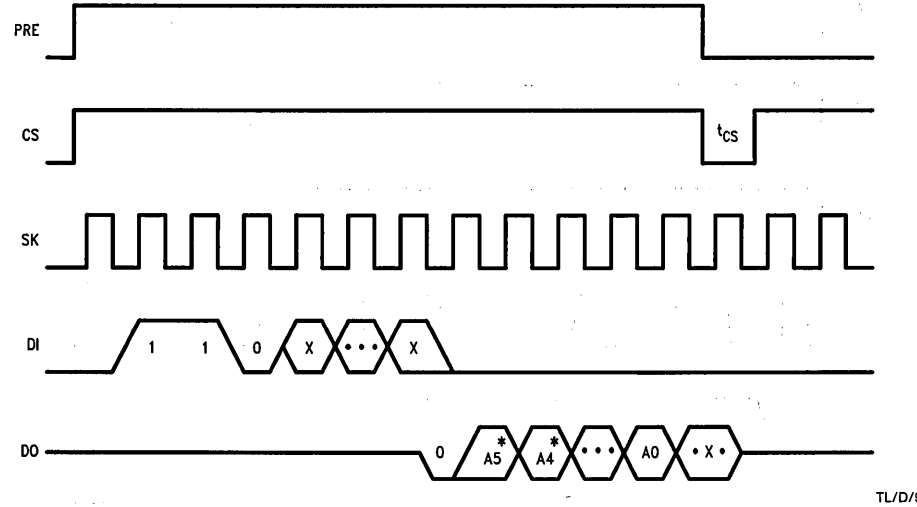
PRREAD*:
PE = X



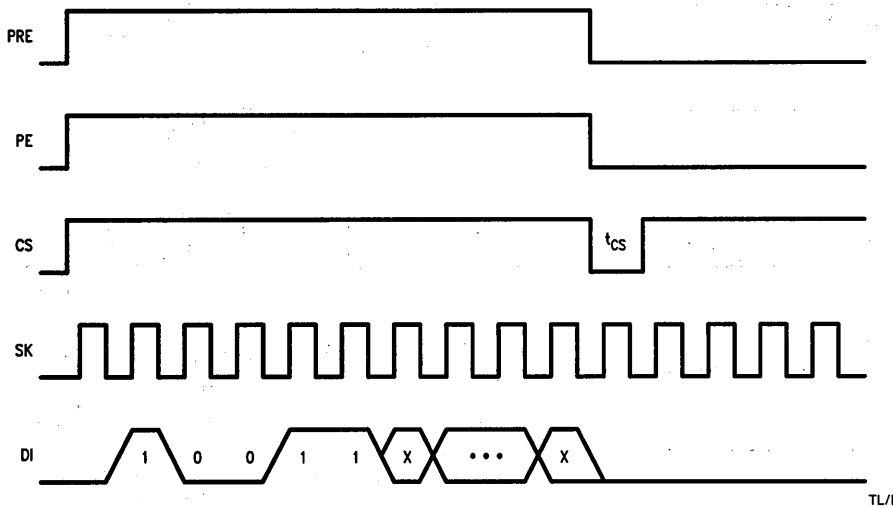
TL/D/9208–10

- Address bit A5 becomes a "don't care" for NMC93CS26
- Address bits A5 and A4 become "don't cares" for NMC93CS06

2

Timing Diagrams (Continued)

PREN*:
D0 = TRI-STATE



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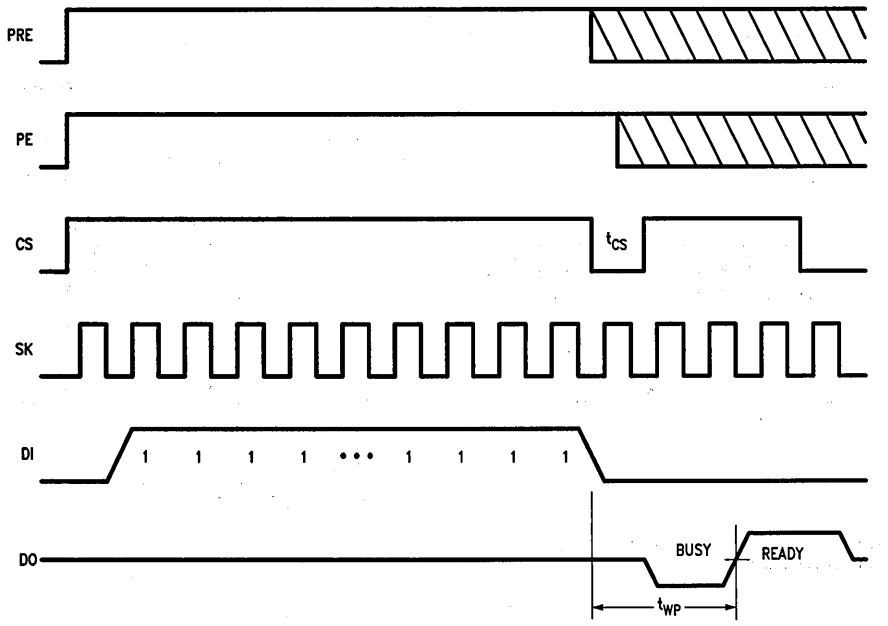
*A WEN cycle must precede a PREN cycle.

PRCLEAR*:



*A PREN cycle must **immediately** precede a PRCLEAR cycle.

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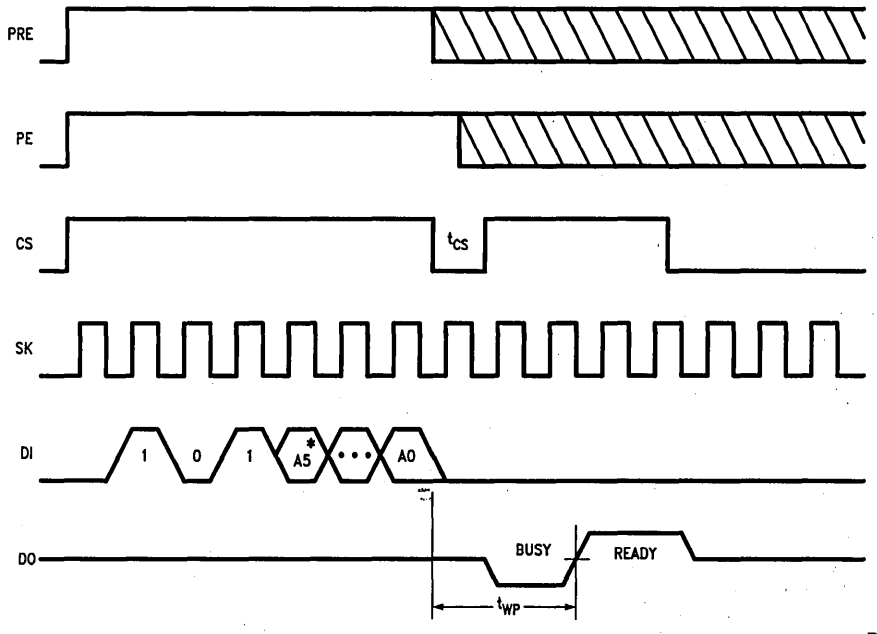
Timing Diagrams (Continued)

PRWRITE†:

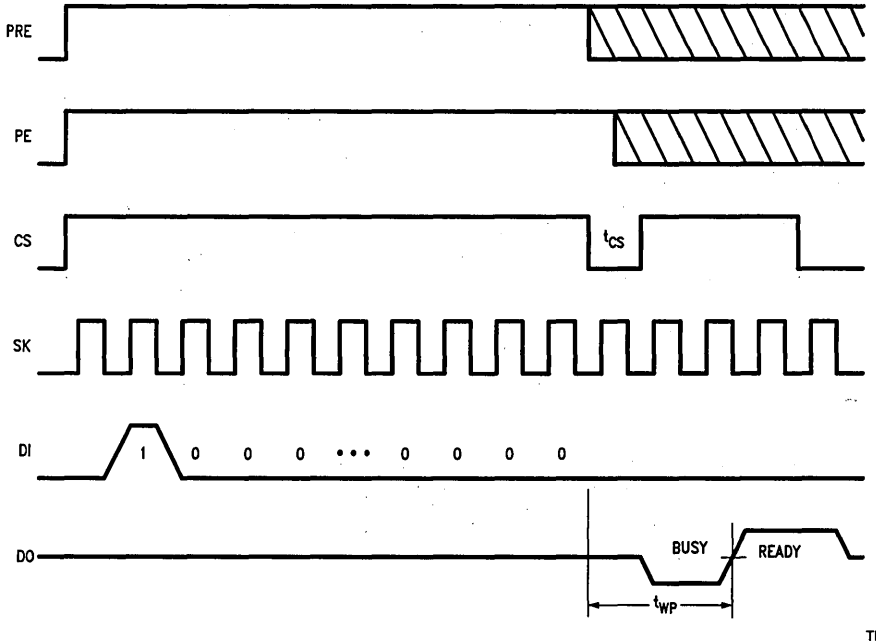


TL/D/9208–13

- Address bit A5 becomes a "don't care" for NMC93CS26
- Address bits A5 and A4 become "don't cares" for NMC93CS06

*Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:



TL/D/9208–14

***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor Corporation

PRELIMINARY

NMC93CS56/NMC93CS66 2048-Bit/4096-Bit Serial Electrically Erasable Programmable Read Only Memories (EEPROM)

General Description

The NMC93CS56/NMC93CS66 are external memories with 2048/4096 bits of read/write memory divided into 128/256 registers of 16 bits each. N registers ($N \leq 128$ or $N \leq 256$) can be protected against data modification by programming into a special on-chip register called the memory "protect register" the address of the first register to be protected. This address can be "locked" into the device, so that these registers can be permanently protected. Thereafter, all attempts to alter data in a register whose address is equal to or greater than the address stored in the "protect register" will be aborted.

The "read" instruction loads the address of the first register to be read into an 8-bit address pointer. Then the data is clocked out serially on the "DO" pin and automatically cycles to the next register to produce a serial data stream. In this way the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 2048/4096 bits. Thus, the NMC93CS56/NMC93CS66 can be viewed as a non-volatile shift register.

The "write" cycle is completely self-timed and includes an automatic register erase so that no separate erase cycle is required. The "write" cycle is only enabled when pin 6 (program enable) is held "high". If the address of the register to be written is less than the address in the "protect register" then the data is written 16 bits at a time into one of the 128/256 data registers. If "CS" is brought "high" following the initiation of a "write" cycle the "DO" pin indicates the ready/busy status of the chip.

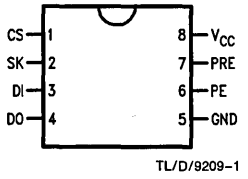
National Semiconductor's EEPROMs are designed and tested for applications requiring extended endurance. Refer to device operation for further endurance information. Data retention is specified to be greater than 10 years.

Features

- Write protection in user defined section of memory
- Typical active current 1 mA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 5 volt only operation in all modes
- Microwire compatible serial I/O
- Self-timed programming cycle with autoerase
- Device status signal during programming mode
- Sequential register read
- Over 10 years data retention

Connection Diagrams

PIN OUT:
Dual-In-Line Package



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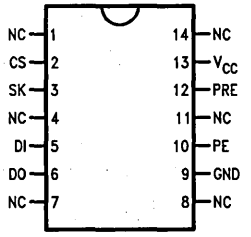
Top View

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:
SO Package



TL/D/9209-2

Top View

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Order Number NMC93CS56N, NMC93CS66N, NMC93CS56EN, NMC93CS66EN, NMC93CS56M, NMC93CS66M, NMC93CS56MN or NMC93CS66MN
See Package Number N08E, M14A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Ambient Operating Temperature
- NMC93CS56/NMC93CS66: −10°C to +80°C
- NMC93CS56E/NMC93CS66E: −50°C to +95°C
- NMC93CS56M/NMC93CS66M (Mil. Temp.): −65°C to +125°C

Ambient Storage Temperature: −65°C to +150°C

All Input or Output Voltages with Respect to Ground: +6.5V to −0.3V

Lead Temp. (Soldering, 10 sec.): +300°C

$-40°C < T_A < 85°C$ E

$-55°C < T_A < 125°C$ M

ESD rating is to be determined.

DC and AC Electrical Characteristics

$0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	CS = V_{IH}, SK = 1 MHz		2 4 4	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	CS = V_{IH}, SK = 1 MHz		3 6 6	mA
I_{CC3}	Standby Current	NMC93CS56M/NMC93CS66M NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	CS = 0V		50 100 100	µA
I_{IL}	Input Leakage	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA µA
I_{OL}	Output Leakage	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	µA µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 µA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 µA I_{OH} = −10 µA	 V_{CC} − 0.2	0.2	V V
f_{SK}	SK Clock Frequency	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M		0	1 0.5 0.5	MHz
t_{SKH}	SK High Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 2)	250 500 500		ns
t_{SKL}	SK Low Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 2)	250 500 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	(Note 3)	250 500 500		ns
t_{CSS}	CS Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns
t_{PRES}	PRE Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns

DC and AC Electrical Characteristics

$0°C < T_A < 70°C$, $4.5V < V_{CC} < 5.5V$ (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PES}	PE Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	50 100 100		ns
t_{DIS}	DI Setup Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to CS Relative to CS Relative to CS	250 500 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS56/NMC93CS66 NMC93CS56E/NMC93CS66E NMC93CS56M/NMC93CS66M	AC Test CS = V_{IL}		100 200 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

$T_A = 25°C$, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

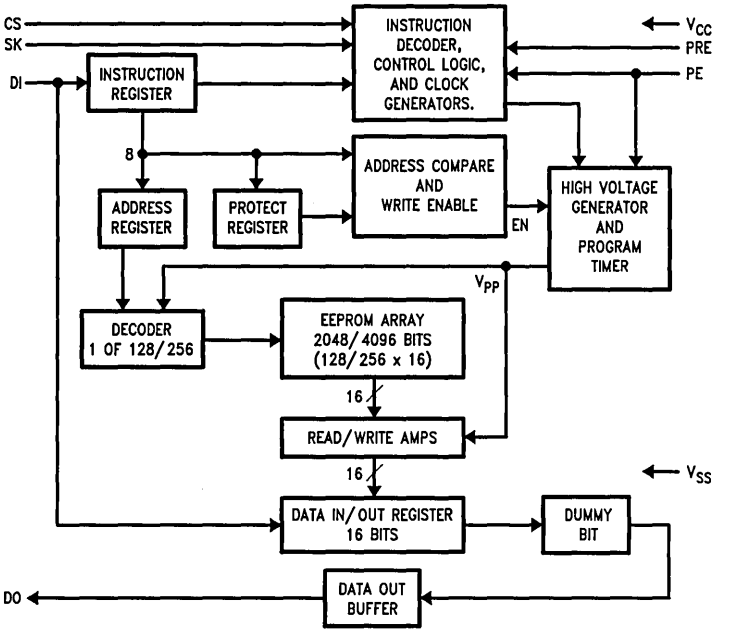
Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Block Diagram



TL/D/9209–03

Instruction Set for the NMC93CS56 and NMC93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when "protect register" is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in "protect register".
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into "protect register". Thereafter, memory addresses ≥ the address in "protect register" are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the "protect register" cannot be altered.

Functional Description

The NMC93CS56 and NMC93CS66 have 10 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for selection of 1 of 256, 16-bit registers.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (DO) is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin **MUST** be held "high" while loading the instruction. Following the PRREAD instruction the 8-bit address stored in the memory "protect register" is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held "high" while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the "protect register" and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the "Protect Register" the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the "Protect Register" must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held "high" while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must *immediately* precede a PRWRITE instruction.

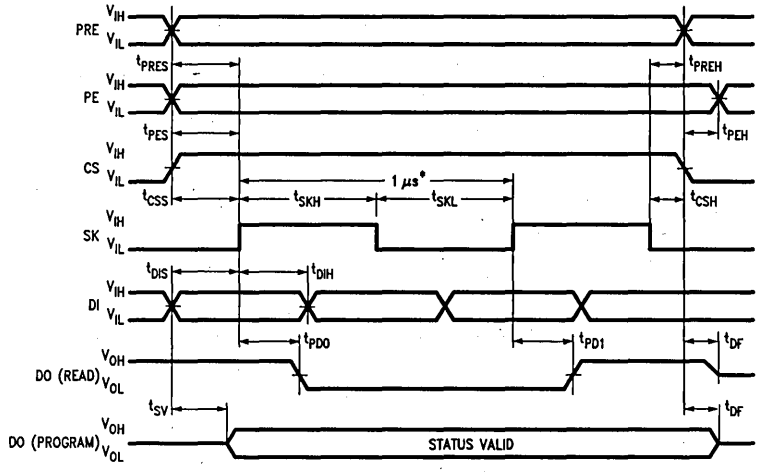
Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the "Protect Register" unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Timing Diagrams

Synchronous Data Timing



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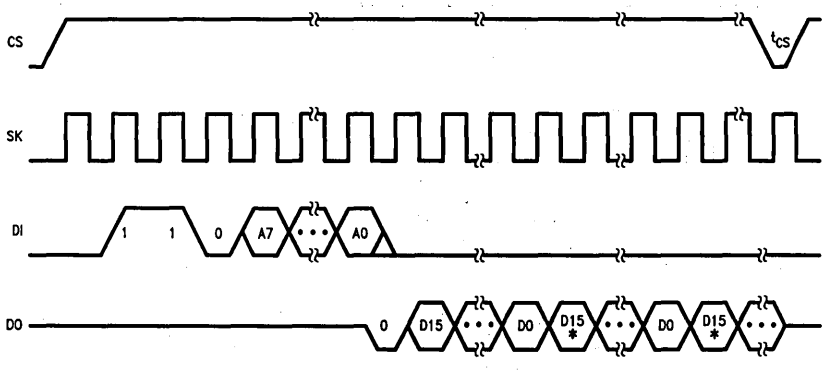
*This is the minimum SK period (See Note 2).

READ:*
PRE = 0, PE = X

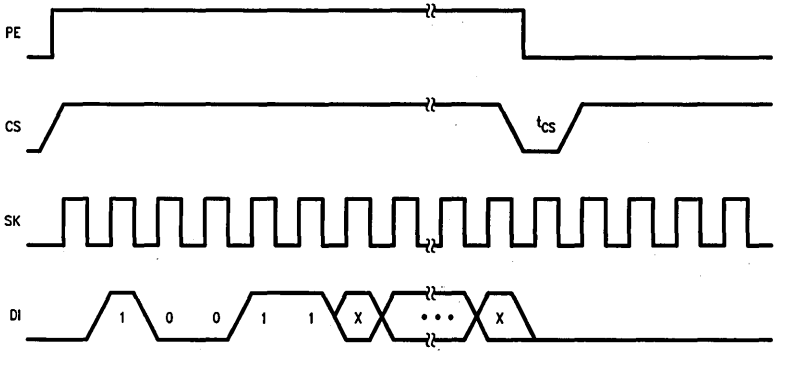


TL/D/9209–5

*Address bit A_7 becomes a "don't care" for NMC93CS56.

*The memory automatically cycles to the next register.

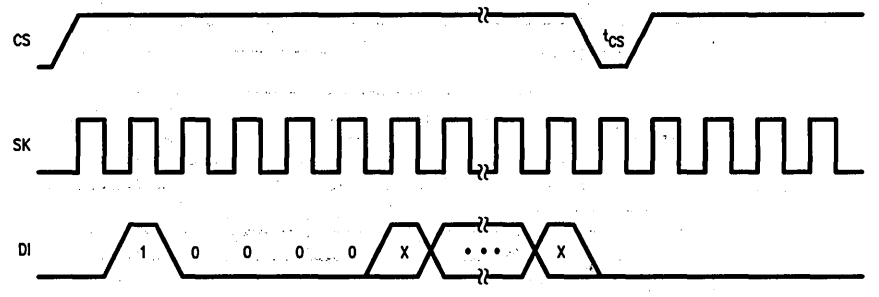
WEN:
PRE = 0, DO = TRI-STATE



TL/D/9209–6

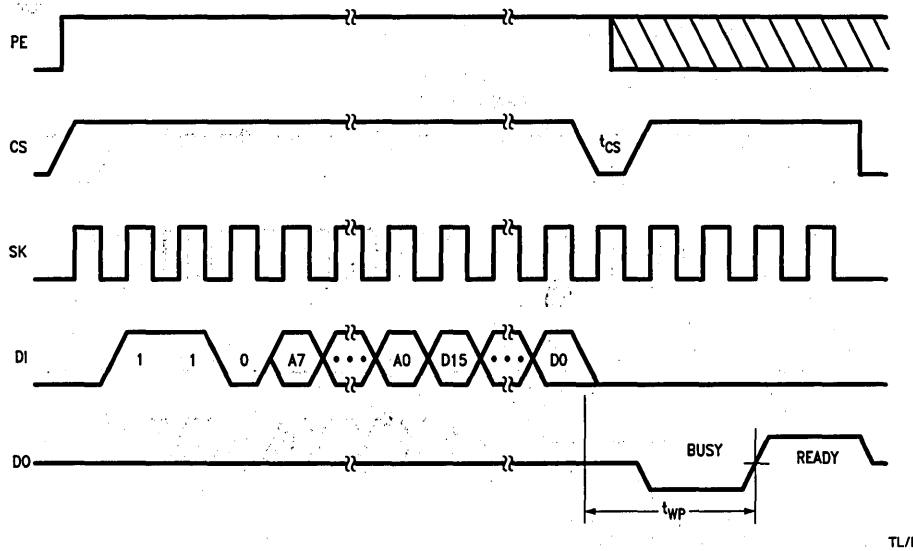
Timing Diagrams (Continued)

WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/9209–7

WRITE:*
PRE = 0

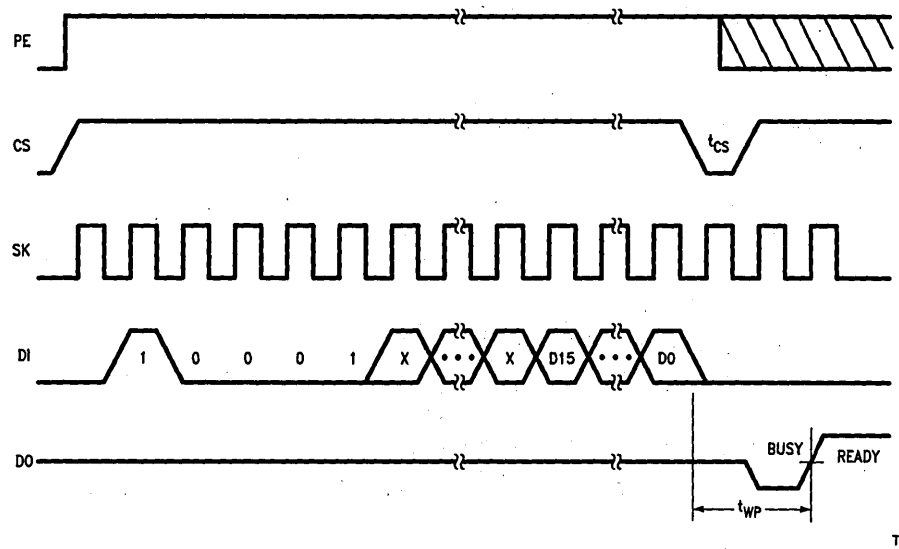


TL/D/9209–8

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

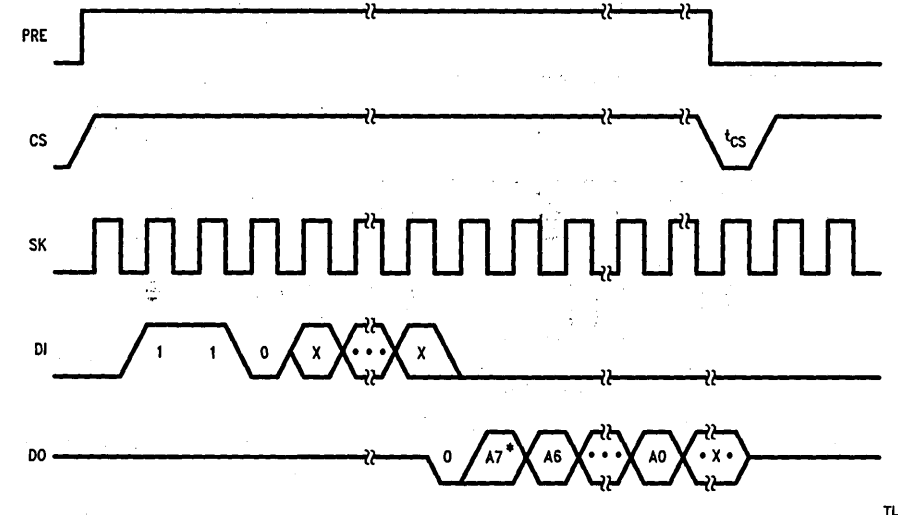
WRALL:*
PRE = 0



TL/D/9209–9

*Protect Register **MUST** be cleared.

PRREAD:*
PE = X

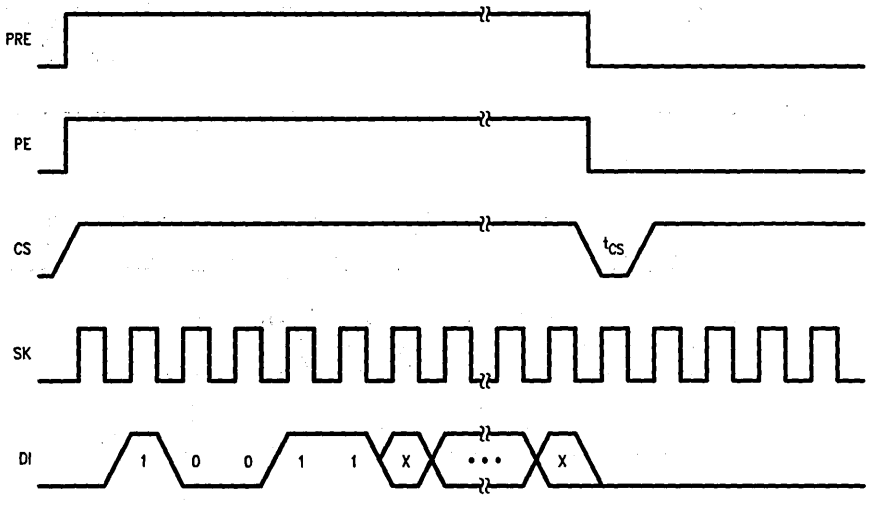


TL/D/9209–10

*Address bit A_7 becomes a "don't care" for NMC93CS56.

Timing Diagrams (Continued)

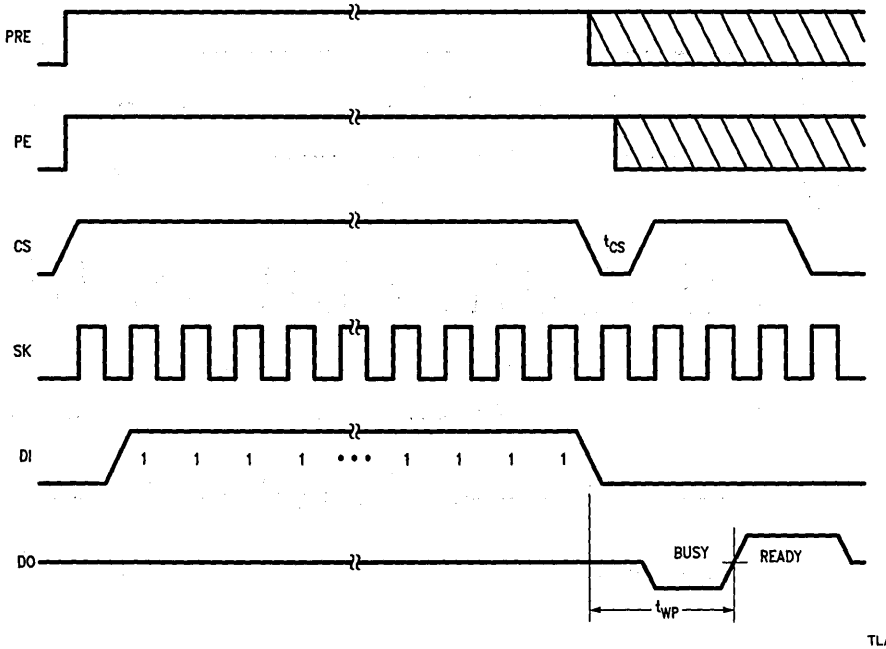
PREN:*
DO = TRI-STATE



TL/D/9209–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR:*



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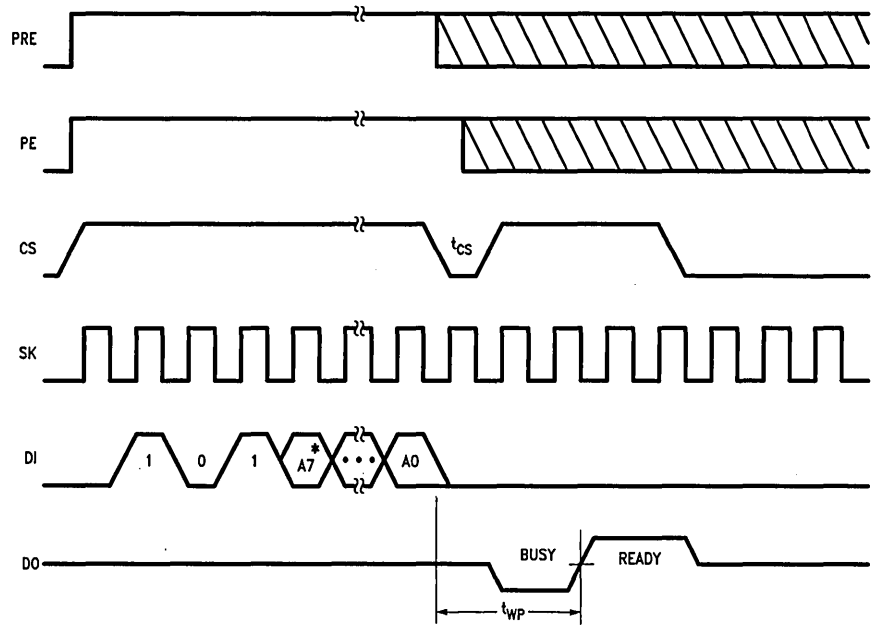
*A PREN cycle must **immediately** precede a PRCLEAR cycle.

Timing Diagrams (Continued)

PRWRITE:*

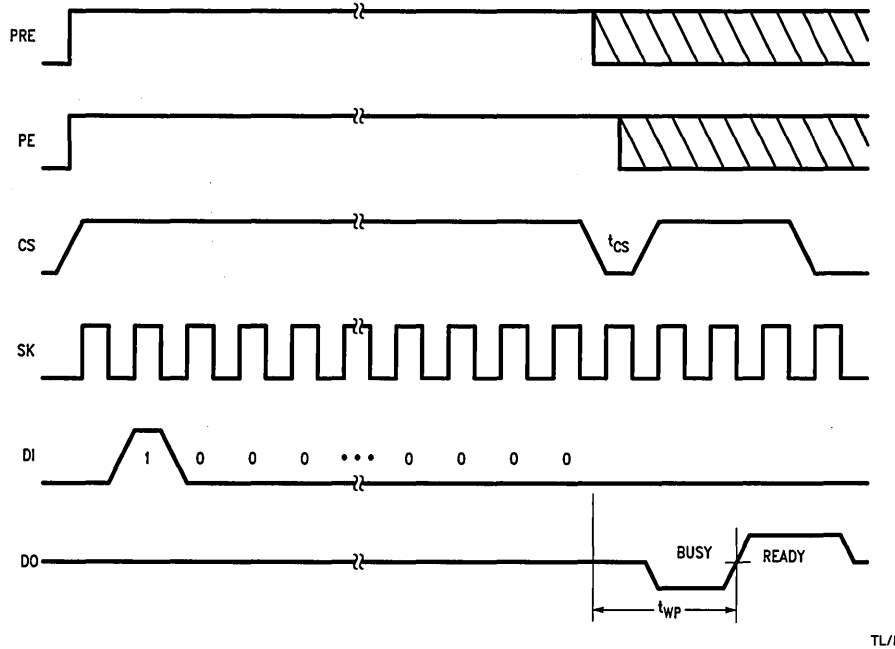


TL/D/9209–13

*Address bit A_7 becomes a "don't care" for NMC93CS56.

*Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS:*



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***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

National Semiconductor Corporation

PRELIMINARY

NMC98C10/NMC98C40 Electrically Erasable, Programmable Memories

General Description

The NMC98C10 and NMC98C40 are 128 by 8 and 512 by 8 5-volt programmable, non-volatile, parallel access memories built with 3-micron CMOS floating gate process. Data and address lines are multiplexed, enabling these devices to be packaged in an 18-pin DIP, saving board space. The pin-out is identical to the Intel 8185 static RAM and the 2001 non-volatile RAM, allowing the memories to directly interface with Intel and other popular 8-bit and 16-bit microprocessors and microcontrollers.

The write cycle is simplified by a self-timed erase before write circuit on-chip. The end of write cycle can be determined by polling the data pins or the controller can simply allow a minimum time between a write command and the subsequent command. To prevent undesirable modification of the memory contents during system power up or power down, a lockout circuit ignores write commands while V_{CC} is below the prescribed level of VLKO.

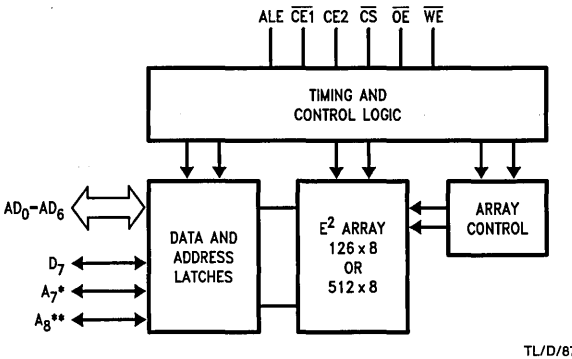
Applications for these memories include storing position data in robotic systems, storing local area network node address and parameter settings in data communications equipment, storing set-up and last position data in industrial control systems and storing PBX switch data in telecommunications equipment.

The NMC98C10 and NMC98C40 are compatible with Sierra Semiconductor SC22101, SC22104.

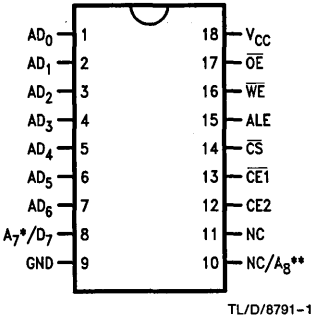
Features

- CMOS EE technology
- Single 5-volt supply
- Reliable CMOS floating gate process
- Eighteen-pin package
- Multiplexed address and data bus
- Self timed write operation
- $\overline{\text{DATA}}$ polling
- Minimum 10,000 erase/write cycles
- Very low power dissipation
- Ten year data retention
- Minimum board space
- Directly compatible with NSC800, NSC32000 and other standard microprocessors
- No external sequencing of erase/write cycle
- End of write cycle verified by polling
- Long product life

Block and Connection Diagrams



TL/D/8791–2



TL/D/8791–1

Order Number NMC98C10N, NMC98C10N-1, NMC98C40N, NMC98C40N-1
See NS Package Number N18A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Voltage on Any Pin	V_{CC} + 0.5V GND − 0.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temp. (Soldering, 10 seconds)	300°C

ESD rating is to be determined.

Operating Conditions

(Applies to DC and AC Characteristics)

Ambient Temperature	0°C to 70°C
Positive Supply Voltage	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = − 400 μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{LKO}	V_{CC} Level for Write Lockout		4.0		4.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}			±10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}			±10.0	μA
I_{CC}	Operating Supply Current	TTL Inputs			15.0	mA
		CMOS Inputs			10.0	mA
I_{CCPD}	Standby Supply Current	TTL Inputs			5.0	mA
		CMOS Inputs			100	μA
I_{SC}	Short-Circuit Current	One Output Pin Shorted		40		mA

AC Electrical Characteristics

Symbol	Parameter	NMC98C10, NMC98C40		NMC98C10-1, NMC98C40-1		Units
		Min	Max	Min	Max	
T_{AL}	Address to Latch Setup Time	50		20		ns
T_{LA}	Address Hold Time after Latch	45		30		ns
T_{LC}	Latch to OE/WE Control	80		35		ns
T_{OE}	Valid Data Out Delay from Read Control		170		120	ns
T_{LD}	ALE to Data Out Valid		300		180	ns
T_{LL}	Latch Enable Width	100		60		ns
T_{OH}	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (Whichever Changes First)	0		0		ns
T_{OLZ}	$\overline{OE}$ Low to Output Driven	10		10		ns
T_{RDF}	Data Bus Float after Read	0	95	0	60	ns
T_{CL}	OE/WE Control to Latch Enable	0		0		ns
T_{CC}	OE/WE Control Width	250		150		ns
T_{DW}	Data In to Write Setup Time	150		150		ns
T_{WD}	Data In Hold Time after Write	20		15		ns
T_{SC}	Chip Select Set-Up to OE/WE Control	50		20		ns
T_{CS}	Chip Select Hold Time after OE/WE Control	10		10		ns
T_{ALCE}	Chip Enable Set-Up to ALE Falling	30		5		ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	NMC98C10, NMC98C40		NMC98C10-1, NMC98C40-1		Units
		Min	Max	Min	Max	
T_{LACE}	Chip Enable Hold Time after ALE Falling	45		40		ns
T_{WR}	Byte Write Cycle Time		20		20	ms
T_{WH}	Data Invalid Time after $\overline{WE}$ Falling		1		1	ms
	Number of Writes Per Byte	10,000		10,000		Cycles

Capacitance (T_A = 25°C, f = 1 MHz) (Note 3)

Parameter	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
$C_{I/O}$	Input/Output Capacitance	$\overline{OE}$ = $\overline{CE1}$ = $\overline{CS}$ = V_{IH}, CE2 = V_{IL}		10	pF

AC Test Conditions

Output Load .....1 TTL Gate + C_L = 100 pF

Input Rise and Fall Times (10% to 90%) .....20 ns

Input Pulse Levels.....0.0V to 3.0V

Input/Output Timing Reference Level.....0.8V to 2.0V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.

Note 3: This parameter is sampled and not 100% tested.

Pin Descriptions

Pin Number	Pin Name	Function
1–8	AD_0–AD_7	Multiplexed address and data bits. Pin 8 is DATA only for NMC98C10.
9	GND	Ground, 0 volts.
10	A8	MSB of address for NMC98C40, NC for NMC98C10.
11	NC	No connection. No internal connection is made to this pin and it may be left floating.
12	CE2	Chip Enable 2 (see Table I)
13	$\overline{CE1}$	Chip Enable 1 (See Table I)
14	$\overline{CS}$	Chip Select (see Table I)
15	ALE	Address Latch Enable
16	$\overline{WE}$	Write Enable
17	$\overline{OE}$	Output Enable
18	V_{CC}	Positive power supply, 5 volts.

Functional Description

Table I shows the different modes of operation as a function of the control signals. Standby powered down mode: both write and read are inhibited and the device's power consumption is greatly reduced. Standby powered up mode: the device consumes the operating power, but read and write are inhibited. Inhibit mode: the device is write protected to avoid inadvertent modifications while the read and write pins are changing.

READ OPERATION

Figure 2 shows the timing diagram for READ operation. The address is latched on the falling edge of ALE. For the NMC98C10 only pins 1 through 7 are used for address bits. NMC98C40 uses pins 8 and 10 in addition to pins 1 through 7 for address bits.

Data appear on pins 1 through 8 after $\overline{OE}$ becomes active (low).

WRITE OPERATION

Write operation's timing is shown in *Figure 3*. Address is latched on the falling edge of the ALE. After the address is latched, the $\overline{WE}$ becomes active (low) for the minimum time of TCC and returns to inactive state. This initiates the internally timed write operation. No external erase before write operation is needed and data lines as well as control lines may change after the write operation is initiated.

TABLE I. Mode Table

Mode	$\overline{CE1}$	CE2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

V_{IL} = Logical Low Input

V_{IH} = Logical High Input

Hi-Z = High Impedance State

X = Don't Care

Functional Description (Continued)

$\overline{\text{DATA}}$ POLLING

After the write operation is initiated, its conclusion can be monitored by putting the device in the READ mode and polling the D7 data bit. The data bit will be logical inverse of the bit being written to a location in memory until the write operation is completed. At this time the D7 data bit will be the same as the last D7 data bit written into memory.

WRITE LOCKOUT

During system power up or power down, an on-chip write lockout circuit prevents spurious WRITES into the memory locations while V_{CC} is lower than the specified lockout voltage VLKO. This frees the system designer from having to design external write protection circuits.

Timing Waveforms

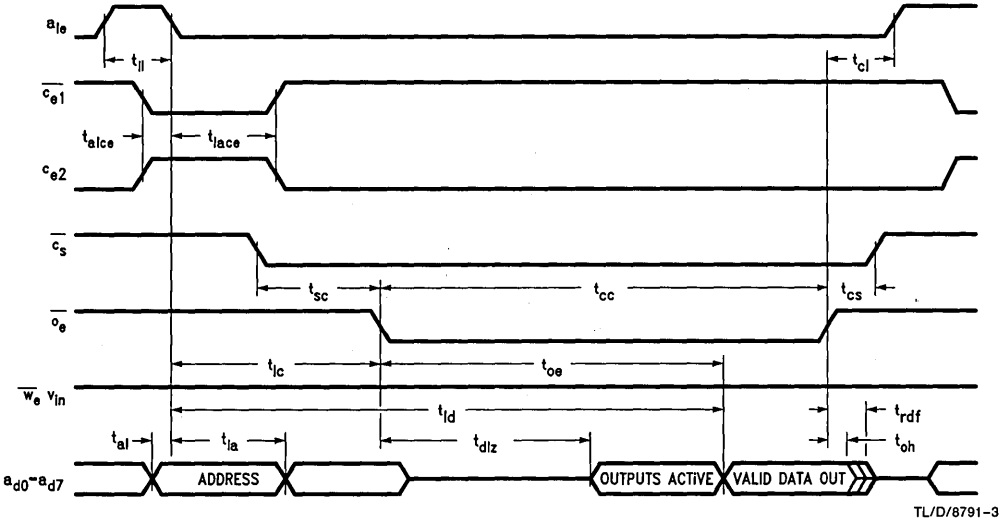


FIGURE 1. Read Timing

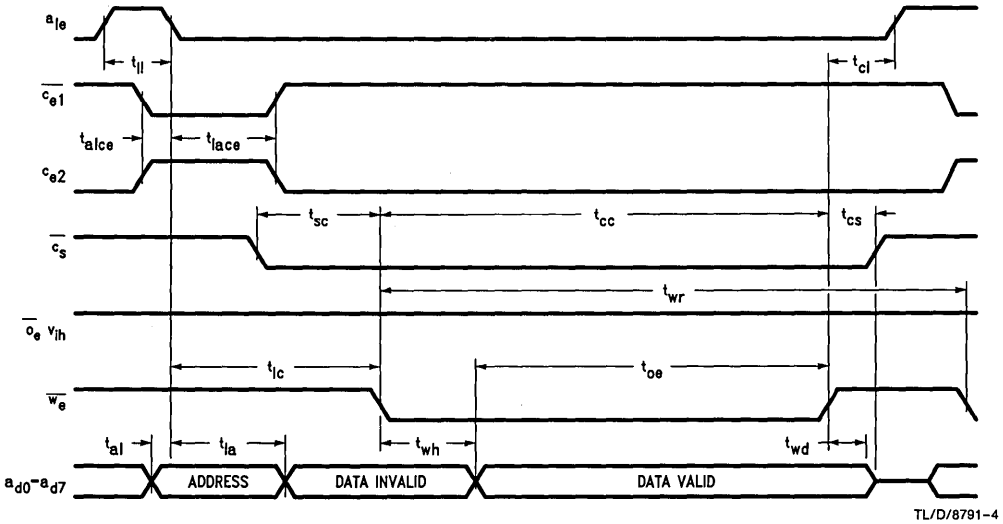
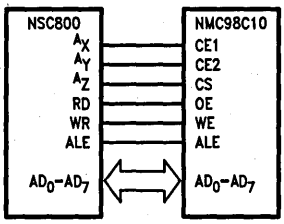


FIGURE 2. Write Timing

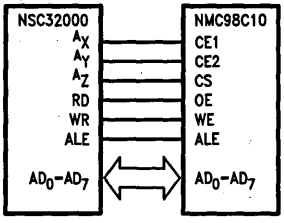
Timing Waveforms (Continued)



TL/D/8791-5

Note: A_X, A_Y, A_Z are any three of the 8051 address pins A8–A15. By connecting $\overline{CE1}$, CE2, and CS to specific address lines. The NMC98C10 and NMC98C40 can be mapped to a particular range in memory, without the need for an external memory address decoder.

FIGURE 3. Using the NMC98C10 with an NSC800 Microcontroller



TL/D/8791-6

FIGURE 4. Using the NMC98C10 with the HPC 16040 Microcontroller or NSC32000

Electronic Compass Calibration Made Easy With E^2 Memory, NMC9306

National Semiconductor Corp.
Application Brief 18
Doug Zrebski

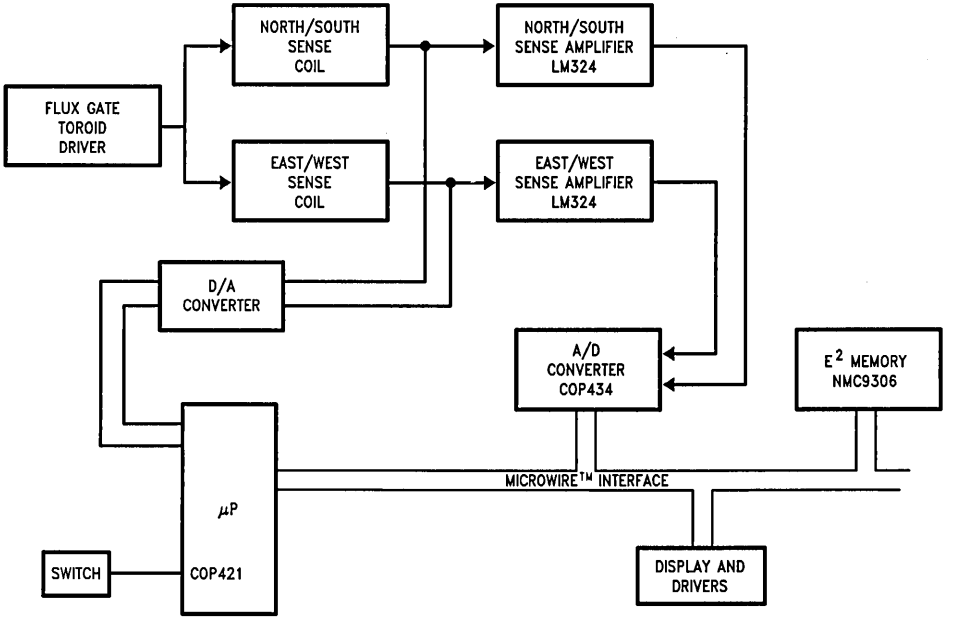
When a compass is first installed in a vehicle, or when new equipment, such as car speakers, are added to a vehicle with a compass, the compass must be compensated for stray magnetic fields. With a magnetic compass, it must be pointed towards magnetic north and then adjusted. This procedure is repeated at all four main points of the compass until the compass is calibrated. This procedure is lengthy and also requires another calibrated compass to point the vehicle in the correct direction.

The block diagram illustrates an electronic compass that, with the aide of an E^2 memory, makes adjusting a compass as easy as pushing a button, and also eliminates the need for another compass. In addition it gives you the ability to adjust for variation between magnetic and true north. This is a major advantage because it is something that even the most expensive magnetic compass cannot do.

The brain of the electronic compass is the COP421 microcontroller. There are two sense coils, one for north/south and one for east/west. The output of each of the sense amplifiers is an analog voltage which is fed into the A to D converter. These voltages are read by the COP421 over the microwire interface. From these voltages, the microcontroller determines the direction and displays the results once again over the microwire interface. To compensate the compass in a new environment the procedure is very simple. Start by pointing the car in any direction and push the switch. The CPU at this time will measure the voltage at the sense amplifiers and store this information in the E^2 memory over the microwire interface. Now the vehicle is turned 180°C, and the button is pushed again. The same procedure will be followed internally. The compensation procedures are now complete. During operation the CPU will compensate for stray fields by adding an analog voltage back into the sense amplifiers. This value is stored in E^2 memory and not lost when the power is turned off, but is readjustable if its environment is modified.

Compass variation is the difference between true and magnetic north. This variation differs all over the world and is something that must be taken into consideration when navigating by compass. With the E^2 memory device, a variance can be programmed in for any given location. In California this is approximately 17°, in Michigan approximately 1°. Once again, this cannot be accomplished by a magnetic compass, and would have been impossible to accomplish without an E^2 memory device.

Electronic Compass Block Diagram



TL/D/8613–1

NMC9346

National Semiconductor Corp.
Application Brief 22
Kent Brooten

Ths application brief describes the use of the NMC9346 (64 x 16) serial EEPROM. With the advent of the inexpensive COPS™ family from National Semiconductor, heretofore "expensive" applications can now be realized inexpensively. Such an application is a low cost thermostat. Typical features of such a device are:

1) Ability to interface to local and remote temperature sensors,
2) Ability to hold changeable settings,
3) Digital display of present temperature,
4) Inexpensive in high volume.

CIRCUIT DESCRIPTION

The basis of the thermostat is the COP410 microcontroller. This, with the addition of 2 ADC0854 A/D converters, an NMC9346 EEPROM and some logic for LED display, comprise an extremely versatile, yet low cost, system. The ADC0854 allows 4 channels of temperature sensors, 1 local and 3 remote. Temperature sensors used are LM34 (for readings in °F) or LM35 (for readings in °C).

While there are several possible choices for A/D converters that are MICROWIRE™ compatible, the ADC0854 was chosen because of its "settability". By presetting the "cold" temperature (i.e., when the cooling unit should come on—say 80°F) all the microcomputer has to do is to multiplex the inputs and read the data in line. Similarly, the "hot" A/D can be preset to the temperature where the furnace should come on (e.g., 60°F) and scanned in a like manner. Since the microcomputer is also keeping time of day, selecting an A/D with more "smarts" (as in the ADC0854) the software can be kept manageable and an external real time clock chip is not needed.

The EEPROM (NMC9346) holds the presettable temperature ranges (high and low settings) by day of the week. Since data is in EEPROM rather than in mask ROM, it can be changed.

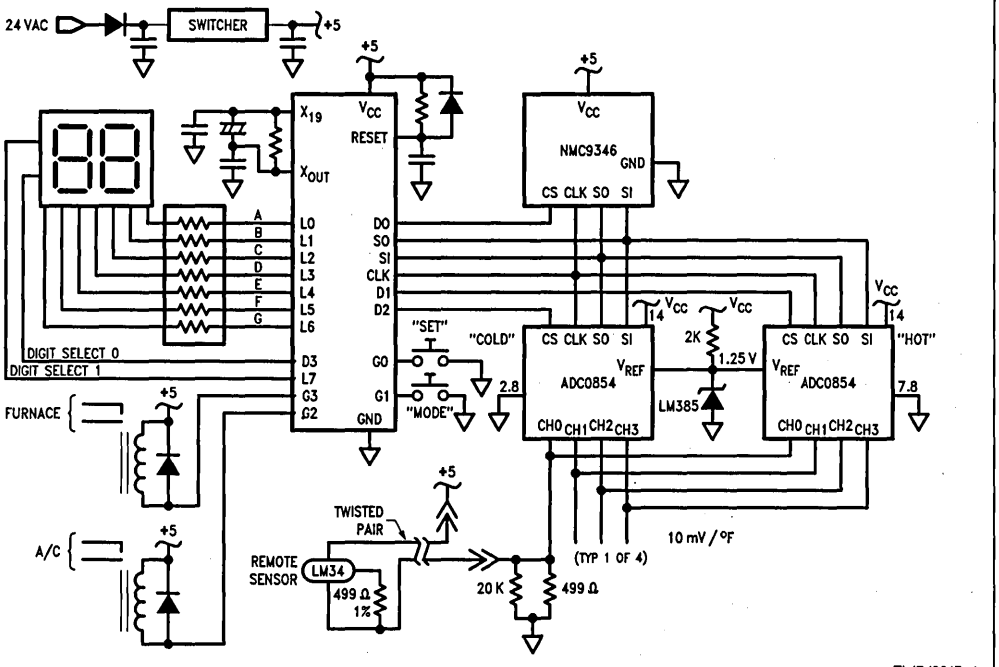
The LED display is multiplexed by the microcomputer. Depending on the type of display selected, external drivers may be necessary.

Input power is typically 24 VAC. Using a linear regulator would cause too much heat to be dissipated, which would upset the local temperature sensors. Thus, a switch mode regulator must be used. Fortunately, National Semiconductor has provided a solution to the problem with the LM3578, a switching regulator in an 8-pin mini-DIP, providing more than enough current for the application, using only a minimum of external components.

SOFTWARE DESCRIPTION

Since a real time clock is implemented in software, all routines must execute the same number of cycles independent of the input. Because of the flexibility of the COPS family instruction set, this is not as difficult a problem as it first appears. Since the EEPROM contains the settings that are periodically sent to the A/D converters, the COPS program merely fetches data from one source and dumps it to another while monitoring the output. Even the SET and MODE keys can be acted upon in a predictable manner IF the software designer carefully plans the program flow BEFORE writing code.

Note: Also see App Brief 15.



TL/D/8647–1

Figure 1

The NMC9346—An Amazing Device

National Semiconductor Corp.
Application Note 423
Stacy Deming

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NMC9346—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

2^{1024} = number of possible combinations

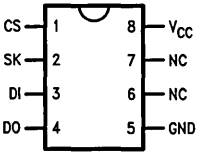
$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NMC9346 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NMC9346. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.

Dual-In-Line Package



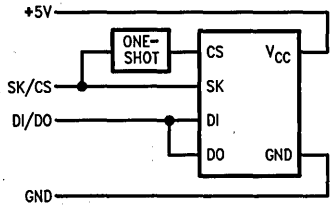
TL/D/8611–1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NMC9346 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

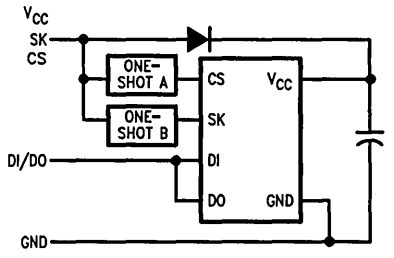


TL/D/8611–2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NMC9346 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611–3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

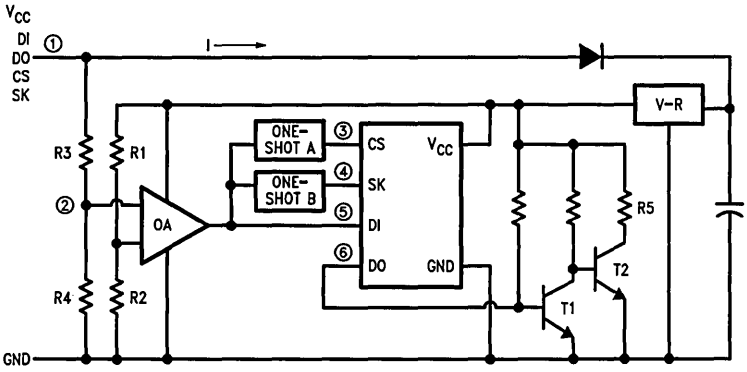
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

Conclusion

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

Note: The circuits in this application note feature the NMC9346. The NMC9306 is a pin-compatible part that stores 256 bits. The NMC9346 was used because it has a self-timing write cycle and the NMC9306 does not. Additional circuitry is not required to use the NMC9306, but an additional chip select signal must occur at the CS pin to terminate a write cycle.



TL/D/8611–4

R1 = 20K

R2 = 30K

R3 = 15K

R4 = 5K

One-Shot A = ½ MM74HC123

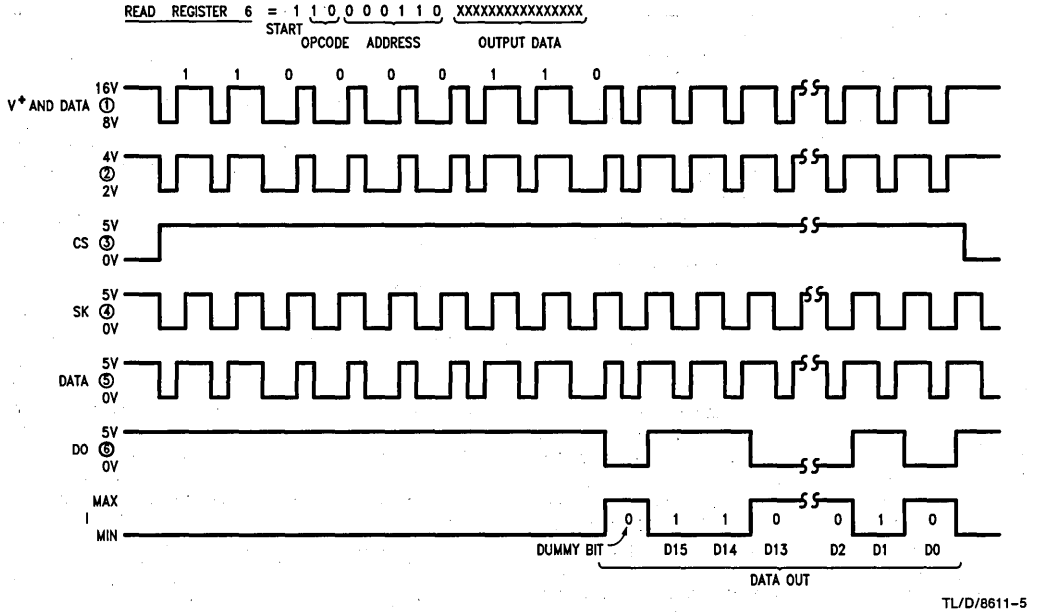
One-Shot B = ½ MM74HC123

V-R = LM2930Z-5.0

OA = LM358

R5 = 1600Ω

FIGURE 4



TL/D/8611–5

FIGURE 5

An Easy/Low Cost Serial EEPROM Interface

National Semiconductor Corp.
Application Note 431
Pat Webster

INTRODUCTION

Designers have resisted using a low cost serial EEPROM because of the uncommon interface required. The added components and circuitry have caused many engineers to resort to a larger parallel EEPROM, even when only a few bytes of non-volatile memory were required.

National Semiconductor has a design that is low in support components and takes advantage of a UART with a 1× external clock. This circuit is useful for DIP switch replacement as well as for a permanent record of the UART's communications activity. It can also be used as a security lock. Ease of interface offers the engineer a low cost solution.

THEORY OF OPERATION

Ordinarily small EEPROMs have been used to replace the DIP switch commonly found in microprocessor circuits. Just as common in such designs are UARTs, and the given application takes advantage of this for ease of interface. Because address decoding and microprocessor bus interfacing have already been accomplished, the UART is an ideal support interface for a serial EEPROM. The only true requirements for a serial EEPROM are the serial data path, clock timing, and chip select signal. All of these signals are derived from a UART in this application.

The Data In for the EEPROM is the transmitted data of the UART. Data Out of the EEPROM is directed to the receive data line of the UART. The chip select required by the EEPROM is a modem control line whose level is used to select either the modem device or the EEPROM. Finally, the serial clock required by the EEPROM can be a 1× clock provided by the UART.

THE WRITE CYCLE

When a write cycle is desired, the UART must be set up for an external 1× clock, 8 data bits, 1 stop bit, no parity and RTS must be programmed for a high output prior to data transmissions. It is also necessary to insure that the transmit buffer has been completely emptied of all prior bytes.

Before data can be written, an erase cycle to the desired address must first take place. This can be accomplished by loading the UART transmit register with an A0, A1, A2, A3, XX11 (e.g., an 03_H would result in location 0 being erased). After the transmit shift register has emptied, RTS should be returned to a low state and an erase/write programming time of 30 ms must elapse.

To write data requires that an address-op byte and two data bytes be loaded in the transmit holding register as soon as the holding register becomes empty. Table I shows the relationship of bits as they travel from the micro to the UART and finally to the EEPROM. The MSB 4 bits of the last byte written will not be saved by the EEPROM due to the 16-bit storage ability of the part. As the UART inserts start and stop bits, a total of 4 bits is saved in the EEPROM that are not usable by the microprocessor but are required by the UART.

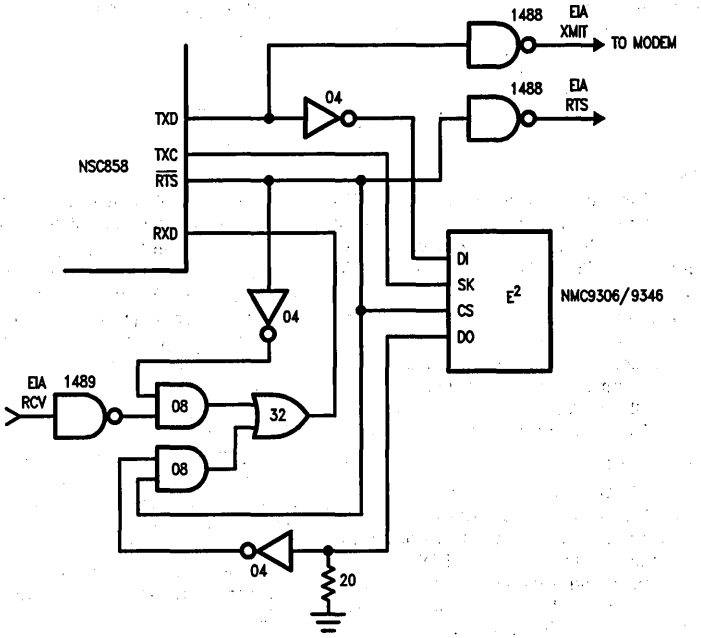
THE READ CYCLE

As was true for the write cycle, the UART must be set up for 8 data bits, 1 stop bit, and an external 1× clock. To start the read cycle, a byte with read op and address must be written to the UART. An example of read location 0 would be 01_H. After the transmit shift register has emptied, the receiver shift register will begin to accumulate the data that was written and two reads will be required before the operation can be considered complete.

CONCLUSION

For a further understanding of this interface, refer to the NMC9306/9346 and the NSC858 data sheets. Parity could be added for data integrity with further sacrifice of usable data bits in the EEPROM and the possibility of the second byte read being in parity error.

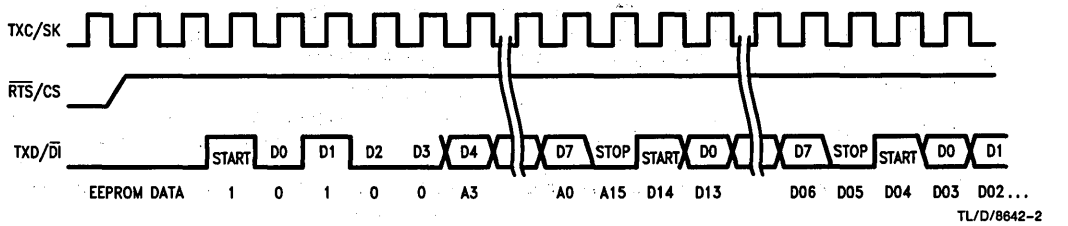
UART/EEPROM Interface



TL/D/8642-1

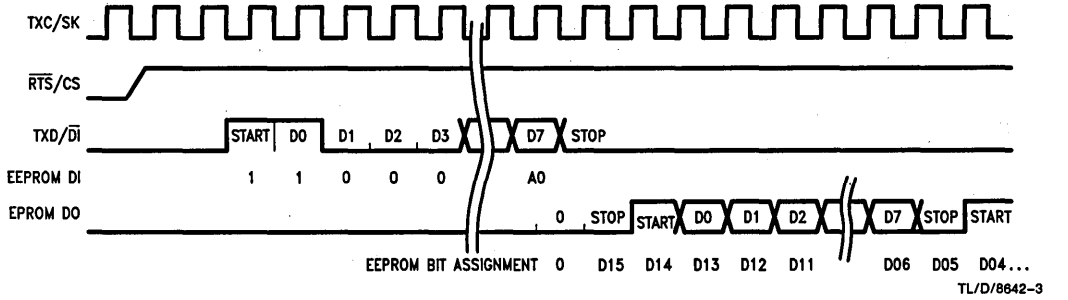
UART/EEPROM Timing

Write Cycle (9306)



TL/D/8642-2

Read Cycle



TL/D/8642-3

Table I

	Micro Data	UART XMIT Data		EEPROM
	—	Start-Bit		1
1st Byte	D0	0		0
	D1	1	Command	1
	D2	0	(Write)	0
	D3	0		0
	D4	A3		A3
	D5	A2		A2
	D6	A1		A1
	D7	A0		A0
	—	Stop-Bit		D15
	—	Start-Bit		D14
2nd Byte	D0	*ED0		D13
	D1	ED1		D12
	D2	ED2		D11
	D3	ED3		D10
	D4	ED4		D09
	D5	ED5		D08
	D6	ED6		D07
	D7	ED7		D06
	—	Stop-Bit		D05
	—	Start-Bit		D04
	D0	ED8		D03
	D1	ED9		D02
	D2	ED10		D01
	D3	ED11		D00
	D4	N/A		N/A
	D5	N/A		N/A
	D6	N/A		N/A
	D7	N/A		N/A
	—	Stop-Bit		N/A

*EDXX = Usable EEPROM Data

Using the NMC9306 for Configuration and Production Information in a TMP Based Terminal System

National Semiconductor Corp.
Application Note 433
Richard Yair

ABSTRACT

This application note gives a detailed description of the use of the NMC9306 E²PROM in a TMP based environment. The function of the E²PROM is to contain all the configuration data for the terminal (i.e., baud rate, auto dial numbers, function selects, etc.) and also production information (i.e., serial number, date of manufacture, etc.)

INTRODUCTION

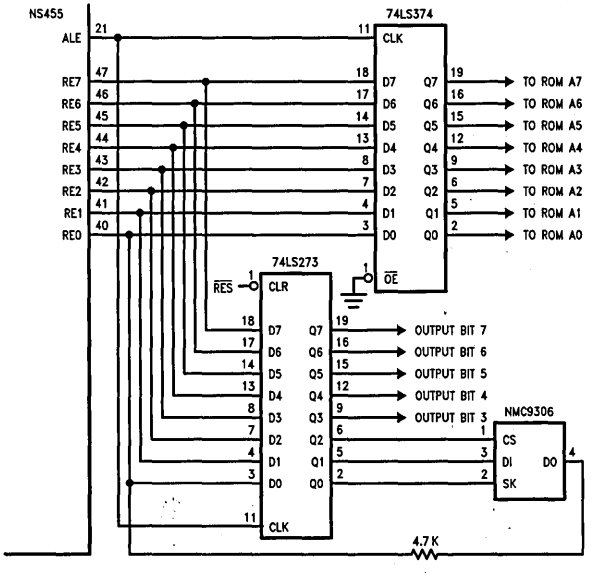
In a computer terminal environment, there are many user selectable options that need to be strapped into the terminal before it can be used. Some terminals have modems built into them that can automatically dial numbers for you. Some terminals can even emulate several different industry standard terminals, all in one. This configuration information is usually programmed into the terminal by using DIP switches accessed through some access cover or by removing a certain panel. A major drawback to this type of configuring is that the terminal must be opened by the user if they are to change the strapping. Another disadvantage is the terminal usually cannot be changed dynamically. Enter NON-VOLATILE RAM or battery-backed-up RAM. This creates another problem in that the system cost is increased, reliability suffers, and board space may not be available. Enter NMC9306 serial E²PROM in an 8-pin Mini-DIP. This device is not only non-volatile, but is small, inexpensive, and simple to use.

HARDWARE MAIN DESCRIPTION

Since the NS455 Terminal Management Processor (TMP) does not have a MICROWIRE™ interface, another method of interfacing must be devised. The TMP has provisions for an external output port attached to the ROM bus which can be used to simulate the MICROWIRE interface. This is done by using three free data bits of a 74LS273 as shown in *Figure 1.* These three bits will be the CHIP SELECT, CLOCK, and the DATA IN inputs to the NMC9306. The TMP also has an input port enable pin that can be used to read a set of buffers such as a 74LS244. A single pin can be used for the DATA OUT signal from the NMC9306 as shown in *Figure 2.* If no input port is required, the DATA OUT signal can be driven directly onto the ROM expansion bus through a 4.7k resistor as shown in *Figure 1.* This is all the hardware that is required to interface the part.

SOFTWARE MAIN DESCRIPTION

This is where things get a bit tricky. Routines must be written to communicate with the NMC9306. These routines must read, write, erase, and enable erase/write in the NMC9306 by simulating the MICROWIRE interface. This is done by turning the output ports pins on and off with the correct timing to simulate the interface without interfering with the other pins. Also, the input data must be converted to usable form as well as converting the outgoing data to serial form. Simple.



TL/D/8644–1

FIGURE 1

To start, there are a few things to be mentioned. The TMP has a modified 8048 processor for its controller. This controller has a 16-bit accumulator, addressed as two 8-bit registers, which are ACC and HACC. The high accumulator (HACC) is accessed through the low accumulator (ACC). This is important since the NMC9306 is arranged in 16 words of 16 bits each. Also, to allow the port to be modified without changing any unwanted bits, a PORT MASK must be defined in the memory of the TMP. Any change to the port should be done by updating the mask, and then sending the mask data to the port. This will also make testing the data on the port possible. The codes for communicating with the NMC9306 can be obtained from the *National Semiconductor 1984 MOS Memory Databook* in Section 7. Also, all critical timing parameters are described therein.

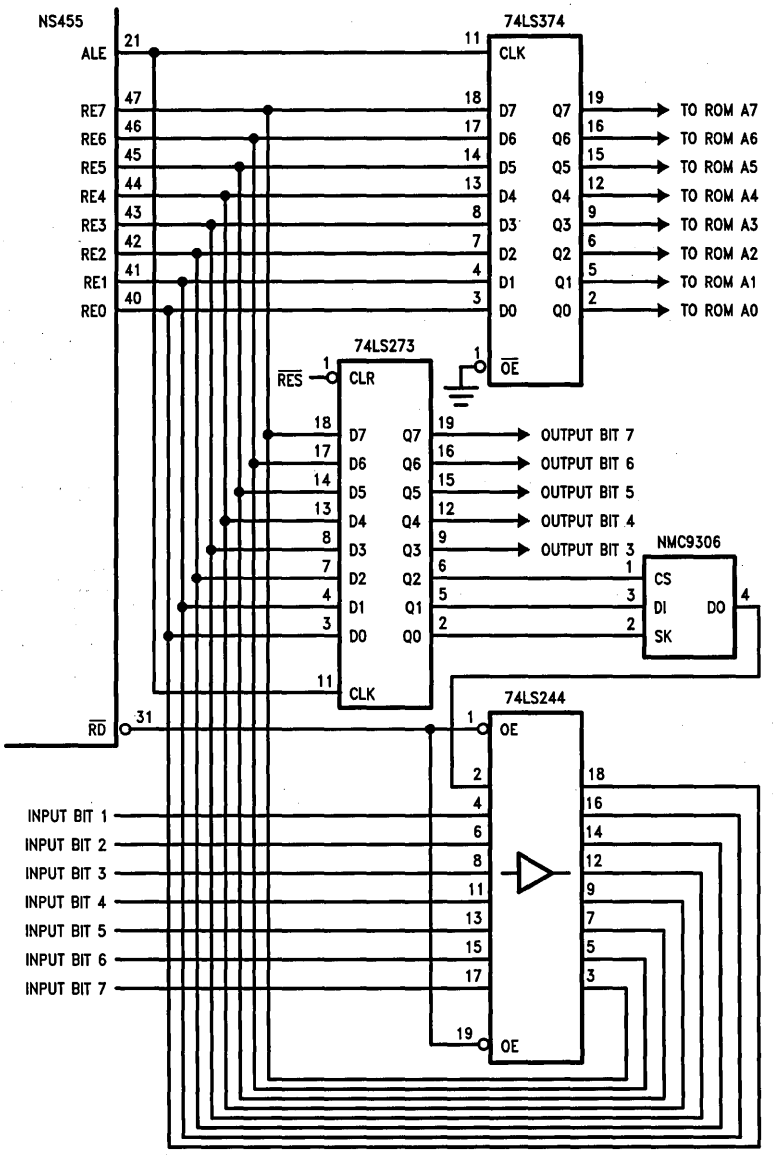
In a typical TMP system, there are large amounts of configuration data that must be set up before the terminal can communicate properly. If the system is really complex, it may need more yet. A typical configuration map is shown below. Along with the configuration data, production information should be included. This may be entered by some code at power-up that is not documented in the end user guide. This set-up screen may ask for the date of assembly, the assembly location code, the serial number, the customer code, the options enabled (tricky sales pitch— "for only $50 more . . . "), the number of times the unit was returned to the factory for service, and any other data that must be tracked for production. If the NMC9306 does not have enough room, the NMC9346 is 4 times larger, and has the same hardware requirements. Only slight software changes are required.

Typical Configuration Map

Location (Hex)		Description
0	Bit 0	Cursor Blink Enable
	Bit 1	Cursor Underline/Block
	Bit 2	Cursor Inverts Video On
	Bit 3	Screen Norm/Inverse Vid
	Bit 4	Local Mode On/Off
	Bit 5	Status Line Enable
	Bits 6–F	(Spare)
1	Bits 0–3	Baud Rate
	Bit 4	1 or 2 Stop Bits
	Bit 5	7 or 8 Data Bits
	Bit 6	Parity On/Off
	Bit 7	Odd or Even Parity
	Bits 8–F	(Spare)
2	Bits 0–F	(Spare)
3	Bits 0–F	Month and Year of Assem.
4	Bits 0–7	Day of Assembly
	Bits 8–F	Assembly Location
5	Bits 0–7	Inspector Code
	Bits 8–F	No. of Returns
6	Bits 0–F	Serial Number (MSW)
7	Bits 0–F	Serial Number
8	Bits 0–F	Serial Number (LSW)
9	Bits 0–7	Failure Code 1
	Bits 8–F	Failure Code 2
A	Bits 0–F	Check Sum
B–F		(Spare)

CONCLUSION

It can be seen that the NMC9306 is simple, yet functional in replacing strapping switches and enhancing the product. The NMC9306/NMC9346 components in this application, replace more costly and larger parts, and are easily integrated into a TMP or other terminal design. The end product will be more versatile through enhanced user interface and tracking of important production data.



TL/D/8644–2

FIGURE 2

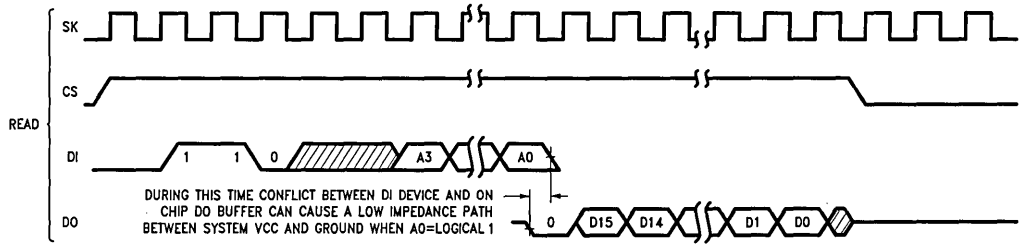
Common I/O Applications of NMC9306/COP494 and NMC9346/COP495 Non-Volatile Serial Access Memories

National Semiconductor Corp.
Application Note 481

NMC9306/COP494 and NMC9346/COP495 are serial access non-volatile memories designed for a 4-wire (MICROWIRE™) interface; Chip Select (CS) input, clock (SK) input, serial data input (DI), and serial data output (DO). Since DO is in TRI-STATE® while instructions, address and data are being shifted into the chip on the DI signal line, DI and DO can be tied together as a common I/O to further simplify the interface. However, the following potentially troublesome situations should be kept in mind and dealt with according to these recommendations:

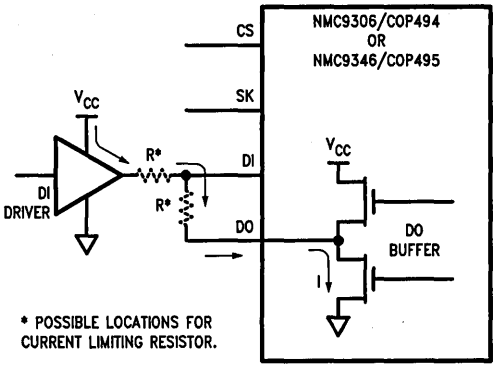
NMC9306/COP494

While clocking in a READ instruction, approximately 500 ns (typical) after the least significant bit (A0) of the register address is clocked into the chip by the rising edge of SK, DO comes out of TRI-STATE and goes low (logical '0') as a dummy bit to signal the start of the data output string *(Figure 1).* In a common I/O application, if A0 is a logical '1' and is still driving DI when the dummy bit becomes valid, a low impedance path between the power supply and ground is created through the DI driver and the on-chip DO buffer *(Figure 2).* If measures are taken to minimize the short circuit current, e.g., by inserting a current limiting resistor between the DI driver and the chip *(Figure 2),* the part will continue to work normally since A0 is clocked onto the chip before this potential disturb condition occurs.



TL/D/9213–1

FIGURE 1. Read Instruction in Common I/O Configuration



TL/D/9213–2

FIGURE 2. Current Path during DI Driver and DO Buffer Conflict during Read Instruction

NMC9346/COP495

The NMC9346/COP495 has a self-timed programming cycle which uses DO to indicate the ready/busy status of the chip. Therefore, in addition to the potential problem in the READ mode similar to NMC9306/COP494 described above, another pitfall may be encountered at the end of a programming cycle in common I/O applications.

The self-timed programming cycle is initiated by the falling edge of CS after a programming instruction (ERASE,

WRITE, ERAL, WRAL) is shifted in. If CS is brought high subsequently, after a minimum of 1 μs (tcs), DO indicates the ready/busy status of the chip. DO = logical '0' indicates that programming is still in progress. DO = logical '1' signals the end of the programming cycle. This 'status check' function of DO is cancelled (i.e., DO returns to TRI-STATE) when a logical '1' on DI is clocked into the chip by SK with CS high. With separate input and output this is automatically accomplished by the start bit of the next instruction *(Figure 3)*.

In a common I/O application, the following clocking sequence is recommended to avoid premature cancellation of the 'ready' status and/or interference of the 'ready' status with the serial input sequence for the next instruction *(Figure 4)*:

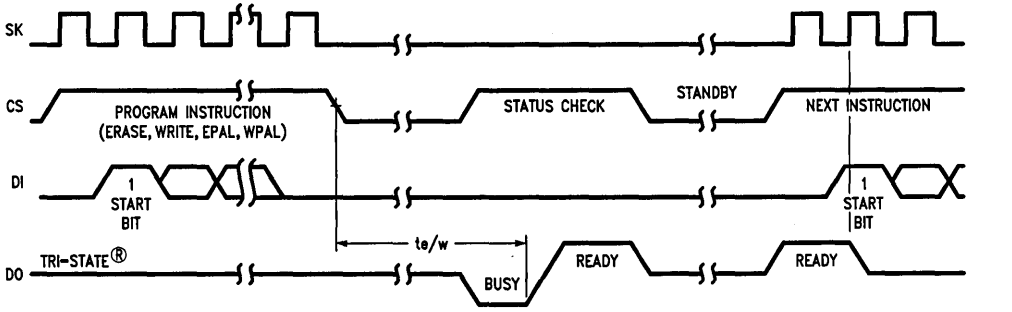
1) Inhibit the SK clock after clocking in the programming instruction.
2) After acknowledging the 'ready' status, clock SK once while the common I/O is still high to cancel the ready/busy status function of DO.
3) Bring CS low for a minimum of 1 μs (tcs) to clear the instruction register before initiating the next instruction.

DO is now reset back to TRI-STATE, and the chip is ready to accept the next instruction.

The chip may enter the 'ready' status mode under certain conditions of V_{CC} power-up. This occurs due to the V_{CC} power-up conditions setting the status mode logic on the chip, and is not an indication of a spurious programming cycle on V_{CC} power-up. The following clocking sequence is recommended to ensure cancellation of this status signal after V_{CC} power-up *(Figure 5)*:

1) Bring CS high.
2) Clock SK once to ensure cancellation of the 'ready' status.
3) Bring CS low for a minimum of 1 μs (tcs) to clear the instruction register before initiating the first instruction.

NMC9346 Timing Diagrams



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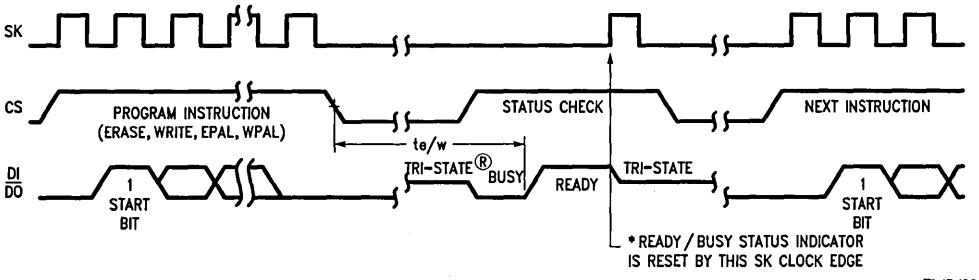
*The Ready/Busy Status Indicator for a program instruction (ERASE, WRITE, ERAL, WRAL) is reset when the Start bit for the following instruction is clocked in.

FIGURE 3. Programming Cycle with 4-Wire Interface

NMC9346 Timing Diagrams (Continued)



TL/D/9213–4

FIGURE 4. Recommended Programming Cycle in Common I/O Configuration

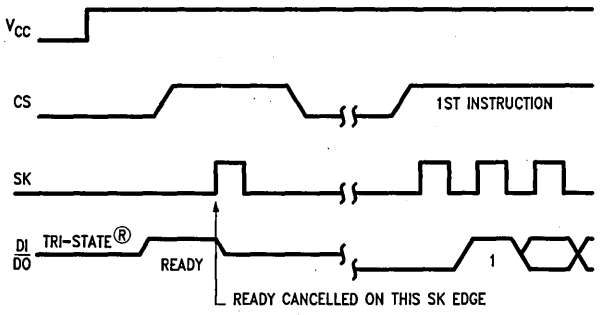


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FIGURE 5. Recommended Clocking Sequence on V_{CC} Power-Up in Common I/O Configuration

Error Detection and Correction Techniques for National Semiconductor's EEPROM Products

National Semiconductor Corp.
Application Note 482

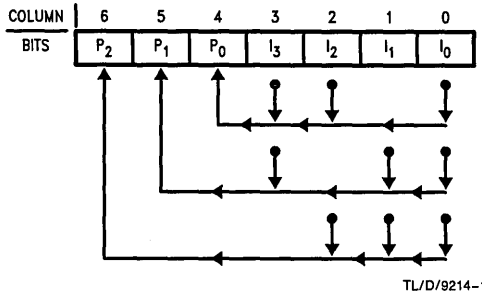
This application note provides the non-volatile memory system designer who cannot tolerate the very low failure rate associated with National Semiconductor's E²PROMs, with a method to assure data integrity and extend the life span of the product.

With a minimum additional parts cost, the following error detection and correction techniques allow the designer to extend the usable life of an EEPROM device. The technique is applicable for applications requiring 100,000 or more erase/write cycles per register.

All EEPROMs fail with extended erase/write cycling. National Semiconductor EEPROMs fail in a statistically predictable and well behaved fashion as the number of erase/write cycles increase. The failure of one bit cell does not influence the operation of adjacent bit cells. Since bit failure is a gradual wearout phenomenon which only affects discrete cell locations one at a time, it is possible to apply simple encoding techniques which can determine the locations of cell failures so that faltering memory addresses can be avoided in the future.

Single parity checking is the simplest way to check for errors in a binary code. In a parity checking system an extra-parity-bit is chosen so that the number of 1s in the block of data, including the parity bit, is even. In practice this is accomplished using modulo 2 addition (i.e., 0 + 0 = 0; 0 + 1 = 1; 1 + 0 = 1; 1 + 1 = 0; 0 + 0 + 1 = 1; etc.). Modulo 2 addition is quickly accomplished through an exclusive OR gate. When the data is read back, the number of ones are counted and the sum is checked to see if it is odd or even. An odd sum is an indication that an error occurred in the data. This method of single parity checking can detect the occurrence of an error in a block but it cannot be used to determine the exact location of the error to correct the bad data.

A natural extension of single parity checking is the Hamming code. A Hamming code uses several parity checks, instead of just one. This allows errors to be corrected as well as detected. Using bits in blocks of 7, where 4 of the bits are information and 3 are parity allows for error detection and correction of any single bit within the block, including the parity bits themselves.



TL/D/9214–1

FIGURE 1. Computation Scheme for Parity Bits Using Hamming Code

The initial parity is calculated as shown in *Figure 1.* The parity bits are in columns 4, 5 and 6, while the actual information bits are in columns 0, 1, 2, and 3. The contents of each parity bit comes from summing the contents of a unique combination of three of the four information bits. The parity bit is chosen so that this sum will be an even number when added to the parity bit itself. Notice that each one of the parity bits calculates its contents by using different combinations of the data bits. Every data bit in the block has its information read at least twice. Using this overlapping scheme is what allows the code to correct errors.

Since there are only 4 bits of information there can be only $2^4 = 16$ possible combinations of 1s and 0s. These 16 possible correct combinations are listed on the code word table in Table I. When the encoded block is read back from memory, the same parity coding scheme is used again on the information bits and compared to the original parity bits. This forms what is called a syndrome. If any errors have occurred in the 7-bit block their locations can be determined and the errors corrected. Table II shows the decoding matrix which is used on the syndromes to determine the location of an error. If no errors occurred the syndrome will be 000. Table III shows all the combinations of the 7-bit block. Note that there are only 128 possible variations of 1s and 0s in the block: (7 mistake combinations per block + 1 correct combination per block) × (16 possible block combinations). All these combinations can be stored in a table and called up quickly to check for possible data errors without the need to even create a syndrome upon reading a word. For example, suppose we want to store the data 1000. From Table I we see that the 7-bit block would be 1111000 after the Hamming code had been applied. If information bit 3 for example goes bad, then the new block would read 1110000. This is case number 112 in Table III, and we see that the correct information is 1000. With Table III available in the computer memory, the received codeword can be corrected automatically. An array of 128 bytes can provide both the corrected information and the syndrome information.

The 7-bit codeword works nicely with National Semiconductor's serial EEPROMs because they are organized as arrays of 16-bit registers. Each 16 bit register is modified or accessed with a simple-serial protocol. The 16-bit unit can be partitioned two eight-bit bytes. Each byte can contain a seven-bit codeword and one-bit flag that indicates whether an error has been previously detected in the byte. This scheme provides one byte of error corrected information per 16-bit register. Slightly more elaborate systems can be used which will detect and correct more errors if additional parity bits are added to the data.

TABLE I. Encoding Table for Hamming Code

Sixteen Code Words							
	Parity Bits			Information Bits			
	P 2	P 1	P 0	I 3	I 2	I 1	I 0
0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	1
2	1	0	1	0	0	1	0
3	0	1	1	0	0	1	1
4	0	1	1	0	1	0	0
5	1	0	1	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	0	1	1	1
8	1	1	1	1	0	0	0
9	0	0	1	1	0	0	1
10	0	1	0	1	0	1	0
11	1	0	0	1	0	1	1
12	1	0	0	1	1	0	0
13	0	1	0	1	1	0	1
14	0	0	1	1	1	1	0
15	1	1	1	1	1	1	1

TABLE II. Syndrome Decoding Table for Hamming Code

Syndrome			Meaning
0	0	0	No error detected
0	0	1	Check bit 0 in error
0	1	0	Check bit 1 in error
0	1	1	Information bit 2 corrected
1	0	0	Check bit 2 in error
1	0	1	Information bit 1 corrected
1	1	0	Information bit 0 corrected
1	1	1	Information bit 3 corrected

With this added data protection the reliability of EEPROMs can be extended because the probability of two or more cells failing on the same codeword is low. To illustrate the Hamming code, an experiment on 16 devices with 1k bits each was conducted. The experiment results are shown in Table IV. While the first bit failure was detected somewhere between 12,589 and 15,849 cycles, the Hamming code just described would have protected against the loss of data until somewhere between 79,433 and 100,000 erase/write cycles. Notice that 55 bit failures were indicated when the first Hamming code failure was detected. This is to be expected because a Hamming failure will not occur until two or more bits within a particular group of seven bits have failed.

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code

	Received Codeword							Syndrome Bits			Corrected Information			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	0	0	0	0	0
2	0	0	0	0	0	1	0	1	0	1	0	0	0	0
3	0	0	0	0	0	1	1	0	1	1	0	1	1	1
4	0	0	0	0	1	0	0	0	1	1	0	0	0	0
5	0	0	0	0	1	0	1	1	0	1	0	1	1	1
6	0	0	0	0	1	1	0	1	1	0	0	1	1	1
7	0	0	0	0	1	1	1	0	0	0	0	1	1	1
8	0	0	0	1	0	0	0	1	1	1	0	0	0	0
9	0	0	0	1	0	0	1	0	0	1	1	0	0	1
10	0	0	0	1	0	1	0	0	1	0	1	0	1	0
11	0	0	0	1	0	1	1	1	0	0	1	0	1	1
12	0	0	0	1	1	0	0	1	0	0	1	1	0	0
13	0	0	0	1	1	0	1	0	1	0	1	1	0	1
14	0	0	0	1	1	1	0	0	0	1	1	1	1	0
15	0	0	0	1	1	1	1	1	1	1	0	1	1	1
16	0	0	1	0	0	0	0	0	0	1	0	0	0	0
17	0	0	1	0	0	0	1	1	1	1	1	0	0	1
18	0	0	1	0	0	1	0	1	0	0	0	0	1	0
19	0	0	1	0	0	1	1	0	1	0	0	0	1	1
20	0	0	1	0	1	0	0	0	1	0	0	1	0	0
21	0	0	1	0	1	0	1	1	0	0	0	1	0	1
22	0	0	1	0	1	1	0	1	1	1	1	1	1	0
23	0	0	1	0	1	1	1	0	0	1	0	1	1	1
24	0	0	1	1	0	0	0	1	1	0	1	0	0	1
25	0	0	1	1	0	0	1	0	0	0	1	0	0	1
26	0	0	1	1	0	1	0	0	1	1	1	1	1	0
27	0	0	1	1	0	1	1	1	0	1	1	0	0	1
28	0	0	1	1	1	0	0	1	0	1	1	1	1	0
29	0	0	1	1	1	0	1	0	1	1	1	0	0	1
30	0	0	1	1	1	1	0	0	0	0	1	1	1	0
31	0	0	1	1	1	1	1	1	1	0	1	1	1	0

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
32	0	1	0	0	0	0	0	0	1	0	0	0	0	0
33	0	1	0	0	0	0	1	1	0	0	0	0	0	1
34	0	1	0	0	0	1	0	1	1	1	1	0	1	0
35	0	1	0	0	0	1	1	0	0	1	0	0	1	1
36	0	1	0	0	1	0	0	0	0	1	0	1	0	0
37	0	1	0	0	1	0	1	1	1	1	1	1	0	1
38	0	1	0	0	1	1	0	1	0	0	0	1	1	0
39	0	1	0	0	1	1	1	0	1	0	0	1	1	1
40	0	1	0	1	0	0	0	1	0	1	1	0	1	0
41	0	1	0	1	0	0	1	0	1	1	1	1	0	1
42	0	1	0	1	0	1	0	0	0	0	1	0	1	0
43	0	1	0	1	0	1	1	1	1	0	1	0	1	0
44	0	1	0	1	1	0	0	1	1	0	1	1	0	1
45	0	1	0	1	1	0	1	0	0	0	1	1	0	1
46	0	1	0	1	1	1	0	0	1	1	1	0	1	0
47	0	1	0	1	1	1	1	1	0	1	1	1	0	1
48	0	1	1	0	0	0	0	0	1	1	0	1	0	0
49	0	1	1	0	0	0	1	1	0	1	0	0	1	1
50	0	1	1	0	0	1	0	1	1	0	0	0	1	1
51	0	1	1	0	0	1	1	0	0	0	0	0	1	1
52	0	1	1	0	1	0	0	0	0	0	0	1	0	0
53	0	1	1	0	1	0	1	1	1	0	0	1	0	0
54	0	1	1	0	1	1	0	1	0	1	0	1	0	0
55	0	1	1	0	1	1	1	0	1	1	0	0	1	1
56	0	1	1	1	0	0	0	1	0	0	1	0	0	0
57	0	1	1	1	0	0	1	0	1	0	1	0	0	1
58	0	1	1	1	0	1	0	0	0	1	1	0	1	0
59	0	1	1	1	0	1	1	1	1	1	0	0	1	1
60	0	1	1	1	1	0	0	1	1	1	0	1	0	0
61	0	1	1	1	1	0	1	0	0	1	1	1	0	1
62	0	1	1	1	1	1	0	0	1	0	1	1	1	0
63	0	1	1	1	1	1	1	1	0	0	1	1	1	1
64	1	0	0	0	0	0	0	1	0	0	0	0	0	0
65	1	0	0	0	0	0	1	0	1	0	0	0	0	1
66	1	0	0	0	0	1	0	0	0	1	0	0	1	0
67	1	0	0	0	0	1	1	1	1	1	1	0	1	1
68	1	0	0	0	1	0	0	1	1	1	1	1	0	0
69	1	0	0	0	1	0	1	0	0	1	0	1	0	1
70	1	0	0	0	1	1	0	0	1	0	0	1	1	0
71	1	0	0	0	1	1	1	1	0	0	0	1	1	1
72	1	0	0	1	0	0	0	0	1	1	1	1	0	0
73	1	0	0	1	0	0	1	1	0	1	1	0	1	1
74	1	0	0	1	0	1	0	1	1	0	1	0	1	1
75	1	0	0	1	0	1	1	0	0	0	1	0	1	1
76	1	0	0	1	1	0	0	0	0	0	1	1	0	0
77	1	0	0	1	1	0	1	1	1	0	1	1	0	0
78	1	0	0	1	1	1	0	1	0	1	1	1	0	0
79	1	0	0	1	1	1	1	0	1	1	1	0	1	1

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							Syndrome Bits			Corrected Information			
80	1	0	1	0	0	0	0	1	0	1	0	0	1	0
81	1	0	1	0	0	0	1	0	1	1	0	1	0	1
82	1	0	1	0	0	1	0	0	0	0	0	0	1	0
83	1	0	1	0	0	1	1	1	1	0	0	0	1	0
84	1	0	1	0	1	0	0	1	1	0	0	1	0	1
85	1	0	1	0	1	0	1	0	0	0	0	1	0	1
86	1	0	1	0	1	1	0	0	1	1	0	0	1	0
87	1	0	1	0	1	1	1	1	0	1	0	1	0	1
88	1	0	1	1	0	0	0	0	1	0	1	0	0	0
89	1	0	1	1	0	0	1	1	0	0	1	0	0	1
90	1	0	1	1	0	1	0	1	1	1	0	0	1	0
91	1	0	1	1	0	1	1	0	0	1	1	0	1	1
92	1	0	1	1	1	0	0	0	0	1	1	1	0	0
93	1	0	1	1	1	0	1	1	1	1	0	1	0	1
94	1	0	1	1	1	1	0	1	0	0	1	1	1	0
95	1	0	1	1	1	1	1	0	1	0	1	1	1	1
96	1	1	0	0	0	0	0	1	1	0	0	0	0	1
97	1	1	0	0	0	0	1	0	0	0	0	0	0	1
98	1	1	0	0	0	1	0	0	1	1	0	1	1	0
99	1	1	0	0	0	1	1	1	0	1	0	0	0	1
100	1	1	0	0	1	0	0	1	0	1	0	1	1	0
101	1	1	0	0	1	0	1	0	1	1	0	0	0	1
102	1	1	0	0	1	1	0	0	0	0	0	1	1	0
103	1	1	0	0	1	1	1	1	1	0	0	1	1	0
104	1	1	0	1	0	0	0	0	0	1	1	0	0	0
105	1	1	0	1	0	0	1	1	1	1	0	0	0	1
106	1	1	0	1	0	1	0	1	0	0	1	0	1	0
107	1	1	0	1	0	1	1	0	1	0	1	0	1	1
108	1	1	0	1	1	0	0	0	1	0	1	1	0	0
109	1	1	0	1	1	0	1	1	0	0	1	1	0	1
110	1	1	0	1	1	1	0	1	1	1	0	1	1	0
111	1	1	0	1	1	1	1	0	0	1	1	1	1	1
112	1	1	1	0	0	0	0	1	1	1	1	0	0	0
113	1	1	1	0	0	0	1	0	0	1	0	0	0	1
114	1	1	1	0	0	1	0	0	1	0	0	0	1	0
115	1	1	1	0	0	1	1	1	0	0	0	0	1	1
116	1	1	1	0	1	0	0	1	0	0	0	1	0	0
117	1	1	1	0	1	0	1	0	1	0	0	1	0	1
118	1	1	1	0	1	1	0	0	0	1	0	1	1	0
119	1	1	1	0	1	1	1	1	1	1	1	1	1	1
120	1	1	1	1	0	0	0	0	0	0	1	0	0	0
121	1	1	1	1	0	0	1	1	1	0	1	0	0	0
122	1	1	1	1	0	1	0	1	0	1	1	0	0	0
123	1	1	1	1	0	1	1	0	1	1	1	1	1	1
124	1	1	1	1	1	0	0	0	1	1	1	0	0	0
125	1	1	1	1	1	0	1	1	0	1	1	1	1	1
126	1	1	1	1	1	1	0	1	1	0	1	1	1	1
127	1	1	1	1	1	1	1	0	0	0	1	1	1	1

TABLE IV. Hamming Code Experimental Demonstration on 16 Devices of 1k Bits Each

Erase/Write Cycles	Total Bit Failures	Total Codeword Failures	Percent Bit Failures	Percent Codeword Failures
1000	0	0	0.00%	0.00%
1259	0	0	0.00%	0.00%
1585	0	0	0.00%	0.00%
1995	0	0	0.00%	0.00%
2512	0	0	0.00%	0.00%
3162	0	0	0.00%	0.00%
3981	0	0	0.00%	0.00%
5012	0	0	0.00%	0.00%
6310	0	0	0.00%	0.00%
7943	0	0	0.00%	0.00%
10000	0	0	0.00%	0.00%
12589	1	0	0.01%	0.00%
15849	1	0	0.01%	0.00%
19953	1	0	0.01%	0.00%
25119	1	0	0.01%	0.00%
31623	3	0	0.02%	0.00%
39811	4	0	0.02%	0.00%
50119	10	0	0.06%	0.00%
63096	16	0	0.10%	0.00%
79433	55	1	0.34%	0.05%
100000	103	3	0.63%	0.15%

The Reliability of National Semiconductor's EEPROM Products

This applications note provides the non-volatile memory system designer with the necessary information to design reliable non-volatile memory subsystems. The first section is an introduction to EEPROM technology. Next, is a description of the intrinsic failure mechanisms common to all EEPROM devices. The third section is a description of the reliability aspects of National Semiconductor's manufacturing process.

INTRODUCTION TO EEPROM TECHNOLOGY

EEPROM Background

The Electrically Erasable Programmable Read Only Memory (EEPROM) is a non-volatile, fully static data storage device which is also electrically erasable. It can be erased and written rapidly without removing the chip from the end application system or using a PROM programmer. The technology allows for both byte- and chip-clear operations. These advantages are in contrast to UVPROMs which require removal from the system and total erasure of all the bits on the chip.

Technology Description

National Semiconductor's NMOS EEPROM devices utilize a 2.5 micron process. This technology was developed from the basic NMOS double poly process, which National Semiconductor's Memory Division has been using for about 10 years.

The new family of CMOS devices is based on National's 2 micron M^{2}CMOS process, which is the process National Semiconductor uses most widely for such diverse products as: Gate Arrays, Telecom, Microprocessing and many others. It is presently fabricated in one of the most modern, state-of-the-art, 6 inch wafer fab facilities in the world.

Device Description

National Semiconductor EEPROM devices utilize a double poly silicon gate process. *Figure 1* depicts the basic memory element in cross section. It is comprised of an N-channel transistor with an additional floating polysilicon gate sandwiched between the control gate and the transistor channel region. The gate structures are separated from each other and from the transistor channel and drain regions by silicon dioxide (SiO_2). A tunnel oxide which is less than 120 Angstroms thick is used in the region between the floating polysilicon gate and the N^+ drain region. National's E^2 Cell allows individual bit erasing and writing.

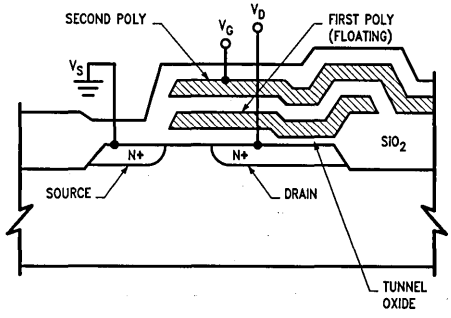


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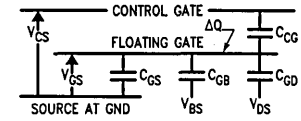
FIGURE 1. Cross Section of MOS Floating Gate EEPROM

EEPROM technology relies upon stored charge on the floating gate to retain information. Floating and control gate voltages are referenced to the source which is grounded. A mode of the equivalent capacitances and voltages for an EEPROM is shown in *Figure 2*. V_{GS} is the voltage on the floating gate, and delta Q is the charge stored on the floating gate. The charge remains on the floating gate even when power is not applied because the surrounding silicon dioxide serves as an excellent insulating material. Electrons are transferred to and from the floating gate and the underlying MOS device through a process known as Fowler-Nordheim tunneling.



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$$V_{GS} = \frac{V_{CS}C_{CG} + V_{DS}C_{GD} + V_{BS}C_{GB} + \Delta Q}{C_{GS} + C_{GB} + C_{GD} + C_{CG}}$$

FIGURE 2. Equivalent Capacitances and Voltages

Tunneling Physics

The non-volatile memory storage in EEPROMs takes advantage of a quantum mechanical phenomenon known as Fowler-Nordheim tunneling. This tunneling process is a function of the energy levels of the materials involved. A schematic of the energy configuration for an EEPROM is illustrated in *Figure 3*. The energy difference between the valence and conduction bands in silicon dioxide (SiO_2) is about 9.05 eV. The energy difference between the same two bands for silicon (Si) is approximately 1.1 eV. When the SiO_2 and the Si are joined together the conduction band of the SiO_2 is 3.25 eV above the conduction band of the Si, while the valence band of the SiO_2 lies about 4.7 eV below the valence band of the Si. Since the thermal energy of an electron at room temperature (23°C) is only 0.025 eV the likelihood of an electron jumping from the valence band of the SiO_2 to the conduction band of the SiO_2 is very slight.

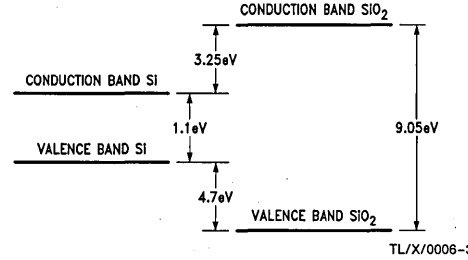

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FIGURE 3. Energy Band Diagram of the Si and SiO_2 System in its Neutral State

Fowler-Nordheim tunneling predicts that these energy bands can be distorted in the presence of an electric field. This process is depicted in *Figure 4*. In EEPROMs, tunneling of electrons occurs between the drain and floating gate through the SiO_2 tunneling region. The direction of Fowler-Nordheim tunneling of electrons through the tunneling region depends on the polarity of the voltages between the control gate and the drain. Tunneling physics predicts that when the electric fields across a thin insulator, such as SiO_2, are high enough, electrons from the negative electrode can acquire enough energy to pass or tunnel through the forbidden gap and enter the conduction band. The resulting current flux (J) is approximately proportional to an exponential function of the applied voltage (V) as illustrated in *Figure 5*. In order to obtain fields strengths large enough to initiate tunneling ($V > 7 \times 10^6$ eV/cm), at reasonable voltages (20V), the SiO_2 layer must be limited to a thickness less than 120 Angstroms.

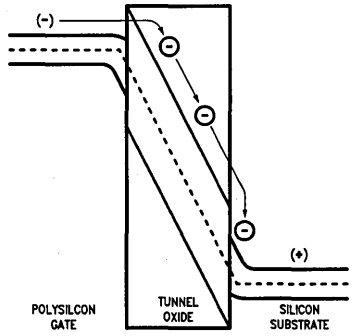

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FIGURE 4. Distortion of Energy Bands in the Presence of a Strong Electric Field

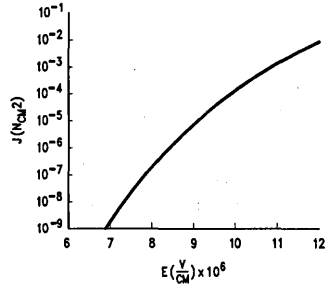

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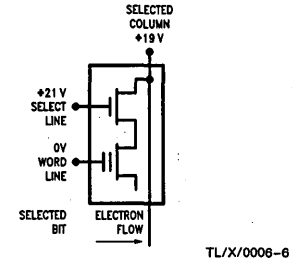
FIGURE 5. Fowler-Nordheim Tunneling I-V Characteristic

Device Operation

To write the cell to logic "0" the control gate is set to ground potential, and a high voltage (19V) is applied to the drain, while the source is left floating. The write operation is shown in *Figure 6*. This causes electrons on the floating gate to tunnel through the SiO_2 into the drain. In this configuration the transistor will allow current to flow. The electric field strength is highest in the region between the floating gate and the drain. Hence tunneling occurs in this thin SiO_2 region. The electric field intensity across the tunneling SiO_2 region is determined by the capacitive coupling ratio of the cell.



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E^2PROM Transistor Write

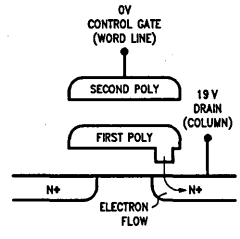

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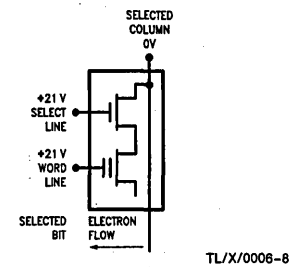
FIGURE 6. Write Operation

During the erase operation the drain is set to ground potential while the control gate is pulled up to 21V, as shown in *Figure 7*. This charging of the control gate causes the floating gate to become capacitively coupled with a positive bias and electrons then tunnel from the drain into the floating gate. The transfer of electrons shifts the cell threshold positive forcing the transistor to pinch-off current flow, which is then interpreted as a logic "1" state at its output.



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E^2PROM Transistor

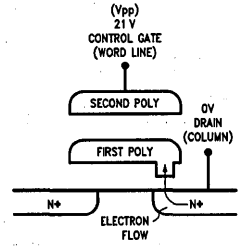

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FIGURE 7. Erase Operation

E²PROM Transistor

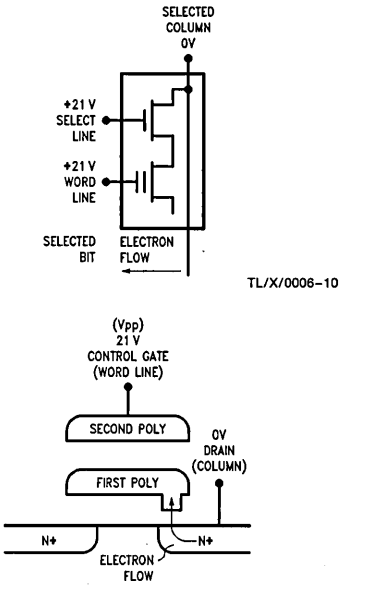

FIGURE 8. Read Operation

The read operation is illustrated in *Figure 8*. To read the bit, 3.5V is applied to the gate of the transistor (word line). The charge stored on the floating gate influences the transistor characteristics. When the floating gate has a net negative charge, the transistor will not conduct current, and while positively charged it will pass current. Distinguishing between current flow and non-current flow allows logical states to be represented by the transistor. *Figure 9* illustrates the situation. When written to, the threshold voltage of the transistor (V_{th}) is equal to $-2V$ and the transistor is turned on. This is subsequently read as a logical 0 on the memory pins. While the bit is erased the threshold voltage will be 6V, the transistor remains off, and the logic is interpreted at the output as a logical 1. This difference between high and low voltage states is known as the cell margin, logic margin, or device window.

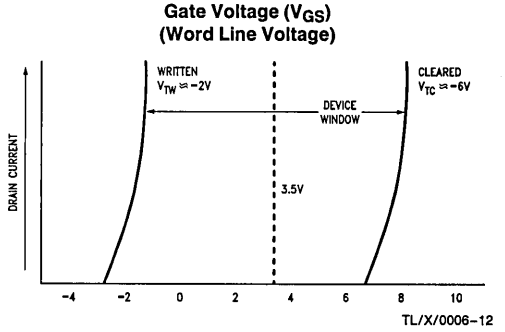

FIGURE 9. I-V Characteristics of Floating Gate EEPROM

INTRINSIC FAILURE MECHANISMS

EEPROMs and light emitting diodes differ from many other semiconductor devices in that they wear out with use. However, with a basic understanding of the intrinsic wear out and failure mechanisms associated with EEPROMs, the designer can construct systems which successfully account for these limitations. The three primary failure mechanisms which affect all EEPROMs are charge trapping and tunnel oxide breakdown which are endurance related, and charge leakage which is data retention related.

Endurance

An EEPROM's endurance—that is, the number of write and erase operations through which each bit can be cycled reliably—is based largely on the degradation of cell margin. The amount of charge that can be stored and removed from an EEPROM cell decreases as the cumulative number of programming cycles rises.

Charge trapping is an intrinsic failure mechanism associated with EEPROMs which tends to narrow the difference between negatively and positively charged threshold voltages (device window) as a function of erase/write cycles. Eventually, after several million cycles, the window is collapsed completely. *Figure 10* illustrates the situation. This charge trapping is cumulative, and increases proportionally with the magnitude and duration of the programming current.

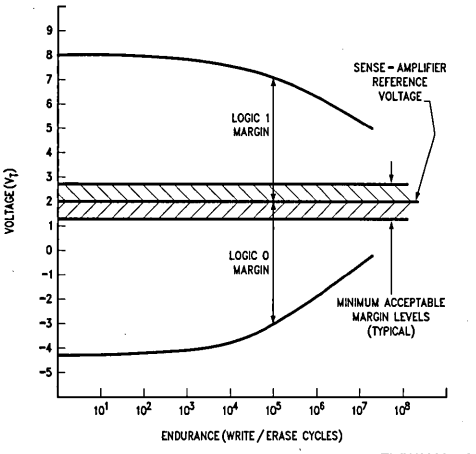

FIGURE 10. Logic Margin vs Endurance for Floating Gate EEPROM

Tunnel oxide breakdown is the primary intrinsic failure mechanism limiting the endurance of EEPROMs. Tiny defects in the tunneling oxide, caused by imperfections in the manufacturing process, can distort the electric field and cause large localized gradients. Excessive amounts of current flow through the regions where the electric field is tightly concentrated leading to high localized mechanical stresses. As write cycles continue, the probability that some imperfection in the oxide will break down increases. Given enough time, the cell will fail to operate correctly because the silicon dioxide which insulates the floating memory cell from the underlying voltage drain will become shorted. The rate of failures due to tunnel oxide breakdown can be reduced by minimizing particulate contaminants, decreasing the cross sectional area as much as is photo-lithographically possible, and controlling the ramp rate of the programming voltage so as to decrease the peak electric field which is created across the tunneling oxide.

Data Retention

Data retention in an EEPROM specification refers to the device's ability to retain a charge on its floating gate with or without an applied bias to the control gate, over extended periods of time. A floating gate on an EEPROM cell requires between one to five million electrons as stored charge. In order to store this amount of charge a current of approximately 10^{-10}A is required for a period of 10 ms. To insure that a wide enough logic margin exists on the cell, the designed floating gate leakage is limited to 10% of the initial charge (1.0^{-10}A) over a period of 10 years. This means that for continuous reading or storage operations over this period, the leakage must be kept below 10^{-21}A per cycle. *Figure 11* shows a typical plot of logic margin vs. time for EEPROMs.

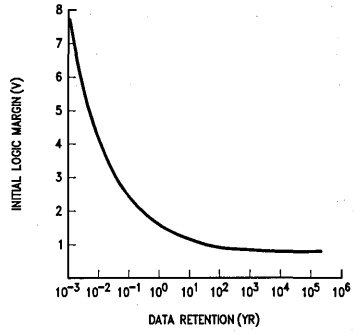

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FIGURE 11. Logic Margin vs Data Retention of MOS Floating Gate EEPROM

Fowler-Nordheim tunneling, the process responsible for charging the floating cell, is also the means by which charge is leaked from the storage cell. This failure mechanism falls into a very broad class of failures which are proportional to $\exp(-E_a/kT)$ where E_a is the activation energy of the process, k is Boltzmann's constant, and T is the absolute temperature. This is very useful because if the activation energy is known for a given process, then tests can be conducted at elevated temperatures, reducing testing time, and the data can be extrapolated to lower operating temperatures using the relationship above.

Combined Effects

The total failure rate of an EEPROM is the sum of the combined rates from all the failure mechanisms involved. *Figure 12* shows the observed failure rate vs. erase/write cycling for EEPROMs. The distribution is a bathtub-shaped curve. The infant mortality region is characterized by an initially high, but rapidly decreasing failure rate. This period is dominated by failures which arise from manufacturing defects. Burn in reliability measures taken during National Semiconductor's manufacturing process are designed to eliminate these devices before they can be shipped to customers. The middle region is dominated by random failures and the rate is approximately level until the wearout region is reached. The wearout region is characterized by an increasing failure rate as the device reaches the end of its useful life.

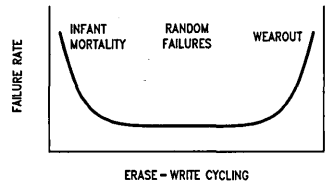

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FIGURE 12. Typical Failure Curve for MOS Floating Gate EEPROM

Comparison to Other Technologies

CMOS static RAM devices with battery backup are often used for non-volatile memory storage. While the CMOS device does not exhibit the wearout mechanisms associated with EEPROM technology, the batteries associated with them do. Nickel Cadmium batteries have a wearout mechanism. Typically, they are good for only a couple of years before they must be replaced. Lithium batteries wear out with use and they display another liability in the fact that when shorted they can become very hot. Cost is another consideration when comparing battery backed up memory vs. EEPROM technology for small sized memory applications. Batteries and their associated mounting hardware can be quite expensive.

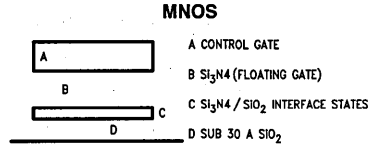

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FIGURE 13. Cross Section of Nitride EEPROM

Some semiconductor manufacturers use nitrides in the production of their EEPROMs, resulting in two similar classes of memories known as SNOS and MNOS devices. A cross section of one of these nitride EEPROMs is illustrated in *Figure 13*. Its operation is similar to an MOS EEPROM. The nitride layer is analogous to the floating gate on the MOS devices. One of the problems encountered with the nitride technology is its temperature dependence on the current/voltage curve. This effect is shown in *Figure 14*. As the temperature increases the curve shifts up and to the left. The higher temperature causes a large increase in current for the same read voltage. This leads to poor data retention because Fowler-Nordheim tunneling is enhanced at these higher current levels and thus large amounts of charge can leak with each read cycle. Transistor voltages on nitride structures are also adversely affected by even small voltage stresses. The final problem associated with this technology is that the oxide-nitride interface is degraded by silicon-gate processing.

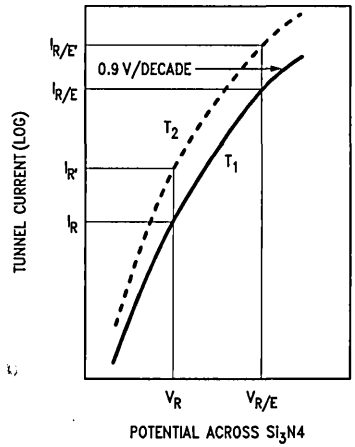

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FIGURE 14. Current Increase from Increased Temperature Leading to Loss of Data Retention for Nitride EEPROM

On the other hand, MOS EEPROMs which use a polysilicon floating gate structure, tend to have better endurance characteristics and superior data retention under voltage and/or temperature stress. Polysilicon floating gate devices also have a longer history in processing, which accounts for their reproducibility and slow wear out as compared to nitride systems.

RELIABILITY ASPECTS OF EEPROMs IN MANUFACTURING

All of the inherent failure mechanisms associated with EEPROM technology can be reduced by applying quality control techniques during the manufacturing process. Quality control measures the component's conformance to specification. Careful monitoring of both the process and the individual devices assures the customer of the highest possible reliability.

Quality Control

The introduction of any new part into the National Semiconductor product line requires first that the product must pass strict design and manufacturing requirements. A table of the reliability qualification procedure which National Semiconductor follows for the introduction of a new EEPROM product appears in Table I.

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products

	Test	Sample	Allowed Fail.
J Pkg.	Operating Life 125°C 1000 Hrs.	3 x 105	2/Lot 5% LTPD (0.78 AQL)
	Dynamic B-I at 5.5. All inputs exercised. (Read, Disable, Read, Disable . . .)		

TABLE I. Reliability Qualification Procedure for All National Semiconductor EEPROM Products (Continued)

	Test	Sample	Allowed Fail.
N Pkg.	1) Operating Life 125°C 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	2) 85/85 1008 Hrs.	3 x 105	2/Lot 5% LTPD (1. 3 AQL)
	3) Autoclave 168 Hrs. (No Bias)	3 x 105	2/Lot 5% LTPD (1.3 AQL)
	4) Bias Pressure Cooker 96 Hrs. (Static B-I)	3 x 105	2/Lot 5% LTPD (1.3 AQL)

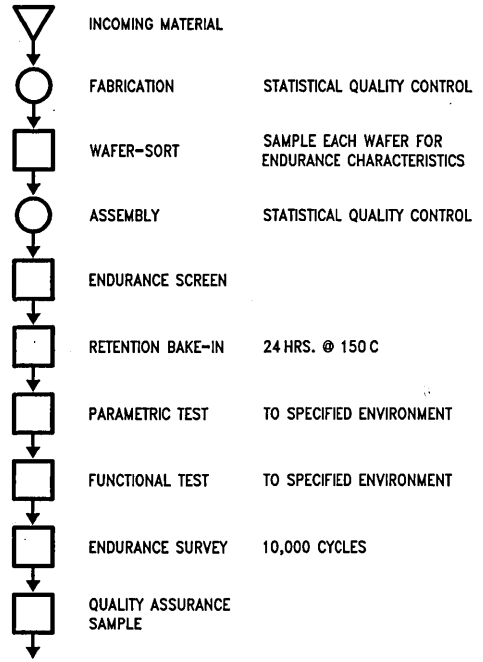

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FIGURE 15. Quality Control Steps for National Semiconductor EEPROMs

For EEPROMs which are in the manufacturing phase, statistical quality control and testing are used to evaluate product compliance to specification. *Figure 15* shows a flow chart of the various quality control steps which National Semiconductor puts their EEPROM chips through.

Burn In

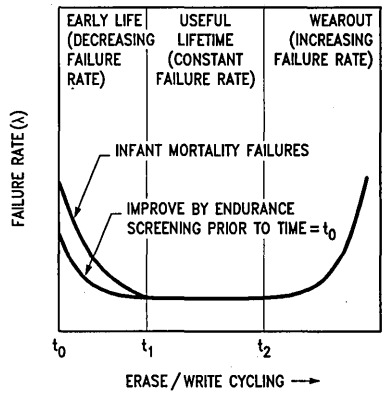
In addition to strict qualifying requirements of products prior to manufacture and tight quality control procedures, National Semiconductor also implements burn-in tests, which weed out the weaker chips, and ensure an even higher level of reliability for the surviving EEPROMs. *Figure 16* is an illustration of typical improvements in product reliability resulting from burning in chips, and removing the ones which would normally fail in the infant mortality region.

RELIABILITY ASPECTS OF EEPROMs IN APPLICATIONS

Reliability Testing and Results

Endurance failure in EEPROM testing is often defined in very different ways. One of the more lenient methods of describing failures on an EEPROM is to simply say that every non-operative cell in a memory device constitutes one failure. National Semiconductor, however, chooses to use a fundamentally more rigorous definition, in which a failure is indicated the first time any single memory bit on the entire chip fails. Depending on memory size and specific devices, one can typically expect a failure rate over 10,000 erase/write cycles of about 3% or less. Of this small percentage of chips which fail after ten-thousand cycles, seldom will any have more than a single-bit error.

It is important to note that the two modes of EEPROM failure, endurance and data retention, are fundamentally orthogonal in applications. That is, a cell that is to be written 10,000 times does not require data retention of 10 years between writes, unless of course you require that the product operate for 100,000 years. Further, even adjacent cells in an EEPROM memory device operate independently from each other, so that any given memory location that is updated only upon rare occasions can be expected to retain its information for long periods, even though adjacent cells are being worn out through extended cycling.



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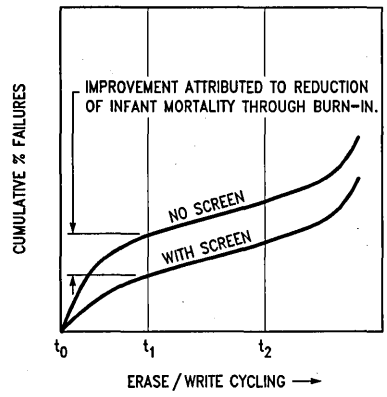

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FIGURE 16. Improvements Attributed to National Semiconductor's Endurance Screen

Section 3

Bipolar PROMs

Section 3 Contents

Section 3 Contents (Continued)

REGISTERED PROMS

Introduction

GENERAL

This generic Schottky PROM family by National Semiconductor makes available to the industry one of the widest selections in sizes and organizations. Four-bit wide PROMs are provided with 256 to 4096 works in pin compatible 16 and 18 pin dual-in-line packages. The 8-bit wide devices range from 32 to 4096 words in a variety of packages. Being 'generic,' all PROMs share a common programming algorithm.

TITANIUM-TUNGSTEN FUSES

National's Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti:W) fuse links designed to program efficiently with only 10.5 Volts applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5 Volts, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti:W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti:W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package), PLCC (V-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

Bipolar PROM Selection Guide

Non-Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) in ns	t_{EA} (Max) in ns	I_{CC} (Max) in mA	Temperature Celsius
256	32 x 8 OC	16	DM54S188	45	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188	35	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288	45	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288	35	20	110	0°C to +70°C
	32 x 8 OC	16	DM54S188A	35	30	110	−55°C to +125°C
	32 x 8 OC	16	DM74S188A	25	20	110	0°C to +70°C
	32 x 8 TS	16	DM54S288A	35	30	110	−55°C to +125°C
	32 x 8 TS	16	DM74S288A	25	20	110	0°C to +70°C
	32 x 8 TS	16	PL77X288B	20	15	140	−55°C to +125°C
	32 x 8 TS	16	PL87X288B	15	12	140	0°C to +70°C
1024	256 x 4 OC	16	DM54S387	60	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387	50	25	130	0°C to +70°C
	256 x 4 TS	16	DM54S287	60	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287	50	25	130	0°C to +70°C
	256 x 4 OC	16	DM54S387A	40	30	130	−55°C to +125°C
	256 x 4 OC	16	DM74S387A	30	20	130	0°C to +70°C
	256 x 4 TS	16	DM54S287A	40	30	130	−55°C to +125°C
	256 x 4 TS	16	DM74S287A	30	20	130	0°C to +70°C
2048	512 x 4 OC	16	DM54S570	65	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570	55	30	130	0°C to +70°C
	512 x 4 TS	16	DM54S571	65	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571	55	30	130	0°C to +70°C
	512 x 4 OC	16	DM54S570A	60	35	130	−55°C to +125°C
	512 x 4 OC	16	DM74S570A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571A	60	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571A	45	25	130	0°C to +70°C
	512 x 4 TS	16	DM54S571B	50	35	130	−55°C to +125°C
	512 x 4 TS	16	DM74S571B	35	25	130	0°C to +70°C
	256 x 8 TS	20	DM54LS471	70	35	100	−55°C to +125°C
	256 x 8 TS	20	DM74LS471	60	30	100	0°C to +70°C
4096	512 x 8 OC	20	DM54S473	75	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473	60	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472	75	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472	60	30	155	0°C to +70°C
	512 x 8 OC	20	DM54S473A	60	35	155	−55°C to +125°C
	512 x 8 OC	20	DM74S473A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472A	60	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472A	45	30	155	0°C to +70°C
	512 x 8 TS	20	DM54S472B	50	35	155	−55°C to +125°C
	512 x 8 TS	20	DM74S472B	35	25	155	0°C to +70°C
	512 x 8 OC	24	DM54S475	75	40	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475	65	35	170	0°C to +70°C
	512 x 8 TS	24	DM54S474	75	40	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474	65	35	170	0°C to +70°C
	512 x 8 OC	24	DM54S475A	60	35	170	−55°C to +125°C
	512 x 8 OC	24	DM74S475A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474A	60	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474A	45	25	170	0°C to +70°C
	512 x 8 TS	24	DM54S474B	50	35	170	−55°C to +125°C
	512 x 8 TS	24	DM74S474B	35	25	170	0°C to +70°C
	1024 x 4 OC	18	DM54S572	75	45	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572	60	35	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573	75	45	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573	60	35	140	0°C to +70°C
	1024 x 4 OC	18	DM54S572A	60	35	140	−55°C to +125°C
	1024 x 4 OC	18	DM74S572A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573A	60	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573A	45	25	140	0°C to +70°C
	1024 x 4 TS	18	DM54S573B	50	35	140	−55°C to +125°C
	1024 x 4 TS	18	DM74S573B	35	25	140	0°C to +70°C

Non-Registered PROMs (Continued)

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{AA} (Max) In ns	t_{EA} (Max) In ns	I_{CC} (Max) In mA	Temperature Celsius
8192	1024 x 8 OC	24	DM77S180	75	35	170	−55°C to +125°C
	1024 x 8 OC	24*	DM77S280	75	35	170	−55°C to +125°C
	1024 x 8 OC	24	DM87S180	55	30	170	0°C to +70°C
	1024 x 8 OC	24*	DM87S280	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181	75	35	170	−55°C to +125°C
	1024 x 8 TS	24*	DM77S281	75	35	170	−55°C to +70°C
	1024 x 8 TS	24	DM87S181	55	30	170	0°C to +70°C
	1024 x 8 TS	24*	DM87S281	55	30	170	0°C to +70°C
	1024 x 8 TS	24	DM77S181A	65	35	170	−55°C to +125°C
	1024 x 8 TS	24	DM87S181A	45	30	170	0°C to +70°C
	2048 x 4 OC	18	DM77S184	70	30	140	−55°C to +125°C
	2048 x 4 OC	18	DM87S184	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185	70	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185	55	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185A	60	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185A	45	25	140	0°C to +70°C
	2048 x 4 TS	18	DM77S185B	50	30	140	−55°C to +125°C
	2048 x 4 TS	18	DM87S185B	35	25	140	0°C to +70°C
16384	2048 x 8 OC	24	DM77S190	80	40	175	−55°C to +125°C
	2048 x 8 OC	24*	DM77S290	80	40	175	−55°C to +125°C
	2048 x 8 OC	24	DM87S190	65	30	175	0°C to +70°C
	2048 x 8 OC	24*	DM87S290	65	30	175	0°C to +70°C
	2048 x 8 TS	24	DM77S191	80	40	175	−55°C to +125°C
	2048 x 8 TS	24*	DM77S291	80	40	175	−55°C to +125°C
	2048 x 8 TS	24	DM87S191	65	30	175	0°C to +70°C
	2048 x 8 TS	24*	DM87S291	65	30	175	0°C to +70°C
	2048 x 8 TS	24	DM77S191A	60	35	175	−55°C to +125°C
	2048 x 8 TS	24	DM87S191A	45	30	175	0°C to +70°C
	2048 x 8 TS	24	DM77S191B	50	30	175	−55°C to +125°C
	2048 x 8 TS	24	DM87S191B	35	25	175	0°C to +70°C
	2048 x 8 TS	24*	DM77S291A	60	35	175	−55°C to +125°C
	2048 x 8 TS	24*	DM87S291A	45	30	175	0°C to +70°C
	2048 x 8 TS	24*	DM77S291B	50	30	175	−55°C to +125°C
	2048 x 8 TS	24*	DM87S291B	35	25	175	0°C to +70°C
	4096 x 4 TS	20	DM77S195A	60	35	170	−55°C to +125°C
	4096 x 4 TS	20	DM87S195A	45	25	170	0°C to +70°C
	4096 x 4 TS	20	DM77S195B	50	30	170	−55°C to +125°C
	4096 x 4 TS	20	DM87S195B	35	25	170	0°C to +70°C
32768	4096 x 8 TS	24	DM77S321	65	35	185	−55°C to +125°C
	4096 x 8 TS	24	DM87S321	55	30	185	0°C to +70°C
	4096 x 8 TS	24*	DM77S421	65	35	185	−55°C to +125°C
	4096 x 8 TS	24*	DM87S421	55	30	185	0°C to +70°C

*—24 Pin Narrow Dual-In-Line Package

Registered PROMs

Size (Bits)	Organization	Pins (DIP)	Part Number	t_{SA} (Min) In ns	t_{PLH} (CLK) t_{PHL} (CLK) (Max) In ns	I_{CC} (Max) In mA	Temperature Celsius
4096	512 x 8 REG	24*	DM77SR474	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR474B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR474	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR474B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM77SR476	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR476B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR25	55	30	185	−55°C to +125°C
	512 x 8 REG	24*	DM77SR25B	40	25	185	−55°C to +125°C
	512 x 8 REG	24*	DM87SR476	55	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR476B	35	20	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR25	50	27	185	0°C to +70°C
	512 x 8 REG	24*	DM87SR25B	35	20	185	0°C to +70°C
8192	1024 x 8 REG	24*	DM77SR181	50	30	175	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR181	40	20	175	0°C to +70°C
	1024 x 8 REG	24*	DM77SR183	45	30	185	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR183	40	25	185	0°C to +70°C
	1024 x 8 REG	24*	DM77SR183B	40	25	185	−55°C to +125°C
	1024 x 8 REG	24*	DM87SR183B	35	20	185	0°C to +70°C
	2048 x 4 REG	24*	DM77SR191**	18	15	195	−55°C to +125°C
	2048 x 4 REG	24*	DM87SR191**	25	10	190	0°C to +70°C
	2048 x 4 REG	24*	DM77SR193**	18	15	190	−55°C to +125°C
	2048 x 4 REG	24*	DM87SR193**	25	10	190	0°C to +70°C

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2 to +5.5V
Output Voltage (Note 2)	−0.5 to +5.5V
Storage Temperature	−65 to +150°C
Lead Temperature (10 seconds)	300°C

*-24 Pin Narrow Dual Inline Package

** To be released June 1987.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

National Semiconductor Corporation

DM54/74S188, DM54/74S288 (32 x 8) 256-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

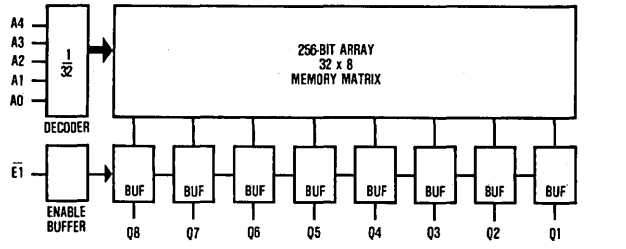
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—22 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J, V
DM74S288		X		X	N, J, V
DM54S188	X		X		J
DM54S288	X			X	J

Block and Connection Diagram



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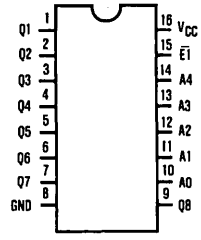

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Top View

Order Number DM54/74S188J, 288J, DM74S188N, 288N, 188V, 288V
See NS Package Number J16A, N16A or V20A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S188/288			DM74S188/288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		70	110		70	110	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM54S188/288			DM74S188/288			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		22	45		22	35	ns
TEA	TEVQV	Enable Access Time		15	30		15	20	ns
TER	TEXQX	Enable Recovery Time		15	35		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	20	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	25	ns

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

DM54/74S188A, DM54/74S288A (32 x 8) 256-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

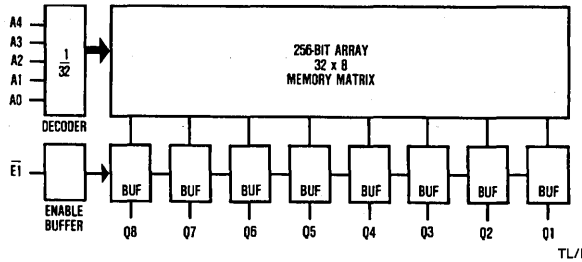
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—17 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188A		X	X		N,J
DM74S288A		X		X	N,J
DM54S188A	X		X		J
DM54S288A	X			X	J

Block and Connection Diagrams



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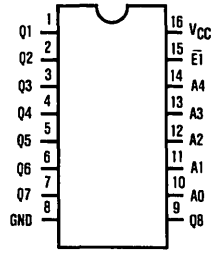
Dual-In-Line Package



TL/L/8360–2

Top View

Order Number DM54S188AJ, DM54S288AJ, DM74S188AJ, N, or DM74S288AJ, N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S188A/288A			DM74S188A/288A			Units
			Min	Typ	Max	Min	Typ	Max	
I_L	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		70	110		70	110	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM54S188A/288A			DM74S188A/288A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		17	35		17	25	ns
TEA	Enable Access Time	TEVQV		15	30		15	20	ns
TER	Enable Recovery Time	TEXQX		15	30		15	20	ns
TZX	Output Enable Time	TEVQX		15	30		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	30		15	20	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

PL77X288B/PL87X288B (32 x 8) 256-Bit TTL Logic PROMs

General Description

These Schottky programmable logic devices are organized in the popular 32 words by 8-bit configuration. An enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the OFF or high impedance state. The memories are available in the TRI-STATE® version only.

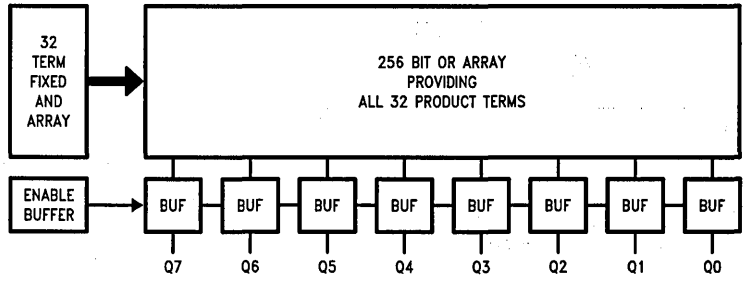
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—10 ns typ
  - Enable access—8 ns typ
  - Enable recovery—8 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- > 2000V input protection for electrostatic discharge

	Military	Commercial	Open-Collector	TRI-STATE	Package
PL87X288		X		X	N, J, V
PL77X288	X			X	J

Block and Connection Diagrams



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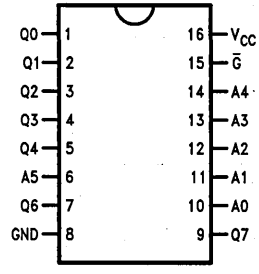
Dual-In-Line Package



TL/L/6747–2

Top View

Order Number PL77X288/PL87X288J, PL87X288N or PL87X288V
See NS Package Number J16A, N16A or V20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to 5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Static Discharge Voltage (per Mil-Std-883 Method 3015.2)	>2001V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
PL77X288	4.50	5.50	V
PL87X288	4.75	5.25	V
Ambient Temperature (T_A)			
PL77X288	−55	+125	°C
PL87X288	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	PL77X288			PL87X288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.4V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 24 mA (Com) I_{OL} = 12 mA (Mil)		0.35	0.50		0.35	0.50	V
V_{IL}	Low Level Input Voltage	(Note 7)			0.80			0.80	V
V_{IH}	High Level Input Voltage	(Note 7)	2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.5		−0.8	−1.5	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	140		110	140	mA
TRI-STATE									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−30		−130	−30		−130	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.4V to 2.4V Chip Disabled			100 −100			100 −100	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 3.2 mA				2.4	3.2		V

AC Electrical Characteristics with standard load and operating conditions

Symbol	Parameter	JEDEC Symbol	PL77X288			PL87X288			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	Address Access Time (Note 5)	TAVQV		10	20		10	15	ns
t_{EA}	Enable Access Time (Note 5)	TEVQV		8	15		8	12	ns
t_{ER}	Enable Recovery Time (Note 6)	TEXQX		8	15		8	12	ns
t_{ZX}	Output Enable Time (Note 5)	TEVQX		8	15		8	12	ns
t_{XZ}	Output Disable Time (Note 6)	TEXQZ		8	15		8	12	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming parameters.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: C_L = 50 pF.

Note 6: C_L = 5 pF.

Note 7: These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Approved Programmers

Manufacturer	System #
DATA I/O	5/17/19/29A
PRO-LOG	M910, M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803

National Semiconductor Corporation

DM54/74S387A, DM54/74S287A (256 x 4) 1024-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

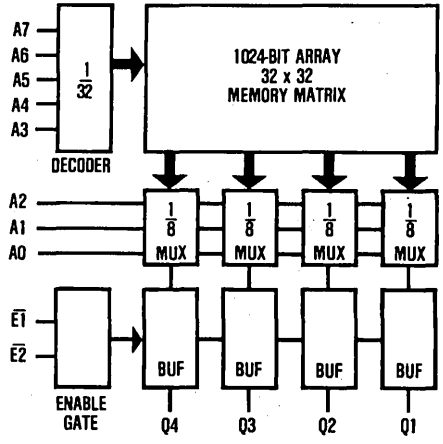
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—20 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- >2000V input protection for electrostatic discharge

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387A		X	X		N,J,V
DM74S287A		X		X	N,J,V
DM54S387A	X		X		J
DM54S287A	X			X	J

Block and Connection Diagrams



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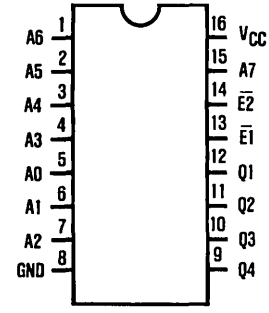
Dual-In-Line-Package



TL/L/8359-2

Top View

Order Number DM54S287AJ, DM54S387AJ, DM74S287AJ, 287AN, 287AV, DM74S387AJ, 387AN, 387AV
See NS Packages J16A, N16A or V20A

3

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2001V

ESD rating to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	70	°C
Logical "0" Input Voltage	0	0.8	V
Logic "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM54S387A/287A			DM74S387A/287A			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL} (Note 4)	Low Level Input Voltage				0.80			0.80	V
V_{IH} (Note 4)	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Ouput Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 5)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM54S387A/287A			DM74S387A/287A			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	Address Access Time	TAVQV		20	40		20	30	ns
T_{EA}	Enable Access Time	TEVQV		15	30		15	20	ns
T_{ER}	Enable Recovery Time	TEXQX		15	30		15	20	ns
T_{ZX}	Output Enable Time	TEVQX		15	30		15	20	ns
T_{XZ}	Output Disable Time	TEXQZ		15	30		15	20	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = +25°C.

Note 4: These are absolute voltages with respect to pin 8 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 5: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

DM54/74S387, DM54/74S287 (256 x 4) 1024-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

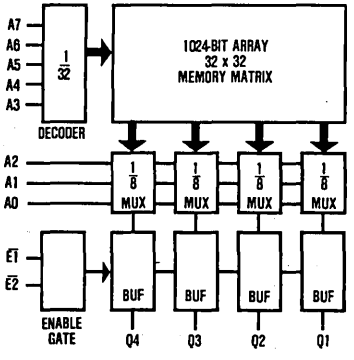
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J, V
DM74S287		X		X	N, J, V
DM54S387	X		X		J
DM54S287	X			X	J

Block and Connection Diagram



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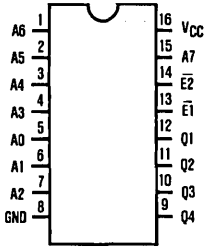

TL/L/9188-2

Top View

Order Number DM54/74S387J, DM54/74S287J, DM74S387N, DM74S387V, DM74S287N or DM74S287V
See NS Package Number J16A, N16A or V20A

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DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S387/287			DM74S387/287			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM54S387/287			DM74S387/287			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	60		35	50	ns
TEA	TEVQV	Enable Access Time		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	25	ns

National Semiconductor Corporation

DM54/74S570, DM54/74S571, DM54/74S570A, DM54/74S571A, DM54/74S571B (512 x 4) 2048-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

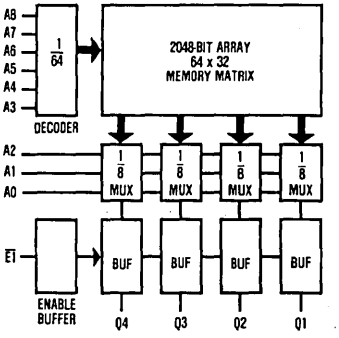
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—30 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J, V
DM74S571		X		X	N, J, V
DM54S570	X		X		J
DM54S571	X			X	J

Block and Connection Diagrams



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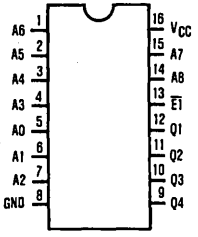


TL/L/9189-2

Top View

Order Number DM54/74S570J, DM54/74S571J, DM74S570N, DM74S571N, DM74S570V or DM74S571V
See NS Package Number J16A, N16A or V20A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S570/571			DM74S570/571			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		90	130		90	130	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter	DM54S570/571			DM74S570/571			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	65		40	55	ns
TEA	TEVQV	Enable Access Time		20	35		20	30	ns
TER	TEXQX	Enable Recovery Time		20	35		20	30	ns
TZX	TEVQX	Output Enable Time		20	35		20	30	ns
TXZ	TEXQZ	Output Disable Time		20	35		20	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol		Parameter	DM54S571A, B/570A			DM74S571A, B/570A			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	571A/570A	Address Access Time		30	60		30	45	ns
		571B			30	50		30	35	ns
TEA	TEVQV		Enable Access Time		15	35		15	25	ns
TER	TEXQX		Enable Recovery Time		15	35		15	25	ns
TZX	TEVQX		Output Enable Time		15	35		15	25	ns
TXZ	TEXQZ		Output Disable Time		15	35		15	25	ns

National Semiconductor Corporation

DM54/74LS471
(256 x 8) 2048-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

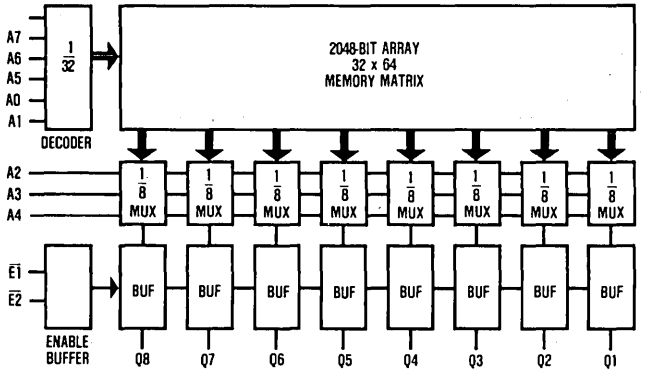
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE®	Package
DM74LS471		X		X	N, J, V
DM54LS471	X			X	J

Block and Connection Diagrams



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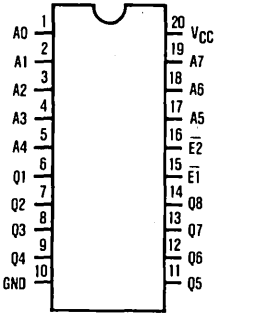


TL/L/9190–2

Order Number DM54LS471J, DM74LS471J, DM74LS471N or DM74LS471V
See NS Package Number J20A, N20A or V20A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		75	100		75	100	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		45	70		40	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

DM54/74S473, DM54/74S472, DM54/74S473A, DM54/74S472A, DM54/74S472B (512 x 8) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

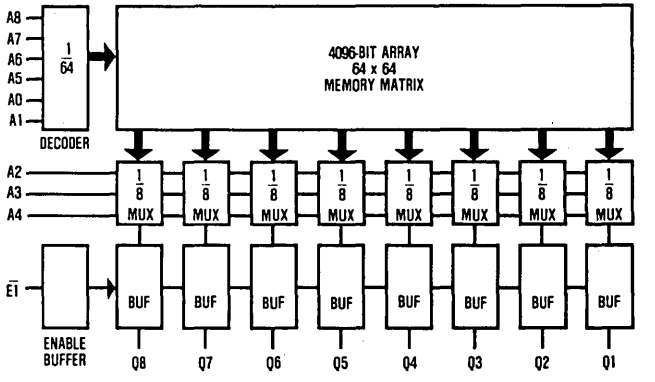
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N, J, V
DM74S472		X		X	N, J, V
DM54S473	X		X		J
DM54S472	X			X	J

Block and Connection Diagrams



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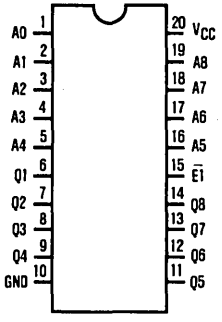

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Top View

Order Number DM54/74S472AJ, 472BJ, DM74S472AN, DM74S472AV, DM74S472BN, DM74S472BV, DM74S472N, DM74S472V, DM74S473AN, DM74S473AV, DM74S473N or DM74S473V
See NS Package Number J20A, N20A or V20A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S473/472			DM74S473/472			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		110	155		110	155	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM54S472/473			DM74S472/473			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		40	60	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol		Parameter	DM54S473A/472A, B			DM74S473A/472A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	473A/472A	Address Access Time		25	60		25	45	ns
		472B			25	50		25	35	ns
TEA	TEVQV	473A/472A	Enable Access Time		15	35		15	30	ns
		472B			15	35		15	25	ns
TER	TEXQX	473A/472A	Enable Recovery Time		15	35		15	30	ns
		472B			15	35		15	25	ns
TZX	TEVQX	473A/472A	Output Enable Time		15	35		15	30	ns
		472B			15	35		15	25	ns
TXZ	TEXQZ	473A/472A	Output Disable Time		15	35		15	30	ns
		472B			15	35		15	25	ns

National Semiconductor Corporation

DM54/74S475, DM54/74S474; DM54/74S475A, DM54/74S474A; DM54/74S474B (512 x 8) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

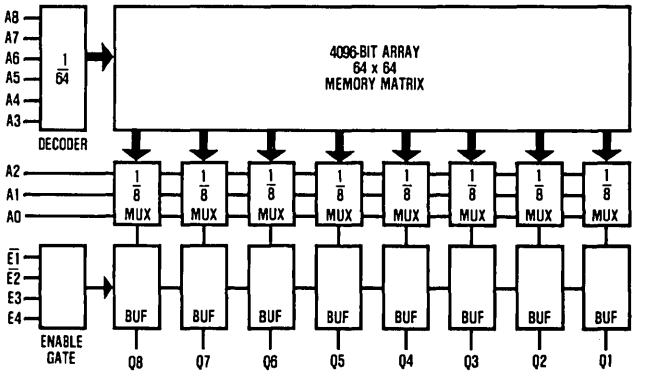
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N, J, V
DM74S474		X		X	N, J, V
DM54S475	X		X		J
DM54S474	X			X	J

Block and Connection Diagrams



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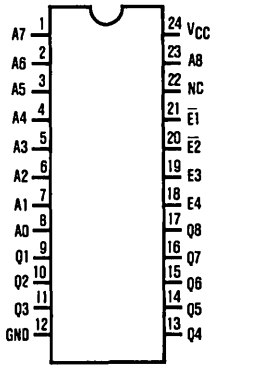


TL/L/9192–2

Top View

Order Number DM54/74S474J, DM54/74S474AJ, DM54/74S474BJ, DM54/74S475J, DM54/74S475AJ or DM74S474N, DM74S474AN, DM74S474BN, DM74S475N, DM74S475AN or DM74S474V or DM74S474AV, DM74S474BV, DM74S475V, DM74S475AV
See NS Package Number J24A, N24A or V28A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S475/474			DM74S475/474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter	DM54S475/474			DM74S475/474			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		40	65	ns
TEA	TEVQV	Enable Access Time		20	40		20	35	ns
TER	TEXQX	Enable Recovery Time		20	40		20	35	ns
TZX	TEVQX	Output Enable Time		20	40		20	35	ns
TXZ	TEXQZ	Output Disable Time		20	40		20	35	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol		Parameter	DM54S475A/474A, B			DM74S475A/474A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	475A/474A	Address Access Time		25	60		25	45	ns
		474B			25	50		25	35	ns
TEA	TEVQV		Enable Access Time		15	35		15	25	ns
TER	TEXQX		Enable Recovery Time		15	35		15	25	ns
TZX	TEVQX		Output Enable Time		15	35		15	25	ns
TXZ	TEXQZ		Output Disable Time		15	35		15	25	ns

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

DM54/74S572, DM54/74S573, DM54/74S572A, DM54/74S573A, DM54/74S573B (1024 x 4) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

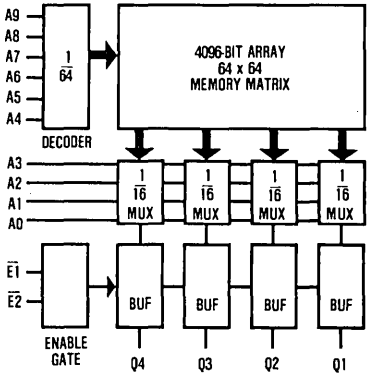
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N, J
DM74S573		X		X	N, J
DM54S572	X		X		J
DM54S573	X			X	J

Block and Connection Diagrams



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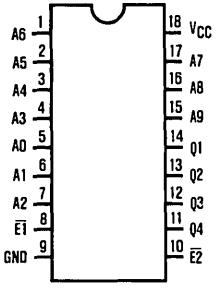


TL/L/9193-2

Top View

Order Number DM54/74S572AJ, DM54/74S572BJ, DM54/74S572J, DM54/74S573J, DM54/74S573AJ, DM54/74S573BJ, DM74S572N, DM74S573N, DM74S573AN, DM74S573BN, DM74S572V, DM74S573V, DM74S573AV or DM74S573BV
See NS Package Number J18A, N18A or V20A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM54S572/573			DM74S572/573			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
TRI-STATE PARAMETERS									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter	DM54S572/573			DM74S572/573			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		40	60	ns
TEA	TEVQV	Enable Access Time		20	45		20	35	ns
TER	TEXQX	Enable Recovery Time		20	45		20	35	ns
TZX	TEVQX	Output Enable Time		20	45		20	35	ns
TXZ	TEXQZ	Output Disable Time		20	45		20	35	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol		Parameter	DM54S572A/573A, B			DM74S572A/573A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	572A/573A	Address Access Time		25	60		25	45	ns
		573B			25	50		25	35	ns
TEA	TEVQV		Enable Access Time		15	35		15	25	ns
TER	TEXQX		Enable Recovery Time		15	35		15	25	ns
TZX	TEVQX		Output Enable Time		15	35		15	25	ns
TXZ	TEXQZ		Output Disable Time		15	35		15	25	ns

National Semiconductor Corporation

DM77/87S180, DM77/87S181, DM77/87S181A, DM77/87S280, DM77/87S281, DM77/87S281A (1024 x 8) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

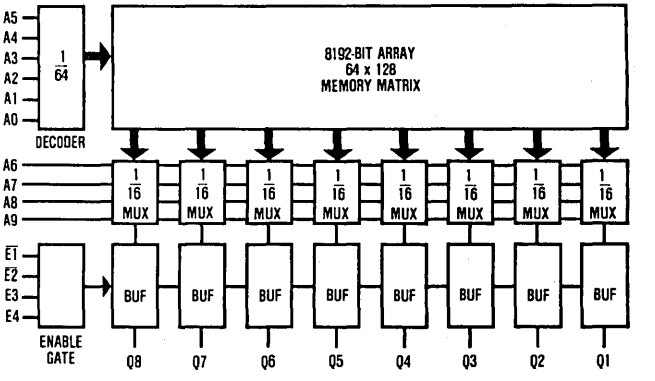
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package	24-Pin Standard	24-Pin Narrow-Dip
DM87S180		X	X		N, J, V	X	
DM87S181		X		X	N, J, V	X	
DM77S180	X		X		J	X	
DM77S181	X			X	J	X	
DM87S280		X	X		N, J, V		X
DM87S281		X		X	N, J, V		X
DM77S280	X		X		J		X
DM77S281	X			X	J		X

Block and Connection Diagrams



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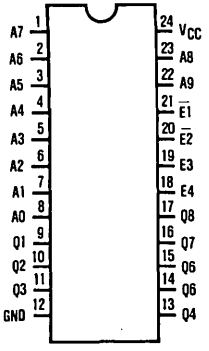


TL/L/9194-2

Top View

Order Number DM77/87S180J, 181J, 280J, 281J, 181AJ, 281AJ, DM87S180N, 181N, 280N, 281N, 181AN, 281AN, DM87S180V, 181V, 280V or 281V

See NS Package Number J24A, N24A, J24F, N24C or V28A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S180/181 DM77S280/281			DM87S180/181 DM87S280/281			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		115	170		115	170	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameters	DM77S180/181 DM77S280/281			DM87S180/181 DM87S280/281			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	75		40	55	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM77S181A			DM87S181A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		35	65		35	45	ns
TEA	TEVQV	Enable Access Time		15	35		15	30	ns
TER	TEXQX	Enable Recovery Time		15	35		15	30	ns
TZX	TEVQX	Output Enable Time		15	35		15	30	ns
TXZ	TEXQZ	Output Disable Time		15	35		15	30	ns

National Semiconductor Corporation

DM77/87SR181
(1024 x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This device is organized as 1024-words by 8-bits and is available in the tri-state output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

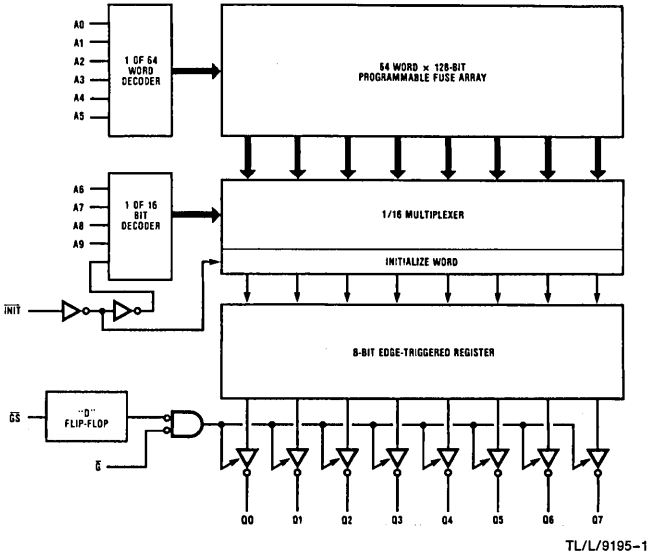
The DM77/87SR181 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register INITIALIZE
- 24-pin, 300 mil package
- 40 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE® outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block and Connection Diagrams



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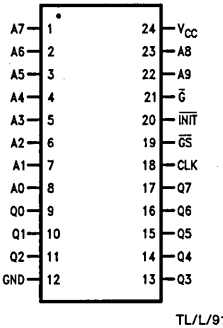


TL/L/9195–2

Top View

Order Number DM77/87SR181J, DM87SR181N or DM87SR181V See NS Package Number J24A, N24C or V28A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	175		115	175	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	C_L = 30 pF	50	20		40	20		ns
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{S(INIT)}$	INIT to CLK (High) Setup Time		35	20		30	20		ns
$t_{H(INIT)}$	INIT to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)			15	30		15	20	ns
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(GS)}$	$\overline{GS}$ to CLK (High) Setup Time		15	0		15	0		ns
$t_{H(GS)}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PZL(CLK)}$	Delay from CLK (High) to Active Output (High or Low)	C_L = 30 pF		20	30		20	25	ns
$t_{PZH(CLK)}$				20	30		20	25	ns
$t_{PZL(G)}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZH(G)}$				15	30		15	25	ns
$t_{PLZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)	C_L = 5 pF (Note 1)		20	30		20	25	ns
$t_{PHZ(CLK)}$				20	30		20	25	ns
$t_{PLZ(G)}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns
$t_{PHZ(G)}$				15	30		15	25	ns

Note: All typical values are for V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM77/87S184, DM77/87S185, DM77/87S185A, DM77/87S185B (2048 x 4) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

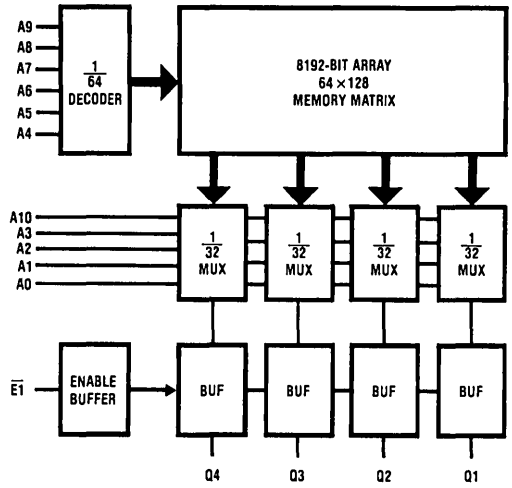
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max (B Version)
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S184		X	X		N, J, V
DM87S185		X		X	N, J, V
DM77S184	X		X		J
DM77S185	X			X	J

Block and Connection Diagram



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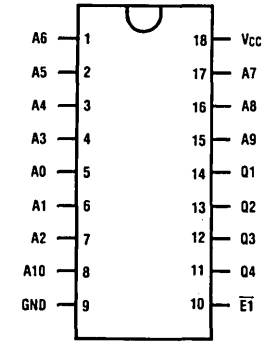


TL/L/9197–2

Top View

Order Number DM77/87S184J, DM77/87S185J, DM77/87S185AJ, DM77/87S185BJ, DM87S184N, DM87S185N, DM87S185AN, DM87S185BN, DM87S184V, DM87S185V, DM87S185AV or DM87S185BV
See NS Package Number J18A, N18A or V20A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S184/185			DM87S184/185			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameters	DM77S184/185			DM87S184/185			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		40	55	ns
TEA	TEVQV	Enable Access Time		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	25	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol		Parameters	DM77S185A/B			DM87S185A/B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	185A	Address Access Time		30	60		30	45	ns
		185B			25	50		25	35	ns
TEA	TEVQV		Enable Access Time		15	30		15	25	ns
TER	TEXQX		Enable Recovery Time		15	30		15	25	ns
TZX	TEVQX		Output Enable Time		15	30		15	25	ns
TXZ	TEXQZ		Output Disable Time		15	30		15	25	ns

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

DM77/87S190, DM77/87S191, DM77/87S290, DM77/87S291, DM77/87S191A, DM77/87S291A, DM77/87S191B, DM77/87S291B (2048 x 8) 16,384-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 2048 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

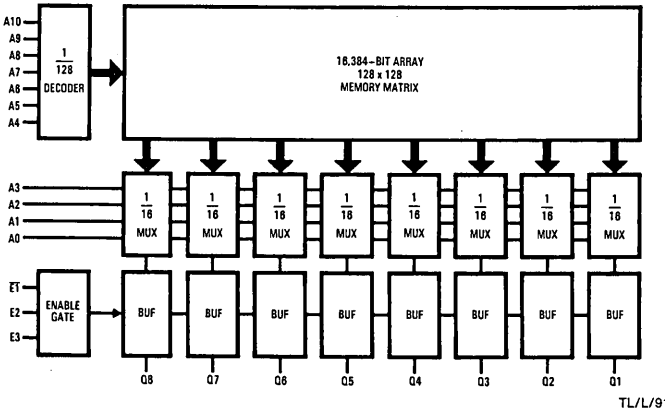
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced tungsten (W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max (B Version)
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package	24-Pin Standard	24-Pin Thin-Dip
DM87S190		X	X		N, J, V	X	
DM87S191		X		X	N, J, V	X	
DM77S190	X		X		J	X	
DM77S191	X			X	J	X	
DM87S290		X	X		N, J, V		X
DM87S291		X		X	N, J, V		X
DM77S290	X		X		J		X
DM77S291	X			X	J		X

Block and Connection Diagrams



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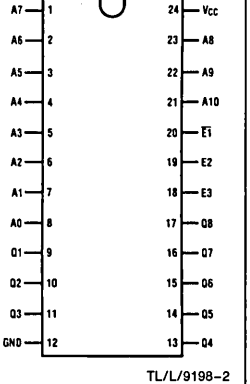


TL/L/9198-2

Top View

Order Number DM77/87S190J, 191J, 290J, 291J, 191A/BJ, 291A/BJ, DM87S190N, 191N, 290N, 291N, 191A/BN, 291A/BN, DM87S190V, 191V, 290V, 291V, 191A/BV or 291A/BV
See NS Package Number J24A, J24F, N24A, N24C or V28A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S190/191 DM77S290/291			DM87S190/191 DM87S290/291			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V, T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded, All Outputs Open		120	175		120	175	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V, Chip Disabled	−50		50	−50		50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol	Parameter	DM77S190/191 DM77S290/291			DM87S190/191 DM87S290/291			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	TAVQV	Address Access Time		35	80		35	65	ns
t_{EA}	TEVQV	Enable Access Time		15	40		15	30	ns
t_{ER}	TEXQX	Enable Recovery Time		15	40		15	30	ns
t_{ZX}	TEVQX	Output Enable Time		15	40		15	30	ns
t_{XZ}	TEXQZ	Output Disable Time		15	40		15	30	ns

AC Electrical Characteristics With Standard Load and Operating Conditions

Symbol	JEDEC Symbol		Parameters	DM77S191A/B DM77S291A/B			DM87S191A/B DM87S291A/B			Units
				Min	Typ	Max	Min	Typ	Max	
t_{AA}	TAVQV	191A/291A	Address Access Time		30	60		30	45	ns
		191B/291B			30	50		30	35	ns
t_{EA}	TEVQV		Enable Access Time		15	30		15	25	ns
t_{ER}	TEXQX		Enable Recovery Time		15	30		15	25	ns
t_{ZX}	TEVQX		Output Enable Time		15	30		15	25	ns
t_{XZ}	TEXQZ		Output Disable Time		15	30		15	25	ns

National Semiconductor Corporation

DM77/87S195A, DM77/87S195B (4096 x 4) 16,384-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 4096 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in TRI-STATE® version only.

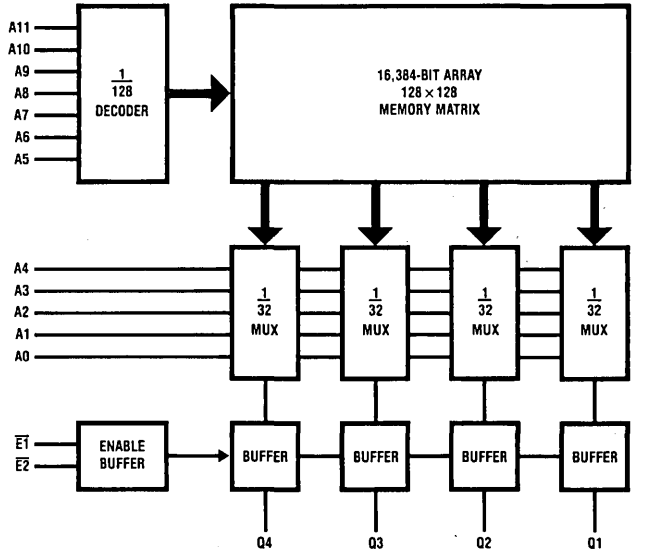
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced tungsten (W) fuse technology
- Schottky-clamped for high speed
  - Address access—30 ns max
  - Enable access— 15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	TRI-STATE	Package
DM87S195A/B		X	X	N, J, V
DM77S195A/B	X		X	J

Block and Connection Diagrams



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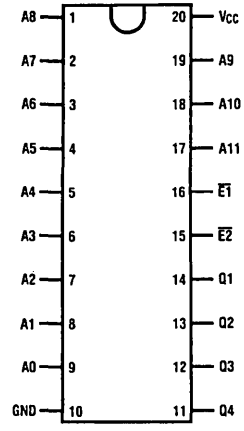
Dual-In-Line Package



TL/L/9199-2

Top View

Order Number DM77/87S195AJ, 195BJ, DM87S195AN, 195BN, DM87S195AV or 195BV
See NS Package Number J20A, N20A or V20A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S195A/B			DM87S195A/B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		120	170		120	170	mA
TRI-STATE PARAMETERS									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V			+50			+50	μA
		Chip Disabled			−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameter		DM77S195A/195B			DM87S195A/195B			Units
				Min	Typ	Max	Min	Typ	Max	
t_{AA}	TAVQV	Address Access Time	195A		30	60		30	45	ns
			195B		30	50		30	35	ns
t_{EA}	TEVQV	Enable Access Time			15	30		15	25	ns
t_{ER}	TEXQX	Enable Recovery Time			15	30		15	25	ns
t_{ZX}	TEVQX	Output Enable Time			15	30		15	25	ns
t_{XZ}	TEXQZ	Output Disable Time			15	30		15	25	ns

National Semiconductor Corporation

DM77/87S321, DM77/87S421 (4096 x 8) 32,768-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 4096 words by 8-bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the eight outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

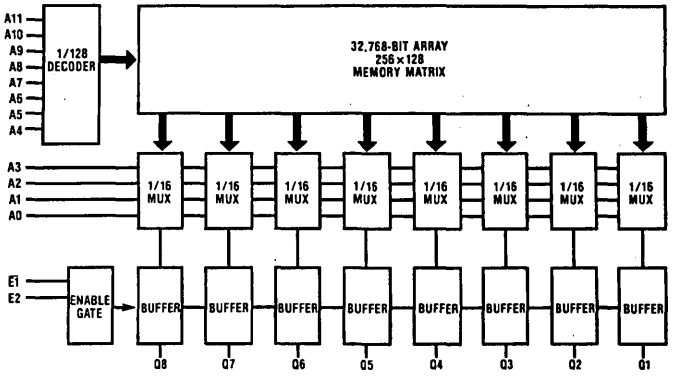
The DM77/87S321 and DM77/87S421 program the same as all other nonregistered PROMs from National.

Features

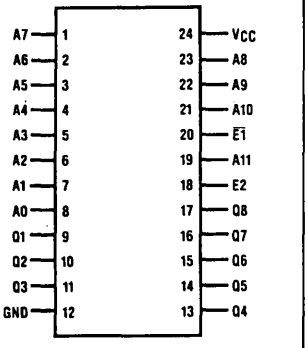
- Advanced fuse technology
- Schottky-clamped for high speed
  - Address access—55 ns max
  - Enable access—20 ns typ
  - Enable recovery—20 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Generic programming

	Military	Commercial	TRI-STATE	Package
DM87S321		X	X	N, J, V
DM77S421	X		X	J
DM87S421		X	X	N, J*, V
DM77S421	X		X	J*

Block and Connection Diagrams



TL/L/9200–1



TL/L/9200–2

Top View

Order Number DM77/87S321J, 421J, DM87S321N, 421N, DM87S321V or DM87S421V
See NS Package Number J24A, N24A or V28A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77S321/421			DM87S321/421			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 12 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Outputs Open		135	185		135	185	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameters	DM77S321/421			DM87S321/421			Units
			Min	Typ	Max	Min	Typ	Max	
T_{AA}	TAVQV	Address Access Time		40	65		40	55	ns
T_{EA}	TEVQV	Enable Access Time		20	35		20	30	ns
T_{ER}	TEXQX	Enable Recovery Time		20	35		20	30	ns
T_{ZX}	TEVQX	Output Enable Time		20	35		20	30	ns
T_{XZ}	TEXQZ	Output Disable Time		20	35		20	30	ns

Note 1: These limits apply over the entire operating range unless otherwise noted. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor Corporation

PRELIMINARY

DM77/87SR474, DM77/87SR474B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR474 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR474 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

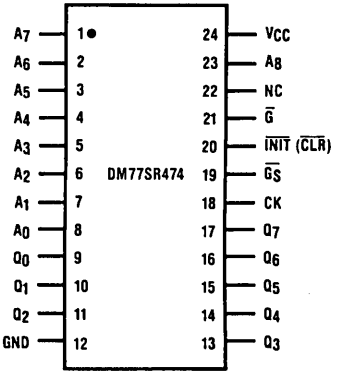
The DM77/87SR474 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows, providing a $\overline{CLEAR}$ function when not programmed.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable synchronous register INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Pinout compatible with DM77SR181 (1k x 8) Registered PROM for future expansion

Connection Diagram



TL/L/9201–2

Top View

Order Number DM77SR474J, DM87SR474J, DM87SR474N, DM77SR474BJ, DM87SR474BJ, DM87SR474BN, DM87SR474V or DM87SR474BV
See NS Package Number J24F, N24C or V28A

3

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

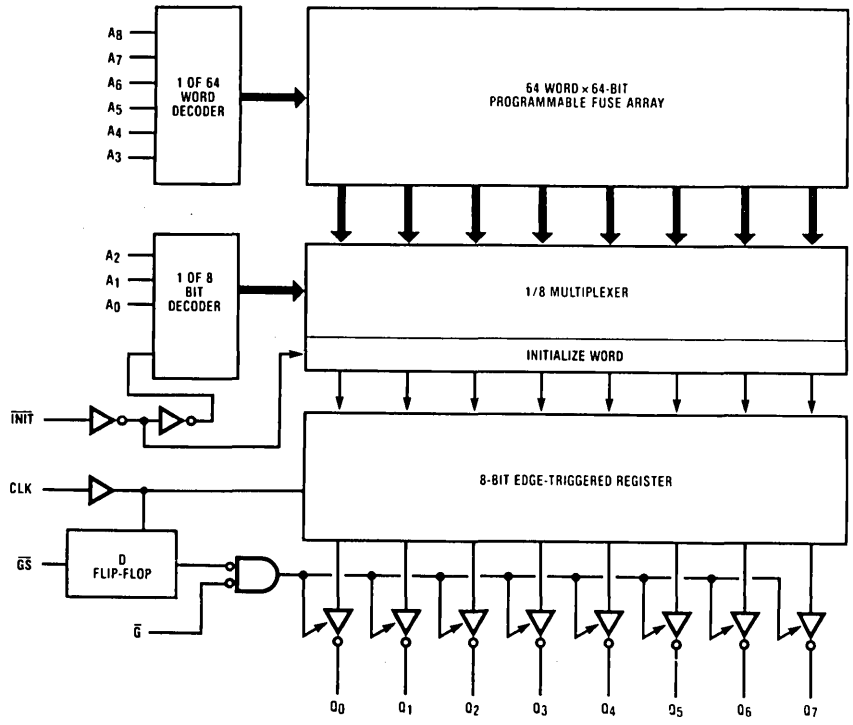
Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR474			DM87SR474			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR474	55	20		50	20		ns
		SR474B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ to CLK (High) Setup Time		30	20		25	20		ns
$t_{H(\overline{INIT})}$	$\overline{INIT}$ to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR474		15	30		15	27	ns
		SR474B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Output Active (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Active (High or Low)			15	30		15	25	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Output Inactive (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Inactive (TRI-STATE)			15	30		15	25	ns

Block Diagram



TL/L/9201–1

National Semiconductor Corporation

DM77/87SR476, DM77/87SR25, DM77/87SR476B, DM77/87SR25B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined micro-programmed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

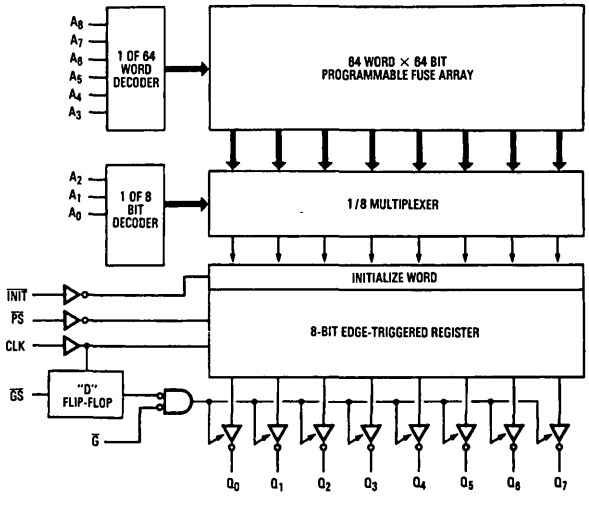
The DM77SR476 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows, which makes it compatible with the CLEAR function on the AM27S25. $\overline{PS}$ loads ones into the output registers when brought low.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

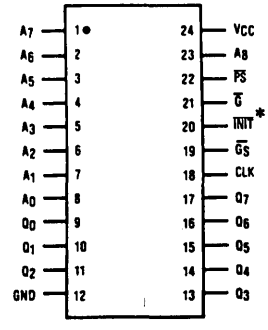
Features

- Functionally compatible with AM27S25
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE (SR476 only)
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameter's guaranteed over temperature
- Preset input

Block and Connection Diagrams



TL/L/9202-1



TL/L/9202-2

Top View

*$\overline{CLR}$ only on DM77/87SR25

Order Number DM77/87SR476J, SR25J, SR476BJ, SR25B, DM87SR476N, SR25N, SR476BN, SR25BN, DM87SR476V, SR25V, SR476BV or SR25BV

See NS Package Number J24F, N24C or V28A

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		135	185		135	185	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 2: During I_{OS} measurements, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR476, SR25	55	20		50	20		ns
		SR476B, SR25B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR476, SR25		15	30		15	27	ns
		SR476B, SR25B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{PS})}$	Delay from $\overline{PS}$ (Low) to Output (High)			20	40		20	30	ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	40		20	30	ns
$t_{WL(\overline{PS})}$	$\overline{PS}$ Pulse Width (Low)		15	10		15	10		ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		15	10		15	10		
$t_{S(\overline{PS})}$	$\overline{PS}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZL(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

National Semiconductor Corporation

DM77/87SR27, DM77/87SR27B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR27 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8 bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

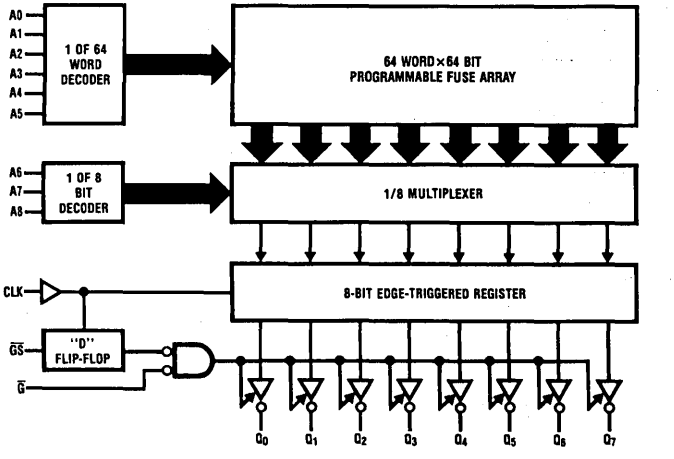
Data is read from the PROM by first applying an address to inputs A0–A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

PROMS are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

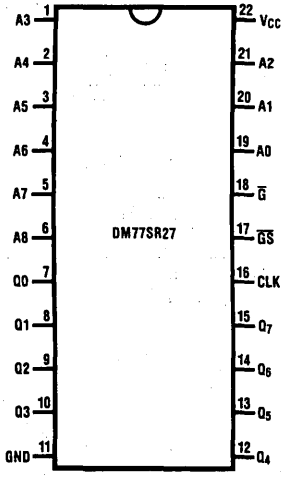
- Functionally compatible with Am27S27
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 22-pin 400-mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block and Connection Diagrams



TL/L/6686–1

Dual-In-Line Package



Top View

TL/L/6686–2

Order Number DM77/87SR27J, DM77/87SR27BJ, DM87SR27N, DM87SR27BN, DM87SR27V or DM87SR27BV
See NS Package Number J22A, N22A or V28A

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 1)	−0.5V to +7.0V
Input Voltage (Note 1)	−1.2V to +5.5V
Output Voltage (Note 1)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (10 sec)	300°C

ESD rating to be determined.

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operations should be limited to those conditions specified under DC Electrical Characteristics.

Operating Conditions

Supply Voltage (V_{CC})	
DM77SR27	4.5V to 5.5V
DM87SR27	4.75V to 5.25V
Ambient Temperature (T_A)	
DM77SR27	−55°C to +125°C
DM87SR27	0°C to +70°C
Logical '0' Input Voltage	0V to 0.8V
Logical '1' Input Voltage	2.0V to 5.5V

DC Electrical Characteristics T_A = 25°C, V_{CC} = 5.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		135	185		135	185	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 2)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled			+50			+50	μA
					−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = − 6.5 mA				2.4	3.2		V

Note 1: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 2: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

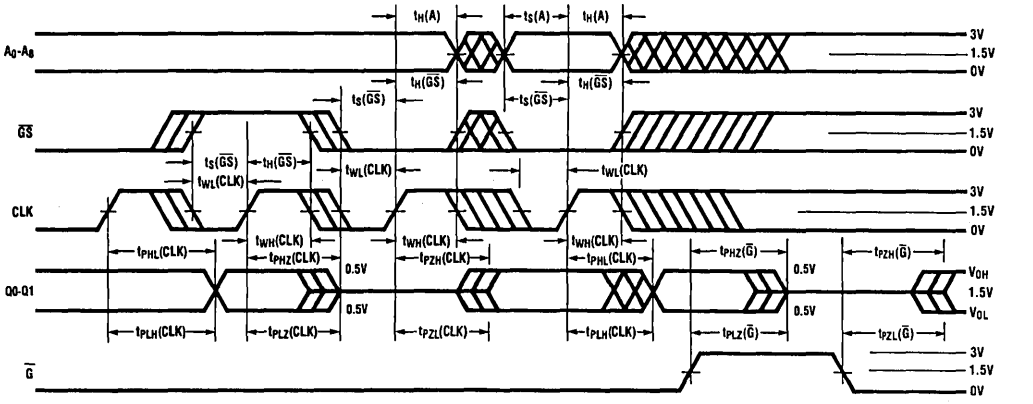
Switching Characteristics

Symbol	Parameter		DM77SR27			DM87SR27			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR27	55	20		50	20		ns
		SR27B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR27		15	30		15	27	ns
		SR27B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		25	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

Programming Parameters Do not test or you may program the device

Symbol	Parameter	Test Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current While Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4	4.2	V
V_{CCVH}	Required High V_{CC} for Verification		5.8	6	6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Switching Waveforms



TL/L/6686–3

Key To Timing Diagram

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

TL/L/6686–4

National Semiconductor Corporation

DM77/87SR183 (1k x 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR183 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 1024 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR183 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

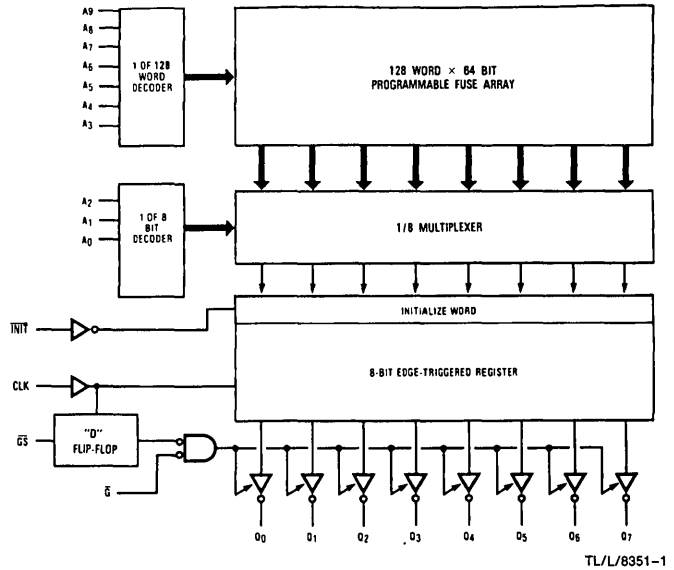
The DM77/87SR183 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S35
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 24-pin, 300 mil thin-dip package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block and Connection Diagrams



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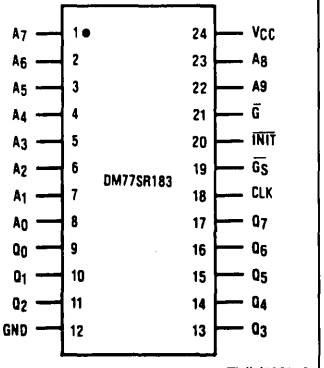


TL/L/8351–2

Top View

Order Number DM77/87SR183J, DM77/87SR183BJ, DM87SR183N, DM87SR183BN, DM87SR183V or DM87SR183BV
See NS Package J24F, N24C or V28A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2 to +5.5V
Output Voltage (Note 2)	−0.5 to +5.5V
Storage Temperature	−65° to +150°C
Lead Temperature (10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77SR183, DM77SR183B	4.50	5.50	V
DM87SR183, DM87SR183B	4.75	5.25	V
Ambient Temperature (T_A)			
DM77SR183, DM77SR183B	−55	+125	°C
DM87SR183, DM87SR183B	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_1	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		135	185		135	185	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

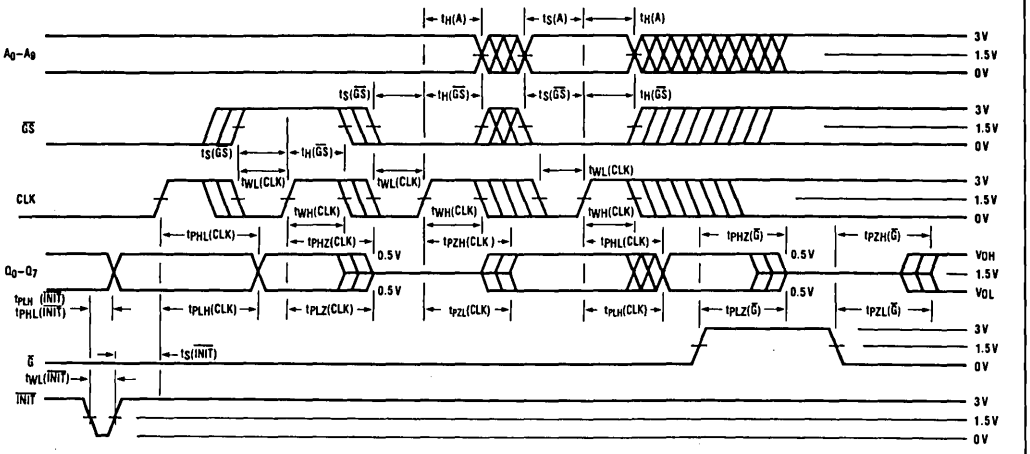
Switching Characteristics

Symbol	Parameter		DM77SR183, 183B			DM87SR183, 183B			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR183	45	20		40	20		ns
		SR183B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR183		15	30		15	25	ns
		SR183B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		20	10		15	10		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		15	0		15	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	35		20	30	ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		30	10		25	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to CLK (High)		20	10		20	10		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			20	35		20	30	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns

Programming Parameters Do not test or you may program the device.

Symbol	Parameter	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8 5.8	4 6	4.2 6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Switching Waveforms



TL/L/8351–3

Key To Timing Diagram

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

TL/L/8351–4

National Semiconductor Corporation

PRELIMINARY

DM77/87SR191, DM77/87SR193 (2k x 8) 16k-Bit Registered TTL PROM

General Description

The DM77/87SR191, DM77/87SR193 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 2K words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR191, DM77/87SR193 also offers maximum flexibility for memory expansion and data bus control by providing either synchronous or asynchronous output enables. When using the asychronous chip select function, all outputs will go "OFF" when $\overline{G}$ is held high. The output will be enabled when $\overline{G}$ is held low. When architecturally programmed to synchronous chip select, all outputs will go "OFF" synchronous to the clock if $\overline{GS}$ is held high before the rising edge of the clock. The output will synchronously be enabled if held low before the rising edge of the clock. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0–A10. During the set-up time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77SR191/DM77SR193 also features an initialize $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. When using the asynchronous initialize SR193, the initialize word is loaded into the output register when $\overline{INIT}$ is brought low. With the synchronous initialize function of the SR191, the initialize word is loaded into the master flip-flop when $\overline{INIT}_S$ is brought low and appears on the output during the rising edge of the clock. The unprogrammed state of the initialize word is all lows.

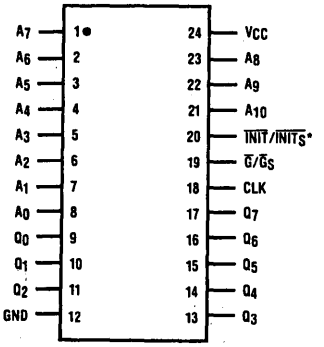
The function of chip select is shipped from the factory as an asynchronous $\overline{G}$ function and must be architecturally programmed to perform the synchronous function, $\overline{GS}$.

Features

- SR191 functionally compatible with AM27S47, SR193 compatible with AM27S45.
- On-chip, edge-triggered registers.
- Architecturally programmable asynchronous/synchronous chip select.
- Single pin INITIALIZE either synchronous (DM77/87SR191) or asynchronous (DM77/87SR193).
- 24 pin, 300 mil thin-dip package.
- 25 ns addresses setup and 15 ns clock to output for maximum system speed.
- Highly reliable, titanium tungsten fuses.
- TRI-STATE outputs.
- Low voltage TRI-SAFE™ programming.
- All parameters guaranteed over temperature.

Connection Diagram

Order Number DM77/87SR191J, DM77/87SR193J, DM77SR191N, DM77SR193N, DM77SR191V or DM77SR193V
See NS Package J24F, N24C or V28A



TL/L/5512-2

Top View

* $\overline{INIT}_S$ only on DM77/87SR191
$\overline{INIT}$ only on DM77/87SR193

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.2 to +5.5V
Output Voltage (Note 2)	−0.5 to +5.5V
Storage Temperature	−65 to +150°C
Lead Temperature (10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77SR191, DM77SR193	4.50	5.50	V
DM87SR191, DM87SR193	4.75	5.25	V
Ambient Temperature (T_A)			
DM77SR191, DM77SR193	−55	+125	°C
DM87SR191, DM87SR193	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR191, DM77SR193			DM87SR191, DM87SR193			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		140	190		140	190	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	DM77SR191, DM77SR193			DM87SR191, DM87SR193			Units
		Min	Typ	Max	Min	Typ	Max	
$t_{S(A)}$	Address to CLK (High) Setup Time	35	20		25	20		ns
$t_{H(A)}$	Address to CLK (High) Hold Time	0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)		10	20		10	15	ns
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)	15	10		12	10		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time (Note 5)	10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Time (Note 5)	5	0		5	0		ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High) (Note 8)		20	30		20	25	ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low) (Note 8)	15	10		15	10		ns
$t_{H(\overline{INITS})}$	$\overline{INITS}$ to CLK (High) Hold Time (Note 7)	0	−5		0	−5		ns
$t_{S(\overline{INITS})}$	$\overline{INITS}$ to CLK (High) Setup Time (Note 7)	30	20		25	20		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (Low or High) to CLK (High) (Note 8)	20	10		20	10		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low) (Note 5)		20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High) (Note 6)		15	30		15	25	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE) (Note 5)		20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE) (Note 6)		15	30		15	25	ns

Programming Parameters Do not test or you may program the device

Symbol	Parameter	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10	10.5	11	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10	10.5	11	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1		10	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8 5.8	4 6	4.2 6.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

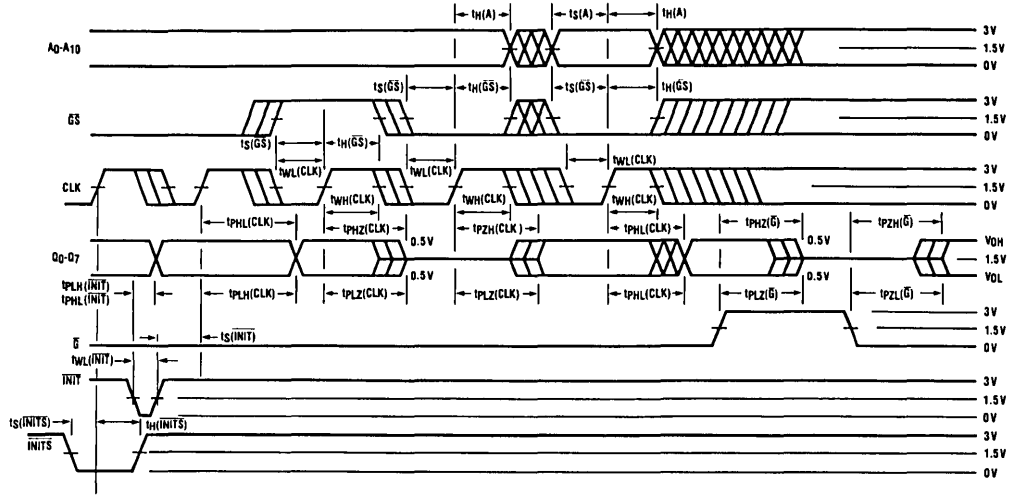
Note 5: Applies only when asynchronous ENABLE ($\overline{GS}$) function is used

Note 6: Applies only when synchronous ENABLE ($\overline{G}$) function is used

Note 7: Applies to synchronous $\overline{INITS}$ function DM77/87SR191.

Note 8: Applies to asynchronous $\overline{INIT}$ function DM77/87SR193.

Switching Waveforms



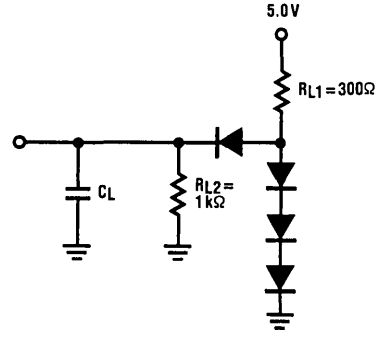
TL/L/5512-3

Key To Timing Diagram

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

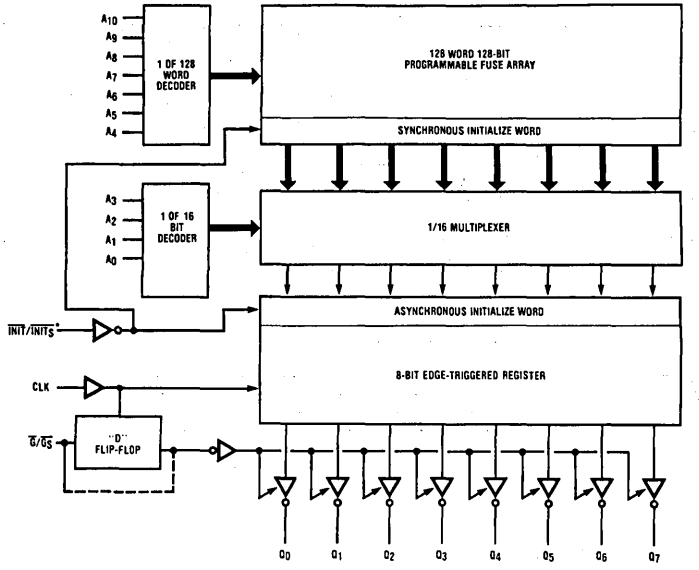
TL/L/5512-4

AC Test Load



TL/L/5512-7

Block Diagram



TL/L/5512–1

*$\overline{\text{INITS}}$ only on DM77/87SR191
$\overline{\text{INIT}}$ only on DM77/87SR193

National Semiconductor Corporation

Bipolar PROM Devices in Plastic Leaded Chip Carriers (PLCC)

Introduction of Surface Mount Technology

Recent years have seen rapid advances in microcircuit technology. The integrated circuits of the 1980's are more complex than the circuit boards of the 1960's. It is evident that the next decade will bring demands for packages with higher lead counts and closer lead spacing, both to support the greater system density sought by designers.

National Semiconductor Corporation is committed to surface mount devices, for they provide the most practical solution to these needs. Geared to development of high-complexity semiconductor chips National has placed great emphasis on package development and introducing plastic leaded chip carriers with various number of leads as surface mounted components.

Features of Surface Mount Devices

Surface mount devices have additional features compared to molded Dual-In-Line Packages (DIP):

1. Compact design that saves space during assembly.
2. Mounting on both sides of the substrate.
3. Easier handling and excellent reliability.
4. Automation of the assembly process.
5. Lower board manufacturing costs.
6. Improved operating speed.
7. Increased board density and reduced weight.

Applications

Surface mount devices can be used where substrate size, as well as weight and thickness are limited. The surface mount device can also be used in areas where conventional packages cannot be used. Areas of application include; portable video cassette recorders, video cameras, hand-held computers, personal computers, electronic toys, car electronics, cameras, telephones, and various telecommunication equipment.

Products in PLCC

National Semiconductor has a broad Family of high performance PROMs. All the PAL and PROM products presently offered in DIP packages will now be available in the PLCC (plastic leaded chip carrier) package including the 15 ns industries fastest PAL.

Advantages of PLCC

1. Permits automated assembly.
2. Lower manufacturing costs.
3. Smaller PCC size, reduces board density and weight.
4. Lower noise and improved frequency response resulting from shorter circuit paths. Automated assembly ensures accurate component placement which improves reliability and provides more consistent product quality.

Additional Information

National Semiconductor offers a variety of technical briefs covering surface mount topics. These include:

STAR™ Tape-and-Reel Shipping System
Order Number 113635

Getting Started in Surface Mount (Equipment Suppliers)
Order Number 570435

A Basic Guide to Surface Mounting of Electronic Components
Order Number 113615

Reliability Report: Small Outline Packages
Order Number 570430

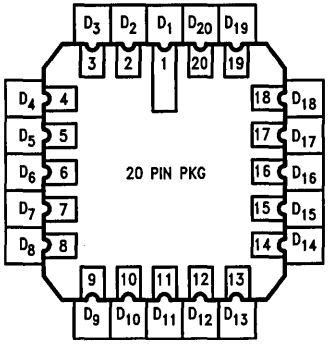
Reliability Report: Plastic Chip Carrier
Order Number 980040

Surface Mount Technology Notebook
Order Number 980020

Plastic Chip Carrier Technology
Order Number 113295

Connection Diagrams

Plastic Chip Carrier (PLCC)

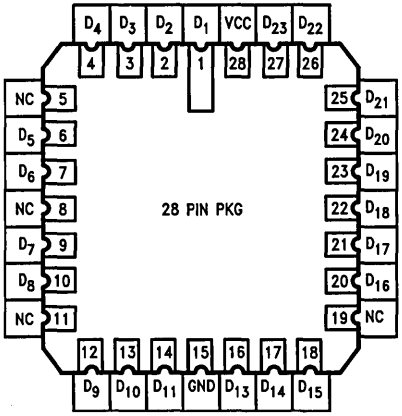


TL/L/9261-1

Note: D1 = DIP Pin 1

Top View

Plastic Chip Carrier (PLCC)



TL/L/9261-2

D1 = DIP Pin 1

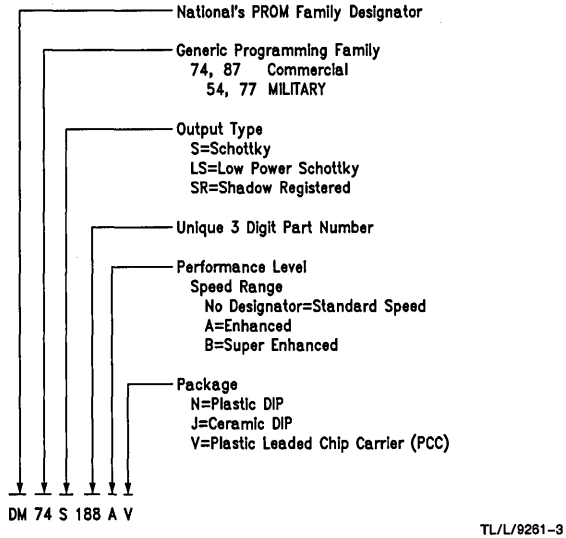
NC = No Connect

Top View

PROM

ORDERING INFORMATION

Example:

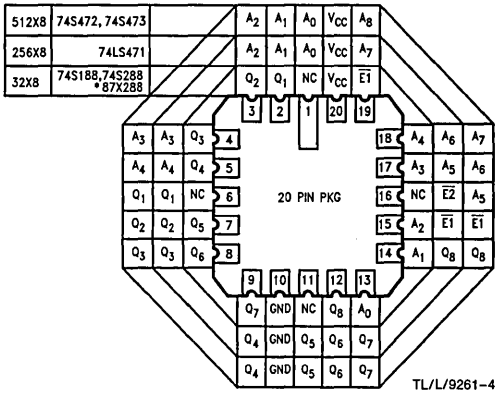


TL/L/9261-3

PROM

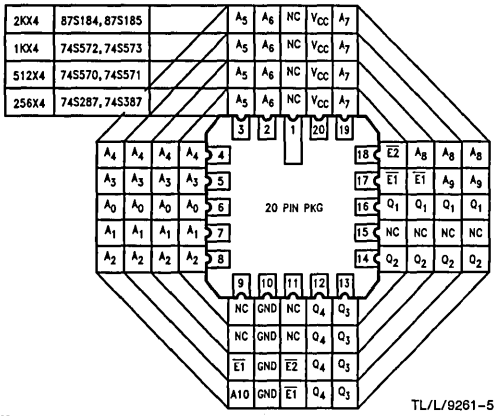
Series-20 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PCC pins
			STD	A-Series	B-Series			
DM74S188 OC DM74S288 TS	256	32 × 8	35	25	—	110	16	
PL87X288 TS	256	32 × 8	—	—	15	140	16	
DM74S287 TS DM74S387 OC	1K	256 × 4	50	30	—	130	16	
DM74S570 OC DM74S571 TS	2K	512 × 4	55 55	45 45	— 35	130	16	
DM74LS471 TS	2K	256 × 8	60	—	—	100	20	20
DM74S572 OC DM74S573 TS	4K	1,024 × 4	60 60	45 45	— 35	140 140	18 18	
DM74S472 TS DM74S473 OC	4K	512 × 8	60 55	45 45	35 —	155 155	20 20	
DM87S184 OC DM87S185 TS	8K	2048 × 4	55 55	45 45	— 35	140 140	18 18	



TL/L/9261–4

*For 87 x 288, outputs are numbered Q_0 through Q_7



TL/L/9261–5

Top View

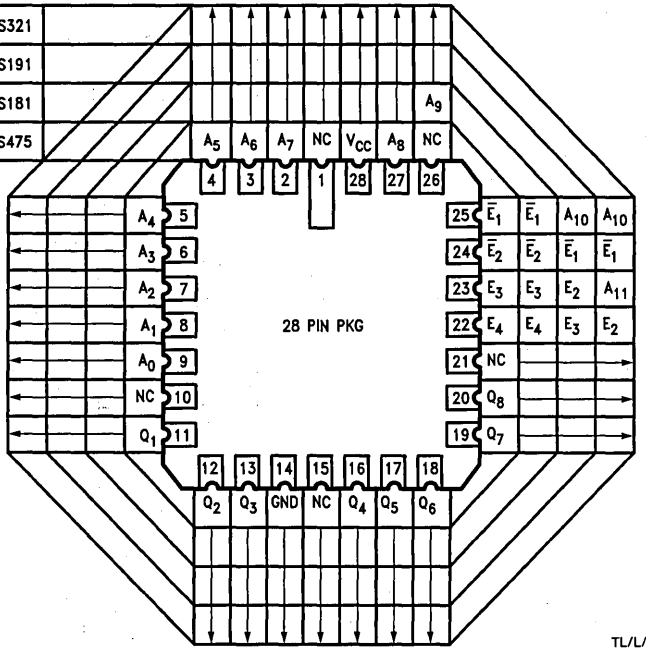
Series-24 Selection Chart

Device	Size (Bits)	Configuration	TAA (max) in ns			ICC max in mA	DIP pins	PCC pins
			STD	A-Series	B-Series			
DM74S474 TS DM74S475 OC	4K	512 × 8	65	45	35	170	24	
DM87SR474 REG DM87SR476 REG	4K	512 × 8	50*	—	35*	170	24	
DM87S180 OC	8K	1024 × 8	55	—	—	170	24	28
DM87S181 TS			55	45	—			
DM87LS181 TS			120	—	—			
DM87SR181 REG			40*	—	—			
DM87SR183 REG			40*	35*	—			
DM87S190 OC	16K	2048 × 8	65	45	—	175	24	
DM87S191 TS			65	45	35			
DM87SR191 REG			25*	—	—			
DM87SR193 REG			25*	—	—			
DM87S321 TS	32K	4096 × 8	55	—	—	185	24	

*setup time

Plastic Chip Carrier

4KX8	87S321
2KX8	87S190, 87S191
1KX8	87S180, 87S181, 87LS181
512X8	74S474, 74S475

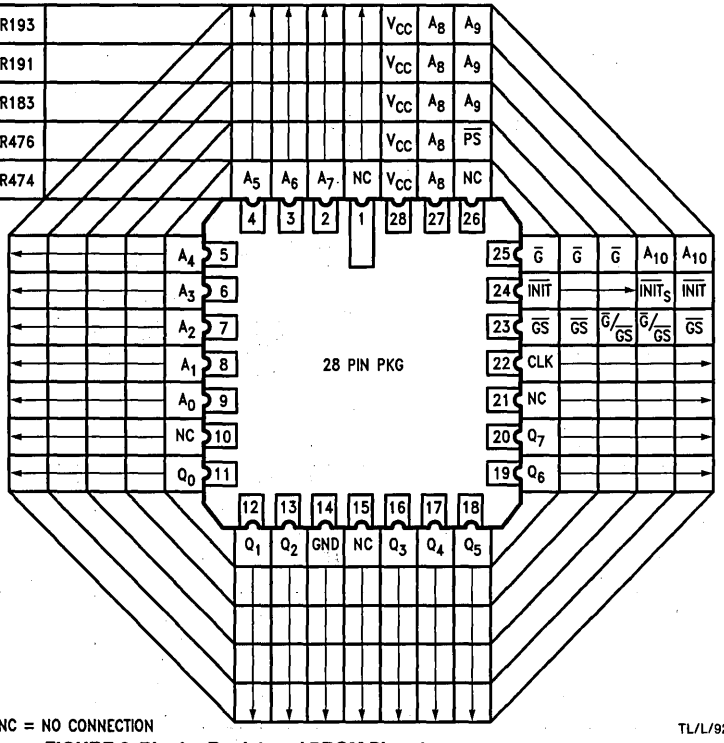


TL/L/9261–6

FIGURE 5. Bipolar PROM Pinout

Plastic Chip Carrier

2KX8	77SR193
2KX8	77SR191
1KX8	87SR181, 87SR183
512X8	77SR476
512X8	77SR474



NC = NO CONNECTION

TL/L/9261–7

FIGURE 6. Bipolar Registered PROM Pinout

Programming Support

PROM devices may be programmed with hardware and software readily available in the market. Most programmer manufacturers will offer a PCC adapter which will fit in existing equipment. For the availability of PCC adapter please check with your programmer manufacturer.

Programming Equipment

1. Data I/O
2. Structured Design
3. Stag
4. Dig Elec
5. Kontron
6. Prolog
7. Citel

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T_1 = 100 ns Min.

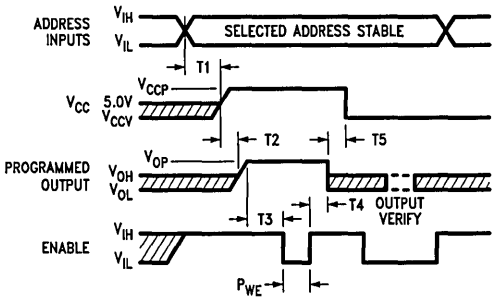
T_2 = 5 μs Min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})

T_3 = 100 ns Min.

T_4 = 100 ns Min.

T_5 = 100 ns Min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.



NOTE: ENABLE WAVEFORM FOR AN ACTIVE LOW ENABLE. SOME PROMS HAVE MORE THAN ONE CHIP ENABLE. HOLD ALL OTHER ENABLE(S) TO ACTIVE STATE(S).

TL/00/2506-1

Registered PROM Programming Procedure

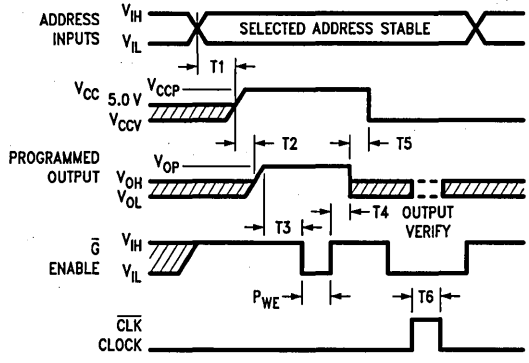
National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. $\overline{GS}$ is held low during the entire programming time.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10.0 V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10.0 V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum. (Remember that the outputs of the device are disabled at this time).
   d) Enable the device by taking the chip enable ($\overline{G}$) to a low level. This is done with a pulse of 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V) for one verification and to 6.0V (±0.2V) for a second verification. Verification at V_{CC} levels of 4.0V and 6.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) The initialize word is programmed by setting $\overline{INIT}$ input to a logic low and programming the initialize word output by output in the same manner as any other address. This can be accomplished by inverting the A9 address input from the PROM programmer and applying it to the $\overline{INIT}$ input. Using this method, the initialize word will program at address 512.
   g) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   h) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCVH}	Required High V_{CC} for Verification		5.8	6.0	6.2	V
V_{CCVL}	Required Low V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM

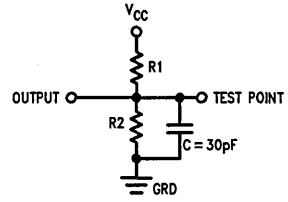


TL/00/2506–2

T_1 = 100 ns Min.
T_2 = 5 μs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)
T_3 = 100 ns Min.
T_4 = 100 ns Min.
T_5 = 100 ns Min.
T_6 = 50 ns Min.

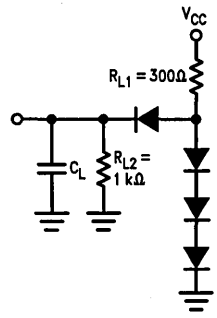
Standard Test Loads

Non-Registered PROMs



TL/00/2506-3

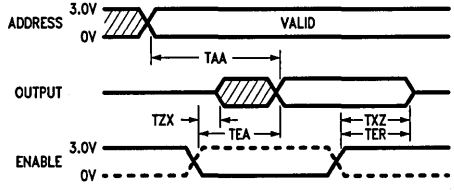
Registered PROMs



TL/00/2506-8

Switching Time Waveforms

Non-Registered PROM



TL/00/2506-4

*Device input waveform characteristics are;
Repetition rate = 1 MHz
Source impedance = 50Ω
Rise and Fall times = 2.5 ns max.
(1.0 to 2.0 volt levels)

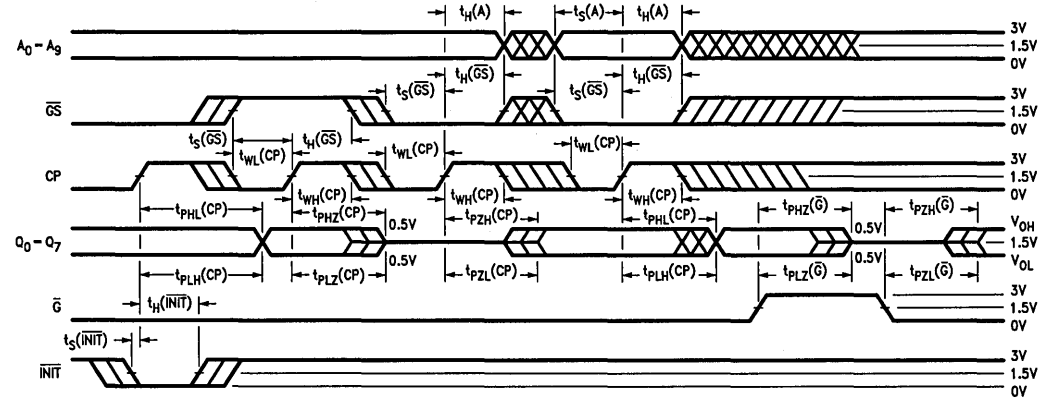
*TAA is measured with stable enable inputs.

*TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.

*For I_{OL} = 16 mA, R1 = 300Ω and R2 = 600Ω
*for I_{OL} = 12 mA, R1 = 400Ω and R2 = 800Ω.

*"C" includes scope and jig capacitance.

Switching Waveforms Registered PROM



TL/00/2506-5

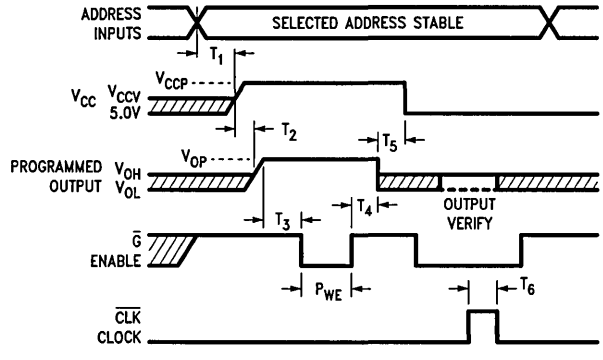
Key To Timing Diagram

Waveform	Inputs	Outputs	Waveform	Inputs	Outputs
	Must Be Steady	Will Be Steady		Don't Care: Any Change Permitted	Changing: State Unknown
	May Change from H to L	Will Be Changing from H to L		Does Not Apply	Center Line Is High Impedance "OFF" State
	May Change from L to H	Will Be Changing from L to H			

Programming Parameters Do not test or you may program the device

Symbol	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} during Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM



TL/00/2506-9

T_1 = 100 ns Min.
T_2 = 5 μs Min. (T2 may be > 0 if V_{CCP} rises at the same rate or faster than V_{OP}.)
T_3 = 100 ns Min.
T_4 = 100 ns Min.
T_5 = 100 ns Min.
T_6 = 50 ns Min.

Approved Programmers for NSC PROMs

Manufacturer	System #
DATA I/O	5/17/19/29A
PRO-LOG	M910,M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C Parametric and Functionality	25°C	0.05	D.C Parametric and Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

Section 4

Physical Dimensions

Section 4 Contents

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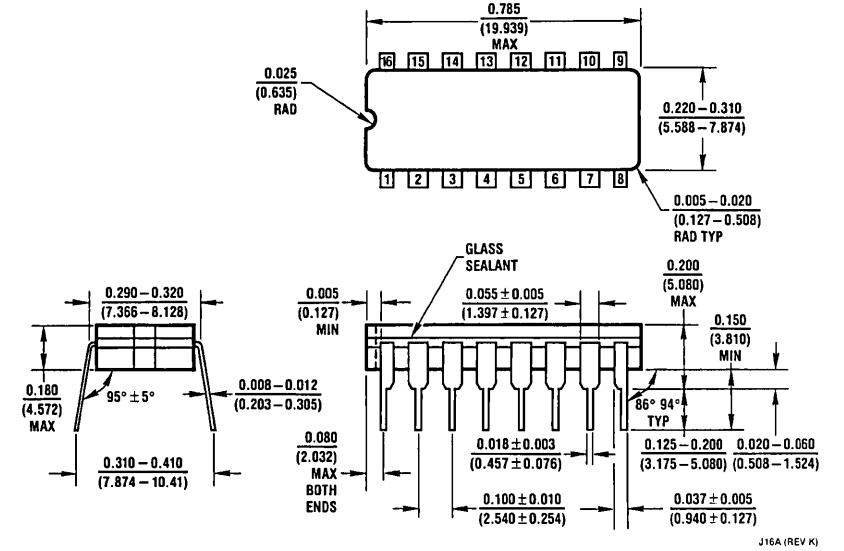
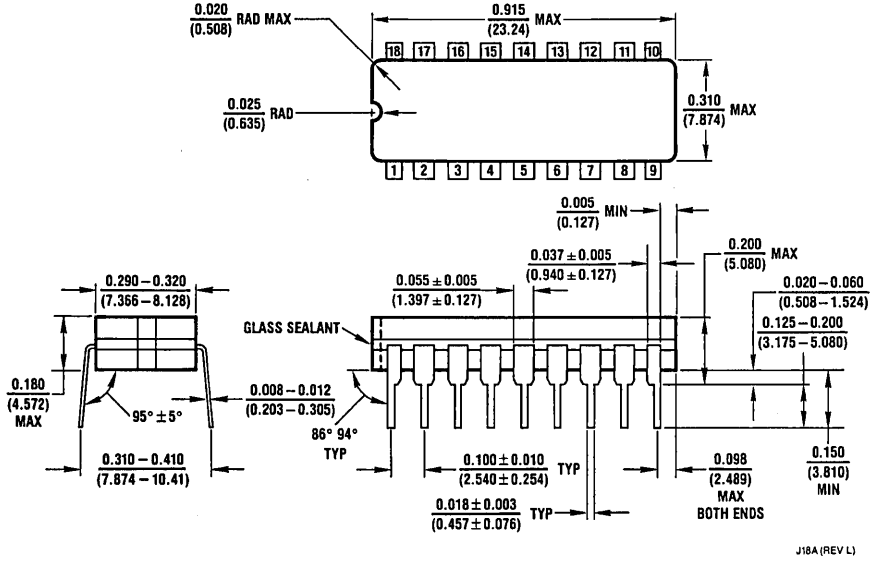
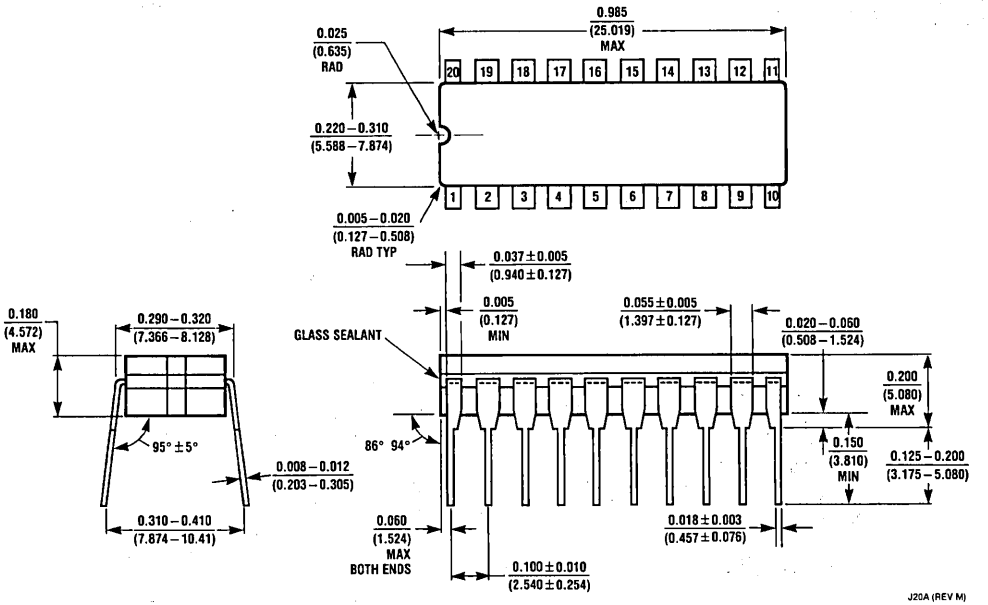
All dimensions are in inches (millimeters)



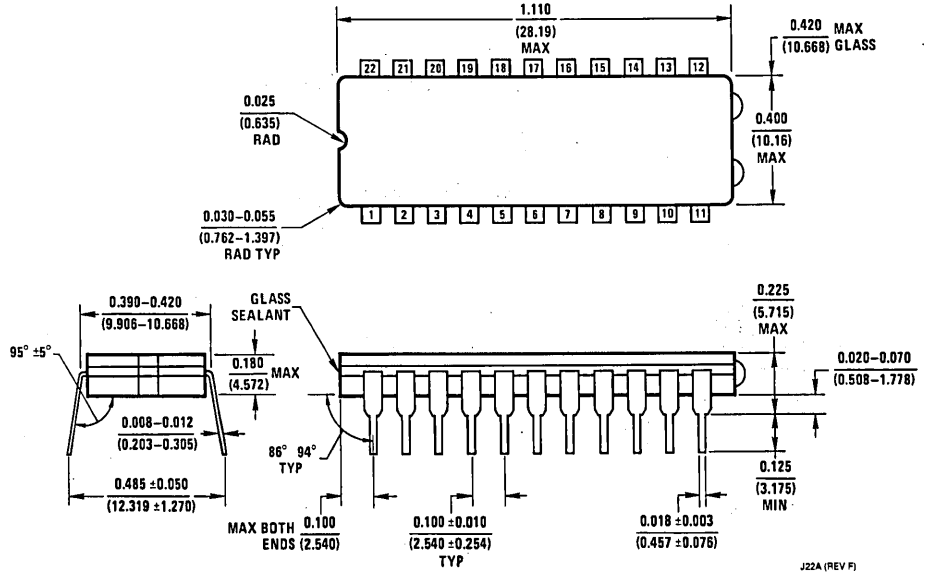
NS Package J16A



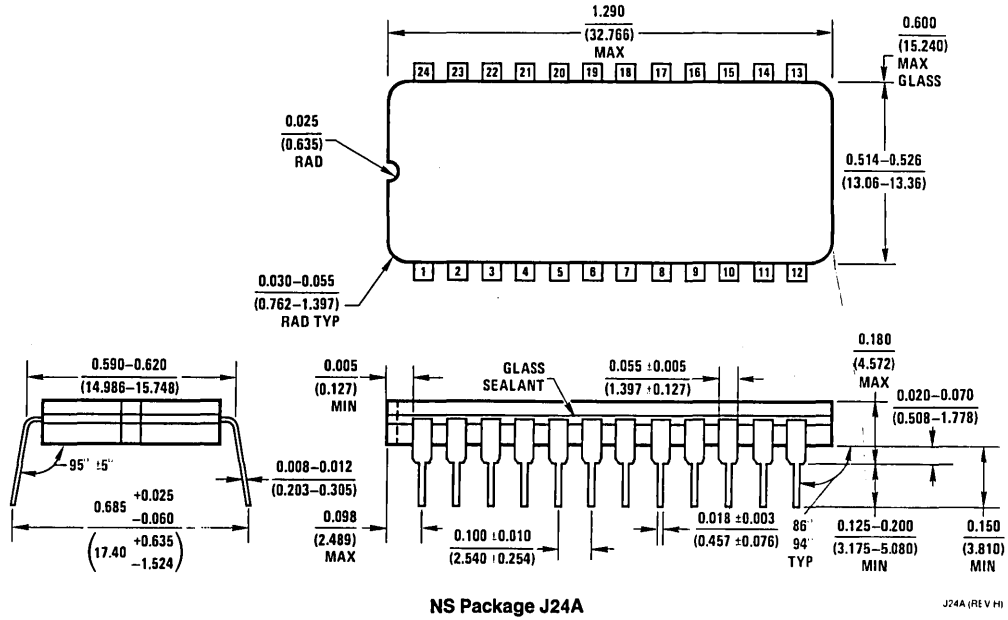
NS Package J18A



NS Package J20A

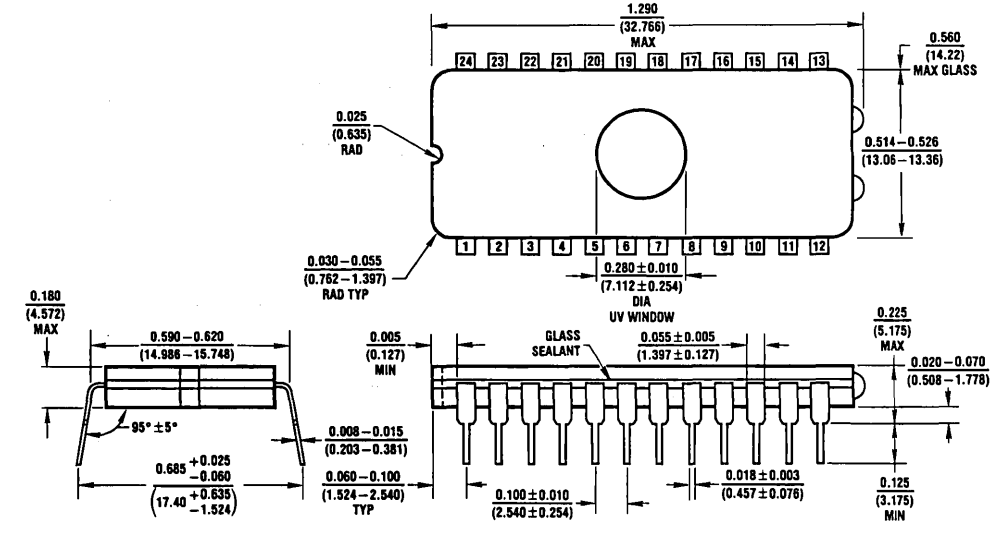


NS Package J22A

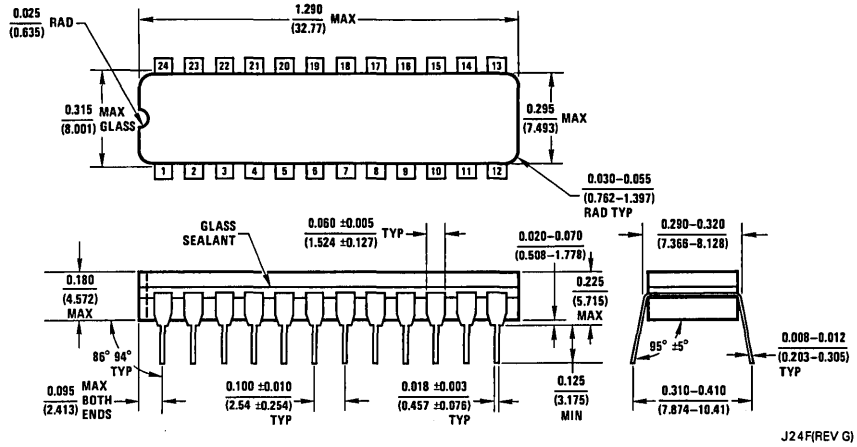


NS Package J24A

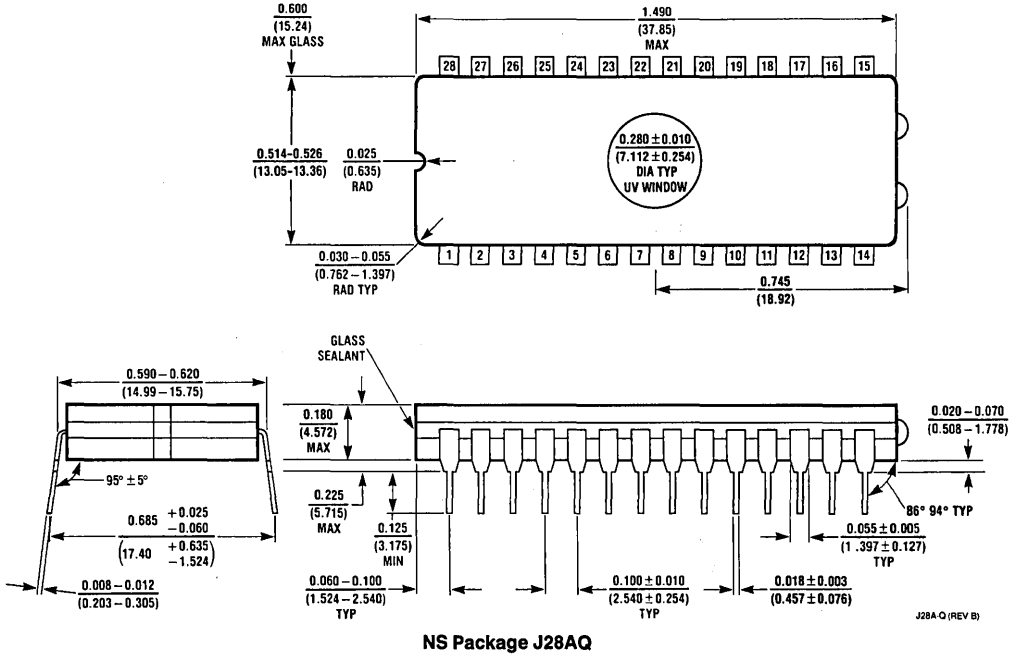
J24A (REV H)



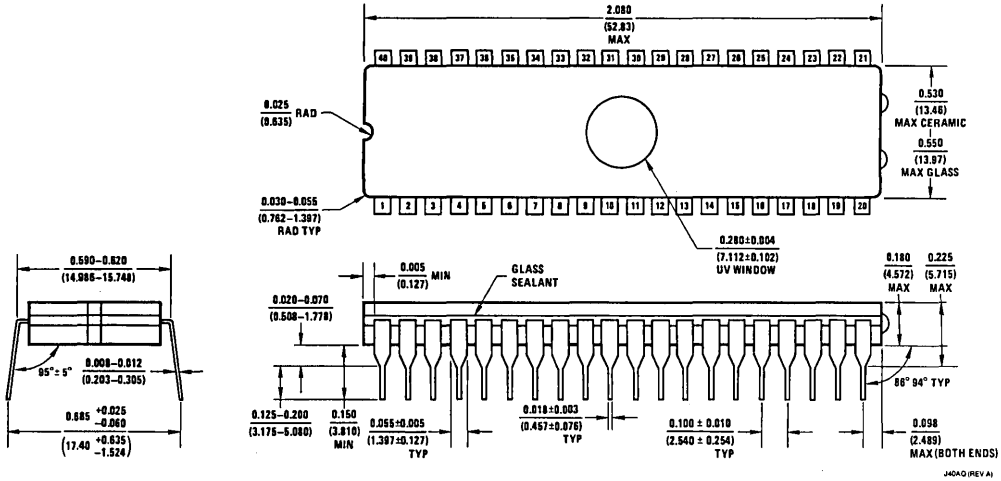
NS Package J24AQ



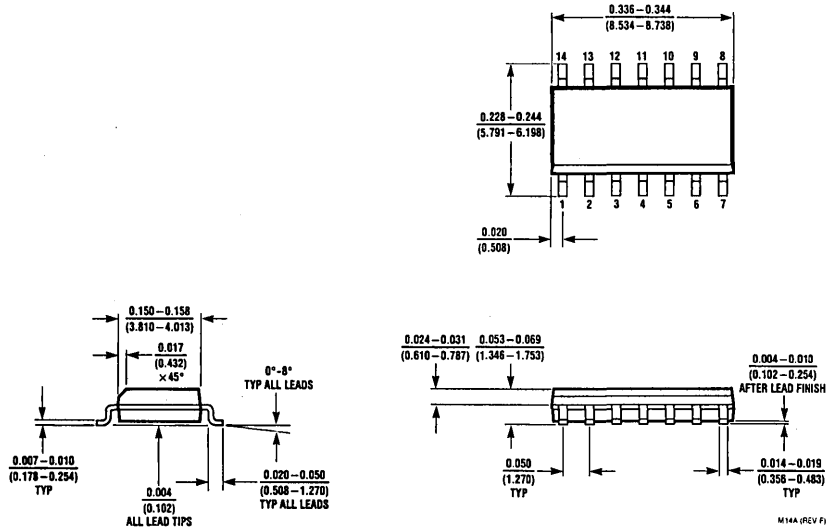
NS Package J24F



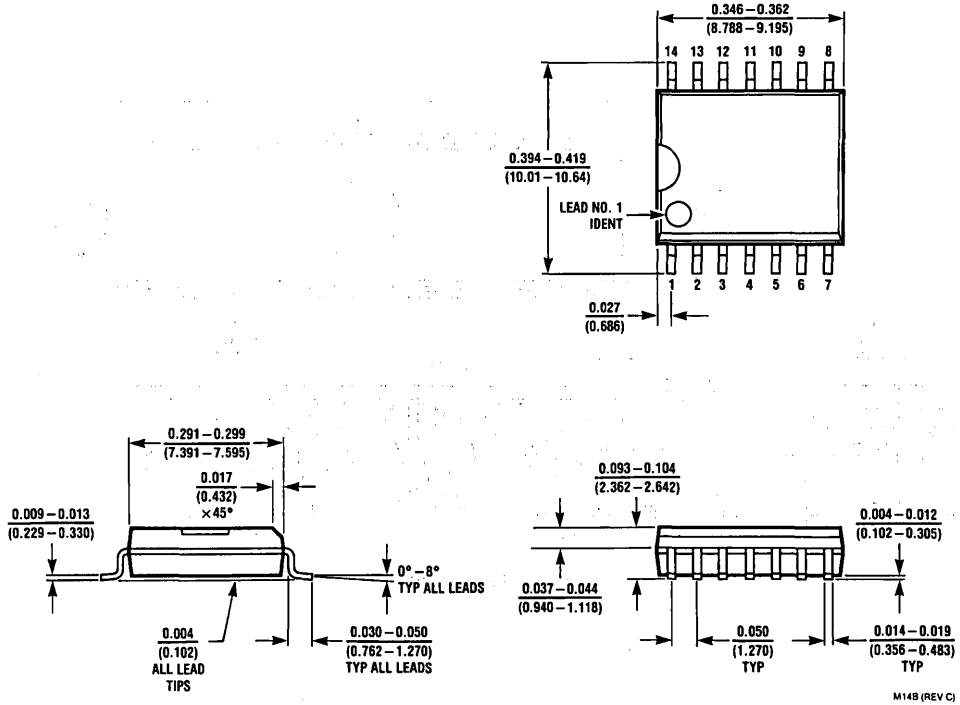
NS Package J28AQ



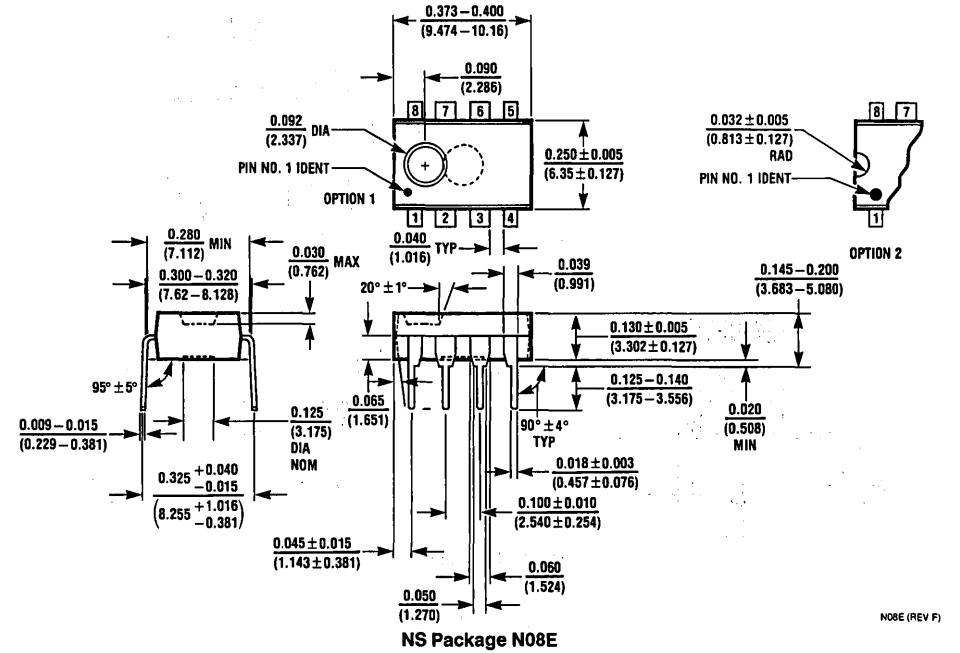
NS Package J40AQ



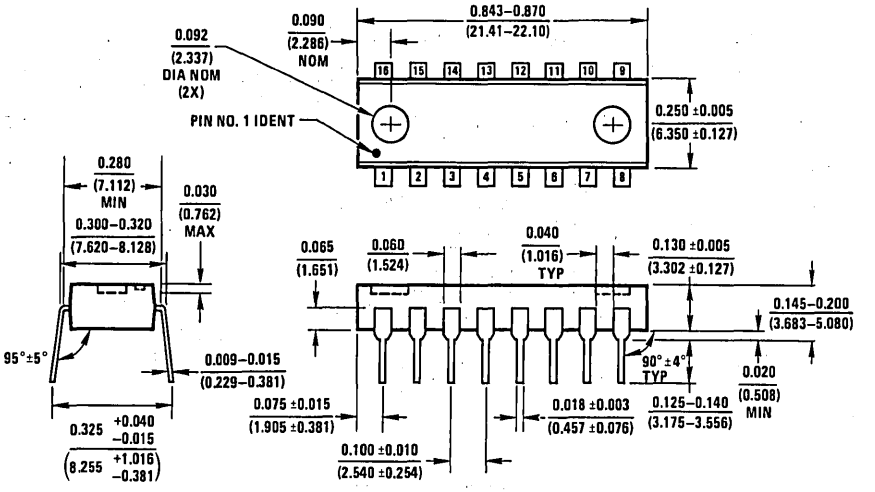
NS Package M14A



NS Package M14B

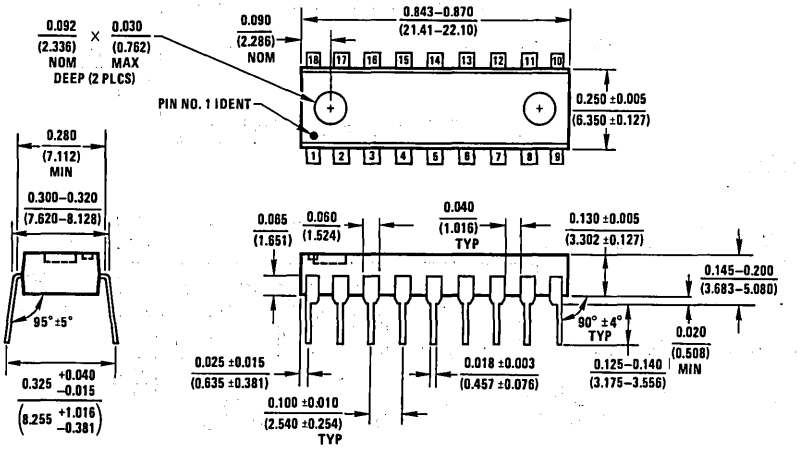


NS Package N08E



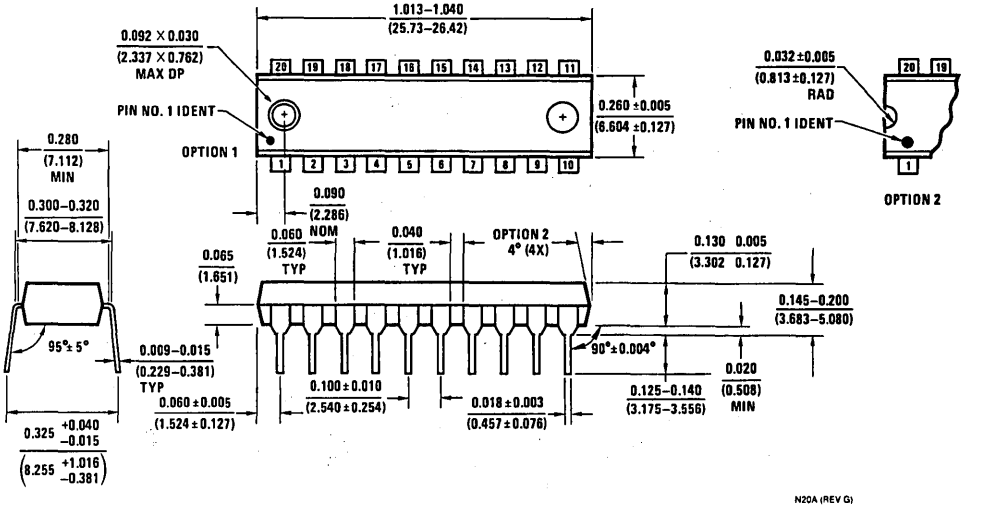
NS Package N16A

N16A (REV E)

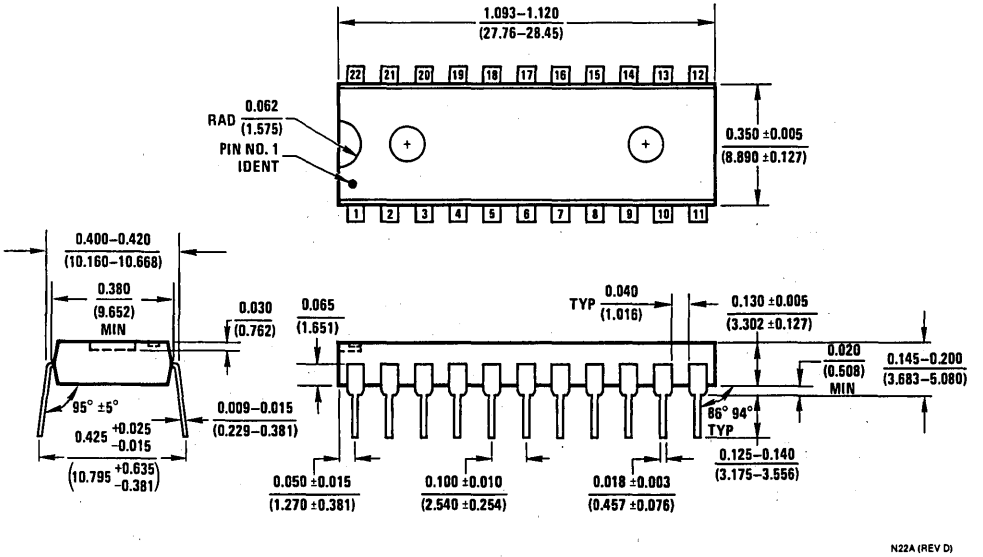


N18A (REV E)

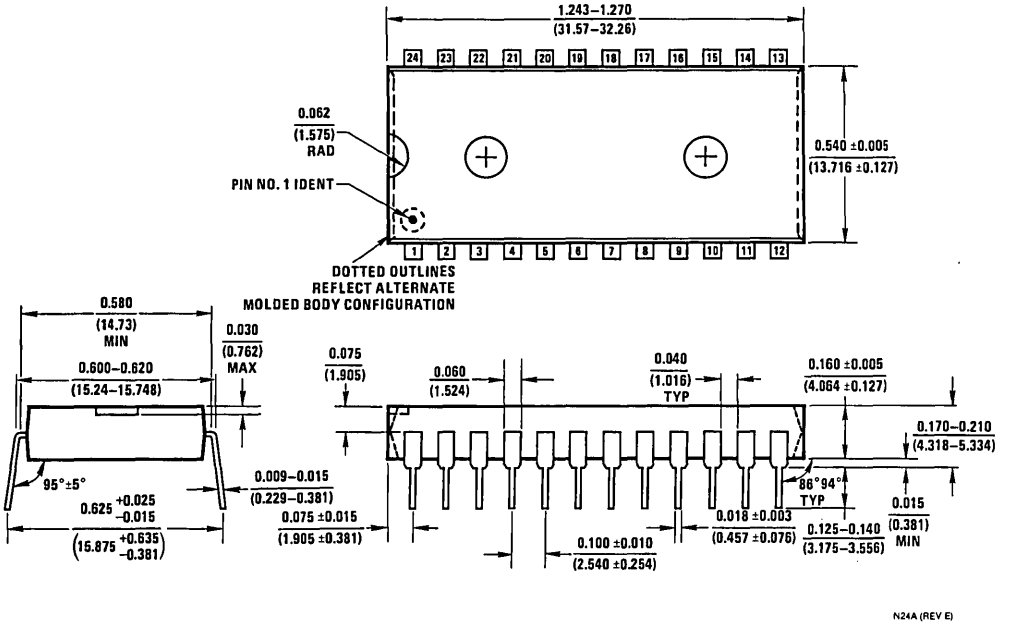
NS Package N18A



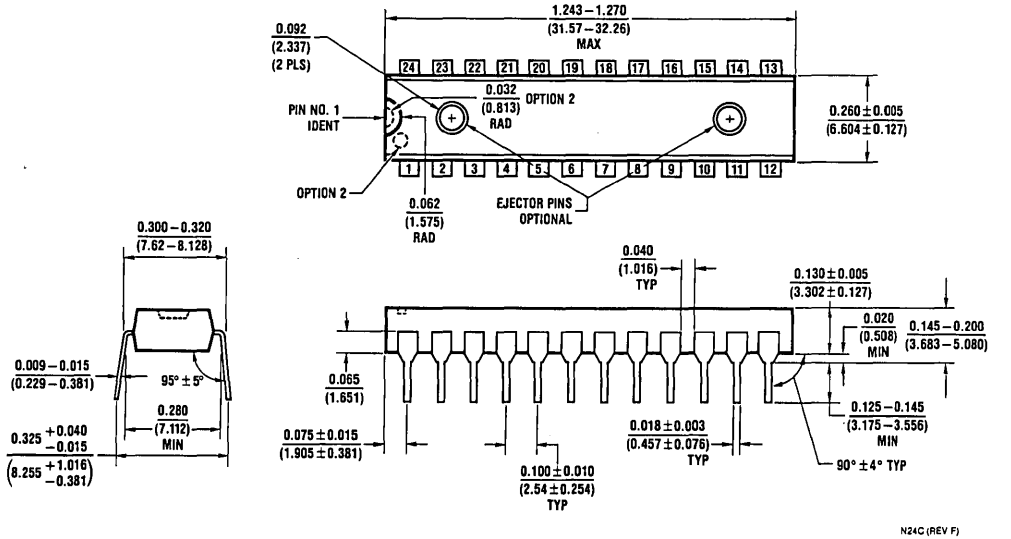
NS Package N20A



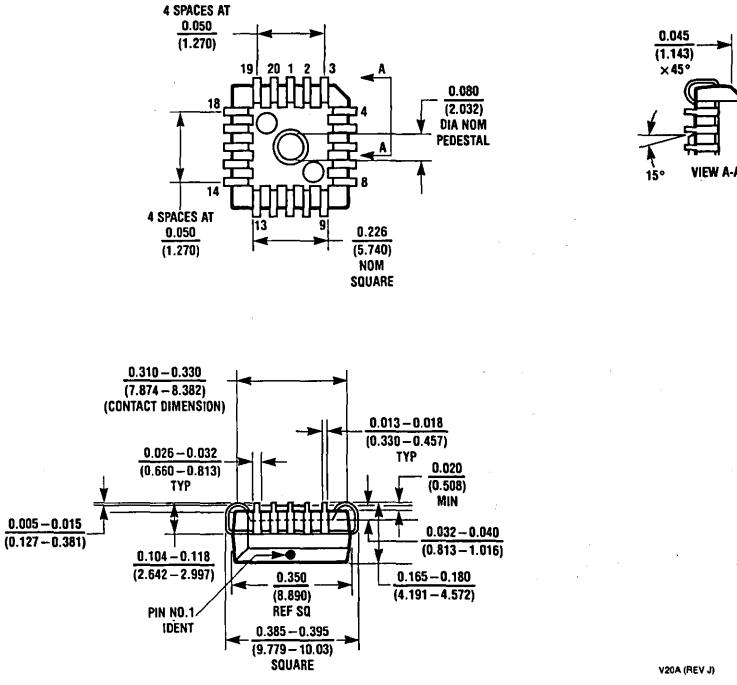
NS Package N22A



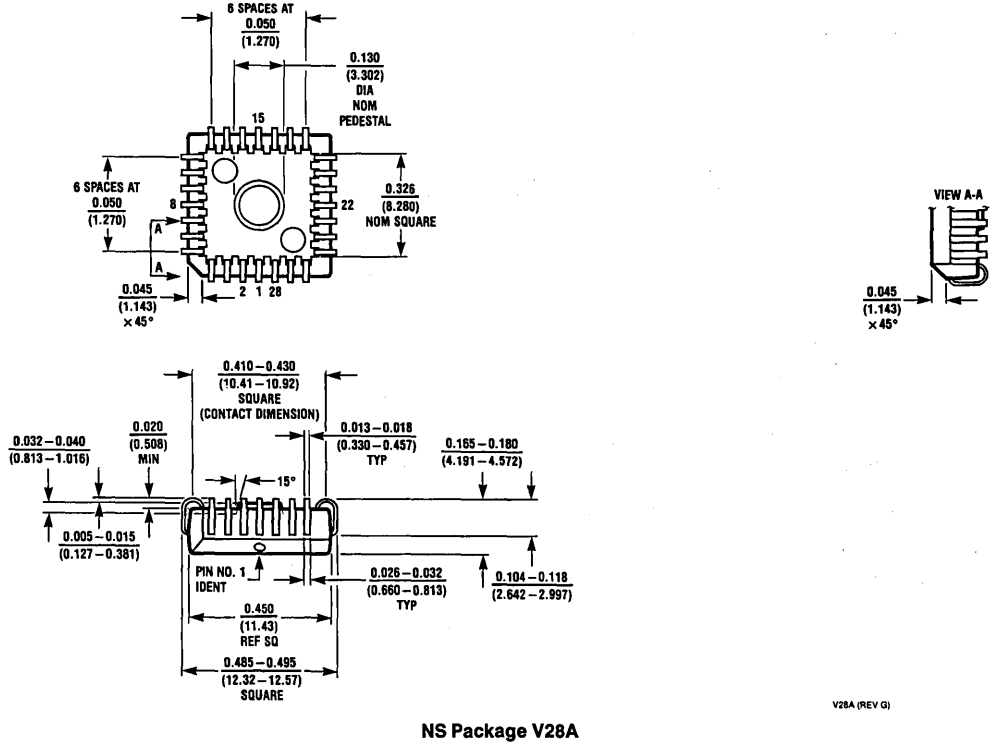
NS Package N24A



NS Package N24C



NS Package V20A



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