EEPROM
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

JULY 1985

A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen von hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauer von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung sind die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig. Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et à augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

EEPROM
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Datasheets

Application Notes

Reliability Information

Physical Dimensions

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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EEPROM Databook

Introduction

National Semiconductor Corporation's EEPROM Databook is a comprehensive collection of information on advanced, non-volatile memory products covering the spectrum of this mainstream semiconductor component category.

Virtually every electronic system being designed today requires some level of storage capacity. National is committed to designing and supplying high-performance programmable non-volatile EPROMs and EEPROMs which are currently finding increasing usage in a wide range of microprocessor-based systems.

National is committed to technical excellence in design, manufacturing, reliability and service to our customers through the continuing development of new devices. If you don't find the memory products you need in this book, please contact your local National Semiconductor sales office or distributor.

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Section 1

Datasheets

National Semiconductor

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

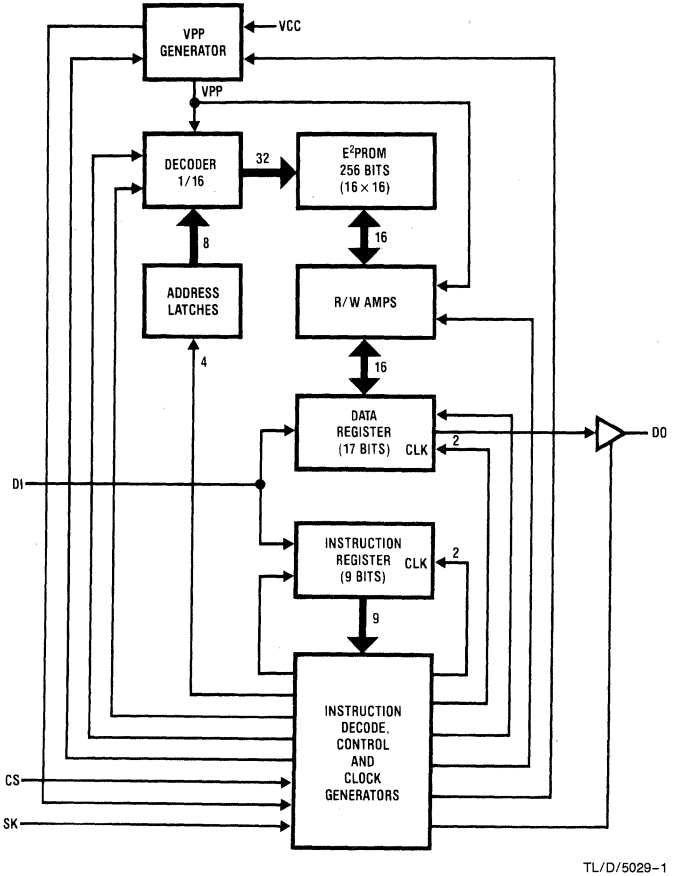
General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



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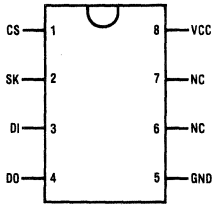
Dual-In-Line Package



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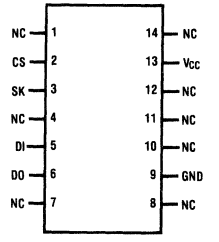
Top View

SO Package



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Top View

Order Number NMC9306N, NMC9306
See NS Package N08E or M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

1

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9306/COP494	0°C to +70°C
Ambient Storage Temperature	
with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics 0°C ≤TA≤ 70°C, V_{CC}=5V±10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC}=5.5V, CS=1			10	mA
Standby Current (I_{CC2})	V_{CC}=5.5V, CS=0			3	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC}+1	V
Output Voltage Levels					
V_{OL}	I_{OL}=2.1 mA			0.4	V
V_{OH}	I_{OH}=−400 μA	2.4			V
Input Leakage Current	V_{IN}=5.5V			10	μA
Output Leakage Current	V_{OUT}=5.5V, CS=0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL=100 pF				
DO t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V			2	μs
t_{PD0}	V_{IL}=0.45V, V_{IH}=2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

NMC9306/COP494 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9306/COP494 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. after a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

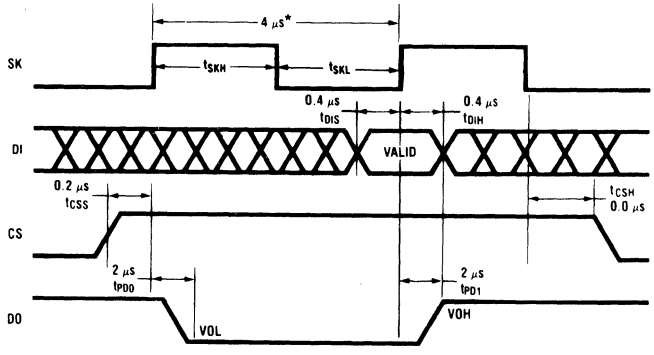
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams



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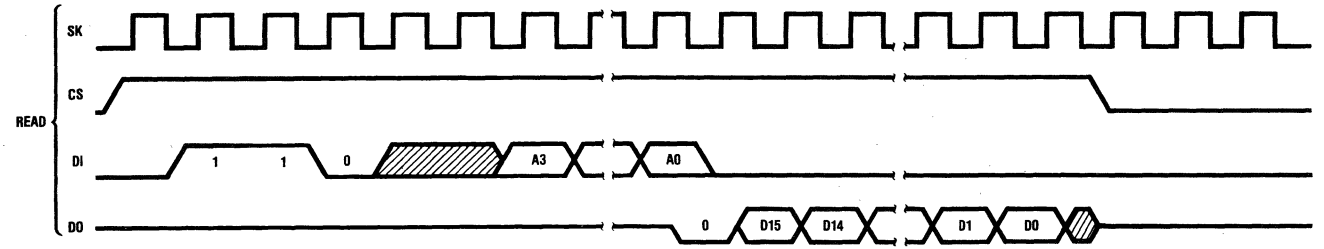
*This is the minimum SK period

Synchronous Data Timing

Timing Diagrams (Continued)



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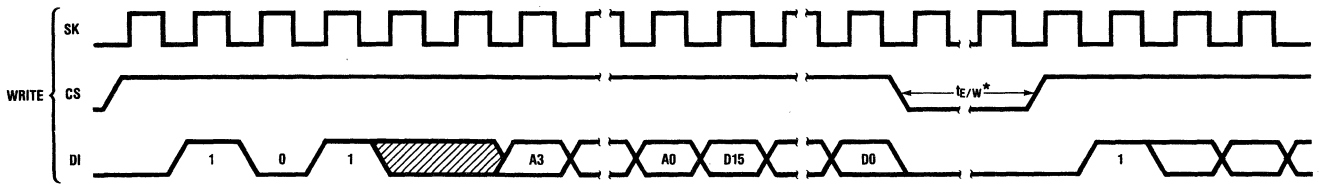

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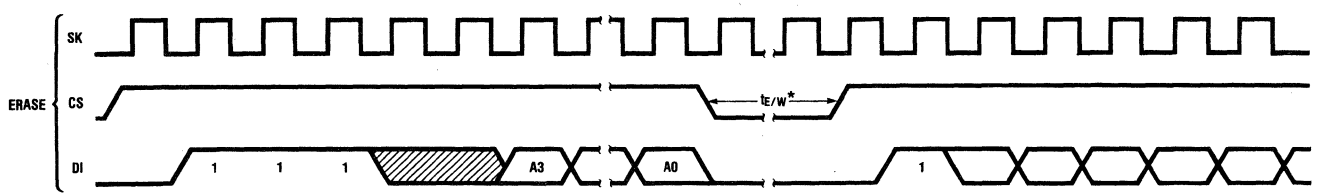

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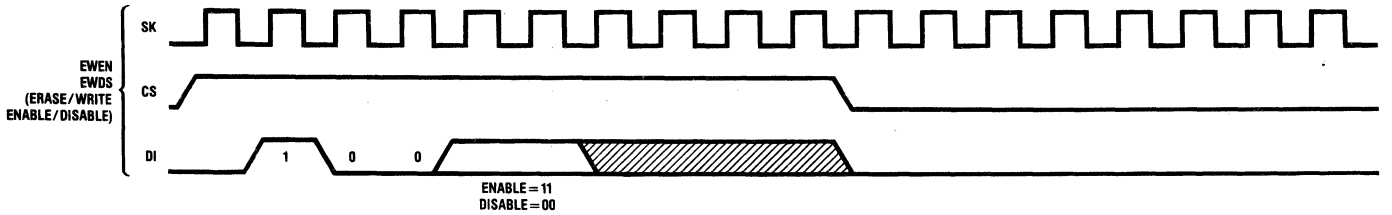
*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing



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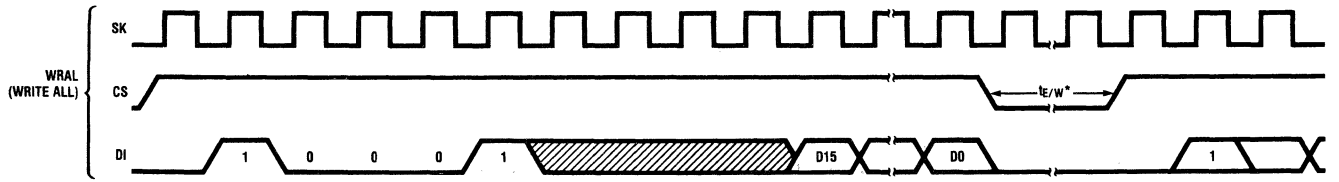

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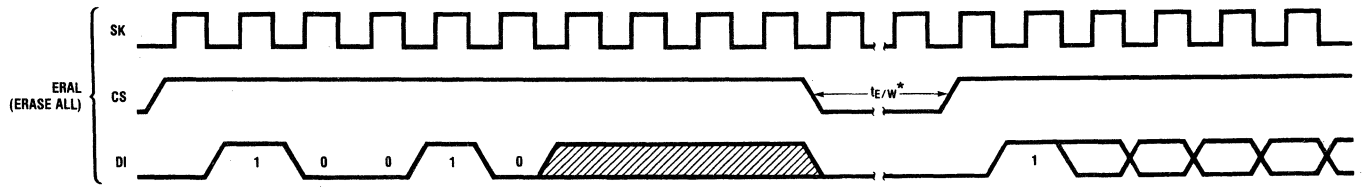

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*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)

National Semiconductor

NMC9306E/COP494E 256-Bit Serial Electrically Erasable Programmable Memory

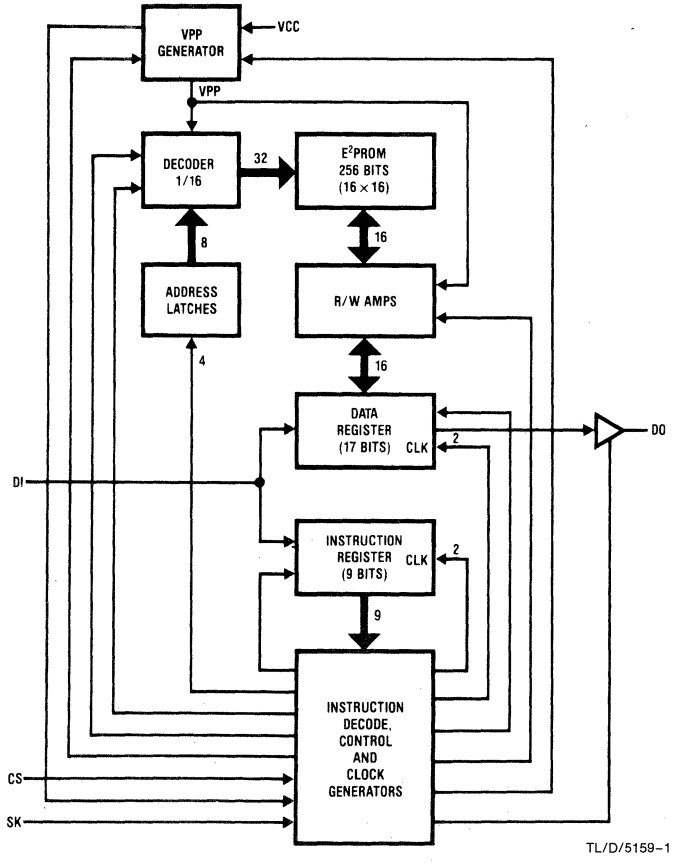
General Description

The NMC9306E/COP494E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306E/COP494E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ±10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



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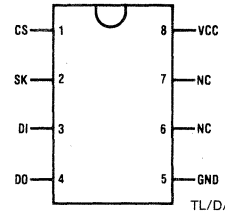
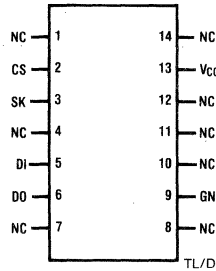
Dual-In-Line Package



TL/D/5159–2

Top View

SO Package



TL/D/5159–10

Top View

FIGURE 2

Order Number NMC9306NE, 9306
See NS Package N08E, M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature NMC9306E/COP494E	−40°C to +85°C
Ambient Storage Temperature with Data Retention	−65°C to +125°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics −40°C ≤ TA ≤ +85°C, VCC = 5V ±10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (VCC)		4.5		5.5	V
Operating Current (ICC1)	VCC = 5.5V, CS = 1			10	mA
Standby Current (ICC2)	VCC = 5.5V, CS = 0			3	mA
Input Voltage Levels					
VIL		−0.1		0.8	V
VIH		2.0		VCC+1	V
Output Voltage Levels					
VOL	IOL = 2.1 mA			0.4	V
VOH	IOH = −400 μA	2.4			V
Input Leakage Current	VIN = 5.5V			10	μA
Output Leakage Current	VOUT = 5.5V, CS = 0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME T_{SKL} (Note 2)		1			μs
Input Set-up and Hold Times					
CS T_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	C_L = 100 pF				
DO t_{PD1}	V_{OL} = 0.8V, V_{OH} = 2.0V			2	μs
t_{PD0}	V_{IL} = 0.45V, V_{IH} = 2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1 μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15-D0	Write all registers

NMC9306E/COP494E has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

FIGURE 3

Functional Description

The NMC9306E/COP494E is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (VCC). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to VIH, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

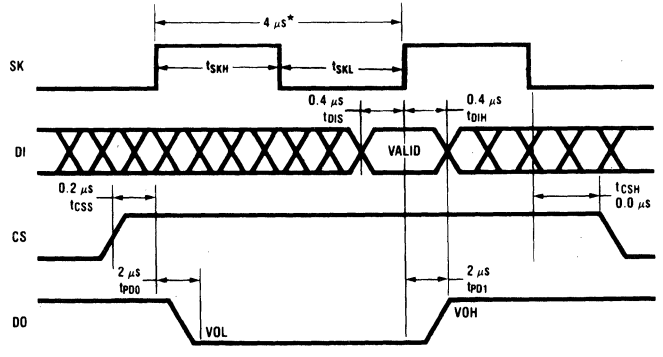
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction. i.e. start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width (t_{EW}).

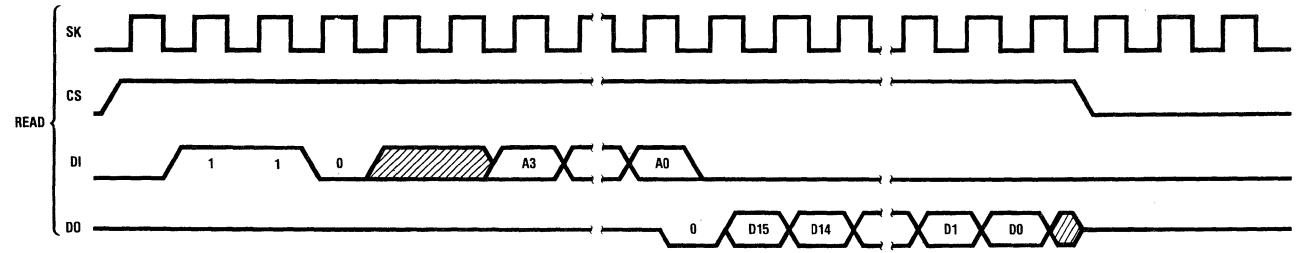
Timing Diagrams



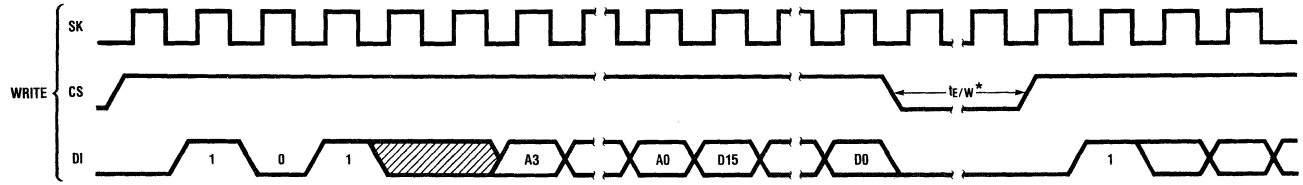
TL/D/5159–3

* This is the minimum SK period

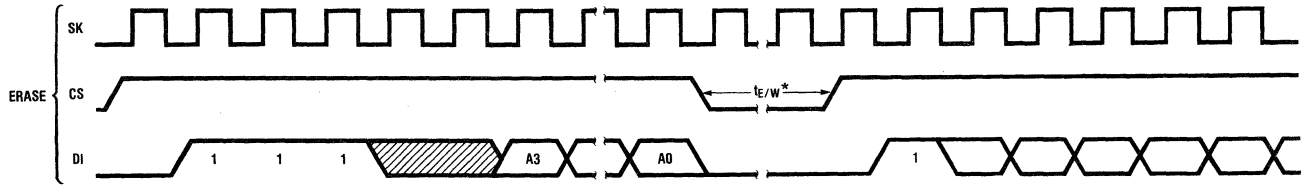
FIGURE 4. Synchronous Data Timing



TL/D/5159–4



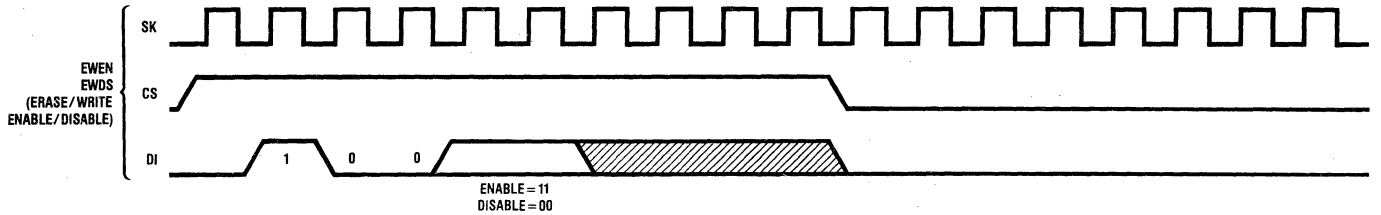
TL/D/5159–5



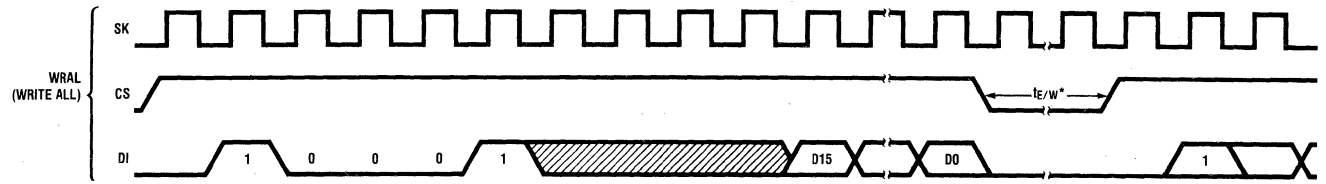
TL/D/5159–6

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

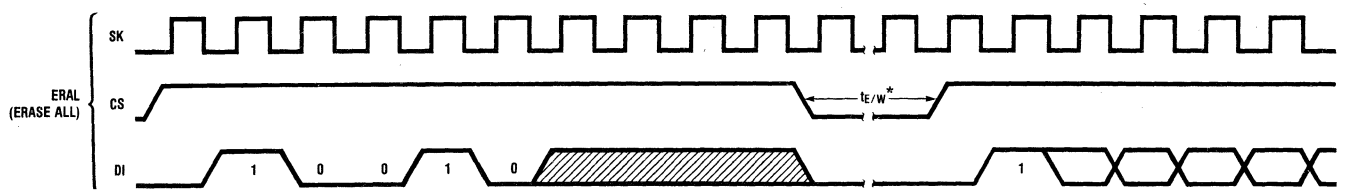
FIGURE 5. Instruction Timing



TL/D/5159–7



TL/D/5159–8



TL/D/5159–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

FIGURE 5. Instruction Timing (Continued)

National Semiconductor

NMC9307E 256-Bit Serial Electrically Erasable Programmable Memory

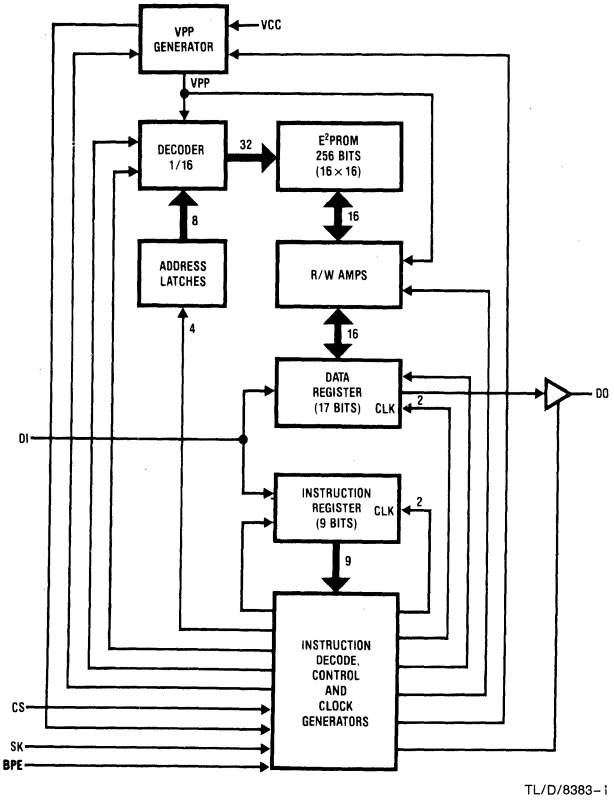
General Description

The NMC9307E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Bulk programming instructions (chip erase, chip write) can be enabled or disabled by the user for enhanced data protection. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9307E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

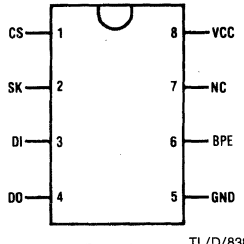
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Bulk programming enable/disable for enhanced data protection

Block and Connection Diagrams



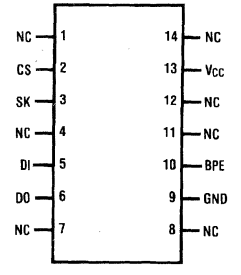
TL/D/8383–1

Dual-In-Line Package



Top View TL/D/8383–10

SO Package



Top View TL/D/8383–2

Order Number NMC9307NE, 9307
See NS Package N08E, M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
BPE	Bulk Program Enable
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9307E	−40°C to +85°C
Ambient Storage Temperature	−65°C to +125°C
Lead Temp. (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics $-40°C \leq TA \leq +85°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	$V_{CC} = 5.5V$, $C_S = 1$			10	mA
Standby Current (I_{CC2})	$V_{CC} = 5.5V$, $C_S = 0$			3	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		$V_{CC} + 1$	V
Output Voltage Levels					
V_{OL}	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	$I_{OH} = -400\ \mu A$	2.4			V
Input Leakage Current	$V_{IN} = 0$ to 5.5V				
PINS 1, 2, 3				±10	μA
PIN 6				±50	μA
Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$			2	μs
t_{PD0}	$V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g. if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (tcs) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	BPE	Comments
READ	1	10XX	A3A2A1A0		X	Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15–D0	X	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0		X	Erase register A3A2A1A0
EWEN	1	0011	XXXX		X	Erase/write enable
EWDS	1	0000	XXXX		X	Erase/write disable
ERAL (Note 5)	1	0010	XXXX		V_{IH}/OPEN	Erase all registers
WRAL (Note 5)	1	0001	XXXX	D15–D0	V_{IH}/OPEN	Write all registers

NMC9307E has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address of 1 of 16, 16-bit registers.

Functional Description

The NMC9307E is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical '1' before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes he DO pin is in TRI-STATE®, eliminating bus contention.

The bulk programming instructions (ERAL, WRAL) are enabled or disabled by the PBE pin. The BPE pin at V_{IH} enables execution of these instructions. The BPE pin at V_{IL} causes these instructions to be ignored. If the BPE pin is not connected, it is pulled up to V_{CC} by an on-chip pull-up and the bulk programming instructions are enabled. Execution of the EWEN, EWDS, READ and byte programming instructions (ERASE, WRITE) are independent of the state of the BPE pin.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by the low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction. The chip erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

CHIP WRITE (Note 4)

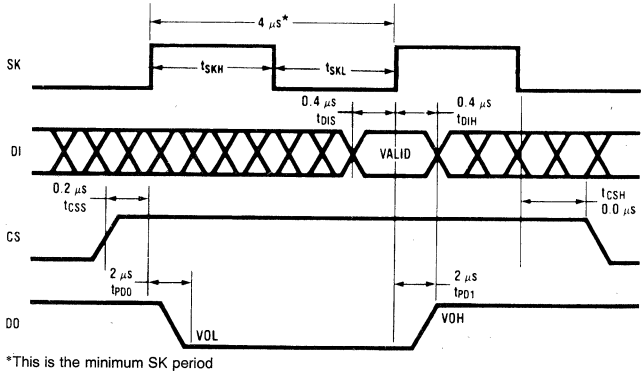
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction. The chip write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e. start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Note 5: The ERAL and WRAL instructions are ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

Timing Diagrams

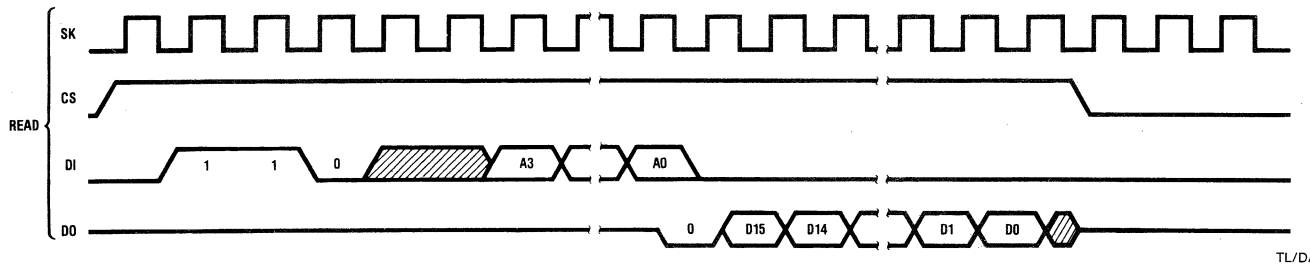
Synchronous Data Timing



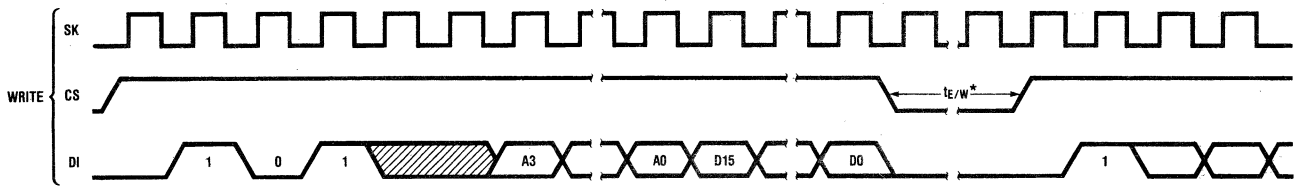
*This is the minimum SK period

TL/D/8383–3

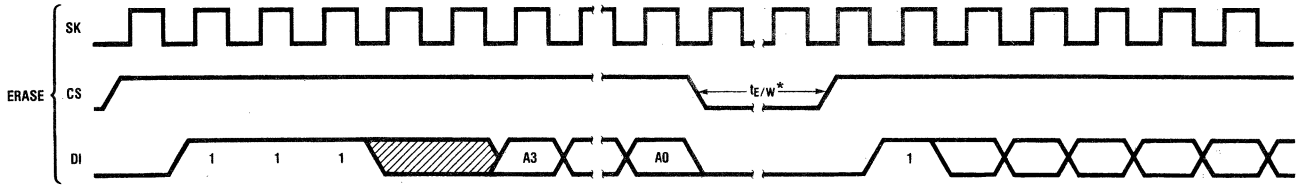
Instruction Timing



TL/D/8383–4



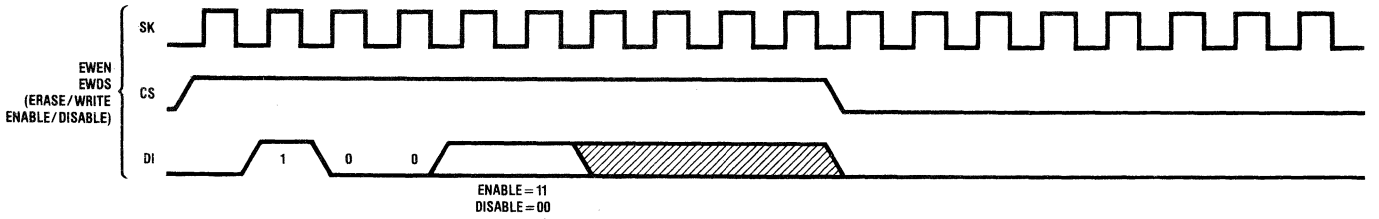
TL/D/8383–5



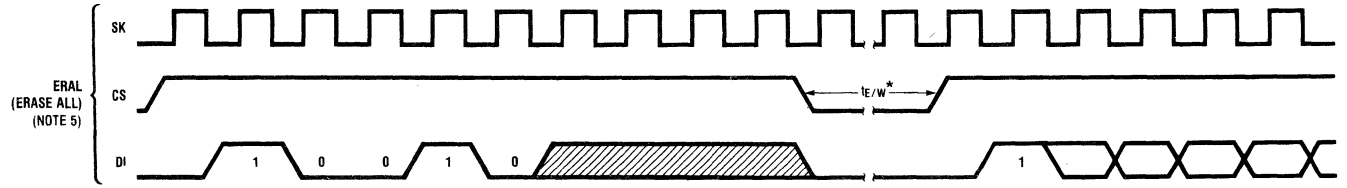
TL/D/8383–6

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

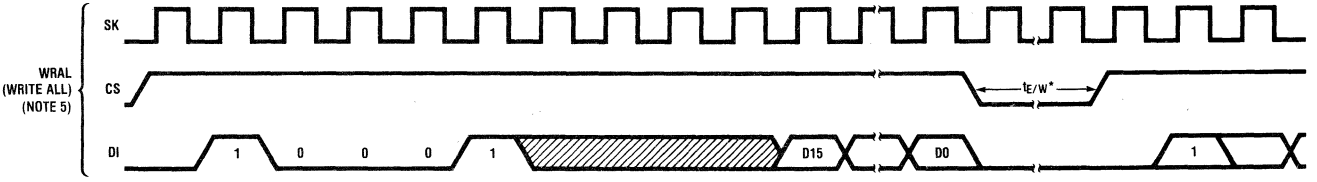
Instruction Timing (Continued)



TL/D/8383–7



TL/D/8383–8



TL/D/8383–9

*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 5: The ERAL and WRAL instructions are ignored if the BPE pin is at VIL, i.e. the array data is not changed.

National Semiconductor

NMC9345/COP495 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

General Description

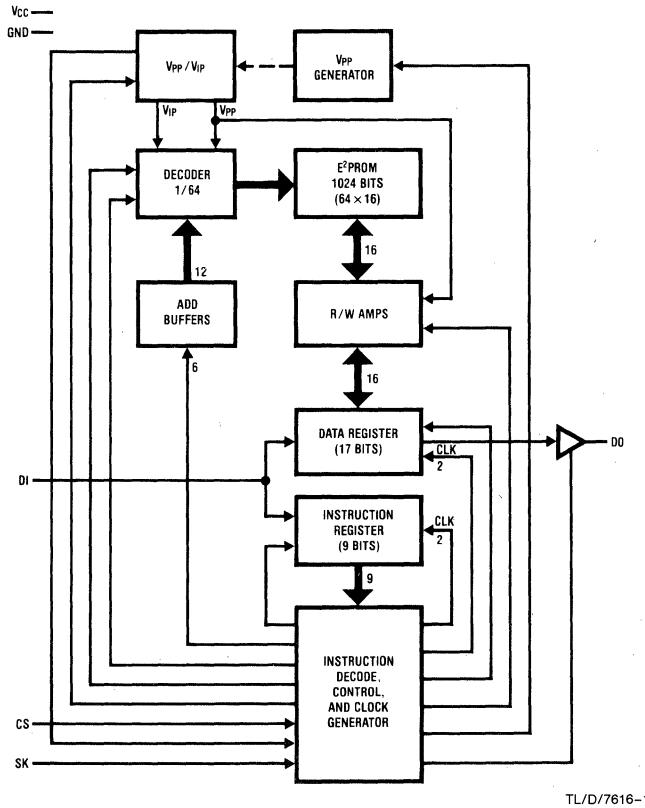
The NMC9345/COP495 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9345 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 × 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

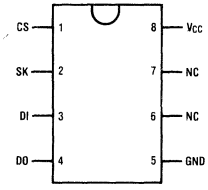
Block and Connection Diagrams

Serial E²PROM



TL/D/7616–1

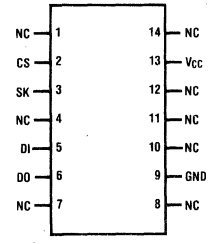
Dual-In-Line Package



TL/D/7616–2

Top View

SO Package



TL/D/7616–10

Top View

Order Number NMC9345N, NMC9345
See NS Package N08E or M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Voltage Relative to GND	+6V to −0.3V	Ambient Storage Temperature	−65°C to +125°C
Ambient Operating Temperature	0°C to +70°C	Lead Temp. (Soldering, 10 seconds)	300°C

DC and AC Electrical Characteristics NMC9345: $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1 $V_{CC} = 5.5V$		12 12	mA mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+1$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
	SK Frequency		0	250	kHz
t_{SKH}	SK High Time		2		μs
t_{SKL}	SK Low Time		1		μs
	Inputs				
t_{CSS}	CS		0.2		μS
t_{CSH}			0		μS
t_{DIS}	DI		0.4		μS
t_{DIH}			0.4		μS
	Output	$C_L = 100$ pF			
$t_{pd}1$	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μS
$t_{pd}0$		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$		2	μS
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time (Note 3)		1		μS
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μS
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μS

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g. if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1μS (t_{CS}) between consecutive instruction cycles.

Functional Description

The NMC9345/COP495 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the read/busy status of the chip.

The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

Functional Description (Continued)

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

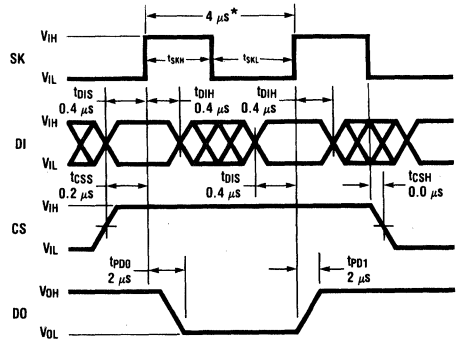
IC INSTRUCTION SET FOR NMC9345/COP495

Instruction	SB	Opcode	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/Write enable
EWDS	1	00	00xxxx		Erase/Write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15-D0	Write all registers

NMC9345/COP495 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Timing Diagrams

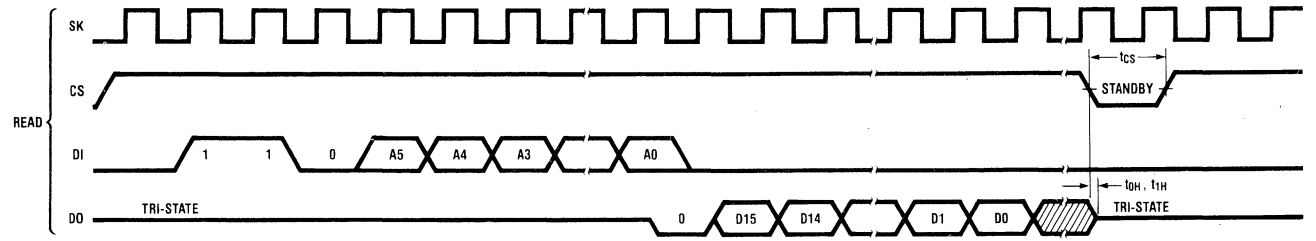
Synchronous Data Timing



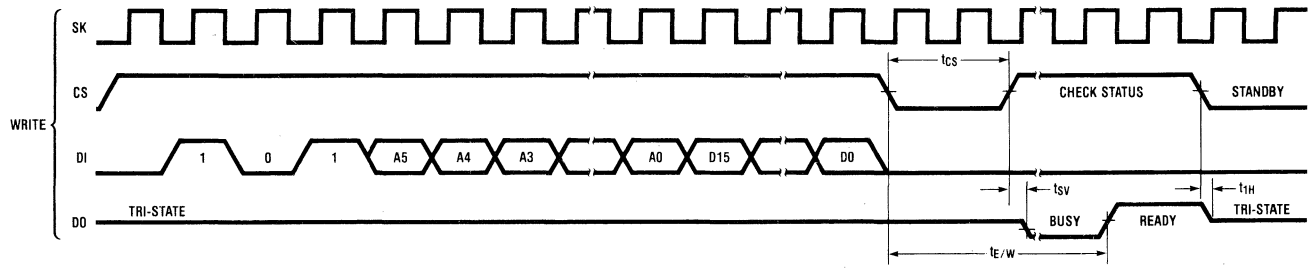
*This is the minimum SK period.

TL/D/7616–3

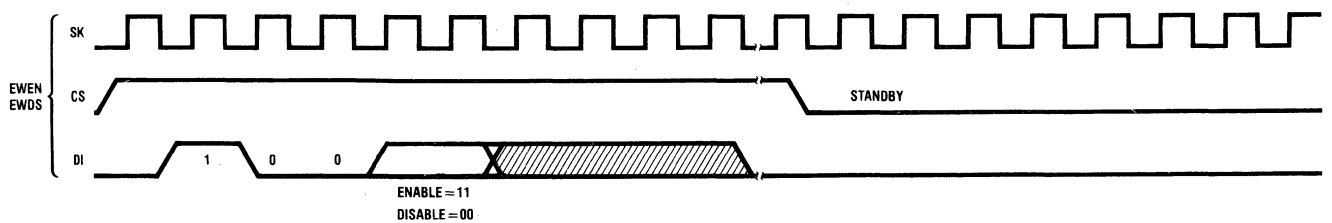
Instruction Timing



TL/D/7616–4

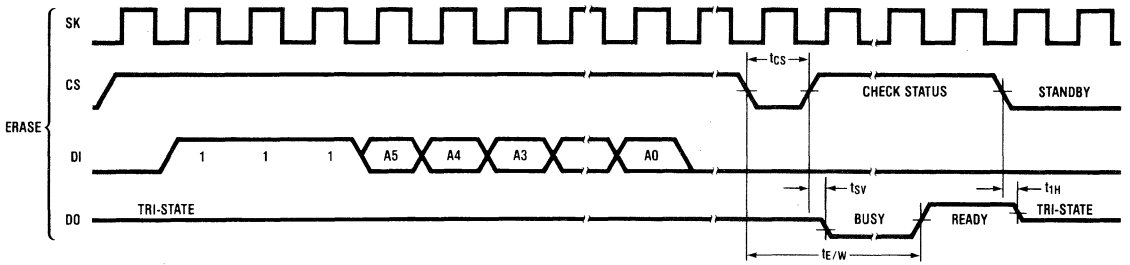


TL/D/7616–5

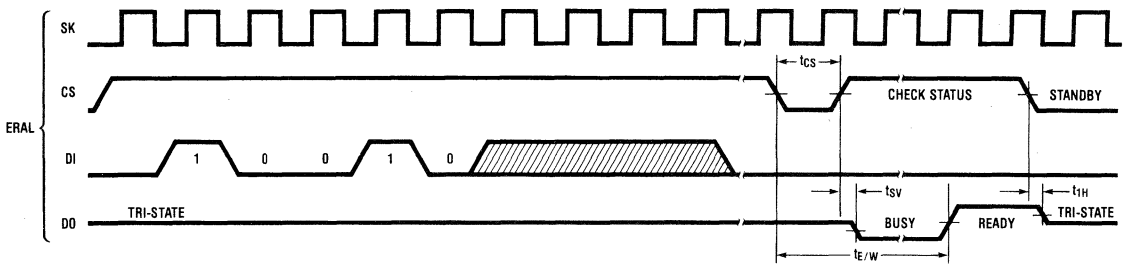


TL/D/7616–6

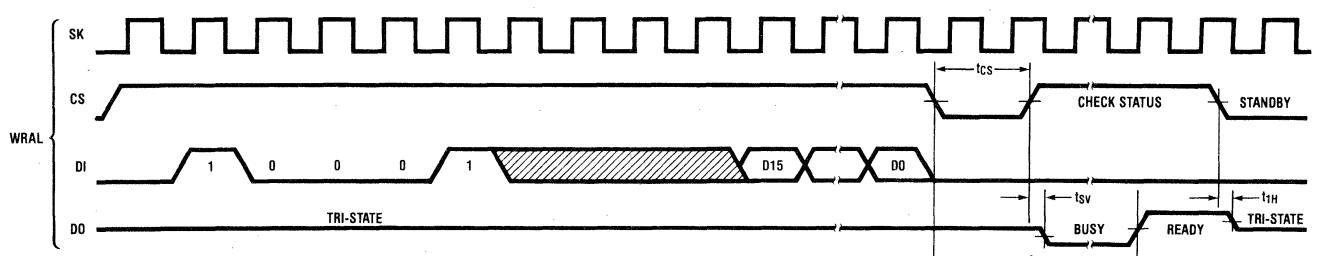
Instruction Timing



TL/D/7616–7



TL/D/7616–8



TL/D/7616–9

National Semiconductor

NMC9346/COP495 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

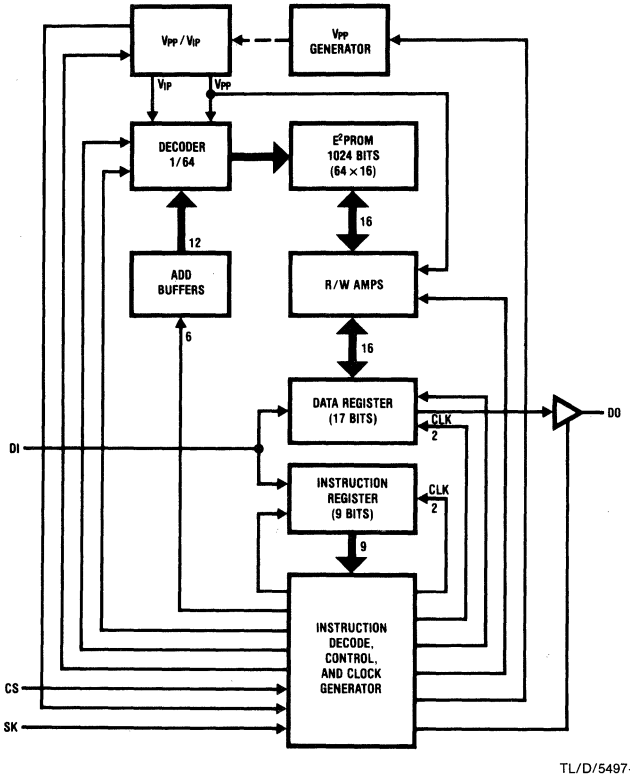
General Description

The NMC9346/COP495 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346/COP495 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

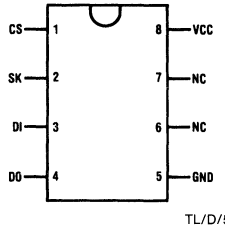
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



TL/D/5497–1

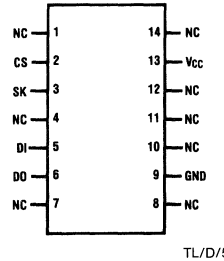
Dual-In-Line Package



TL/D/5497–6

Top View

SO Package



TL/D/5497–2

Top View

Order Number NMC9346N, NMC9346NE
See NS Package N08E, M14B

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Voltage Relative to GND	+6V to −0.3V	Ambient Storage Temp.	−65°C to +125°C
Ambient Operating Temperature	0°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1 $V_{CC} = 5.5V$		12 12	mA mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+1$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
	SK Frequency		0	250	kHz
t_{SKH}	SK High Time (Note 2)		1		μs
t_{SKL}	SK Low Time (Note 2)		1		μs
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L = 100$ pF			
$t_{pd}1$	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
$t_{pd}0$		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 4 μs. e.g., if $t_{SKL} = 1$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9346/COP495

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9346/COP495 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346/COP495 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E^2PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

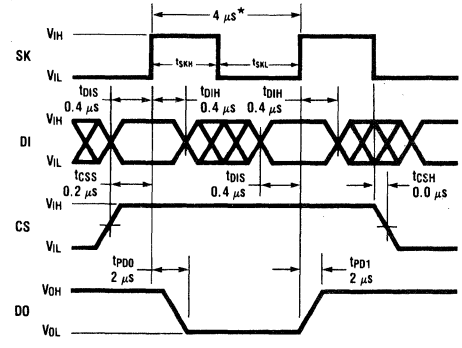
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

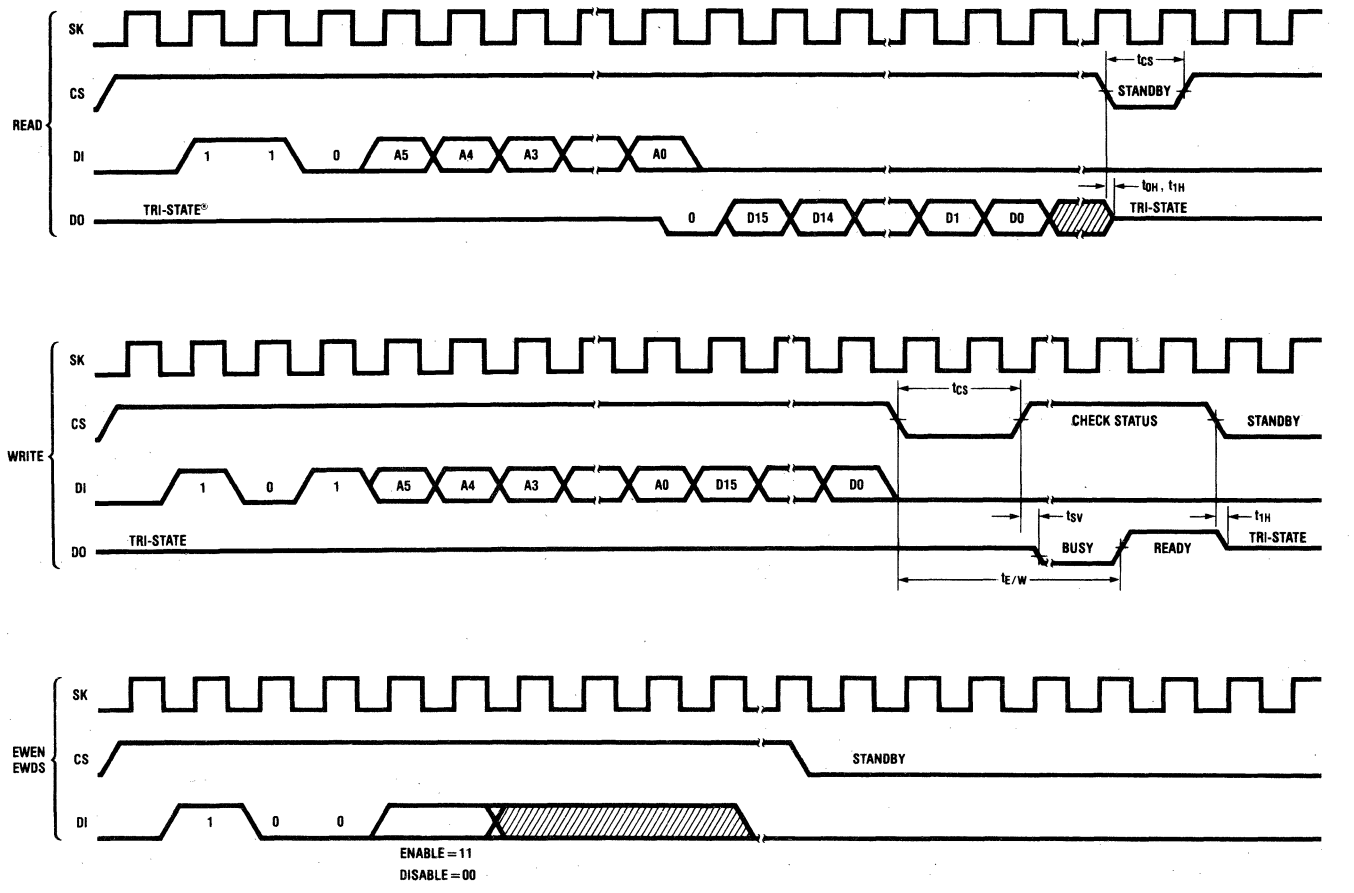
Synchronous Data Timing



TL/D/5497–3

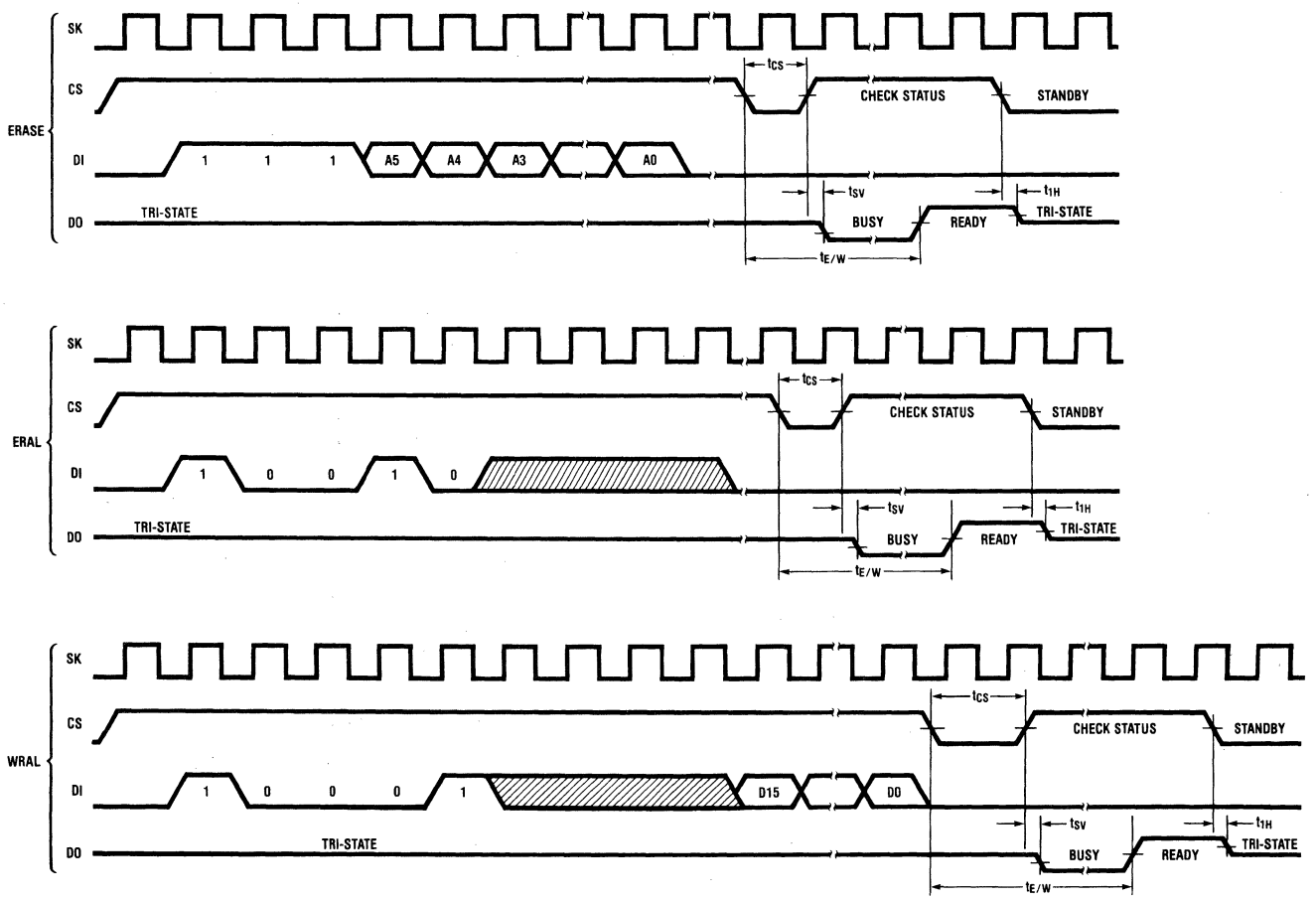
*This is the minimum SK period.

Instruction Timing



TL/D/5497–4

Instruction Timing



TL/D/5497–5

National Semiconductor

NMC9346E/COP395 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

General Description

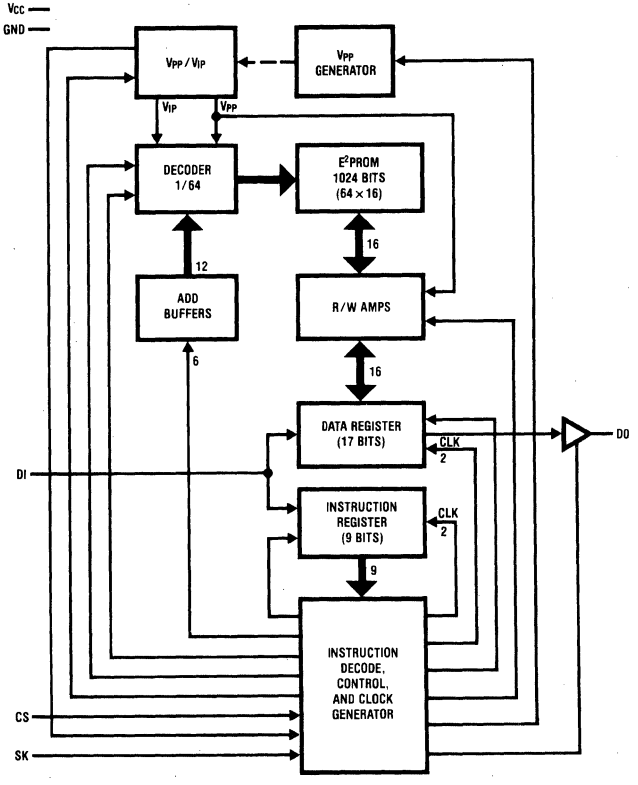
The NMC9346E/COP395 is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346E/COP395 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

- Low cost
- Single supply read/write/erase operations (5V ±10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

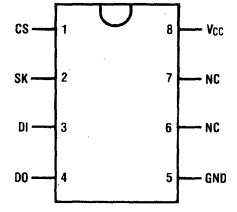
Block and Connection Diagrams

Serial E²PROM



TL/D/5582–1

Dual-In-Line Package



TL/D/5582–2

Top View

Order Number NMC9346NE
See NS Package N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Voltage Relative to GND	+6V to −0.3V	Ambient Storage Temperature with Data Retention	−65°C to +125°C
Ambient Operating Temperature NMC9346E/COP395	−40°C to +85°C	Lead Temp. (Soldering, 10 seconds)	300°C

DC and AC Electrical Characteristics

$-40°C - T_A \leq 85°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current P/E Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1 $V_{CC} = 5.5V$		12 12	mA mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC} + 1$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
	SK Frequency SK Duty Cycle		0 25	250 75	kHz %
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L = 100$ pF			
$t_{pd}1$	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
$t_{PD}0$		$V_{IL} = 0.45V$, $V_{IH} = 2.4V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Instruction Set for NMC9346E/COP395

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read Register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write Register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase Register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/Write Enable
EWDS	1	00	00xxxx		Erase/Write Disable
ERAL	1	00	10xxxx		Erase All Registers

NMC9346E/COP395 has 6 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346E/COP395 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. The output data changes during the high states of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE

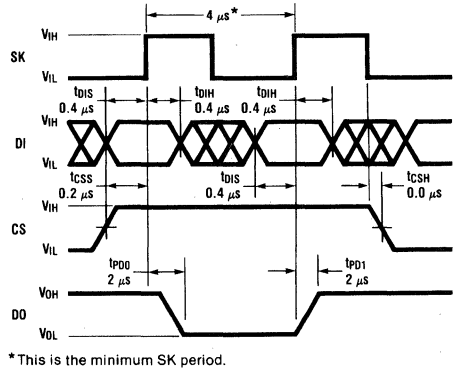
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is indentical to the erase cycle except for the different op code.

Note 1: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

Synchronous Data Timing



* This is the minimum SK period.

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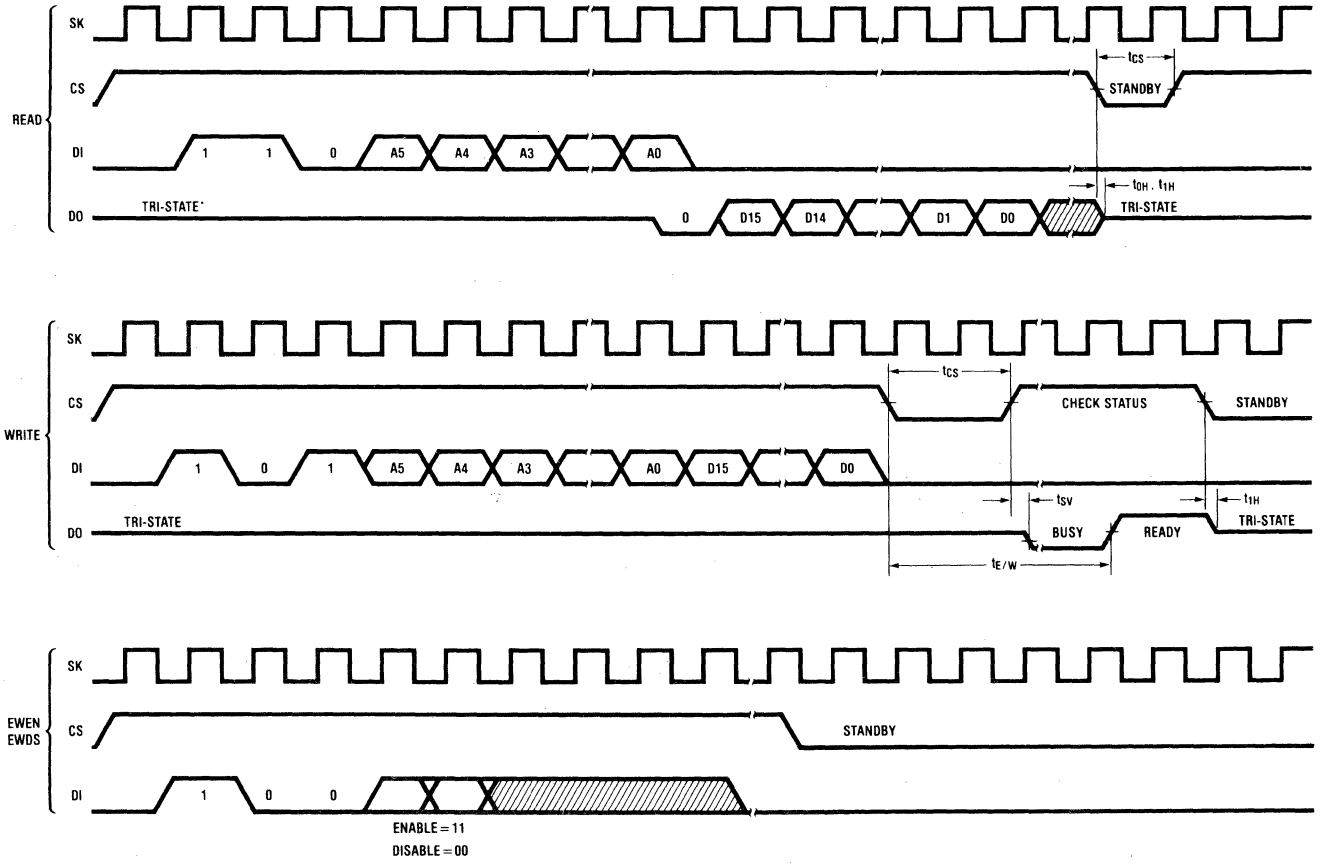
Instruction Timing



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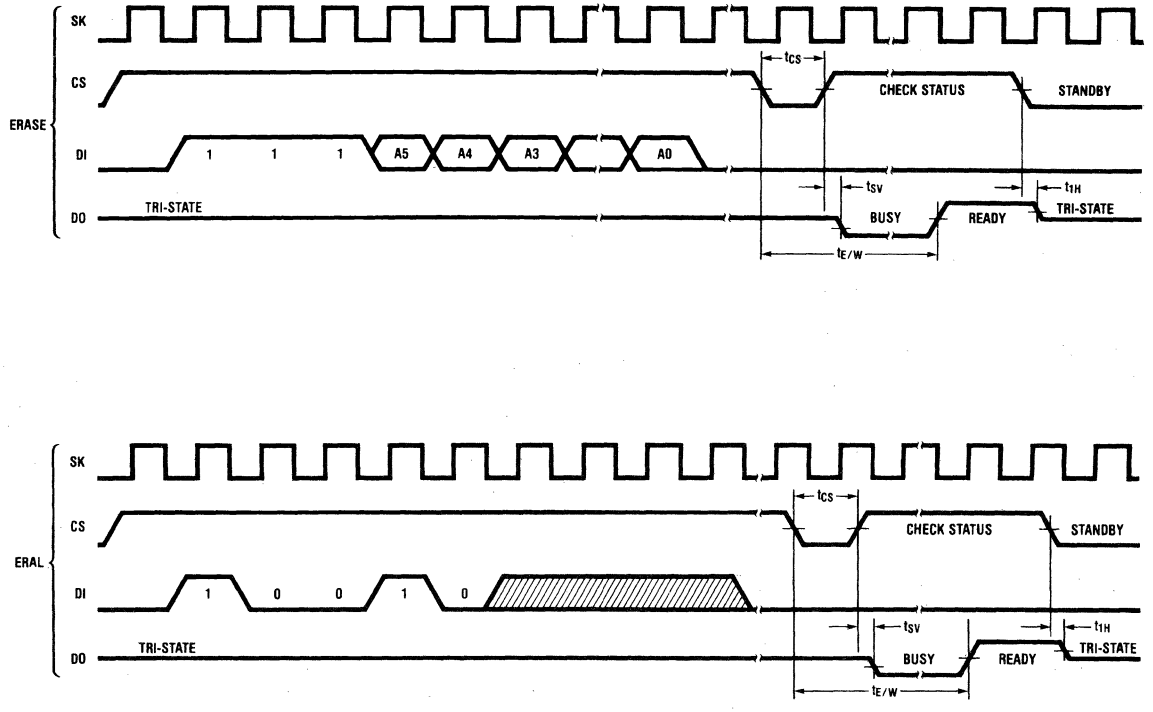
Timing Diagram (Continued)

Instruction Timing



TL/D/5582–5

National Semiconductor

PRELIMINARY

NMC9802 2048-Bit Parallel (256 x 8) Electrically Erasable Programmable ROM

General Description

The NMC9802 is a 2048 bit electrically erasable programmable read-only memory (E^2PROM) organized as 256 words by eight bits. Fabricated using National's double poly silicon gate n-channel technology, the device utilizes a novel memory architecture that results in the memory operating as a non-volatile register file. A single bidirectional eight bit data port is used for transmitting the address, data and status information. Both address and input data are latched into onboard registers elminating the need to hold them valid during the long erase/write operation. In addition, all the erase/write control logic is incorporated on chip completely freeing the microprocessor once the erase/write cycle has been initiated. Both a $\overline{BUSY}$ signal and status register are available to facilitate easy interface in a wide variety of microprocessor based systems.

The in-system erase/write capability of the NMC9802 make it suitable for a wide variety of applications requiring a small amount of alterable non-volatile storage. Any byte can be erased and written without affecting the rest of memory. Alternatively, the entire memory can be erased.

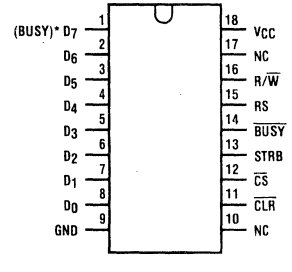
The NMC9802 utilizes fully static circuitry and is completely TTL compatible in the read and erase/write modes. The device has an on-chip voltage generator eliminating the need for any high voltage pulses or power supplies. The single +5V power supply is all that is required for any operation. The NMC9802 can be a direct replacement for Synertek's SY2802E.

Features

- Reliable E^2 floating gate technology
- Microprocessor compatible architecture
- On-chip address/data latches
- Single cycle byte erase/write capability
- Fully TTL compatible
- Endurance 1 x 10^4 write cycles (Min.)
- Single +5V operation
- Erase/write specifications guaranteed 0–70°C
- On-chip ERASE/WRITE timing and control
- Both $\overline{BUSY}$ signal and status register
- Data retention: 10 years (Min.)

Connection and Block Diagrams

Dual In-Line Package



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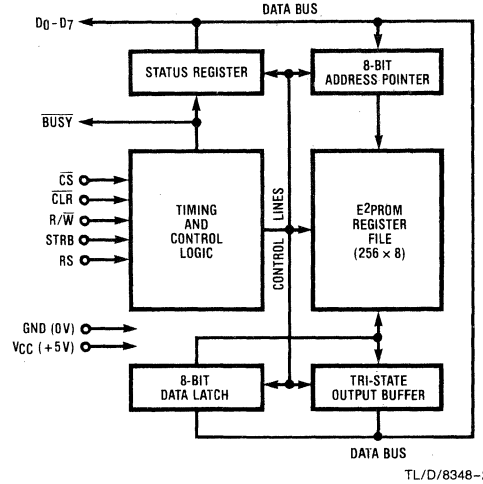
Top View

*SEE STATUS REGISTER

See Ordering Information



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Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°
Storage Temperature	−65°C to 125°
Voltage on Any Pin with Respect to Ground	−0.5V to +7V

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±10% (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{CC}	V_{CC} Current	Outputs Open			80	mA
V_{IL}	Input LOW Voltage		−0.3		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{CC} +1	V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA	2.4			V

Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±10% (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CYC}	Cycle Time		350			ns
t_{CS}	Chip Select Access Time				120	ns
t_{SA}	Valid Data from Strobe				450	ns
t_{LZ}	Select to Output LOW Z		10			ns
t_{HZ}	Select to Output HIGH Z	(Note 2)	10		75	ns
t_{AR}	Access Time from RS or R/$\overline{W}$				200	ns
t_{WS}	Write Setup Time		120			ns
t_{WH}	Write Hold Time		0			ns
t_{DS}	Data Setup Time		60			ns
t_{DH}	Data Hold Time		0			ns
t_{SH}	Strobe Pulse Width High		85			ns
t_{SL}	Strobe Pulse Width Low		120			ns
t_{BA}	$\overline{BUSY}$ Active From Strobe		30		300	ns
t_{BLW}	$\overline{BUSY}$ Low Pulse Width (WRITE)				25	ms
t_{SCY}	Busy HIGH to Cycle Start		0			ns
t_{BLC}	$\overline{BUSY}$ Low Pulse Width (CLEAR)				12.5	ms

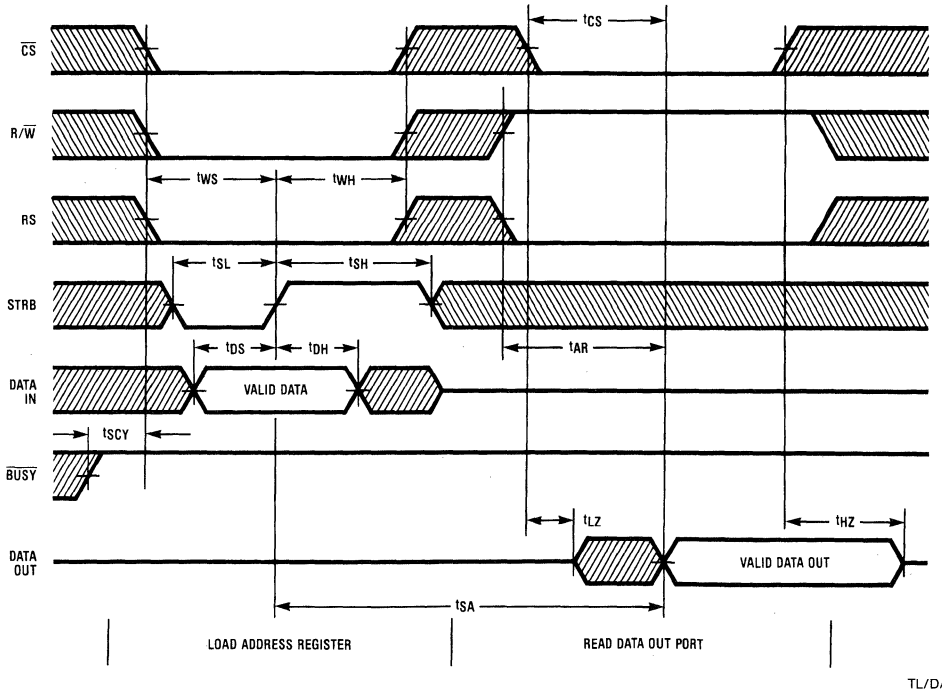
Note 1: A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Note 2: Current goes through 50% change from I_{OH} (MAX) or I_{OL} (MAX).

Note 3: Pins 11 and 16 must be held below V_{CC} during power up.

Timing Diagrams

Data Fetch ($\overline{CLR}$ = HIGH, $\overline{BUSY}$ = HIGH) (Note 1)



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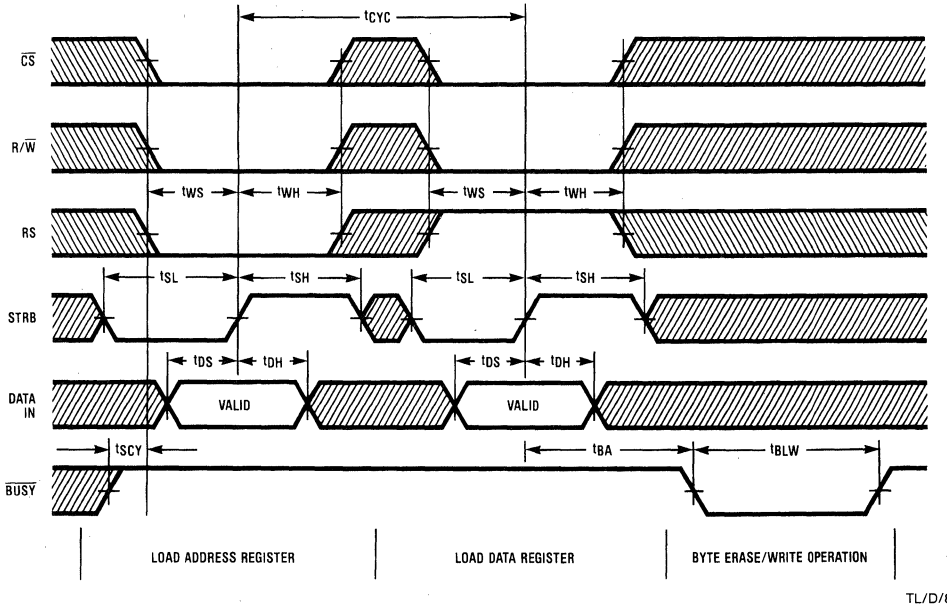
Data Store ($\overline{CLR}$ = HIGH) (Note 1)



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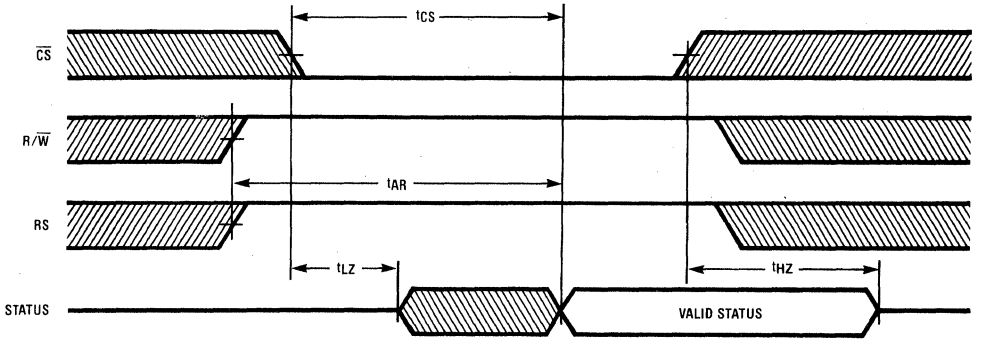
Timing Diagram (Continued)

Read Status Register ($\overline{CLR}$ = HIGH, $\overline{BUSY}$ = Don't Care) (Note 1)



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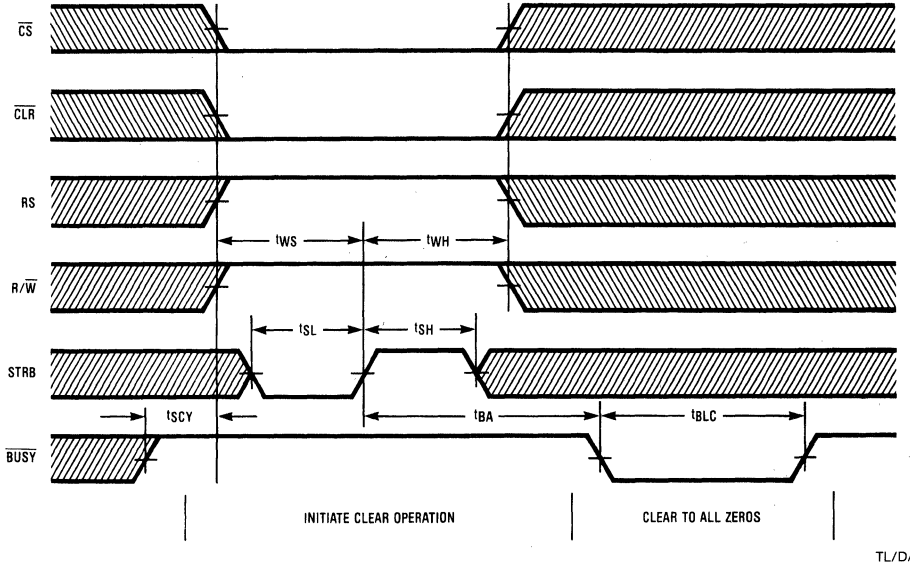
Clear Cycle (Data = Don't Care) (Note 1)



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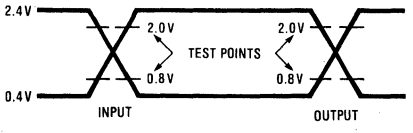
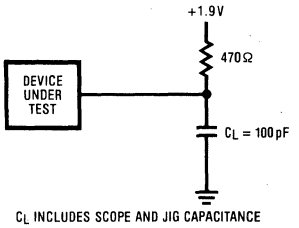
A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5ns.

TL/D/8348–7

A.C. Testing Load Circuit



C_L INCLUDES SCOPE AND JIG CAPACITANCE

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DEVICE OPERATION

The NMC9802 has seven modes of operation as listed in Table I. All the modes of the NMC9802 involve reading or loading registers. This eliminates any timing problems associated with interfacing to a wide variety of microprocessors and microcomputers.

DATA FETCH

Reading the NMC9802 involves two cycles as shown in the timing diagram. First the address pointer is loaded and then the data from the selected location can be read. Both the address and data are transmitted through the same eight bit port.

DATA STORE

Writing the device requires two cycles as shown in the timing diagram. As with the read operation, first the address pointer must be loaded. Loading the data input register then initiates the byte erase/write operation and the microprocessor is free to do other tasks. The timing interface with the microprocessor is handled with both a $\overline{BUSY}$ signal and a status register. Loading the data in register causes the open-drain $\overline{BUSY}$ signal to be set LOW and bit seven (pin 1) of the status register to be set HIGH for the duration of the byte erase/write operation. Once complete, these two signals are reset to their inactive states. Note that it is not necessary for the microprocessor to erase the location prior to writing new data. This is automatically done by the memory itself.

Once the erase/write operation has been initiated, the NMC9802 doesn't allow access to address pointer, data input register or data output drivers.

READ STATUS REGISTER

To facilitate interfacing the NMC9802 in microprocessor based systems, a status register has been provided that is accessible at all times including during the erase/write operation. This allows a polling routine to be used to determine if the NMC9802 is busy. If bit 7 (pin 1) is a logic "1", the device is in the erase/write operation and if it is a logic "0" it is available for normal operation.

CLEAR CYCLE

The NMC9802 can be block cleared to all zeros as shown in the timing diagram. As with the data store operation, this cycle only needs to be initiated, all the timing is controlled internally. On initiating the clear cycle, $\overline{BUSY}$ and bit 7 (pin 1) are set active and remain so until the operation is complete. During the clear cycle, only the status register is accessible.

ENDURANCE CHARACTERISTIC

A characteristic of E^2PROMs is that the number of erase/write cycles is limited. The NMC9802 has been designed to meet applications where up to 1×10^4 erase/write cycles per word are required. The erase/write cycling is completely word independent. Adjacent words are not affected during the erase/write cycling.

TABLE I. Mode Selection $V_{CC} = +5V$ (Note 1)

Mode	Pin						Data Input/ Outputs (0-7)
	$\overline{CS}$ (12)	R/$\overline{W}$ (16)	RS (15)	STRB (13)	$\overline{BUSY}$ (14)	$\overline{CLR}$ (11)	
Read Register File	0	1	0	X	1	1	Data Out
Read Status Register	0	1	1	X	X	1	Data Out
Write Address Pointer	0	0	0	↗	1	1	Data In
Write Data-In Latch	0	0	1	↗	⊓	1	Data In
Deselected	1	X	X	X	X	X	High Z
Write Inhibited	X	X	0	0	1	X	X
Block Clear	0	1	1	↗	⊓	0	High Z

X = DON'T CARE

↗ = POSITIVE TRANSITION

⊓ = NEGATIVE PULSE

Ordering Information

Order Number	Select Access Time	Cycle Time (Min)	Supply Current (Max)	Package Type
NMC9802J	120 ns	350	70 mA	Cerdip
NMC9802N	120 ns	350	70 mA	Plastic

National Semiconductor

PRELIMINARY

NMC9816A 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9816A is a fast 5V-only E²PROM which offers many desired features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9816A include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy doing erase-write; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9816A is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9816A sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9816A also features $\overline{\text{DATA}}$ Polling, which enables the E²PROM to signal the processor that a write operation is complete without requiring the use of any external hardware.

Improved data protection during V_{CC} power up/down transitions is provided by an on-chip V_{CC} sensing circuit which disables the initiation of all 5V-only programmable modes when V_{CC} is less than 4 volts.

The NMC9816A's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment.

An optional high voltage chip erase feature is provided for quick erasure of the memory data pattern in a single 9 msec Chip Erase Cycle.

The density, and level of integrated control, make the NMC9816A suitable for users requiring minimum hardware overhead, high systems performance, minimal board space and design ease. Designing with and using the NMC9816A is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1, 2,* and *3* for the NMC9816A block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply
- Self-timed byte-write with auto erase
- On-chip address and data latches
- On-chip power up/down protection
- Two line output control
- TRI-STATE® outputs
- $\overline{\text{Data}}$ polling verification
- High voltage chip erase
- Fast byte-writing
  - Write cycle (2 ms typical)
  - E/W cycle (4 ms typical)
- Very fast access time
  - NMC9816A-20—200 ns
  - NMC9816A-25—250 ns
  - NMC9816A-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

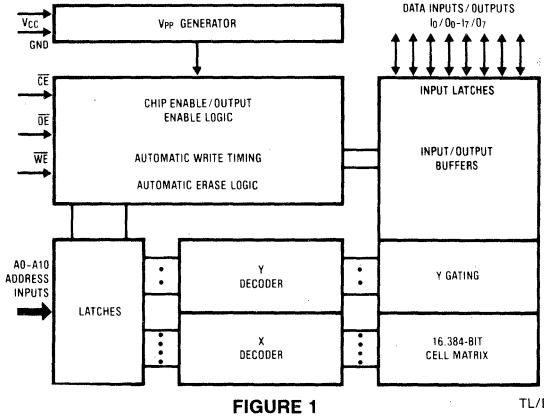

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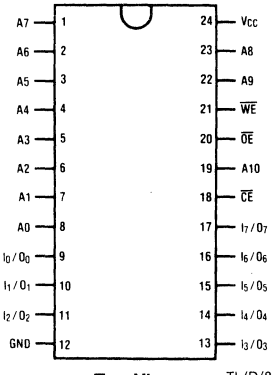
FIGURE 1

Pin Names

A0–A10	Addresses	O_0–O_7	Data Outputs
$\overline{\text{CE}}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{\text{OE}}$	Output Enable	$\overline{\text{WE}}$	Write Enable

Dual-In-Line Package



Top View

TL/D/8451-2

FIGURE 2

Order Number NMC9816A-20, NMC9816A-25 or NMC9816A-35
See NS Package Number J24A or N24A

Absolute Maximum Ratings

Temperature Under Bias	
NMC9816A	−10°C to +80°C
NMC9816AE	−50°C to +95°C
NMC9816AM	−65°C to +135°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	
NMC9816A	0°C to +70°C
NMC9816AE	−40°C to +85°C
NMC9816AM	−55°C to +125°C
V_{CC} Power Supply (Notes 2 and 3)	
NMC9816A	5V ±5%
NMC9816AE	5V ±10%
NMC9816AM	5V ±10%

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Electrical Characteristics T_A for NMC9816A = 0°C to +70°C, V_{CC} = 5V ±5% (Note 7)

Symbol	Parameter		Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION							
I_{LI}	Input Leakage Current	NMC9816A	GND to V_{CC}			10	μA
		NMC9816AE				10	
		NMC9816AM				10	
I_{LO}	Output Leakage Current	NMC9816A	GND to V_{CC}			10	μA
		NMC9816AE				10	
		NMC9816AM				10	
I_{CCA}	V_{CC} Current (Active)	NMC9816A	$\overline{CE} = \overline{OE} = V_{IL}$		40	80	mA
		NMC9816AE			40	100	
		NMC9816AM			40	100	
I_{CCS}	V_{CC} Current (Standby)	NMC9816A	$\overline{CE} = V_{IH}$		12	25	mA
		NMC9816AE			12	30	
		NMC9816AM			12	30	
V_{IL}	Input Low Voltage			−0.1		0.8	V
V_{IH}	Input High Voltage	NMC9816A		2.0		V_{CC} + 1	V
		NMC9816AE		2.2		V_{CC} + 1	
		NMC9816AM		2.2		V_{CC} + 1	
V_{OL}	Output Low Voltage		I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage		I_{OH} = −400 μA	2.4			V
WRITE OPERATION							
I_{CCW}	V_{CC} Current (Write)	NMC9816A			40	80	mA
		NMC9816AE			40	100	
		NMC9816AM			40	100	
V_{LKO}	V_{CC} Level for Write Lockout			4.0			V
HIGH VOLTAGE CHIP ERASE							
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode			12		22	V

Capacitance T_A = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			10	pF

AC Test Conditions

Output Load	1 TTL gate and $C_L = 100$ pF	Timing Measurement Reference Level	
Input Pulse Levels	0.45V to 2.4V	Input	1V and 2V
		Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	NMC9816A-20			NMC9816A-25			NMC9816A-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time		20			ns
t_{WP} (Note 6)	Write Pulse Width		150			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DL}	Data Latch Time		50			ns
t_{WC}	Byte-Write Cycle Time			4	10	ms
t_{OES}	Output Enable Setup Time		10			ns
t_{OEH}	Output Enable Hold Time		10			ns

High Voltage Chip Erase AC Electrical Characteristics (Note 5)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{CS}	$\overline{CE}$ Set-Up Time	$\overline{WE} = 6V$	10			ns
t_{OS}	Output Enable Set-Up Time	$\overline{WE} = 6V$	10			ns
t_{OH}	Output Enable Hold Time	$\overline{WE} = 6V$	1			μs
t_{WR}	Write Recovery Time	$\overline{WE} = 6V$	1			μs
t_{WP}	Chip Erase Pulse Width	$\overline{WE} = V_{ER}$	9		15	ms

Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before $V_{CC} = 4V$. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC} falls before 4V.

Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

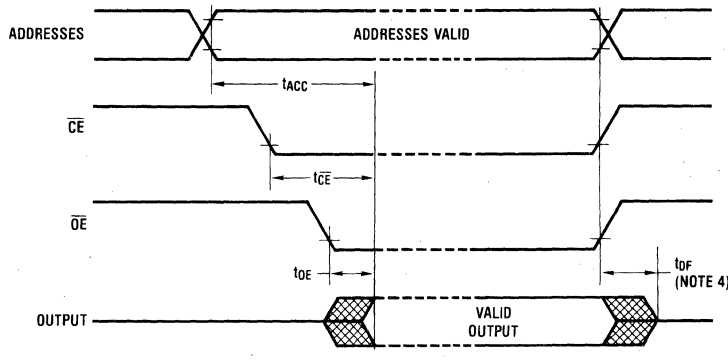
Note 5: Low voltage V_{CC} sense circuit does not inhibit the high voltage Chip Erase feature.

Note 6: $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.

Note 7: T_A for NMC9816AE = $-40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, T_A for NMC9816AM = $-55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$.

Switching Time Waveforms

Read



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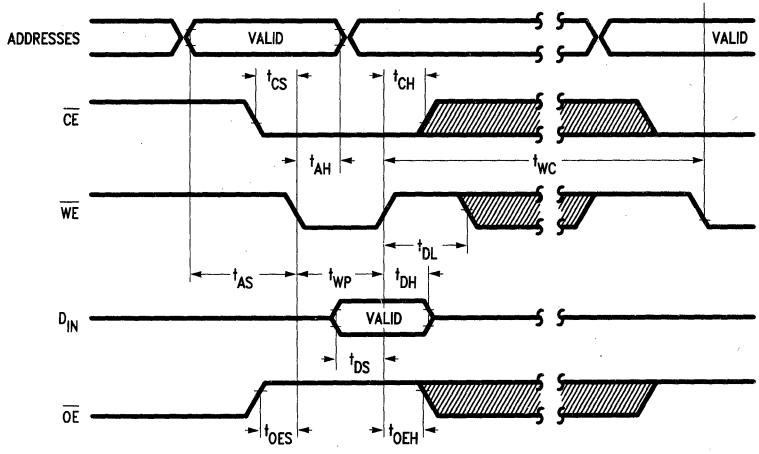
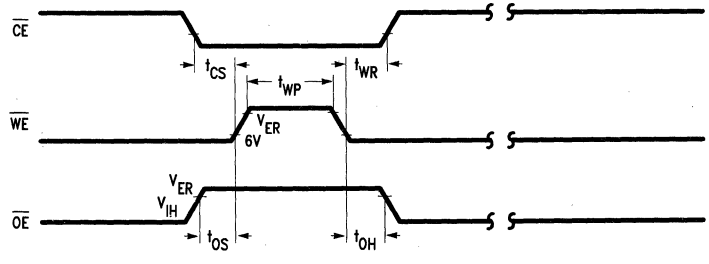
Write



TL/D/8451–4

Chip Erase Cycle



DATA IN = DON'T CARE

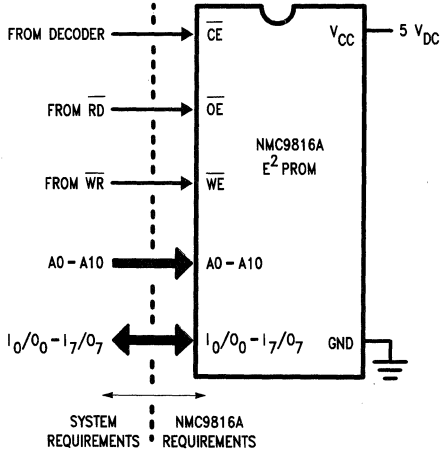
TL/D/8451–6

Device Operation

The NMC9816A has 6 modes of user operation which are detailed in Table I. All modes are designed to enhance the NMC9816A's functionality to the user and provide total microprocessor compatibility.

TABLE I. V_{CC} = 5V

Mode / Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I_0/O_0-I_7/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	Hi-Z
Write	V_{IL}	V_{IH}	⊔	D_{IN}
Busy	V_{IH}	X	X	High-Z
	X	V_{IH}	X	High-Z
Data Polling	V_{IL}	V_{IL}	X	$I_7/O_7 = \overline{D_{IN}}$
Chip Erase	V_{IL}	V_{ER}	V_{ER}	X



TL/D/8451–5

FIGURE 3. Simple NMC9816A Interface Requirements

WRITE MODE

The NMC9816A is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9816A automatically latches the address, data, and control signals and starts the write cycle. During the write cycle V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

$\overline{DATA}$ POLLING

The NMC9816A features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA PROTECTION ON V_{CC} POWER UP AND POWER DOWN

An erase/write of a byte in the NMC9816A is accomplished with input signals $\overline{CE}$, $\overline{WE}$ = V_{IL}. During system (V_{CC}) power up and power down, this condition may be present as V_{CC} ramps up to or down from its steady state value of 5V. To prevent the possibility of an inadvertant byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if V_{CC} falls below 4V (VLKO).

OPTIONAL HIGH VOLTAGE CHIP ERASE CYCLE

All data can be changed to "1" or erase state in one 10 ms cycle by raising $\overline{OE}$ to 12–22V and bringing $\overline{WE}$ to 12–22V for t_{WP} msec.

READ MODE

One aspect of the NMC9816A's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMS and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9816A can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9816A has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9816A's. This mode occurs when the device is deselected ($\overline{CE}$ = V_{IH}). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9816A is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9816A is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9816A in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9816A. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9816A.

The NMC9816A is cost effective for lower density E²PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9816A reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

Device Operation (Continued)

The NMC9816A will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9816A. Several NMC9816A's can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

WRITE TIME CHARACTERISTICS

The NMC9816A's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. The 2816 has a write time specification of 9 ms. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9816A's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. The NMC9816A maximum specification is 10 ms.

WRITE PROTECTION

There are three features that protect the nonvolatile data from an inadvertant write.

- Noise Protection — A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense — When V_{CC} is below approximately 4V all 5V-only write functions are inhibited.
- Write Inhibit — Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power-on and power-off (V_{CC}).

National Semiconductor

PRELIMINARY

NMC9817 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9817 is a fast 5V-only E²PROM which offers many desired features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9817 include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy during erase-write; 'Ready' line indicator to indicate status of chip to the microprocessor; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9817 is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9817 sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the NMC9817 signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

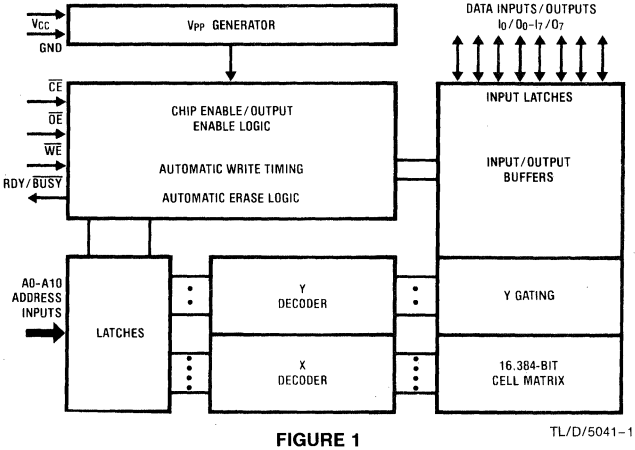
The NMC9817's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817's open-drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E²PROM memory.

The density, and level of integrated control, make the NMC9817 suitabie for users requiring minimum hardware overhead, high system performance, minimal board space and design ease. Designing with and using the NMC9817 is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1*, *2* and *3* for the NMC9817 block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply (eliminates an external 21V V_{PP})
- Self-timed byte-write with auto erase
- No external capacitor or pulse shaping circuits
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- Fast byte-writing
  Write cycle (2 ms typical)
  E/W cycle (4 ms typical)
- Very fast access times
  NMC9817-20—200 ns
  NMC9817-25—250 ns
  NMC9817-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams



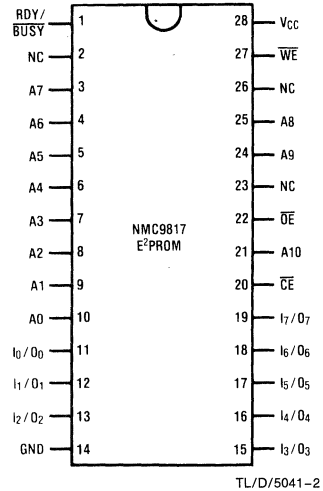
TL/D/5041-1

FIGURE 1

Pin Names

A0–A10	Addresses	I_0–I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy (Open-Drain Output)
$\overline{OE}$	Output Enable	NC	No Connect
O_0–O_7	Data Outputs		

Dual-In-Line Package



TL/D/5041-2

Top View
FIGURE 2

Order Number NMC9817J-20, NMC9817J-25 or NMC9817-35
See NS Package Number J28A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	0°C to +70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ±5%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics $T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
I_{LI}	Input Leakage Current	$V_{IN} = 5.25V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$			10	μA
I_{CCA}	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		40	80	mA
I_{CCS}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$		12	25	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
WRITE OPERATION						
I_{CCW}	V_{CC} Current (Write)	$RDY/\overline{BUSY} = V_{OL}$		40	80	mA

Capacitance $T_A = 25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$			10	pF

AC Test Conditions

Output Load	1 TTL gate and $C_L = 100$ pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC9817-20			NMC9817-25			NMC9817-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time (Note 5)		20			ns
t_{WP}	Write Pulse Width		100			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{WR}	Byte-Write Cycle Time			4	10	ms

Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before application of V_{CC}. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC}.

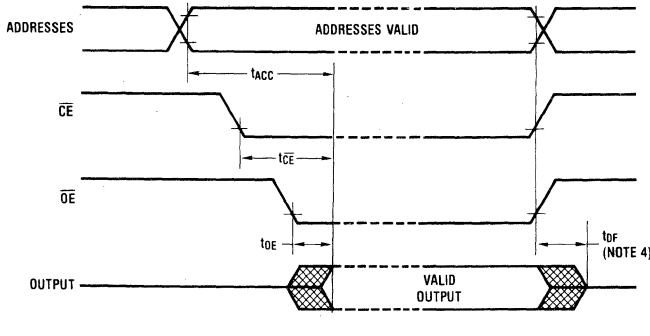
Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Note 5: T_{CS} = 35 ns on −25 and −35 devices.

Switching Time Waveforms

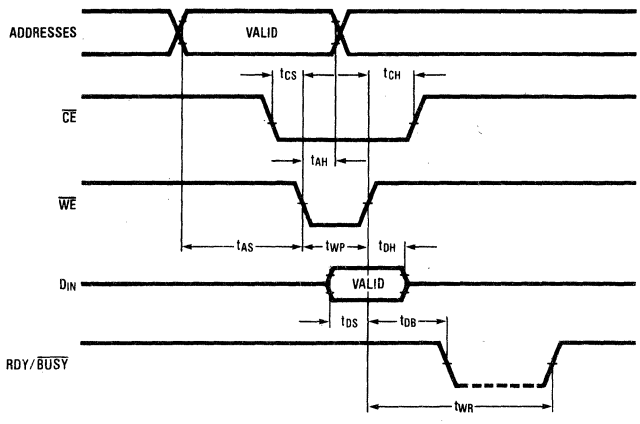
Read



TL/D/5041–3

Switching Time Waveforms (Continued)

Write



TL/D/5041–4

Device Operation

The NMC9817 has 4 modes of user operation which are detailed in Table 1. All modes are designed to enhance the NMC9817's functionality to the user and provide total microprocessor compatibility.

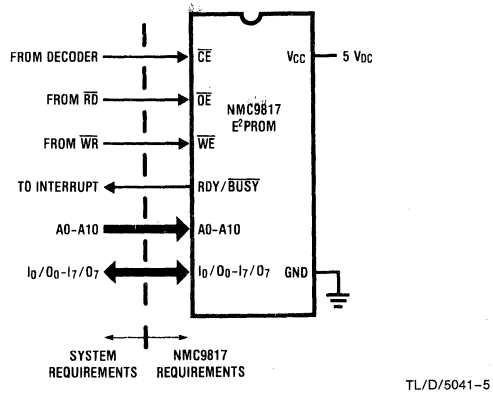
TABLE I. V_{CC} = 5V

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I_0/O_0-I_7/O_7$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z	Hi-Z
Write	V_{IL}	V_{IH}	⊓	D_{IN}	V_{OL}
Busy	X	X	X	Hi-Z	V_{OL}

WRITE MODE

The NMC9817 is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9817 automatically latches the address, data, and control signals and starts the write cycle. Concurrently, the 'Ready' line goes low, indicating that the NMC9817 is busy and that it can be deselected to allow the processor to perform other tasks. The Ready/$\overline{Busy}$ signal is an open-drain output. During the write, a high V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

As a precaution against spurious signals which may cause an inadvertant write cycle, or interfere with a valid signal, it is recommended that a pullup resistor be used on the $\overline{WE}$ pin, pin 27 (see *Figure 4*).



TL/D/5041–5

FIGURE 3. Simple NMC9817 Interface Requirements

Device Operation (Continued)

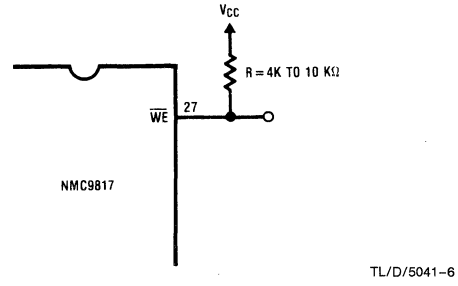


FIGURE 4. Pullup R on $\overline{WE}$

READ MODE

One aspect of the NMC9817's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMS and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9817 can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9817 has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9817s. This mode occurs when the device is deselected ($\overline{CE} = V_{IH}$). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9817 is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9817 is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9817 in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9817. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9817.

The NMC9817 is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9817 reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

The NMC9817 will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9817. Several NMC9817s can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

WRITE TIME CHARACTERISTICS

The NMC9817's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9817's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. This cycle is the time that 'Ready' is held low by the device. The NMC9817 maximum specification is 10 ms.

National Semiconductor

PRELIMINARY

NMC9817A 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9817A is a fast 5V-only E²PROM which offers many desired features ideally suited for efficiency and ease in system design. The features on the NMC9817A include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and free the microprocessor while the chip is busy during erase-write; 'Ready' line indicator to indicate status of chip to the microprocessor; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9817A is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

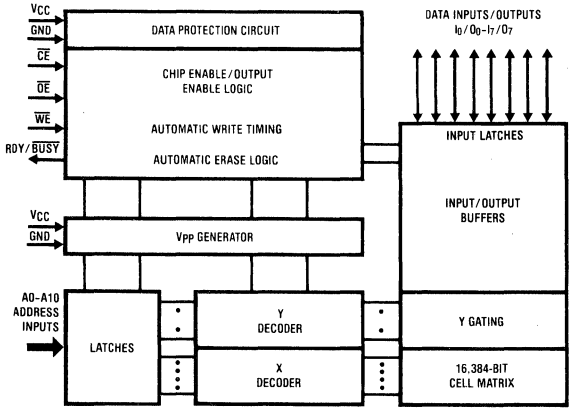
The NMC9817A sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device is self-timed which leaves the processor free to perform other tasks until the NMC9817A signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9817A also features $\overline{\text{DATA}}$ Polling, which enables the E²PROM to signal the processor that a write operation is complete without requiring the use of any external hardware. Improved data protection during V_{CC} power up/down transitions is provided by an on-chip V_{CC} sensing circuit which disables the initiation of all 5V-only programming modes when V_{CC} is less than 4 volts. See *Figures 1, 2* and *3* for the NMC9817A block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply
- Self-timed byte-write with auto erase
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- $\overline{\text{Data}}$ polling verification
- High voltage chip erase
- Fast byte-writing
  - Write cycle (2 ms typical)
  - E/W cycle (4 ms typical)
- Very fast access times
  - NMC9817A-20—200 ns
  - NMC9817A-25—250 ns
  - NMC9817A-35—350 ns
- On chip power up/down protection
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams



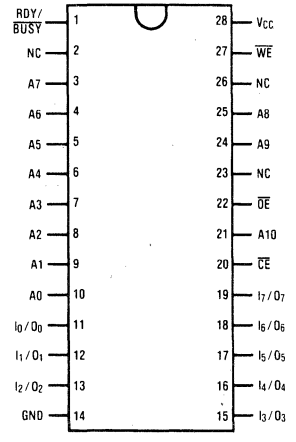
TL/D/8370-1

FIGURE 1

Pin Names

A0-A10	Addresses	I_0-I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy (Open-Drain Output)
$\overline{OE}$	Output Enable	NC	No Connect
O_0-O_7	Data Outputs	$\overline{WE}$	Write Enable

Dual-In-Line Package



Top View

TL/D/8370-2

FIGURE 2

Order Number NMC9817AN-20, NMC9817AN-25 or NMC9817AN-35
See NS Package J28A or N28B

Absolute Maximum Ratings

Temperature Under Bias	
NMC9817A	−10°C to +80°C
NMC9817AE	−50°C to +95°C
NMC9817AM	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	
NMC9817A	0°C to +70°C
NMC9817AE	−40°C to +85°C
NMC9817AM	−55°C to +125°C
V_{CC} Power Supply (Notes 2 and 3)	
NMC9817A	5V ±5%
NMC9817AE & NMC9817AM	5V ±10%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics T_A for NMC9817A = 0°C to +70°C, V_{CC} = 5V ±5% (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
I_{LI}	Input Leakage Current NMC9817A NMC9817AE NMC9817AM	GND to V_{CC}			10 10 10	μA
I_{LO}	Output Leakage Current NMC9817A NMC9817AE NMC9817AM	GND to V_{CC}			10 10 10	μA
I_{CCA}	V_{CC} Current (Active) NMC9817A NMC9817AE NMC9817AM	$\overline{OE} = \overline{CE} = V_{IL}$		40 40 40	80 100 100	mA
I_{CCS}	V_{CC} Current (Standby) NMC9817A NMC9817AE NMC9817AM	$\overline{CE} = V_{IH}$		12 12 12	25 30 30	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage NMC9817A NMC9817AE NMC9817AM		2.0 2.2 2.2		V_{CC} + 1 V_{CC} + 1 V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4			V
WRITE OPERATION						
I_{CCW}	V_{CC} Current (Write) NMC9817A NMC9817AE NMC9817AM	RDY/$\overline{BUSY}$ = V_{OL}		40 40 40	80 100 100	mA
V_{LKO}	V_{CC} Level For Write Lockout		4.0			V
HIGH VOLTAGE CHIP ERASE						
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode		12		22	V

Capacitance T_A = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			10	pF

AC Test Conditions

Output Load	1 TTL gate and C_L = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	NMC9817A-20			NMC9817A-25			NMC9817A-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time		20			ns
t_{WP} (Note 6)	Write Pulse Width		150			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{WC}	Byte-Write Cycle Time			4	10	ms
t_{DL}	Data latch time		50			ns
to_{ES}	Output Enable Set-up Time		10			ns
to_{EH}	Ouput Enable Hold Time		10			ns

High Voltage Chip Erase AC Electrical Characteristics (Note 5)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{CS}	$\overline{CE}$ Set-up Time	$\overline{WE} = 6V$	10			ns
t_{OS}	Output Enable Set-up Time	$\overline{WE} = 6V$	10			ns
t_{OH}	Output Enable Hold Time	$\overline{WE} = 6V$	1			μs
t_{WR}	Write Recovery Time	$\overline{WE} = 6V$	1			μs
t_{WP}	Chip Erase Pulse Width	$\overline{WE} = V_{ER}$	9		15	ms

Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before $V_{CC} = 4V$. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC} falls below 4V.

Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

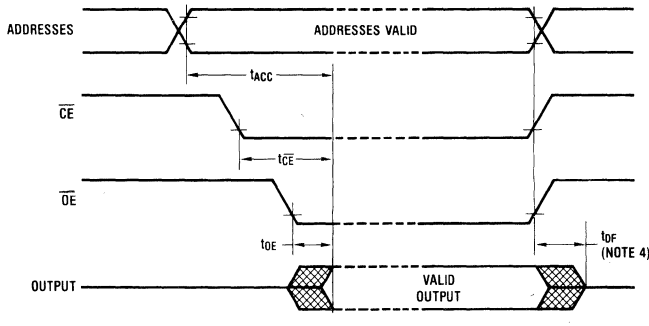
Note 5: Low voltage V_{CC} sense circuit does not inhibit the high voltage chip erase feature.

Note 6: $\overline{WE}$ is noise protected. Less than 20 ns write pulse will not activate a write cycle.

Note 7: NMC9817AE = $-40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, NMC9817AM = $-55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$.

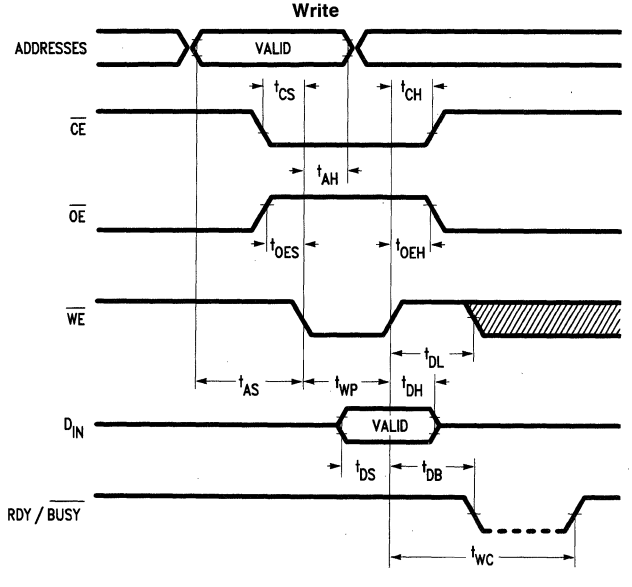
Switching Time Waveforms

Read



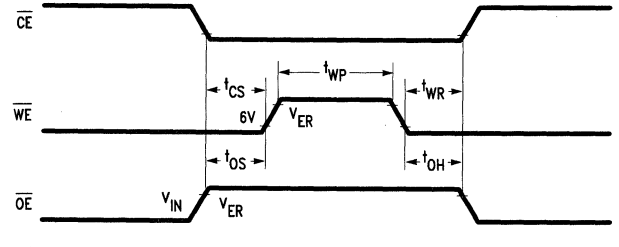
TL/D/8370–3

Write



TL/D/8370–4

Chip Erase Cycle



TL/D/8370–6

Data In = Don't Care

Device Operation

The NMC9817A has 6 modes of user operation which are detailed in Table I. All modes are designed to enhance the NMC9817A's functionality to the user and provide total microprocessor compatibility.

TABLE I. V_{CC} = 5V

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I_0/O_0 \cong I_7/O_7$	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z	Hi-Z
Write	V_{IL}	V_{IH}	⊓	D_{IN}	V_{OL}
Busy	V_{IH}	X	X	Hi-Z	V_{OL}
	X	V_{IH}	X	Hi-Z	V_{OL}
Data Polling	V_{IL}	V_{IL}	X	$I_7/O_7 = \overline{D_{IN}}$	V_{OL}
Chip Erase	V_{IL}	V_{ER}	V_{ER}	X	V_{OL}

WRITE MODE

The NMC9817A is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMs and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9817A automatically latches the address, data, and control signals and starts the write cycle. Concurrently, the 'Ready' line goes low, indicating that the NMC9817A is busy and that it can be deselected to allow the processor to perform other tasks. The Ready/$\overline{Busy}$ signal is an open-drain output. During the write, cycle V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

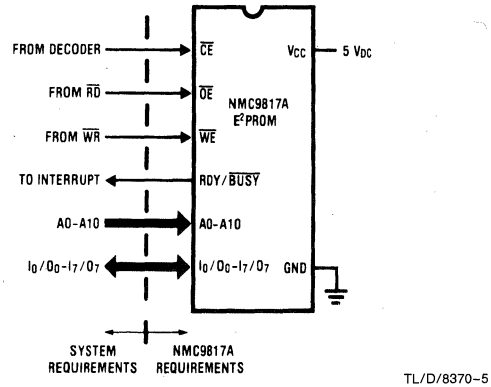


FIGURE 3. Simple NMC9817A Interface Requirements

Device Operation (Continued)

$\overline{\text{DATA}}$ POLLING

The NMC9817A also features $\overline{\text{DATA}}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{\text{DATA}}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

ON-CHIP DATA PROTECTION ON V_{CC} POWER UP AND POWER DOWN

An erase/write of a byte in the NMC9817A is accomplished with input signals $\overline{CE}$, $\overline{WE}$ = V_{IL}. During system (V_{CC}) power up and power down, this condition may be present as V_{CC} ramps up to or down from its steady state value of 5 volts. To prevent the possibility of an inadvertent byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if V_{CC} falls below 4 volts (V_{LKO}).

WRITE TIME CHARACTERISTICS

The NMC9817A's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. The 2816 has a write time specification of 9 ms. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9817A's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. This cycle is the time that 'Ready' is held low by the device. The NMC9817A maximum specification is 10 ms.

WRITE PROTECTION

There are three features that protect the nonvolatile data from an inadvertent write.

- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—When V_{CC} is below approximately 4 volts all 5V-only write functions are inhibited.
- Write Inhibit—Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power-on and power-off (V_{CC}).

OPTIONAL HIGH VOLTAGE CHIP ERASE CYCLE

All data can be changed to "1" or erase state in one 10 ms cycle by raising $\overline{OE}$ to 12-22V and bringing $\overline{WE}$ to 12-22V for t_{WP} msec.

READ MODE

One aspect of the NMC9817A's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMs and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9817A can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9817A has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9817As. This mode occurs when the device is deselected ($\overline{CE}$ = V_{IH}). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9817A is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9817A is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9817A in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9817A. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9817A.

The NMC9817A is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9817A reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

The NMC9817A will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9817A. Several NMC9817As can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

The NMC9817A's very fast read access times make it compatible with high performance microprocessor applications. It uses proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817A's open-drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E^2PROM memory.

The density, and level of integrated control, make the NMC9817A suitable for users requiring minimum hardware overhead, high system performance, minimal board space and design ease. An optional high voltage chip erase feature is provided for quick erasure of the memory data pattern in a single 9 msec Chip Erase cycle. Designing with and using the NMC9817A is extremely cost effective as the required high voltage and interfacing hardware required for other E^2PROM devices has been eliminated by 5V-only operation and on-chip latches.

National Semiconductor

PRELIMINARY

microCMOS

NMC98C64
8k x 8 CMOS Electrically Erasable PROM

General Description

The NMC98C64 is a 5V only CMOS E²PROM with desirable ease of use features that facilitate in-circuit programming using a single suppy and TTL level signals. In addition, the NMC98C64 is compatible with present high density EPROMs which require high voltage programming and UV erasing. The NMC98C64 is a state-of-the-art product that uses the advanced microCMOS stepper based technology. The process is an enhancement of the proven XMOS™ process for reliable, non-volatile data storage.

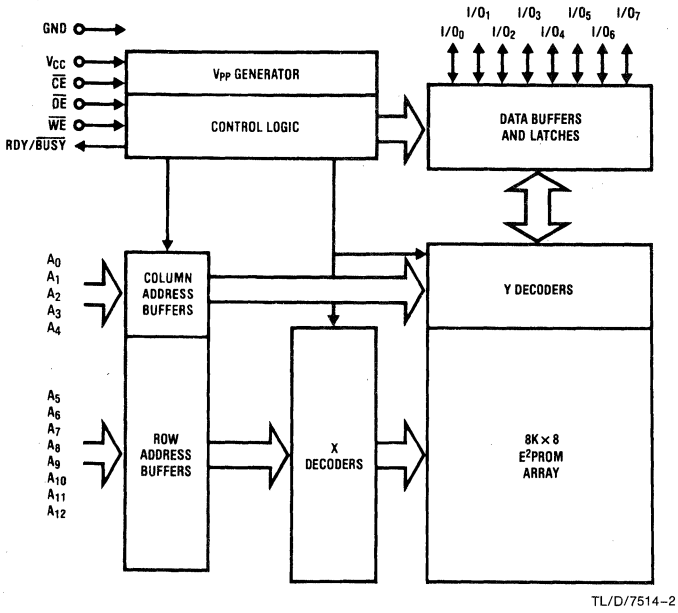
Writing data in NMC98C64 is analagous to writing to a SRAM. A 200 ns min TTL pulse to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out. Address and data latches free the system bus for the duration of the write. Ready/$\overline{Busy}$ facilitates service by providing an interrupt to the controller; an open drain output facilitates "wire or" connection in larger systems.

A 32-byte page write allows data to be accepted at an effective rate of 300 μs/page or 2.6 seconds to write an entire chip.

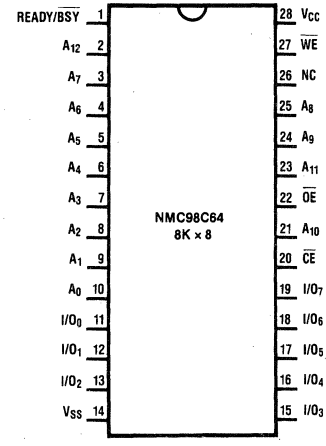
Features

- Single 5-V power supply
- Low CMOS power
  - — Active, 10 mA typical
  - — Standby, 100 μA typical
  - — Quiescent, 100 μA typical
- Simple byte write and page write
  - — On-chip address and data latches
  - — Self-timed cycle, auto erase before write
  - — Page write up to 32 bytes per page
  - — Ready/$\overline{Busy}$ open drain status output and $\overline{DATA}$ polling verification
  - — Write protection
- Fast write time
  - — Byte or page write, 10 ms max
  - — Entire chip write in 2.6 seconds
  - — Page data load, 300 μs typical
- Fast access time: 200 ns/250 ns/350 ns
- CMOS and TTL compatible level inputs/outputs

Block and Connection Diagrams



TL/D/7514–2



TL/D/7514–1

Order Number NMC98C64
See NS Package J28A

A_0–A_4	Column Addresses
A_5–A_{12}	Row Addresses
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BUSY}$	Device Ready/Busy
NC	No Connect

TABLE I. Operation Modes (V_{CC} = 5V + 10%)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/00-I/07	RDY/$\overline{BUSY}$	Power
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z	Active/Quiescent
Write Single Byte or 1st Byte in a Page	V_{IL}	V_{IH}	⊓	D_{IN}	High Z → Vol	Write
Write Subsequent Bytes in a Page	V_{IL}	X	⊓	D_{IN}	Vol	Write
Busy	V_{IH} X	X V_{IH}	X X	Hi-Z Hi-Z	Vol Vol	Write Write
$\overline{DATA}$ Polling	V_{IL}	V_{IL}	V_{IH}	$I/O_7 = \overline{D_{IN}}$	Vol/Hi-Z	—
Standby	V_{IH}	X	X	High Z	High Z	Standby
Write Inhibit	X X	V_{IL} X	X V_{IH}	– –	High Z High Z	– –

Device Operation

The NMC98C64 is organized as 256 rows of 32 bytes (256 × 32 × 8). Address inputs A5 through A12 are decoded to select one of the 256 rows (pages) of storage locations. A0 through A4 are decoded to select one of the 32 bytes within the selected row. The device has various modes of user operation (detailed in Table I). All input/output levels are TTL compatible. "X" denotes don't care situation to TTL levels.

READ MODE

The read cycle of the NMC98C64 is similar to that of an EPROM or a static RAM. A low $\overline{CE}$ and a low $\overline{OE}$ enable the output buffers. The Ready/$\overline{Busy}$ pin is at high impedance state during the read cycle.

WRITE MODE

Writing data to the NMC98C64 is similar to writing to a static RAM. There are two ways to load data into data latches of the device in a write cycle, which once initiated will automatically continue to the completion in 10 ms.

A byte write is accomplished by applying to the device a data load cycle in which a low going pulse to $\overline{WE}$ with $\overline{CE}$ low and $\overline{OE}$ high is required. The data presented at I/O pins are written into the location selected by a byte address.

A page write allows a page of data to be written into E²PROM in a single write cycle. Instead of one data load cycle, up to 32 (page size) data load cycles can be applied to the device in 300 μs after the first data load cycle. The address (A5-A12), which is presented to address pins before the first $\overline{WE}$ pulse going low, is latched in the device and used as the page address for the rest of the cycle. The byte addresses (A0–A4) may be put in any order providing they are on the same page. Through page writes the entire memory can be written (or rewritten) in 2.6 seconds.

The data load cycle can be finished by bringing $\overline{CE}$ or $\overline{WE}$ high and keeping that through the rest of the data load time.

The row address (page address) is latched internally after first data load cycle.

The WRITE mode status can be interrogated in two ways:

- Ready/$\overline{Busy}$ — The Ready/$\overline{Busy}$ pin (pin 1) goes to a logic low level indicating that the NMC98C64 is in a write cycle. When Ready/$\overline{Busy}$ goes back to high impedance the NMC98C64 has completed writing, and is ready to accept another cycle.
- $\overline{DATA}$ Polling — The NMC98C64 features $\overline{DATA}$ Polling to signal the completion of a byte or page write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

STANDBY MODE

A device is disabled by bringing $\overline{CE}$ high. The power dissipation is reduced to I_{CCS} if it is disabled between operations. Writing to the memory in the standby mode is inhibited.

WRITE INHIBIT MODE

Holding $\overline{OE}$ low or $\overline{WE}$ high always inhibits a write cycle.

WRITE PROTECTION

There are three features that protect the non-volatile data from an inadvertent write:

- Noise Protection — A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- Write Inhibit — Holding $\overline{CE}$ high, $\overline{OE}$ low or $\overline{WE}$ high inhibits a write during the time when V_{CC} supply is being powered up/down,
- Optional V_{CC} Sense — To avoid the initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.8 volts. It is the user's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.8 volts.

To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE}$ = V_{IH} must be applied simultaneously or before application of V_{CC}. $\overline{WE}$ or $\overline{CE}$ = V_{IH} must be removed simultaneously or after V_{CC}.

To prevent damage to the device it must not be inserted into or removed from a board with power applied.

ENDURANCE

National Semiconductor E²PROM devices are designed for applications requiring up to 10,000 Erase/Write cycles per byte.

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temp. (Soldering, 10 Seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Conditions

Temperature Range	0°C to +70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 10%

DC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol		Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION							
I_{LI}		Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}			10	μA
I_{LO}		Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$			10	μA
I_{CCA}	TTL	V_{CC} Current Active (Operating)	Inputs toggling with V_{IH} & V_{IL} levels, I/O's = Open		10	20 + 5/MHz	mA
	CMOS		Inputs toggling with CMOS levels (V_{CC} − 0.2V; V_{SS} + 0.2V), I/O's = Open			0.2 + 5/MHz	mA
I_{CCS}	TTL	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			2	mA
	CMOS		$\overline{CE} \geq V_{CC}$ − 0.2V		100	200	μA
I_{CCQ}	TTL	V_{CC} Current Quiescent	$\overline{OE} = \overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$, A_0–$A_{12} = V_{IL}$ or V_{IH}, I/O's = Open			20	mA
	CMOS		$\overline{OE} = \overline{CE} \leq V_{SS}$ + 0.2V, $\overline{WE} \geq V_{CC}$ − 0.2V, I/O's = Open, A_0–$A_{12} = V_{SS}$ + 0.2V or V_{CC} − 0.2V			200	μA
V_{IL}		Input Low Voltage		−0.1		0.8	V
V_{IH}		Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	TTL	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
	CMOS	Output Low Voltage	I_{OL} = 10 μA			0.2	V
V_{OH}	TTL	Output High Voltage	I_{OH} = −400 μA	2.4			V
	CMOS	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.2			V
WRITE OPERATION							
I_{CCW}		V_{CC} Current (Write)	RDY/$\overline{Busy}$ = V_{OL}			20	mA

Capacitance T_A = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			10	pF

AC Test Conditions

Output Load	1 TTL gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V
Input Rise and Fall	5 ns

Read Mode AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Conditions	NMC98C64-20			NMC98C64-25			NMC98C64-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200			250			350	ns
t_{CE}	Chip Enable Access Time	$\overline{OE}$ = V_{IL}			200			250			350	ns
t_{OE}	Output Enable Access Time	$\overline{CE}$ = V_{IL}			75			100			120	ns
t_{HZ}	Output in Hi-Z from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ or $\overline{OE}$ = V_{IL}			80			100			100	ns
t_{OH}	Output Hold from Address Change	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			0			0			ns
t_{TR}	Input Rise and Fall Time		3		50	3		50	3		50	ns (Notes 1 & 2)
t_{LZ}	Output Active from $\overline{CE}$ or $\overline{OE}$	$\overline{CE}$ or $\overline{OE}$ = V_{IL}	20			20			20			ns

Write Mode AC Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 10% (Note 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to $\overline{WE}$ Setup Time		10			ns
t_{AH}	Address to $\overline{WE}$ Hold Time		200			ns
t_{CS}	Write Setup Time		0			ns
t_{CH}	Write Hold Time		0			ns
t_{OES}	$\overline{OE}$ to $\overline{WE}$ Setup Time		30			ns
T_{OEH}	$\overline{OE}$ to $\overline{WE}$ Hold Time		200			ns
t_{WP}	Write Pulse Time		200			ns
t_{WPH}	Write Pulse High		200			ns
t_{DS}	Data Setup Time	$\overline{OE}$ = V_{IH}	100			ns
t_{DH}	Data Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{DLP}	Page Data Load Time		300		1000	μs (Note 4)
t_{WC}	Write Cycle Time				10	ms
t_{TR}	Input Rise and Fall Time		3		50	ns (Note 1 & 2)

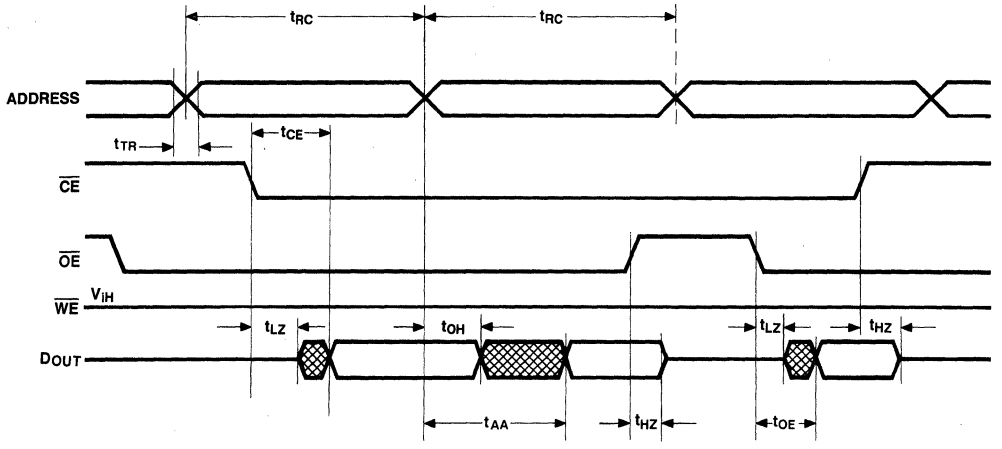
Note 1: This parameter only sampled and not 100% tested.

Note 2: All input signals must transit from V_{IL} to V_{IH} or from V_{IH} to V_{IL} in a monotonic manner. Transition times are measured between V_{IL} (max) and V_{IH} (min).

Note 3: Write cycles can be controlled by either $\overline{WE}$ or $\overline{CE}$. Timing Diagram on page 5 indicates $\overline{WE}$ controlled Write Cycle. For $\overline{CE}$ controlled Write Cycle (i.e. $\overline{CE}$ goes LOW after $\overline{WE}$ and goes HIGH before $\overline{WE}$) timing specs referenced to $\overline{WE}$ edges should be referenced to $\overline{CE}$ edges.

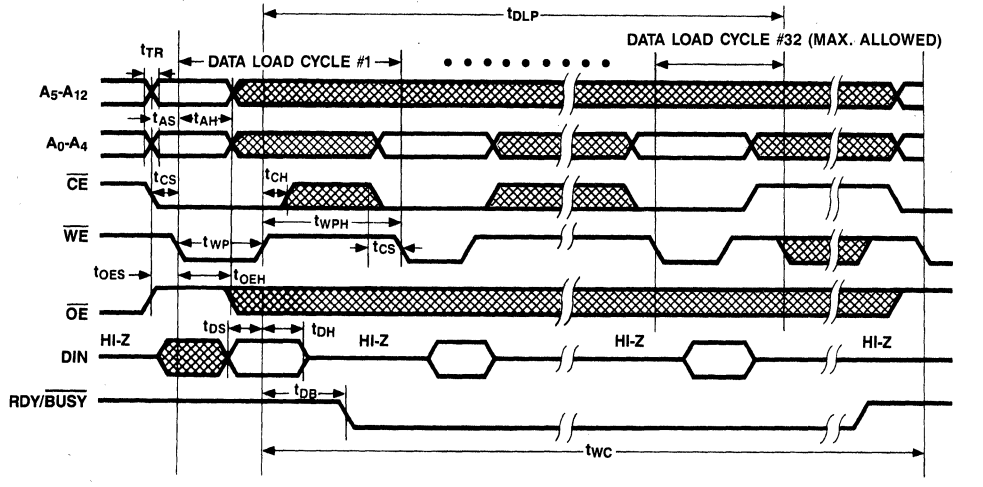
Note 4: Proper DL cycles are guaranteed up to Minimum t_{DLP} time. $\overline{CE}$ or $\overline{WE}$ DON'T CARE starts after Maximum t_{DLP} time.

Timing Waveforms



TL/D/7514–4

FIGURE 3. NMC98C64 Read Cycle Switching Time Waveforms



TL/D/7514–5

FIGURE 4. NMC98C64 Write Cycle Switching Time Waveforms

Section 2

Application Notes

Avoiding Problems Caused by Capacitive Coupling Between Input Signal Lines on 21-Volt EEPROMs

National Semiconductor
Application Brief 13
Elroy Lucero
May 1984

The high input impedance of MOS memories, such as the NMC 2816, makes such parameters as board layout, signal shielding, device package, and driver characteristics of great importance in minimizing the effects of pin to pin coupling between input signal lines.

This problem is exaggerated on 21 volt EEPROMs where the high voltage programming pulse applied to the VPP input (pin 21) can couple sufficient voltage to the OE signal line (pin 20) as to force the circuit into the chip erase mode of operation, thereby causing data loss.

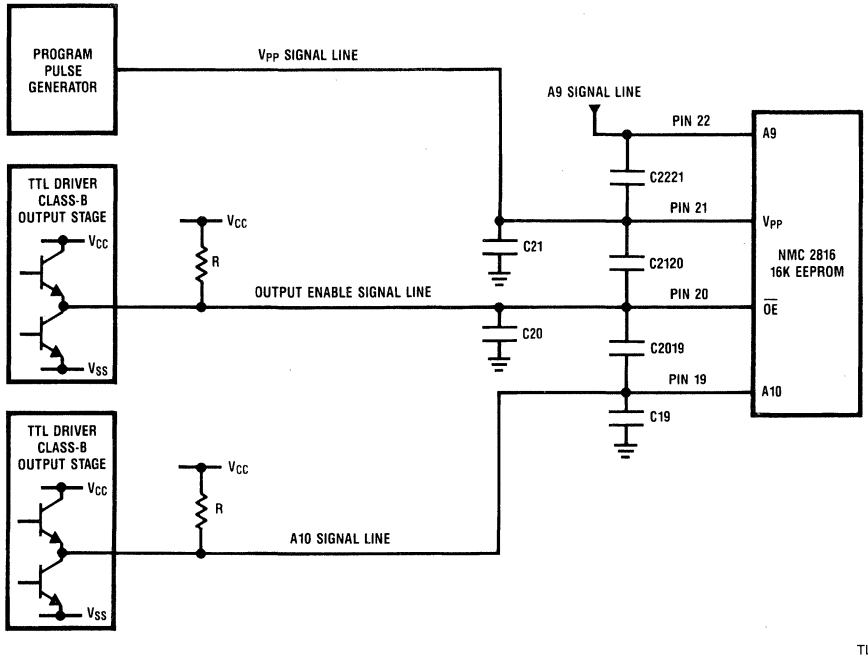
Figure 1 is a simplified schematic diagram showing the possible sources of pin to pin capacitive coupling and the output stages of standard TTL drivers used to drive the address and OE input signal lines.

The voltage coupled to the OE input signal line is

$$V20 = V_{oh} + \left(\frac{C2120}{C2120 + C20}\right)\Delta V21 + \left(\frac{C2019}{C2019 + C20}\right)\Delta V19$$

In standard 5-volt systems the amount of voltage coupled between input signal lines is small and does not usually present problems. However, for EEPROMs requiring 21 volt pulses, the voltage coupled between input signals can be much larger and may damage other devices on the signal line whose input characteristics require that V_{in} does not exceed V_{CC} + 1 volt. Moreover, an input signal coupled above the specified V_{ih} maximum may cause the device to enter an undesired or non-user test mode (e.g., "read redundancy" or "stress array").

The input impedance of an MOS input is typically greater than 50 megohm for V_{in} less than 20 volts and T_a = 25°C. This extremely high input impedance is limited only by the reverse diode leakage of the pn junction present at the input. This pn junction (part of the input protection circuitry used to guard against possible ESD damage) is temperature sensitive causing the effective input impedance to increase at lower temperatures.



TL/D/7084–1

Note: All capacitors are total effective capacitance caused by trace to trace capacitance on PC board, package pin to pin capacitance, device input capacitance, signal line capacitance, etc.
Note: Resistor R limits voltage overshoot above V_{ih} cause by capacitive coupling.

FIGURE 1. Schematic Diagram Showing Pin to Pin Capacitive Coupling and the Output Stages of TTL Drivers Used to Drive Signal Lines

The output impedance of a standard TTL driver is quite low and suitable for driving an MOS input signal line for V_{oh} less than 4.5 volts. However, if the output voltage of the driver is coupled above this potential the driver enters a high impedance region, with only the reverse diode leakage of the output pn junction to limit the final voltage coupled to this signal line. Therefore care must be taken to minimize the amount of signal to signal coupling and insure that the driver output characteristics remain compatible with the characteristics of the MOS input being driven.

Fortunately for users of MOS memories the solution is simple and straightforward. By adding a resistor between V_{CC} (or V_{SS}) and the output of the TTL driver the effective output impedance of the driver can be lowered for voltages above V_{oh}. This modification will provide a low impedance path to V_{CC} (or V_{SS}) for discharging the coupled voltage. This simple technique will ensure that the voltage seen by the MOS input will not exceed the specified V_{ih} maximum (V_{CC} + 1 volt). In the case of 21-volt EEPROMs this technique used on the OE driver will prevent inadvertent chip erase cycles from occurring and therefore enhance the overall system reliability. In addition, steps taken to reduce the amount of capacitive coupling between input signal lines and proper shielding of input signals further reduces the possibility of data loss.

Protecting Data in the NMC9306/COP494 and NMC9346/COP495 Serial EEPROMs

National Semiconductor
Application Brief 15
Asim Bajwa
May 1984

The NMC9306/COP494 and NMC9346/COP495 are non-volatile serial access memories with the following salient features:

- Low cost
- Single supply read/write/erase operation (5V ± 10%)
- TTL compatible
- MICROWIRE™ compatible I/O
- 16 × 16 serial read/write memory (NMC9306/COP494)
  64 × 16 serial read/write memory (NMC9346/COP495)
- Self-timed programming cycle (NMC9346/COP495 only)
- Ready/busy status signal during programming (NMC9346/COP495 only)
- Read-only mode

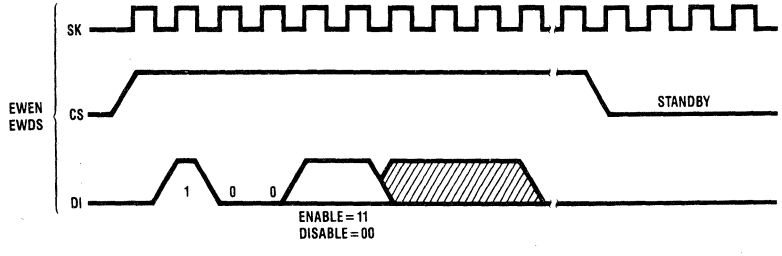
The read-only mode is provided to prevent accidental data disturb, especially during V_{CC} power up, power down or excessive noise on the I/O or power supply pins.

Executing the EWDS instruction (*Figure 1*) activates this mode by disabling the programming modes and the high voltage pump. The READ instruction is not affected and can be executed as usual. However, all programming instructions (ERASE, WRITE, ERAL and WRAL) are ignored until the EWEN instruction is executed to enable programming.

On V_{CC} power up the device is designed to automatically enter the read-only mode to avoid accidental data loss due to power up transients. Putting the device in the read-only mode before powering down V_{CC} avoids spurious programming during power down.

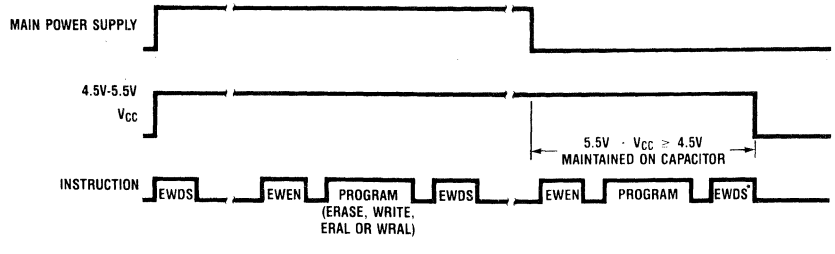
The following guidelines are presented and should be incorporated into the user's designs to achieve the maximum possible protection of stored data *(Figure 2)* :

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.
2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return



TL/D/7085–1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085–2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Using E²PROM's with ROMless Single Chip Microcontroller

National Semiconductor
Application Brief 17
Joel Fishman
July 1984

When developing programs for single chip microcontrollers, current thinking suggests that engineers use μvEPROMs as program memory. This technology offers the advantage of non-volatility yet allows the designer to change the program when necessary. This technology has manifested itself in ROMless versions of the COPS™ 4-bit and 8048 8-bit families with parts such as the 8035 and 87P50 piggyback version.

The major disadvantage of this technology is that the entire chip must be erased and reprogrammed regardless of the size of the change. The chip erase cycle takes 20 minutes, typically, and as such, lengthens the software development cycle. Although a number of μvEPROMs' may be held as spares for reprogramming this is not the most efficient method available.

Emerging Electrically Erasable PROM (E²PROM) technology solves this problem. The entire chip may be programmable using a PROM programmer such as the one you'd use for the μvEPROMs. In addition, thanks in part to the 5V only operation, on-board address and data latches, self-timed writing, and single byte programming the E²PROM may be modified in the system with minimal hardware overhead. This application note shows how to design the hardware to interface a ROMless version of the 8048 family with the NMC9817, National's 16k (2k x 8), 5V only E²PROM.

When making program changes manually, it may be more efficient to just make patches than to reprogram large sections of memory. After the program is running, a final step would be to reassemble. This manual technique is also suitable for changing minor errors in instruction coding.

Description

Figure 1 shows the block diagram required to implement a ROMless 8-bit microcontroller with 4k bytes of E²PROM.

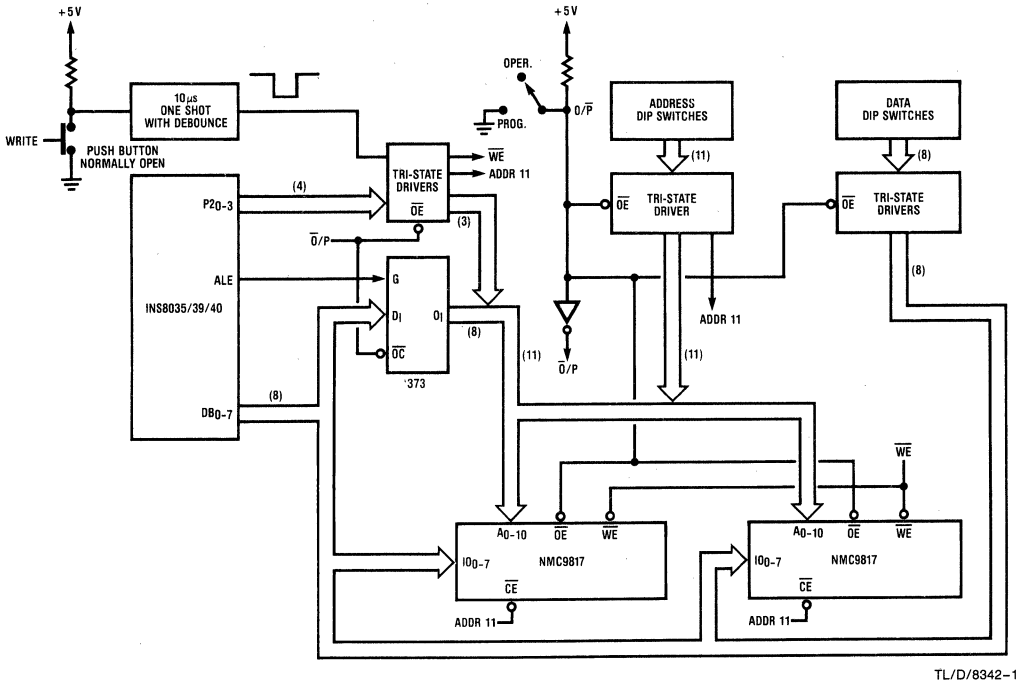
Normal operation of the system occurs when the PROG/OPER switch is in the OPER position. This enables the output of the address latch from the microcontroller, while putting the TRI-STATE® drivers from the DIP switches to the high impedance state. The system functions as current designs using EPROMs.

When a location in memory needs to be changed the switch is set to the PROG position. This enables the DIP SWITCH DRIVERS. The address of the byte to be modified and the data to be written are set on the binary DIP switches. The WRITE push button is pressed, generating a 10 μsec negative going pulse.

The write pulse ($\overline{WE}$) latches the address and the data into the proper 2k page of memory, as selected by ADDR11 and the write cycle takes place.

This technique may be used to change one byte, a few bytes, or to put a patch into the software. If a routine is incorrect a jump instruction to a blank area of memory can be used to create a new routine.

Block Diagram



TL/D/8342–1

FIGURE 1

AN-328
EEPROM Application Note
Vpp Generation on Board

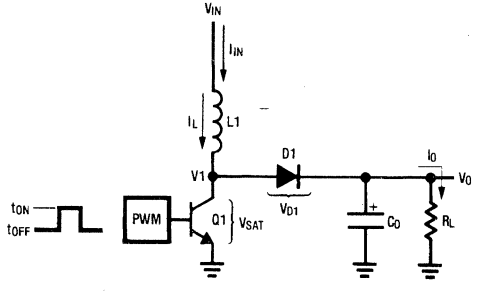
National Semiconductor
Application Note 328
Massood Alavi, Sr. Apps Mgr
February 1983

The NMC2816 requires a 21V pulse for writing and erasing. The rise time on the pulse going from 5–21V is to be 600μs ideally. The NMC 9716 requires a stable 21V. This application note discusses two methods of generating the required Vpp voltage or the high level pulse from a 5V supply.

The first method shows how to generate 21V from a single 5V supply using an LM3524 switching voltage regulator, a power inductor and a number of capacitors as the main active elements. The principle involved is explained by the circuit of Figure 1.

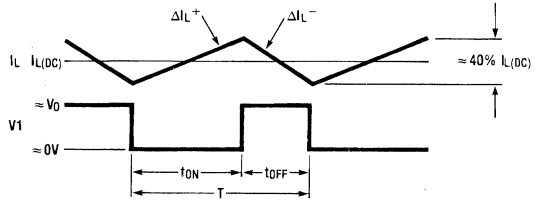
THE STEP-UP SWITCHING REGULATOR

Figure 1 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}. Q1 is ON and energy is drawn from V_{IN} and stored in L1:D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens during t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1,D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here the current through L1 has a DC component plus some ΔI_L. ΔI_L is selected to be approximately 40% of I_L. Figure 2 shows the inductor's current in relation to Q1's ON and OFF times.



TL/D/5152–1

FIGURE 1. Basic Step-Up Switching Regulator



TL/D/5152–2

FIGURE 2. Voltage and Current Waveforms at V1

The following equations are derived to give the reader a theoretical understanding of the operation.

From $\Delta I_L = \frac{V_L T}{L}$, $\Delta I_L{}^+ \cong \frac{V_{IN} t_{ON}}{L1}$

and $\Delta I_L{}^- \cong \frac{(V_o - V_{IN}) t_{OFF}}{L1}$

Since $\Delta I_L{}^+ = \Delta I_L{}^-$, $V_{IN} t_{ON} = V_o t_{OFF} - V_{IN} t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \cong V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)} \quad 1.$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)} V_{IN}$$

$$P_{OUT} = I_o V_o = I_o\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

for $\eta = 100\%$, $P_{OUT} = P_{IN}$

$$I_o\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\ V_{IN}$$

$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)} \quad 2.$$

So far it is assumed $\eta = 100\%$, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1} = 1V$ this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_o}{P_{IN}} = \frac{V_o I_o}{V_o I_o + I_{IN}(1V)} = \frac{V_o I_o}{V_o I_o + I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

From $V_o = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$,

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}} \quad 3.$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_o t_{ON}}{C_o} \text{ or } C_o = \frac{I_o t_{ON}}{\Delta V_o}$$

From $V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right)$; $t_{OFF} = \frac{V_{IN}}{V_o} T$

where $T = t_{ON} + t_{OFF} = \frac{1}{f}$

$t_{ON} = T - \frac{V_{IN}}{V_o} T = T\left(\frac{V_o - V_{IN}}{V_o}\right)$ therefore:

$$C_o = \frac{I_o T\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o(V_o - V_{IN})}{f \Delta V_o V_o}} \quad 4.$$

where: C_o is in farads, f is the switching frequency,
ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$L1 = \frac{V_{IN} t_{ON}}{\Delta I_L +}$, since during t_{ON},

V_{IN} is applied across L1

$\Delta I_{Lp.p} = 0.4 I_L = 0.4 I_{IN} = 0.4 I_o\left(\frac{V_o}{V_{IN}}\right)$, therefore:

$$L1 = \frac{V_{IN} t_{ON}}{0.4 I_o\left(\frac{V_o}{V_{IN}}\right)} \text{ and since } t_{ON} = \frac{T(V_o - V_{IN})}{V_o}$$

$$\boxed{L1 = \frac{2.5\ V_{IN}{}^2 (V_o - V_{IN})}{f\ I_o V_o{}^2}} \quad 5.$$

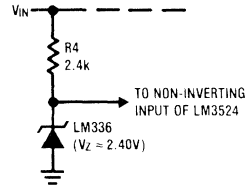
where: L1 is in henrys, f is the switching frequency in Hz

To apply the above theory, a complete step-up switching regulator is shown in Figure 3. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \bullet V_{INV} = 2.5\left(1 + \frac{R2}{R1}\right) \quad 6.$$

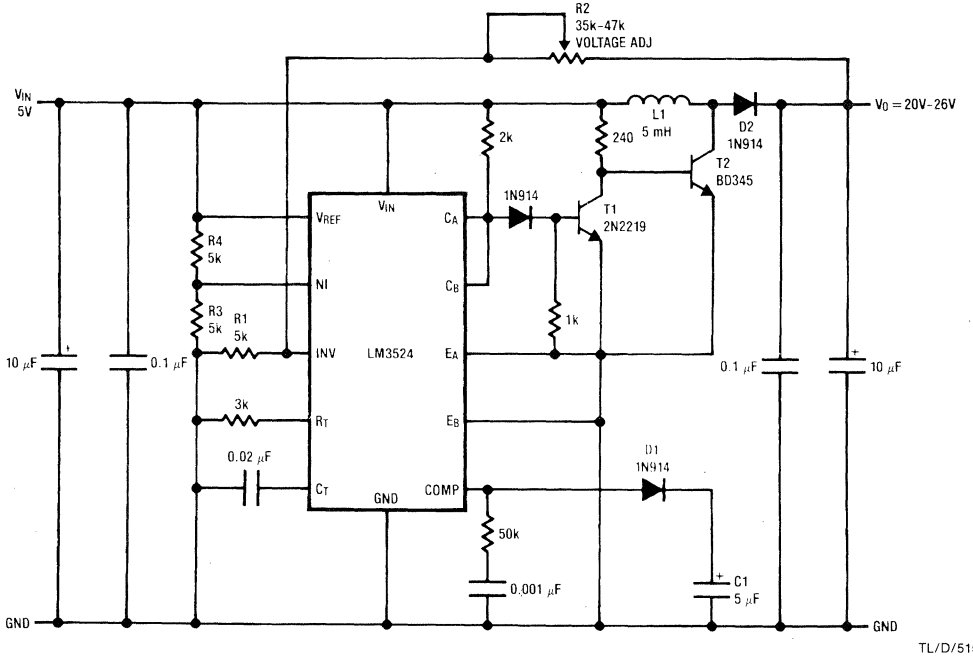
The network D1, C1 forms a slow start circuit. This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from OV. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see Figure 4, the input voltage variations are rejected.

Using equation 1 any desired supply voltage can be generated at V_o by selecting a suitable value for R_2. If R_2 is a pot in the 25K–50K range, it can be used to set V_o from 15V–27.5V. For standard E²PROM and EPROM applications this range is very suitable for Vpp set up. Table I shows various values of R_2 for corresponding values of V_o.



TL/D/5152–4

FIGURE 4. Voltage Reference



TL/D/5152–3

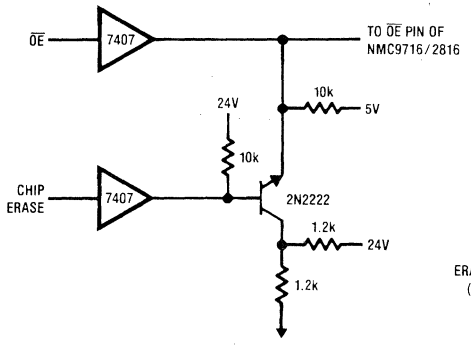
FIGURE 3. A 5V–21V Vpp Voltage Generator Circuit for E²PROM Application

TABLE I.

R_2	V_o
47K	26V
45K	25V
43K	24V
41K	23V
39K	22V
37K	21V
35K	20V

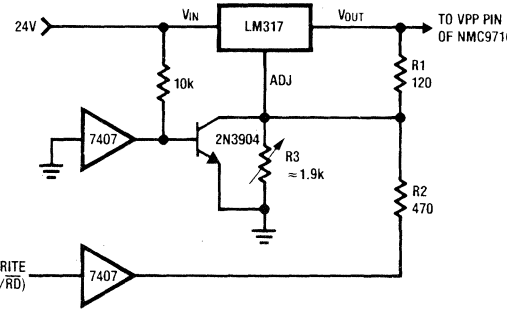
The current sourcing capability of V_o can be made as high as 500mA. If no more than 100mA are desired, T_1 and 240 ohms resistor can be replaced by T_2 alone; the base of T_2 should be connected to the node at base of T_1; T_2 collector and emitter should be left intact. 100mA is sufficient to support up to 20 NMC2816's or NMC9716's.

The Vpp voltage generated by the circuit of Figure 3, can be used to provide the E/W pulses on the NMC2816 or the stable Vpp on NMC9716. The 9V–15V needed for chip erase can also be generated. Figures 5, 6, 7 demonstrate how to achieve that.



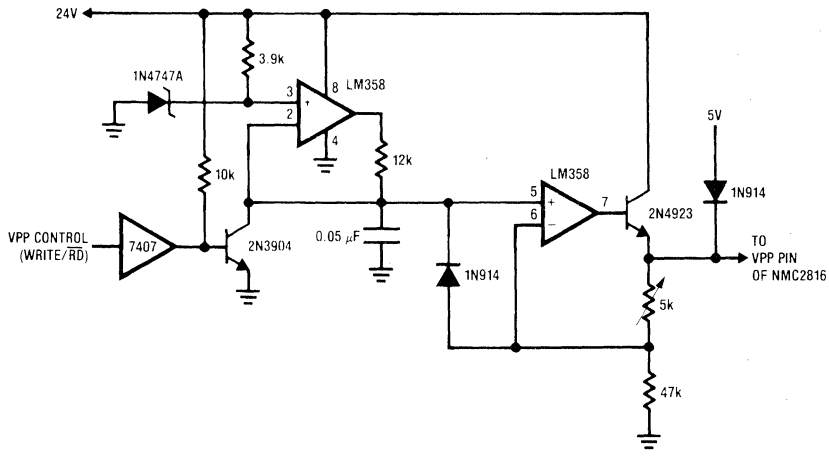
TL/D/5152–5

FIGURE 5. $\overline{OE}$ Chip Erase Control for NMC2816/NMC9716



TL/D/5152–6

FIGURE 6. VPP Switch Design with Electronic Shutdown for $\overline{CE}$ Pulsed Erase/Write for NMC9716



TL/D/5152–7

Note 1: 5k is 21V fine adjust.

Note 2: Resistors are ¼W.

FIGURE 7. Operational Amplifier VPP Switch Design for NMC2816

The following paragraphs outline a second method of generating a 21V pulse from a single 5V supply. Figure 8 shows such a DC-DC converter circuit.

In the circuit, inductor L1 in conjunction with transistors Q1 & Q2 form a self driven 5–30V converter. Transitors Q3 & Q4 are meant to strobe the converter allowing it to draw power and run only when a TTL high is presented at the input node A. Trace A, Figure 9 shows the signal to be applied at the input node. This makes the Q3-Q4 transistor pair conduct biasing Q1 & Q2. Trace B, Figure 9 shows the resultant waveform generated at node B, the collector of Q2. As the converter runs, its output at node C rises to the desired high voltage of 30V quickly. The output is lightly filtered by the .1F capacitor. Trace C, Figure 9 shows this waveform.

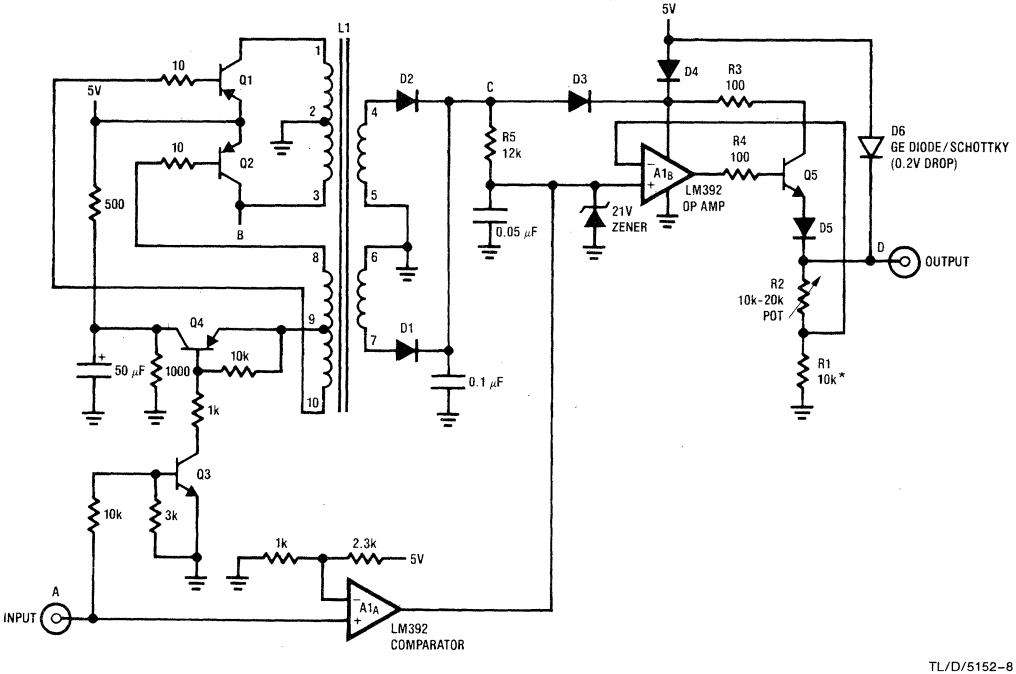
The voltage at node C is used to charge the 12k, .05μF combination at the desired RC of 600μS. This signal cut off at 21V by the Zener at the input to A1B is presented to the amplifier A1B to be outputted to node D as the desired V_{PP}. The amplitude and pulse shape is controlled by setting the cut-off Zener voltage in conjunction with the gain of A1B set by R2. For example, if 7V Zener voltage is used for cut off a gain of 3 will have to be set for A1B to get a 21V output pulse.

When the capacitor reaches the Zener cut off, the Zener clamps, charging ceases and the circuit output sits at 21V.

When the signal at node A goes to TTL low, the open collector output of comparator A1A clamps low, discharging the .05 capacitor and getting the circuit ready for the next pulse. Any EEPROM programming requirement can be met by varying the gain of A1B, the time constant at its input and/or the Zener value across the capacitor. Any TTL detect value can be set by the voltage-divider on the A1A comparator in this case set at about 1.5V.

Transistor Q5 is provided to source boosted output current. Diode D6 is provided to hold the output or V_{PP} as close to Vcc as possible when 21V is not desired. A Ge or Schottky diode must be used to optimize the diode forward drop at $\leq$.2V. D5 is provided to maximize the reverse breakdown from node D to base of Q5, when 21 volts is at node D.

Figure 9 shows the idealized signals generated at various nodes. When the input at node A is at TTL low level, the output D sits at 4.8V. As the input A goes to a TTL high level the output D rises to 21V at RC of 600μS. The waveform at node A may be derived from the $\overline{CE}$ by inverting the $\overline{CE}$ signal. The resulting waveform at node D is used for V_{PP}.



TL/D/5152–8

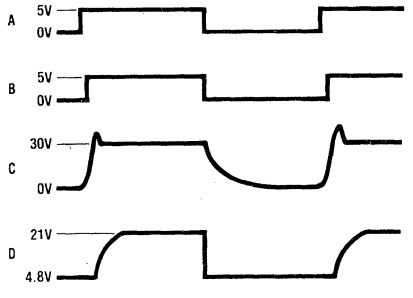
FIGURE 8. V_{PP} Pulse Generator Circuit

References:

Circuit of Figure 3 is derived from NSC voltage regulator application.

Circuit of Figure 9 is from Electronic design, October 15, 1981.

"Design DC-DC converters to catch noise at source" — J Williams.



TL/D/5152–9

FIGURE 9. Idealized Signals at Various Nodes

Designing with the NMC9306/COP494 a Versatile Simple to Use E² PROM

National Semiconductor
Application Note 338
Masood Alavi
June 1983

This application note outlines various methods of interfacing an NMC9306/COP494 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NMC9306; as well as how serial data outputted from an NMC9306 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NMC9306/COP494.

The third part of the application note shows a list of various applications that can use a NMC9306/COP494.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

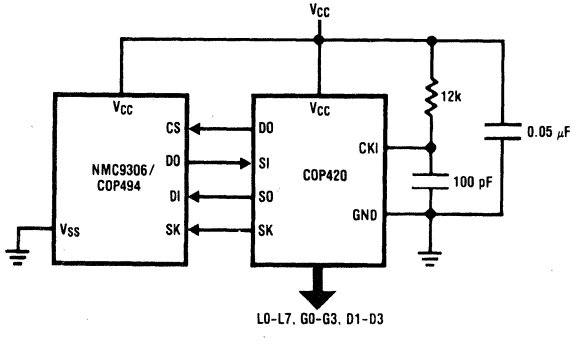
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E²PROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NMC9306/COP494 — COP420 Interface

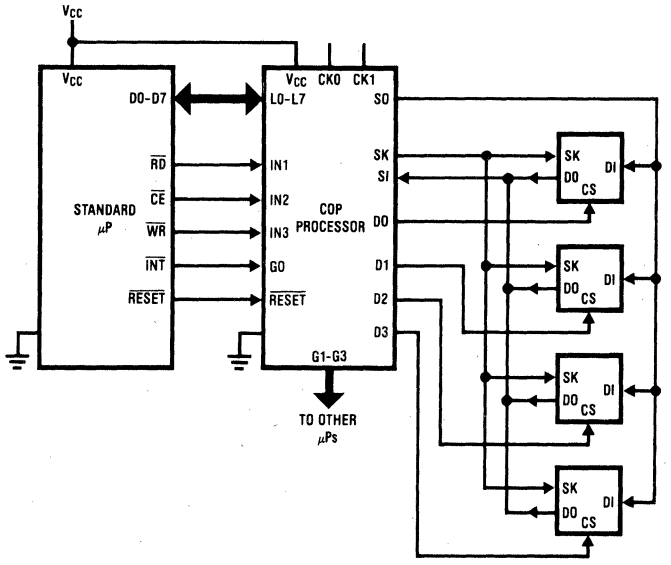
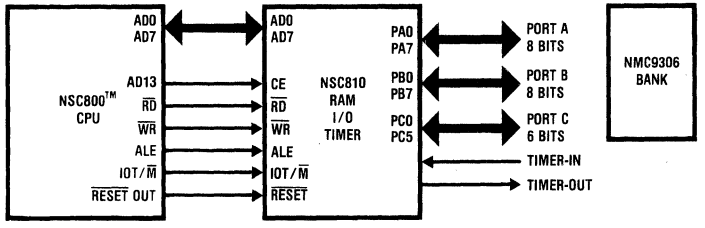


FIGURE 2. NMC93O6 — Standard μP Interface Via COP Processor

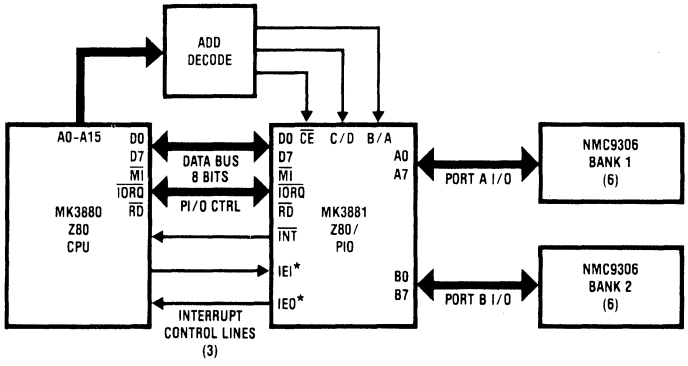


PA0 → SK
PA1 → DI/DO
PA2–7 → 6CS for 6– 9306's

Common to all 9306's

* SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.
* CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.

FIGURE 3. NSC800™ to NMC9306 Interface (also Valid for 8085/8085A and 8156)



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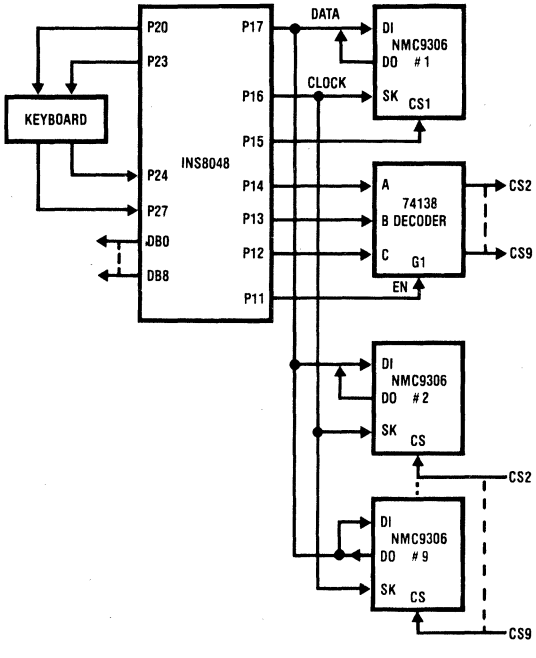
Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

FIGURE 4. Z80 — NMC9306 Interface Using Z80-PIO Chip



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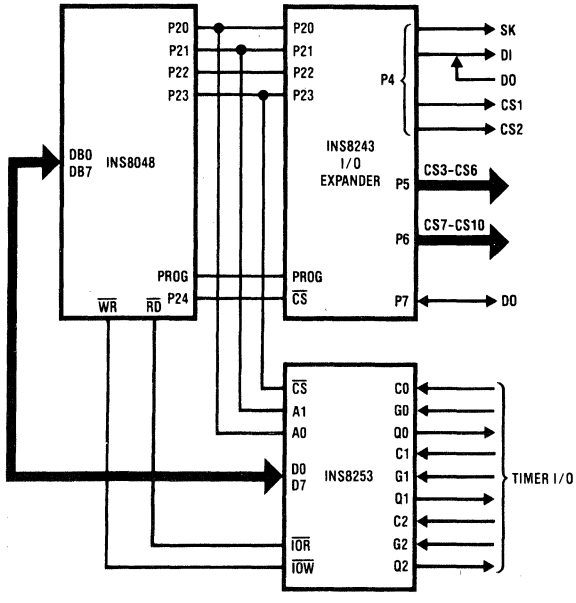
* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NMC9306 frequency range.
* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP — NMC9306 Interface



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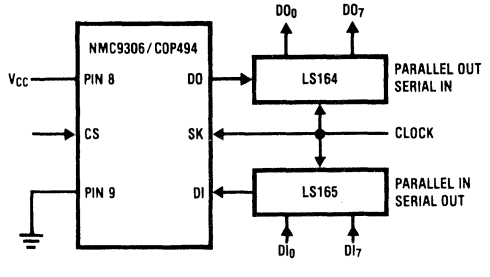
Expander outputs

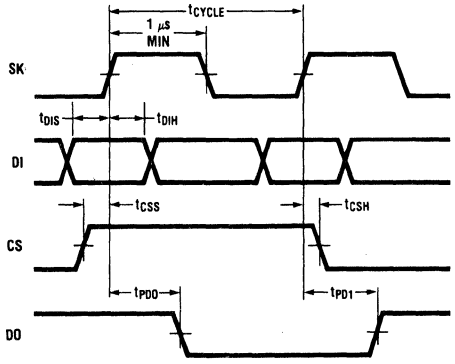
	DI SK	(COMMON)
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion



TL/D/5286–7

FIGURE 7. Converting Parallel Data into Serial Input for NMC9306/COP494



Min	Max
t_{CYCLE} 0	250 kHz
DUTY CYCLE 25%	75%
t_{DIS} 400	ns
t_{D1H} 400	ns
t_{CSS} 200	ns
t_{CSH} 0	ns
t_{PD0}	2 μs
t_{PD1}	2 μs

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FIGURE 8. NMC9306/COP494 Timing

THE NMC9306/COP494

Extremely simple to interface with any μP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Clock input for data bit maneuvering
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

* Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

** DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NMC9306/COP494

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most μPs in the 1–11 MHz range this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard μP speeds. Symmetrical duty cycle is irrelevant if SK HI time is $\geq$ 2 μs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for up to ten years independent of V_{CC}, which may be on or off. For all practical purposes any number of read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

INSTRUCTION SET

Commands	Opcode	Comments
READ	10000A3A2A1A0	Read Register 0–15
WRITE	11000A3A2A1A0	Write Register 0–15
ERASE	10100A3A2A1A0	Erase Register 0–15
EWEN	111000 0 0 1	Write/Erase Enable
ENDS	111000 0 1 0	Write/Erase Disable
*** WRAL	111000 1 0 0	Write All Registers
ERAL	111000 1 0 1	Erase All Registers

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

ERASE

ERASE ALL — Command shifted in followed by

WRITE ALL — Pulsing CS low for 10 ms.

WRITE

ENABLE/DISABLE — Command shifted in.

*** (This Instruction is not speced on Data sheet.)

The following is a list of various systems that could use a NMC9306/COP494

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control

B. Bathroom scale
Blood analyzer
Bus interface

C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator

D. Data acquisition system
Data terminal

E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system

F. Flow computer
Frequency synthesizer
Fuel computer

G. Gas analyzer
Gasoline pump

H. Home energy management
Hotel lock

I. Industrial control
Instrumentation

J. Joulemeter

K. Keyboard -softkey

L. Laser machine tool

M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector

N. Navigation receiver
Network system
Number comparison

O. Oilfield equipment

P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter

Q. Quiescent current meter

R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer

S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer

T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller

U. Ultrasound diagnostics
Utility telemetering

V. Video games
Video tape system
Voice/data phone switch

W. Winchester disk controller

X. X-ray machine
Xenon lamp system

Y. YAG—laser controller

Z. Zone/perimeter alarm system

Designing with the NMC9817, a 2nd Generation E²PROM

National Semiconductor
Application Note 342
Masood Alavi
December 1983

The NMC9817 offers the non-volatile memory designer the following features:

- 16K bits of non-volatile storage organized as 2K × 8
- fully 5V only operation in all modes
- address, data and $\overline{WE}$ latches, upward and downward compatible with E²'s, EPROMs, ROMs and SRAMs
- fast read access times
- direct microprocessor interfacing capability
- 10,000 write cycles per byte open-drain ready/$\overline{busy}$
- 10-year data retention

The purpose of this application note is to detail the new features and the simple interface considerations inherent to using the NMC9817.

The JEDEC-28 pin universal memory pin-out has been selected for the NMC9817. *Figure 1* shows this pin-out and how it relates to other memory types.

This philosophy allows for interchanging memory types and to provide the required densities. E²PROMs can be mixed with PROMs, ROMs, RAMs or EPROMs. Upward or downward compatibility is possible in density selection, providing great flexibility in system design requirements, even as they change through the course. New features or upgrades can be added with minimal hardware modifications. With the 28-pin selected pin-out of the NMC9817, E²PROM devices from 4k to 128k will fit perfectly without external interface requirements. The pin-out also allows inserting 24-pin E²PROM devices because of common data, address and control pins.

Figure 2 shows a block diagram of the NMC9817.

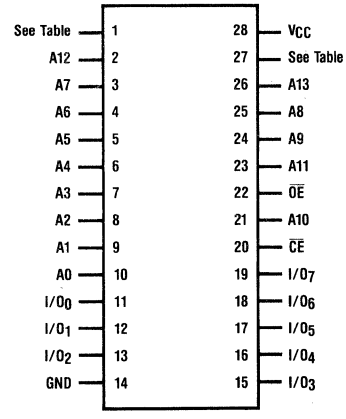
The basic constraints on 1st generation E²PROMs have been quite cumbersome. 10,000 erase/write cycles/byte, 10 ms or more erase/write times, external 21V generation, lack of on-chip buffers and latches have been the important generic considerations. Many support components have been essential to incorporate these requirements.

External programming voltage entailed either a DC-DC converter or a step down voltage regulator (See AN-328). In addition, support circuitry for sequencing write cycles was necessary because 10 ms erase/write time is a much longer period than a typical microprocessor cycle. This required external data and address latches and a counter to time out the erase/write periods. Analog pulse-shaping circuitry for erase/write pulses is also an external interface requirement.

Figure 2 shows how all the above interface requirements are integrated on the NMC9817. This allows for a direct interface with any microprocessor capable of providing the required control signals. Even the generic constraint of 10 ms write time has been efficiently designed around. To initiate a RAM like write cycle the microprocessor signals with a 100 ns $\overline{WE}$ pulse after $\overline{CE}$ is valid. Only one instruction is required to do so after which the intelligence in the NMC9817 takes care of the rest allowing the microprocessor to execute other instructions while the E²PROM writes the byte. This is so because the NMC9817 contains all the necessary data in on-chip latches. A ready/$\overline{busy}$ output is provided on pin 1 which goes to logic low when the part goes into a write cycle and logic high when the write is done.

Not only can this pin be used to signal an interrupt to the microprocessor to put the E²PROM on or off line, it also serves to optimize the best possible write time that a part has. In other words, if the NMC9817 gets programmed in less than 10 ms, the ready/$\overline{busy}$ line output will allow the microprocessor to take advantage of this. This is implemented by a method referred to as multiple-hits of write pulses. Refer to *Figure 3*.

SRAM	NOVRAM	ROM	EPROM	E²PROM	
8K ↓ 256K	4K ↓ 128K	8K ↓ 256K	8K ↓ 256K	4K ↓ 128K	
A14	$\overline{NE}$	NC	V_{PP}	RDY/BUSY	Pin 1
$\overline{WE}$	$\overline{WE}$	A14	PGM/A14	$\overline{WE}$	Pin 27



TL/D/5477–1

FIGURE 1. Universal 28-Pin Pin-out

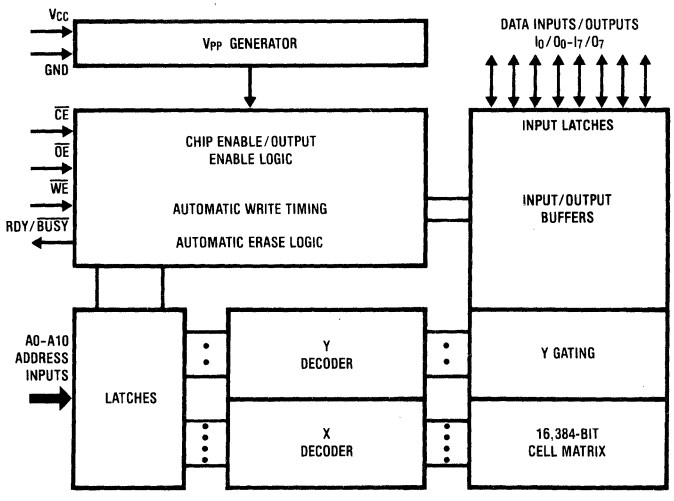


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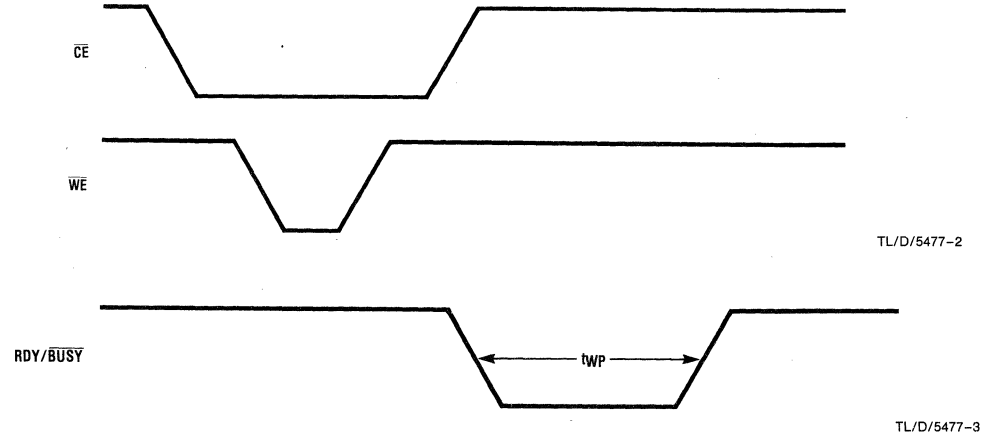
FIGURE 2. Functional Block Diagram



TL/D/5477–2

TL/D/5477–3

FIGURE 3. Write Waveforms

As soon as the write pulse is detected by the device, the following sequence of events commences:

- Ready/$\overline{\text{busy}}$ goes low and puts the device off the microprocessor bus.
- A read before write is internally initiated to determine whether or not an Erase before write is required.
- If any zero is detected in the byte during the read a 5 ms max Erase cycle is initiated during which internal V_{PP} is raised to 21V. Following the Erase, a 5 ms max write cycle is executed.
- If all ones are detected in the byte during the read, the Erase before write cycle is skipped and a 5 ms max write cycle is executed.
- Once write is verified and completed, the ready/$\overline{\text{busy}}$ is raised to interrupt the microprocessor.

The above sequence allows for achieving fast write times without compromising data retention or data integrity.

For convenience in system design, full 5V operation is designed in the NMC9817. This has been done by incorporating on chip a 5-21V charge pump, a 21-volt regulator and-power up/down sequencer to avoid inadvertent spurious writes. Regulation of the 21V internal supply is an important consideration, more so over temperature since it is directly related to endurance. Voltage spikes can cause early damage to the integrity of the tunnel-oxides.

Interface Requirements

Figure 4 shows the simple interface requirements in using the NMC9817. Besides the direct bus connections to the microprocessor, three or four (if ready/$\overline{busy}$ is used) connections are required viz $\overline{CE}$ to decoder, $\overline{OE}$ to $\overline{RD}$, $\overline{WE}$ to $\overline{WR}$ and ready/$\overline{busy}$ to an interrupt. Ready/$\overline{busy}$ may be multiplexed for hardware handling. It can also be OR-tied if desired since it is an open-drain output; the slowest device will control the write time in such a case.

Figure 5 shows a typical large system application with multiplexed ready/$\overline{busy}$.

In summary, the NMC9817 has been designed as a monolithic solution to the problems that arose with the first generation of E²PROMs. It attempts to establish a standard for future E²PROMs, both from an electrical parametric viewpoint and ease-of-use system design considerations. It solves the following problems that confronted the first generation E²PROMs:

1. A 21V external power supply.
2. A rise time restricted 10 ms wide minimum pulse for erase/write.
3. Lack of on-chip address and data latches.
4. Absence of an interrupt ready/busy output.
5. Non-integrated erase before write.
6. Non-upgradable package.

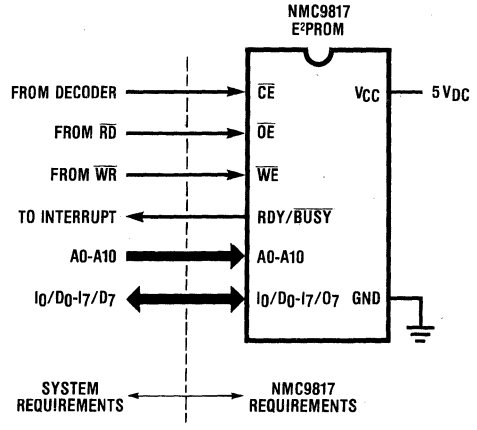


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FIGURE 4. Simple NMC9817 Interface Requirements

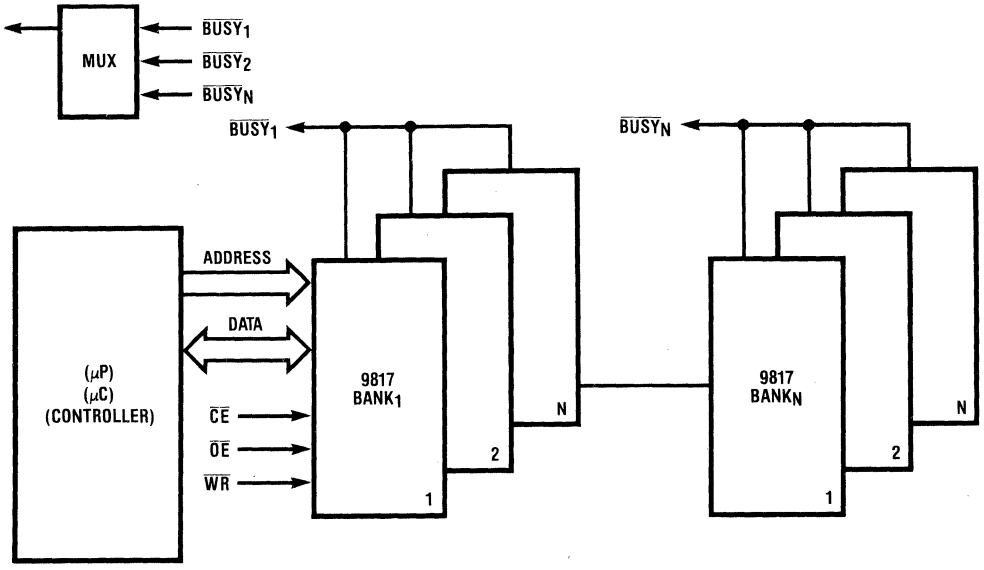


FIGURE 5. A Typical NMC9817 System

Section 3

Reliability Information

THE A+ RELIABILITY ENHANCEMENT PROGRAM

The quality and reliability of National Semiconductor's products have always stood among the best in the business.

But as the complexity of semiconductor devices increased over the years, many of our customers—especially those whose products were highly sensitive to warranty and repair considerations—began asking us for the benefits associated with additional processing.

So we set out to develop ways to provide the extra measure of quality and reliability needed for high-stress or difficult-to-service applications; to make these enhanced products available on an immediate-delivery basis; and to do it all for a cost low enough that our customers could remain competitive in their own markets.

This led to the A+ product reliability enhancement program which incorporates lot stress screening and testing beyond that which standard product receives.

HERE'S HOW WE DO IT

Quality—the measure of a component's conformance to specification—and reliability—the measure of the component's performance over time—both depend upon the tight control of materials; on precision design and fabrication techniques; and on the perfection of a component's assembly and packaging.

But quality and reliability also depend upon the kind of thorough testing that we do at National Semiconductor.

Using state-of-the-art, automated test equipment and handling methods, we test each and every A+ device under the most extreme conditions in which it might be used. We monitor test results, and feed those results to our special failure-analysis laboratory. And we do it all for only pennies a unit.

WEIGH THE ADVANTAGES

Our A+ program allows you:

- To minimize the need for incoming electrical inspection.
- To eliminate the need for (and cost of) using an independent testing laboratory and purchasing excess inventory to cover expected yield loss.
- A reduction in infant mortality rate.
- A reduction in the cost of reworking boards.
- A reduction in warranty and service costs.

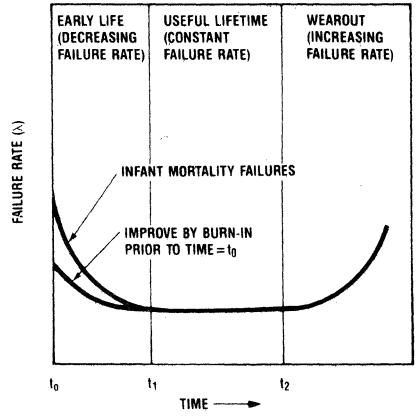
ABOUT A+ PRODUCT ENHANCEMENT

If your business is driven by the need to minimize electrical inspection, to cut down on board rework, and to gain a further reduction in infant mortality rate, National's A+ Product Enhancement is the program you should consider.

A+ incorporates the benefits of the multiple-pass and elevated temperature testing found in the B+ Program, along with an additional test—a combination of increased temperature and applied voltage known as "burn-in"—that in just hours can stress a device to the equivalent of years of normal operation.

The A+ Program gives you:

- High-temperature electrical testing at or above the commercial ambient limit.
- 100% multiple-pass electrical testing.
- A "burn-in" test combining increased temperature with applied voltage.
- Acceptable Quality Levels many times more stringent than the industry norm.



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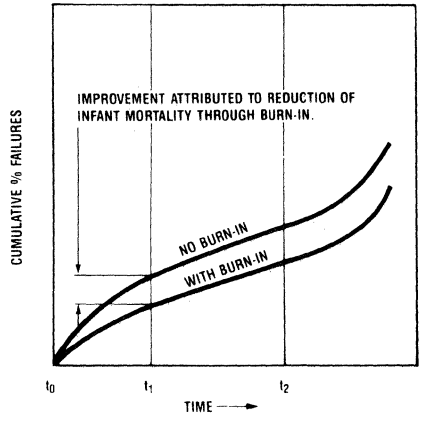

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Component Burn-In Featured In the A+ Program, Reduced Infant Mortality Failures and Total Component Failures Over the Life of Your Products.

THE A+ FLOW

- SEM: Randomly selected wafers are regularly taken from production and subjected to SEM analysis.
- Assembly and seal: All assembly processes are designed and monitored to produce products of the highest quality and reliability. Molded semiconductors are encapsulated with expoxy B.
- Six hour, 150°C bake. This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, eliminating marginal bonds and insuring an optimum plastic seal.
- Five temperature cycles (0°C to 100°C) based on Mil-STD-88 method 1011, condition A, exercising each device over a 100°C temperature range provides an additional die and package stress.
- Electrical test: Each device is electrically tested prior to submission to burn-in.
- Burn-In: Each device is burned-in for the equivalent of 160 hours at +125°C. The combination of elevated temperature and applied voltages places the die and package under severe stress.
- DC parametric and functional tests: These room temperature and high temperature functional parametric tests are the comprehensive final test through which all parts pass and are designed to guarantee compliance to data sheet parameters and functionality over the specified operating range.
- Tightened quality control inspection plans: Each lot is guaranteed to meet the AQL's listed in the following table:

Product Availability

The following MOS Memory Parts are currently available with A+ screening:

NMC9306	256-Bit EEPROM
NMC9307	256-Bit EEPROM
NMC9346	1024-Bit EEPROM
NMC9802	2K EEPROM
NMC9816A	16K EEPROM
NMC9817A	16K EEPROM

At National Semiconductor we turn out more than six million semicondutor products every day, and we build each one to standards that have been called the best in the business.

But if your business requires the benefits associated with additional processing, take a look at the A+ Product Enhancement Program from National Semiconductor.

You'll find a combination of state-of-the-art processing, manufacturing and testing facilities combined with quality and reliability monitoring that provides you with the broadest base of enhanced semiconductor products available in the market.

CALL US ON IT.

If you would like to know more about how our off-the-shelf product enhancement programs can benefit you, give us a call. We'd be happy to show you, in detail, how our A+ Programs can work for you.

When it comes to the many uses of semiconductor technology, National Semiconductor is making the most of a good thing.

Reliability Qualification Procedure for all EEPROM Products

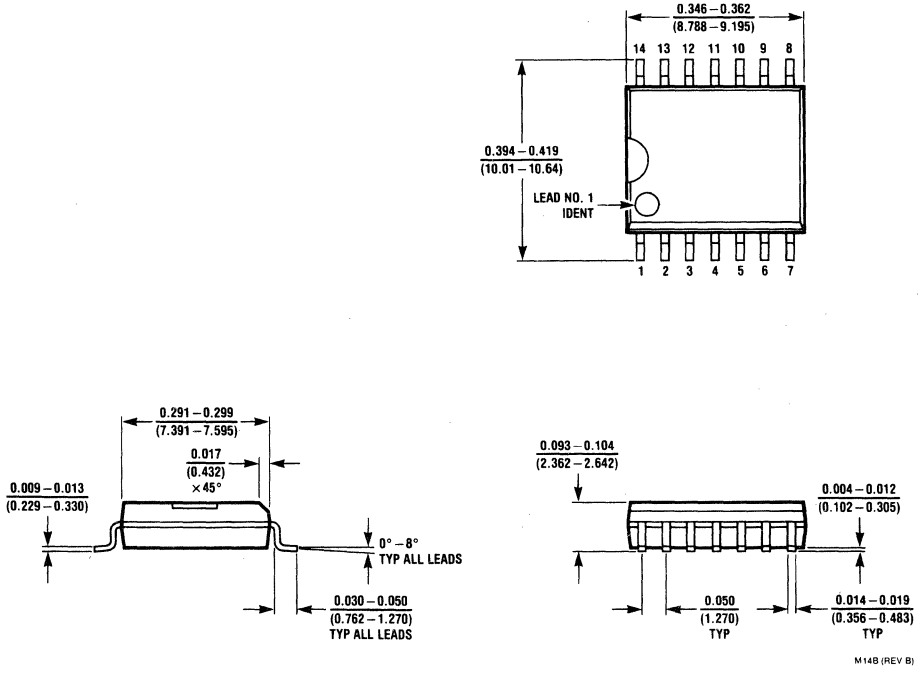
	Test	Sample	Allowed Fail
J Pkg.	Operating Life 125°C 1000 Hrs.	4x105 (1 All 0 1 All 1 2 CHKBD	2/Lot (5% AOQL) (*0.78 LTPD)
	Dynamic B-I at 5.5. All inputs exercised. (Read, Disable, Read, Disable . . .)		
N Pkg.	1.) Operating Life 125°C 1008 Hrs.	Sample 4x158 1 All 0 1 All 1 2 CHKBD	4/Lot 5% AOQL (1.3 LTPD)
	2.) 85/85 1008 Hrs.	4x158 1 All 0 1 All 1 2 CHKBD	4 Lot 5% AOQL (1.3 LTPD)
	3.) Autoclave 168 Hrs. (No Bias)	4x158 1 All 0 1 all 1 2 CHKBD	4 Lot 5% AOQL (1.3 LTPD)
	4.) Biased Pressure Cooker 96 Hrs. (Static B-I)	4x158 1 All 0 1 All 1 2 CHKBD	4 Lot 5% AOQL (1.3 LTPD)

Section 4

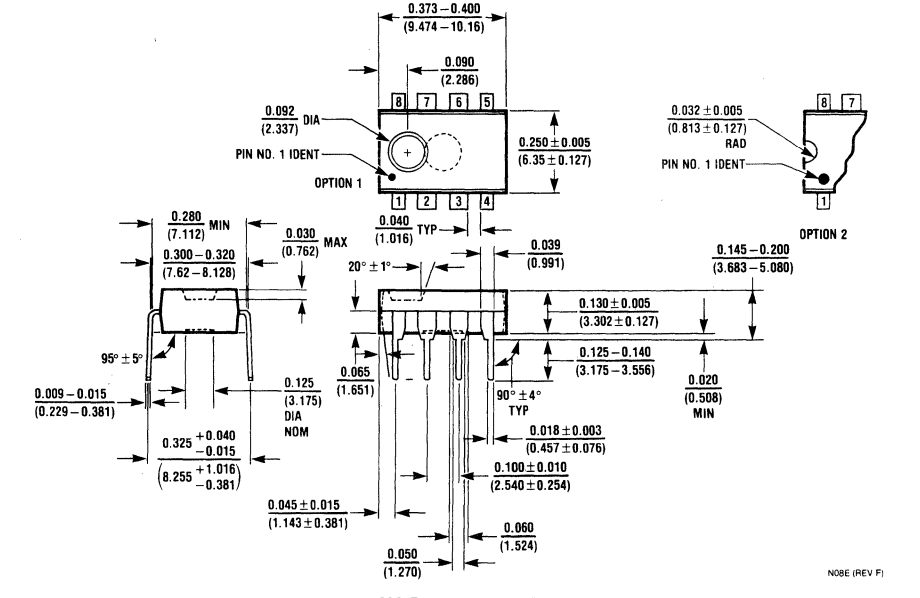
Physical Dimensions

National Semiconductor

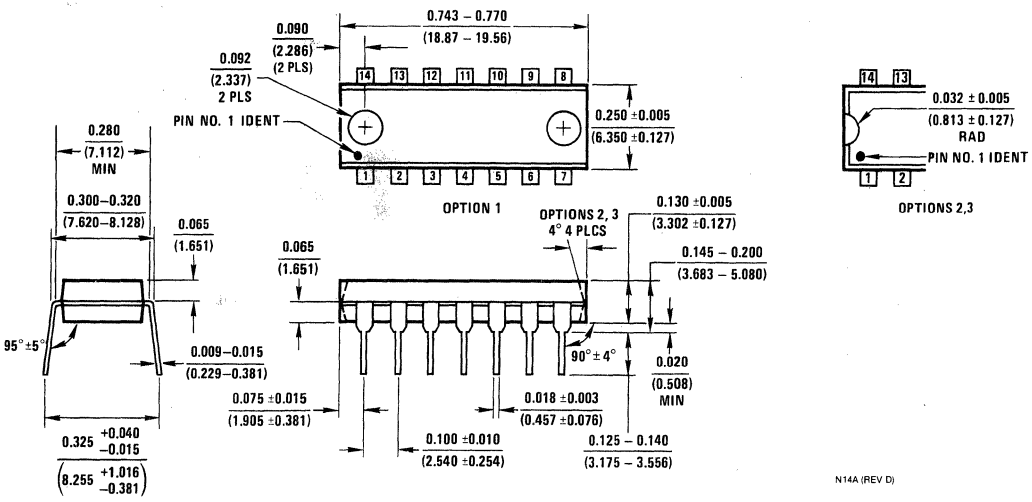
All dimensions are in inches (millimeters)



NS Package M14B



NS Package N08E



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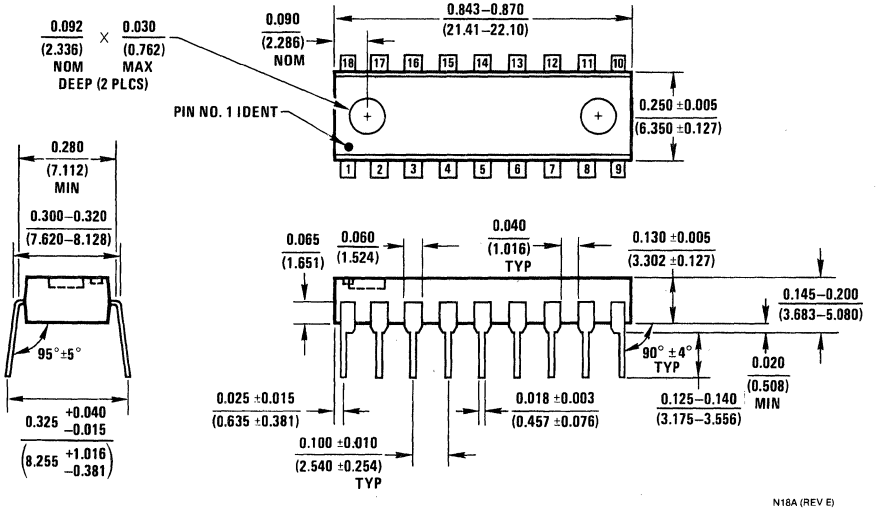

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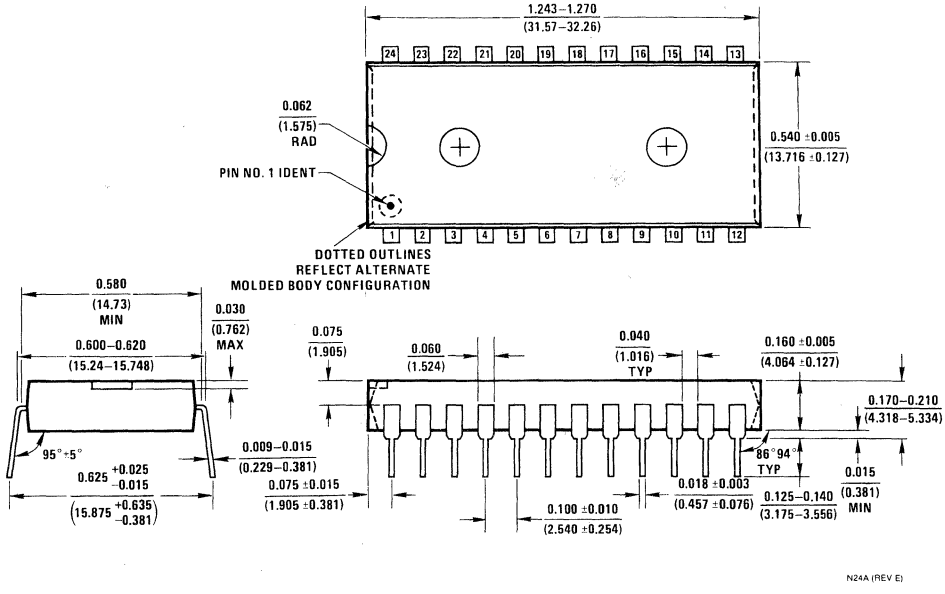
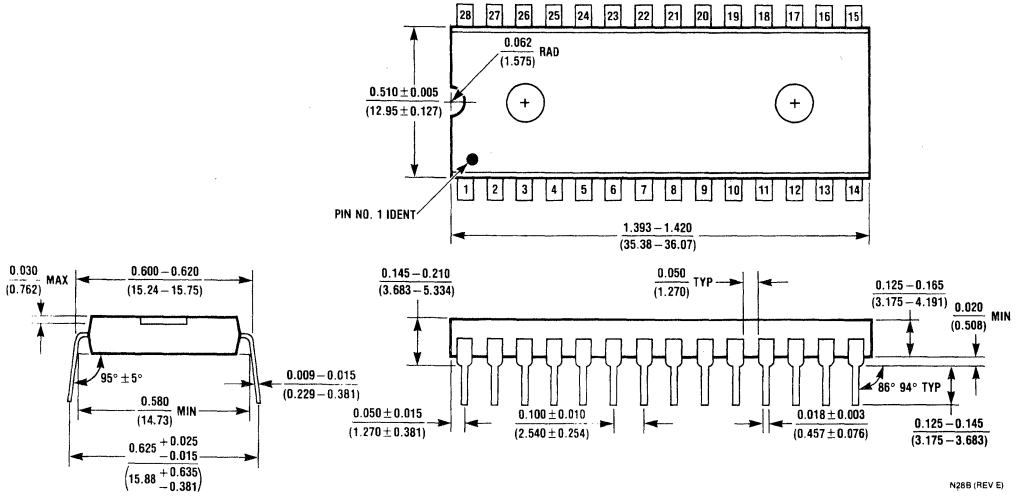


NS Package N24A



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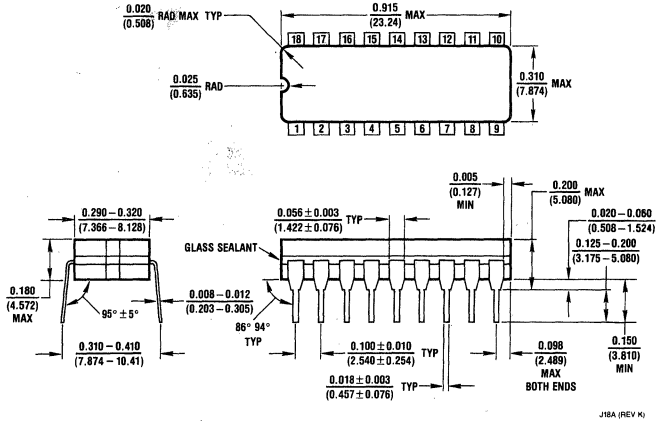
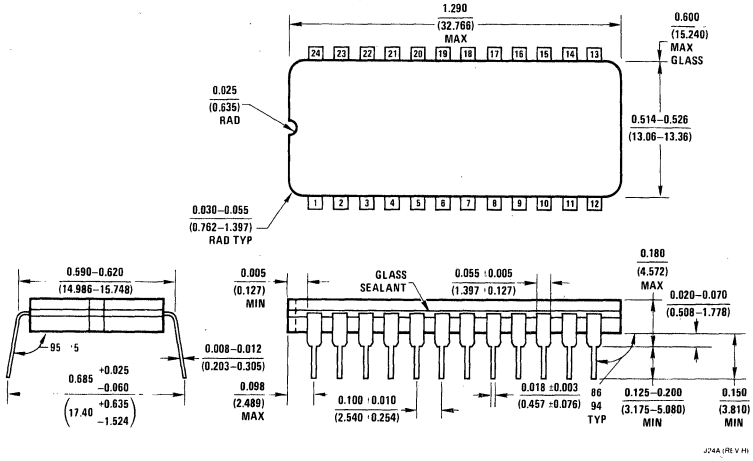


NS Package J18A



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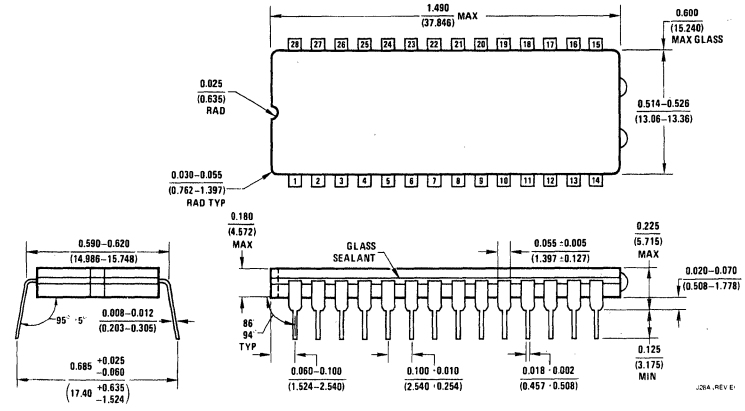

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