Using the COP8ACC with Integration “A/D” Application Considerations

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INTRODUCTION

The COP8ACC is a member of National’s COP888 feature family of 8-bit CMOS microcontrollers. This device is dedicated for all those applications requiring multi channel, higher resolution A/D conversion in small packages. In fact it contains an analog function block with an input multiplexer enabling the user to scan four inputs in the 20-pin version (available in the WM-package), and six inputs in the 28-pin versions (available in the WM- and DIP packages).

Besides the analog function block, featuring fast integration type A/D conversion techniques, the COP8ACC contains other useful features as shown in *Figure 1* below.

With the help of the 16-bit free running “T0” timer the user can generate a time base in programmable steps of 4k, 8k, 16k, 32k or 64k instruction cycle clocks. Placing the microcontroller in idle mode using software, wakeup from “idling” occurs after the specified internal clock cycles have passed. The current consumption of the microcontroller is about ⅓ of the normal I_{DD} current at higher frequencies (CKI > 4 MHz) in this mode. There is an interrupt source available which allows convenient handling of a time base counting function established with help of T0.

The MICROWIRE/PLUS™ serial interface, inherent in all COP888 feature family devices, allows you to program the shift-polarity of the serial clock and also has an interrupt source assigned to it. A 16-bit timer associated with 2 autoreload/capture registers and 2 dedicated h/w pins (T1A and G2) can be configured for true PWM, external event counting or time/frequency measurements. Interrupt conditions can be set for timer underflow, autoreload, or capture events (with programmable transition). The D-port pins have high current sink capabilities allowing to direct drive regular LED’s (min. 15 mA).

Additionally, a WATCHDOG™/clock monitor block, Software Trap interrupt, high ESD immunity, and quite design techniques (low radiated noise) support applications demanding high safety standards.

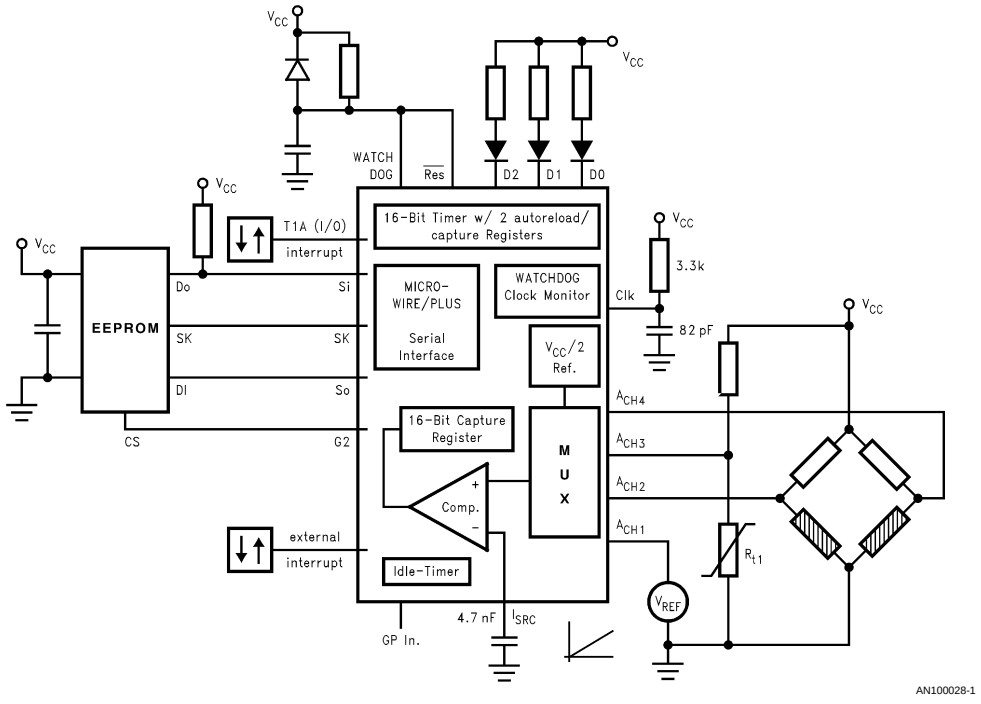

FIGURE 1. Principal Application Scheme of a COP8ACC in a 20-Pin Bondout Version

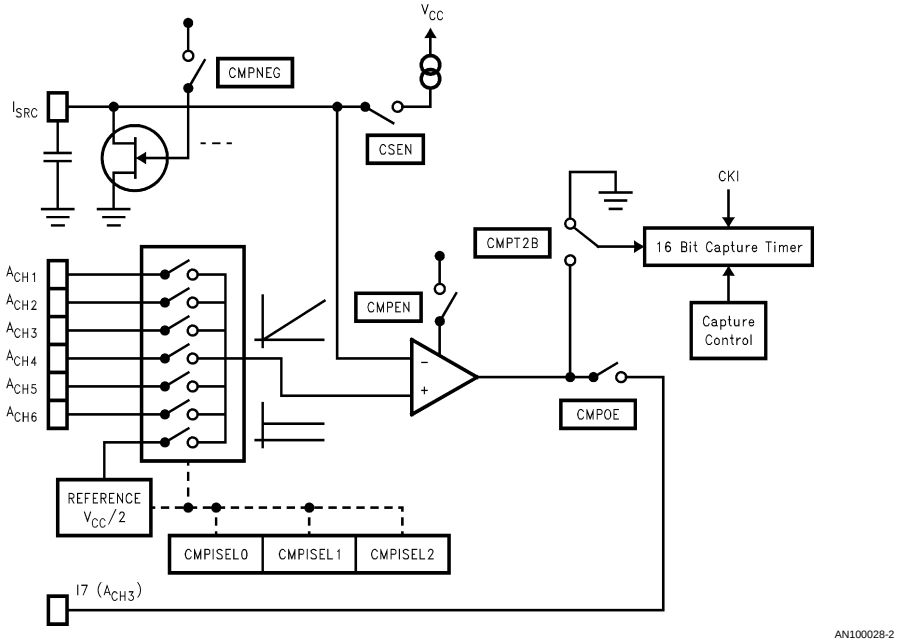

FIGURE 2. Analog Function Block and Control Bits

INTEGRATING A/D CONVERTERS

The principal of an integration type A/D converter is illustrated in *Figure 2*. One of 6 (4) analog inputs is selected and multiplexed onto the positive terminal of an on-chip comparator. With the help of an on-chip constant current source and an external capacitor a linear voltage ramp can be established and fed to the negative terminal of the comparator. When the ramp started the capture timer starts counting up. The user can place a defined start-up value into the capture timer (see initialization example). When the voltage ramp reaches the level of the selected analog input, the output of the comparator changes state and stops the capture timer.

A digital equivalent of the analog level is now available in the capture register and can be saved for later processing.

Comparator Select Register ″CMPSL″ (Address X'00B7)							
CMPT2B	CMPSIEL2	CMPSIEL1	CMPSIEL0	CMPOE	CSEN	CMPEN	CMPNEG
Bit 7							Bit 0

Capture Control Register ″CAPCNTL″ (Address X'00CE)							
unused	unused	unused	CAPMOD	CAPRUN	CAPOVL	CAPPND	CAPIEN
Bit 7							Bit 0

FIGURE 3. Analog Function Block Control Registers, Bits and Mapping

The digital value of the conversion is equal to the number of external CKI clock cycles passing from the time on, when the ramp was started, until the capture timer was stopped from the comparators output. In order to calculate the conversion time, multiply the amount of clock cycles with the external clock cycle time. Assuming a CKI clock of 4 MHz and a maximum resolution of 12 bits, the time elapsing during the conversion is equal to 250 ns x 4096 = 1.0 ms.

An 8-bit conversion at a CKI clock of 10 MHz however, can be executed as fast as 26 µs. So, it has to be carefully analyzed and evaluated if A/D conversion **and** data processing can create timing problems in the application. The setup for the analog function block has to be defined accordingly. The following considerations may help the user to find the right compromise.

INITIALIZING THE ANALOG FUNCTION BLOCK

A proper initialization of the analog function block is essential to gather good conversion results. Secondly, there are different control bits out of 2 control registers to be respected. Therefore, this important task is discussed in more detail below.

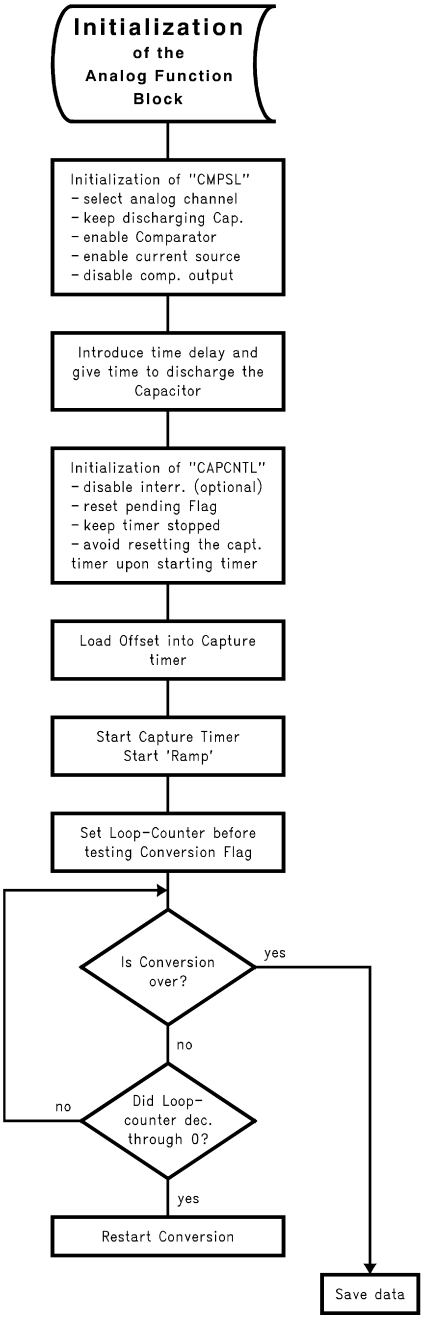

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FIGURE 4. "Flowchart" A/D Conversion Initialization

The assembler code following the steps defined in the below flowchart will look as follows:

```
; Initialization of A/D (Subroutine)
ATOD:
     LD CMPSL,#097       ; b# 1001 0111
                         ; -pin I_SRC will be held
                         ; low (discharge Cap.)
                         ; -Ch. ACH2 is select.
                         ; -Comparator = enabled
                         ; -Current src = enabled
                         ; -Comp.out = disabled

     LD 0F0,#10          ; Init loop counter
Delay:
     DRSZ 0F0            ; Ensure capacitor
     JP Delay            ; completely discharged

     LD CAPCNTL,#010     ; b# 0001 0000
                         ; -Disable Capture int.
                         ; -Reset pending flag
                         ; -keep timer stopped
                         ; -Reset CAPOVL
                         ; -Avoid Capture timer
                         ; to be set to zero
                         ; when starting timer.
     LD B,#CMPSL         ; B-Pointer points to
                         ; Comp. select register

     LD CAPTLO,#010      ; Place correction off-
     LD CAPTHI,#000      ; set into capture Reg.
                         ; (see (Note 1) below)
     SBIT CAPRUN,CAPCNTL ; Start Capture Timer
     RBIT CMPNEG,[B]     ; Start “Ramp”

     LD 0F0,#0FF         ; Init special loop
     LD 0F1,#0FF         ; counter.

ATODLOOP:

     IFBIT CAPPND,CAPCNTL; Test pending flag to
                         ; see if convers. done.
     JP DONE

     DRSZ 0F0
     JP ATODLOOP
     DRSZ 0F1
     JP ATODLOOP
     JMP FAIL

DONE:

     RBIT CMPEN,[B]      ;Disable comparator
     RET

FAIL:

     JMP RESTART         ; a failure occured
                         ; reinitialize and try
                         ; again.
```

Note 1: The actual offset phase is a count of 30 “ticks”, because the capture timer contents is already 30 at the time the “ramp” is released. This offset is depending on the capacitor value and the CKI clock speed and is tailored to the setup shown in *Figure 1*. This offset is only critical if absolute accuracy is required.

A special loop counter will be decremented while checking the capture timer pending flag. If this flag is set before the loop counter “runs out”, the conversion was successful and the data can be further processed. If the loop counter runs out and the pending flag was not set, then a problem has occurred. This can happen if the level at the analog input is too low or too high. Therefore, it is recommended to establish a similar kind of precaution at this place in the source code. Please refer also to *Figures 2, 3* for better understanding of the A/D initialization.

DISCUSSION OF AN IMPLEMENTATION EXAMPLE

Figure 5 is an implementation example. The software scans sequentially the voltage reference and channels A_{CH2} and A_{CH3}. The voltage ramps are being built across the capacitor at pin I_{SRC} by enabling the constant current source of the analog function block (see also *Figures 1, 4*).

The voltage across the capacitor can be described with the following equation:

$$Uchx(t) = \frac{1}{C} \cdot \int_{ta}^{tb} i(t)dt$$

Time ***ta*** represents the start of the integration (the capacitor is fully discharged) and time ***tb*** the end of the integration (the voltage level at the capacitor is equal to the voltage across the analog input).

Since the current delivered from the current source is constant the solution of above the integral becomes:

$$UCHx = \frac{1}{C} \cdot I \cdot (tb - ta)$$

In practice, the term (tb-ta) will be represented by a "count" proportional to the voltage level at the measured analog input U_{CHx}.

It is recommended to also measure the reference input in each measurement cycle to compensate possible inaccuracies introduced from noise, drifting RC-clock ... etc. Secondly, the measurements on each input should be executed at least twice and compared to each other. If the digital results of 2 subsequent conversions on a particular input have a close enough match (plus or minus 1 count), the results are valid for further processing. Otherwise, the measurements should be repeated.

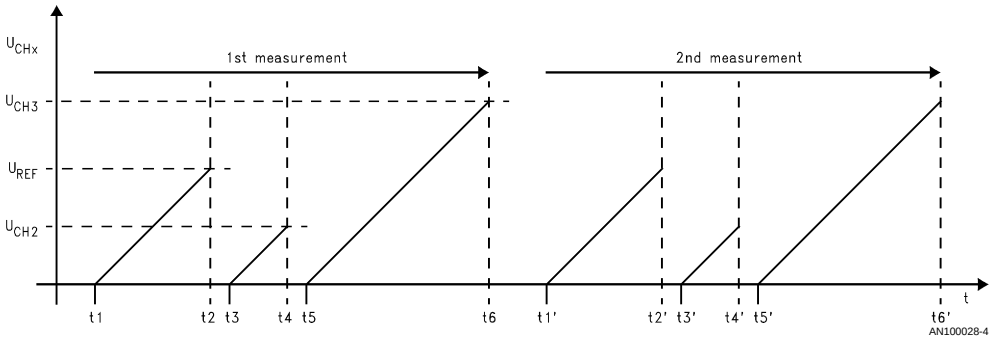


FIGURE 5. Timing Diagram "Conversion Time in Relation to Input Voltage Levels"

RESOLUTION AND ACCURACY

Careful attention should be paid to the application needs in terms of resolution and accuracy of the A/D converter. The linearity of the "ramp" is mainly dependant on the current source and to a lesser extent on the quality of the capacitor. In addition, the common mode range of the comparator limits the usable input range of the analog inputs. It is recommended to limit the input voltage range from about 200 mV minimum to about 0.6 x V_{CC}. If the absolute voltage range of an input exceeds this boundary, an attenuation network (voltage divider in simple cases) is required.

If the maximum possible input range of 2.5V is being used, a good choice for the minimum resolution is 10 bits (this yields a typical resolution of 11 bits). In many cases, there is a smaller input span from minimum to maximum possible voltage at a particular analog input. Linear temperature sensors yield output voltage in a span of about 600 mV. This is also true for other sensors like strain gauge bridges, pressure transducers ... etc. Therefore, any attempts to establish higher resolution should be made dependant on the input voltage range.

Table 1 is intended to assist the user in making a proper choice regarding the resolution of the A/D.

TABLE 1. Input Voltage Range and Recommended Resolution

Input Voltage Range/V	Min Resolution Over Full Range	Achievable Accuracy
2.5	10 Bits	+2.5 LSB
2.0	11 Bits	+3.0 LSB
1.5	12 Bits	
1.0	13 Bits	
0.5	14 Bits	

The resolution is thereby always referring to an input voltage range of 2.5V. Achievable accuracy depends on various hardware and software conditions, and therefore is intentionally left open for the last 3 cases.

Table 2 gives a quick overview on different cases showing the relations between CKI-clock frequency, the capacitor at I_{SRC}, and the conversion times over the maximum input voltage range (typical as well as minimum resolution). The input voltage range is always assumed to be 2.5V.

TABLE 2. Resolution in Dependance of the CKI-Clock and Capacitor at I_{SRC}

Capacitor Value	CKI-Clock/MHZ	Min.-Resolution/ Capt. Timer Counts	Conversion Time at Min. Resolution	Typ-Resolution/ Capt. Timer Counts	Conversion Time at Typ Resolution
4.7 nF	4 MHz	1343 (10 to 11 Bits)	336 µs	2611 (11 to 12 Bits)	652 µs
3.3 nF	10 MHz	2357 (11 to 12 Bits)	236 µs	4583 (12 to 13 Bits)	458 µs
6.8 nF	10 MHz	4857 (12 to 13 Bits)	486 µs	9444 (12 to 13 Bits)	945 µs
2.2 nF	2 MHz	314 (8 to 9 Bits)	1.57 ms	611 (9 to 10 Bits)	3.1 ms
6.8 nF	1 MHz	486 (> 9 Bits)	486 µs	944 (~10 Bits)	944 µs
15 nF	8 MHz	8571 (13 to 14 Bits)	1.07 ms	16667 (14 to 15 Bits)	2.08 ms

LIMITATIONS

The current delivered from the constant current source has theoretically a spread from 7 µA to 35 µA.

Calculating the resolution (counts of the capture timer) can be done with the following equation:

$$\text{CaptureTimerValue} = \frac{C \cdot dV}{Imax \cdot tclk}$$

with:

C = Value of Capacitance

dV = Analog Input volt. range

I_{max} = maximum current delivered from current source

t_{CLK} = External oscillator clock cycle

Regarding the setup given in *Figure 1* the minimum Capture Timer Value resulting from the above equation would be about 1220 counts (taking C=4n7, dV=3V, I_{max}=35 µA and t_{CLK}=0.33 µs). The typical resolution for this case would be about 2374 counts taking I=18 µA instead of 35 µA.

An RC-clock with 82 pF and 3.3k resistor establishes a CKI clock of about 3 MHz at the COP8ACC controller.

CONVERSION TIME AND DATA PROCESSING

The conversion time is calculated by multiplying the amount of "counts" with the CKI clock cycle time. For the typical case in the above example we would find a conversion time of 2374 x 0.33 µs = 783 µs.

It was suggested to measure each channel twice in conjunction with the reference input. A complete conversion cycle on one channel including the scanning of the reference input would, therefore, take about 4 x 783 µs = 3.12 ms plus 50 to hundred instruction cycles needed to initialize the conversions and saving the data. In addition, to that there may be a considerable time spent on evaluating and processing the data. Usually the software will have to execute divisions (24/16), multiplications (16x16 and higher) HEX to BCD conversions, and other time consuming tasks in the "Data Processing Phase" of the program. When critical system timings have to be respected it is essential to do a worst case calculation, a thorough evaluation of the time needed for A/D conversion, and the processing of the data afterwards.

VOLTAGE REFERENCE FOR THE A/D

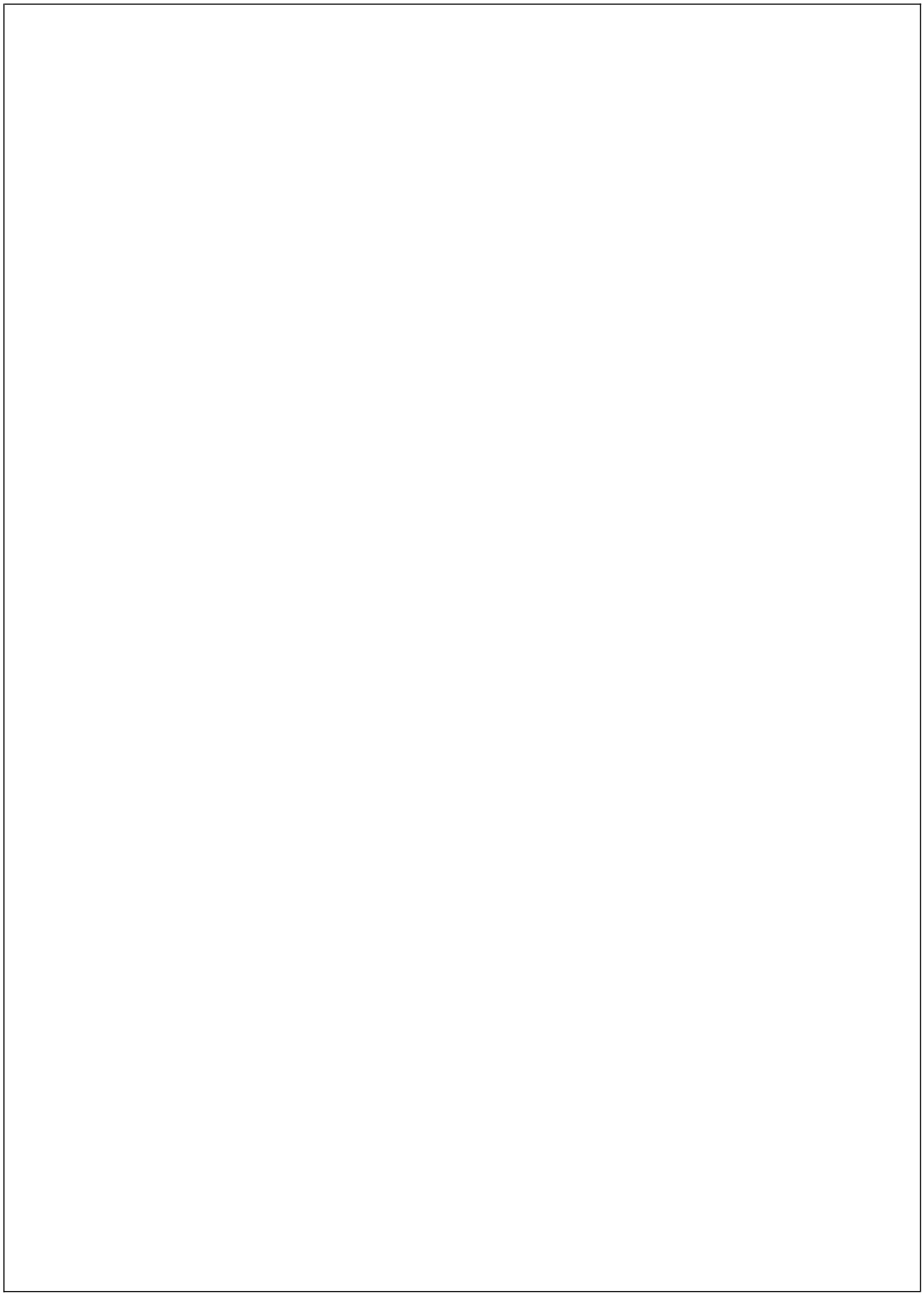
The COP8ACC has an internal V_{CC}/2 reference which can be scanned in the same way as the external analog inputs by appropriately setting the select bits. The use of this reference is depending on the required accuracy. This reference deviates at a maximum of ±40 mV from the ideal V_{CC}/2 voltage. If higher accuracy is required, an external reference has to be established on one of the analog inputs. Another convenient way to install a good reference would be to feed an accurate voltage into one of the analog channels during the production phase and store the counts of the reference measurement in an external EEPROM (see *Figure 1*). In this case, it is either necessary to use a crystal clock instead of an RC-clock or include the internal V_{CC}/2 into the measurements to compensate drifting of the RC clock.

CONCLUSION

The COP8ACC is ideally suited for all kinds of controller tasks demanding higher resolution A/D, such as the scanning of linear temperature sensors, strain gauges, and various types of other sensors.

Due to the nature of the serial A/D approach, the conversion time of an A/D cycle is typically in the lower msec range (please refer to *Table 2*).

In addition to the analog function block, the COP8ACC provides a set of other useful features demonstrating its versatility and applicability for a wide variety of applications.



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